CS577 Project Outline

This project involves high-level synthesis (HLS) of machine learning models for implementation on FPGAs. Each group will be assigned a model from a pool of 20 models, and the objective is to convert the model to C using Keras2C perform HLS using Vivado HLS, and compare results with the results obtained through HLS4ml.

1 Model Assignment

Groups will be assigned models from a Google Sheets document:
https://docs.google.com/spreadsheets/d/181_nmCKM2Kb2DjPuQMKNLxHpdLuRF7KecYZfMSeWdWM/edit?usp=sharing

2 Tools and Setup

Groups must install

Keras2C : Generates C from the Keras model (https://github.com/f0uriest/keras2c)

Vivado HLS : Used to perform HLS (http://jatinga.iitg.ernet.in/download/).

License info: `XILINXD_LICENSE_FILE=2103@172.16.112.7`

Note : Every group must install Vivado from above link. No other versions are encouraged.

HLS4ML : (https://fastmachinelearning.org/hls4ml/)

3 Execution and Conversion

Each group will run assigned models with Keras2C to generate C files. These files will then be synthesized with Vivado HLS. Results has to be compared with the ones generated using HLS4ml.

4 Optimization and Analysis

Optimization pragmas will be applied to the C files to improve performance. A detailed report on synthesis parameters such as latency and resource utilization has to be be prepared.

5 Conclusion

This project aims to explore HLS techniques for ML models and assess their performance on FPGA platforms.