Національний університет "Львівська політехніка"
Кафедра електронних обчислювальних машин (ЕОМ)

Автоматизоване проектування комп'ютерних та кіберфізичних систем

спеціальність 123 “Комп’ютерна інженерія”
спеціалізація 123.04 “Кіберфізичні системи”
4-ий курс

Лекція 5. Високорівневі засоби системного проектування (3)

2021

01.1. Системна шина AMBA.

AMBA specification (First version) defines two buses/interfaces:

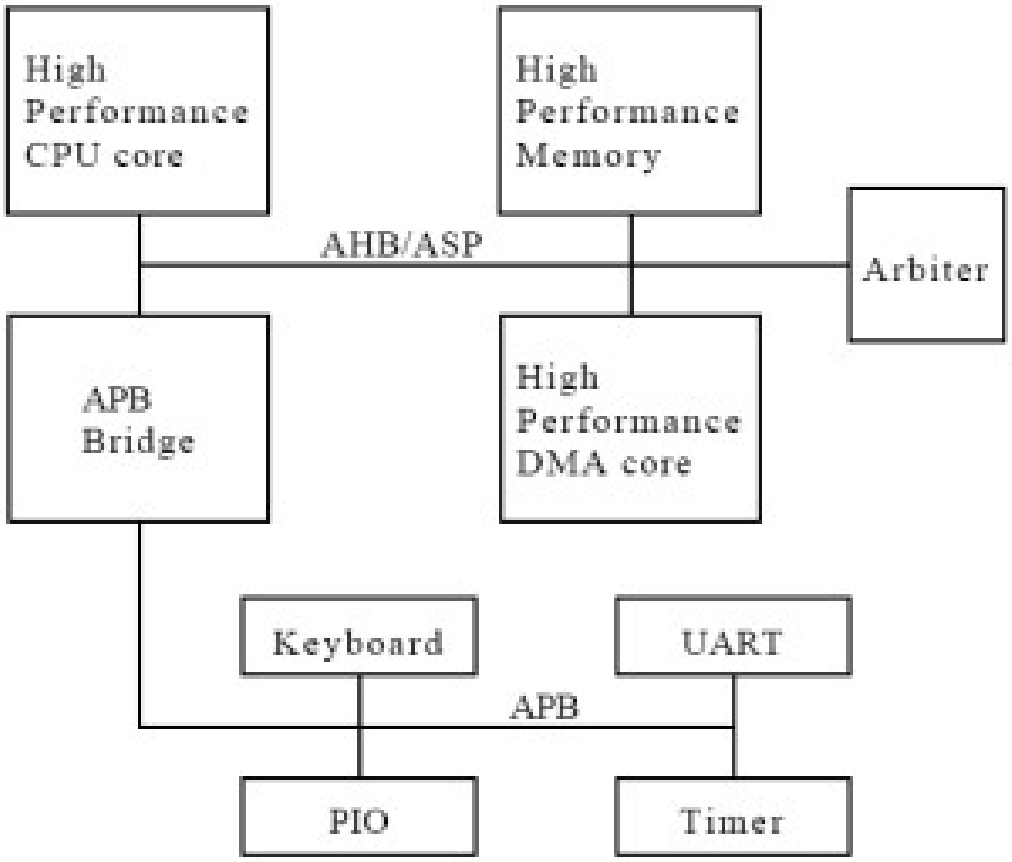
- *Advanced System Bus (ASB)*
- *Advanced Peripheral Bus (APB)*

AMBA 2 specification defines three buses/interfaces:

- *Advanced High-performance Bus (AHB) - widely used on ARM7, ARM9 and ARM Cortex-M based designs*
- *Advanced System Bus (ASB)*
- *Advanced Peripheral Bus (APB2 or APB)*

01.2. Системна шина AMBA.

Logical Bus Structure

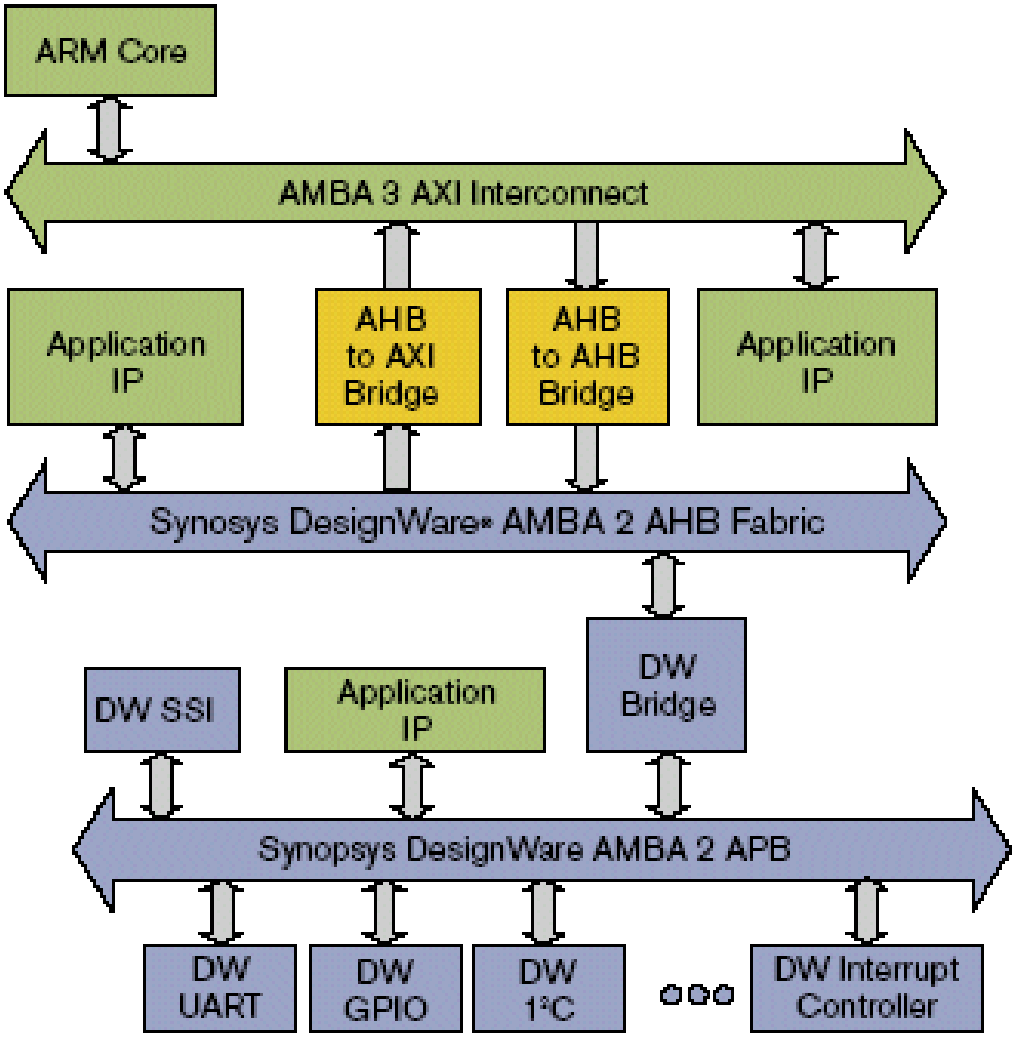


01.3. Системна шина AMBA.

AMBA 3 specification defines four buses/interfaces:

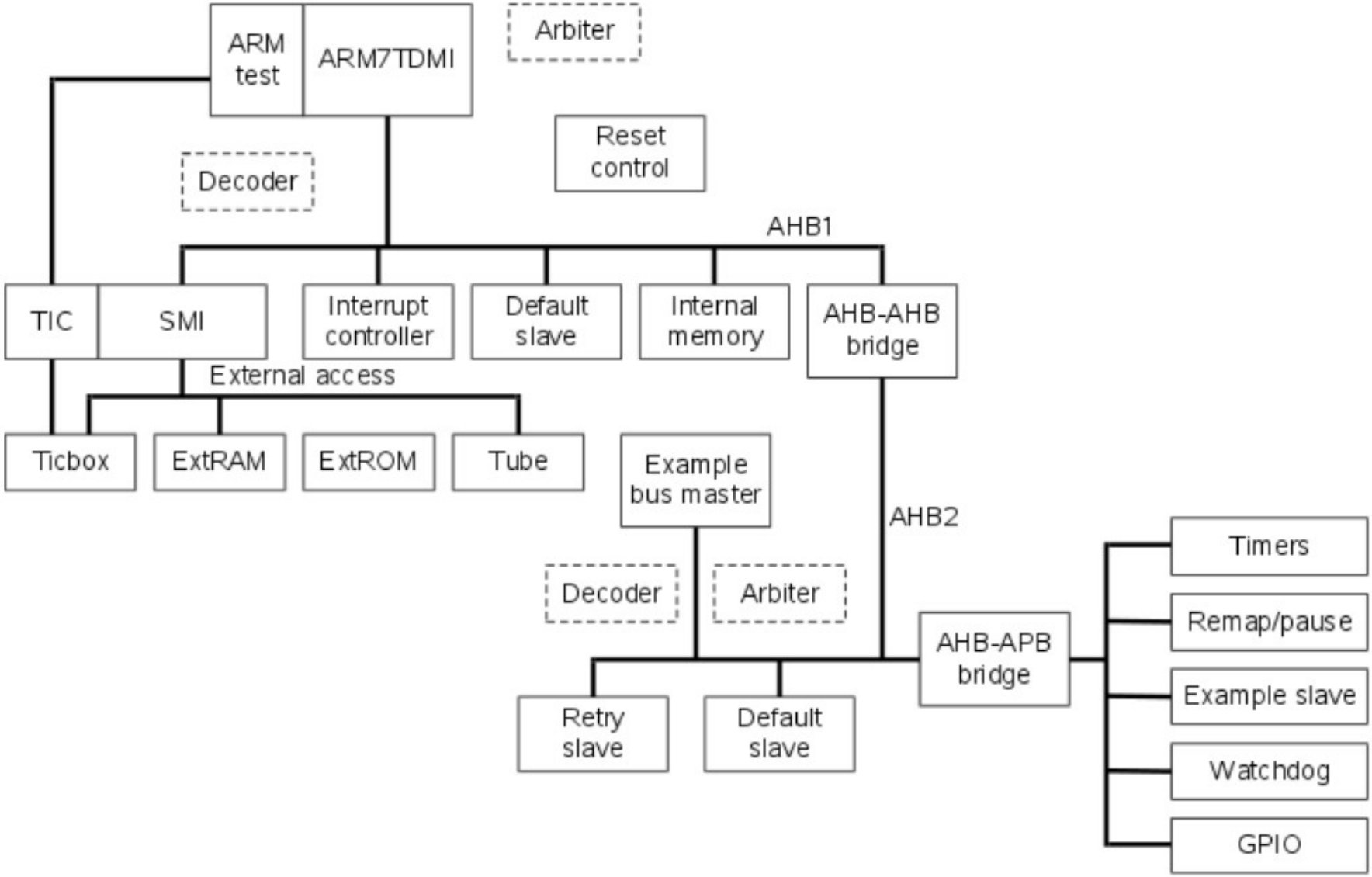
- *Advanced eXtensible Interface (AXI3 or AXI v1.0) - widely used on ARM Cortex-A processors including Cortex-A9*
- *Advanced High-performance Bus Lite (AHB-Lite v1.0)*
- *Advanced Peripheral Bus (APB3 v1.0)*
- *Advanced Trace Bus (ATB v1.0)*

01.4. Системна шина AMBA.



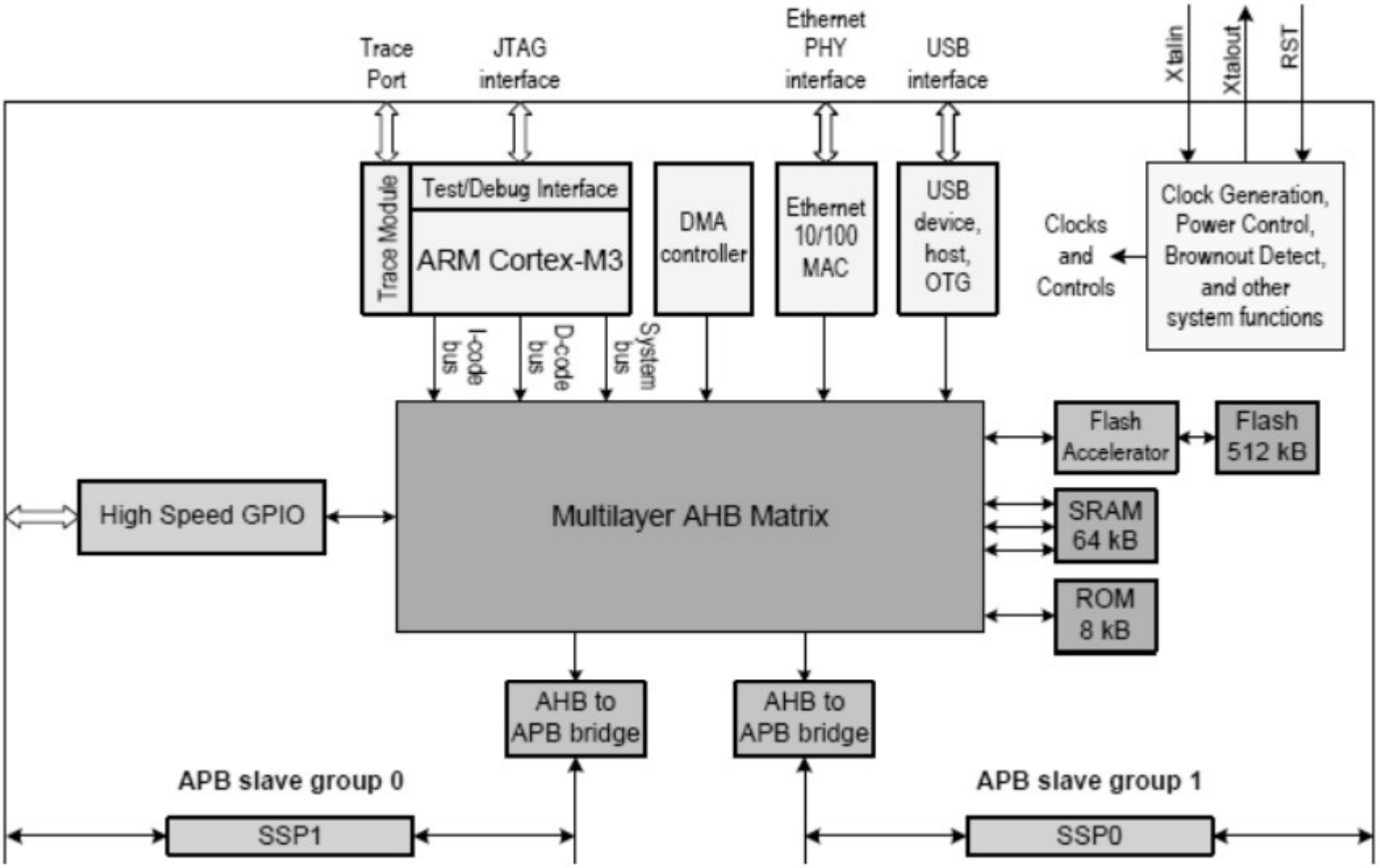
01.5. Системна шина AMBA.

(Застосування AMBA AHB та AMBA APB для ARM7)



01.6. Системна шина AMBA.

(AMBA AHB в мікроконтролері NXP LPC1768 на Cortex-M3)



01.7. Системна шина AMBA.

The AMBA 4 specification defines following buses/interfaces:

- AXI Coherency Extensions (ACE) - widely used on the latest ARM Cortex-A processors including Cortex-A7 and Cortex-A15
- AXI Coherency Extensions Lite (ACE-Lite)
- Advanced Extensible Interface 4 (AXI4)
- Advanced Extensible Interface 4 Lite (AXI4-Lite)
- Advanced Extensible Interface 4 Stream (AXI4-Stream v1.0)
- Advanced Trace Bus (ATB v1.1)
- Advanced Peripheral Bus (APB4 v2.0)
- AMBA Low Power Interfaces (Q-Channel and P-Channel)

01.8. Системна шина AMBA.

The AMBA 5 specification defines the following buses/interfaces:

- AXI5, AXI5-Lite and ACE5 Protocol Specification
- Advanced High-performance Bus (AHB5, AHB-Lite)
- Coherent Hub Interface (CHI)
- Distributed Translation Interface (DTI)
- Generic Flash Bus (GFB)

01.9. Шина ASP(частина шини AMBA).

The ASP is the general purpose system bus. It is a high performance interconnect for micro controller and system peripherals. The main features are:

- *First Generation System Bus*
- *Multiple Masters*
- *Burst Transfers*
- *Pipeline Transfers*
- *32 - 128+ bit bus width*
- *Includes a access protection mechanism, to distinguish between such access as privileged and non privileged modes, instruction and data fetch, etc.*
- *Bidirectional data bus*
- *Address space limited to 32 bits*
- *Throttling of data for slower devices provided*
- *Arbitration support, REQ, GNT and LOCK*
- *Supports transfers of bytes, half-word and word*

01.10. Шина AHB(частина шини AMBA). *(появився в AMBA 2)*

The AHB is the advanced system bus. It's main purpose if for interconnecting high performance, high through put devices, such as CPU, DMA and DSP. It's main features are:

- *High Performance Bus (New Generation Bus)*
- *Multi Master*
- *Split transfers*
- *Single cycle bus master handover*
- *Non tristate implementation*
- *32 - 128+ bit bus width*
- *Includes a access protection mechanism, to distinguish between such access as privileged and non privileged modes, instruction and data fetch, etc.*
- *Bursts limited to 16 'beats' max*
- *Address space limited to 32 bits*
- *Throttling of data for slower devices provided*
- *Arbitration support, REQ, GNT and LOCK*
- *Supports transfers of bytes, half-word and word*

01.11. Шина APB(частина шини AMBA).

The APB is the peripheral interconnect bus. Focus here was minimal power consumption
and ease of use. The main features include:

- *Low performance, low power peripheral bus*
- *Single Master*
- *Very Simple, only 4 control signals (plus clock and reset)*
- *32 bit address space*
- *up to 32 bit data bus*
- *separate read and write data bus*