Mikro MiMo model CPE – krmilni signali v0

PROGRAM Zbirnik	Korak	Address Vir naslova	ReadWrite Vpis/branje RAM pomn.	dwrite Vpis reg. Rd	RegSrc Vhod v reg.	aluop ALU Operac.	ADR Sub Rx,PC,#odm	Irload Vpis v uk. reg. IR	PC
Opis		0..PC, 1..Rn	0..branje, 1..pisanje	0..ne, 1..da	0..Databus, 1..ALU, 2..Immediate	0..ADD, 2..SUB	0..ne, 1..da	0..ne, 1..da	Naslov ukaza
adr r0,STEV1	(PC+4) Fetch							1	0x2C
(sub r0,pc,#0x0c)	Execute			1	1	2	1		
ldr r1,[r0]	(PC+4) Fetch							1	0x30
	Execute	1		1	0				
adr r0,STEV2	(PC+4) Fetch							1	0x34
(sub r0,pc,#0x10)	Execute			1	1	2	1		
ldr r2,[r0]	(PC+4) Fetch							1	0x38
	Execute	1		1	0				
add r3,r1,r2	(PC+4) Fetch							1	0x3C
	Execute			1	1	0			
adr r0,REZ	(PC+4) Fetch							1	0x40
(sub r0,pc,#0x18)	Execute			1	1	2	1		
str r3,[r0]	(PC+4) Fetch							1	0x44
	Execute	1	1						

Mikro MiMo - Simple CPU Model

v0 EVO

Reset [ ] — ⟨reset⟩   **SysClk** ⟨CLK⟩

PC

pc

0 / 16 / 32 extend   pc32

002c   002c   UUUU / 0   002c

Rn   15-0

addrsel

Address BUS

0 0 2 C

address

CPU Info

PC	Address	Data	Instruction:					
pc	address	data	InstrTyp	opcode	Rdsel	Rnsel	Rmsel	ImmVal
002c	002c	e24f000c	1	2	0	15	12	0000000c
				Rd	Rn	Rm	immed	

0 — Phase
🔴 ⚫
Fetch Execute

0 — ReadWrite
🔴 ⚫
Read Write

IR

reset
e24f000c
irload
CLK   1 | 2 | 1   0 | 15 | 12   ImmVal

InstrTyp opcode Itype Rdsel Rnsel Rmsel

RAM

A

RAM 64K x 32

0022	00000000 00000000
0024	00000010 00000000
0026	00000000 00000000
0028	00000000 00000000
002a	00000000 00000000
002c	e24f000c 00000000

WE
OE

CLK

D

Registers

Rd   Rn   Rm

e24f000c / 0

reset
dwrite
CLK
Rdsel   **R0** 00000000
Rnsel   **R1** 00000000
Rmsel   **R2** 00000000
        R3 00000000
        00000000

RegSrc

Rd

Data BUS

E 2 4 F 0 0 0 C

data

ALU

aluop   Rn

UUUUUUUU
UUUUUUUU
00000000

0 / 1

pc32

ImmVal

aluout

ADR

🔴 c   🔴 z   🔴 n

Carry Zero Neg

RAMSel

Control BUS

🔴 ⚫
Read Write

ReadWrite

Control Unit - signals

addrsel	ReadWrite	dwrite	RegSrc	aluop	ADR	irload
🟢	🟢	🟢	0 0	0 0	🟢	🟢
0	0	0	0 0	0 0	0	1

Address	**ReadWrite**	**RegWrite**	**RegSrc**	**aluop**	**ADR**	**irload**
0 PC	1 Write	1 Write Rd	0 DBus	0 ADD	1 ADR instr.	1 Write
1 Rn			1 ALU	2 SUB		
			2 IMM			

Fetch (PC+4):   Address=0, ReadWrite=0,   RegSrc=0;   irload=1

Pseudo instr. ADR R0,Address -> SUB R0, PC, #imm

Exec ADR: RegWrite=1, RegSrc=1, aluop=2,ADR=1

Exec LDR: Address=1,   RegWrite=1, RegSrc=0

Exec ADD: RegWrite=1, RegSrc=1, aluop=0

Exec STR: Address=1, ReadWrite=1

Control Unit: How to Fetch and Execute