

Quiz 1 and 2

Answer all questions. Each question carries 1 mark

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Points:

13/20

1.It is impossible to mask interrupt(s) in 8085

(1/1 Point)

☐

22

☐

55

☐

11

☐

33

2.If HL=3040H, SP=2700H, (2700H)=50H and (2701H)=60H. What will be the contents of 2701H after the execution of XTHL instruction?

(1/1 Point)

☐

50

☐

40

☐

30

☐

60

3.Which of the following is not applicable in 8085?

(1/1 Point)

☐

Register addressing mode

☐

Immediate addressing mode

☐

Indirect addressing mode

☐

Relative addressing mode

☐

None of the above addressing modes

4.Which of the following is not true regarding 8085?

(1/1 Point)

☐

It has 8-bit accumulator

- ☐ It has 16 address lines
- ☐ It doesn't support serial communication
- ☐ It uses address latch enable

5. In 8085, CMP D instruction

(1/1 Point)

- ☐ compares accumulator with register D
- ☐ complements contents of D register
- ☐ This instruction is incomplete
- ☐ compares the contents of D register and E register

6.If the flag register of 8085 has 11X0X1X0, then execution of STC instruction makes the flag register as

(1/1 Point)

- ☐ 11X0X0X0
- ☐ 11X0X1X1
- ☐ 1100X1X0
- ☐ 10X0X1X0

7.If accumulator of 8085 has B3H, ORI 07H makes the accumulator contents as

(1/1 Point)

- ☐ B8H
- ☐ B7H
- ☐ C6H
- ☐ CCH

8.LDA 2050H is an example for

(1/1 Point)

- ☐ Immediate addressing mode
- ☐ Register addressing mode
- ☐ Indirect addressing mode
- ☐ Direct addressing mode

9.XCHG is an example for

(0/1 Point)

- ☐ None of the below addressing modes
- ☐ Immediate addressing mode
- ☐ Indirect addressing mode
- ☐ Register addressing mode

10.If the Accumulator of 8085 has ADH and carry flag=0, What results in accumulator and carry after executing two RAL instructions

(0/1 Point)

- ☐ A=10101101, CY=1
- ☐ A=01011010, CY=1
- ☐ A=10110101, CY=0
- ☐ None of the above

11. Identify the false statement about 8086 microprocessor

(1/1 Point)

- ☐ has fourteen 16-bit registers
- ☐ has 16-bit bi-directional data and 16-bit address bus
- ☐ BIU fetches more than one instruction bytes ahead of time
- ☐ has four segment registers

12. Which of the following is not true regarding flag register of 8086 after performing the addition of 0110010111010001 and 0010001101011001

(1/1 Point)

- ☐ AF=1, OF=1
- ☐ CF=0, PF=1
- ☐ SF=1, ZF=0
- ☐ ZF=0, OF=1

13. If [DF]=0, [DS]=3000H, [SI]=0500H, [ES]=5000H, [DI]=0200H, [30600H]=38H and [50400H]=45H. After execution of MOVSB instruction, [50400H]=38H

(0/1 Point)

- ☐ [SI]=0501H, [DI]=0201H
- ☐ [SI]=0500H and [DI]=0200H
- ☐ [SI]=0502H, [DI]=0202H
- ☐ [SI]=0501H, [DI]=0202H

14. Identify the false statement regarding 8086

(1/1 Point)

- ☐ LDS CX instruction is used for loading CX and DS with words from memory
- ☐ LODSB instruction copies a byte from a string location pointed by SI to AH
- ☐ IN AX, 95H instruction copies a word from port 95H to AX
- ☐ LAHF loads lower byte of flag register in AH

15. In 8086, assume that AL register has 96 BCD, BL register has 07 BCD. After executing ADD AL, BL and DAA instructions, what will be the contents of AL?

(0/1 Point)

- ☐ 3A
- ☐ A3

☐ 02

☐ 03

16. Identify the false statement about 8086

(1/1 Point)

- ☐ The assembler ignores any statement after an END directive
- ☐ PAGE 132,52 assembler directive means 52 lines per page and 132 characters per line
- ☐ To reserve 50 bytes for stack operation, the following directive is used: .STACK 50
- ☐ None of the above are false

17. Identify the false statement about 8051

(1/1 Point)

- ☐ It has bit addressability feature
- ☐ Port 2 pins have more than one function
- ☐ Port 0 pins have more than one function
- ☐ Port 1 pins have more than one function

18. Identify the false statement about 8051

(0/1 Point)

- ☐ Only one register bank (among Bank 0, Bank 1, Bank 2 and Bank 3) can be used at a time.
- ☐ Bank selection can be done using PSW bits
- ☐ DPTR can be accessed as two 8-bit registers
- ☐ loading PSW with #00001000B selects register bank-1

19. In 8051 microcontroller, assume that DPH contains 12H and DPL contains FEH. When INC DPTR instruction is executed twice, the contents of DPH and DPL will become

(0/1 Point)

- ☐ 13 and FF respectively
- ☐ 12 and FF respectively
- ☐ 13 and 00 respectively
- ☐ 12 and 00 respectively

20. In 8051, assume that register A has FBH and register B has 12H. After execution of DIV AB instruction, B register will contain

(0/1 Point)

- ☐ 14H
- ☐ 10H
- ☐ 16H
- ☐ 11H