EE341 Fall 2019 HW 4
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github.com/LewisCollum/microelectronics

5.4

5.4 An NMOS transistor that is operated with a small v_{DS} is found to exhibit a resistance r_{DS}. By what factor will r_{DS} change in each of the following situations?

(a) V_{OV} is doubled.
(b) The device is replaced with another fabricated in the same technology but with double the width.
(c) The device is replaced with another fabricated in the same technology but with both the width and length doubled.
(d) The device is replaced with another fabricated in a more advanced technology for which the oxide thickness is halved and similarly for W and L (assume μ_n remains unchanged).

(a)

$$r_{DS} = \frac{1}{g_D S}$$
$$g_{DS} = k_n v_{OV}$$
$$\implies r_{DS} = \frac{1}{k_n v_{OV}}$$
$$\frac{r_{DS_{new}}}{r_{DS}} = \frac{1/(k_n 2 v_{OV})}{1/(k_n v_{OV})} = \frac{1}{2}$$

$\boxed{r_{DS} \text{ is halved.}}$

(b)
The device width is proportional to the MOSFET transconductance parameter, k_n. So,

$$k_{n_{new}} = 2k_n.$$

As in (a),

$$\frac{r_{DS_{new}}}{r_{DS}} = \frac{1/(2k_n v_{OV})}{1/(k_n v_{OV})} = \frac{1}{2}.$$

$\boxed{r_{DS} \text{ is halved.}}$

(c)
Since the aspect ratio stays the same, the MOSFET transconductance parameter, stays the same. Therefore,
$\boxed{r_{DS} \text{ stays the same.}}$

(d)
As per (c), the aspect ratio stays the same and hence we will disregard the width, W, and length, L, for the total effect on r_{DS}.
The thickness of the oxide layer will have an effect on r_{DS}. The MOSFET transconductance parameter is proportional to the process transconductance parameter. The thickness of the oxide layer is inversely proportional to the process transconductance parameter. So, the MOSFET transconductance parameter, k_n, is inversely proportional to the thickness of the oxide layer, t_{ox}. We can relate this proportionality to r_{DS}:

$$k_n \propto t_{ox}^{-1}$$

$$r_{DS} \propto k_n^{-1}$$

$$\implies r_{DS} \propto t_{ox}.$$

Since t_{ox} is halved, $\boxed{r_{DS} \text{ is halved.}}$

5.8

5.8 Consider an NMOS transistor operating in the triode region with an overdrive voltage V_{OV}. Find an expression for the incremental resistance

$$r_{ds} \equiv 1 \Big/ \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{v_{DS}=V_{DS}}$$

Give the values of r_{ds} in terms of k_n and V_{OV} for $V_{DS} = 0$, $0.2V_{OV}$, $0.5V_{OV}$, $0.8V_{OV}$, and V_{OV}.

If $V_{DS} \ll V_{OV}$, then,

$$i_D = k_n V_{OV} V_{DS}$$

However, as V_{DS} rises,

$$i_D = k_n \left(V_{OV} - \frac{1}{2}V_{DS}\right) V_{DS}$$

where $V_{OV} - \frac{1}{2}V_{DS}$ replaces V_O due to tapering from an increase in holes at the drain.
So,

$$r_{DS} = \left[\frac{\delta i_D}{\delta v_{DS}}\right]^{-1}$$

becomes,

$$\begin{aligned} r_{DS} &= \left[\frac{1}{\delta v_{DS}}\left(k_n\left(V_{OV} - \frac{1}{2}V_{DS}\right)V_{DS}\right)\right]^{-1} \\ &= \left[k_n\left(V_{OV}\frac{1}{\delta v_{DS}}V_{DS} - \frac{1}{2}\frac{1}{\delta v_{DS}}V_{DS}^2\right)\right]^{-1} \\ &= \left[k_n\left(V_{OV} - V_{DS}\right)\right]^{-1} \end{aligned}$$

case $V_{DS} = 0$**:**

$$\boxed{r_{DS} = \frac{1}{k_n V_{OV}}}$$

case $V_{DS} = 0.2V_{OV}$**:**

$$\boxed{r_{DS} = \frac{1}{k_n \cdot 0.8V_{OV}}}$$

case $V_{DS} = 0.5V_{OV}$**:**

$$\boxed{r_{DS} = \frac{1}{k_n \cdot 0.5V_{OV}}}$$

case $V_{DS} = 0.8V_{OV}$**:**

$$\boxed{r_{DS} = \frac{1}{k_n \cdot 0.2V_{OV}}}$$

case $V_{DS} = V_{OV}$**:**

$$\boxed{r_{DS} = \infty}$$

5.24

5.24 When the drain and gate of a MOSFET are connected together, a two-terminal device known as a "diode-connected transistor" results. Figure P5.24 shows such devices obtained from MOS transistors of both polarities. Show that

(a) the i–v relationship is given by

$$i = \frac{1}{2}k'\frac{W}{L}(v - |V_t|)^2$$

(b) the incremental resistance r for a device biased to operate at $v = |V_t| + V_{OV}$ is given by

$$r \equiv 1\bigg/\left[\frac{\partial i}{\partial v}\right] = 1\bigg/\left(k'\frac{W}{L}V_{OV}\right)$$

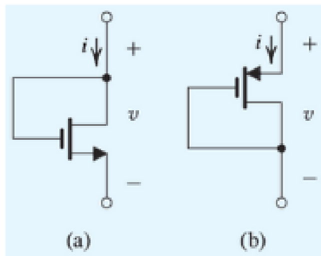


Fig. P5.24

(a)

Since $V_{DS} = V_{OV}$, the NMOS is saturated and the current through the transistor is,

$$i = \frac{1}{2}k_n(v - |V_t|)^2$$

where $i = i_{DS}$ and $v = V_{GS} = V_{DS}$.

(b)

$$\begin{aligned} r &= \left[\frac{\delta i}{\delta v}\right]^{-1} \\ &= \frac{1}{2k'\frac{W}{L}(v - V_t)} \\ &= \frac{1}{k_n'\frac{W}{L}V_{OV}} \end{aligned}$$

5.28

5.28 The NMOS transistor in Fig. P5.28 has $V_t = 0.4$ V and $k_n'(W/L) = 1$ mA/V^2. Sketch and clearly label i_D versus v_G with v_G varying in the range 0 to +1.8 V. Give equations for the various portions of the resulting graph.

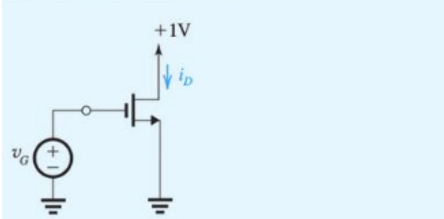


Figure P5.28

graph i_D **vs** V_G

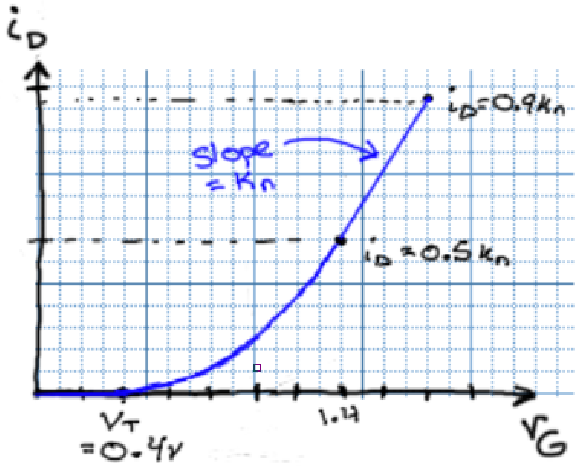


Figure 1: Note that $k_n = k_n' \frac{W}{L} = 1$mA and represents the MOSFET transconductance parameter.

case $0\text{V} \leq V_G \leq V_t = 0.4\text{V}$

The NMOS is off since $V_G < V_t$. So,

$$i_D = 0\text{mA}$$

case $V_t = 0.4\text{V} < V_G \leq V_t + V_{DS} = 1.4\text{V}$

The NMOS is saturated since $V_{DS} \geq V_G - V_t$.

$$i_D = \frac{1}{2} k_n V_{OV}^2 = \frac{1}{2} \cdot 1\text{mA} \cdot (V_G - 0.4\text{V})^2$$

case $V_t + V_{DS} = 1.4\text{V} \leq V_G \leq 1.8\text{V}$

The NMOS is operating in the triode region.

$$i_D = k_n \left(V_{OV} - \frac{1}{2} V_{DS} \right) V_{DS} = 1\text{mA} \cdot (V_G - 0.9)$$

5.39

5.39 A p-channel transistor for which $|V_t| = 0.8$ V and $|V_A| = 40$ V operates in saturation with $|v_{GS}| = 3$ V, $|v_{DS}| = 4$ V, and $i_D = 3$ mA. Find corresponding signed values for v_{GS}, v_{SG}, v_{DS}, v_{SD}, V_t, V_A, λ, and $k_p'(W/L)$.

$$v_{GS} = -3\text{V}$$

$$v_{SG} = 3\text{V}$$

$$v_{DS} = -4\text{V}$$

$$v_{SD} = 4\text{V}$$

$$V_t = -0.8\text{V}$$

$$V_A = -40\text{V}$$

$$\lambda = \frac{1}{V_A} = -25\text{mV}$$

$$i_D = \frac{1}{2}k_p(V_{GS} - V_t)^2(1 + \lambda v_{DS})$$

$$3\text{mA} = \frac{1}{2}k_p(-3 + 0.8)^2(1 + .025 \cdot 4)$$

$$\rightarrow k_p = 1.13\text{mA/V}^2$$

5.44

D 5.44 Design the circuit of Fig. P5.44 to establish a drain current of 0.1 mA and a drain voltage of +0.3 V. The MOSFET has $V_t = 0.5$ V, $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$, $L = 0.4\ \mu\text{m}$, and $W = 5\ \mu\text{m}$. Specify the required values for R_S and R_D.

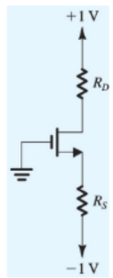


Fig. P5.44

find R_D

We know the voltage drop across R_D and the branch current. So,

$$R_D = \frac{1\text{V} - 0.3\text{V}}{0.1\text{mA}} = \boxed{7\text{k}\Omega}$$

find R_S

We need to know the voltage at the NMOS source, V_S, to figure out the voltage drop across R_S.

$$k_n = \mu_n C_{OX}\frac{W}{L} = 0.4\text{mA/V}^2 \cdot \frac{5\mu\text{m}}{0.4\mu\text{m}} = 5\text{mA/V}^2$$

Since $V_D > V_G$, the NMOS is saturated. So,

$$i_D = \frac{1}{2}k_n v_{OV}^2$$

$$0.1\text{mA} = \frac{1}{2} \cdot 5\text{mA/V}^2 \cdot v_{OV}^2$$

$$v_{OV} = 0.2\text{V}$$

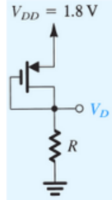
$$V_{GS} = v_{OV} + V_t = 0.2 + 0.5 = 0.7\text{V}$$

$$V_S = -0.7\text{V}$$

$$R_S = \frac{V_S - (-1\text{V})}{i_D} = \frac{-0.7 + 1}{0.1\text{mA}} = \boxed{3\text{k}\Omega}$$

5.49

D 5.49 The PMOS transistor in the circuit of Fig. P5.49 has $V_t = -0.5$ V, $\mu_p C_{ox} = 100\ \mu\text{A/V}^2$, $L = 0.18\ \mu\text{m}$, and $\lambda = 0$. Find the values required for W and R in order to establish a drain current of 180 μA and a voltage V_D of 1 V.



$$R = \frac{V_D}{i_D} = \frac{1\text{V}}{.18\text{mA}} = \boxed{5.6\text{k}\Omega}$$

Since $V_D = V_G$, the PMOS is saturated.

$$i_D = \frac{1}{2}k_p'\frac{W}{L}\left(v_{SG} - |V_t|\right)^2$$

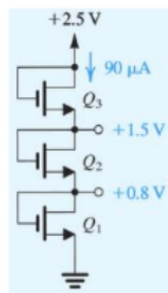
$$v_{SG} = V_{DD} - V_D = 0.8\text{V}$$

$$.18\text{mA} = \frac{1}{2} \cdot .1\text{mA/V}^2 \cdot \frac{W}{.18\mu\text{m}} \cdot (0.8\text{V} - 0.5\text{V})^2$$

$$\rightarrow \boxed{W = 7.2\mu\text{m}}$$

5.51

D 5.51 The NMOS transistors in the circuit of Fig. P5.51 have $V_t = 0.5$ V, $\mu_n C_{ox} = 90\ \mu\text{A/V}^2$, $\lambda = 0$, and $L_1 = L_2 = L_3 = 0.5\ \mu$m. Find the required values of gate width for each of Q_1, Q_2, and Q_3 to obtain the voltage and current values indicated.



i_D: 90μA

Since $V_D = V_G$ for each NMOS, each NMOS is saturated, This gives,

$$i_D = \frac{1}{2} k_n' \frac{w}{L} V_{OV}^2$$

$$90\mu\text{A} = \frac{1}{2} \cdot 90\mu\text{A/V}^2 \cdot \frac{w}{0.5\mu\text{m}} V_{OV}^2$$

For each Q,

$$w = \frac{1}{V_{OV}^2} \quad \text{where} \quad V_{OV} = V_{DS} - V_t$$

$$w = \frac{1}{(V_{DS} - 0.5)^2}$$

Case Q_3 $(V_{DS} = 1)$:

$$\boxed{w_3 = 4\mu\text{m}}$$

Case Q_2 $(V_{DS} = 0.7)$:

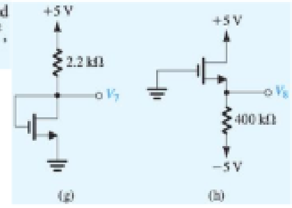
$$\boxed{w_2 = 25\mu\text{m}}$$

Case Q_1 $(V_{DS} = 0.8)$:

$$\boxed{w_1 = 11.1\mu\text{m}}$$

5.56

5.56 For each of the circuits in Fig. P5.56, find the labeled node voltages. For all transistors, $k_n'(W/L) = 0.5\ mA/V^2$, $V_t = 0.8$ V, and $\lambda = 0$.



$k_n = 0.5\ mA/V^2$, Let $V = V_{GS} = V_{DS}$

(g) $V_D = V_G$, so NMos is saturated.

$i_D = \frac{1}{2}k_n(V - V_t)^2$

$R = \frac{5 - V}{i_D}$

$\frac{5-V}{2.2E3} = \frac{1}{2}\cdot 0.5E\text{-}3\cdot(V - 0.8)^2$

$9.09 - 1.82V = V^2 - 1.6V + 0.64$

$V^2 + 0.22V - 8.45 = 0$

From python,

$\boxed{V = 2.8\ [V]}$

(h) $V_D > V_G$, so NMOS is saturated.

$i_D = \frac{1}{2}k_n(V_{GS} - V_t)^2$ $V_{GS} = 0 - V_S = -V_S$

$R = \frac{V_S + 5}{i_D} \rightarrow i_D = \frac{V_S + 5}{400k}$

$\frac{V_S + 5}{400E3} = \frac{1}{2}0.5E\text{-}3(-V_S - 0.8)^2$

$0.01V_S + 0.05 = (-V_S - 0.8)^2$
$= V_S^2 + 1.6V_S + 0.64$

$V_S^2 + 1.59V_S + 0.59$

$V_S = -1, -0.59$

← $V_{GS} = 0.59 < V_T$ BAD ROOT

$\boxed{V_S = -1\ [V]}$

5.58