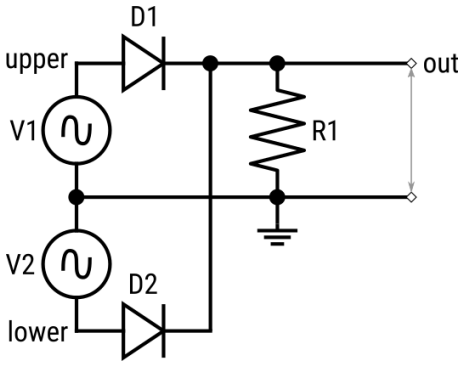
EE341 Fall 2019 HW 3
Lewis Collum
Updated: November 10, 2019

SPICE LAYOUT



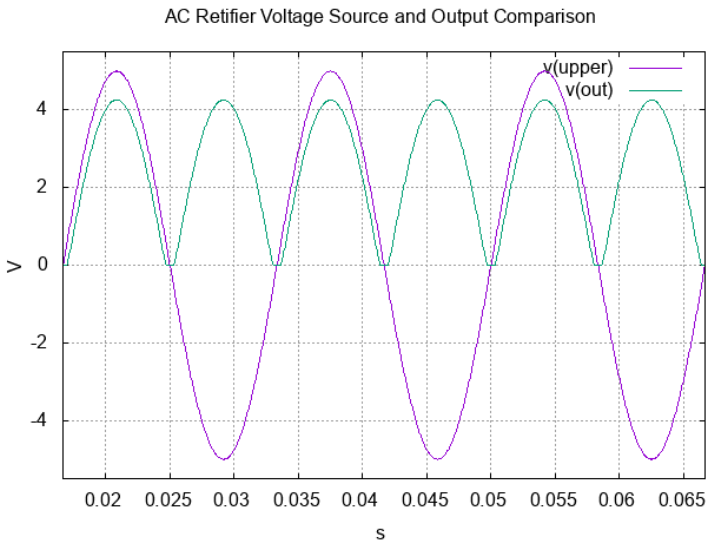
(A) v_S VS v_O

Voltage Source and Output Comparison Plot

```
.title AC Retifier Voltage Source and Output Comparison
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
.end
.control
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file v(upper) v(out)
.endc
```

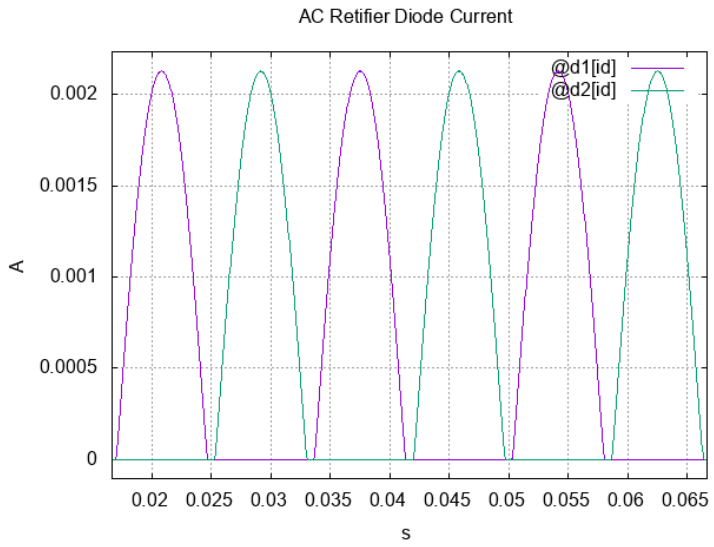


Current Through Diodes Plot

```
.title AC Retifier Diode Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
.end
.control
save @d1[id] @d2[id]
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file @d1[id] @d2[id]
.endc
```

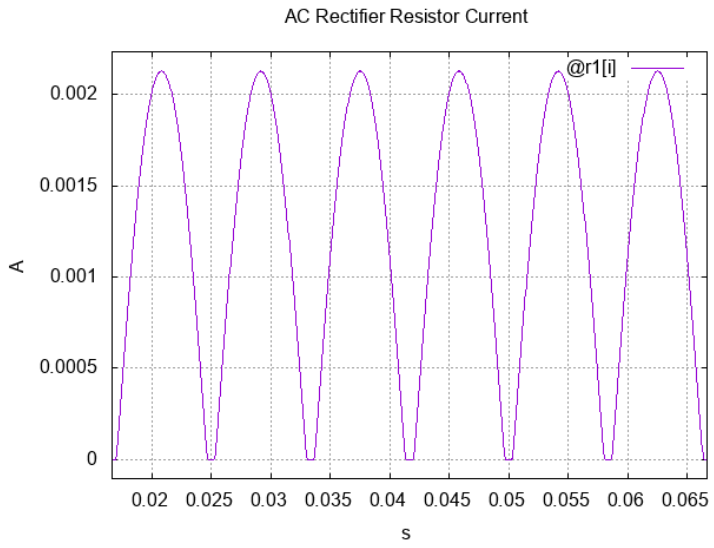


Current Through the Resistor Plot

```
.title AC Rectifier Resistor Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
.end
.control
save @r1[i]
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file @r1[i]
.endc
```



Analysis of the Voltage Difference between v_S and v_O

The difference between the source and output voltage is not constant — assuming the conducting diode does not have a constant voltage drop. The relationship between v_S and v_O is

$$v_S - v_D = v_O.$$

Using spice to simulate, we can plot the transfer function as well as the difference between the source and output voltages.

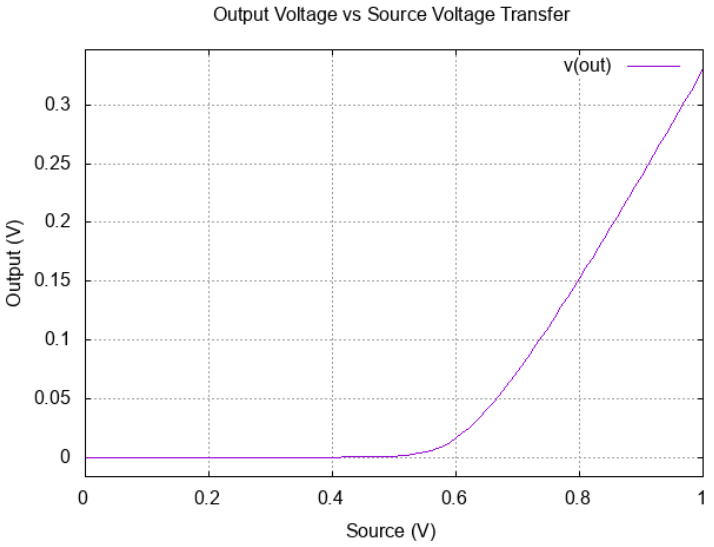


Figure 1: Demonstrates a non-constant voltage drop across the diode in relation to the source voltage.

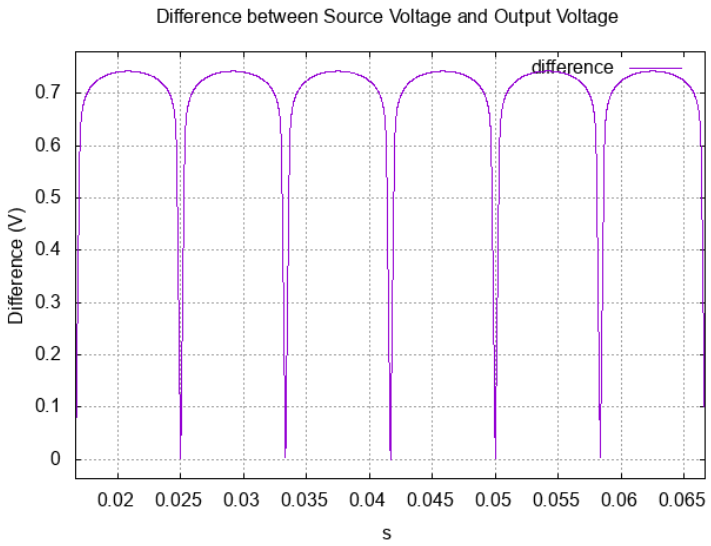


Figure 2: Demonstrates a non-constant difference between the source voltage and the output voltage over time. The difference reaches its max at every quarter cycle, with the maximum difference being about 0.75V.

(B) PIV ESTIMATION

Theoretical PIV

The peak inverse voltage (PIV) for a full-wave rectifier is estimated as

$$PIV = 2V_S - V_D.$$

V_S is 5V and V_D (from the previous section) was observed to be about 0.75V.

So,

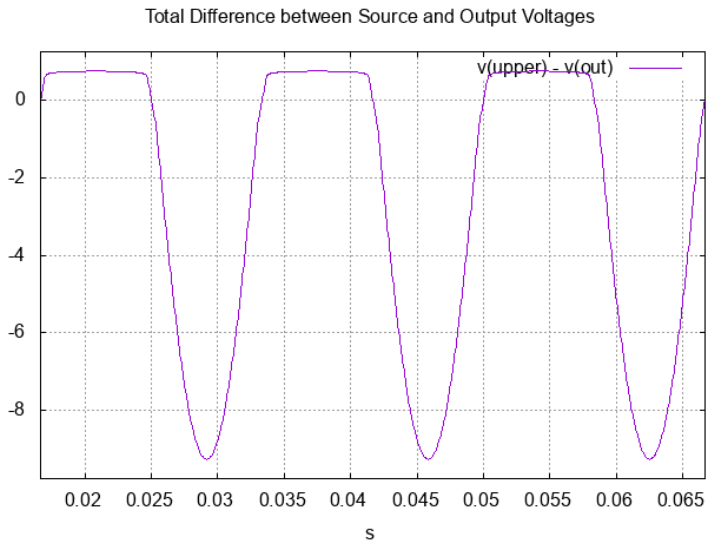
$$\boxed{PIV = 2 \cdot 5 - 0.75 = 9.25\text{V}}$$

Graphical PIV

```
.title Total Difference between Source and Output Voltages
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
.end
.control
run
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
let difference = abs(v(upper) - v(out))
meas tran maxDifference max difference
echo "$&maxDifference" > $file
gnuplot $file v(upper) - v(out)
.endc
```



The PIV can be found, in simulation, by getting the max of the absolute difference between v_S and v_O. In this case, the simulation reports that the maximum absolute difference is 9.25787 .

Error

$$Error = \frac{|graphical - theoretical|}{theoretical}$$

```
theoretical = 2*5 - float(theoretical)
graphical = float(graphical)
print(f"Error = {(graphical - theoretical)*100/theoretical:.3}%")
```

Error = 1.15e+03%
The error was obtained from analogous simulation results and therefore is approximately 0%.

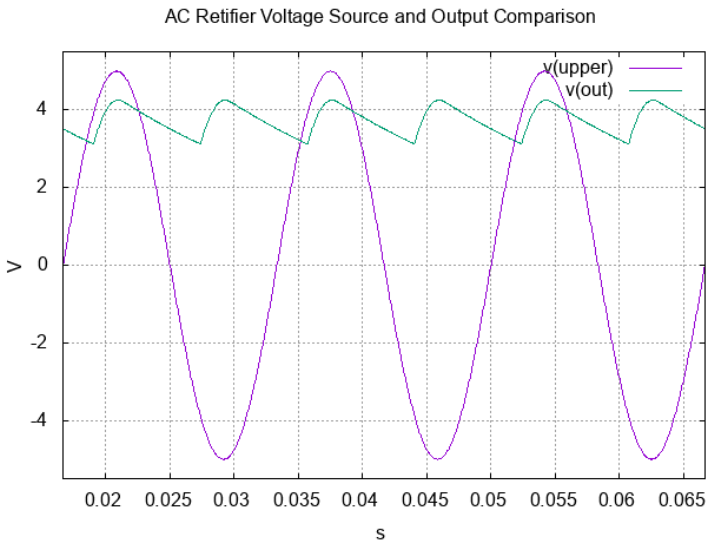
10μF Capacitor across R

Voltage Source and Output Comparison Plot

```
.title AC Retifier Voltage Source and Output Comparison
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

c1 out 0 10u
r1 out 0 2k
.end
.control
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
meas tran ripple pp v(out)
echo "$&ripple" > $file
gnuplot $file v(upper) v(out)
.endc
```

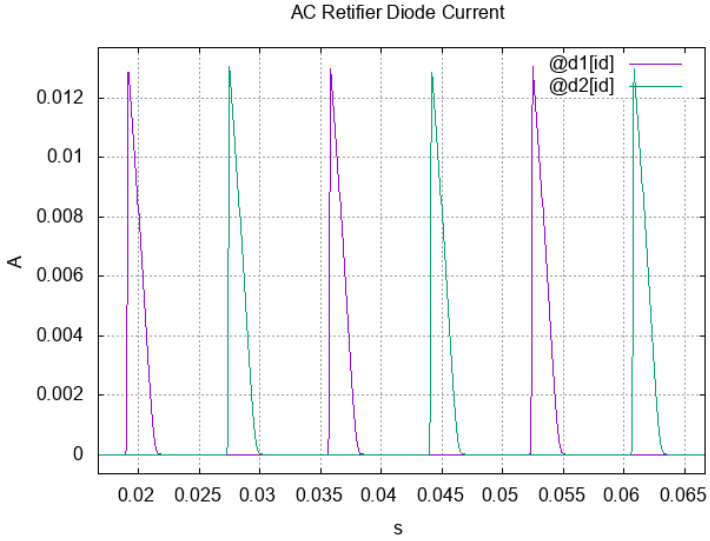


Current Through Diodes Plot

```
.title AC Retifier Diode Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

c1 out 0 10u
r1 out 0 2k
.end
.control
save @d1[id] @d2[id]
tran 0.05ms 66.66ms 16.66ms
meas tran maxCurrent max @d1[id]
echo "$&maxCurrent" > $file
set gnuplot_terminal=png/quit
gnuplot $file @d1[id] @d2[id]
.endc
```

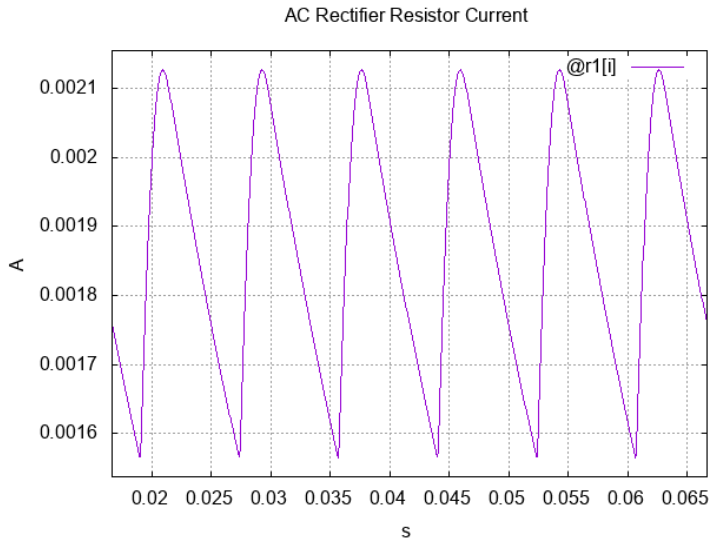


Current Through the Resistor Plot

```
.title AC Rectifier Resistor Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

c1 out 0 10u
r1 out 0 2k
.end
.control
save @r1[i]
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file @r1[i]
.endc
```



150μF Capacitor across R

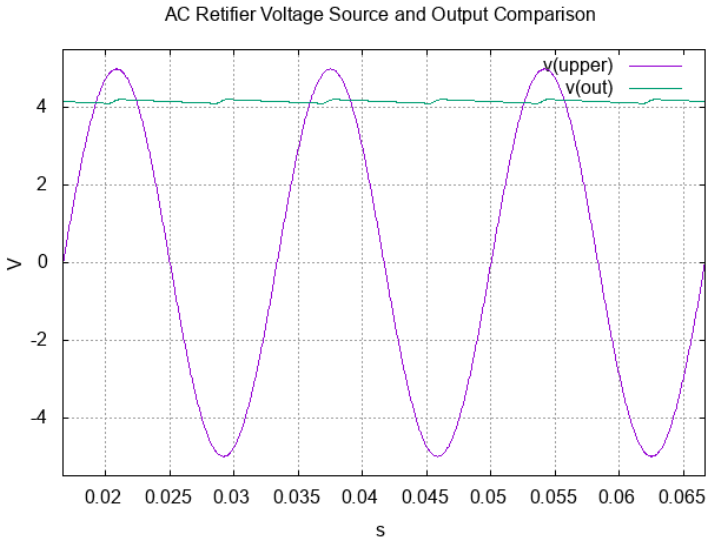
Voltage Source and Output Comparison Plot

```
.title AC Retifier Voltage Source and Output Comparison
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

c1 out 0 150u
r1 out 0 2k
.end
.control
tran 0.05ms 66.66ms 16.66ms
meas tran ripple pp v(out)
echo "$&ripple" > $file
set gnuplot_terminal=png/quit
```

```
gnuplot $file v(upper) v(out)
.endc
```

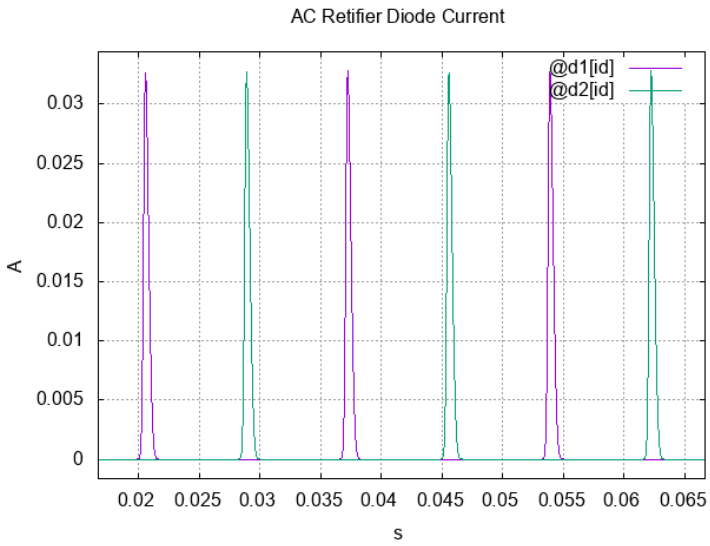


Current Through Diodes Plot

```
.title AC Retifier Diode Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

c1 out 0 150u
r1 out 0 2k
.end
.control
save @d1[id] @d2[id]
tran 0.05ms 66.66ms 16.66ms
meas tran maxCurrent max @d1[id]
echo "$&maxCurrent" > $file
set gnuplot_terminal=png/quit
gnuplot $file @d1[id] @d2[id]
.endc
```

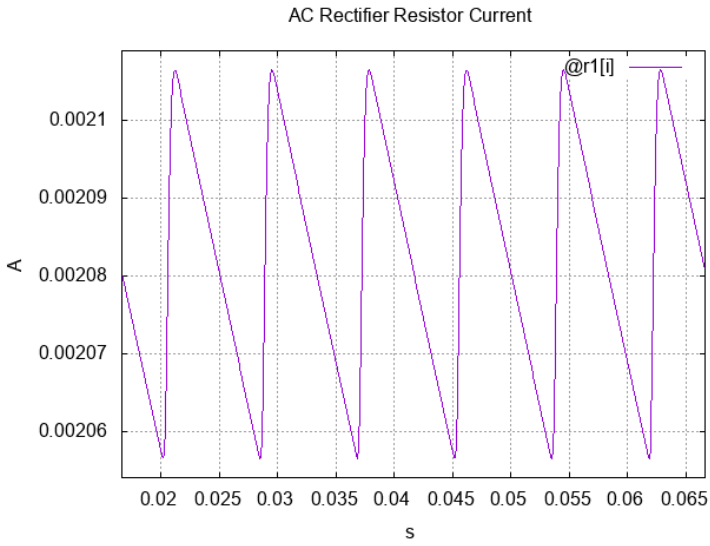


Current Through the Resistor Plot

```
.title AC Rectifier Resistor Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

c1 out 0 150u
r1 out 0 2k
.end
.control
save @r1[i]
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file @r1[i]
.endc
```



V_r AND i_{Dmax} FOR 10μF AND 150μF CAPACITOR CIRCUITS

```
import math
from recordtype import recordtype
PeakRectifier = recordtype('PeakRectifier', ['vp', 'f', 'c', 'r'])

vs = 5
vd = 0.75

capacitors = [10e-6, 150e-6]
vrSim = [1.12335, 0.099591]
idmaxSim = [0.0130566, 0.0327946]
peakRectifier = PeakRectifier(
    vp = vs - vd,
    f = 60,
    c = None,
    r = 2e3)

def rippleVoltage(pr: PeakRectifier) -> float:
    return pr.vp / 2 / pr.f / pr.c / pr.r

def diodeMaxCurrent(pr: PeakRectifier) -> float:
    return (pr.vp / pr.r) * (1 + 2*math.pi*math.sqrt(pr.vp / 2 / rippleVoltage(pr)))

for i, capacitor in enumerate(capacitors):
    peakRectifier.c = capacitor
    vr = rippleVoltage(peakRectifier)
    idmax = diodeMaxCurrent(peakRectifier)
    print((f"{peakRectifier.c}F:\n"
           f"  Ripple Voltage (Theory) = {vr:.5}\n"
           f"  Ripple Voltage (Sim) = {vrSim[i]:.5}\n"
           f"  Ripple Voltage Error = {abs(vr - vrSim[i])*100/vrSim[i]:.3}%\n\n"
           f"  Diode Current Max (Theory) = {idmax:.5}\n"
           f"  Diode Current Max (Sim) = {idmaxSim[i]:.5}\n"
           f"  Diode Max Current Error = {abs(idmax - idmaxSim[i])*100/idmaxSim[i]:.3}%\n"))
```

```
1e-05F:
  Ripple Voltage (Theory) = 1.7708
  Ripple Voltage (Sim) = 1.1234
  Ripple Voltage Error = 57.6%

  Diode Current Max (Theory) = 0.016751
  Diode Current Max (Sim) = 0.013057
  Diode Max Current Error = 28.3%

0.00015F:
  Ripple Voltage (Theory) = 0.11806
  Ripple Voltage (Sim) = 0.099591
  Ripple Voltage Error = 18.5%

  Diode Current Max (Theory) = 0.058772
  Diode Current Max (Sim) = 0.032795
  Diode Max Current Error = 79.2%
```

The high amount error is possibly due to our simulation components being less ideal than theoretical components.