EE341 Fall 2019 HW 6
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7.30

7.30 For the NMOS amplifier in Fig. P7.30, replace the transistor with its T equivalent circuit, assuming $\lambda = 0$. Derive expressions for the voltage gains v_s/v_i and v_d/v_i.

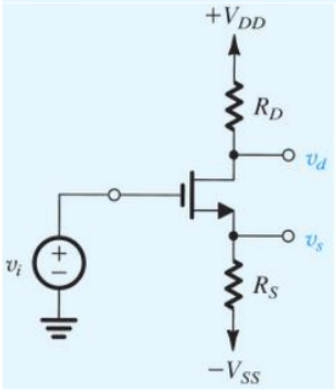
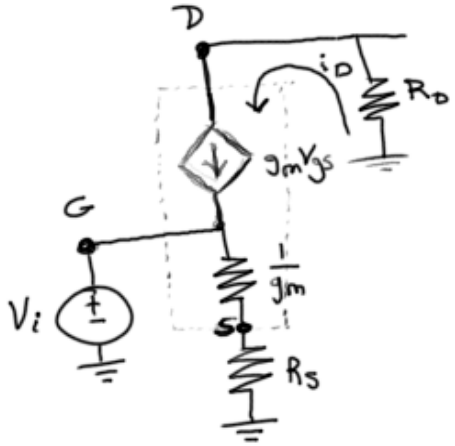


Fig. P7.30



$i_D = g_m v_{gs}$

$v_i = i_D\left(\frac{1}{g_m} + R_S\right)$

$v_S = i_D R_S$

$v_D = -i_D R_D \quad \therefore \quad \frac{0 - v_D}{R_D} = i_D$

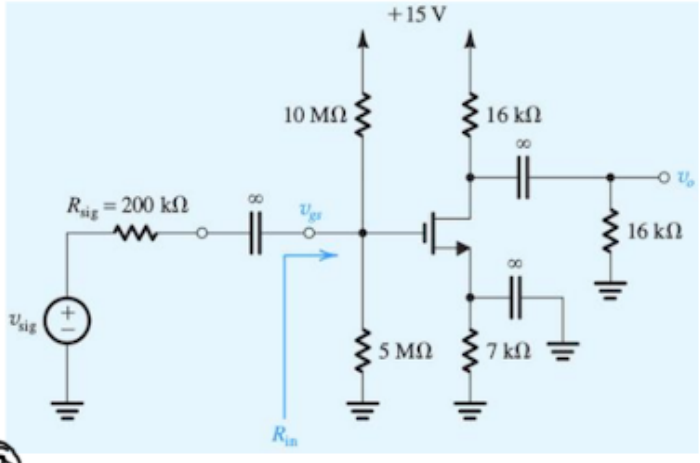
$$\therefore \frac{v_S}{v_i} = \frac{i_D R_S}{i_D\left(\frac{1}{g_m} + R_S\right)} = \frac{R_S}{\frac{1}{g_m} + R_S} = \frac{1}{\frac{1}{g_m R_S} + 1}$$

$$\therefore \frac{v_D}{v_i} = \frac{-i_D R_D}{i_D\left(\frac{1}{g_m} + R_S\right)} = -\frac{R_D}{R_S}\frac{1}{\frac{1}{g_m R_S} + 1}$$

7.33

***7.33** Figure P7.33 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for dc.

(a) If the transistor has $V_t = 1$ V, and $k_n = 4$ mA/V^2, verify that the bias circuit establishes $V_{GS} = 1.5$ V, $I_D = 0.5$ mA, and $V_D = +7.0$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
(b) Find g_m and r_o if $V_A = 100$ V.
(c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.
(d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.



(a)

$V_{ov} = V_{GS} - V_t = 1.5 - 1.0 = 0.5\ V$

Since $V_{DS} \geq V_{ov}$, the NMOS is saturated.

$I_D = \frac{1}{2} K_n V_{ov}^2 \rightarrow 0.5 = \frac{1}{2} \cdot 4 \cdot 0.5^2 = 0.5.$

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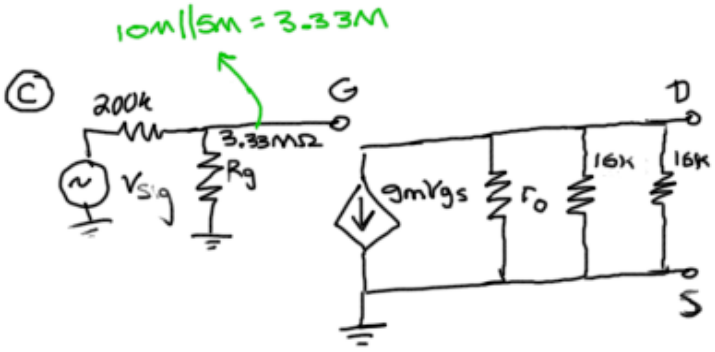
(b)

$$r_o = \frac{|V_A|}{I_D} = \frac{100V}{0.5mA} = 200\,k\Omega$$

$$g_m = \sqrt{2k_n I_D} = \sqrt{2 \cdot 4 \cdot 0.5} = 2\,mU$$

(c)



(d)

$$R_{in} = R_G = 3.33M\Omega$$

$$V_{gs} = V_{sig}\frac{R_g}{R_g + R_{sig}} \rightarrow \frac{V_{gs}}{V_{sig}} = \frac{R_g}{R_g + R_{sig}} = 0.94$$

$$\frac{V_o}{V_{gs}} = -g_m(r_o||16k||16k) = -15.4$$

$$\frac{V_o}{V_{sig}} = \frac{V_o}{V_{gs}} \cdot \frac{V_{gs}}{V_{sig}} = -15.4 \cdot 0.94 = -14.48$$

7.121

D *7.121 The MOSFET in the circuit of Fig. P7.121 has $V_t = 0.8$ V, $k_n = 5$ mA/V^2, and $V_A = 40$ V.

(a) Find the values of R_S, R_D, and R_G so that $I_D = 0.4$ mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ± 0.8 V is possible, and the input resistance at the gate is 10 MΩ. Neglect the Early effect.

(b) Find the values of g_m and r_o at the bias point.

(c) If terminal Z is grounded, terminal X is connected to a signal source having a resistance of 1 MΩ, and terminal Y is connected to a load resistance of 10 kΩ, find the voltage gain from signal source to load.

(d) If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?