EE341 Fall 2019 HW 3

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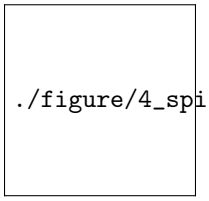
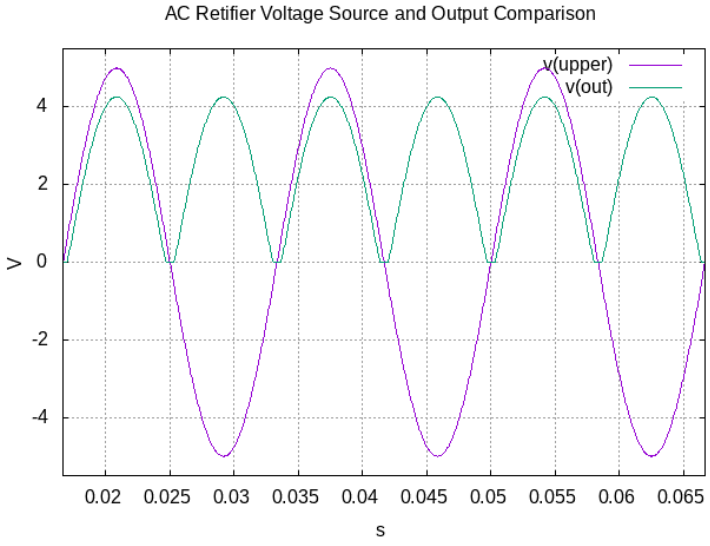
github.com/LewisCollum/microelectronics




```
.title AC Retifier Voltage Source and Output Comparison
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
.end
.control
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file v(upper) v(out)
.endc
```

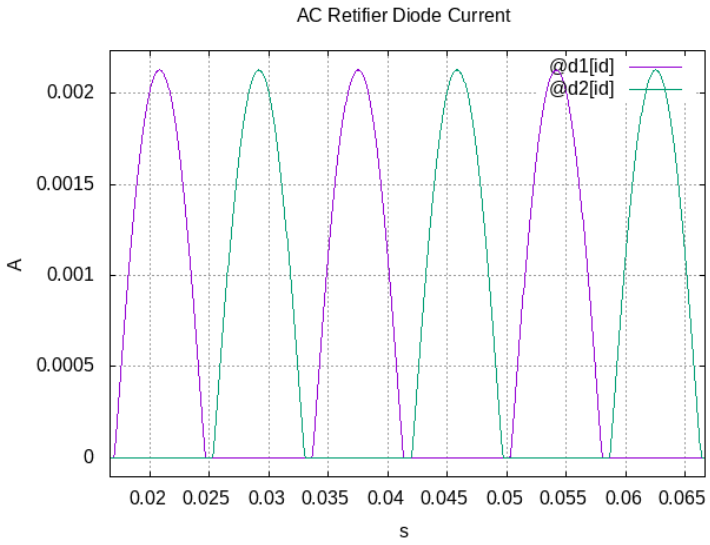



```
.title AC Retifier Diode Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
```

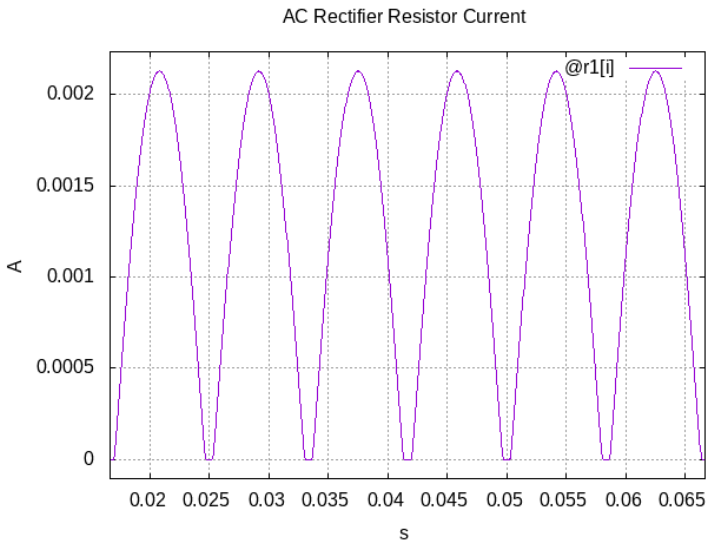
```
.end
.control
save @d1[id] @d2[id]
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file @d1[id] @d2[id]
.endc
```




```
.title AC Rectifier Resistor Current
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
.end
.control
save @r1[i]
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file @r1[i]
.endc
```

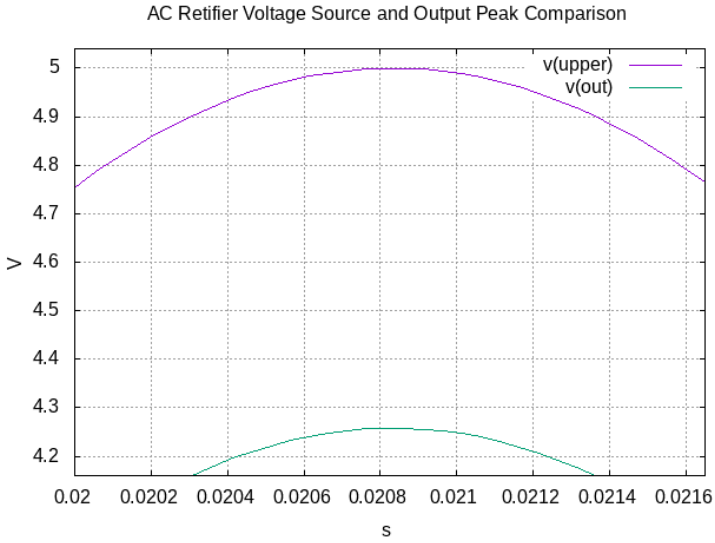


$V_S - V_O$

```
.title AC Retifier Voltage Source and Output Peak Comparison
.model diode d(IS=10e-15, n=1.1)
v1 upper 0 dc 0 ac 5 sin(0 5 60Hz)
v2 0 lower dc 0 ac 5 sin(0 5 60Hz)

d1 upper out diode
d2 lower out diode

r1 out 0 2k
.end
.control
tran 0.05ms 66.66ms 16.66ms
set gnuplot_terminal=png/quit
gnuplot $file v(upper) v(out) xlimit 20ms 21.65ms ylimit 4.2 5
.endc
```



The difference is not constant. This is because as the current through the diode increase, the voltage drop across the diode increase logarithmically.

The difference reaches its max at every quarter cycle. From the plot above, the maximum observable difference is about $5\text{V} - 4.25\text{V} = 0.75\text{V}$.