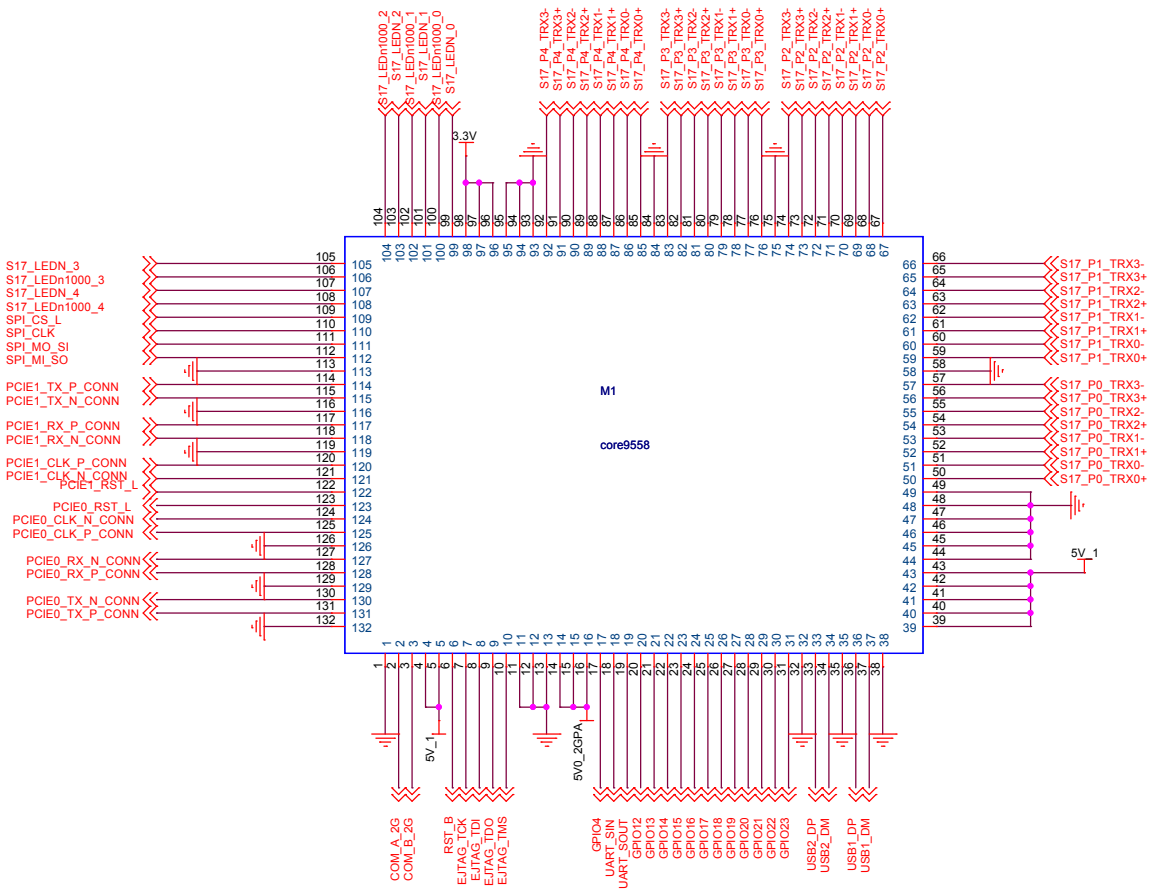

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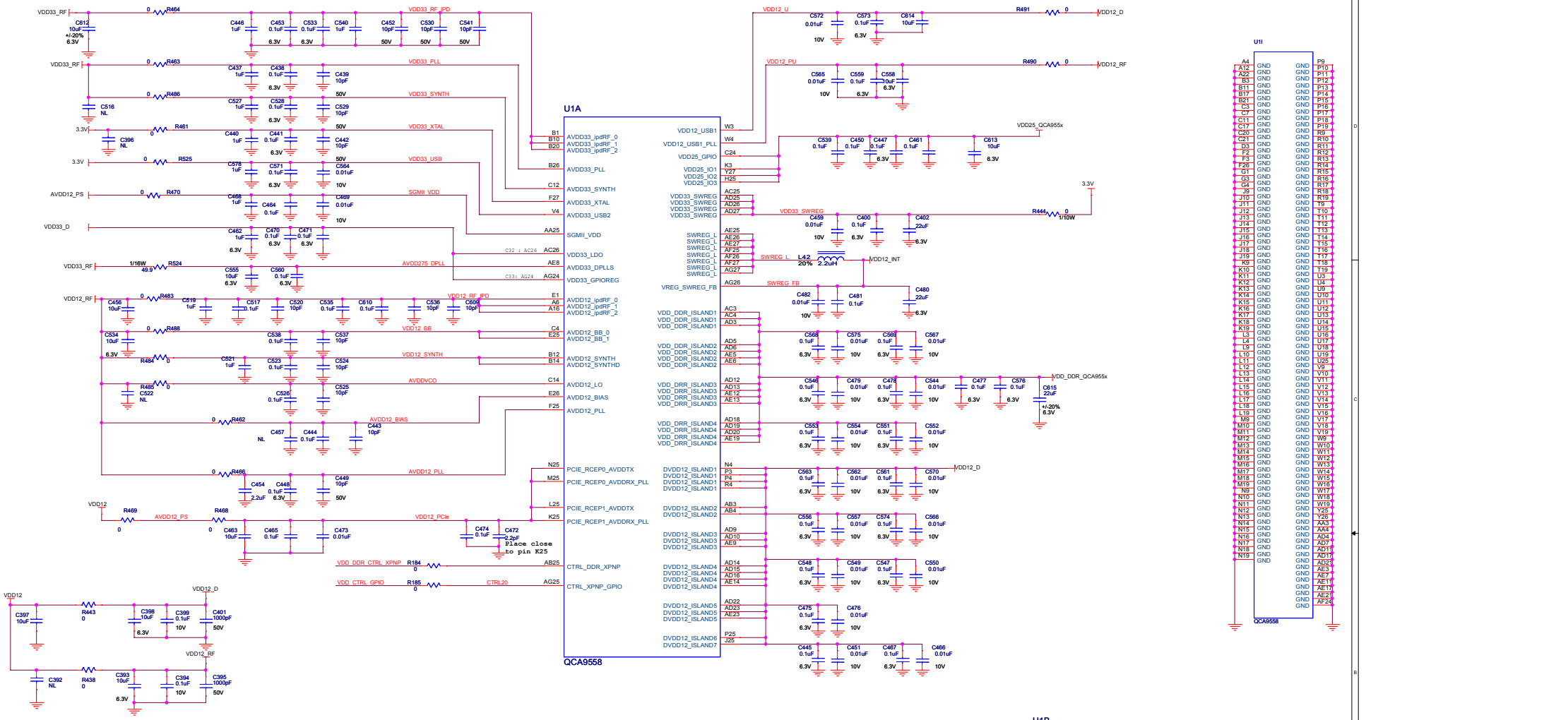
Size A3	Document Number <Doc>	Rev <RevCod
Date: Friday, December 22, 2017	Sheet 1 of 1	



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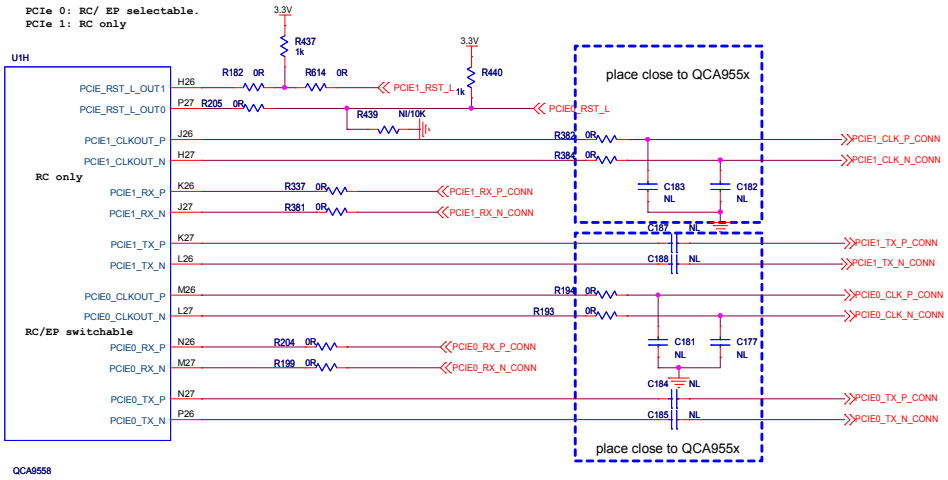
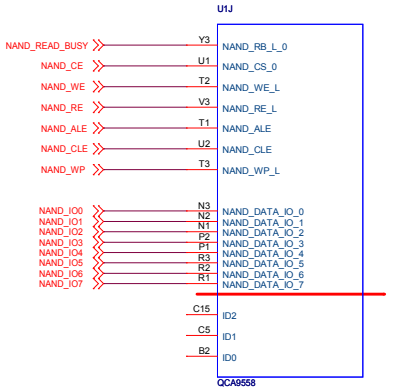
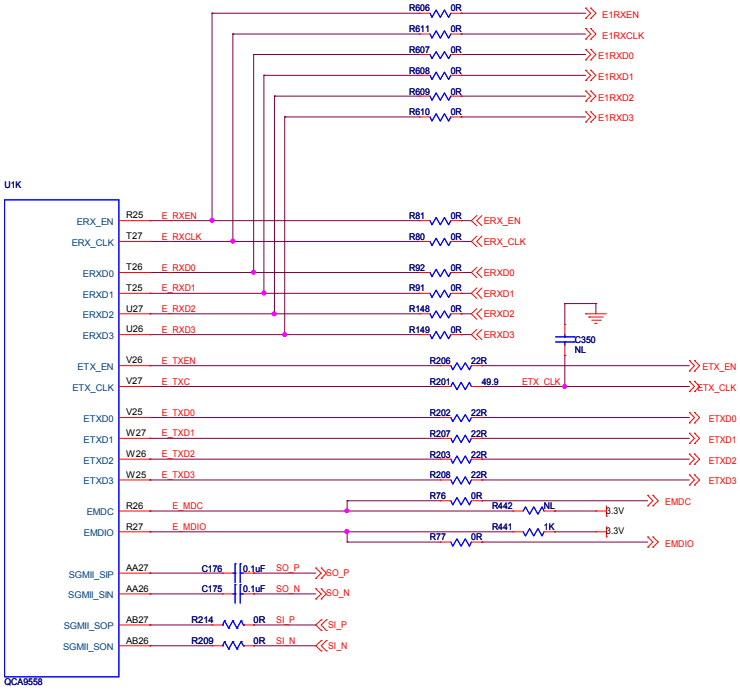
Qualcomm ATHEROS
QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

TITLE: QCA955x_Pwr_Gnd_USB

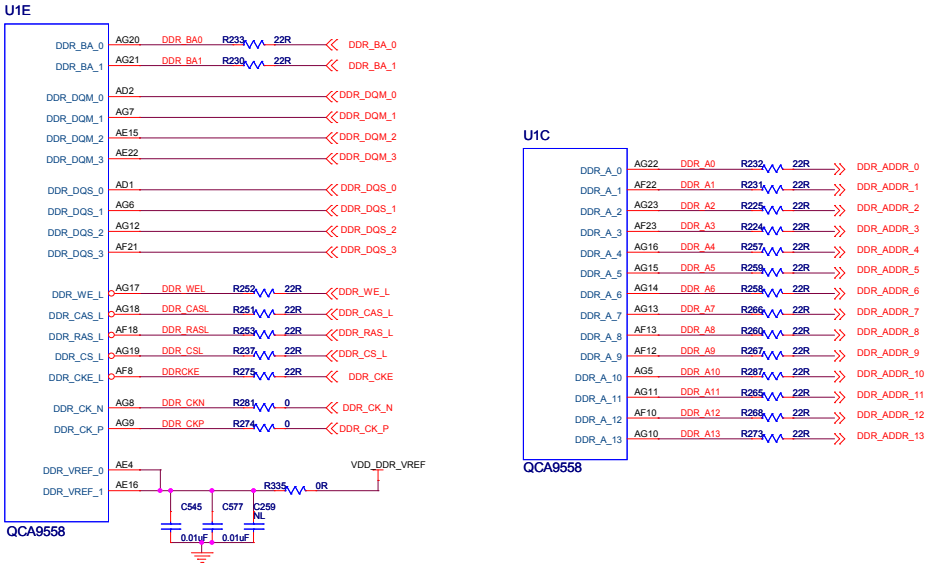
DATE	SIZE	REV	SHEET	OF	DWG NO
9/17/2012	C	D	4	18	245-02376-023

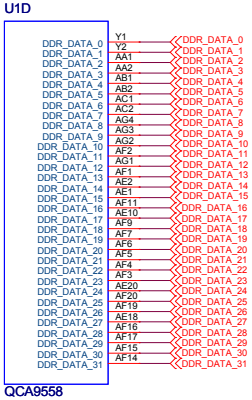






Qualcomm ATHEROS	QUALCOMM ATHEROS 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110			TITLE	QCA955x_SGMII_RGMII_PCIe
DATE 9/17/2012	SIZE C	REV D	SHEET 5 OF 18	DWG NO	245-02376-023





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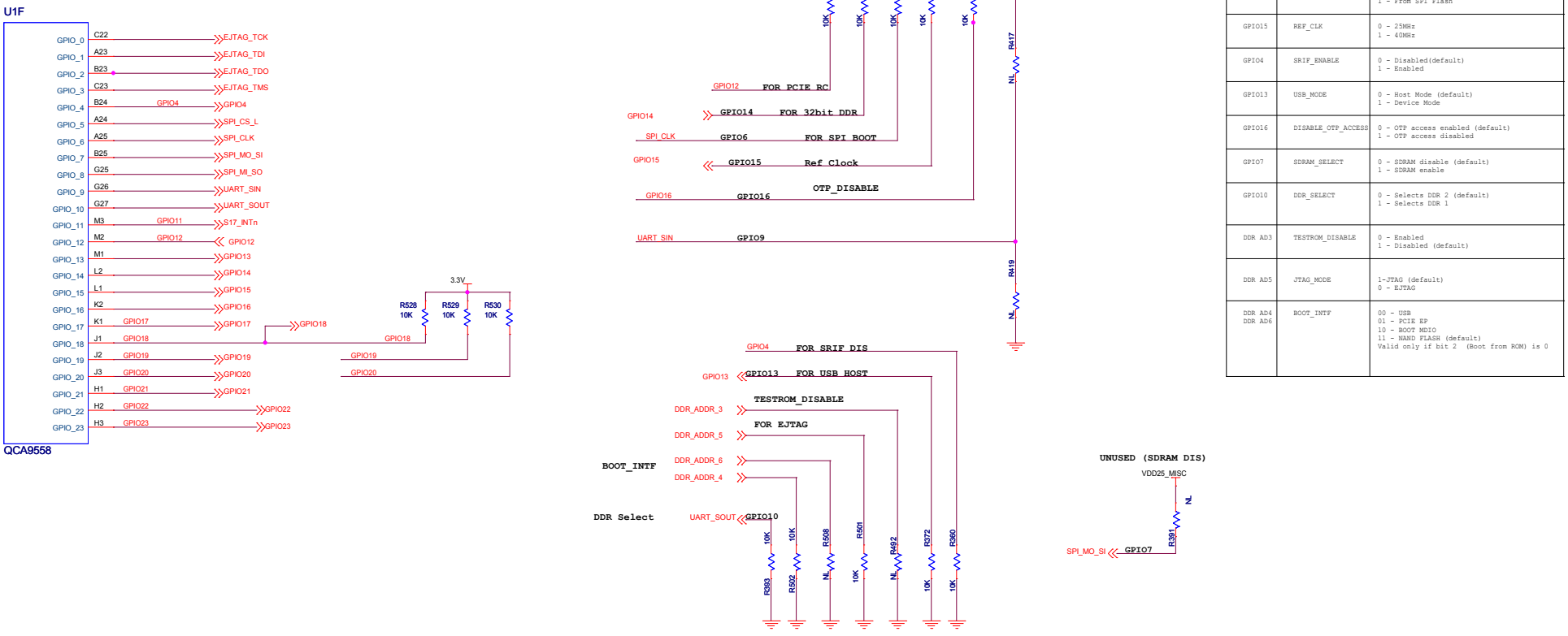
QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

TITLE: QCA955x_DDR

DATE	SIZE	REV	SHEET	DWG NO
9/17/2012	C	D	6 OF 18	245-02376-023

Boot Strap Options



PIN	NAME	DESCRIPTION
GPIO12	RC_SELECT	0 - PCIE EP (default) 1 - PCIE RC
GPIO14	DDR_WIDTH	0 - 16bit 1 - 32bit
GPIO6	BOOT_SELECT	0 - Select from ROM 1 - From SPI Flash
GPIO15	REF_CLK	0 - 25MHz 1 - 40MHz
GPIO4	SRIF_ENABLE	0 - Disabled(default) 1 - Enabled
GPIO13	USB_MODE	0 - Host Mode (default) 1 - Device Mode
GPIO16	DISABLE_OTP_ACCESS	0 - OTP access enabled (default) 1 - OTP access disabled
GPIO7	SDRAM_SELECT	0 - SDRAM disable (default) 1 - SDRAM enable
GPIO10	DDR_SELECT	0 - Selects DDR 2 (default) 1 - Selects DDR 1
DDR AD3	TESTROM_DISABLE	0 - Enabled 1 - Disabled (default)
DDR AD5	JTAG_MODE	1-JTAG (default) 0 - EJTAG
DDR AD4 DDR AD6	BOOT_INTF	00 - USB 01 - PCIE EP 10 - BOOT MDIO 11 - NAND FLASH (default) Valid only if bit 2 (Boot from ROM) is 0

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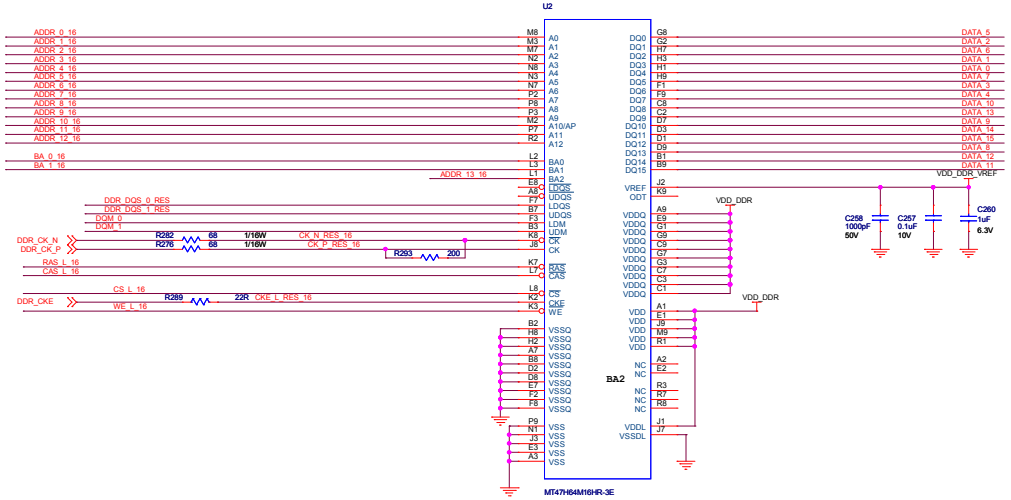
QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

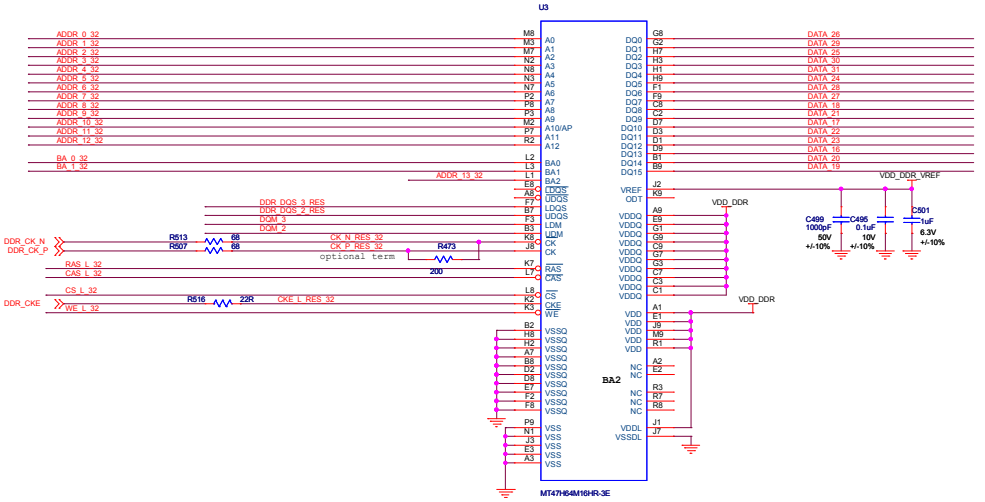
TITLE: QCA955x_GPIOs_Boot STRAP

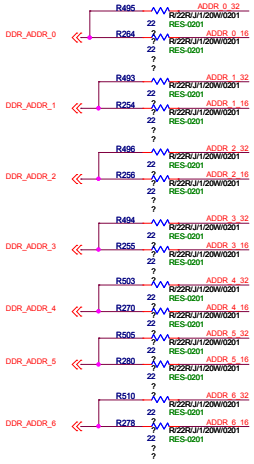
DWG NO: 245-02376-023

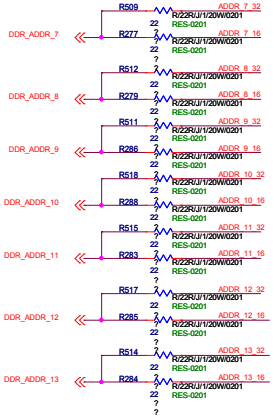
DATE 9/17/2012 | SIZE C | REV D | SHEET 7 OF 18

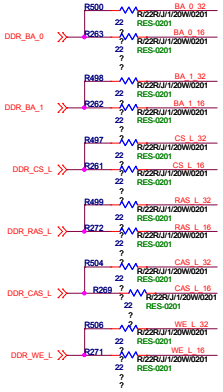
DDR2

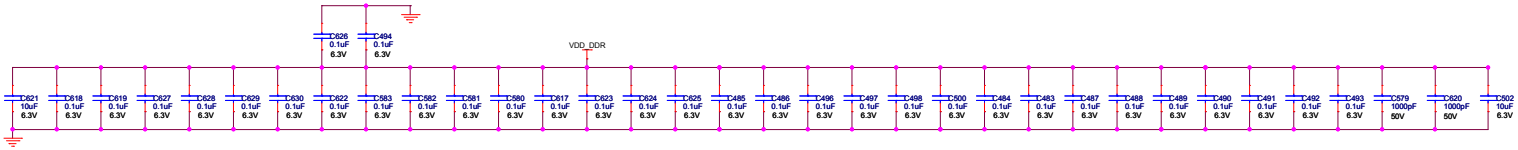










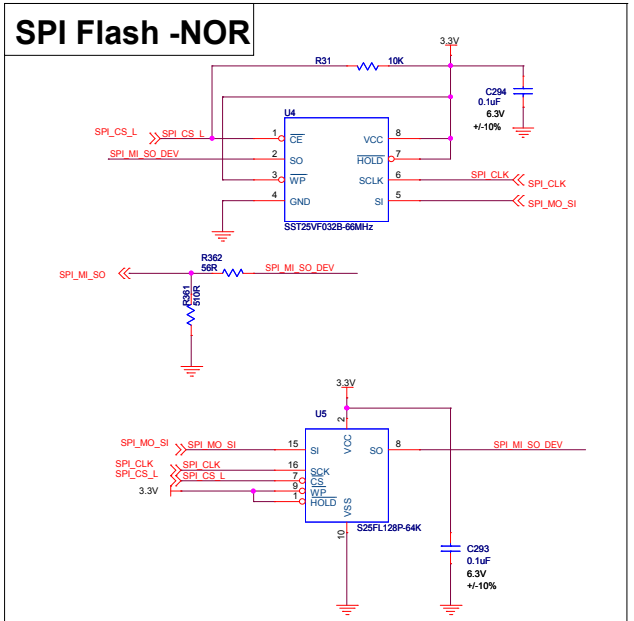


QUALCOMM ATHEROS 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110			TITLE	DDR2		
DATE	9/17/2012	SIZE C	REV D	SHEET 8 OF 18	DWG NO	245-02376-023

EJTAG HEADER

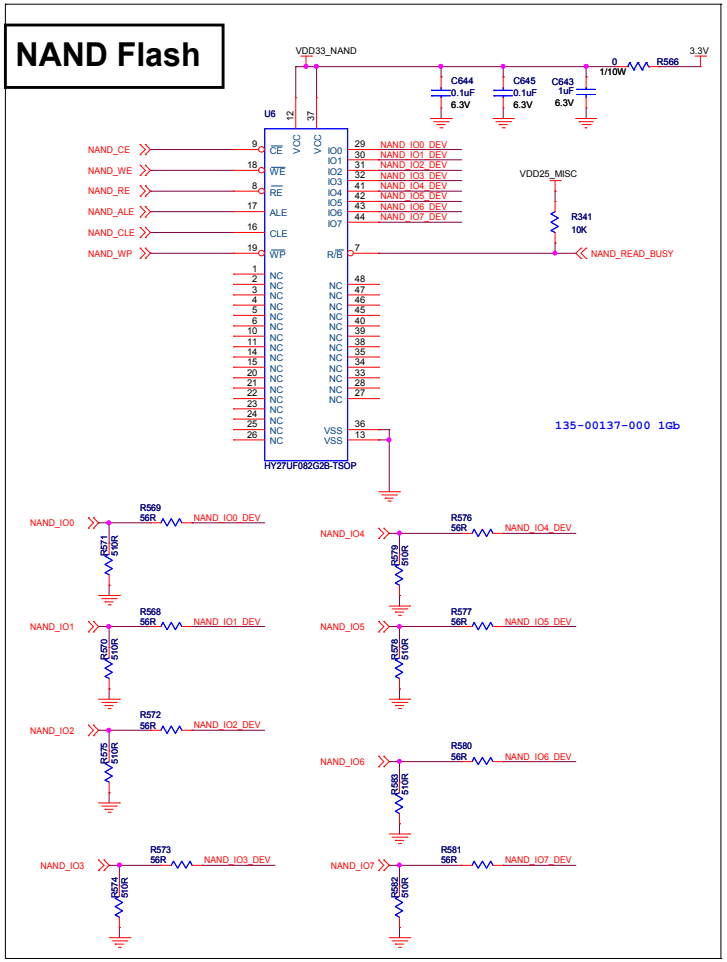
UART HEADER

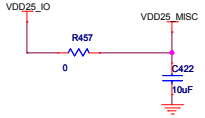
SPI Flash -NOR



USB

NAND Flash





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Qualcomm ATHEROS

QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

TITLE: EJTAG_USB_UART_NAND

DATE	SIZE	REV	SHEET	DWG NO
9/17/2012	C	D	9 OF 18	245-02376-023

SGMII i/f to QCA9558

SO_P 0R R168 SOP
SO_N 0R R165 SON
SI_P C136 0.1uF SIP
SI_N C137 0.1uF SIN

RGMII i/f to QCA9558

to RGMII0

ETX_CLK R154 0R GTXCLK
ETXD3 R163 0R TXD3
ETXD2 R164 0R TXD2
ETXD1 R159 0R TXD1
ETXD0 R160 0R TXD0
ETX_EN R155 0R TXEN

ERX_EN 0R R86 RXDV
ERXD0 0R R94 RXD0
ERXD1 0R R93 RXD1
ERXD2 0R R151 RXD2
ERXD3 0R R150 RXD3
ERX_CLK 0R R82 RXCLK
EMDIO 0R R88 TXD_MDIO
EMDC 0R R87 RXD_MDC

to RGMII1

ETX_EN R600 0R RG1_TXEN
ETX_CLK R601 0R RG1_GTXCLK
ETXD3 R602 0R RG1_TXD3
ETXD2 R603 0R RG1_TXD2
ETXD1 R604 0R RG1_TXD1
ETXD0 R605 0R RG1_TXD0

E1RXEN R594 0R RG1_RXDV
E1RXD0 R595 0R RG1_RXD0
E1RXD1 R596 0R RG1_RXD1
E1RXD2 R597 0R RG1_RXD2
E1RXD3 R598 0R RG1_RXD3
E1RXCLK RG1_RXCLK

SYS_RST_L SYS_RST_L
S17_INTn S17_INTn 0R R167 S17_INTn0

Eth LED i/f to LED display

S17_LEDn_0 S17_LEDn_0
S17_LEDn_1 S17_LEDn_1
S17_LEDn_2 S17_LEDn_2
S17_LEDn_3 S17_LEDn_3
S17_LEDn_4 S17_LEDn_4

S17_LEDn1000_0 S17_LEDn1000_0
S17_LEDn1000_1 S17_LEDn1000_1
S17_LEDn1000_2 S17_LEDn1000_2
S17_LEDn1000_3 S17_LEDn1000_3
S17_LEDn1000_4 S17_LEDn1000_4

Power On Strapping

DVDD_2.5V_S17

pin-B44 S17_SPI_DO 10K NL R415 R414 — MDIO_EN (D:1)
pin-B49 RG1_RXD2 NL R97 — SPI_SIZE(D:0)
pin-A65 RXCLK NL 10K R83 R84 — LED_OPEN_EN(D:1), SPI_EN(D:0)
pin-A54 RG1_RXDV 10K NL R412 R413 — AZ_EN
pin-A69 RXD1 10K NL R408 R407 — Mode_oclk_selH

1, use ext reg
0, set 1.1V at int reg LX

place close to AR8327

Normal Setting

pin-A64 RXDV 10K R409
pin-B60 RXD3 10K R428
pin-A70 RXD2 NL 10K R430 R429
pin-A55 RG1_RXD0 10K NL R410 R411

11: most save power; PHY power is minimize.
01: short cable save some power, long cable does not.
10: short and long cable all save some power. (recommended)
00: not save power.

25MHz Source

Y2 40MHz-7M40000005
XTLI C506 27pF — 3XTLO_XTLO C429 27pF

Amplitude of XTLI input clock must be less than 1.5V.

SPI Interface

C142 NL (1000pF)
U10 16Bit Mode
S17_SPI_CS 1 CS
S17_SPI_CLK 2 CLK
S17_SPI_DO 3 DI
S17_SPI_DI 4 DO
VCC 8 — C143
NC2 7
NC1 6
GND 5 — NL
No Load

Reset

SYS_RST_L 4.7K R96 S17_RSTL
R95 33.2K
R416 (100K) NL
C325 NL (0.1uF)

1.25V PLL Power

AVDDVCO_O
0R R434 C388 0.1uF NL C382
+/-10%
AVDDVCO_I
C376 0.1uF NL C378

Eth i/f to Transformers

S17_P0_TRX0+ S17_P0_TRX0-
S17_P0_TRX1+ S17_P0_TRX1-
S17_P0_TRX2+ S17_P0_TRX2-
S17_P0_TRX3+ S17_P0_TRX3-

S17_P1_TRX0+ S17_P1_TRX0-
S17_P1_TRX1+ S17_P1_TRX1-
S17_P1_TRX2+ S17_P1_TRX2-
S17_P1_TRX3+ S17_P1_TRX3-

S17_P2_TRX0+ S17_P2_TRX0-
S17_P2_TRX1+ S17_P2_TRX1-
S17_P2_TRX2+ S17_P2_TRX2-
S17_P2_TRX3+ S17_P2_TRX3-

S17_P3_TRX0+ S17_P3_TRX0-
S17_P3_TRX1+ S17_P3_TRX1-
S17_P3_TRX2+ S17_P3_TRX2-
S17_P3_TRX3+ S17_P3_TRX3-

S17_P4_TRX0+ S17_P4_TRX0-
S17_P4_TRX1+ S17_P4_TRX1-
S17_P4_TRX2+ S17_P4_TRX2-
S17_P4_TRX3+ S17_P4_TRX3-

U8 Atheros AR8327N

DVDD_2.5V_S17 — R431 4.7K, R432 4.7K
VDD3P3_ETH — C424 1uF, C423 10uF
GTXCLK — R456 0R, C365 0.1uF, C351 0.1uF

RXCLK — R85 0R C88 NL
DVDD_2.5V_S17 — R406 NL (1.5K), C89 0.1uF, C323 NL
RG1_GTXCLK — R613 0R C657 NL
RG1_RXCLK — R612 0R C656 NL

DVDD_1.2V_S17 — C156 0.1uF — FIL_CAP0
AVDD_1.2V_S17 — C163 0.1uF — FIL_CAP2
DVDD — C162 0.1uF — FIL_CAP3
VDD25_REG — C360 1000pF, R433 2.37K, C160 0.1uF

C141 0.1uF, R70 2.37K, C139 1000pF, C140 0.1uF, C138 0.1uF

Close to S17

LX_S17 — L23 4.7uH — R169 NL — C135 NL

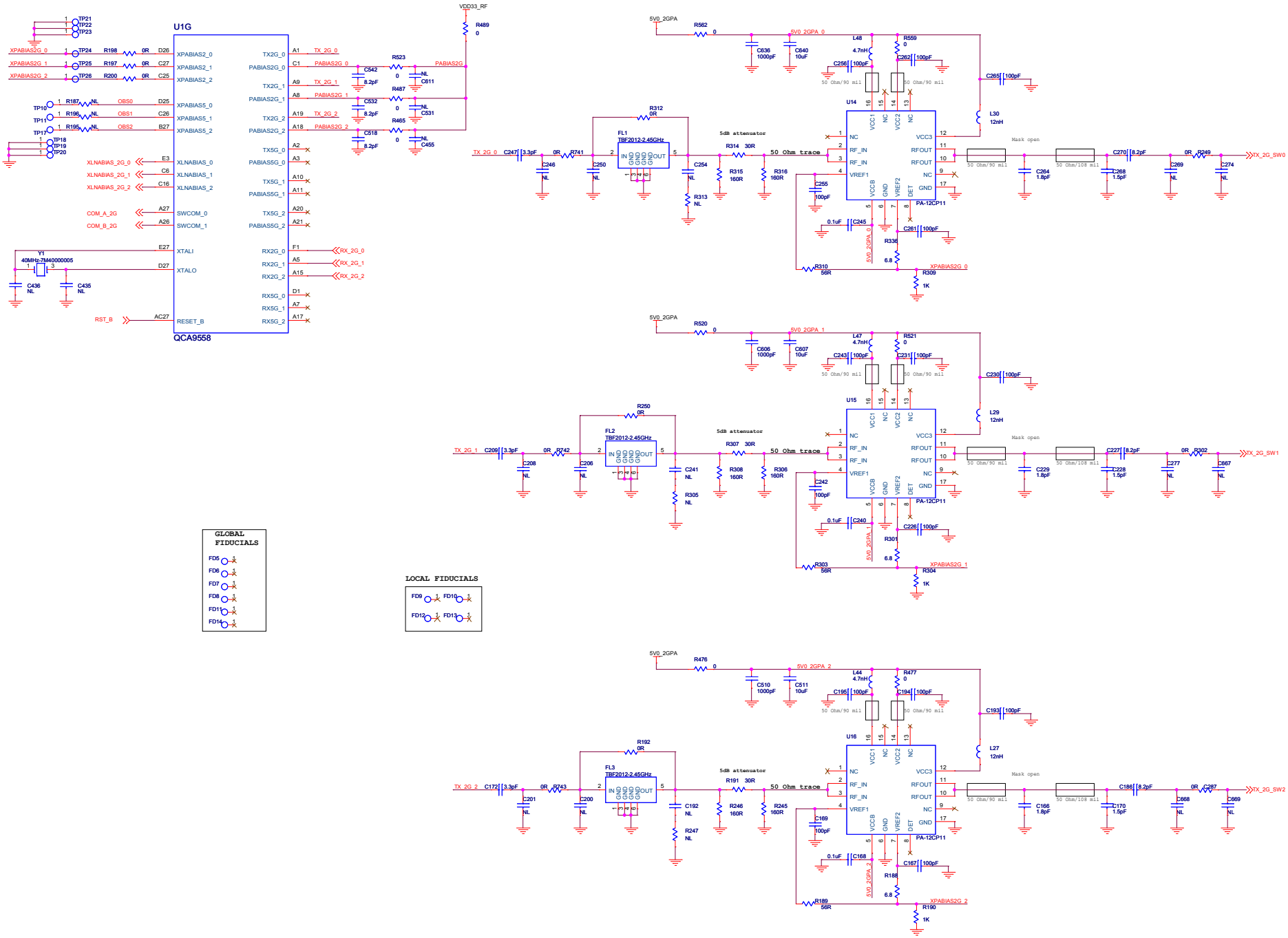
DVDD_1.2V_S17 — R186 NL
C155 22uF, C158 1uF, C364 0.1uF, C366 0.1uF, C354 0.1uF, C348 0.1uF, C352 0.1uF, C361 0.1uF, C425 0.1uF
L38 22 — AVDD_1.2V_S — C356 0.1uF
L23 25 — 2.5m Ohm/3A
AVDD_1.2V_S17
C159 10uF, C365 0.1uF, C369 0.1uF, C371 0.1uF, C373 0.1uF, C374 0.1uF, C379 0.1uF, C387 0.1uF, C386 0.1uF, C384 0.1uF, C383 0.1uF, C359 0.1uF, C358 0.1uF
C377 1uF, L41 56nH — DVDD — C161 0.1uF

VDD3P3_ETH — L40 25 — AVDD_3.3V — C504 10uF, C505 1uF
AVDD_3.3V
C370 0.1uF, C372 0.1uF, C375 0.1uF, C380 0.1uF, C385 0.1uF, C381 0.1uF, C362 0.1uF

C656,C657 close to L66

DVDD_2.5V_S17 — L22 22
VDD25_REG — C157 1uF, C428 1uF
DVDD_2.5V_S17 — C368 0.1uF, C367 0.1uF, C349 0.1uF, C357 0.1uF, C324 1uF
VDD15_REG_0 — C353 0.1uF
VDD15_REG_1 — C363 0.1uF

Qualcomm ATHEROS	QUALCOMM ATHEROS 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110		TITLE	AR8327_GIGA_Switch	
DATE 11/07/2012	SIZE C	REV D	SHEET 10 OF 18	DWG NO	245-02376-023



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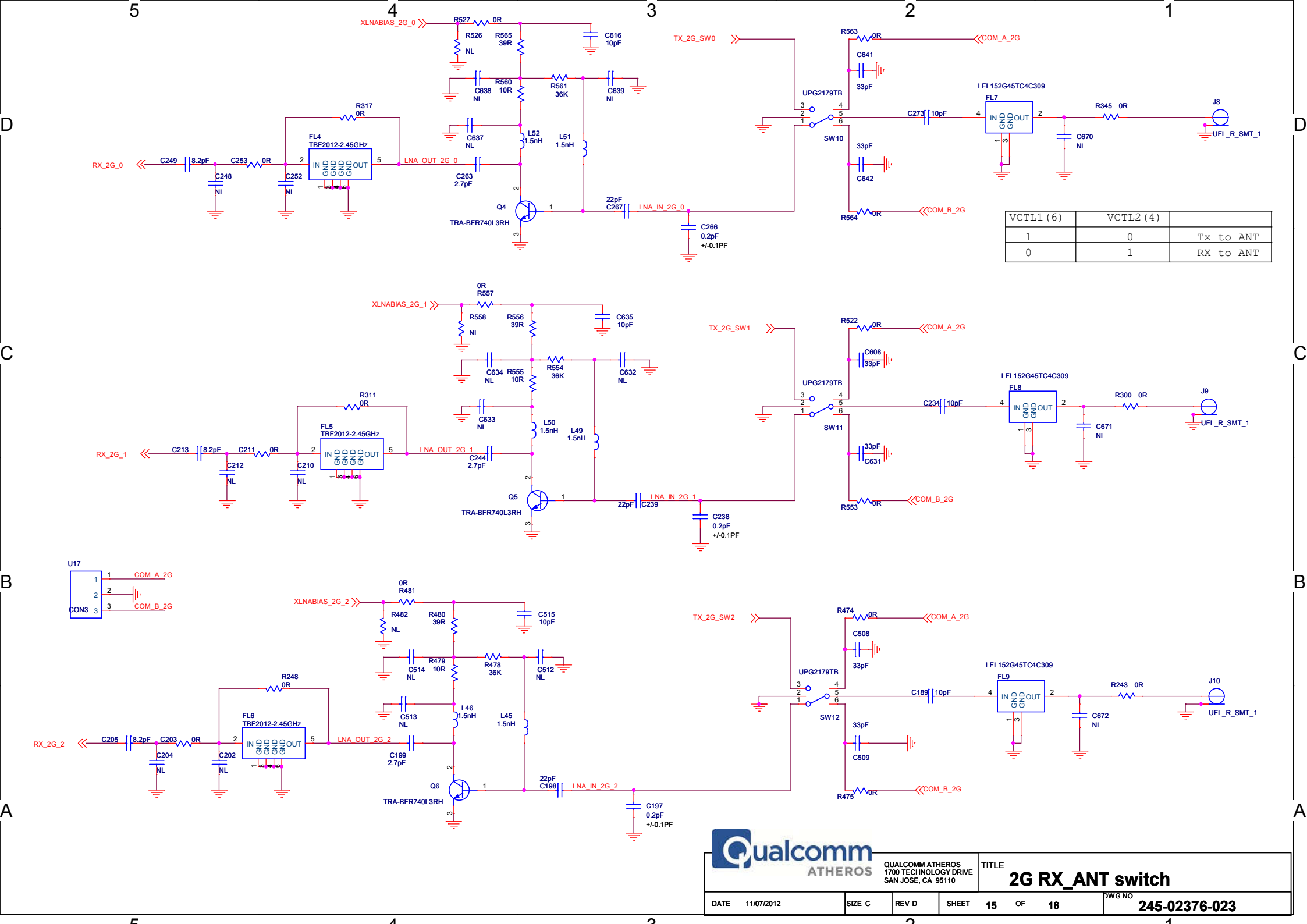
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

TITLE: 2G RF_QCA955x

DATE	SIZE	REV	SHEET	DWG NO
11/07/2012	C	D	14 OF 18	245-02376-023



VCTL1(6)	VCTL2(4)	
1	0	Tx to ANT
0	1	RX to ANT

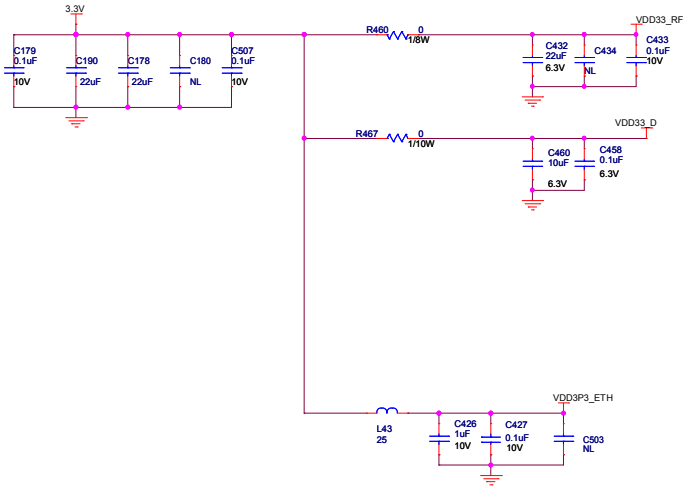
QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

TITLE: 2G RX_ANT switch

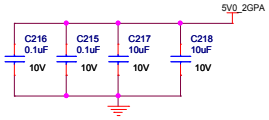
DATE	SIZE	REV	SHEET	DWG NO
11/07/2012	C	D	15 OF 18	245-02376-023

POWER SUPPLY, REGULATORS & DECOUPLING

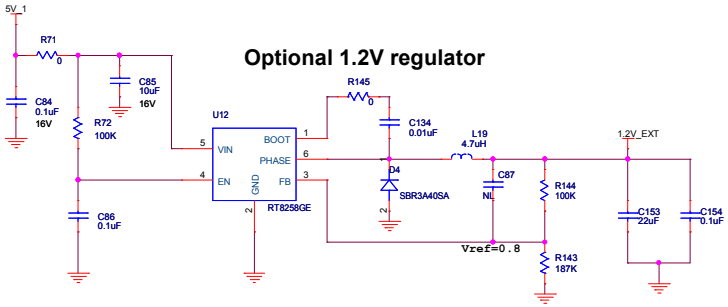
3.3V VOLTAGE DOMAINS

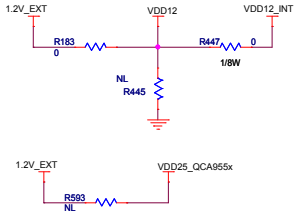


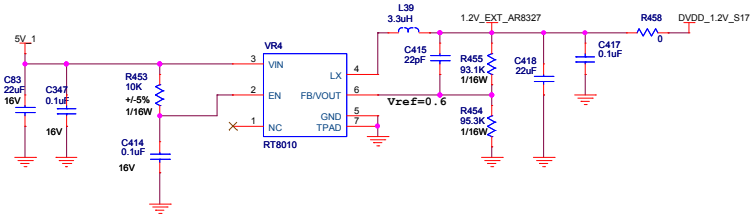
Change R173 to 52.3K and R174 to 12.1K => Vout = 4.2V



Optional 1.2V regulator







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QUALCOMM ATHEROS
1700 TECHNOLOGY DRIVE
SAN JOSE, CA 95110

TITLE: Power regulators

DATE	SIZE	REV	SHEET	DWG NO
<DATE>	C	D	18 OF 18	245-02376-023