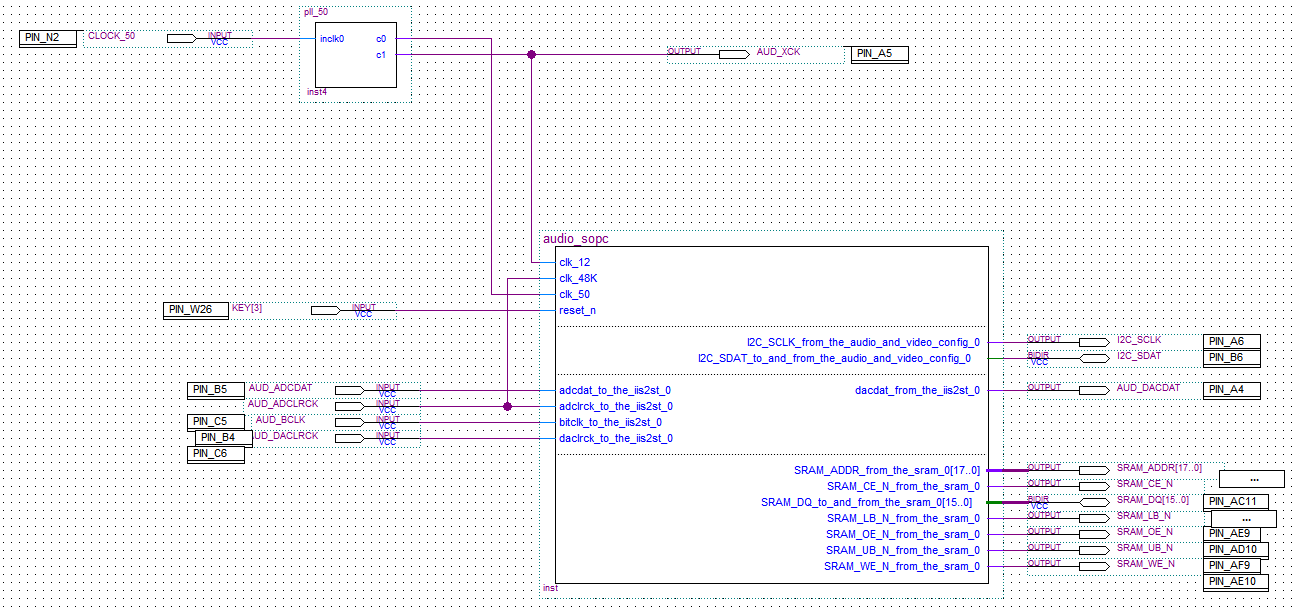
Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)

Audio design using external PLL (archive : sopc_ii2st)

Below is shown a simple version of the design found in the archive sopc_ii2st.arc.



Target

Device Family: Cyclone II

Clock Settings

Name	Source	MHz
clk_50	External	50,0
clk_12	External	12,0
clk_48K	External	1,0

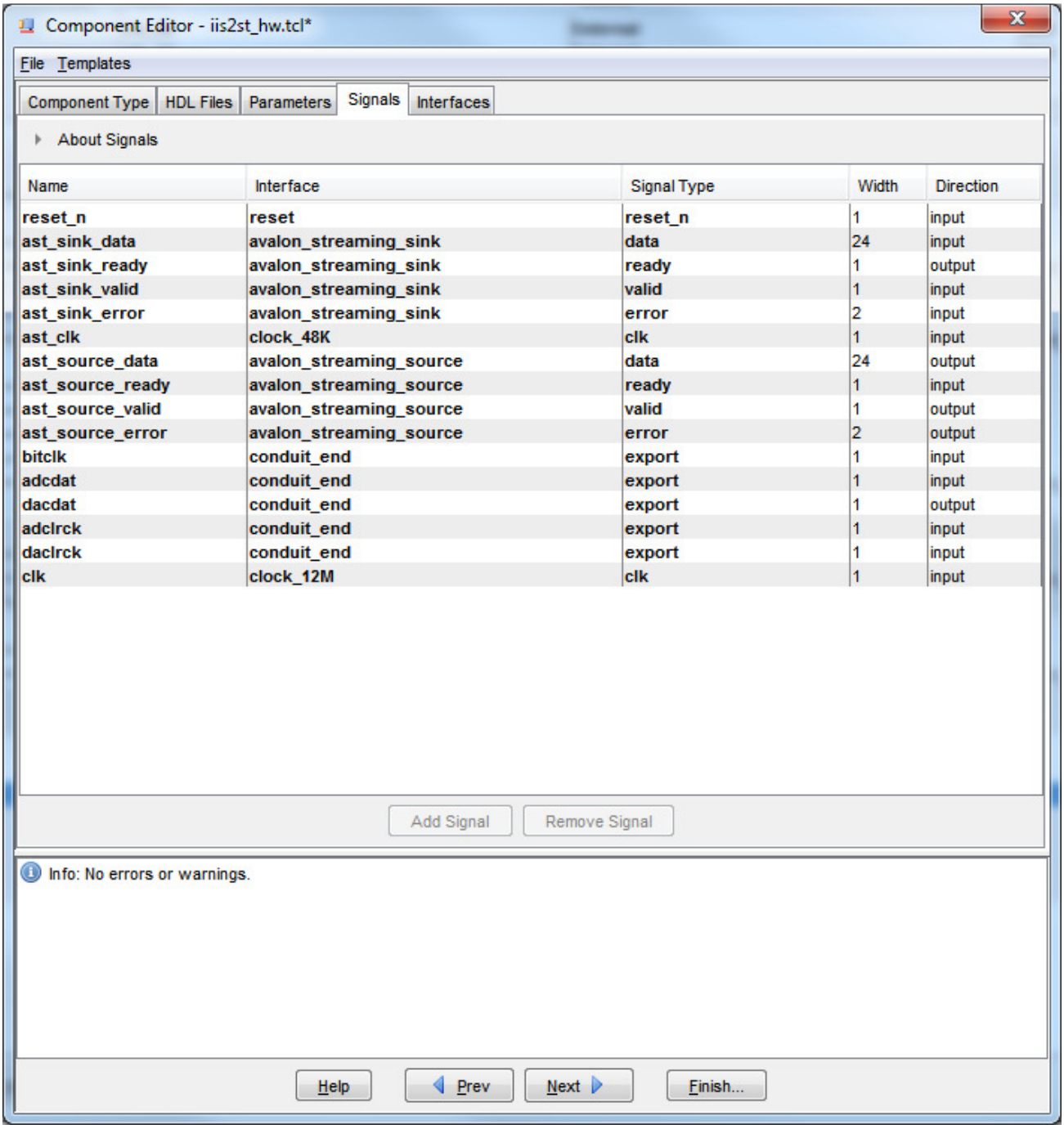
Use	Connections	Name	Description	Clock	Base	End	IRQ	Tags
☑		clk_50	Clock Source					
		clk	Clock Output	clk_50				
☑		audio_and_video_co...	Audio and Video Config					
		clock_reset	Clock Input	clk_50				
		avalon_av_config_slave	Avalon Memory Mapped Slave	[clock_reset]	0x0010_1000	0x0010_100f		
☑		sram_0	SRAM/SSRAM Controller					
		clock_reset	Clock Input	clk_50				
		avalon_sram_slave	Avalon Memory Mapped Slave	[clock_reset]	0x0008_0000	0x000f_ffff		
☑		cpu_0	Nios II Processor					
		clk	Clock Input	clk_50				
		instruction_master	Avalon Memory Mapped Master	[clk]				
		data_master	Avalon Memory Mapped Master	[clk]				
		d_irq	Interrupt Receiver	[clk]	IRQ 0	IRQ 31		
		jtag_debug_module	Avalon Memory Mapped Slave	[clk]	0x0010_0800	0x0010_0fff		
		custom_instruction_m...	Custom Instruction Master					
☑		jtag_uart_0	JTAG UART					
		clk	Clock Input	clk_50				
		avalon_jtag_slave	Avalon Memory Mapped Slave	[clk]	0x0010_1010	0x0010_1017		
		irq	Interrupt Sender	[clk]			0	
☑		sysid	System ID Peripheral					
		clk	Clock Input	clk_50				
		control_slave	Avalon Memory Mapped Slave	[clk]	0x0010_1018	0x0010_101f		
☑		clk_12	Clock Source					
		clk	Clock Output	clk_12				
☑		clk_48K	Clock Source					
		clk	Clock Output	clk_48K				
☑		iis2st_0	iis2st					
		avalon_streaming_sink	Avalon Streaming Sink	[clock_48K]				
		clock_48K	Clock Input	clk_48K				
		avalon_streaming_sou...	Avalon Streaming Source	[clock_48K]				
		clock_12M	Clock Input	clk_12				

Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)

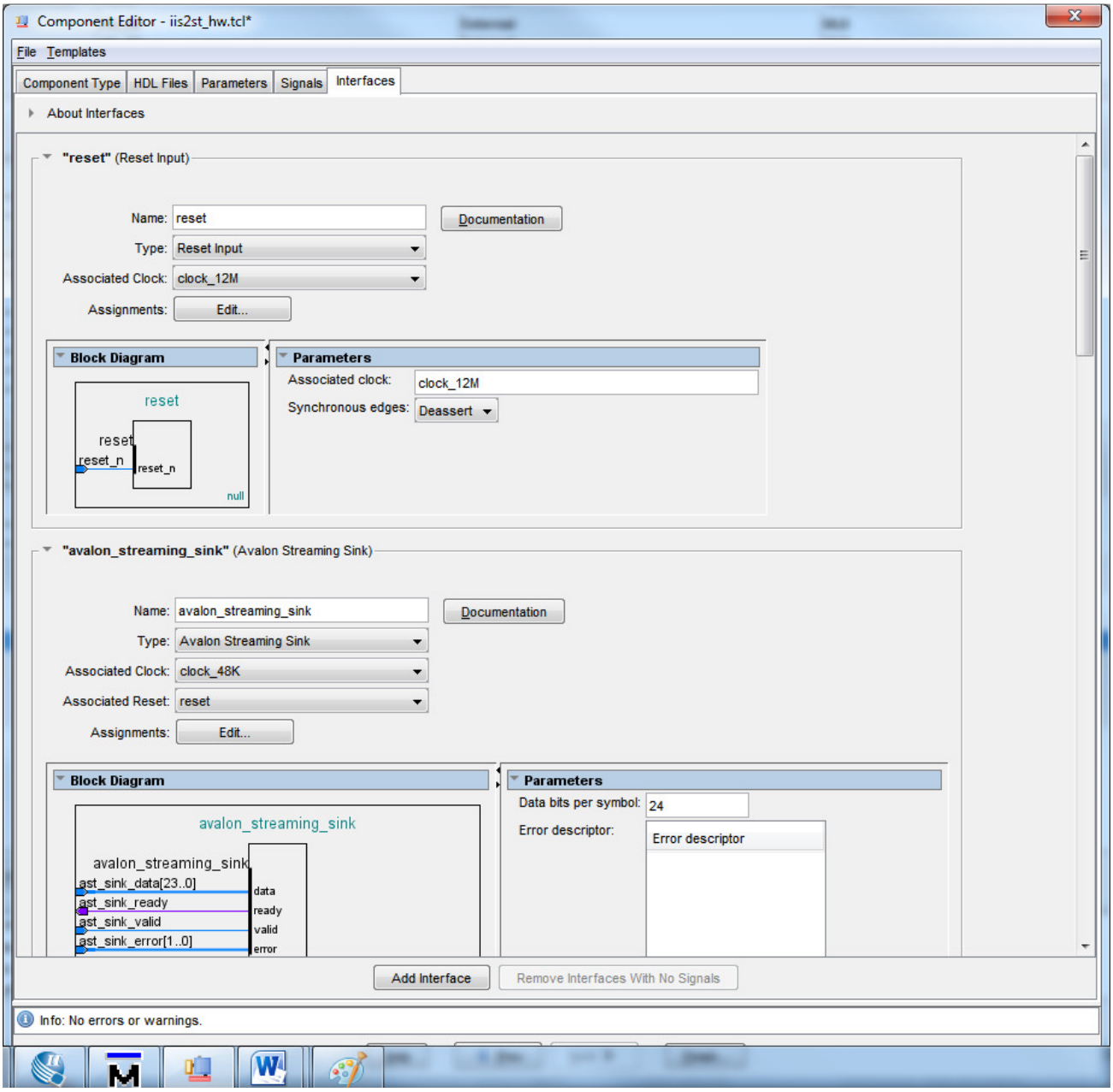
The following guide describes how to configure the iis2st module and inserting it into the SOPC design.

Contents

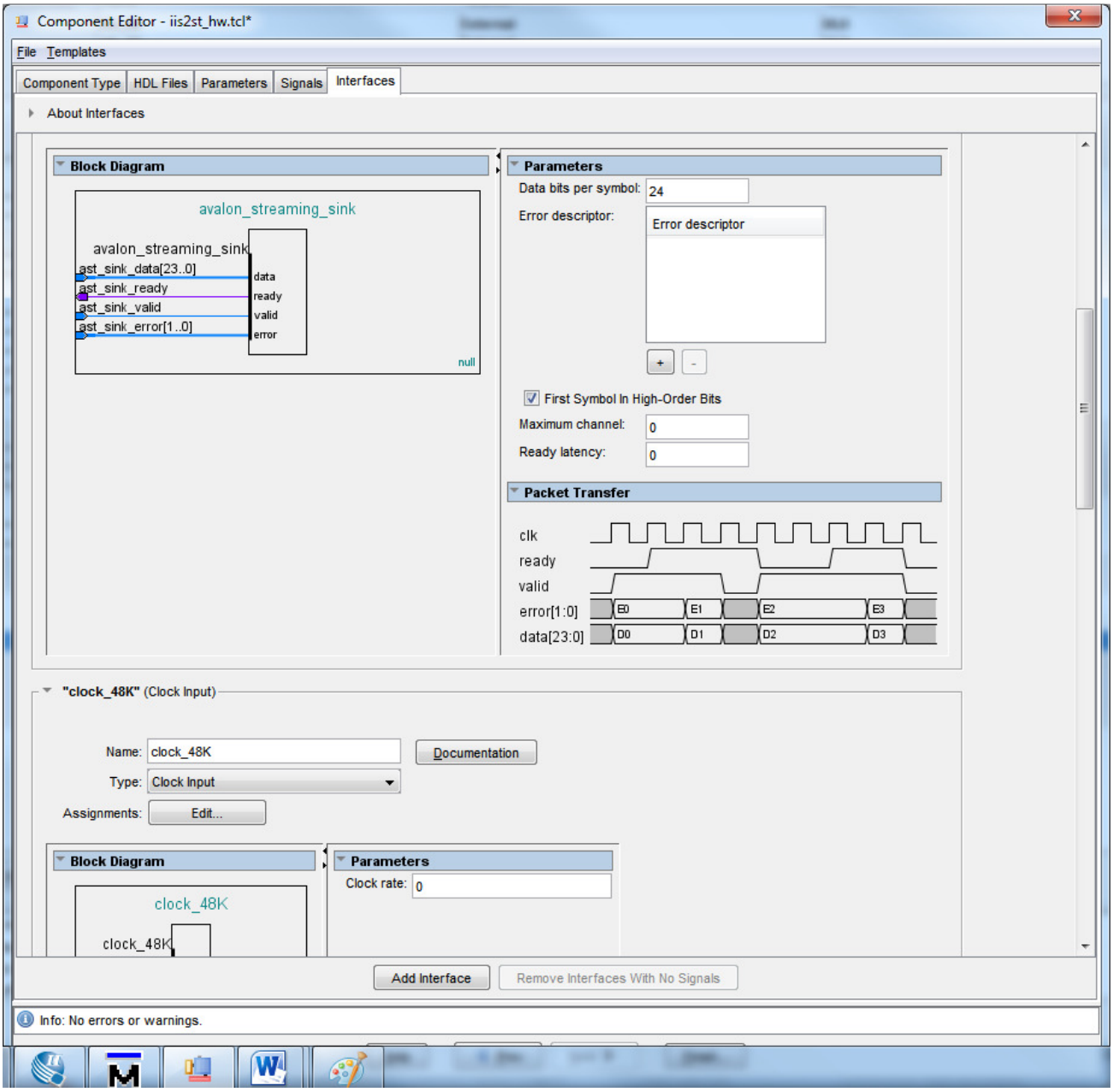
Configuration of component IIS2ST



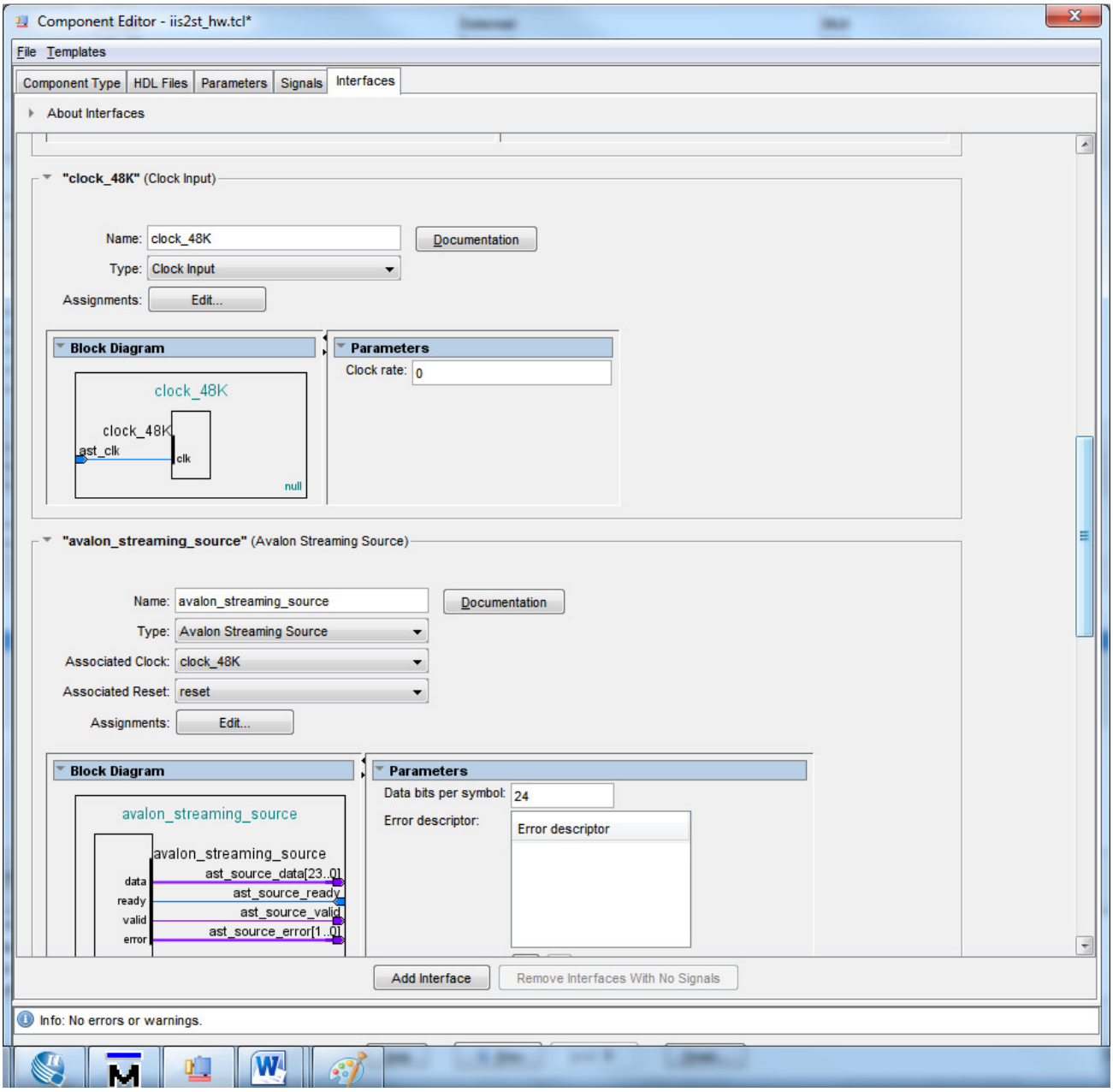
Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)



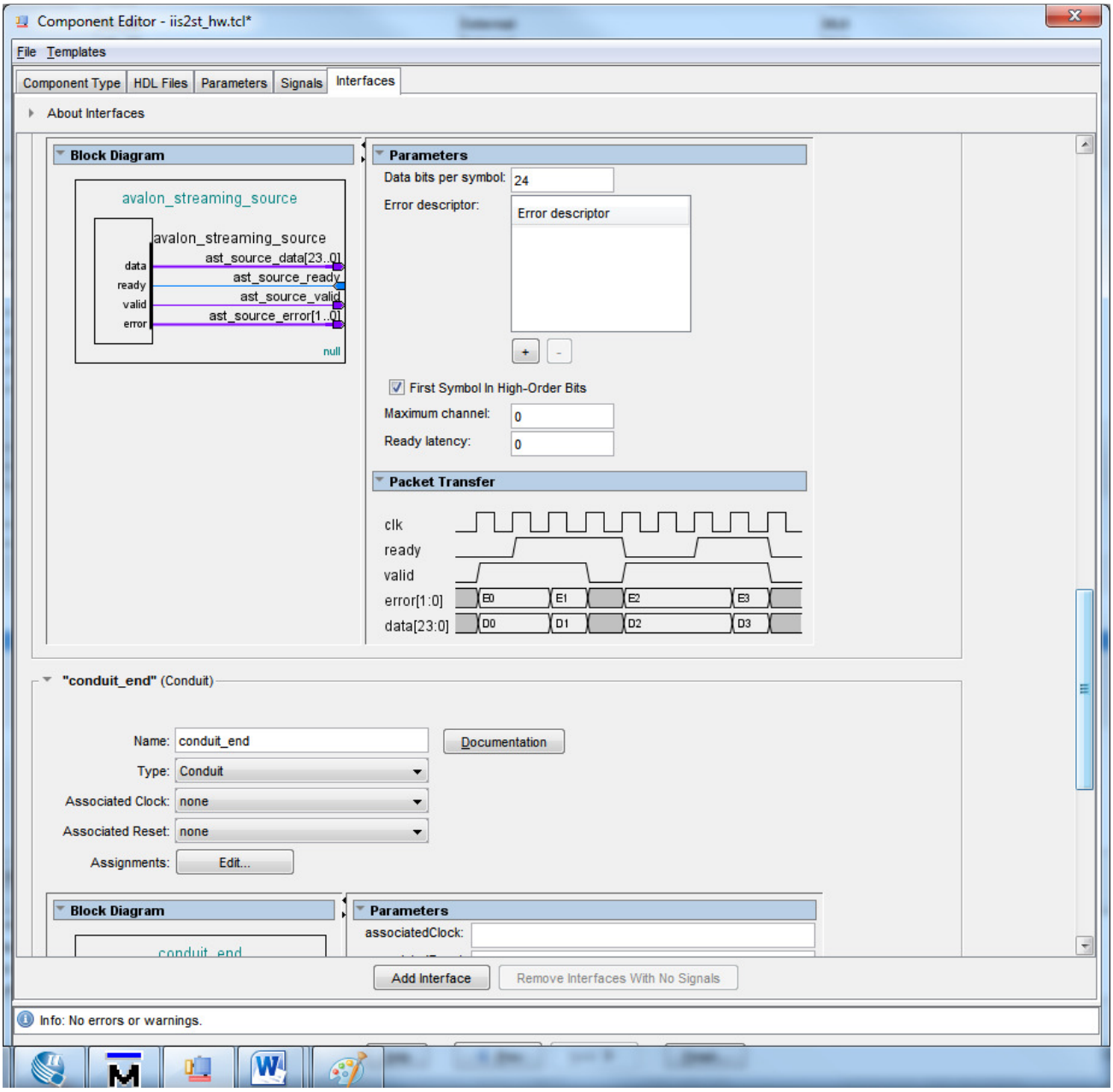
Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)



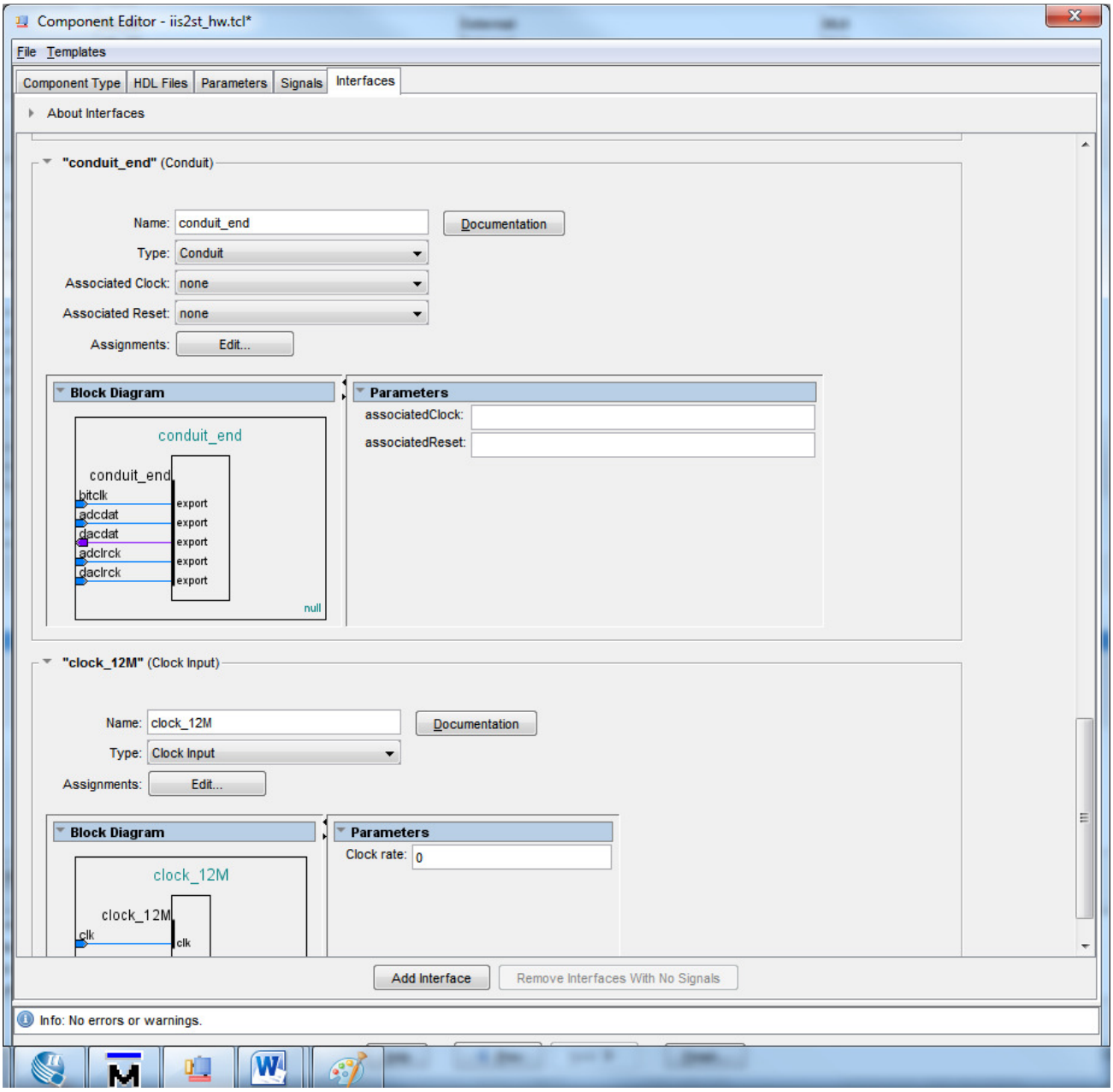
Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)



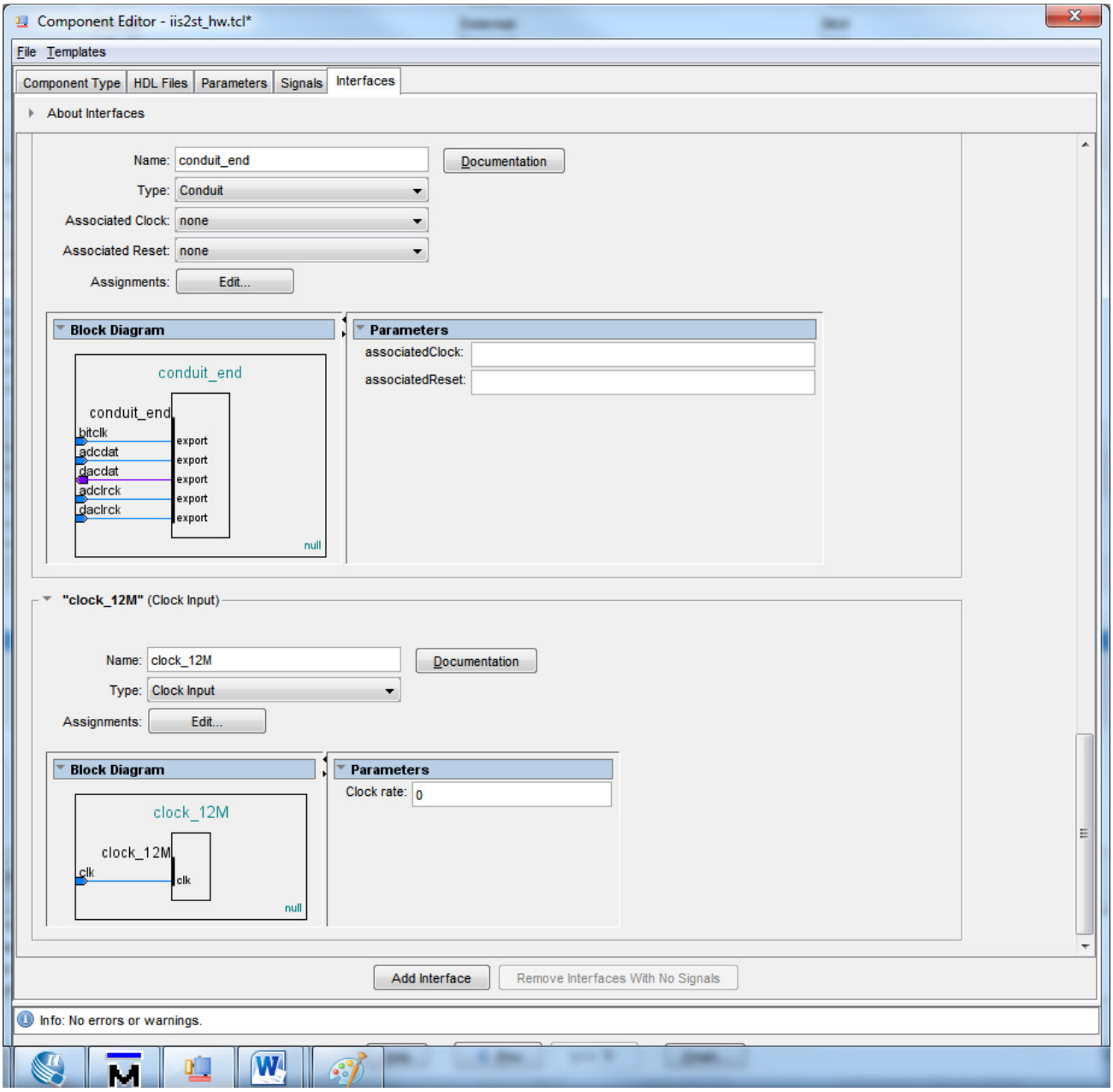
Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)



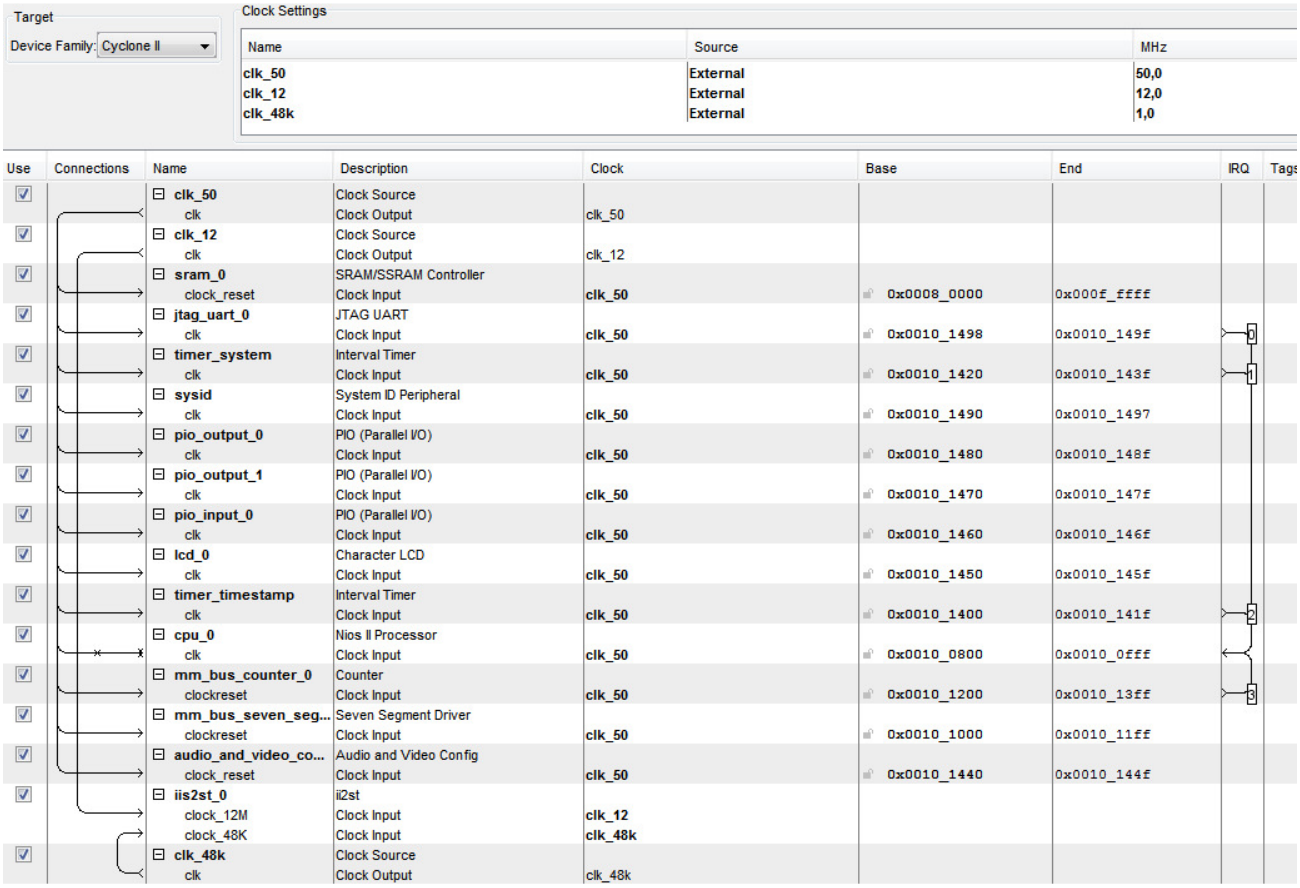
Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)



Quartus Screen dumps for configuration of Audio design using the II2ST component (Exercise 10, ST Bus)



Setting up clock signals in SOPC design



Target

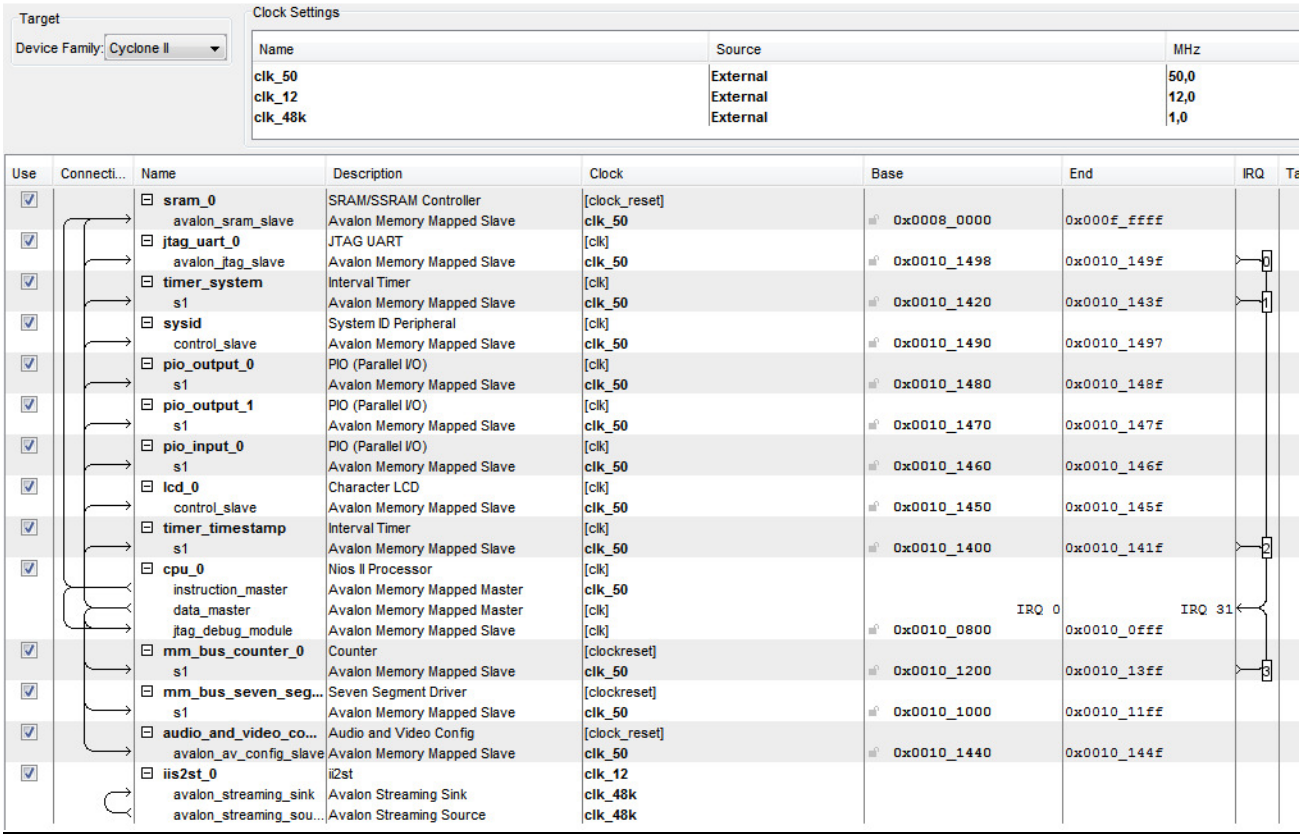
Device Family: Cyclone II

Clock Settings

Name	Source	MHz
clk_50	External	50,0
clk_12	External	12,0
clk_48k	External	1,0

Use	Connections	Name	Description	Clock	Base	End	IRQ	Tags
☑		clk_50	Clock Source					
		clk	Clock Output	clk_50				
☑		clk_12	Clock Source					
		clk	Clock Output	clk_12				
☑		sram_0	SRAM/SSRAM Controller					
		clock_reset	Clock Input	clk_50	0x0008_0000	0x000f_ffff		
☑		jtag_uart_0	JTAG UART					
		clk	Clock Input	clk_50	0x0010_1498	0x0010_149f	0	
☑		timer_system	Interval Timer					
		clk	Clock Input	clk_50	0x0010_1420	0x0010_143f	1	
☑		sysid	System ID Peripheral					
		clk	Clock Input	clk_50	0x0010_1490	0x0010_1497		
☑		pio_output_0	PIO (Parallel I/O)					
		clk	Clock Input	clk_50	0x0010_1480	0x0010_148f		
☑		pio_output_1	PIO (Parallel I/O)					
		clk	Clock Input	clk_50	0x0010_1470	0x0010_147f		
☑		pio_input_0	PIO (Parallel I/O)					
		clk	Clock Input	clk_50	0x0010_1460	0x0010_146f		
☑		lcd_0	Character LCD					
		clk	Clock Input	clk_50	0x0010_1450	0x0010_145f		
☑		timer_timestamp	Interval Timer					
		clk	Clock Input	clk_50	0x0010_1400	0x0010_141f	2	
☑		cpu_0	Nios II Processor					
		clk	Clock Input	clk_50	0x0010_0800	0x0010_0fff		
☑		mm_bus_counter_0	Counter					
		clockreset	Clock Input	clk_50	0x0010_1200	0x0010_13ff	3	
☑		mm_bus_seven_seg...	Seven Segment Driver					
		clockreset	Clock Input	clk_50	0x0010_1000	0x0010_11ff		
☑		audio_and_video_co...	Audio and Video Config					
		clock_reset	Clock Input	clk_50	0x0010_1440	0x0010_144f		
☑		iis2st_0	i2st					
		clock_12M	Clock Input	clk_12				
		clock_48K	Clock Input	clk_48k				
☑		clk_48k	Clock Source					
		clk	Clock Output	clk_48k				

Setting up MM and ST bus in SOPC design



Target

Device Family: Cyclone II

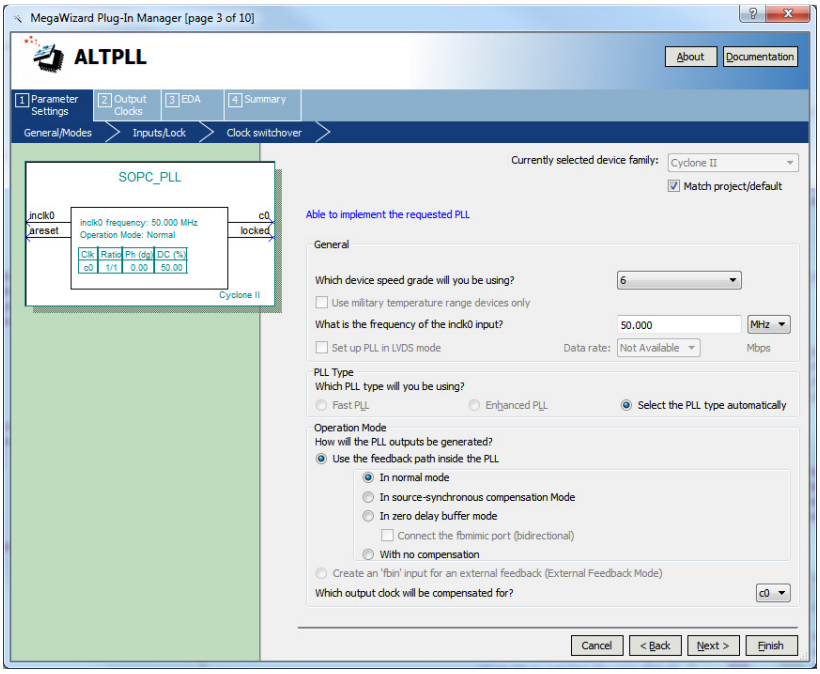
Clock Settings

Name	Source	MHz
clk_50	External	50,0
clk_12	External	12,0
clk_48k	External	1,0

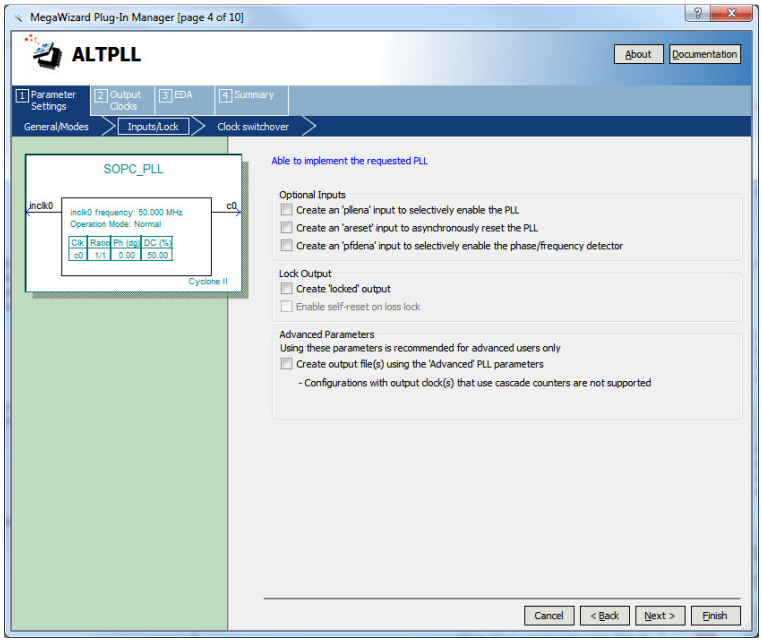
Use	Connecti...	Name	Description	Clock	Base	End	IRQ
☑		sram_0	SRAM/SSRAM Controller	[clock_reset]			
		avalon_sram_slave	Avalon Memory Mapped Slave	clk_50	0x0008_0000	0x000f_ffff	
☑		jtag_uart_0	JTAG UART	[clk]			
		avalon_jtag_slave	Avalon Memory Mapped Slave	clk_50	0x0010_1498	0x0010_149f	0
☑		timer_system	Interval Timer	[clk]			
		s1	Avalon Memory Mapped Slave	clk_50	0x0010_1420	0x0010_143f	1
☑		sysid	System ID Peripheral	[clk]			
		control_slave	Avalon Memory Mapped Slave	clk_50	0x0010_1490	0x0010_1497	
☑		pio_output_0	PIO (Parallel I/O)	[clk]			
		s1	Avalon Memory Mapped Slave	clk_50	0x0010_1480	0x0010_148f	
☑		pio_output_1	PIO (Parallel I/O)	[clk]			
		s1	Avalon Memory Mapped Slave	clk_50	0x0010_1470	0x0010_147f	
☑		pio_input_0	PIO (Parallel I/O)	[clk]			
		s1	Avalon Memory Mapped Slave	clk_50	0x0010_1460	0x0010_146f	
☑		lcd_0	Character LCD	[clk]			
		control_slave	Avalon Memory Mapped Slave	clk_50	0x0010_1450	0x0010_145f	
☑		timer_timestamp	Interval Timer	[clk]			
		s1	Avalon Memory Mapped Slave	clk_50	0x0010_1400	0x0010_141f	2
☑		cpu_0	Nios II Processor	[clk]			
		instruction_master	Avalon Memory Mapped Master	clk_50			
		data_master	Avalon Memory Mapped Master	[clk]			IRQ 0 / IRQ 31
		jtag_debug_module	Avalon Memory Mapped Slave	[clk]	0x0010_0800	0x0010_0fff	
☑		mm_bus_counter_0	Counter	[clockreset]			
		s1	Avalon Memory Mapped Slave	clk_50	0x0010_1200	0x0010_13ff	3
☑		mm_bus_seven_seg...	Seven Segment Driver	[clockreset]			
		s1	Avalon Memory Mapped Slave	clk_50	0x0010_1000	0x0010_11ff	
☑		audio_and_video_co...	Audio and Video Config	[clock_reset]			
		avalon_av_config_slave	Avalon Memory Mapped Slave	clk_50	0x0010_1440	0x0010_144f	
☑		iis2st_0	ii2st	clk_12			
		avalon_streaming_sink	Avalon Streaming Sink	clk_48k			
		avalon_streaming_sou...	Avalon Streaming Source	clk_48k			

Configuration of PLL

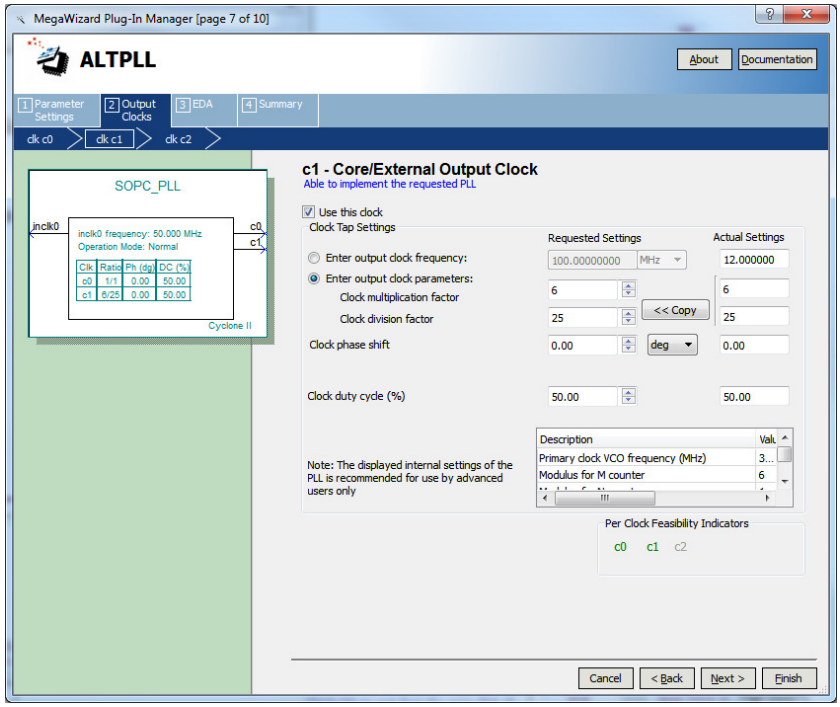
1. Start the MegaWizard Plug-In Manager
2. Create a new custom megafunction
3. Search for the ALTPLL select it and name it SOPC_PLL create it as a VHDL instance and press next
4. Set the input clock to 50 Mhz



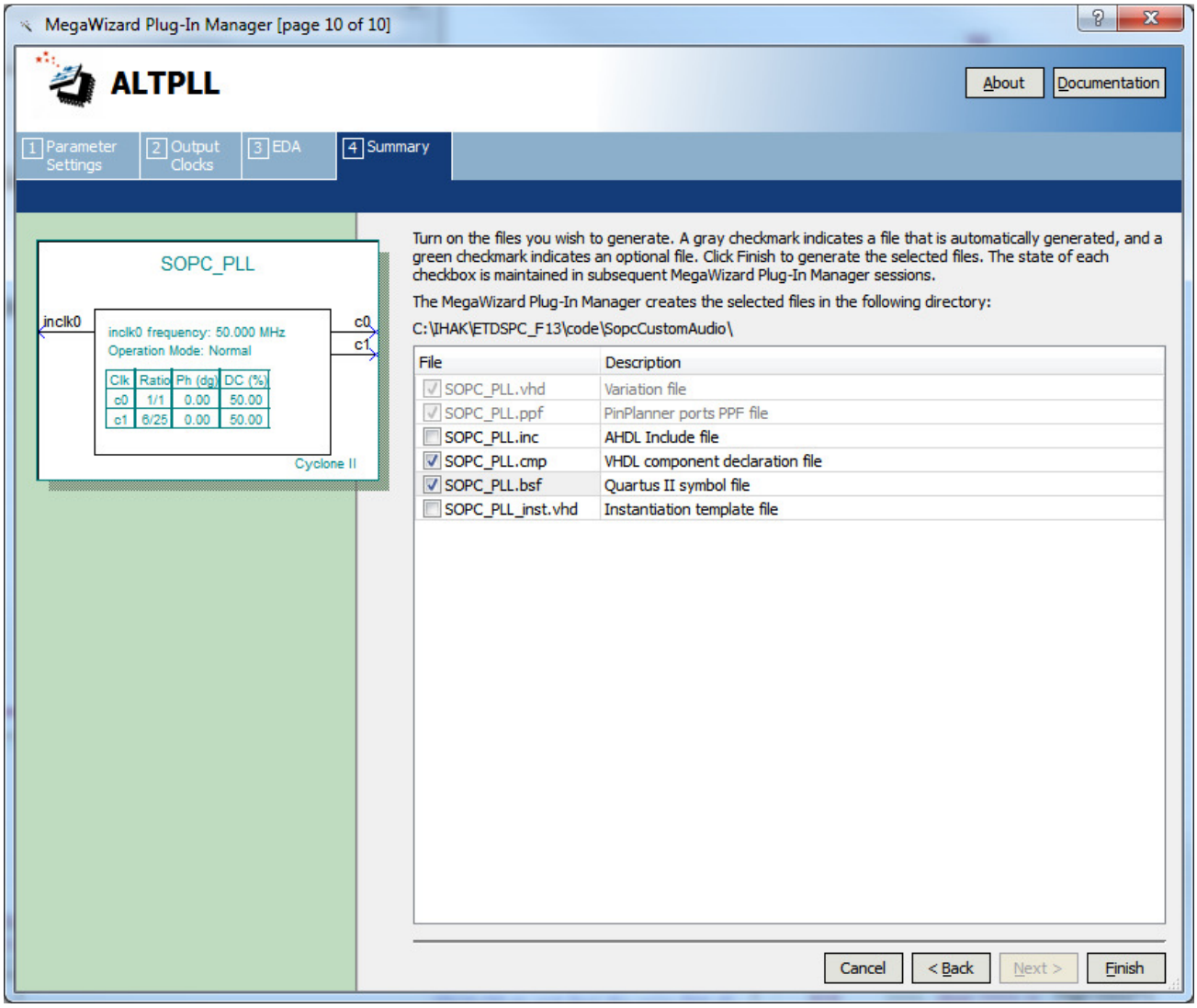
5. Unmark to create a ‘areset’ input and ‘locked’ output



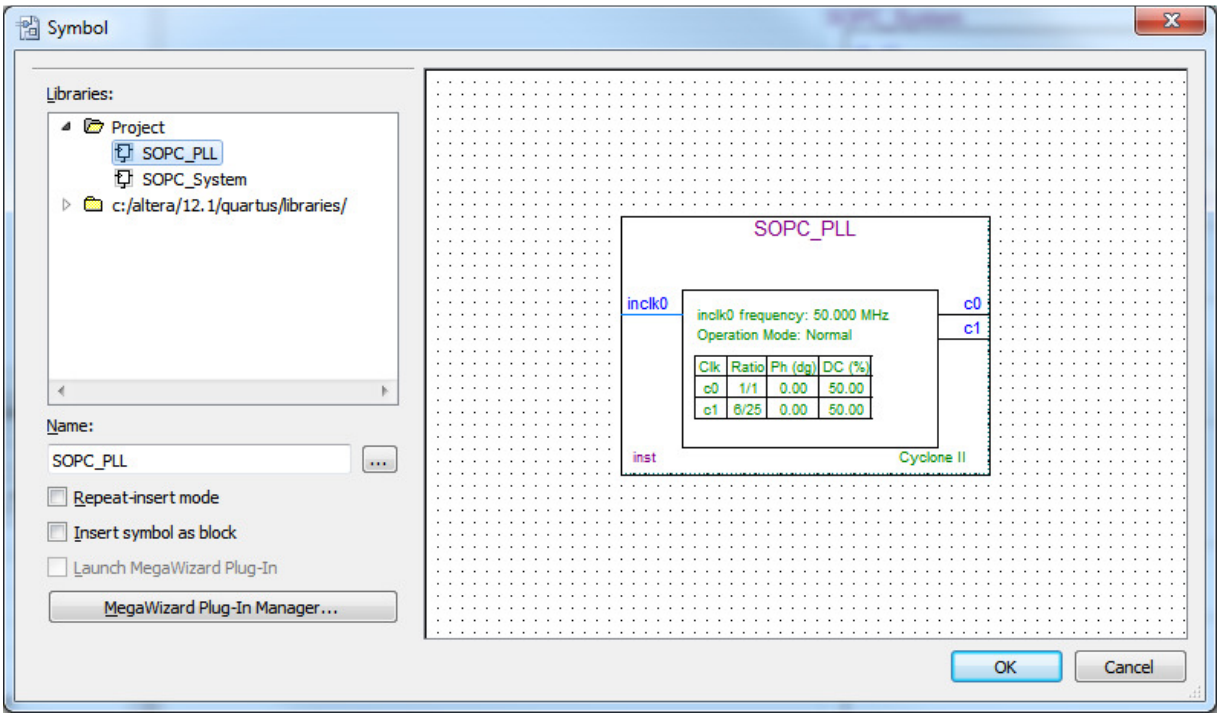
6. Create a second clock output c1 setting the multiplication factor to 6 and division factor to 25.



Finally select to create a ***Quartus II symbol file*** and press finish



Insert the new PLL symbol into the design



SOPC Design with PLL and SOPC system and pin connections