RMIT University Vietnam

School of Science and Technology (SST)

EEET2600 – Electronics

BJT AMPLIFIER DESIGN

Lecturer: Mr. Thanh Pham

Team Members:

Student 1 (Nguyen Huynh Hai Long) (S3877624)

Student 2 (Hoang Thai Kiet) (S3855250)

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CIRCUIT 1 – ANALYZING SINGLE-STAGE AMPLIFIER

In this following task, we will be analyzing as well as designing a suitable circuit from the provided BJT Amplifier schematic through the usage of Multisim Simulation and Elvis Build. From the given circuit of the single-stage amplifier, we would first analyze the DC bias of the circuit and determine the Q-point values.

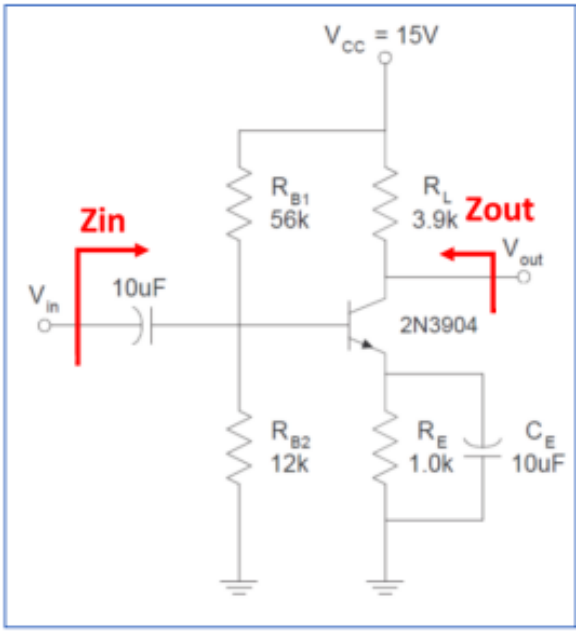


Figure 1. The schematic of the provided single-stage amplifier

1.1.DC Analysis (1.5 pages max)

We determine the values of the Q-point (I_{CEQ} and V_{CEQ}) by applying the equations:

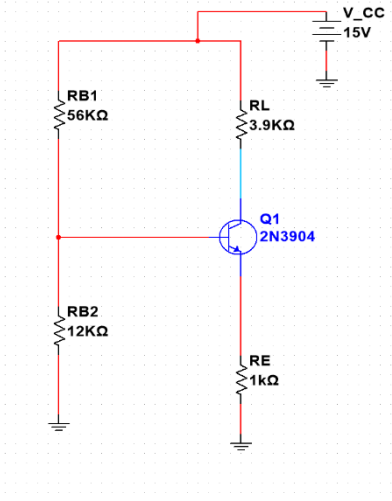


Figure 2. The schematic of DC bias in circuit 1

$$I_{C(sat)} = \frac{Vcc}{Rc} = \frac{15\,V}{3.9\,k\Omega} = 3.896\,mA$$

$$V_{TH} = V_{BE} = 0.7\,V \text{ (Assuming the BJT is in Active mode)}$$

$$V_B = \frac{R_2}{R_2 + R_1} \times V_{cc} = \frac{12\,k\Omega}{12\,k\Omega + 56\,k\Omega} \times 15\,V$$

$$= 2.647\,V\ (Apply\ Voltage\ Divider\ Rule)$$

$$V_E = V_B - V_{BE} = 2.647\,V - 0.7\,V = 1.947\,V$$

$$I_E = \frac{V_E - 0}{R_E} = \frac{1.947\,V}{1.0\,k\Omega} = 1.947\,mA$$

$$I_E = I_B + I_C = \frac{1}{\beta} I_C + I_C \Rightarrow I_C = \left(\frac{\beta}{\beta + 1}\right) \times I_E = \frac{100}{100 + 1} \times 1.947\ mA = 1.928\ mA$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 15\ V - (1.928\ mA \times 3.9\ k\Omega) - (1.947\ mA \times 1.0\ k\Omega) = 5.534\ V$$

$$\Rightarrow Q(I_{CQ}, V_{CEQ}) = (1.928\ mA, 5.534\ V).$$

Draw the Q point together with the DC load line. From there determine the maximum output swing from the graph:

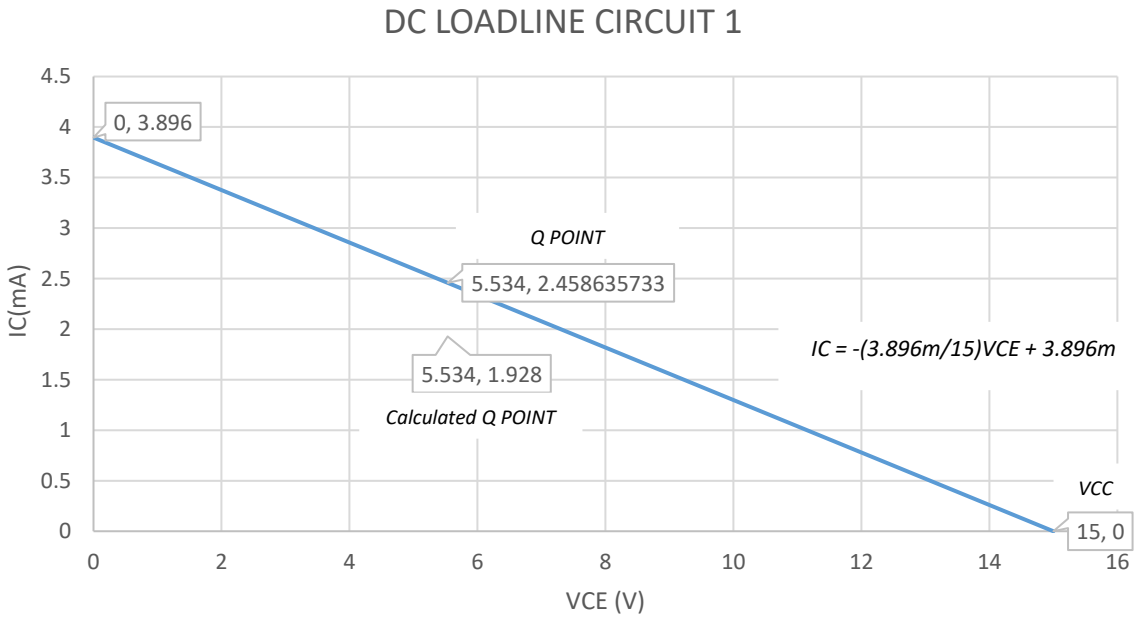


Figure 3. DC load line of circuit 2 and its Q point. 'm' = 10^{-3}

By looking at the DC load line graph, we observe that the actual Q point in circuit 1 is Q (2.458635733mA, 5.534V by substituting VCE = 5.534V to the equation IC, which is evaluated from the coordinates of IC saturation and VCC. To guarantee its maximum output swing, VCE is foreseen to oscillate in a range: $0 < VCE \leq 2 * VCEQ = 5.534 * 2 = 11.068$, if the VCE maximum output swing is larger than 11.068, the left wing will be clipped as it exceeds the cutoff point. Similarly, if the maximum output swing is larger than VCC=9V, VCE will experience both its sides clipped. As a result, the maximum output swing is 11.068.

1.2.AC Analysis (2 pages max)

With values of the Q-point from the DC Analysis, we continued by calculating the h-parameters for small-signal models:

$$g_m = \frac{I_C}{V_T} = \frac{1.928\,mA}{25\,mV} = 0.07712$$

$$Input\ resistance\ r_\pi = \frac{\beta_0}{I_C} \times V_T = \frac{100}{1.928\,mA} \times 25\,mV = 1296.680\,\Omega = 1.297\,k\Omega$$

$$Output\ resistance\ r_0 = \frac{V_A + V_{CE}}{I_C} = \frac{75\,V + 5.534\,V}{1.928\,mA} = 41.770\,k\Omega$$

Then draw the small-signal circuit below:

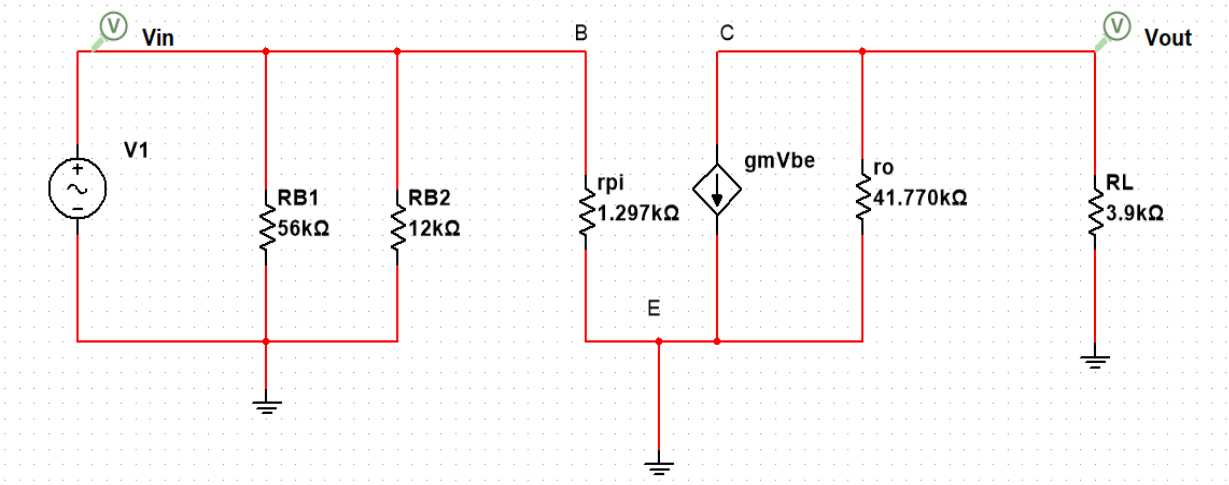


Figure 4. Hybrid-pi model of small signal circuit 1.

Utilizing the circuit above from figure., we applied the values from previous DC Analysis and h-parameters into the formulas of:

- Gain

$$A_v = \frac{V_0}{V_{BE}} = \frac{V_0}{V_{in}} = -g_m\left(\frac{R_L \times R_0}{R_L + R_0}\right) = -0.07712 \times \left(\frac{3.9\,k\Omega \times 41.770\,k\Omega}{3.9\,k\Omega + 41.770\,k\Omega}\right) = -275.084$$

- Zin

$$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1} + R_{B2}} = \frac{(56\,k\Omega \times 12\,k\Omega)}{(56\,k\Omega + 12\,k\Omega)} = 9882.353\,\Omega = 9.882\,k\Omega$$

$$Z_{in} = \frac{R_B \times R_\pi}{R_B + R_\pi} = \frac{(9.882\,k\Omega \times 1.297\,k\Omega)}{(9.882\,k\Omega + 1.297\,k\Omega)} = 1146.520\,\Omega$$

- Zout

$$Z_{out} = \left(\frac{R_L \times R_0}{R_L + R_0}\right) = \left(\frac{3.9\ k\Omega \times 41.770\ k\Omega}{3.9\ k\Omega + 41.770\ k\Omega}\right) = 3566.959\ \Omega$$

1.3. Simulating Circuit (2 pages max)

In this section, you need to build and show the schematic that you built in the Multisim

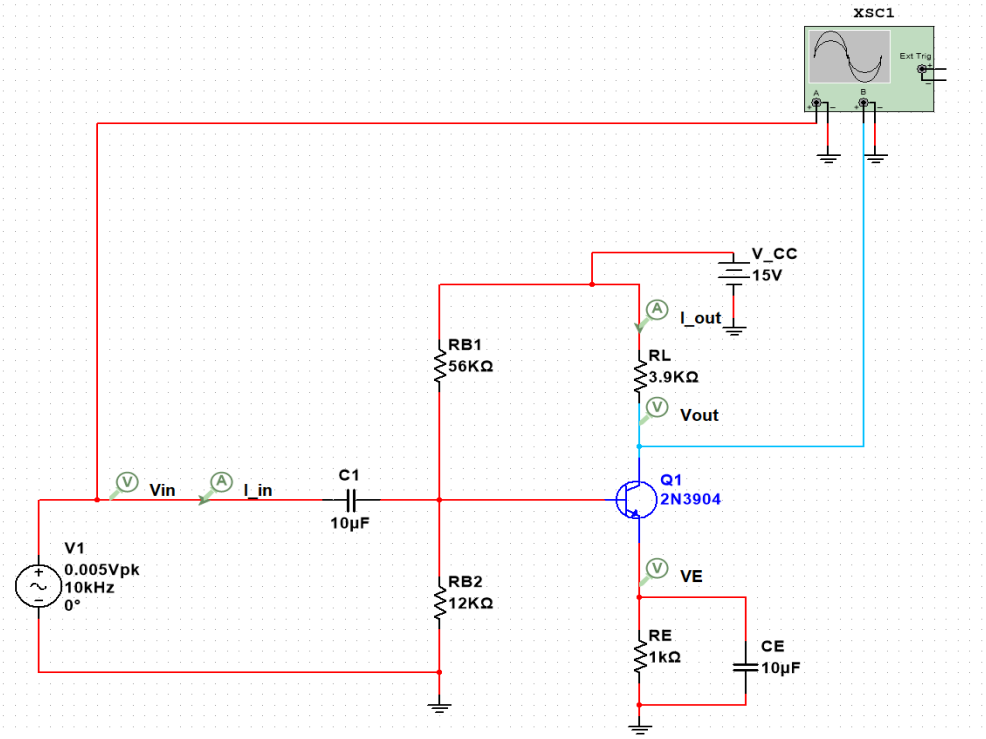


Figure 5. The schematic of the single-stage amplifier in NI Multisim (Circuit 1)

The AC Voltage supply is adjusted to have Vpp = 0.005V and frequency = 10k Hz (including for the Single Frequency AC). By doing so, the risks of clipped voltage waveform when we run oscilloscope is reduced significantly. Moreover, we observed the values with nearly the same as the ones in the calculation and Multisim simulation. Same doing is applied in circuit 2 design.

The DC simulation:

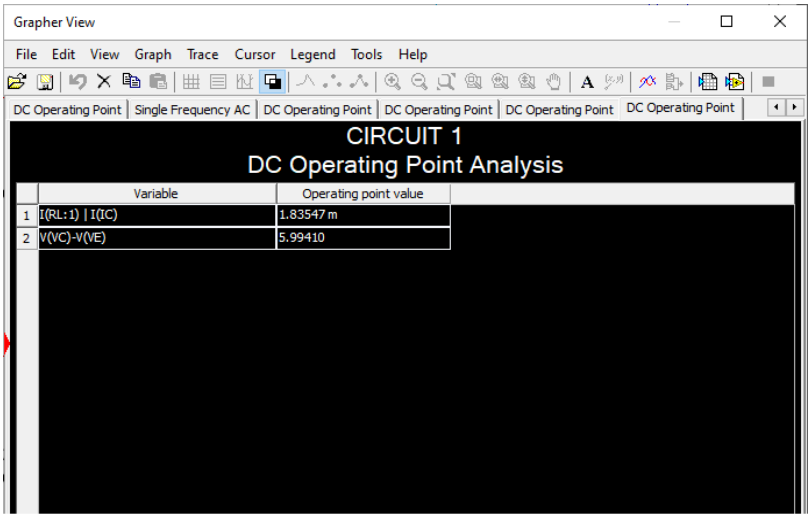


Figure 6. The Q-point (ICQ = 1.835 mA, VCEQ = 5.994 V) values obtained from NI Multisim (Circuit 1)

The AC simulation:

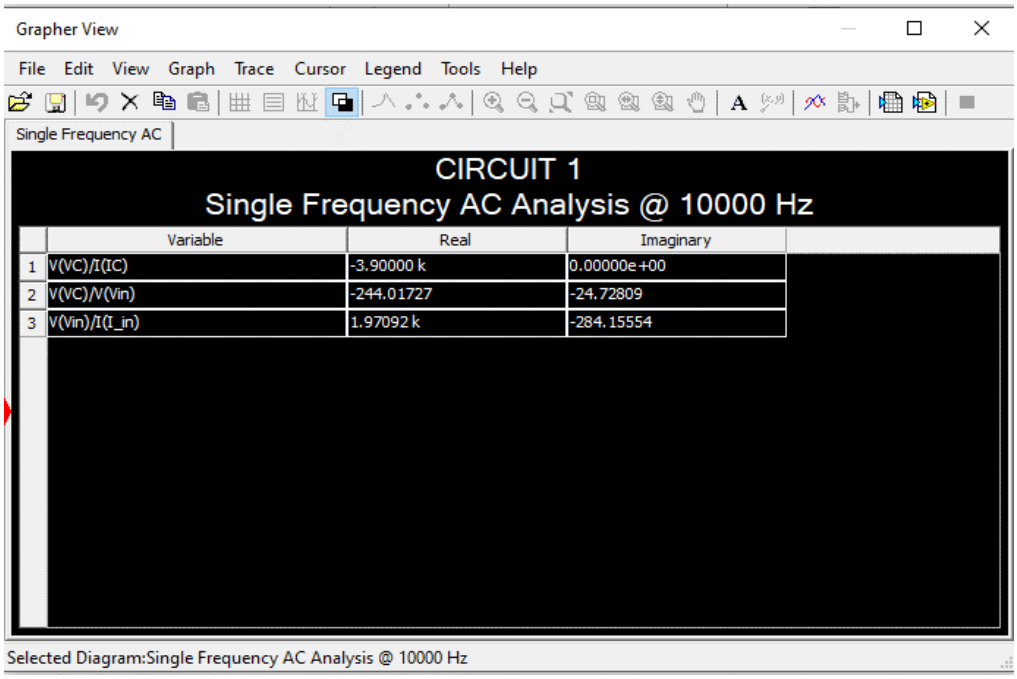


Figure 7. Voltage gain and input/output impedances from circuit in NI Multisim (Circuit 1)

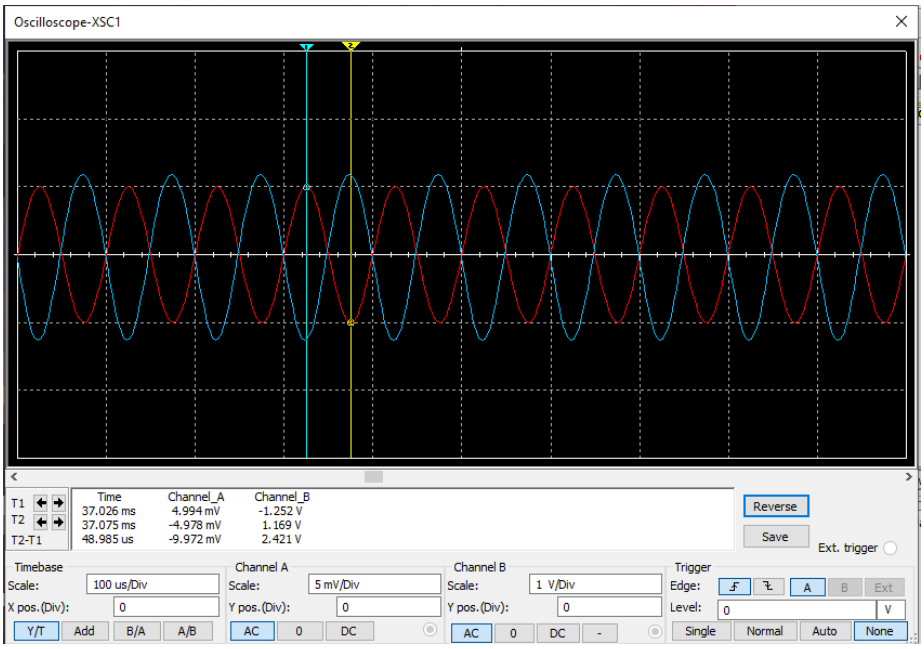


Figure 8. Voltage gain displayed in Oscilloscope of circuit 2 in Multisim. The blue curve indicates VC (V output) while the red one is the Voltage source.

$$A_V = \frac{-1.252\ \text{V}}{4.994\ \text{mV}} = -253.236$$

1.4. Building circuit (2 pages max)

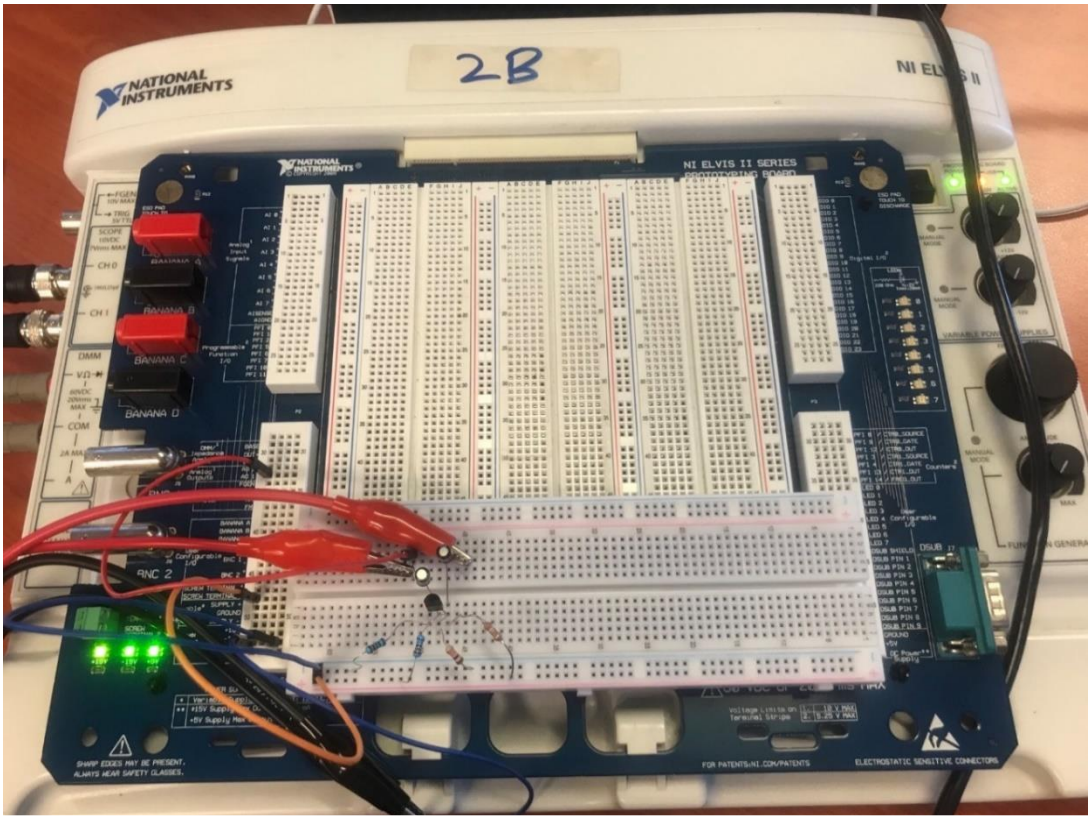


Figure 9. The circuit design implementation of the single-stage amplifier on Elvis Board II (Circuit 1)

Measure DC:

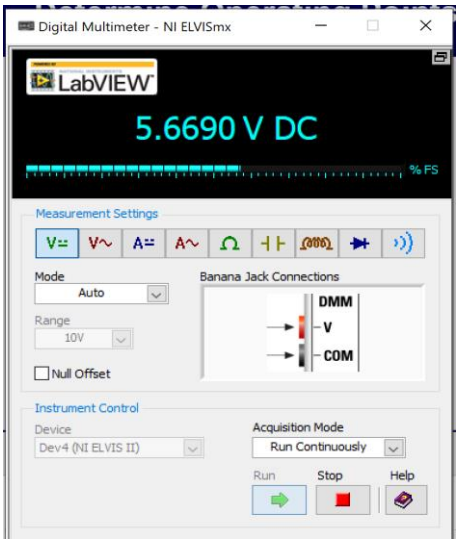


Figure 10. VCE measured value from circuit 1 on Elvis board.

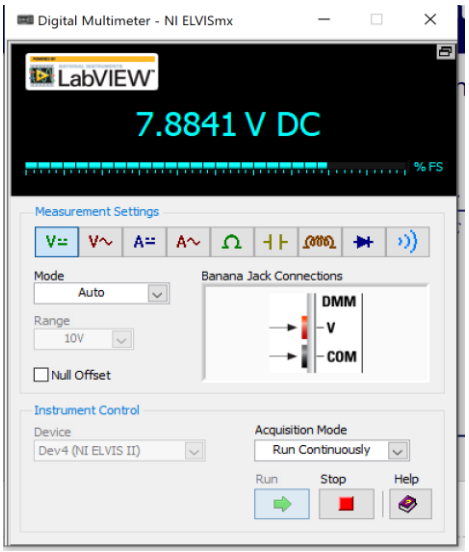


Figure 11. VC measured value from circuit 1 on Elvis board.

Measure AC:

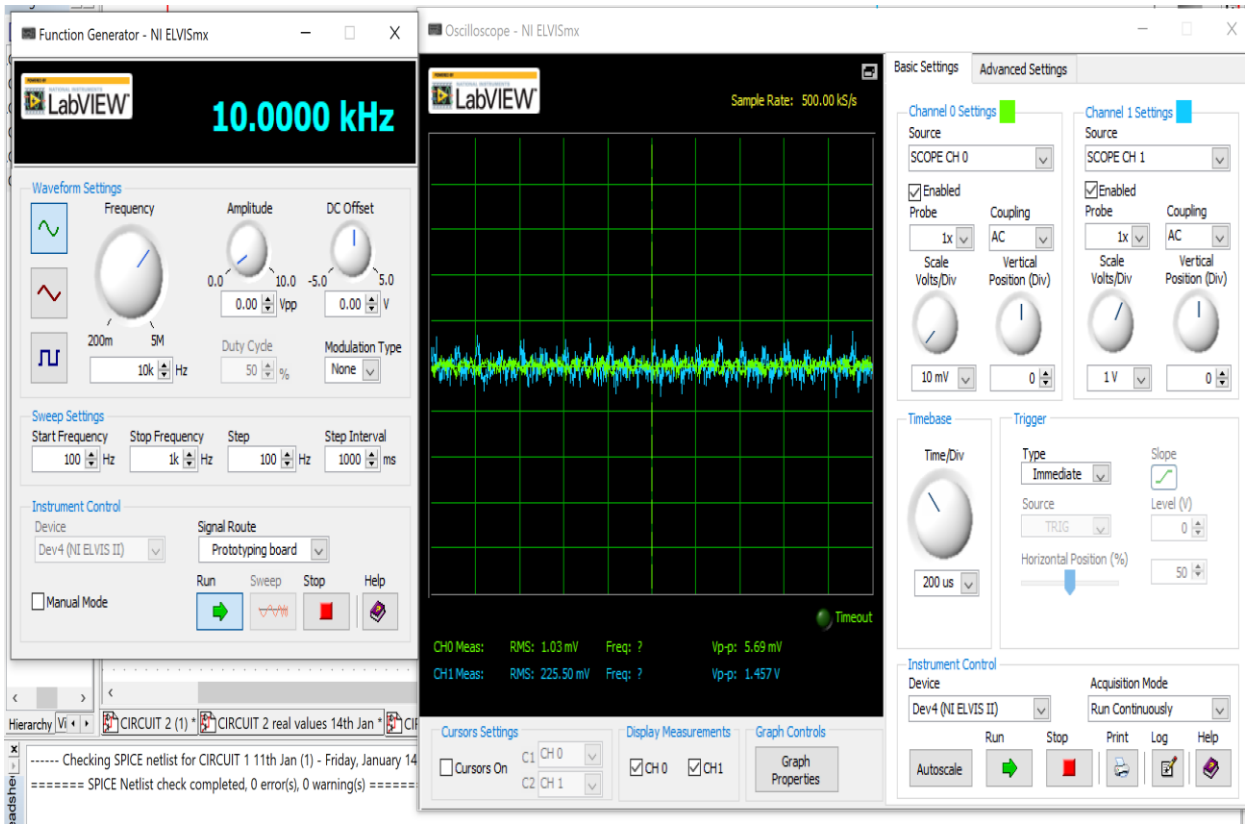


Figure 12. Voltage gain of circuit 1 measured by inspecting on the oscilloscope from Elvis board II. The Blue signal indicates the output while the Green signal is the input

$$A_V = \frac{1.457\ V}{5.69\ mV} = 256.063$$

Measure components' values: **[APPENDIX 1].**

Measure Input/Output Impedances: **[APPENDIX 2].**

1.5. Discussion (1-page max)

	Manual Calculation	Simulation	Build	Percentage Difference between Calculation vs. Simulation	Percentage difference between Calculation vs. Build

DC – Q-point	(I_{CQ}): 1.928mA (V_{CEQ}): 5.334V Max output swing(MOS): 11.068V	(I_{CQ}): 1.835mA (V_{CEQ}): 5.994V (MOS): 5.994*2=11.988	(I_{CQ}): 2.032mA (V_{CEQ}): 5.669V (MOS): 5.669*2=11.338	(I_{CQ}): 4.824 % (V_{CEQ}): 12.373% (MOS): 8.312%	(I_{CQ}): 5.394 % (V_{CEQ}): 6.280% (MOS): 2.891%
AC – A_v	-275.084	-244.017	256.063	11.294 %	6.915 %
AC – Z_{in}	1146.520 Ω	1970.920 Ω	1093.629 Ω	71.905 %	4.613 %
AC – Z_{out}	3566.959 Ω	-3900 Ω	3534.881 Ω	9.337 %	0.899 %

Table 1. Result table of Calculation Vs Simulation Vs Build, along with the percentage difference between each value (Circuit 1)

$$\%\ Difference = \left|1 - \frac{Simulated\ Multisim\ Value\ or\ Elvis\ Board\ Value}{Manual\ Calculated\ Value}\right| \times 100\%$$

Overall, the analysis and the implementation of building the given first-stage amplifier went indisputably as the circuit design includes all of the required components needed in the schematic and were able to obtain results from both Multisim Simulation and Elvis Build.

However, it is worth pointing out that despite the differences among the majority of values between calculation, simulation and built model; can be seen as having only slightly more when compared with each other (as shown in **[Table 1]**), there is one particular difference between the calculation's vs simulation at AC – Z_{in} that has a very high percentage difference when compared with the rest. While the percentage difference between the calculation vs builds for AC – Z_{in} is only at 4.613%, the percentage difference between the calculation vs simulation for AC – Z_{in} is at its highest of 71.905% (as shown in **[Table 1]**).

There is no clear explanation for such a significant percentage indifference for the values of AC-Z_{in}, but one theory might have suggested that it is due to the method of obtaining the Q-point values between the manual calculation and simulation are not similar. This is further supported by the difference in Q-point values and max output swing (MOS) between the two methods where the Q-point and MOS values of manual calculation are Q (1.928 mA, 5.334 V), MOS=11.068V

whereas the Q-point values of simulation are Q (1.835 mA, 5.994 V), MOS=11.988V (this greatly affect the results of the input resistance in the h-parameter and later altered the values of Z_{in}). Aside from that, the rest of the values from the calculation, simulation and build witness a considerable difference which is likely due to the connection hole on the breadboard along with the Elvis board might be too loose (causing the measurement equipment to be less accurate) and the resistor values are not identical when measured on the board. Further adjustment of wiring connection, choosing new resistor, and swapping out new breadboard would increase the accuracy and reliability for testing and designing.

CIRCUIT 2 – DESIGN SINGLE-STAGE AMPLIFIER (12 PAGES MAXIMUM)

For this particular task, we will be developing a circuit for the single-stage Common Emitter amplifier and analyzing the circuit according to the required specifications. To build a suitable circuit that would meet the requirement, we must choose the values for all the resistors along with all the capacitors present in the schematic. Additionally, the design must utilize the power supply V_{CC} = 9V; has both AC coupled input and output; a minimum gain at 1KHz of A_V = -10 and the amplifier works for maximum symmetrical output swing. Moreover, the BJT model we used for circuit 2 design is 2N2222A because it is already available for in our system.

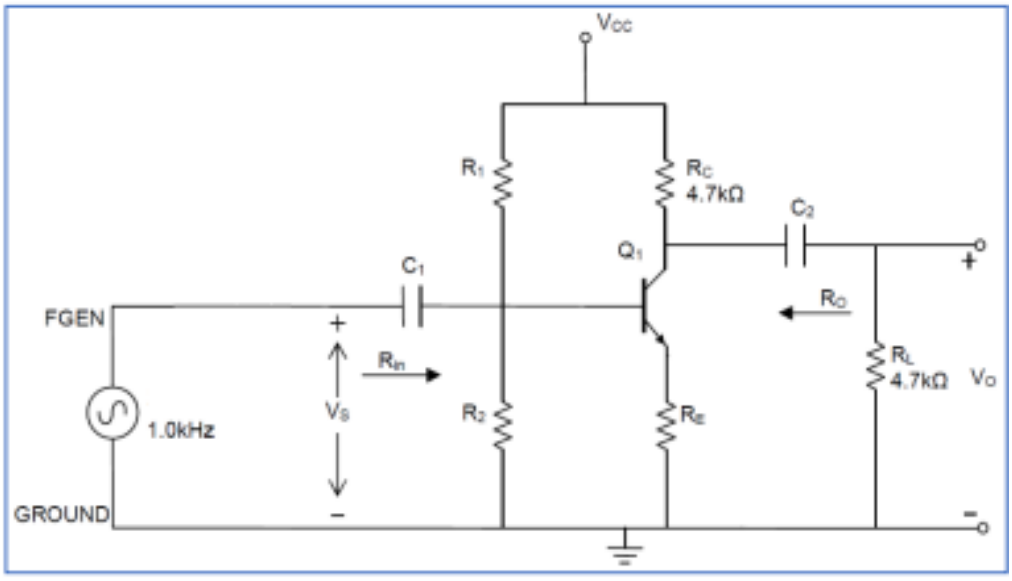


Figure 13. The schematic of the single-stage Common Emitter amplifier (Circuit 2)

2.1.DC Analysis

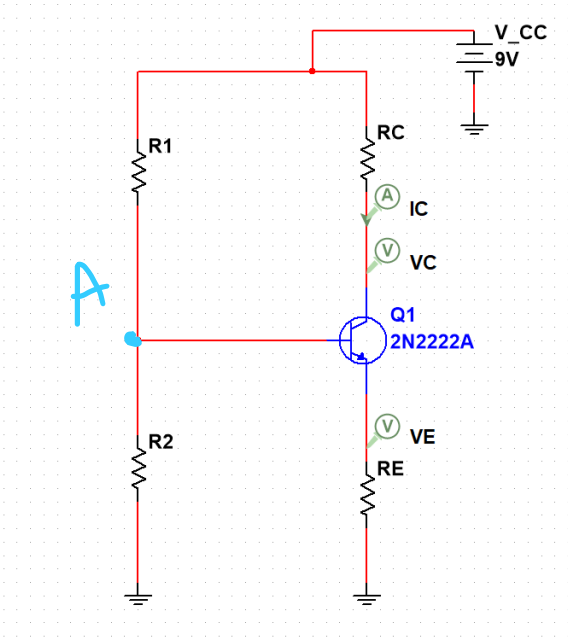


Figure 14. The schematic of the DC biasing single-stage Common Emitter amplifier.

Assume $V_{CE} = \frac{1}{2}V_{CC} = \frac{1}{2}9V = 4.5V$, $\beta = 100$, $V_T = 25mV$. Thus, we evaluate the expressions for the following variables:

- Apply Voltage Divider Rule at node A:

$$V_B = \frac{R_2}{R_2 + R_1}V_{CC} = \frac{R_2}{R_2 + R_1} * 9V$$

- $V_E = V_B - V_{BE} = \frac{R_2}{R_2+R_1} * 9V - 0.7V$ (BJT is in Active mode).
- $V_C = V_{CE} - V_E = 4.5V + \frac{R_2}{R_2+R_1} * 9V - 0.7V$

$$V_C = 3.8V + \frac{R_2}{R_2 + R_1} * 9V$$

- $I_E = \frac{\beta+1}{\beta}I_C = 1.01 * \frac{V_C}{R_C}$

$$I_E = 1.01 * \frac{3.8V + \frac{R_2}{R_2 + R_1} * 9V}{4.7k\Omega}$$

- $R_E = \frac{V_e}{I_e} = (\frac{R_2}{R_2+R_1} * 9V - 0.7V)/(1.01 * \frac{3.8V+\frac{R_2}{R_2+R_1}*9V}{4.7k\Omega})$

2.2.AC Analysis

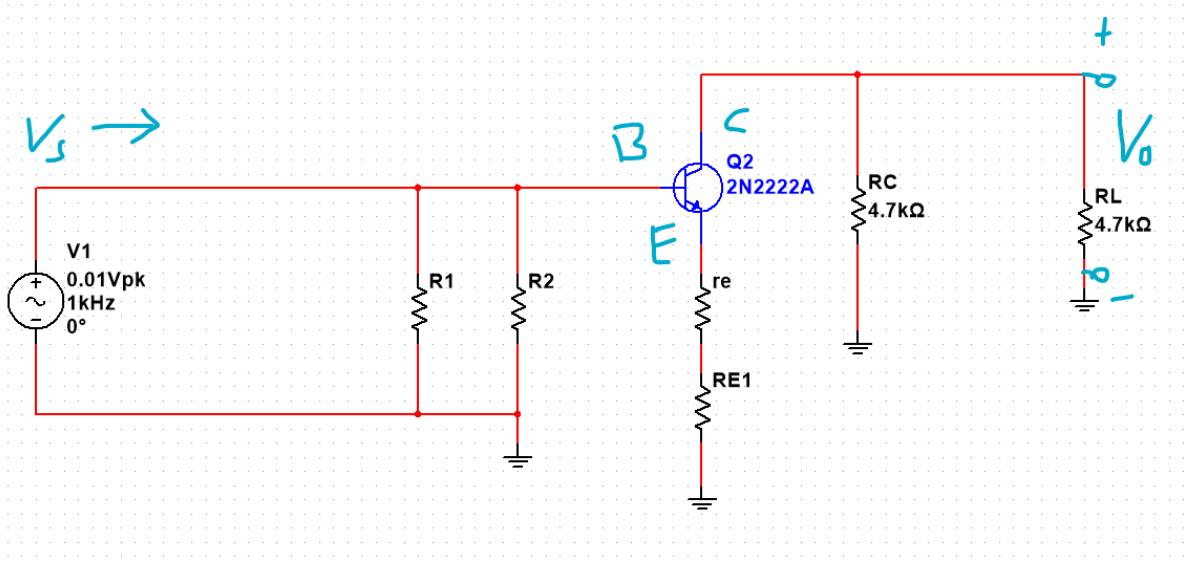


Figure 15. The schematic of the AC biasing single-stage Common Emitter amplifier.

- AC emitter resistance:

$$re = \frac{V_T}{I_E} = \frac{25mV}{1.01 * \frac{3.8V + \frac{R_2}{R_2 + R_1} * 9V}{4.7k\Omega}}$$

- Voltage Gain

$$A_V = \frac{V_o}{V_s} = \frac{V_o}{V_{BE}} = -\frac{R_L // R_C}{re + R_E} = -\frac{4.7k\Omega // 4.7k\Omega}{re + R_E} = -\frac{2.35k\Omega}{re + R_E}$$

$$A_V = -(2.35k\Omega)/(\frac{25mV + \frac{R_2}{R_2 + R_1} * 9V - 0.7V}{1.01 * \frac{3.8V + \frac{R_2}{R_2 + R_1} * 9V}{4.7k\Omega}})$$

- According to the requirement: $A_V = -10\ times$, we obtain:

$$(2.35k\Omega)/(\frac{25mV + \frac{R_2}{R_2 + R_1} * 9V - 0.7V}{1.01 * \frac{3.8V + \frac{R_2}{R_2 + R_1} * 9V}{4.7k\Omega}}) = 10 => \frac{25mV + \frac{R_2}{R_2 + R_1} * 9V - 0.7V}{1.01 * \frac{3.8V + \frac{R_2}{R_2 + R_1} * 9V}{4.7k\Omega}} = 235\Omega$$

- Assuming $R_2 = 8.2k\Omega$, $R_1 = 82k\Omega$, we'll get:

$$A_V = -\frac{2.35k\Omega}{223.451\Omega} = -10.517$$

- As a result, we implement $R_2 = 8.2k\Omega$, $R_1 = 82k\Omega$ in the design.

2.3. Substitution:

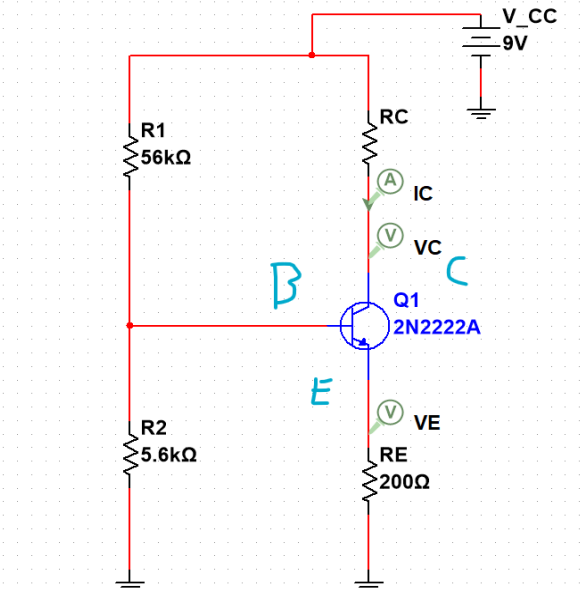


Figure 16. The schematic of the DC biasing single-stage Common Emitter amplifier with new values.

DC BIASING:

With $V_{CE} = 4.5V$, $\beta = 100$, $R_2 = 5.6k\Omega$, $R_1 = 56k\Omega$ $V_T = 25mV$ and some assumptions, we compute:

- $V_B = \frac{R_2}{R_2 + R_1} V_{CC} = \frac{8.2k\Omega}{8.2k\Omega + 82k\Omega} * 9V \cong 0.9V$
- $V_E = V_B - V_{BE} = 0.9V - 0.7V = 0.2V$
- $V_C = V_{CE} - V_E = 4.5V + 0.2V = 4.7V$
- $I_E = \frac{\beta + 1}{\beta} I_C \cong I_C = \frac{V_C}{R_C} = \frac{4.7V}{4.7k\Omega} \cong 1\ mA$
- $I_{C\ (sat)} = \frac{V_{CC}}{R_C} = \frac{9V}{4.7k\Omega} = \frac{9}{4700} A$
- $R_E = \frac{V_e}{I_e} = \frac{0.2V}{1\ mA} = 200\Omega$

  Therefore, the Q point is Q($I_C = 1\ mA$, $V_{CE} = 4.5V$)

AC BIASING

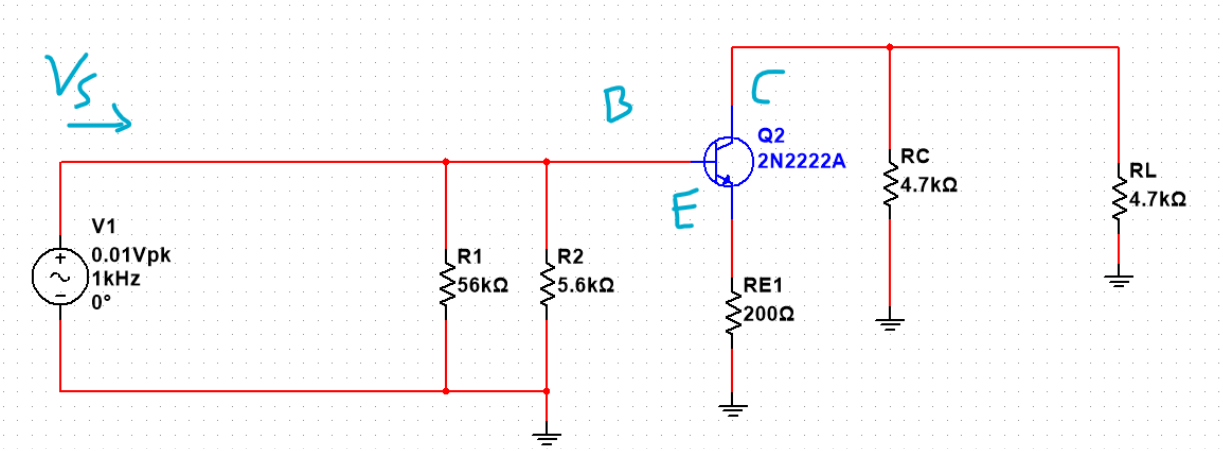


Figure 17. The schematic of the AC biasing single-stage Common Emitter amplifier with new values.

Assume Thermal Voltage $V_T = 25mV$, $V_A = 75V$, and $\beta = 100$, and fcut = 35Hz the following variables are orderly expressed as:

- $re = \frac{V_T}{I_E} = \frac{25mV}{1mA} = 25\Omega$
- $A_V = \frac{V_o}{V_s} = -\frac{R_L//R_C}{re+R_E} = -\frac{2.35k\Omega}{25\Omega+200\Omega} = -10.444\ times$
- $r_o = \frac{V_A+V_{CE}}{I_C} = \frac{75V+4.5V}{1mA} = 79.5k\Omega$

- $Z_{in} = (R_1//R_2)//\beta(re + R_E) = (8.2k\Omega//82k\Omega)//150(25\Omega + 200\Omega)$
  $\boldsymbol{Z_{in}} = 7.454k\Omega//22.5k\Omega = \mathbf{5.599}\boldsymbol{k}\Omega$
- $Z_{out} = (R_C)//r_o = (R_L)$ ($r_o$is too big so we can neglect it)
  $\boldsymbol{Z_{out}} = \mathbf{4.7}\boldsymbol{k}\Omega$

With f=35Hz, we can adjust the values for the Capacitors by doing as followed:

- The X_{C1} of the coupling capacitor, C_1, should be at least 10 times less than Z_{in}
  $$C_1 = \frac{1}{2\pi * (f = 35Hz) * X_{C1}} = \frac{1}{2\pi * 35Hz * 0.1 * Z_{in}} = \mathbf{9.465}\mu\boldsymbol{F}$$
- The X_{C2} of the coupling capacitor, C_2, should be at least 10 times less than Z_{in}
  $$C_1 = \frac{1}{2\pi * (f = 35Hz) * X_{C2}} = \frac{1}{2\pi * 35Hz * 0.1 * Z_{out}} = \mathbf{9.675}\mu\boldsymbol{F}$$

  So, we will pick $\boldsymbol{C_1 = C_2 = 10\mu F}$ for the design implementation on Elvis board.

2.4. Simulation

2.4.1. MULTISIM SIMULATION

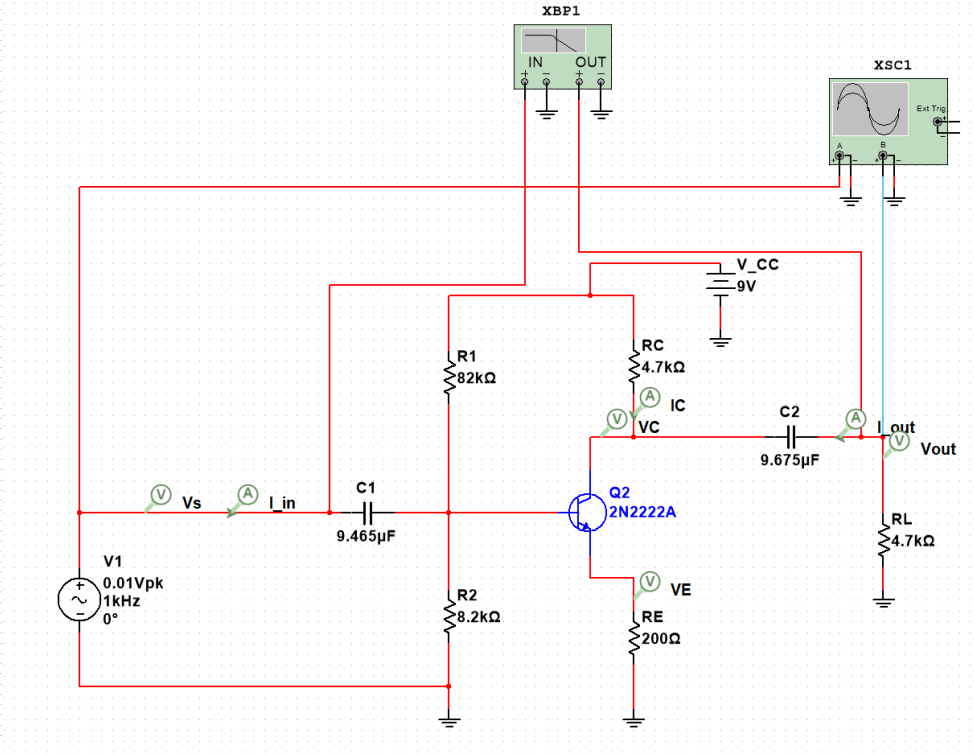


Figure 18. The schematic of the single-stage Common Emitter amplifier with chosen values displayed in Multisim.

Q point

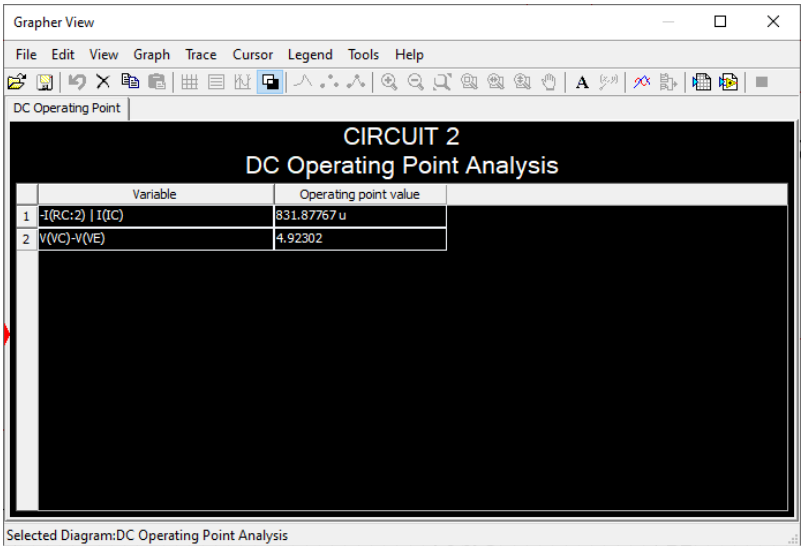


Figure 19. Q point Q (ICQ = 0.832mA, VCEQ = 4.923V) of the designed schematic of circuit 2 in Multisim.

Voltage Gain

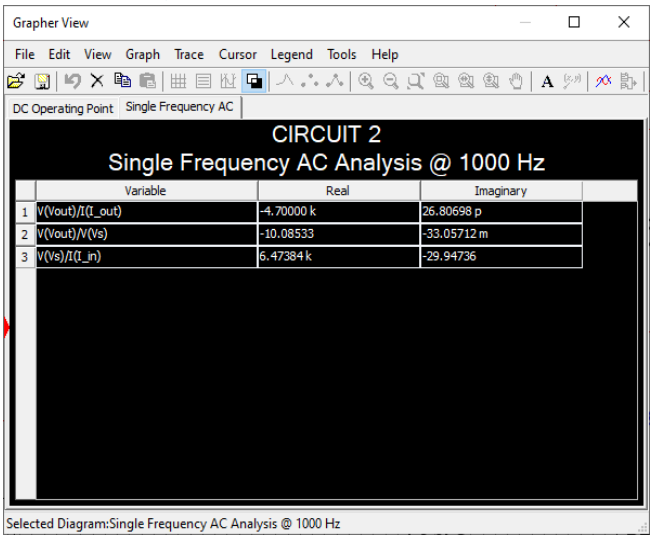


Figure 20. Voltage gain and input/output impedances from circuit in Multisim.

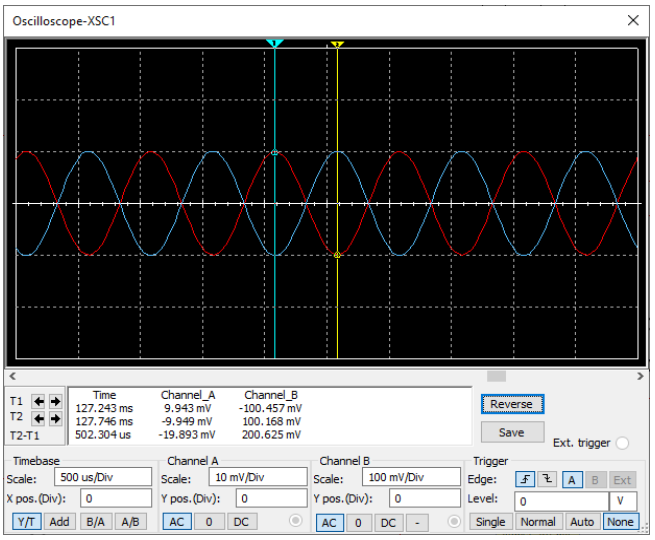


Figure. Voltage gain displayed in Oscilloscope of circuit 2 in Multisim. $A_V = \frac{-100.457mV}{9.943mV} = -10.103$

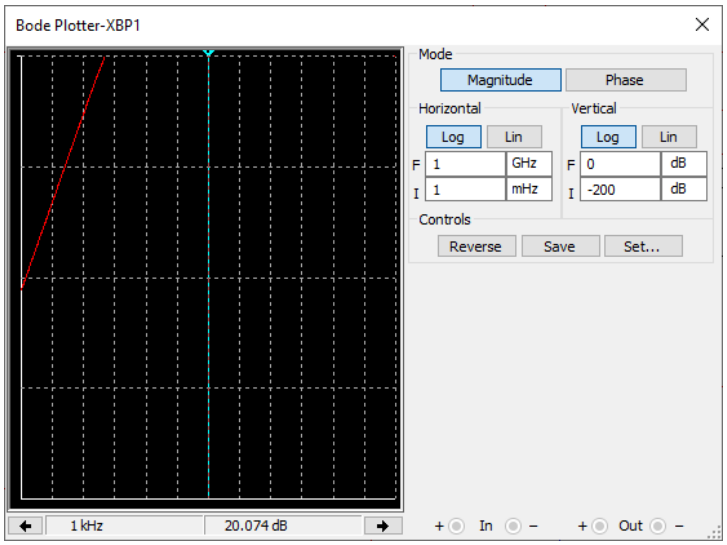


Figure 21. Voltage gain displayed in Bode plot of circuit in Multisim. $A_V = 10.085$

2.4.2. MULTISIM SIMULATION (REAL VALUES)

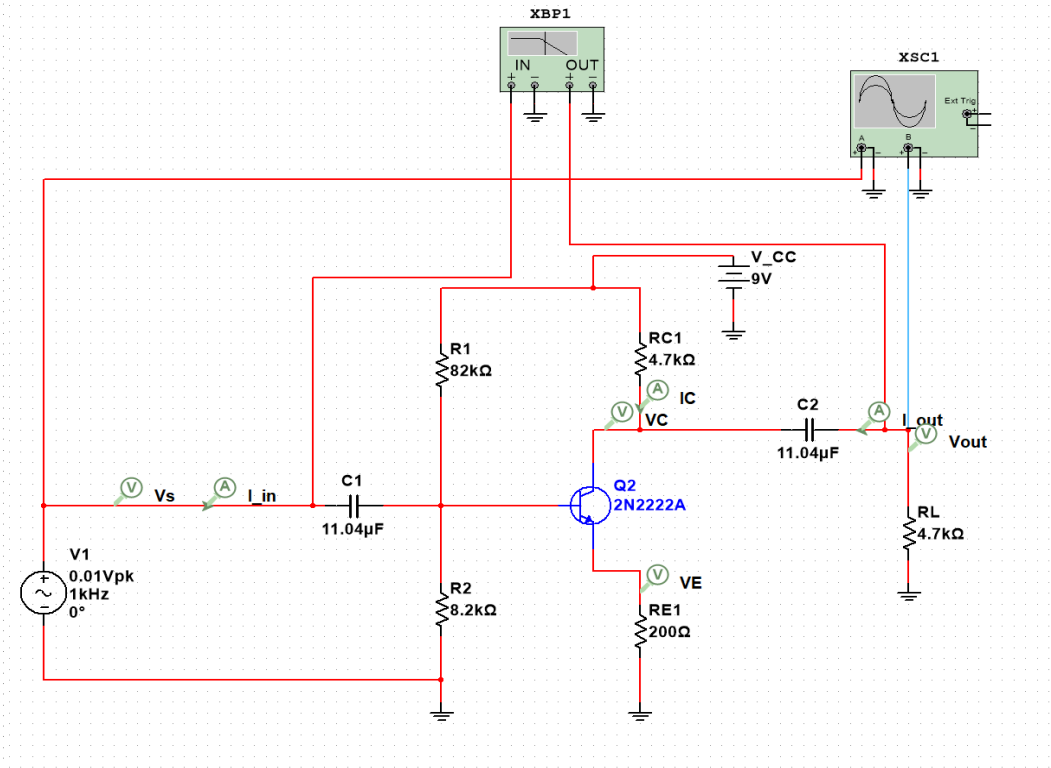


Figure 18. The schematic of the single-stage Common Emitter amplifier with real values displayed in Multisim.

Q point

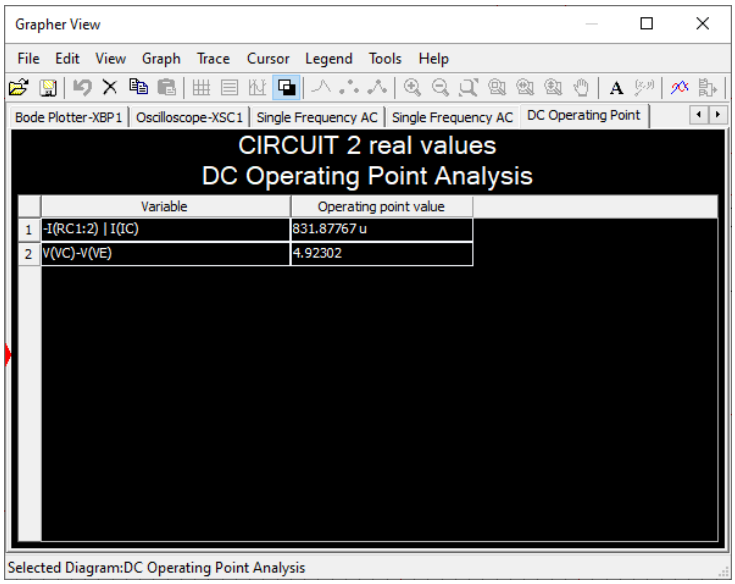


Figure 19. Q point Q(ICQ = 0.832mA, VCEQ = 4.923V) of the designed schematic of circuit 2 with components' measured values in Multisim.

Voltage Gain

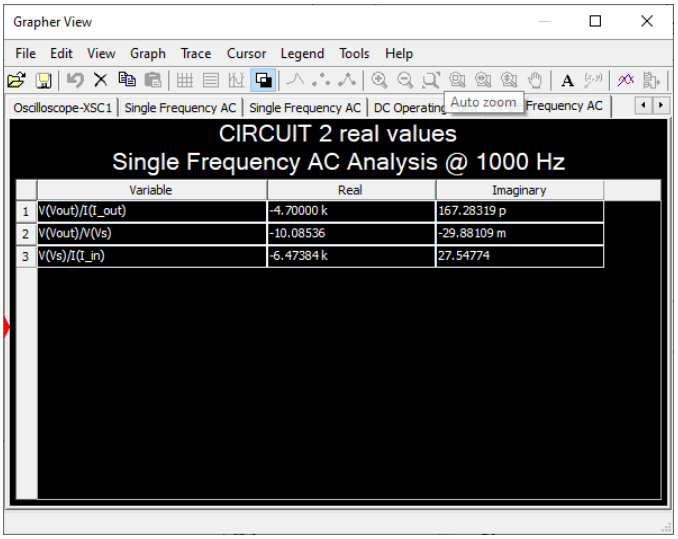


Figure 20. Voltage gain and input/output impedances from circuit 2 with components' real values in Multisim

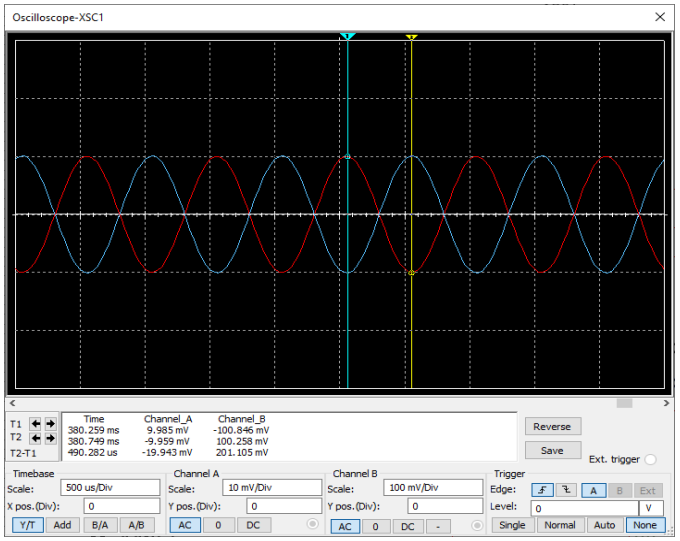


Figure 21. Voltage gain displayed in Oscilloscope of circuit 2 in Multisim. $A_V = \frac{-100.846mV}{9.985mV} = -10.100$

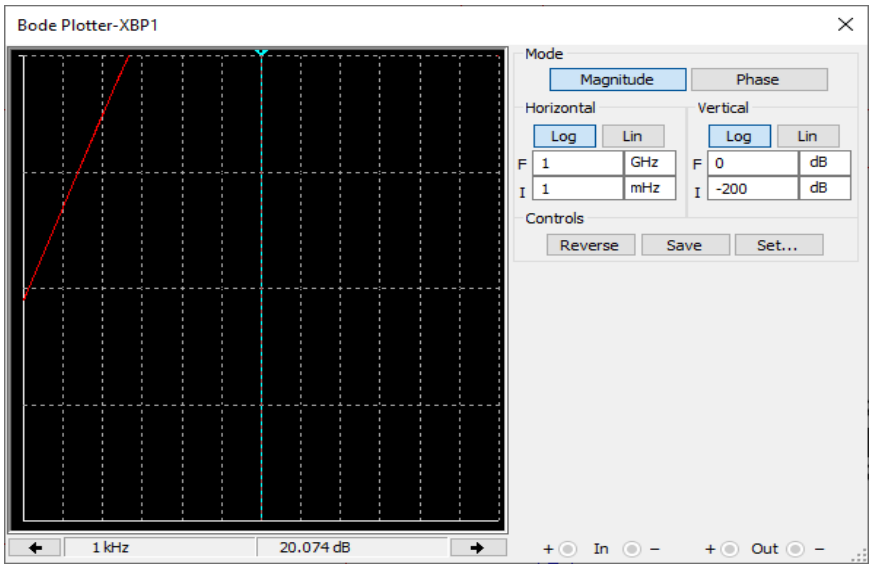


Figure 22. Voltage gain displayed in Bode plot of circuit in Multisim. $A_V = 10.085$

2.4.3. ELVIS SIMULATION

Q POINT

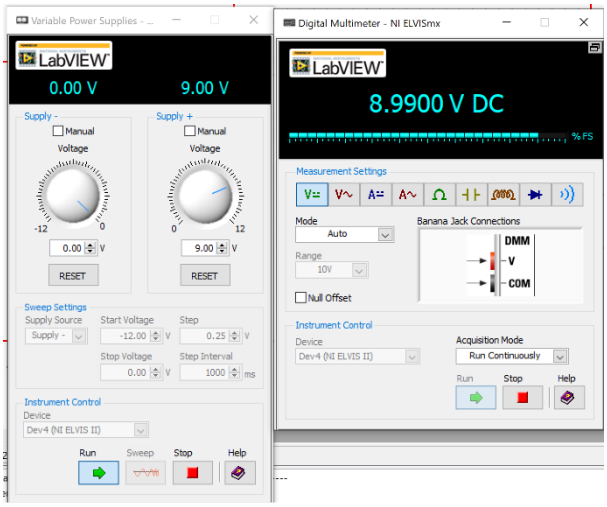


Figure 23. VCC measured value from circuit 2 on Elvis board.

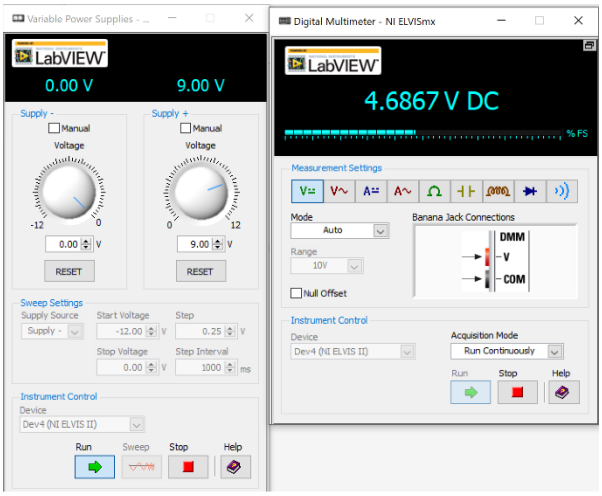


Figure 24. VCE measured value from circuit 2 on Elvis board.

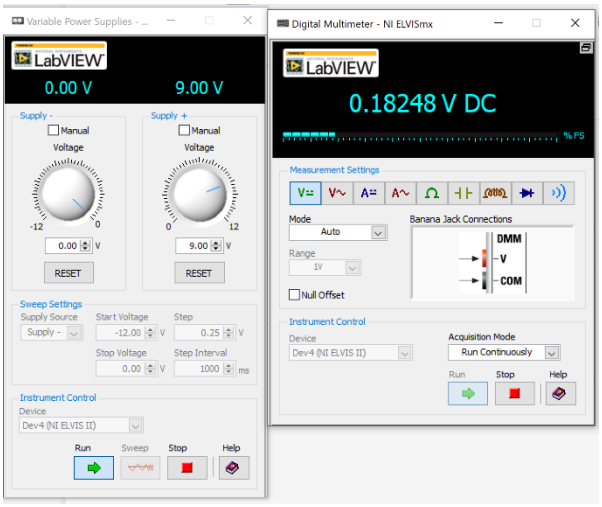


Figure 25. VE measured value from circuit 2 on Elvis board.

Due to the insufficient probes to measure the current, we proceeded to measure the voltage and use the Ohm's law to find out the I_C:

By applying KVL to the collector-emitter branch, we observe:

$$V_C = V_{CC} - V_{CE} - V_E$$

$$V_C = 8.9900V - 4.6867V - 0.18248V = 4.12082V$$

Hence, we compute the I_C:

$$I_C = \frac{V_C}{R_C} = \frac{4.12082V}{4.7K\Omega} = 0.877mA$$

Therefore, we have Q($I_C = 0.877mA, V_C = 4.6867V$) real value

GAIN

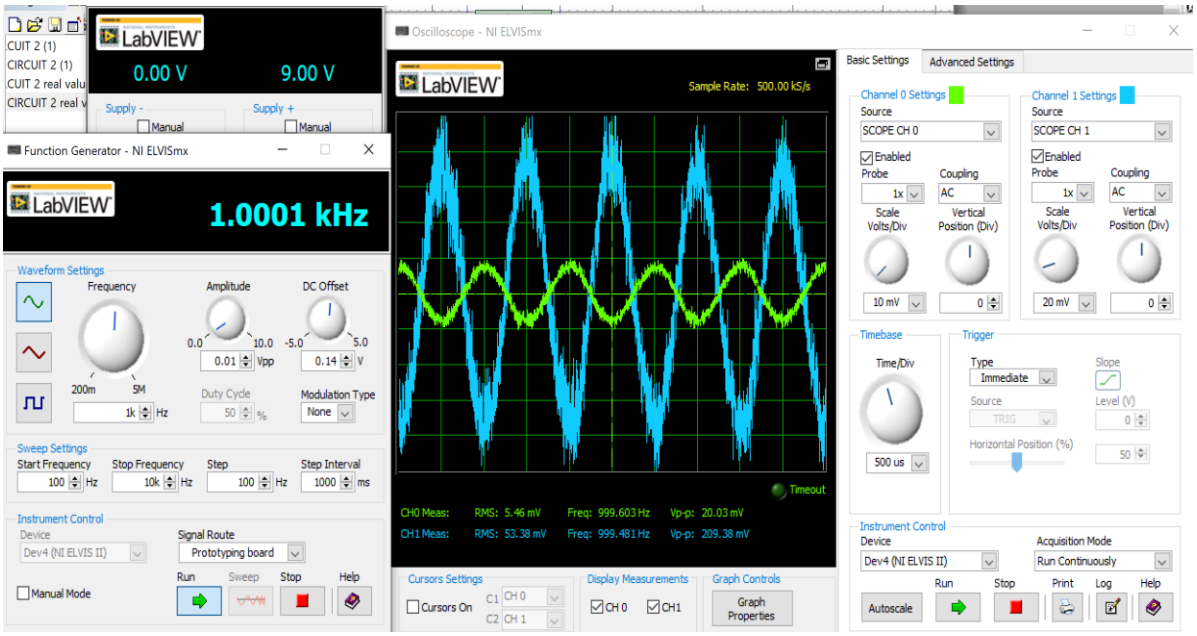


Figure 26. Voltage gain of circuit 2 measured by inspecting on the oscilloscope from Elvis board II.

$$A_V = -\frac{209.38mV}{20.03mV} - 10.453$$

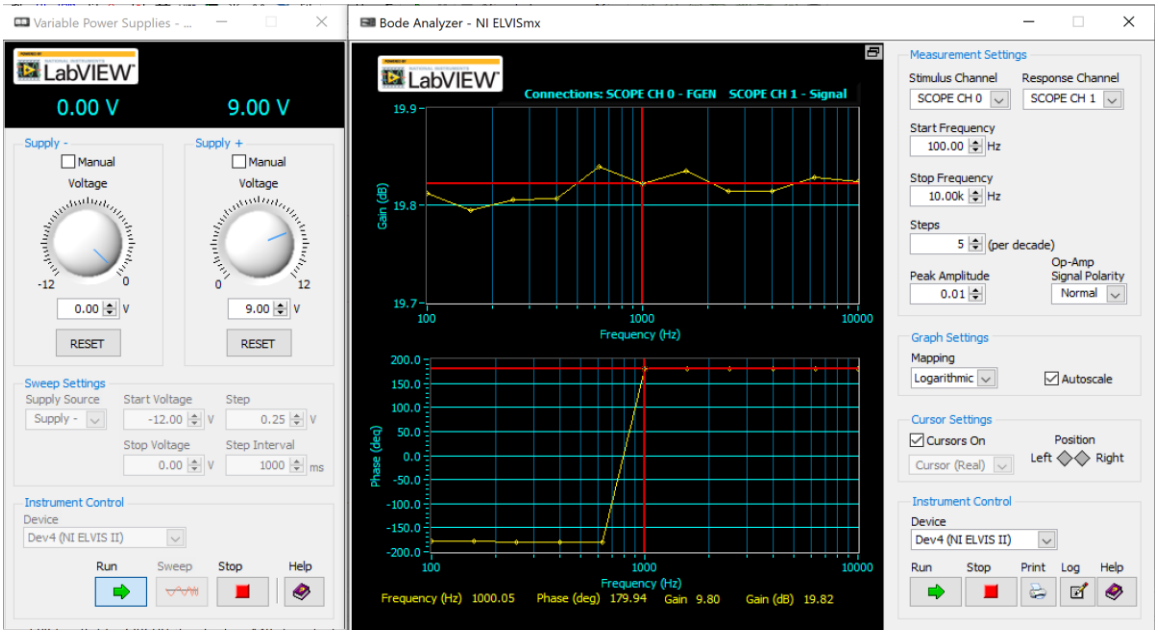


Figure 27. Voltage gain of circuit 2 measured by running Bode plot from Elvis board II.

$$A_V = 9.800$$

2.5. Build

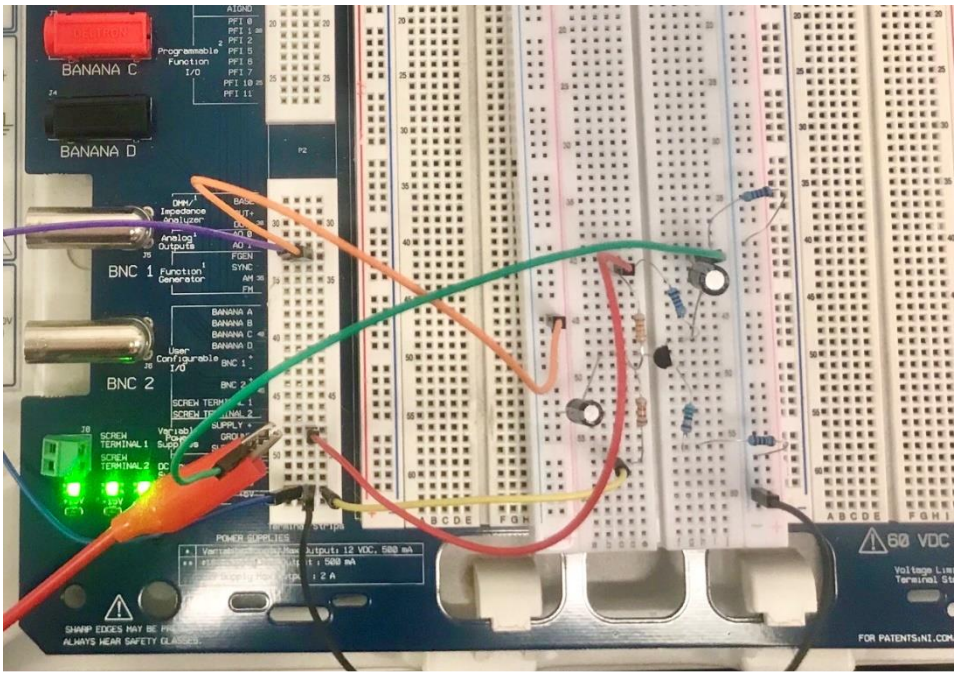


Figure 28. Implementation of the designed circuit 2 on Elvis board II

2.6. Discussion

DC LOADLINE (by using Mx word)

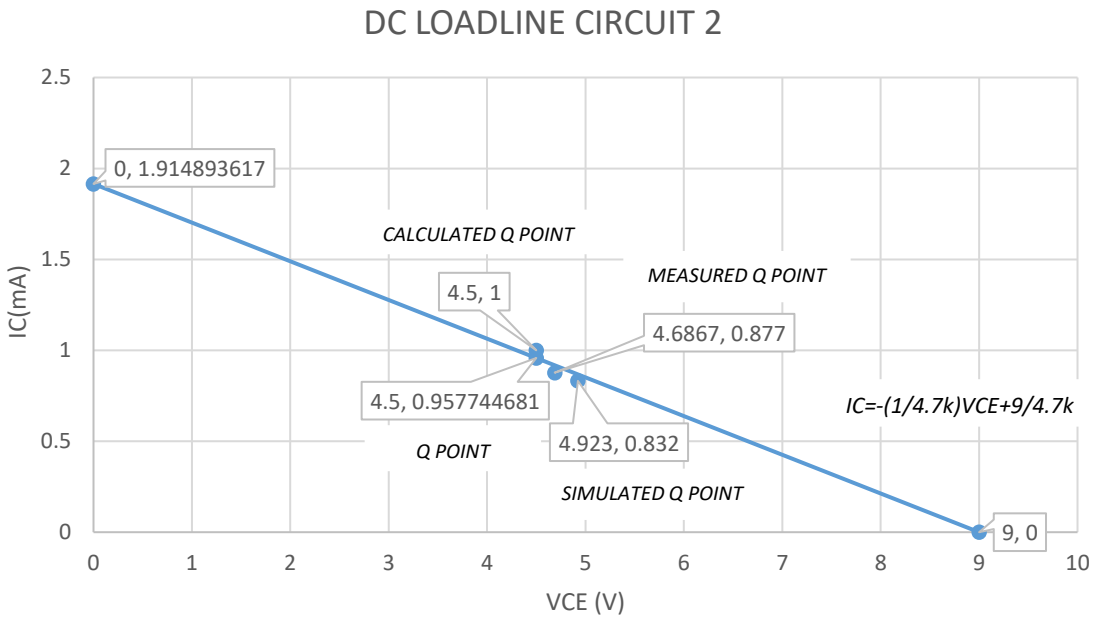


Figure 29. DC load line of circuit 2 and its Q point. 'm' = 10^{-3}, k =1000

	Manual Calculation	Simulation (Real values)	Build	Percentage Difference between Calculation vs. Simulation	Percentage difference between Calculation vs. Build
DC – Q-point	(I_{CQ}): 1 mA (V_{CEQ}): 4.5V (MOS): 4.5*2=9V	(I_{CQ}): 0.832mA (V_{CEQ}): 4.923V (MOS): 4.923*2=9.846V	(I_{CQ}): 0.877mA (V_{CEQ}):4.686V (MOS): 4.686*2=9.372V	(I_{CQ}): 16.8% (V_{CEQ}): 8.592% (MOS):9.400%	(I_{CQ}): 12.3% (V_{CEQ}): 4.149% (MOS):4.133%
AC – A_v	-10.444	(Oscilloscope): -10.100 (Bode plot): 10.085	(Oscilloscope): -10.453 (Bode plot): 9.800	(Oscilloscope): 3.294% (Bode plot): 3.437%	(Oscilloscope): 0.086% (Bode plot): 6.166%

Table 2. Result table of Calculation Vs Simulation Vs Build, along with the percentage difference between each value (Circuit 2)

Overall, the development and process of designing the single-stage Common Emitter amplifier went well as the circuit design included all the required components together with the implements of the 9V power supply, having both AC coupled input and output as well as satisfying the requirement of a minimum gain of A_V = -10 at 1KHz

It is important to emphasize that the differences in the Voltage Gain and Q-point between calculation vs simulation vs build are likely from the circumstances of which the simulation and build is constructed throughout the development. Since the circuit design of simulation is built in an ideal environment (where the board doesn't have any issues or problems), the values are exact and always remain constant without any interference of outside force that could impact the outcome results. While the circuit design of the build has multiple factors that could affects the overall design considerably (such as loose connection in the connection hole, the board having its own resistance, the board producing noise, etc.).

However, the Q point when comes to simulation and implementation witness its sides clipped. Even though the assumption was made, the percentage of difference is around 10% when compared to the simulations. This is due to the changes in values from the components of the

design in reality. Hence, the requirement where the design produces a maximum symmetrical output swing is now achieved.

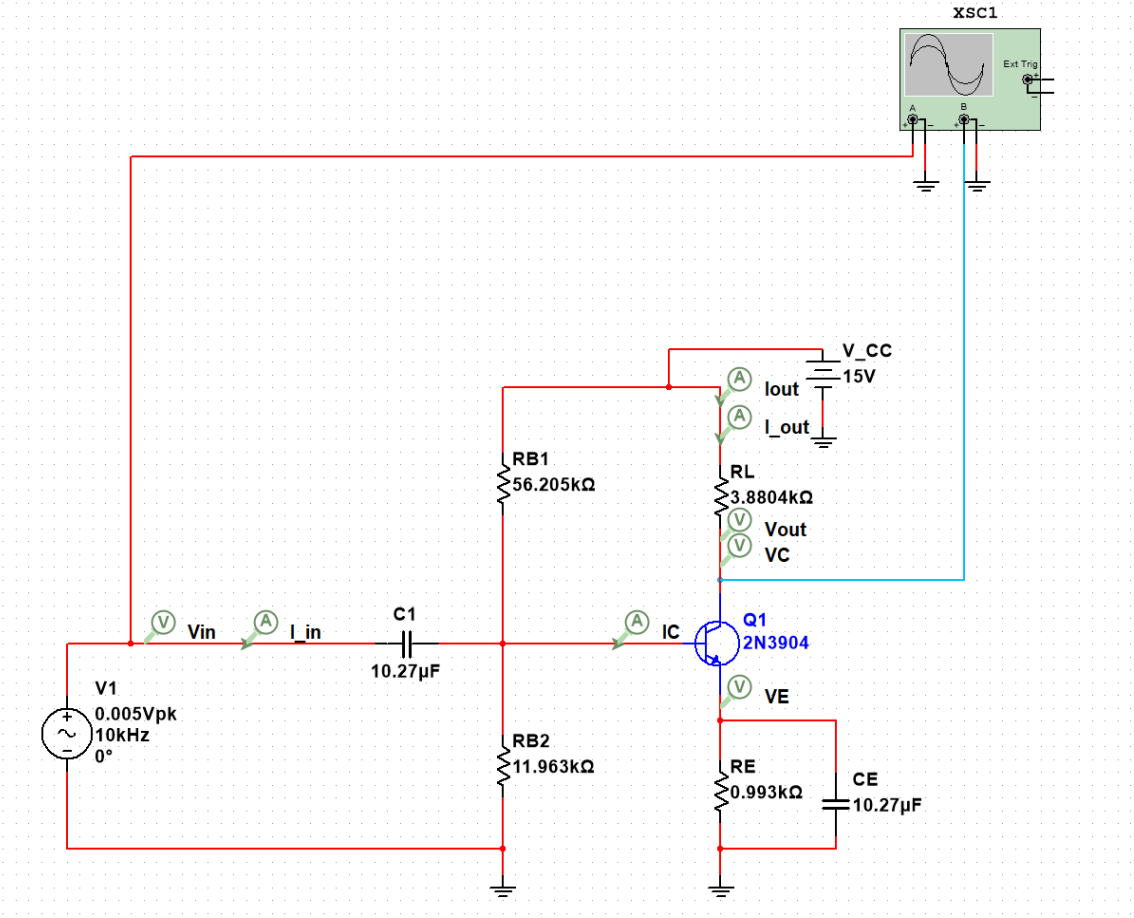
Aside from that, the values from calculation, simulation and build witness a considerable difference as it can be seen to having slightly more when compared with each other (as shown in **[Table 2]**). Further adjustment on the wiring connections, swapping out new breadboard alongside choosing new resistors values to ensure the accuracy and reliability when testing and re-designing.

REFERENCES

Thomas L. Floyd, *Electronic Devices : Conventional Current Version*, Global ed. , Tenth ed. Harlow, England: Pearson, 2018., page 273-292

APPENDIX

APPENDIX 1: THE VALUES OF COMPONENTS MEASURED ON ELVIS BOARD II (CIRCUIT 1) NOTED DOWN IN MULTISIM.



APPENDIX 2: THE VALUES OF Z_{IN} AND Z_{OUT} OBTAIN FROM THE SUBSTITUTION OF MEASURED AND REAL VALUES ON ELVIS BOARD II (CIRCUIT 1)

The equations to obtain Z_{IN} and Z_{OUT} from measured and real values on Elvis Board II (Circuit 1):

$$I_C = \frac{V_C}{R_C} = \frac{7.8841\ V}{3.8804\ k\Omega} = 2.032\ mA$$

$$R_\pi = \frac{\beta_0}{I_C} \times V_T = \frac{100}{2.032\ mA} \times 25\ mV = 1230.315\ \Omega = 1.230\ k\Omega$$

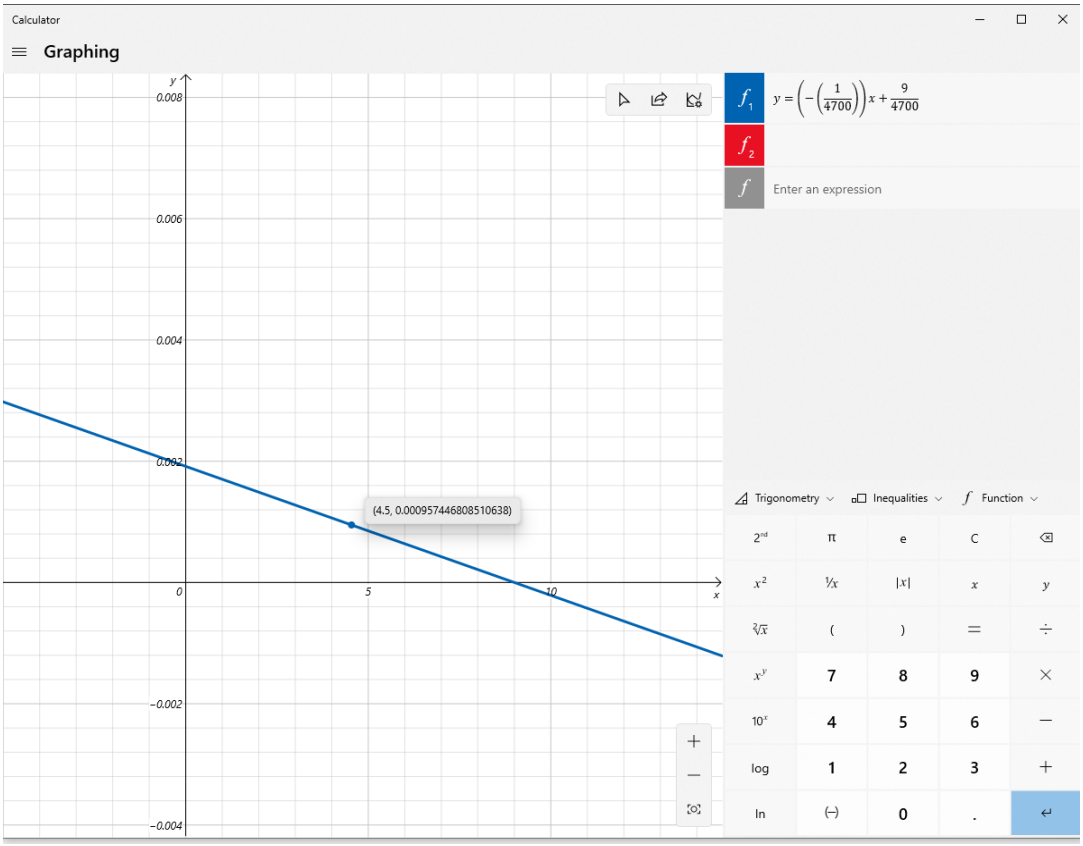
$$R_0 = \frac{V_A + V_{CE}}{I_C} = \frac{75V + 5.6690\ V}{2.032\ mA} = 39.699\ k\Omega$$

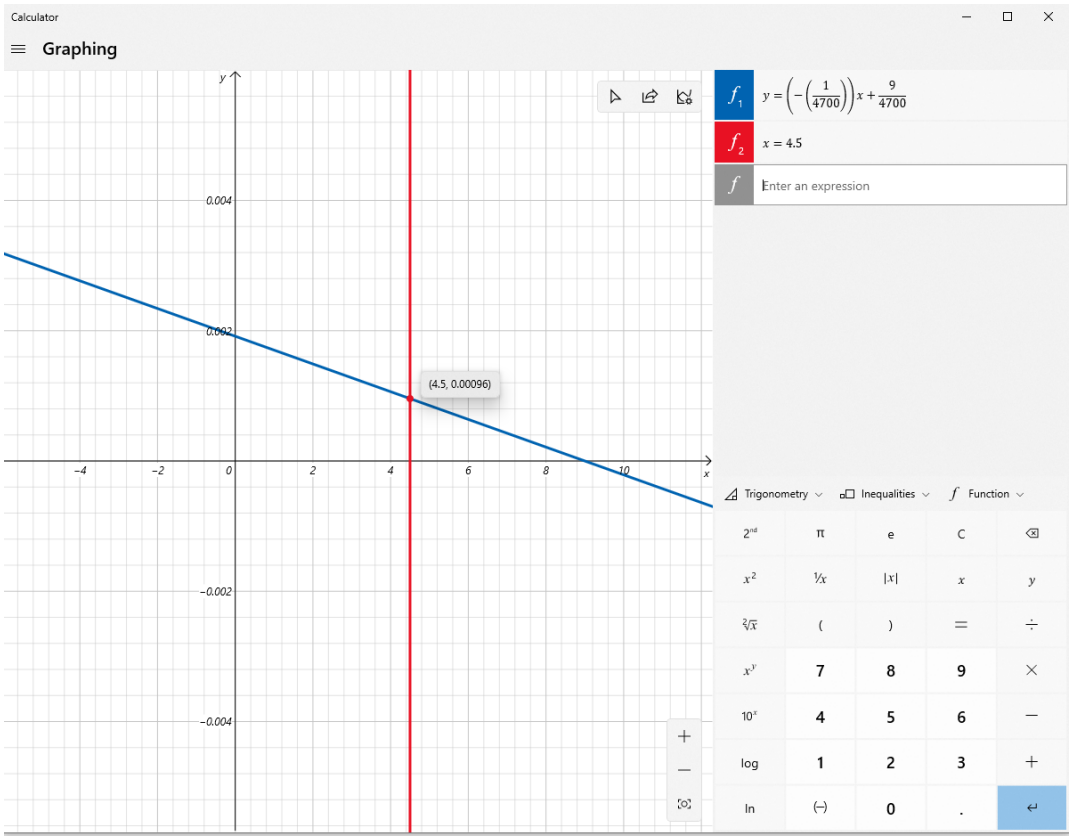
$$R_B = \frac{R_1 \times R_2}{R_1 + R_2} = \frac{(56.205\ k\Omega \times 11.963\ k\Omega)}{(56.205\ k\Omega + 11.963\ k\Omega)} = 9863.578\ \Omega = 9.864\ k\Omega$$

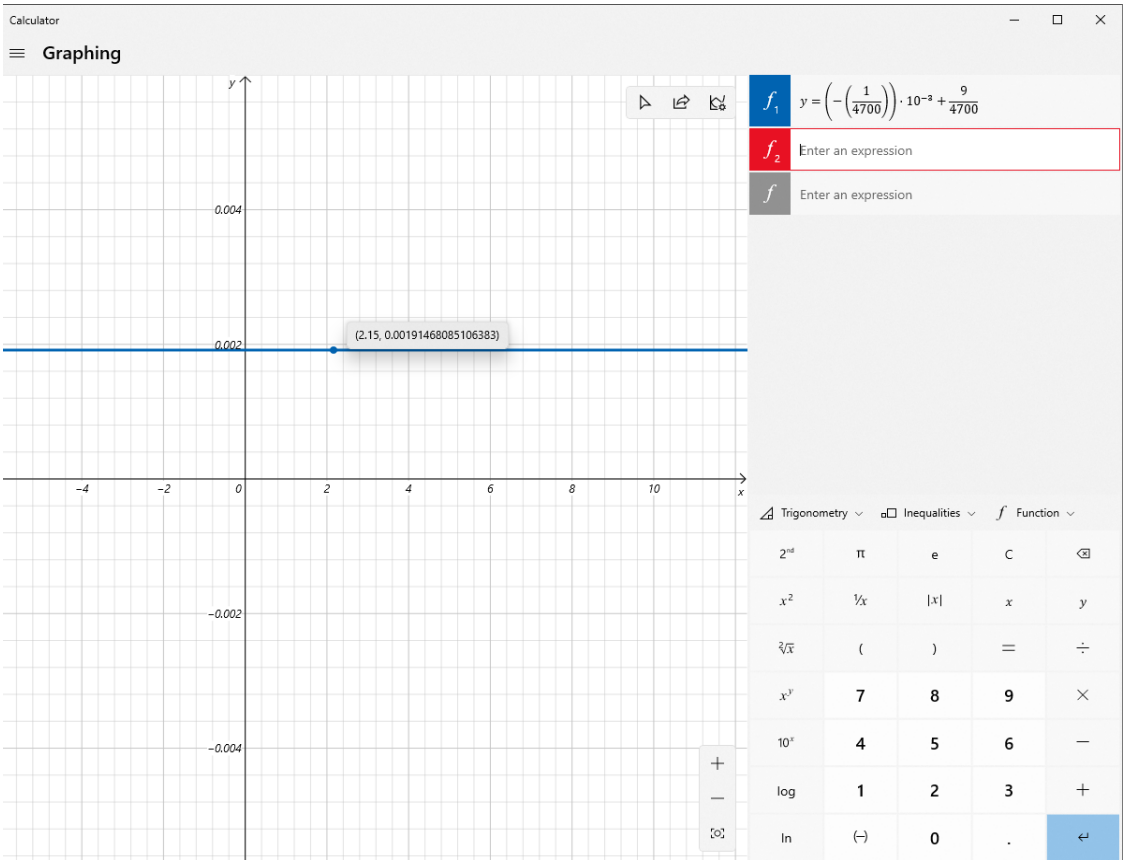
$$\Rightarrow Z_{IN} = \frac{R_B \times R_\pi}{R_B + R_\pi} = \frac{(9.864\ k\Omega \times 1.230\ k\Omega)}{(9.864\ k\Omega + 1.230\ k\Omega)} = 1093.629\ \Omega$$

$$\Rightarrow Z_{OUT} = \frac{R_0 \times R_C}{R_0 + R_C} = \frac{(39.699\ k\Omega \times 3.8804\ k\Omega)}{(39.699\ k\Omega + 3.8804\ k\Omega)} = 3534.811\ \Omega$$

APPENDIX 3: CIRCUIT 2 DC LOADLINE DISPLAYED ON WINDOW 10 CALCULATOR'S GRAPHING.


Calculator
Graphing
$y = \left(-\left(\frac{1}{4700}\right)\right)x + \frac{9}{4700}$
Enter an expression
(4.5, 0.000957446808510638)
0.008
0.006
0.004
0.002
0
−0.002
−0.004
5
10
x
y
Trigonometry
Inequalities
Function


Calculator
Graphing
$y = \left(-\left(\frac{1}{4700}\right)\right)x + \frac{9}{4700}$
$x = 4.5$
Enter an expression
(4.5, 0.00096)
0.004
0.002
−0.002
−0.004
−4
−2
0
2
4
6
8
10
x
y
Trigonometry
Inequalities
Function


Calculator
Graphing
$y = \left(-\left(\frac{1}{4700}\right)\right) \cdot 10^{-2} + \frac{9}{4700}$
Enter an expression
Enter an expression
(2.15, 0.00191468085106383)
0.004
0.002
−0.002
−0.004
−4
−2
0
2
4
6
8
10
x
y
Trigonometry
Inequalities
Function