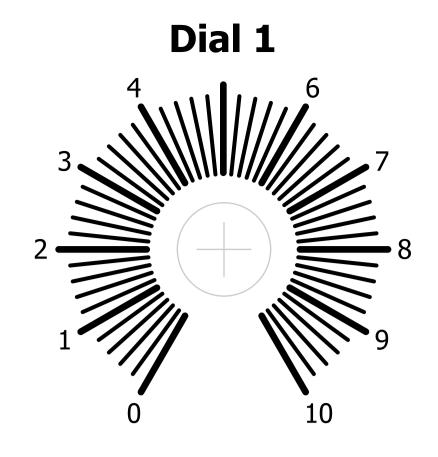
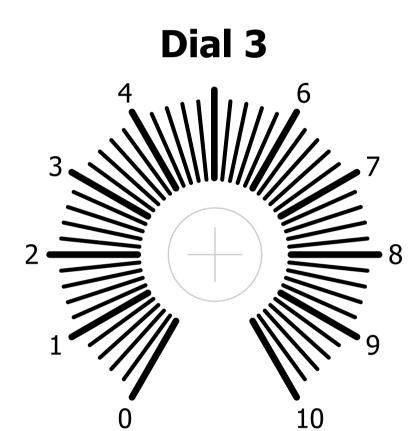
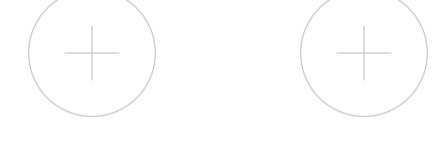
## 110 HEAD



# Dial 2

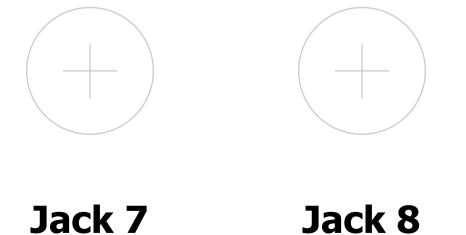


Jack 1 Jack 2



Jack 3 Jack 4

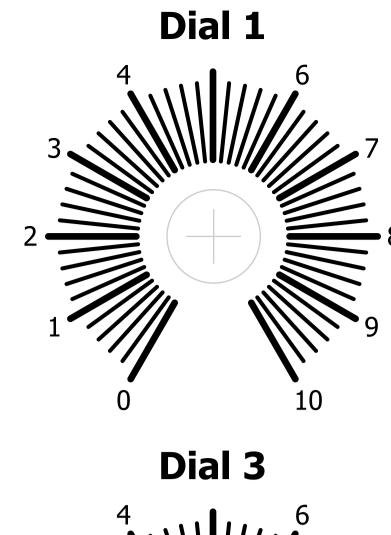


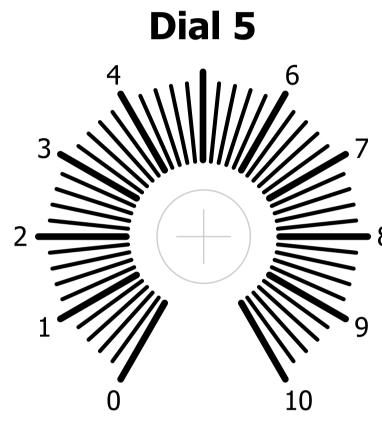


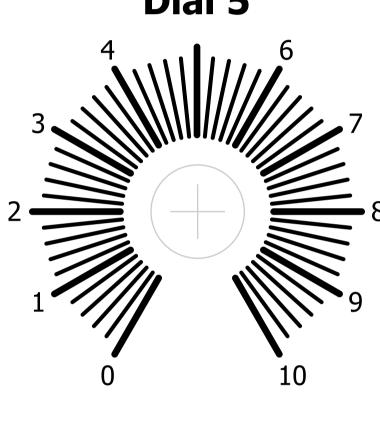


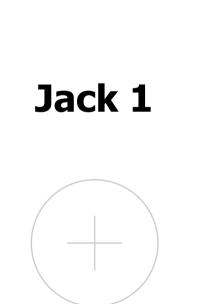
## **2U HEADER**











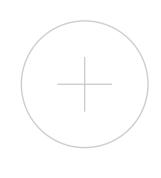
Jack 4

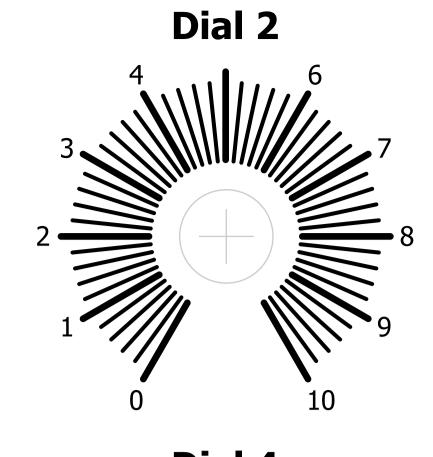


Jack 7

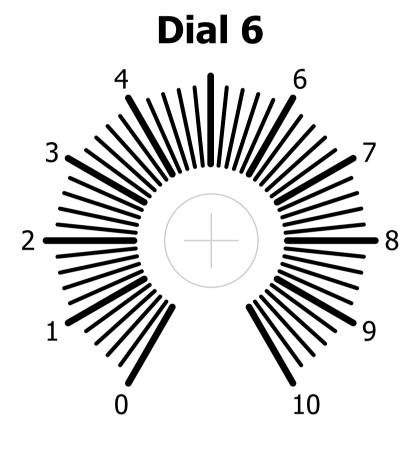


Jack 10





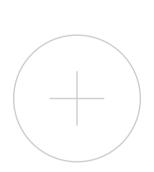
Dial 4 10



Jack 2



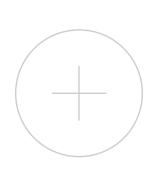
Jack 5



Jack 8



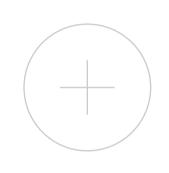
Jack 11



Jack 3



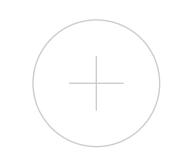
Jack 6



Jack 9



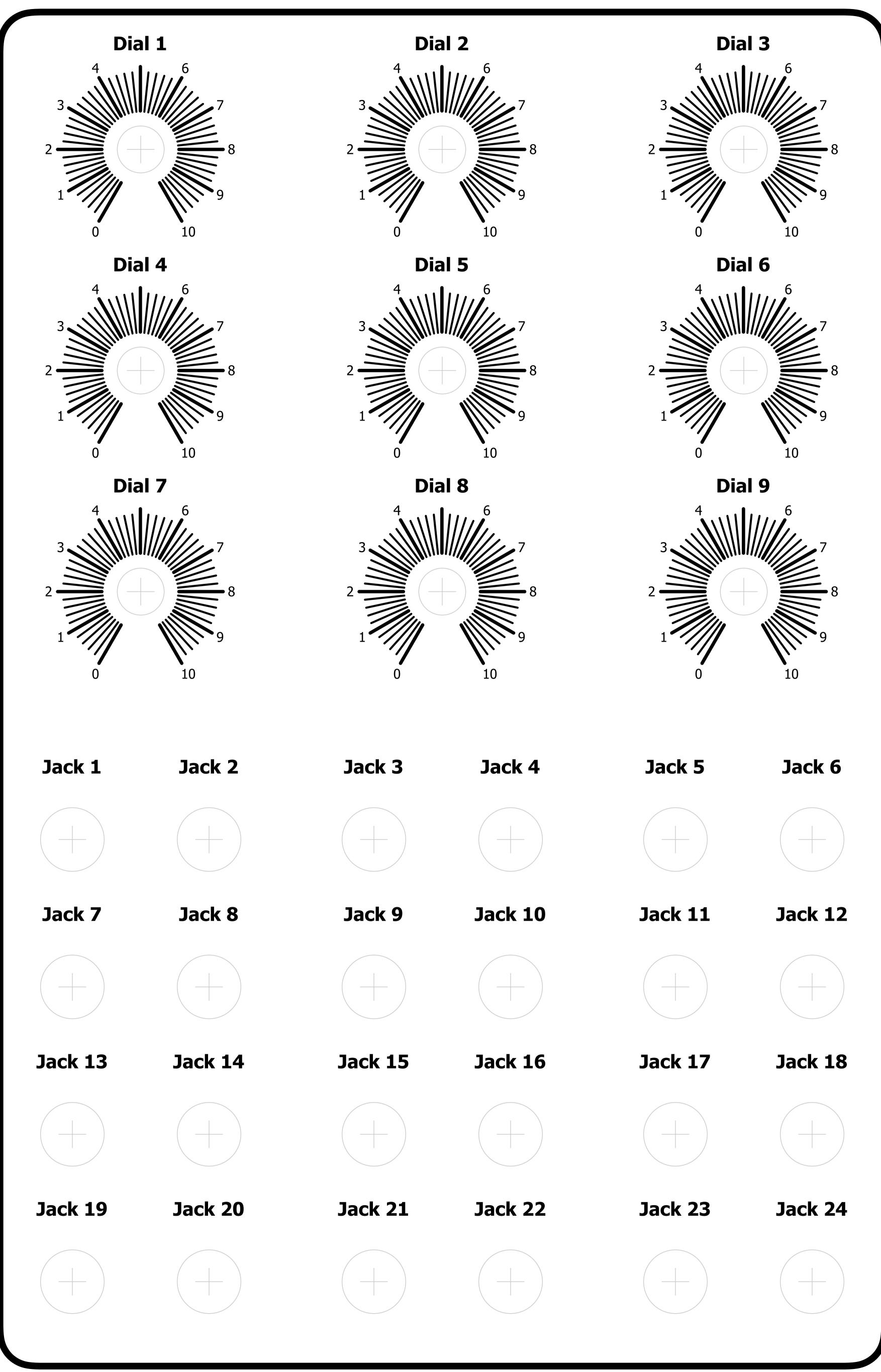
Jack 12

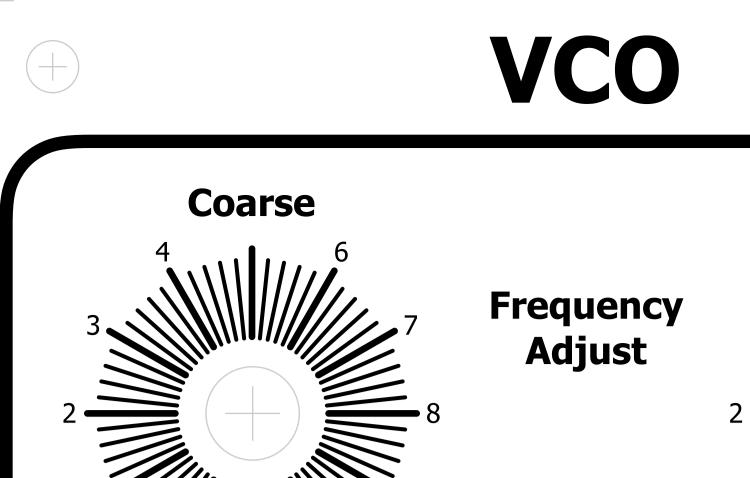


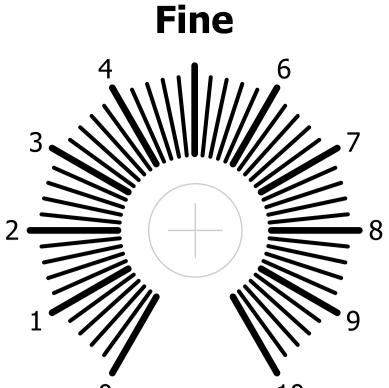
#### $\bigcirc$

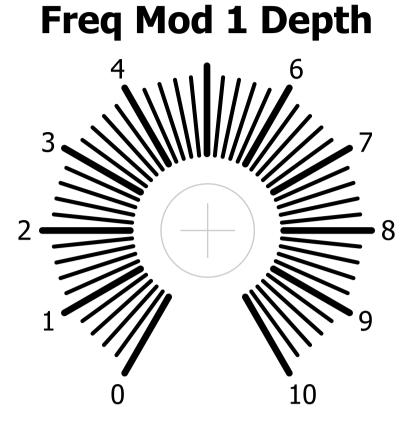
## **3U HEADER**

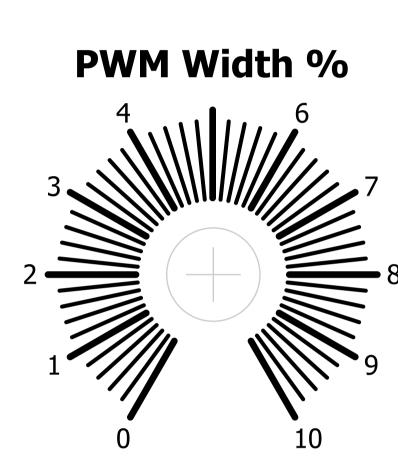


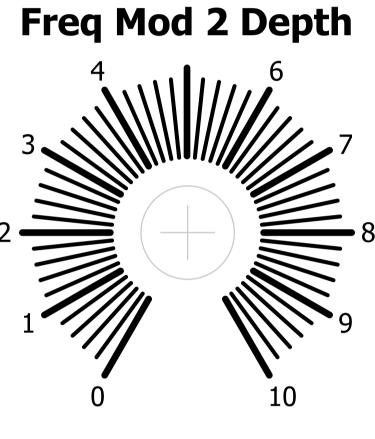


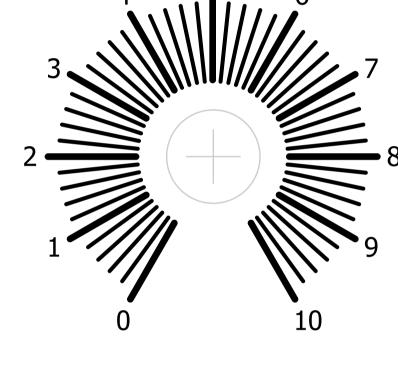


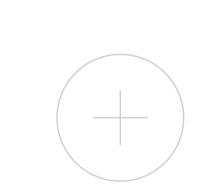




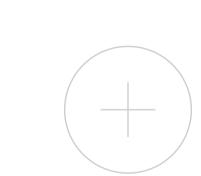








Freq Mod 1 In



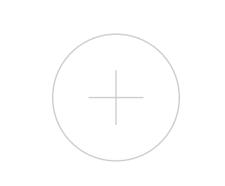
**PWM CV In** 

Freq Mod 1 In **Sync In** 



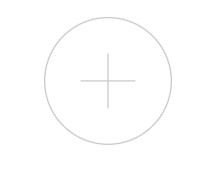


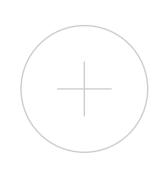




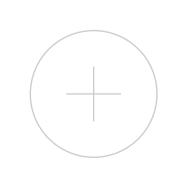
**Square Out** 

**CV** Linear In **Ramp Out** 





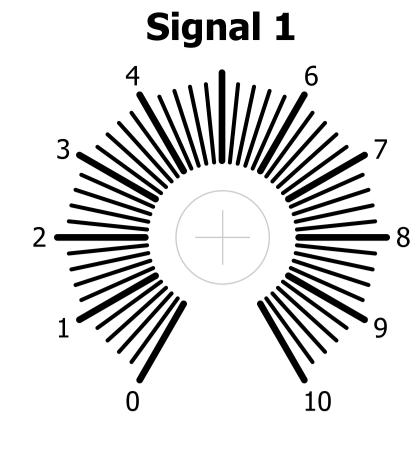
**CV In** 



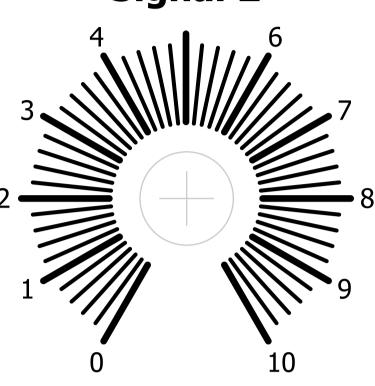
## +

## **VCF 12**

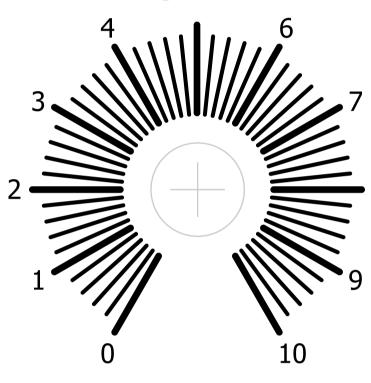




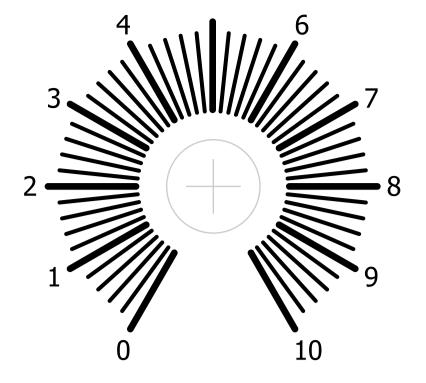
Signal 2



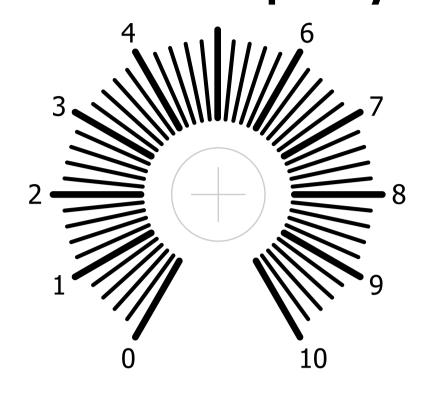
Signal 3



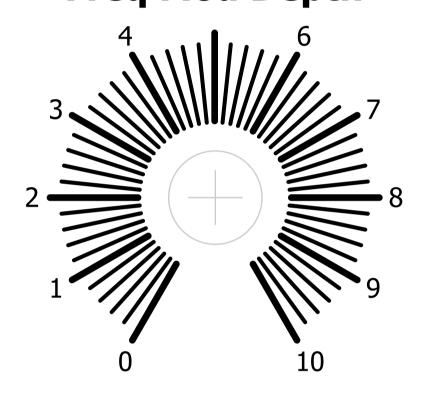
Resonance



**Cut-Off Frequency** 



**Freq Mod Depth** 





Signal 1 In



Signal 2 In



Signal 3 In



Cut-Off CV In



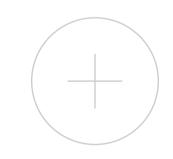
Freq Mod In



**Resonance CV In** 



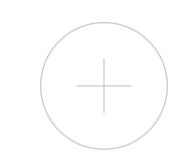
**High-Pass Out** 



**Band-Pass Out** 



**Low-Pass Out** 



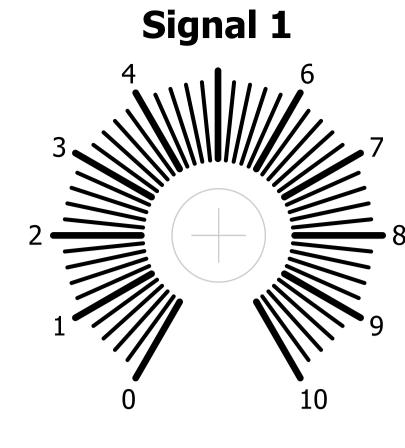




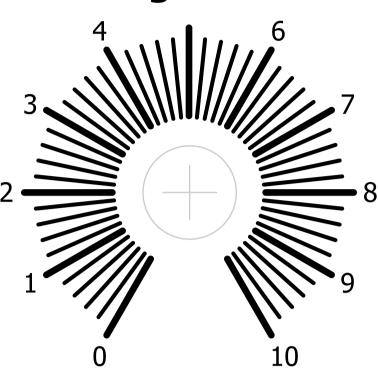


#### **VCF 24**

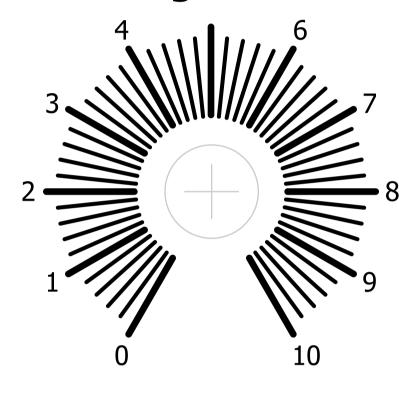




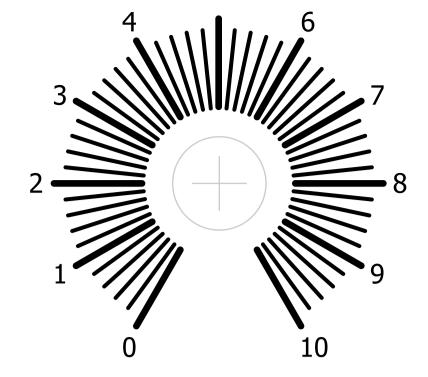
Signal 2



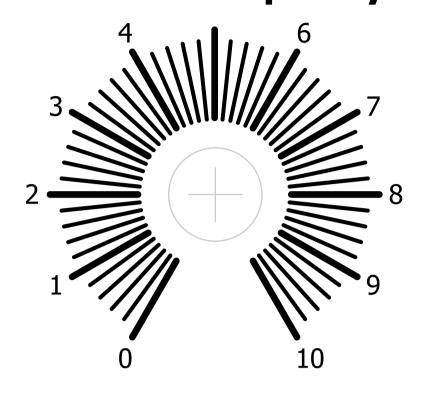
Signal 3



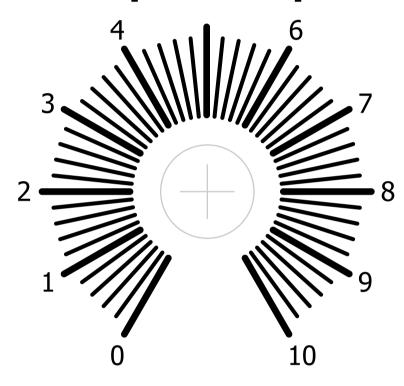
Resonance



**Cut-Off Frequency** 



**Freq Mod Depth** 





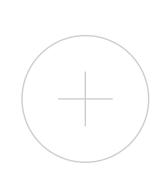
Signal 1 In



Signal 2 In



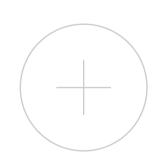
Signal 3 In



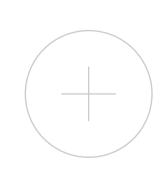
Cut-Off CV In



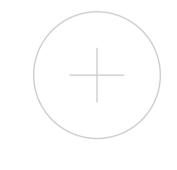
Freq Mod In



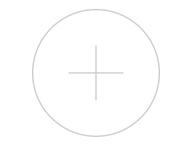
**Resonance CV In** 



**Cut-Off CV In** 



**Low-Pass Out** 





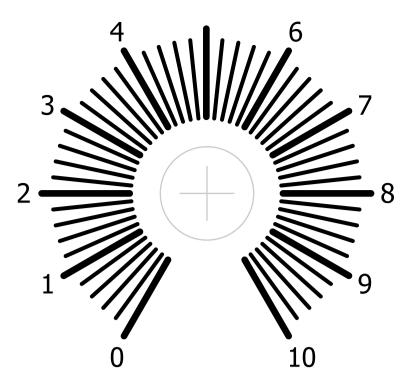




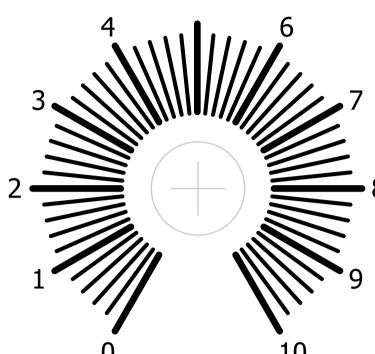
#### **ADSR**



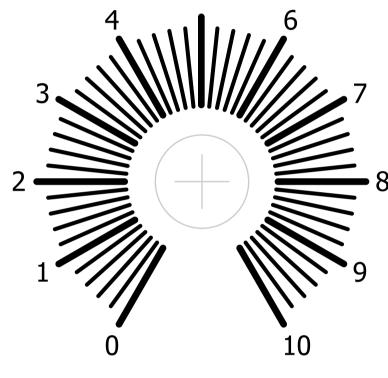




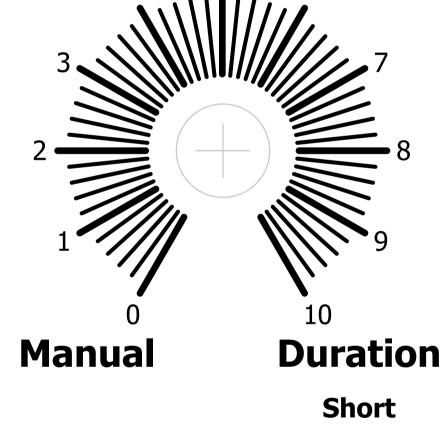
**Decay** 



Sustain



Release .













MFOS

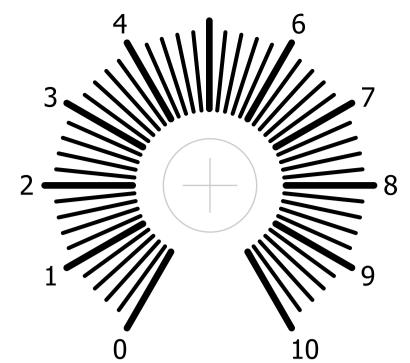




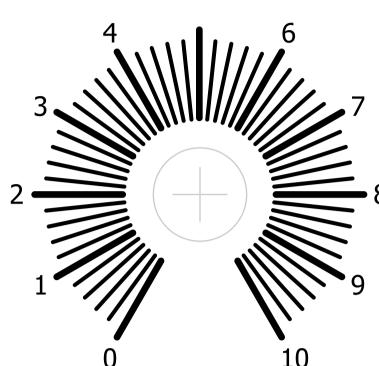
#### **VCA**







#### VCA 2 Gain



#### VCA 1

VCA 2

Response Log



Response

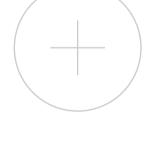


Linear



Input





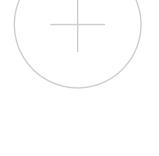


**Gain CV In** 



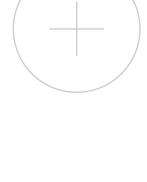


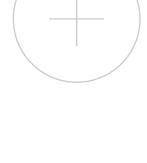






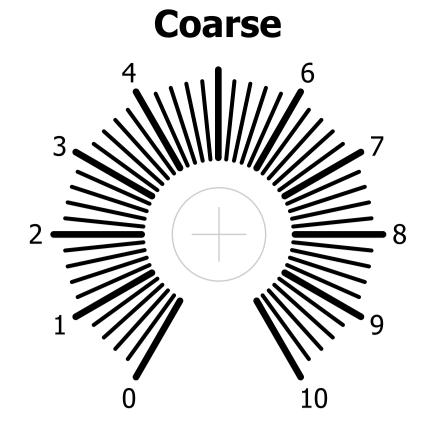












Fine

3

4

7

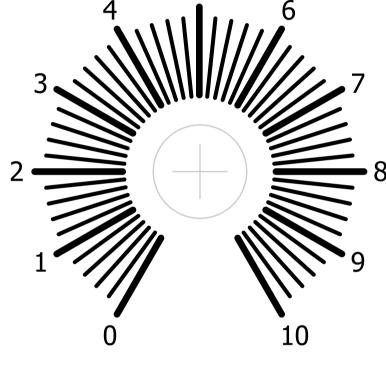
2

1

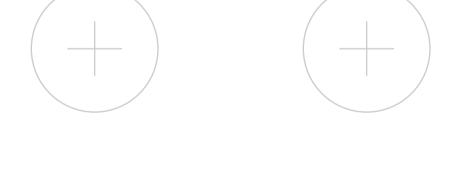
0

10



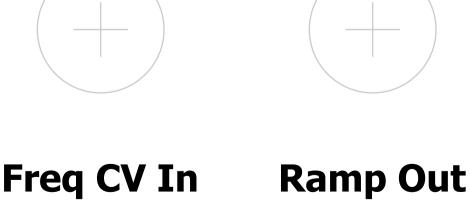


**Square Out** Sine Out



**PWM CV In** Triangle Out







+ MFOS









On





On







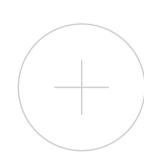




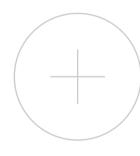


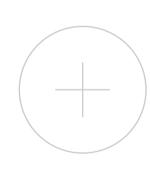


Bank 2

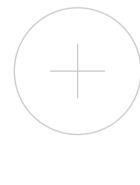




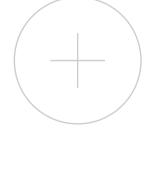


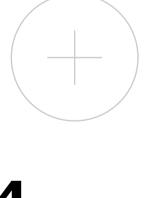


Bank 3



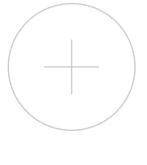






Bank 4





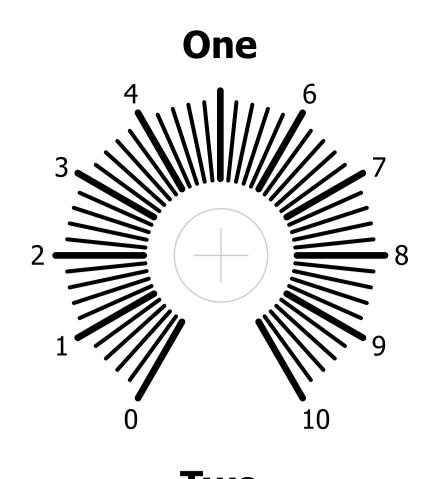


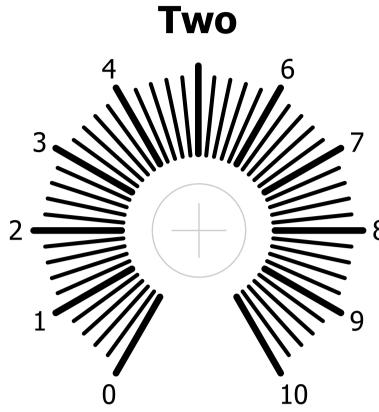
LukeLabs

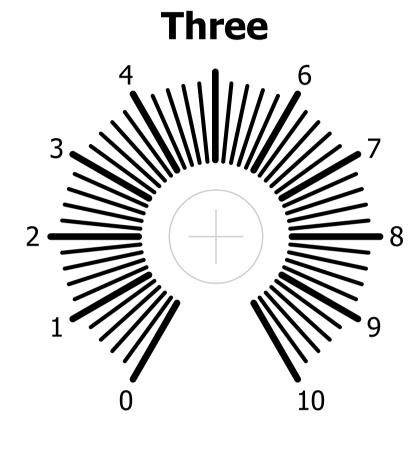
















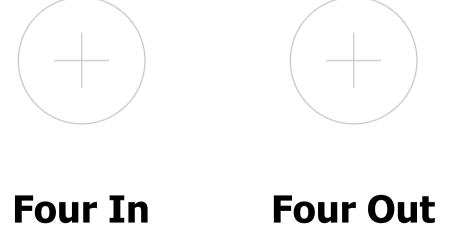
**One Out** 

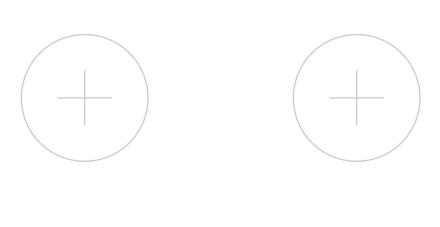
**Two Out** 

Two In



**Three In** Three Out



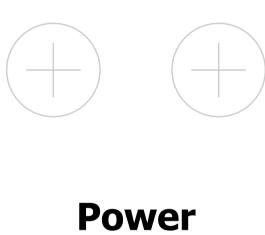




LukeLabs







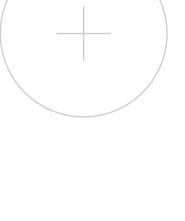
+12V

-12V

Off

On

12V 1A





LukeLabs

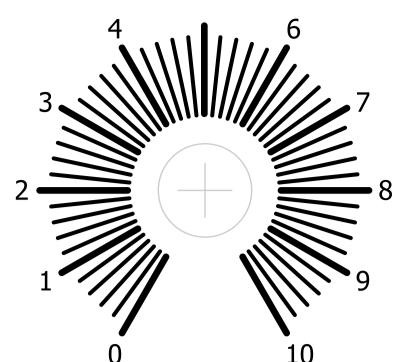




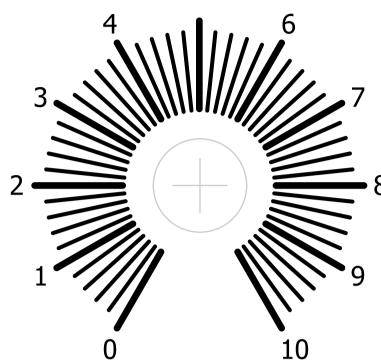
#### DMOD



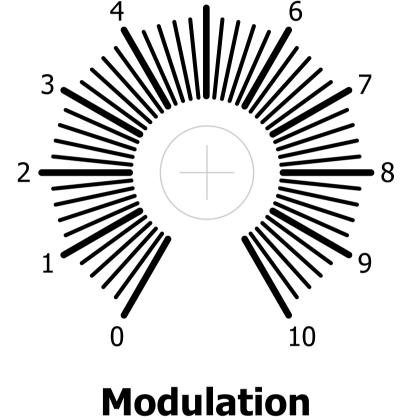




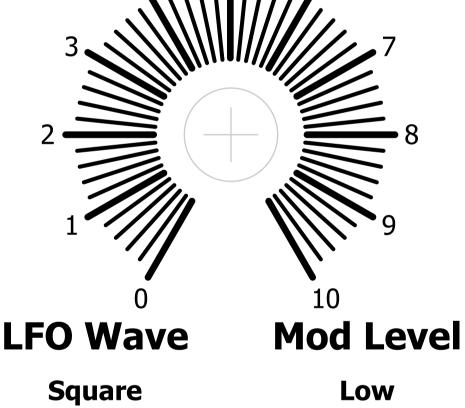
#### Release

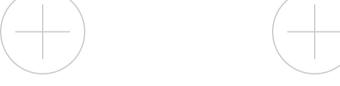


#### LFO Frequency



#### 4 .... 6



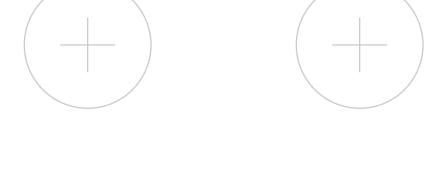


High



Sine







MFOS

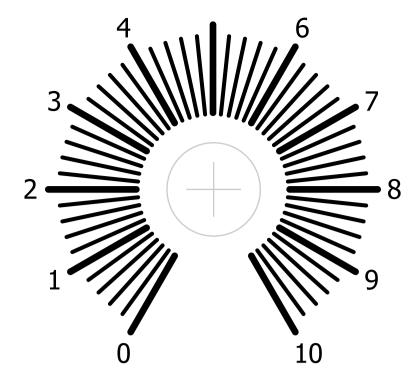




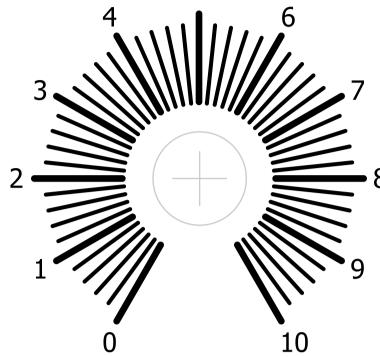
## S&H



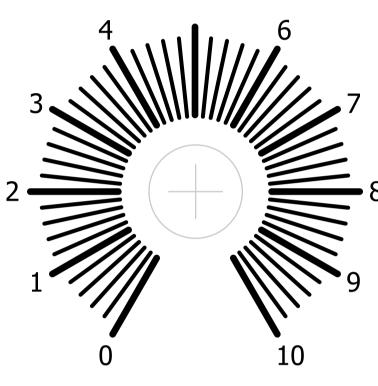




Sample Rate



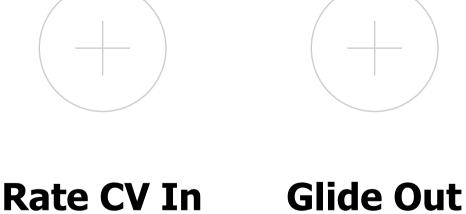
Glide



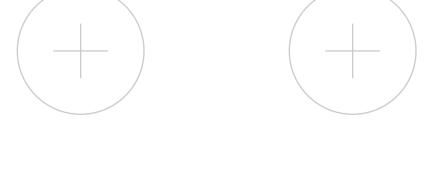
Sample Rate



Signal In Out









**MFOS** 

