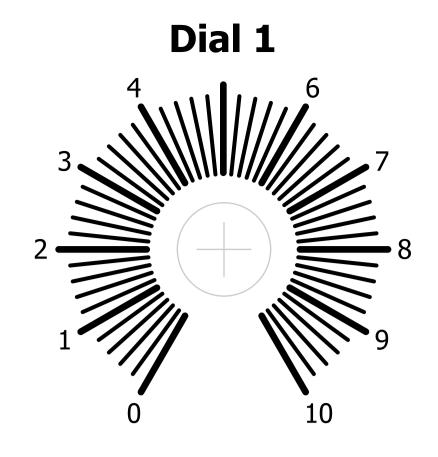
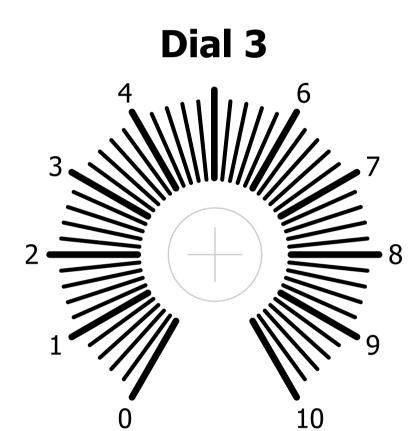
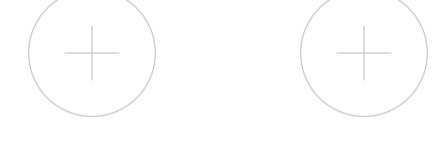
110 HEAD



Dial 2

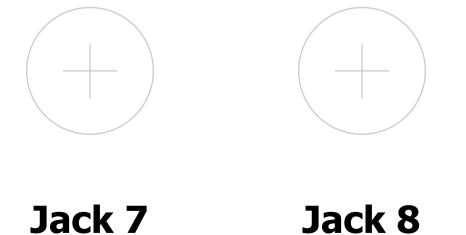


Jack 1 Jack 2



Jack 3 Jack 4

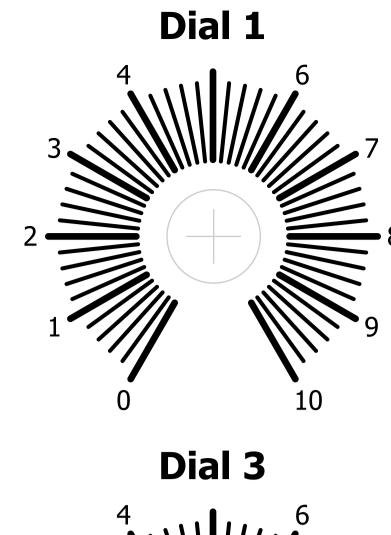


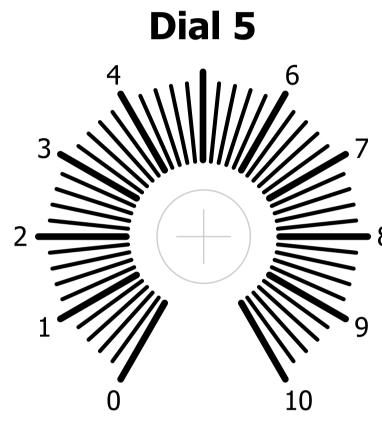


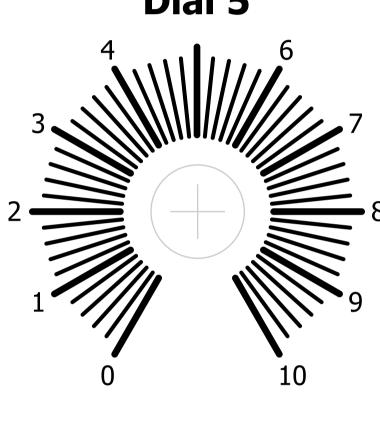


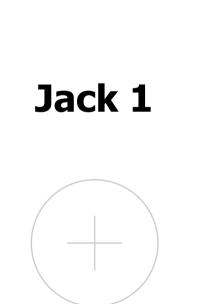
2U HEADER











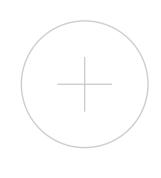
Jack 4

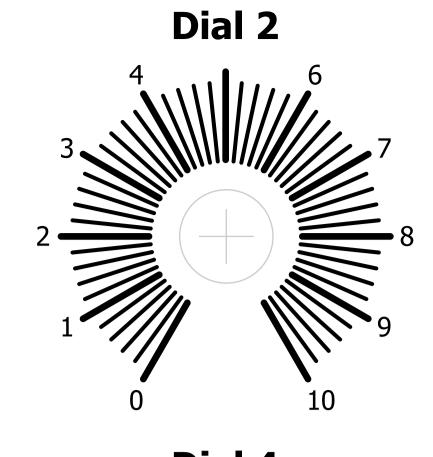


Jack 7

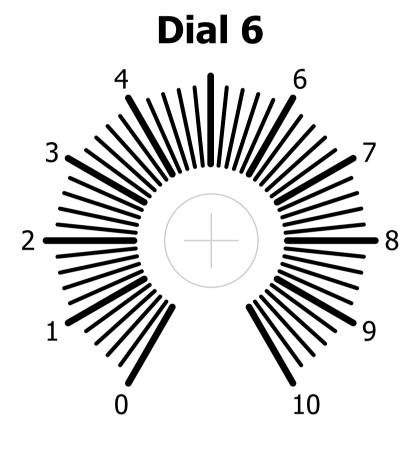


Jack 10





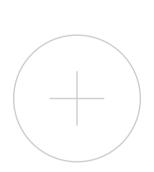
Dial 4 10



Jack 2



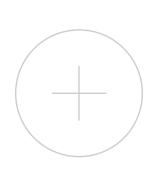
Jack 5



Jack 8



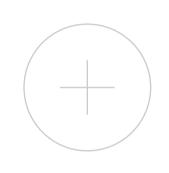
Jack 11



Jack 3



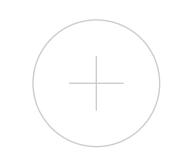
Jack 6

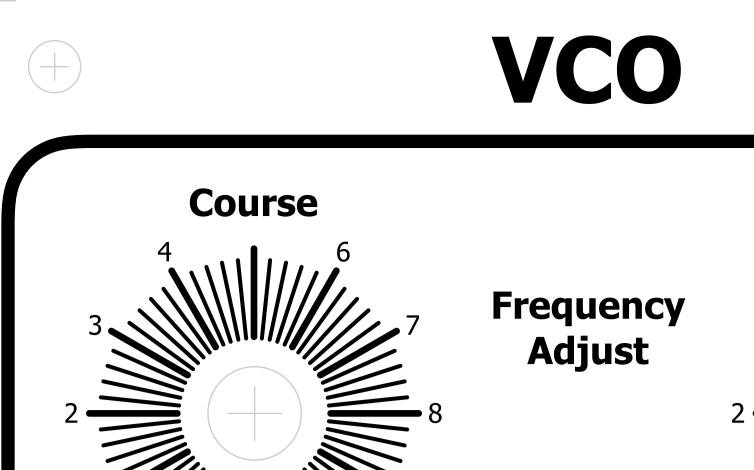


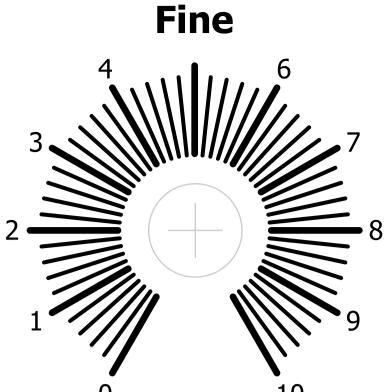
Jack 9

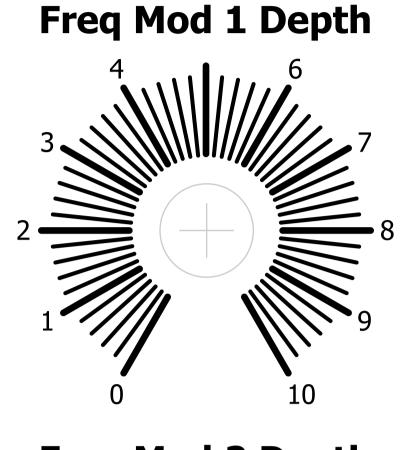


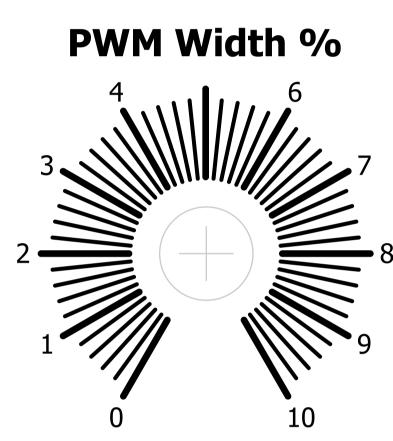
Jack 12

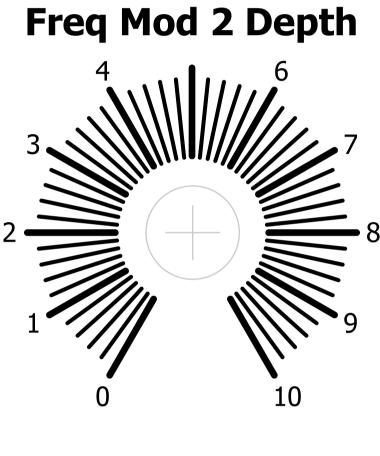


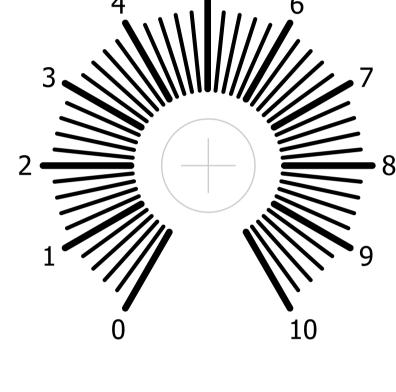


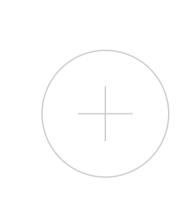




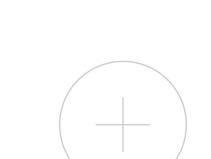






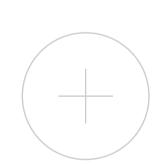


Freq Mod 1 In



PWM CV In

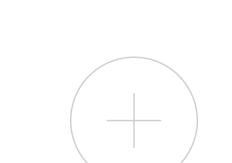












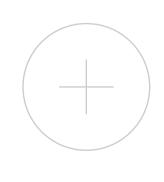
Triangle Out



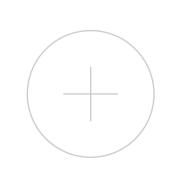
CV In

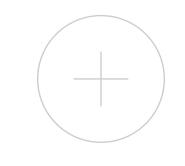
Ramp Out

Square Out



CV Linear In

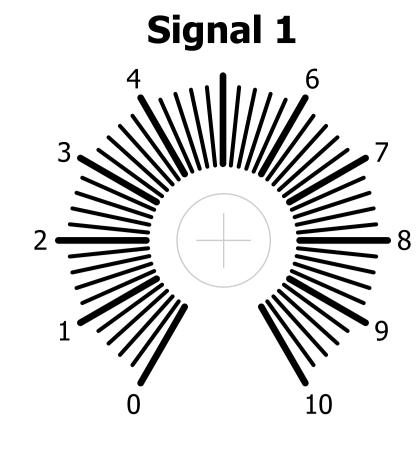




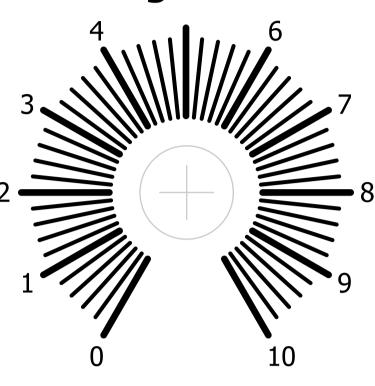
\bigcirc

VCF 12

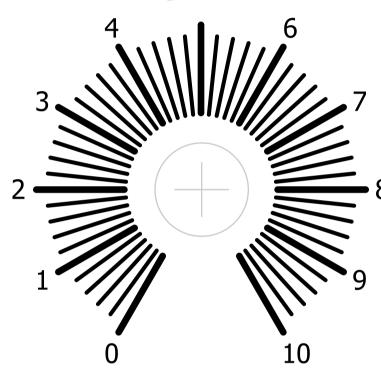




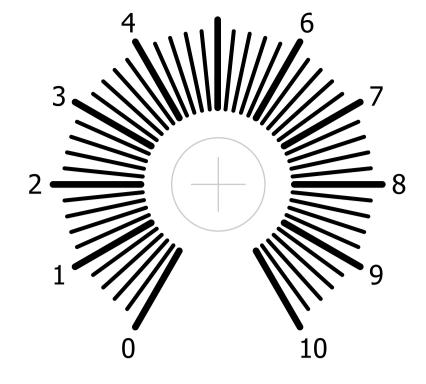
Signal 2



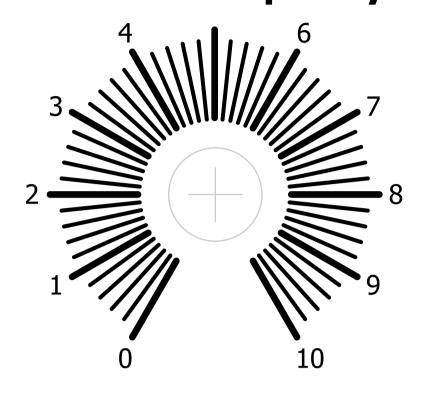
Signal 3



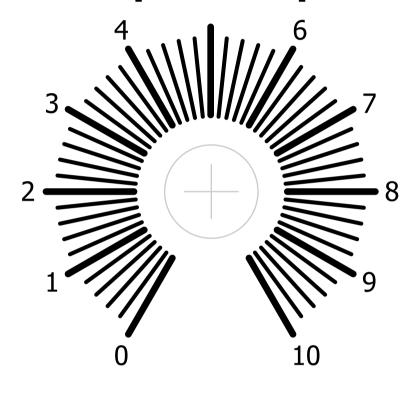
Resonance



Cut-Off Frequency



Freq Mod Depth

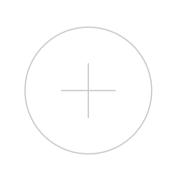




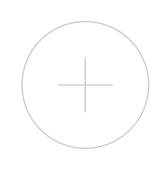
Signal 1 In



Signal 2 In



Signal 3 In



Cut-Off CV In



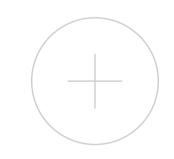
Freq Mod In



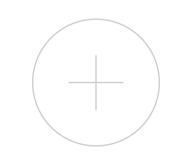
Resonance CV In



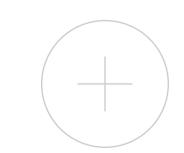
High-Pass Out



Band-Pass Out



Low-Pass Out



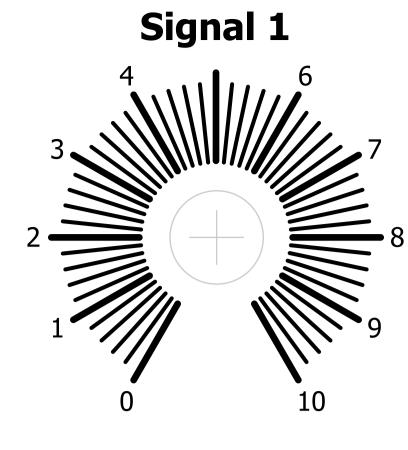




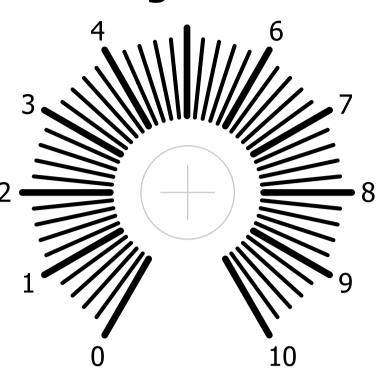


VCF 24

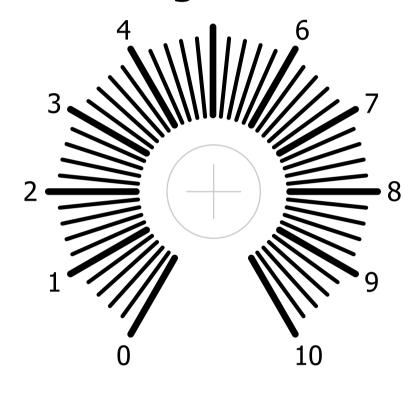




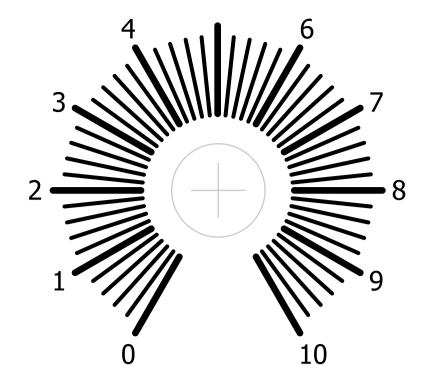
Signal 2



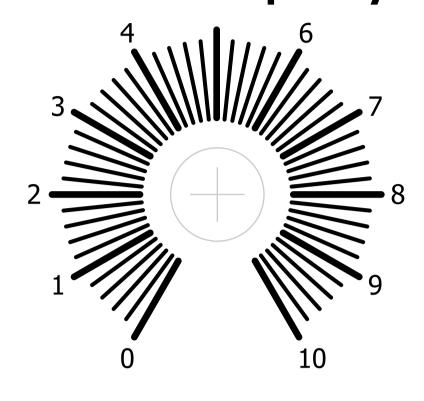
Signal 3



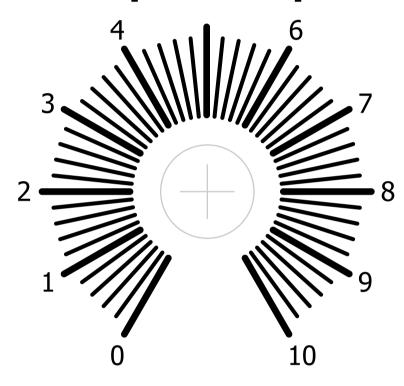
Resonance



Cut-Off Frequency



Freq Mod Depth





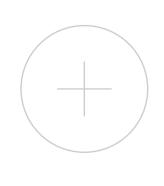
Signal 1 In



Signal 2 In



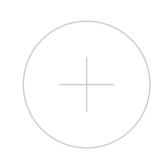
Signal 3 In



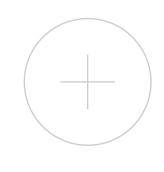
Cut-Off CV In



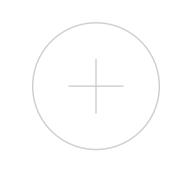
Freq Mod In



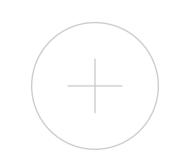
Resonance CV In



Cut-Off CV In



Low-Pass Out





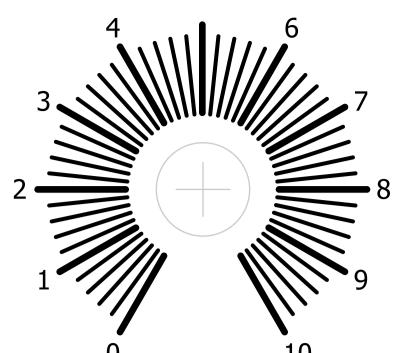
LukeLabs.com / MFOS



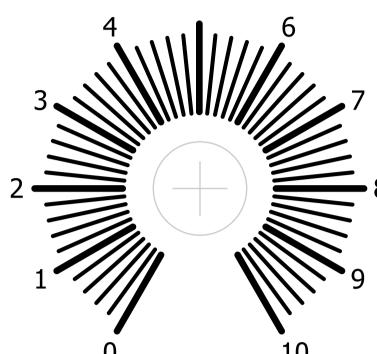
ADSR



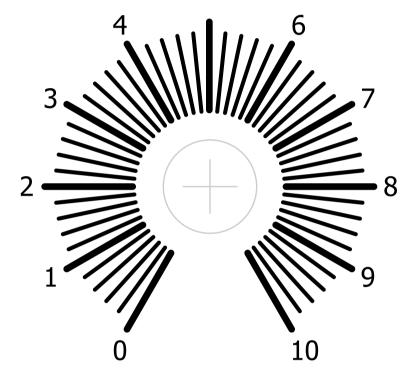




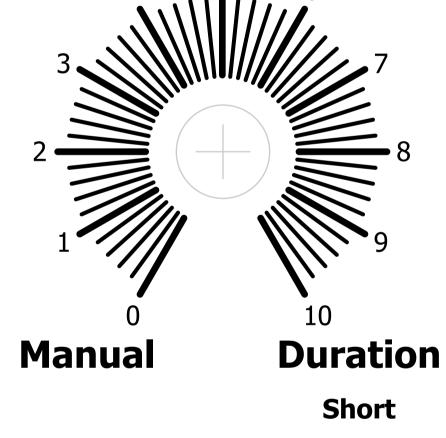
Decay

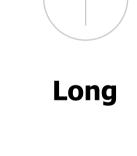


Sustain

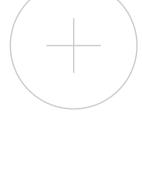


Release .





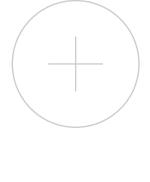
Gate In



Trigger In



Out





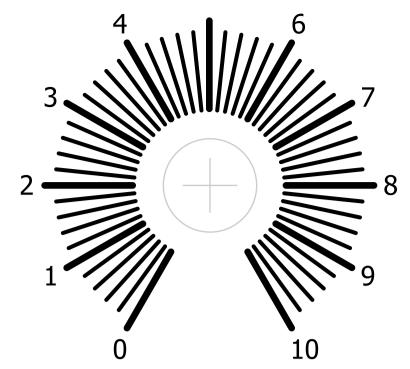




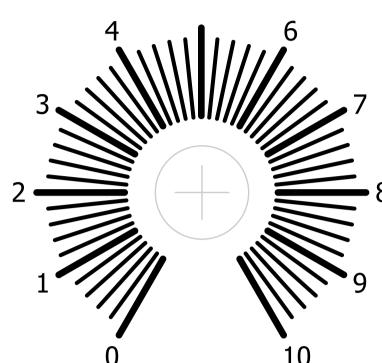
VCA







VCA 2 Gain



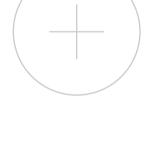
VCA 1

Response Log



Input

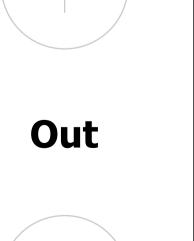
Linear



Gain CV In







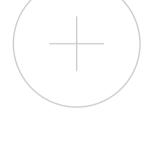
VCA 2

Response Log



Input

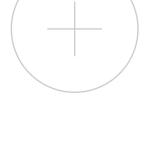
Linear



Gain CV In







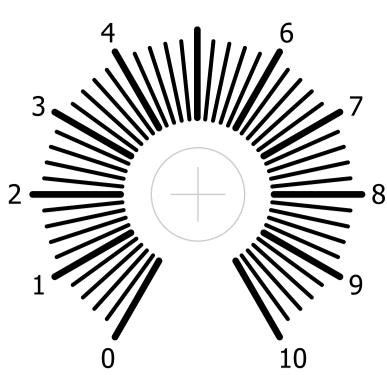




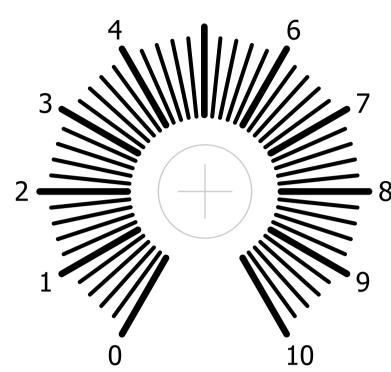




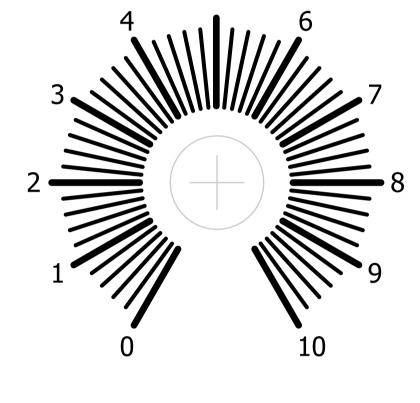




Fine

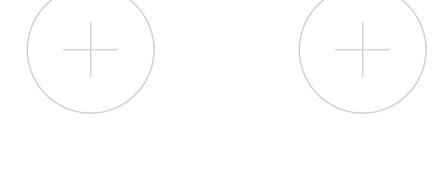


PWM Width %

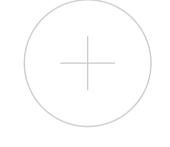


Square Out Sine Out

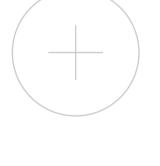




PWM CV In Triangle Out







Freq CV In

Ramp Out











On

Link 3/4
Off



On





Bank 1

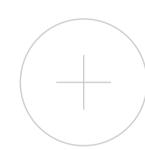




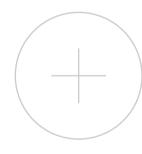


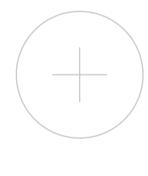


Bank 2









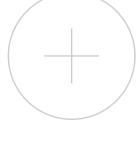
Bank 3













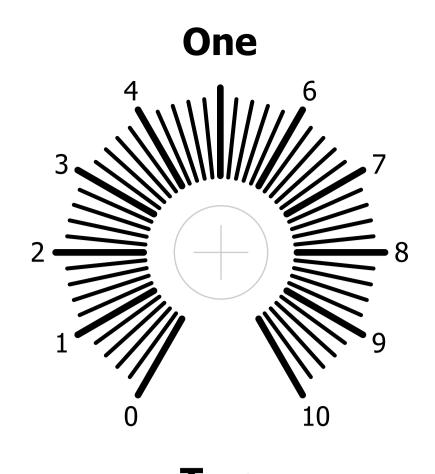
+

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Two

3

4

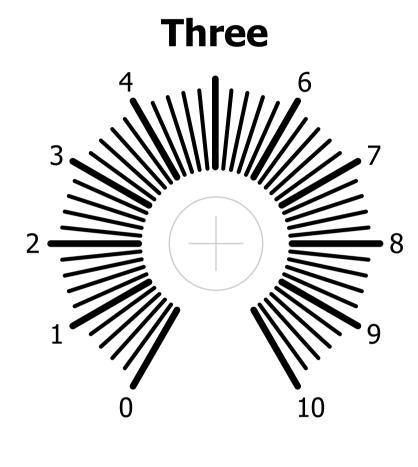
6

7

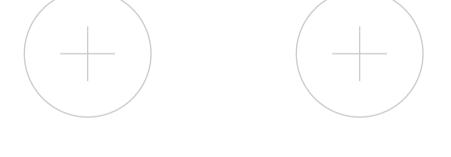
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0

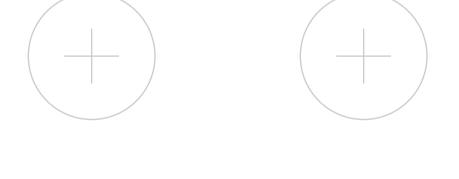
10





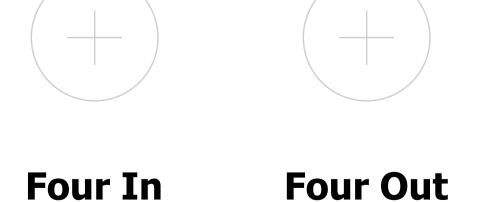


Two In Two Out





Three In Three Out

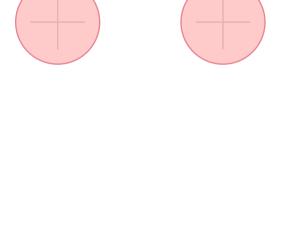






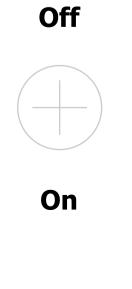






+12V

-12V



Power



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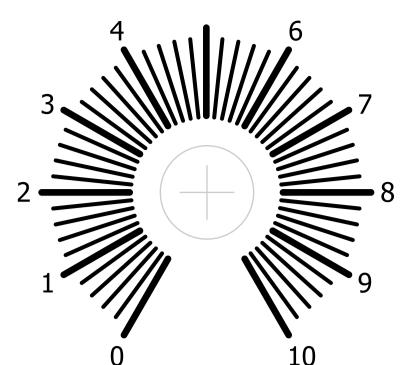




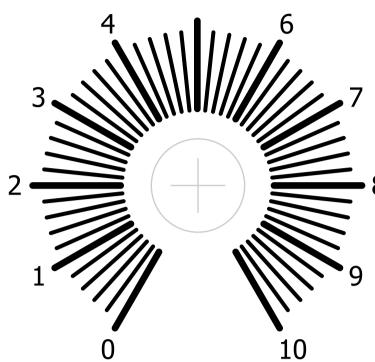
DMOD



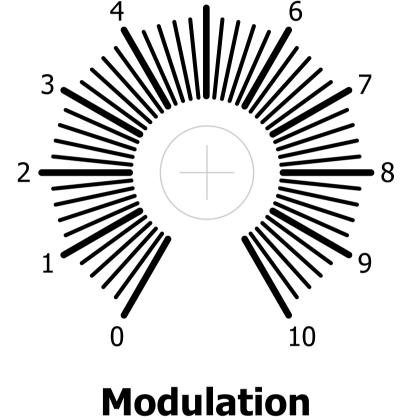


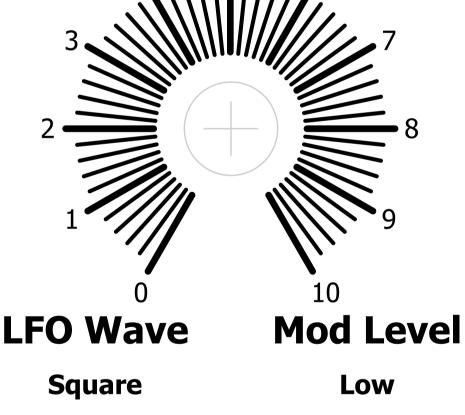


Release



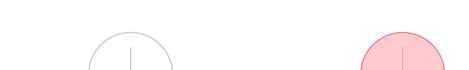
LFO Frequency







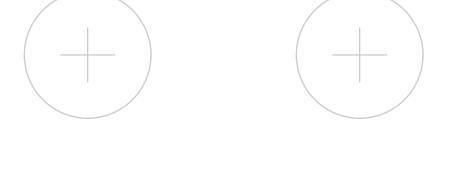
Active



Input Type

Gated







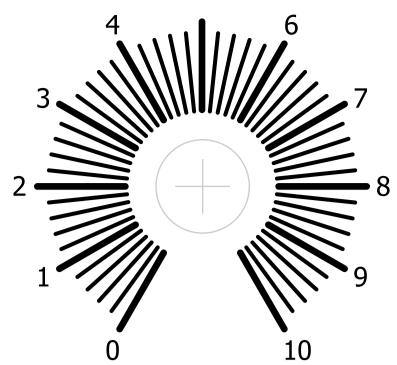




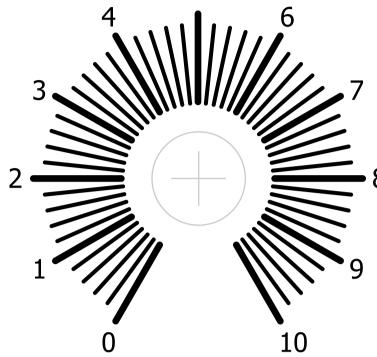




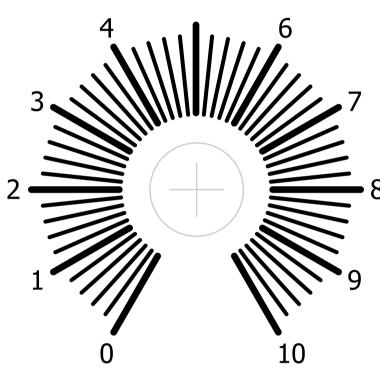




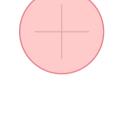
Sample Rate



Glide

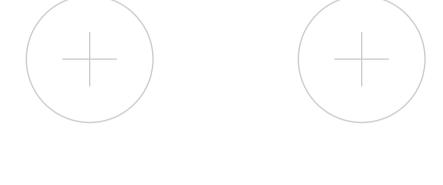


Sample Rate



Out

Signal In



Rate CV In Glide Out







