Understanding analog to digital converter specifications

Len Staller - February 24, 2005

Confused by analog-to-digital converter specifications? Here's a primer to help you decipher them and make the right decisions for your project.

Although manufacturers use common terms to describe analog-to-digital converters (ADCs), the way ADC makers specify the performance of ADCs in data sheets can be confusing, especially for a newcomers. But to select the correct ADC for an application, it's essential to understand the specifications. This guide will help engineers to better understand the specifications commonly posted in manufacturers' data sheets that describe the performance of successive approximation register (SAR) ADCs.

ABCs of ADCs

ADCs convert an analog signal input to a digital output code. ADC measurements deviate from the ideal due to variations in the manufacturing process common to all integrated circuits (ICs) and through various sources of inaccuracy in the analog-to-digital conversion process. The ADC performance specifications will quantify the errors that are caused by the ADC itself.

ADC performance specifications are generally categorized in two ways: DC accuracy and dynamic performance. Most applications use ADCs to measure a relatively static, DC-like signal (for example, a temperature sensor or strain-gauge voltage) or a dynamic signal (such as processing of a voice signal or tone detection). The application determines which specifications the designer will consider the most important.

For example, a DTMF decoder samples a telephone signal to determine which button is depressed on a touchtone keypad. Here, the concern is the measurement of a signal's power (at a given set of frequencies) among other tones and noise generated by ADC measurement errors. In this design, the engineer will be most concerned with dynamic performance specifications such as signal-to-noise ratio and harmonic distortion. In another example, a system may measure a sensor output to determine the temperature of a fluid. In this case, the DC accuracy of a measurement is prevalent so the offset, gain, and nonlinearities will be most important.

DC accuracy

Many signals remain relatively static, such as those from temperature sensors or pressure transducers. In such applications, the measured voltage is related to some physical measurement, and the absolute accuracy of the voltage measurement is important. The ADC specifications that describe this type of accuracy are *offset error, full-scale error, differential nonlinearity (DNL)*, and *integral nonlinearity (INL)*. These four specifications build a complete description of an ADC's absolute accuracy.

Although not a specification, one of the fundamental errors in ADC measurement is a result of the data-conversion process itself: *quantization error*. This error cannot be avoided in ADC measurements. DC accuracy, and resulting absolute error are determined by four specs—offset, full-scale/gain error, INL, and DNL. Quantization error is an artifact of representing an analog signal with a digital number (in other words, an artifact of analog-to-digital conversion). Maximum quantization error is determined by the resolution of the measurement (resolution of the ADC, or measurement if signal is oversampled). Further, quantization error will appear as noise, referred to as *quantization noise* in the dynamic analysis. For example, quantization error will appear as the noise floor in an FFT plot of a measured signal input to an ADC, which I'll discuss later in the dynamic performance section).

The ideal transfer function

The transfer function of an ADC is a plot of the voltage input to the ADC versus the code's output by the ADC. Such a plot is not continuous but is a plot of 2^N codes, where N is the ADC's resolution in bits. If you were to connect the codes by lines (usually at code-transition boundaries), the ideal transfer function would plot a straight line. A line drawn through the points at each code boundary would begin at the origin of the plot, and the slope of the plot for each supplied ADC would be the same as shown in Figure 1.

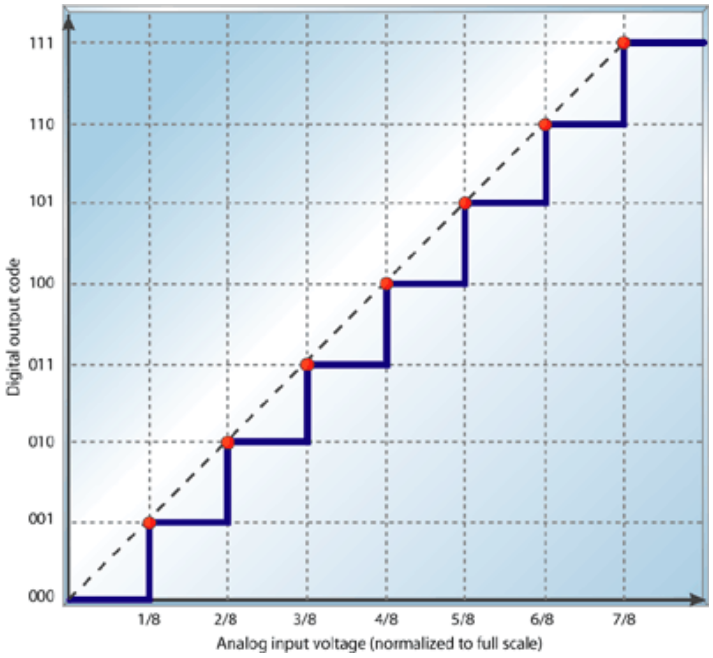

Figure 1: Ideal transfer function of a 3-bit ADC

Figure 1 depicts an ideal transfer function for a 3-bit ADC with reference points at code transition boundaries. The output code will be its lowest (000) at less than 1/8 of the full-scale (the size of this ADC's code width). Also, note that the ADC reaches its full-scale output code (111) at 7/8 of full scale, not at the full-scale value. Thus, the transition to the maximum digital output does not occur at full-scale input voltage. The transition occurs at one code width—or least significant bit (LSB)—less than full-scale input voltage (in other words, voltage reference voltage).

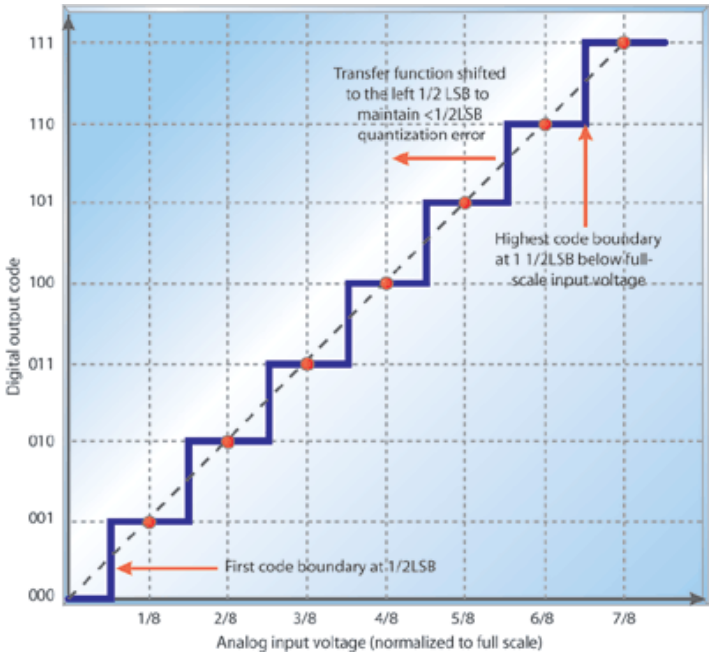

Figure 2: 3-bit ADC transfer function with - 1/2 LSB offset

The transfer function can be implemented with an offset of - 1/2 LSB, as shown in Figure 2. This shift of the transfer function to the left shifts the quantization error from a range of (- 1 to 0 LSB) to (- 1/2 to +1/2 LSB). Although this offset is intentional, it's often included in a data sheet as part of offset error (see section on offset error).

Limitations in the materials used in fabrication mean that real-world ADCs won't have this perfect transfer function. It's these deviations from the perfect transfer function that define the DC accuracy and are characterized by the specifications in a data sheet.

The DC performance specifications described have accompanying figures that depict two transfer function segments: the ideal transfer function (solid, blue lines) and a transfer function that deviates from the ideal with the applicable error described (dashed, yellow line). This is done to better illustrate the meaning of the performance specifications.

Offset error, full-scale error

The ideal transfer function line will intersect the origin of the plot. The first code boundary will occur at 1 LSB as shown in Figure 1. You can observe *offset error* as a shifting of the entire transfer function left or right along the input voltage axis, as shown in Figure 3.

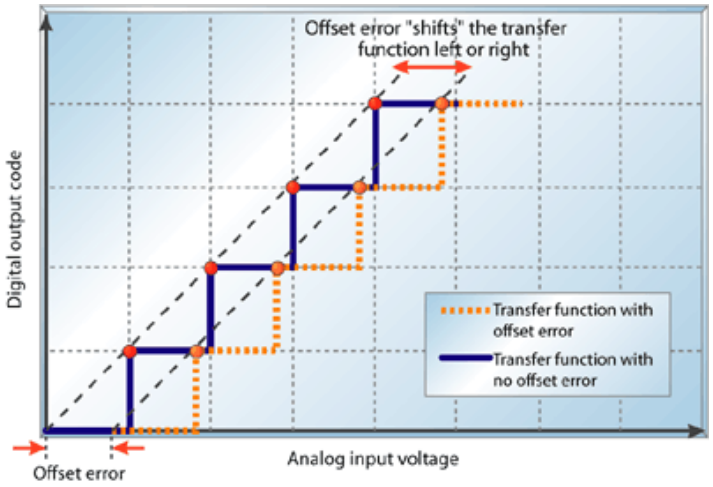

Figure 3: Offset error

An error of - 1/2 LSB is intentionally introduced into some ADCs but is still included in the specification in the data sheet. Thus, the offset-error specification posted in the data sheet includes 1/2 LSB of offset by design. This is done to shift the potential quantization error in a measurement from 0 to 1 LSB to - 1/2 to +1/2 LSB. In this way, the magnitude of quantization error is intended to be < 1/2 LSB, as Figure 4 illustrates.

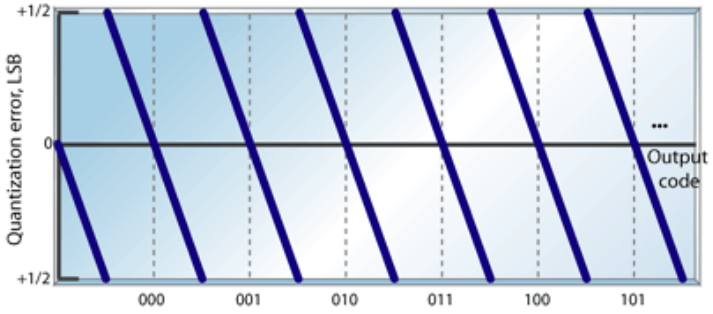

Figure 4: Quantization error vs. output code

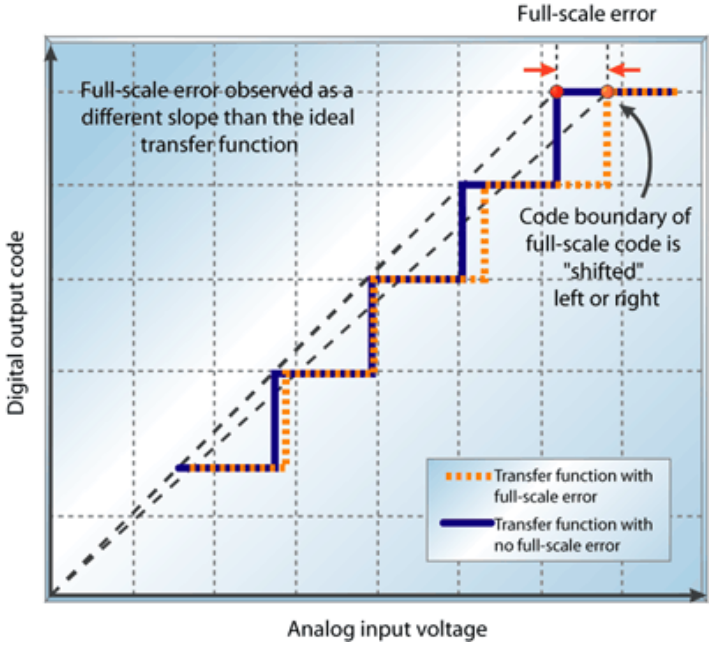

Figure 5: Full-scale error

Full-scale error is the difference between the ideal code transition to the highest output code and the actual transition to the output code when the offset error is zero. This is observed as a change in slope of the transfer function line as shown in Figure 5. A similar specification, gain error, also describes the nonideal slope of the transfer function as well as what the highest code transition would be without the offset error. Full-scale error accounts for both gain and offset deviation from the ideal transfer function. Both full-scale and gain errors are commonly used by ADC manufacturers.

Nonlinearity

Ideally, each code width (LSB) on an ADC's transfer function should be uniform in size. For example, all codes in Figure 2 should represent exactly 1/8th of the ADC's full-scale voltage reference. The difference in code widths from one code to the next is *differential nonlinearity (DNL)*. The code width (or LSB) of an ADC is shown in Equation 1.

$$\text{LSB} = \frac{V_{ref}}{2^N}$$

(Equation 1)

The voltage difference between each code transition should be equal to one LSB, as defined in Equation 1. Deviation of each code from an LSB is measured as DNL. This can be observed as uneven spacing of the code "steps" or transition boundaries on the ADC's transfer-function plot. In Figure 6, a selected digital output code width is shown as larger than the previous code's step size. This difference is DNL error. DNL is calculated as shown in Equation 2.

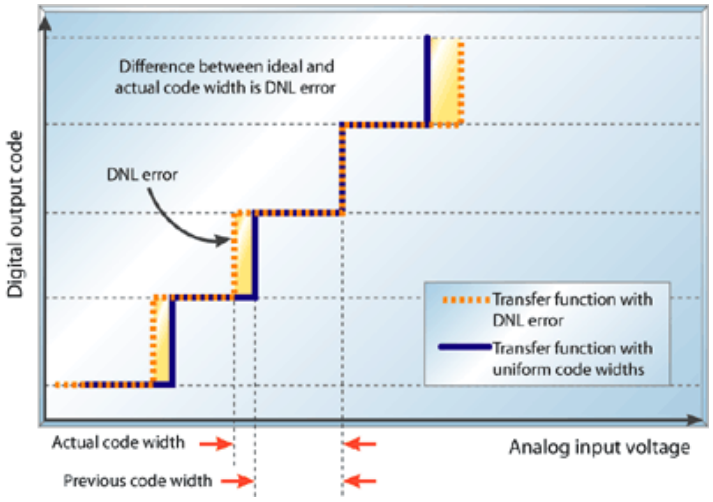

Figure 6: Differential nonlinearity

$$\text{DNL} = \frac{\left(V_{n+1} - V_n\right)}{V_{LSB}}$$

(Equation 2)

The *integral nonlinearity (INL)* is the deviation of an ADC's transfer function from a straight line. This line is often a best-fit line among the points in the plot but can also be a line that connects the highest and lowest data points, or endpoints. INL is determined by measuring the voltage at which all code transitions occur and comparing them to the ideal. The difference between the ideal voltage levels at which code transitions occur and the actual voltage is the INL error, expressed in LSBs. INL error at any given point in an ADC's transfer function is the accumulation of all DNL errors of all previous (or lower) ADC codes, hence it's called *integral* nonlinearity. This is observed as the deviation from a straight-line transfer function, as shown in Figure 7.

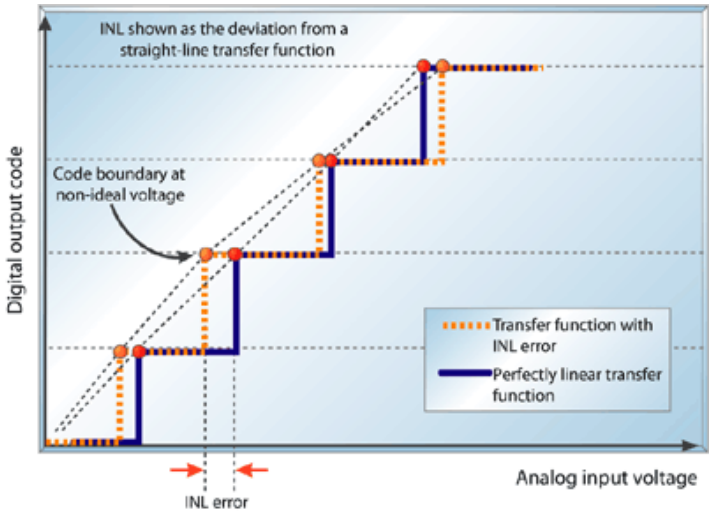

Figure 7: Integral nonlinearity error

Because nonlinearity in measurement will cause distortion, INL will also affect the dynamic performance of an ADC.

Absolute error

The *absolute error* is the total DC measurement error and is characterized by the offset, full-scale, INL, and DNL errors. Quantization error also affects accuracy, but it's inherent in the analog-to-digital conversion process (and so does not vary from one ADC to another of equal resolution). When designing with an ADC, the engineer uses the performance specifications posted in the data sheet to calculate the maximum absolute error that can be expected in the measurement, if it's important. Offset and full-scale errors can be reduced by calibration at the expense of dynamic range and the cost of the calibration process itself. Offset error can be minimized by adding or subtracting a constant number to or from the ADC output codes. Full-scale error can be minimized by multiplying the ADC output codes by a correction factor. Absolute error is less important in some applications, such as closed-loop control, where DNL is most important.

Dynamic performance

An ADC's dynamic performance is specified using parameters obtained via frequency-domain analysis and is typically measured by performing a fast Fourier transform (FFT) on the output codes of the ADC. In Figure 8, the fundamental frequency is the input signal frequency. This is the signal measured with the ADC. Everything else is noise—the unwanted signals—to be characterized with respect to the desired signal. This includes harmonic distortion, thermal noise, $1/f$ noise, and quantization noise. (The figure is exaggerated for ease of observation.) Some sources of noise may not derive from the ADC itself. For example, distortion and thermal noise originate from the external circuit at the input to the ADC. Engineers minimize outside sources of error when assessing the performance of an ADC and in their system design.

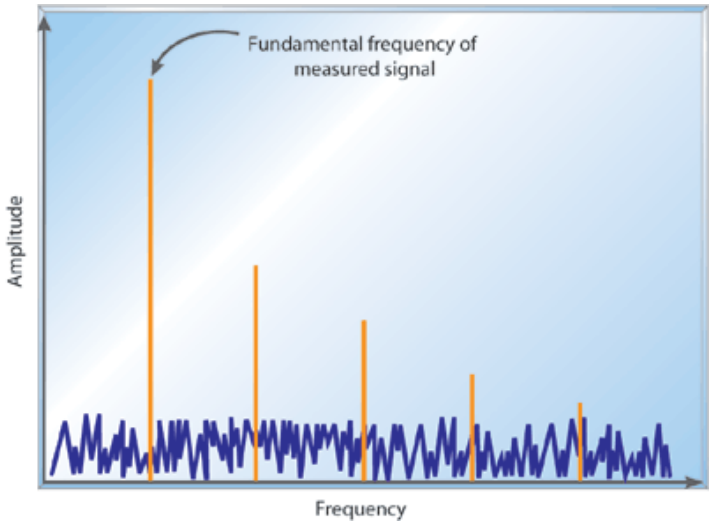

Figure 8: An FFT of ADC output codes

Signal-to-noise ratio

The *signal-to-noise ratio (SNR)* is the ratio of the root mean square (RMS) power of the input signal to the RMS noise power (excluding harmonic distortion), expressed in decibels (dB), as shown in Equation 3.

$$\mathrm{SNR(dB)} = 20\log\left(\frac{V_{signal(rms)}}{V_{noise(rms)}}\right)$$

(Equation 3)

SNR is a comparison of the noise to be expected with respect to the measured signal. The noise measured in an SNR calculation doesn't include harmonic distortion but does include quantization noise (an artifact of quantization error) and all other sources of noise (for example, thermal noise). This noise floor is depicted in the FFT plot in Figure 9. For a given ADC resolution, the quantization noise is what limits an ADC to its theoretical best SNR because quantization error is the only error in an ideal ADC. The theoretical best SNR is calculated in Equation 4.

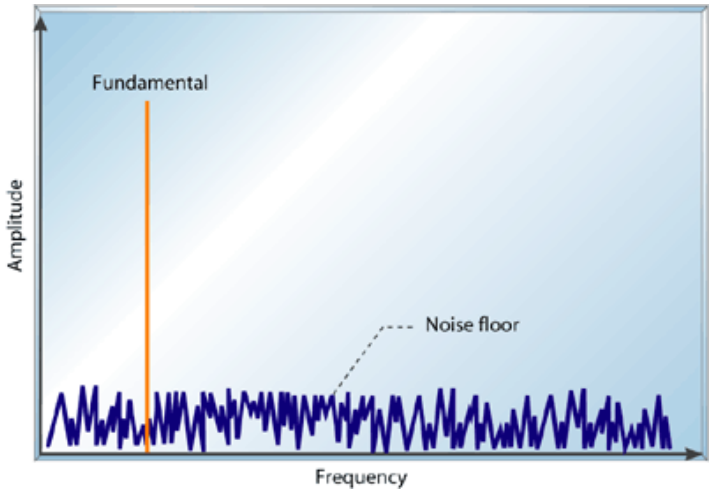

Figure 9: SNR— A measure of the signal compared to the noise floor

SNR(dB)=6.02N+1.76 (4)
Where N is the ADC resolution
(Equation 4)

Quantization noise can only be reduced by making a higher-resolution measurement (in other words, a higher-resolution ADC or oversampling). Other sources of noise include thermal noise, $1/f$ noise, and sample clock jitter.

Harmonic distortion

Nonlinearity in the data converter results in harmonic distortion when analyzed in the frequency domain. Such distortion is observed as "spurs" in the FFT at harmonics of the measured signal as illustrated in Figure 10. This distortion is referred to as *total harmonic distortion (THD)*, and its power is calculated in Equation 5.

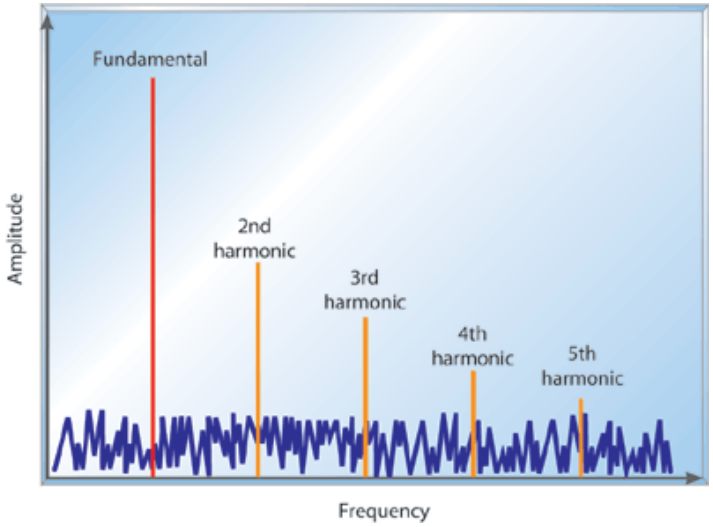

Figure 10: FFT showing harmonic distortion

$$\mathrm{THD} = 20\log\left(\frac{\sqrt{V_2^2 + V_3^2 + \ldots + V_n^2}}{V_1}\right)$$

(Equation 5)

The magnitude of harmonic distortion diminishes at high frequencies to the point that its magnitude is less than the noise floor or is beyond the bandwidth of interest. Data sheets typically specify to what order the harmonic distortion has been calculated. Manufacturers will specify which harmonic is used in calculating THD; for example, up to the fifth harmonic is common (see the example ADC specification in Table 1).

Table 1: Example: Silicon Labs C8051F060 16-bit ADC electrical characteristics

Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNITS**
DC accuracy					
Resolution					bits
Integral nonlinearity ()	Single-ended differential		0.75 0.5	2 1	LSB LSB
Integral nonlinearity ()	Single-ended differential		1.5 1	4 2	LSB
Differential nonlinearity	Guaranteed monotonic		0.5		LSB
Offset error			0.1		mV
Full-scale error			0.008		%F.S.
Gain temperature coefficient			TBD		ppm/ C
Dynamic performance	**Conditions**	**MIN**	**TYP**	**MAX**	**UNITS**
Signal-to-noise plus distortion	Fin = 10kHz, single-ended Fin = 10kHz, differential		86 89		dB dB
Total harmonic distortion	Fin = 10kHz, single-ended Fin = 10kHz, differential		96 103		dB dB
Spurious-free dynamic range	Fin = 10kHz, single-ended Fin = 10kHz, differential		97 104		dB dB
CMRR	Fin = 10kHz		86		dB
Channel isolation			100		dB

Timing	**Conditions**	**MIN**	**TYP**	**MAX**	**UNITS**
SAR clock frequency					MHz
Conversion time in SAR clocks					clocks
Track/hold acquisition time					ns
Throughput rate					Msps
Aperture delay	External CNVST signal		1.5		ns
RMS aperture jitter	External CNVST signal		5		ps
Analog inputs	**Conditions**	**MIN**	**TYP**	**MAX**	**UNITS**
Input voltage range	Single-ended (AIN-AING) differential (AIN-AIN)	0 -VREF		VREF VREF	V V
Input capacitance			80		pF
Operating input range	AIN or AIN AING or AING (DC only)	-0.2		AV+	V V
Power specifications	**Conditions**	**MIN**	**TYP**	**MAX**	**UNITS**
Power supply current (each ADC)	Operating mode, Msps AV+ AVDD Shutdown Mode	 4.0 1.5 1		mA mA mA	
	AVDD		1.5		mA
	Shutdown Mode		1		mA
Power-supply rejection	VDD 5%		0.5		LSB
VDD = 3.0V, AV+ = 3.0V, AVDD = 3.0V, VREF = 2.50V (REFBE=0), -40 C to +85 C unless otherwise specified					

Signal-to-noise and distortion

Signal-to-noise and distortion (SiNAD) offers a more complete picture by including the noise and harmonic distortion in one specification. SiNAD gives a description of how the measured signal will compare to the noise and distortion. You can calculate the SiNAD ratio using Equation 6.

$$\text{SiNAD} = 20\log\left(\frac{V_1}{\sqrt{V_2^2 + V_3^2 + \ldots + V_n^2 + V_{noise}^2}}\right)$$

(Equation 6)

Spurious-free dynamic range

Finally, *spurious-free dynamic range (SFDR)* is the difference between the magnitude of the measured signal and its highest spur peak. This spur is typically a harmonic of the measured signal but doesn't have to be. SFDR is shown in Figure 11.

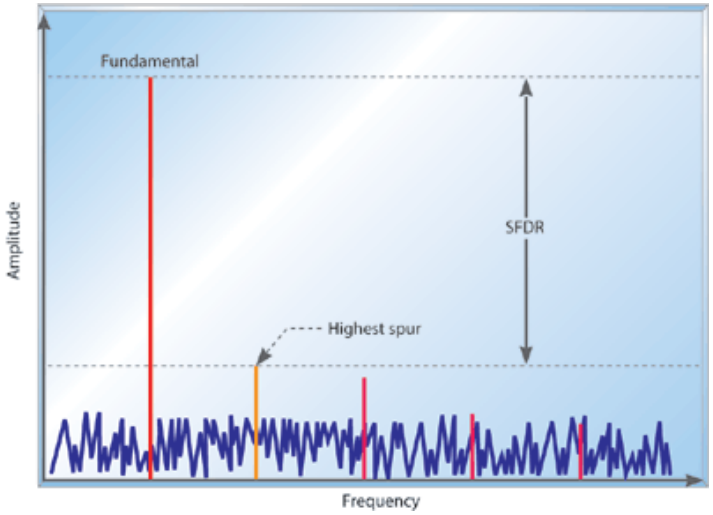

Figure 11: Spurious-free dynamic range (SFDR)

Reading ADC spec numbers

The ADC specifications posted in data sheets serve to define the performance of an ADC in different types of applications. The engineer uses these specifications to define if, how, and in what way the ADC should be used in an application. Performance specifications can also be a guarantee that an ADC will perform in a certain way. If a specification is labeled as a maximum or minimum, this is implied. For example, in the ADC specification shown in Table 1, the data sheet excerpt gives an INL error maximum of 1 LSB. This should mean the manufacturer has tested the ADC and is stating that INL error should not be greater or less than 1 LSB. Besides minimum and maximum, specifications listed as typical are also given. This is not a guarantee but simply represents typical performance for that ADC. For example, if a data sheet specifies 2 LSB INL in the "Typical" column, there's no implied guarantee that the engineer won't find the ADC with higher INL error.

Though a typical number is not a guarantee, it should give the designer an idea of how the ADC will perform, since these numbers are generally derived from the manufacturer's characterization data or are expected by design. Typical numbers are more helpful when the manufacturer gives the standard deviation from the mean of the tested specification. This gives the engineer more information on how the ADC's performance can be expected to deviate from the numbers posted as typical. Keep this in mind when comparing ADC data sheets, especially if the specification is critical to your design. An ADC with a typical 2 LSB INL may yield higher INL error than expected, making a 12-bit ADC effectively a 10-bit ADC—*caveat emptor*!

Len Staller serves as an applications engineer for Silicon Laboratories' microcontroller products. Previously, he was an applications engineer for Cygnal Integrated Products, which was acquired by Silicon Laboratories in 2003. Staller has a bachelor's degree in electrical engineering from The University of Texas at Austin. He can be reached at Len.Staller@silabs.com.