

The diagram illustrates the internal circuitry of a 100W RF PA module. It features an LT1013DIDR (U2) as the main power amplifier. The input stage is biased by RF_PA_1V1 and includes a 10k resistor (R3) connected to FWD_SENSE_IND. The output stage is biased by RF_PA_7V and includes a 100k resistor (R11) connected to GND. The output of the PA is connected to RF_PA_7V and includes a 10k resistor (R10) connected to RF_PA_VGG. The circuit also includes a 3nF capacitor (C2) connected to RF_PA_VGG and a 10k resistor (R9) connected to RF_PA_1V1. The input matching network consists of a 7k5 resistor (R1) in series with a 22k resistor (R2) in shunt to GND. The output matching network consists of a 2k2 resistor (R14) in series with a 100nF capacitor (C8) in shunt to GND. The circuit is powered by PWR_SPD and includes several test points (TP1, TP2, TP4) for measurement.

The schematic diagram shows the PA block implemented with the RA60H3847H1 component (U4). The component has four pins: Pin 1 (In) is connected to RF_IND; Pin 2 (VGG) is connected to RF_PA_VGG; Pin 3 (VDD) is connected to RF_PA_VDD; and Pin 4 (Out) is connected to DRF_OUT.

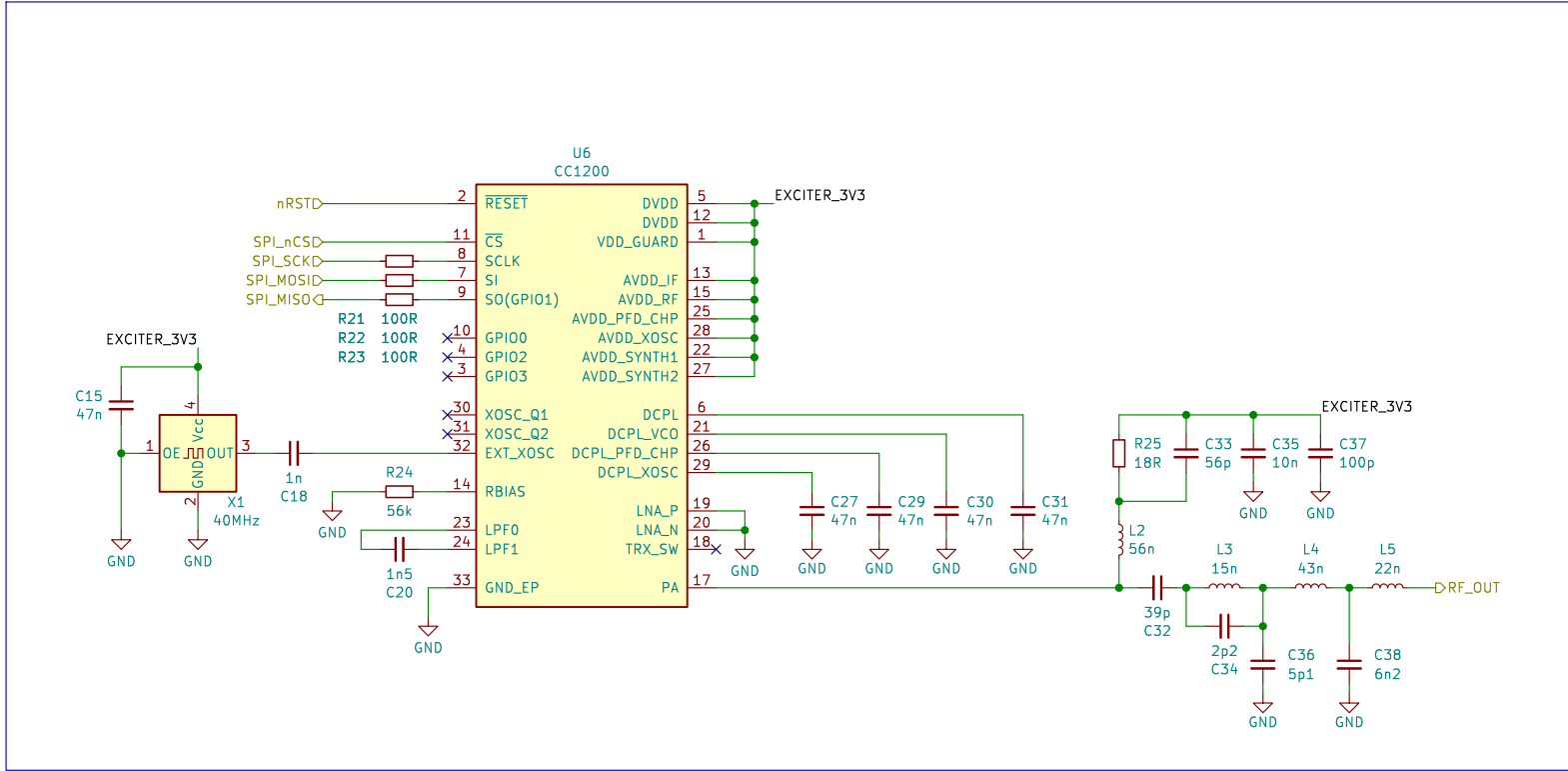
The circuit diagram shows a 13.8V input connected to the VI pin of the LM317SOT-223. A 100nF capacitor (C1) is connected between the input and ground. The output of the regulator is connected to the V0 pin, which is also connected to a 240R resistor (R6) and a 1k resistor (R7) in series with a 100R resistor (R8) to ground. A 100nF capacitor (C3) is connected between the output and ground. The output is also connected to a diode (D2) to ground. A feedback bead (FB1) is connected between the output and ground. A 1uF capacitor (C4) is connected between the output and ground. A 100nF capacitor (C6) and a 1nF capacitor (C7) are connected between the output and ground. A test point (TP3) is connected to the output. A diode (D1) is connected between the input and the output.

The schematic diagram illustrates the PA_VDD and PA_END circuit. It features a 13.8V input connected to a network of resistors and MOSFETs. A 100R resistor (R15) is connected to PA_END, which is also connected to a 10k resistor (R16) to GND. A 47k resistor (R17) is connected to the 13.8V input and a node labeled TP6. This node is connected to the gate of MOSFET Q1 (BSS138), which has its source to GND and drain to a node labeled TP5. TP5 is connected to the gate of MOSFET Q2 (NP100P04PDG), which has its source to GND and drain to RF_PA_VDD. RF_PA_VDD is also connected to a 100u/50V capacitor (C9) to GND and a diode (D4 SS1P4L) to GND. A diode (D3 SS1P4L) is connected from RF_PA_VDD to GND. The 13.8V input is also connected to a diode (D4 SS1P4L) to GND.

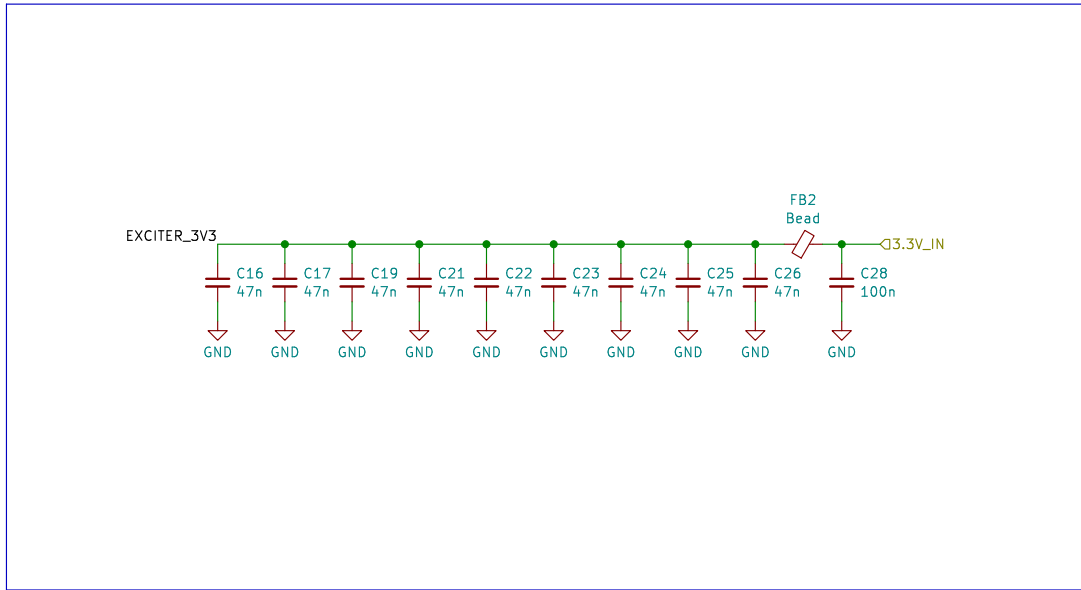
The schematic shows a buck converter circuit. The input is connected to a terminal block J1, specifically Conn_01x01_Pin. The input voltage is 13.8V_OUT, with a test point TP7. The input capacitor C10 is 22uF/6.3V. The input filter capacitor C11 is 100nF. The input resistor R18 is 100k. The IC is a TP6841S6, with pins 1 (BST), 2 (GND), 3 (FB), 4 (EN), 5 (VIN), and 6 (SW). The output is 3.3V_OUT, with a test point TP8. The output capacitor C14 is 22uF/6.3V. The output filter capacitor C12 is 100nF. The output inductor L1 is 10uH. The output resistor R19 is 24k. The output filter capacitor C13 is 100uF/50V. The output resistor R20 is 75k.

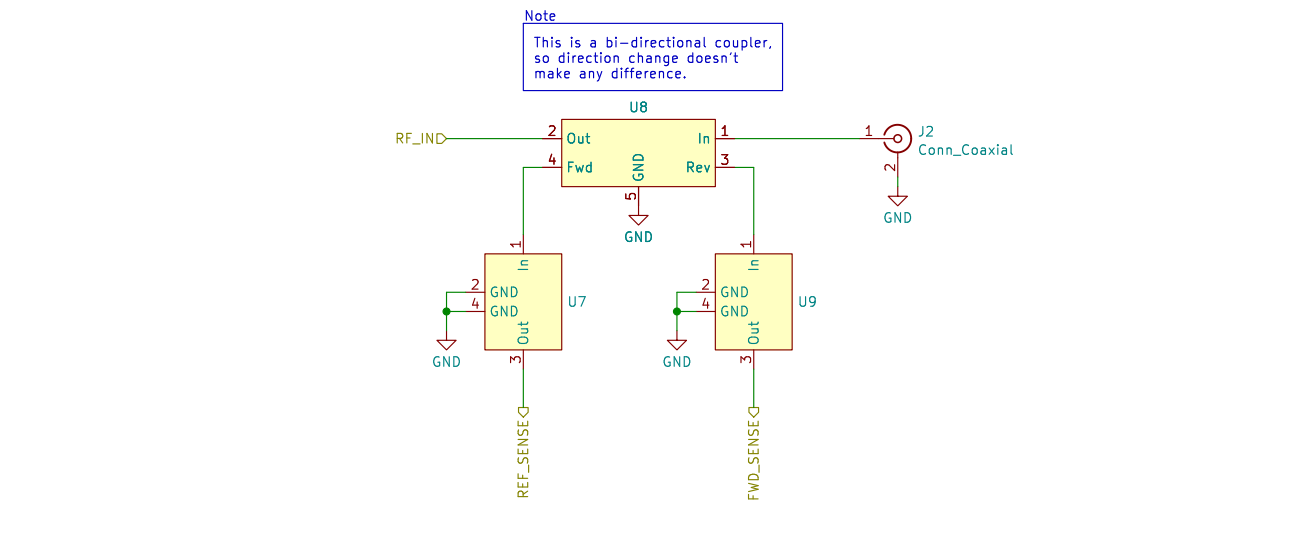
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Exciter



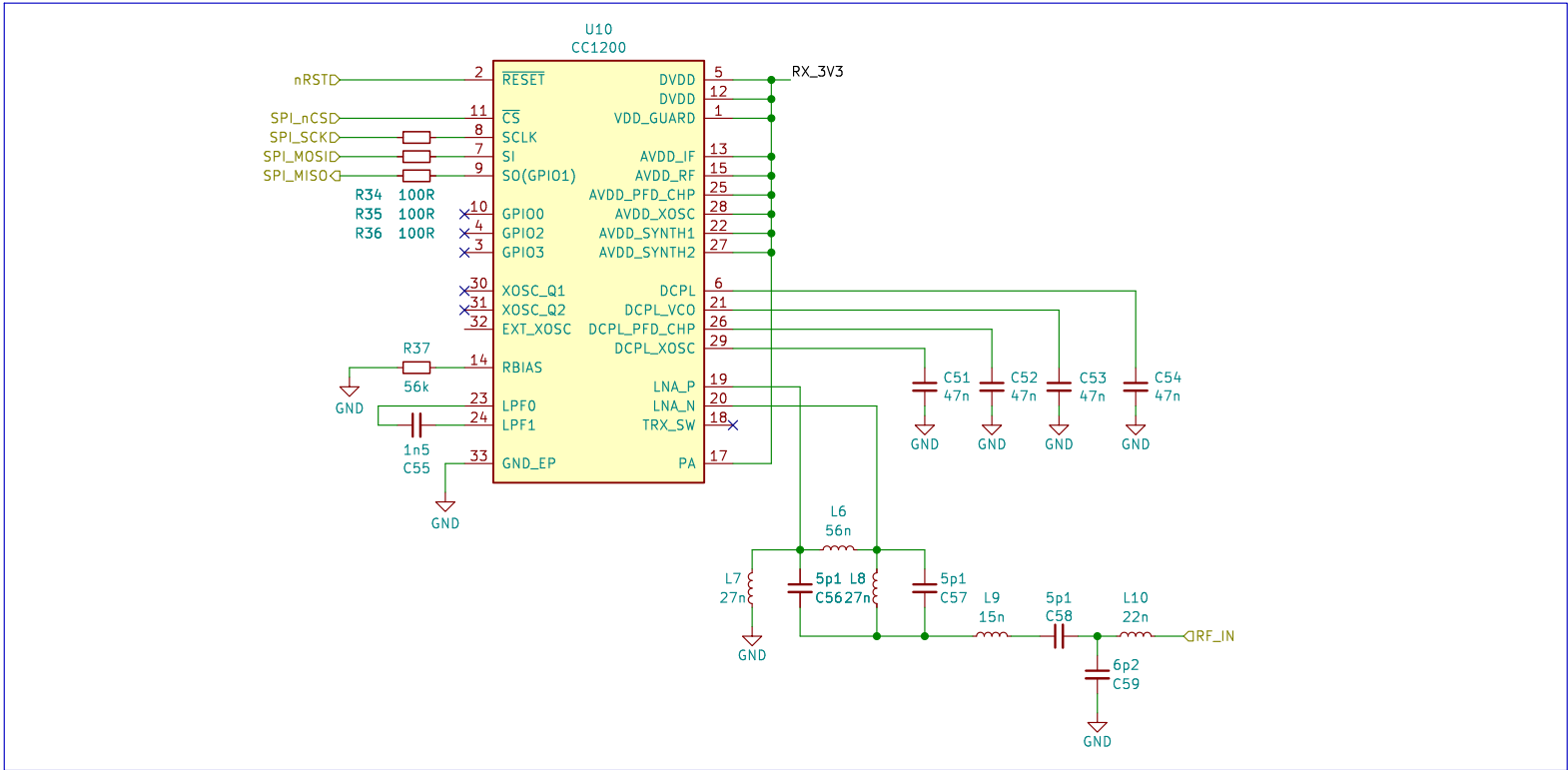
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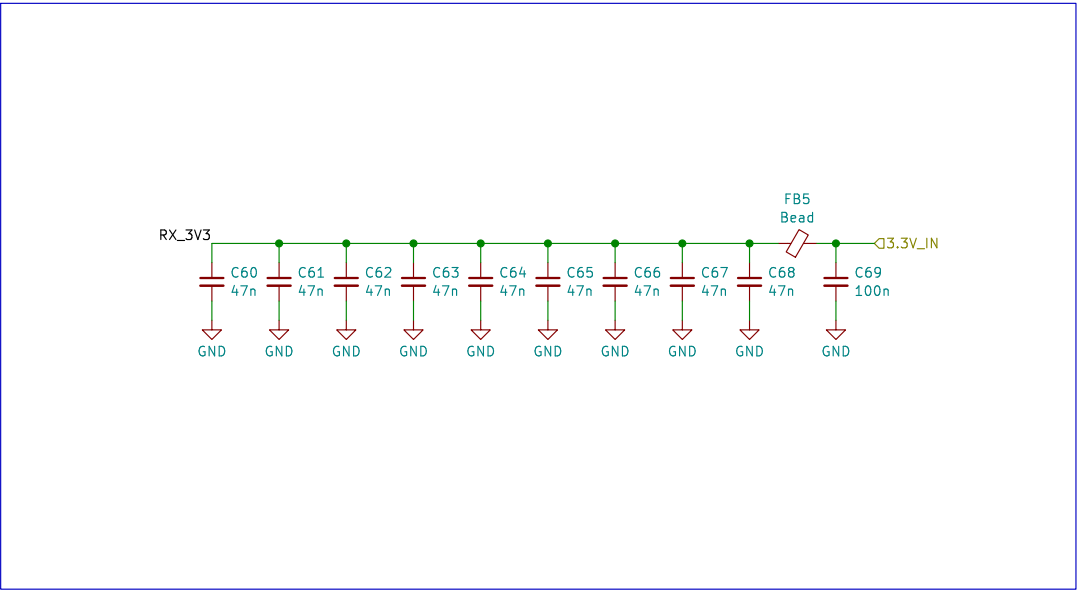


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Receiver



Decoupling



Wojciech Kaczmarek, SP5WWP

M17 Project

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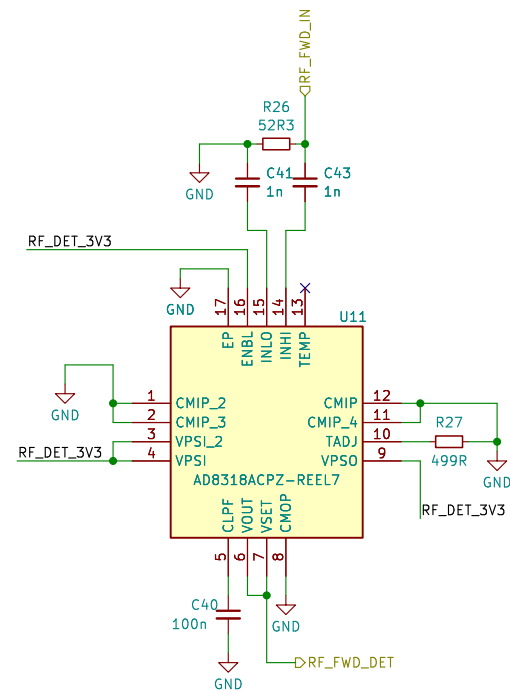
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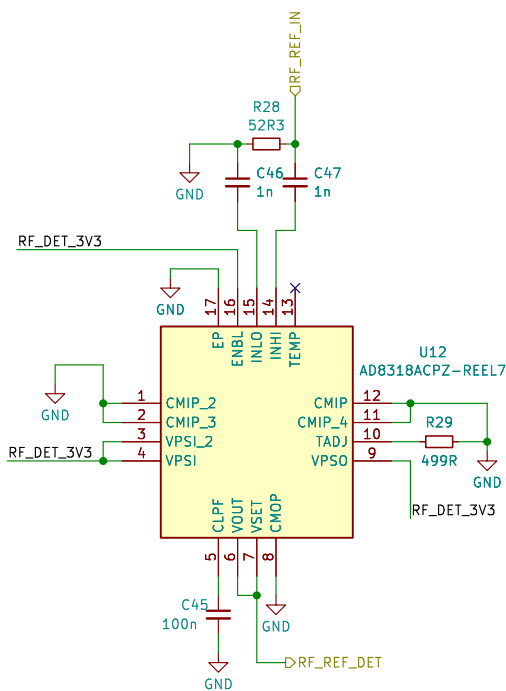
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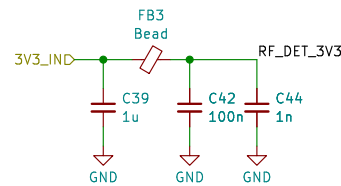
FWD power sense

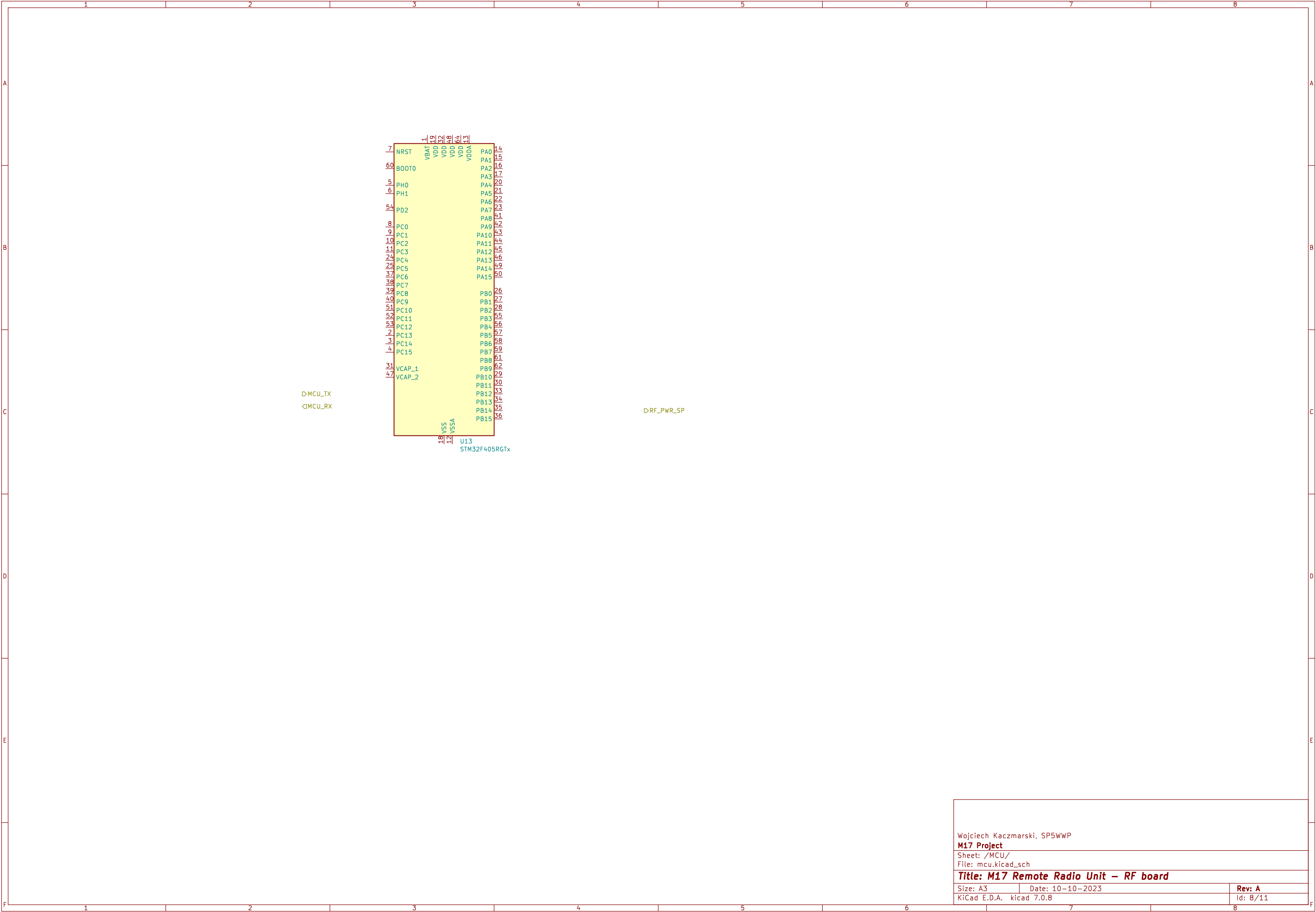


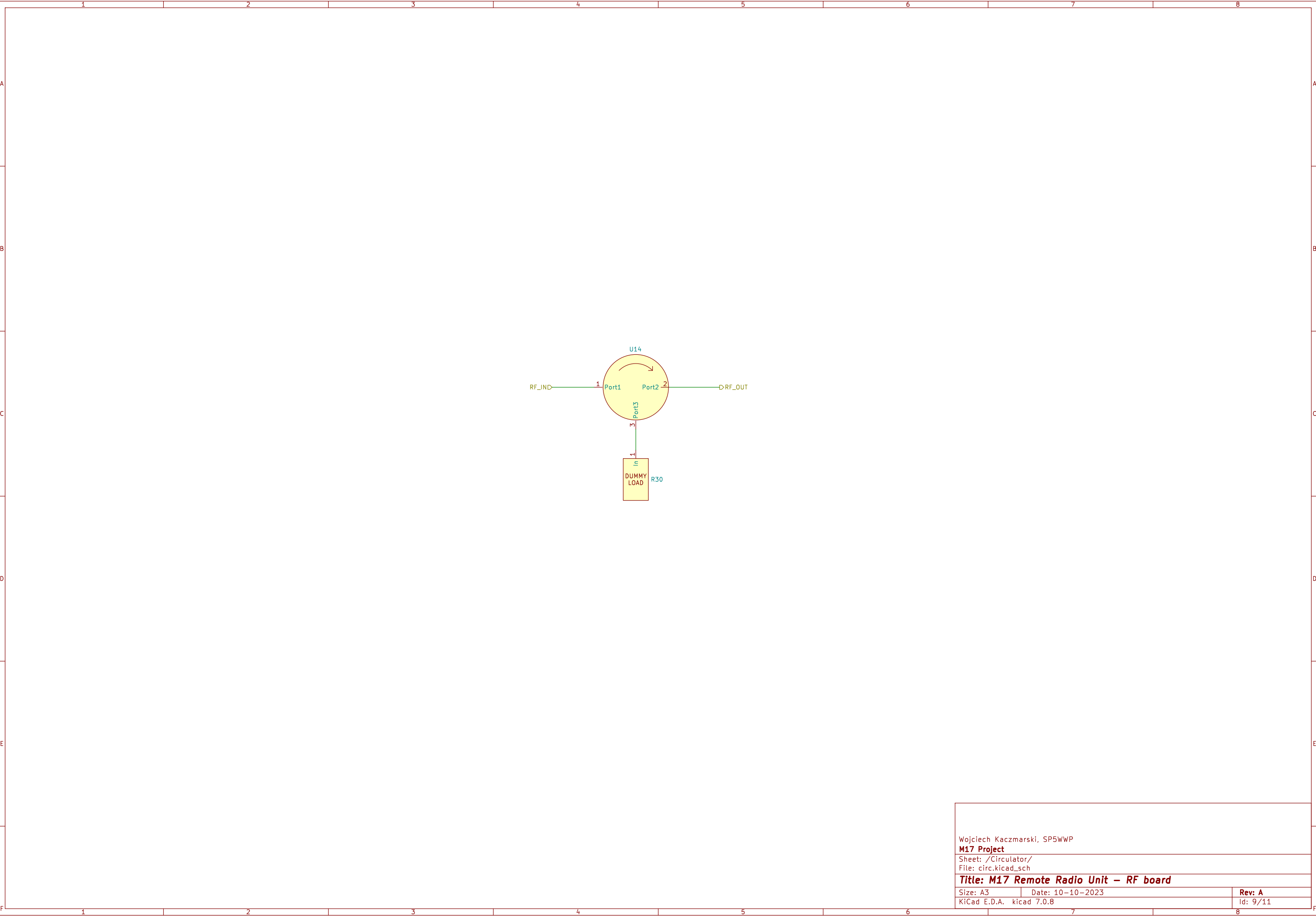
REF power sense



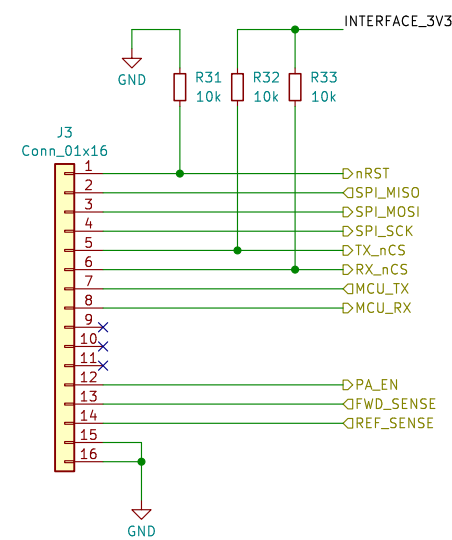
Decoupling



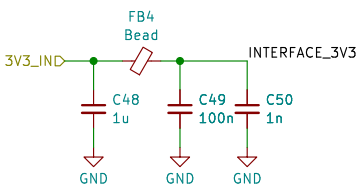


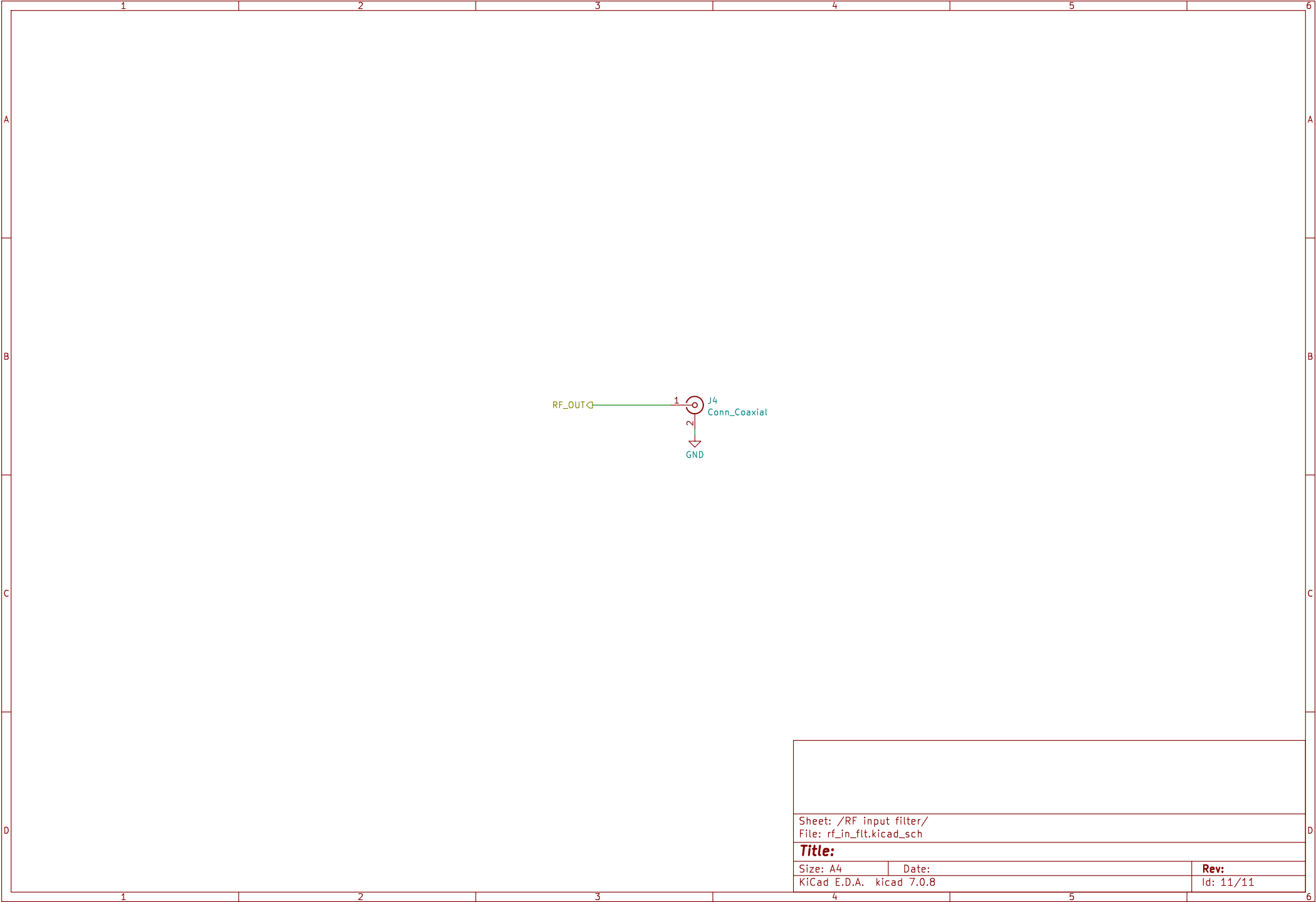


External connector



Decoupling





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