Cape Peninsula University of Technology

F'SATI French South African Institute of Technology

User Manual

CMC-01-00045

Document no.: USM-01-00045

Revision: A

Date: 10 November 2015

	Name	Date	Signed
Author	Charl Jooste	**10 November 2015**	
Approved	Etnard Louw		
Approved	Leon Steenkamp		

Table of Contents

1 Document Control

Revision	Date	Section	Description
A	2015-11-10	All	First Release

2 Revision Control

Product	Part Number	Revisions Covered	Notes
CMC	CMC-01-00045	A	

3 Related Documents

No.	Document Name	Document Reference
ICD-01-00045	Interface Control Document: CMC	Rev A
OPT-01-00045	Options Sheet: CMC	Rev A

4 Nomenclature/Definitions

4.1 Abbreviations

BCD Binary coded decimal

CRC Cyclic redundancy check

FCS Frame check sequence

FPGA Field programmable gate array

TBC To be confirmed

TBD To be determined

PA Power amplifier

RSSI Received signal strength indicator

Rx Receive

SMPS Switched-mode power supply

SSID Secondary station identifier

Tx Transmit

5 Introduction

This document describes the operation, handling and storage of the transceiver. The transceiver is an integrated UHF-transmitter, VHF-receiver supporting both 9600 bps GMSK and 1200 bps AFSK. The transceiver operates in full-duplex mode with the options listed in Table 4.

6 Overview

An overview of the transceiver is illustrated in Figure 1. The transceiver is a compact VHF/UHF Transceiver designed for CubeSat nanosatellite missions. It is compatible with the CubeSat nanosatellite standard, with a CubeSat Kit PC/104 form factor. The transceiver implements both 9600 bps GMSK and 1200 bps AFSK and operates in full-duplex mode with the options listed in Table 4.

The communication protocol implemented is AX.25 using unnumbered information (UI) packets. The transceiver also implements a transparent mode allowing the OBC to implement their own modulation scheme. CCSDS (1/2 Rate, K=7) encoding is available in transparent mode. All telemetry, commands and data are issued via I^2C. The transceiver operates as a slave on the I^2C bus and does not implement any pull-up resistors. The transmit frequency of the hardware has a range of 430–440 MHz. The frequency of operation is software selectable within the band and is adjustable in 25 kHz steps. The output power is adjustable from 27 to 33 dBm.

The receive frequency of the hardware has a range of 140–150 MHz. The frequency of operation is software selectable within the band and is adjustable in 12.5 kHz steps. The transceiver requires power from regulated 3.3 V and 5 V rails.

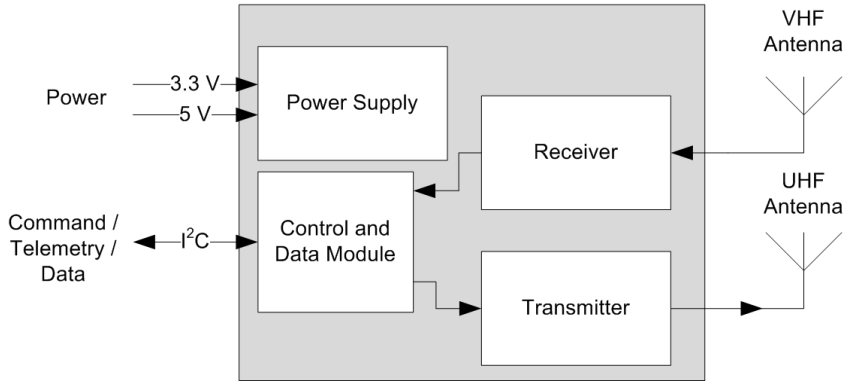

Figure 1: System block diagram

7 Absolute maximum ratings

Parameter	Notes	Value	Unit
Supply Voltage(s)	Regulated 5.0 V from bus	5.5	V
	Regulated 3.3 V from bus	4	V
Operating temperature		–25 to +61	°C
Storage Temperature		–40 to +85	°C

8 Electrical characteristics

Parameter	Notes	Min	Typ	Max	Unit
Power					
Voltage(s)	From a regulated 3.3 V bus	3.2	3.3	3.5	V
	From a regulated 5 V bus	4.7	5	5.5	V
Receiver only					
Current	From 3.3 V bus	-	64	-	mA
	From 5 V bus	-	<100	-	uA
Transmit only					
Current (from 5 V bus)	0.5 W (27 dBm) RF out	-	563	-	mA
	1 W (30 dBm) RF out	-	812	-	mA
	2 W (33 dBm) RF out	-	1202	-	A
DC Power					
Idle power	Receiver ON, transmitter OFF	-	211	-	mW
Transmit 0.5 W RF	Receiver ON, transmitter ON	-	3.0	-	W
Transmit 1 W RF	Receiver ON, transmitter ON	-	4.3	-	W
Transmit 2 W RF	Receiver ON, transmitter ON	-	6.2	-	W
RF characteristics					
Transmitter					
Frequency range		430	-	440	MHz
Output power		27	-	33	dBm
Spurious responses	10 MHz reference oscillator. 25 kHz comparison frequency.	-	<-65	-	dBc
Harmonic outputs		-	<-40	-	dBc
Frequency stability		-	±2.7	-	ppm
Frequency deviation		-	3	-	kHz
Channel spacing		-	25	-	kHz
Receiver					
Frequency range		140	-	150	MHz
Sensitivity	For 12 dB SINAD	-116	-117	-117	dBm
Dynamic range		-117	-	-70	dBm

Noise figure		-	<1.5	-	dB
Frequency stability		-	±2.7	-	ppm
Channel spacing		-	12.5	-	kHz
I^2C					
SCL frequency		50	400	500	kHz
Node address		-	0x25	-	hex
Address scheme		-	7	-	bit

9 Mechanical characteristics

Parameter	Notes	Min	Typ	Max	Unit
Physical					
Dimensions	See diagrams				
Weight		--	<100	--	g
Output ports					
RF connectors	Rx = SMA, Tx = SMA				

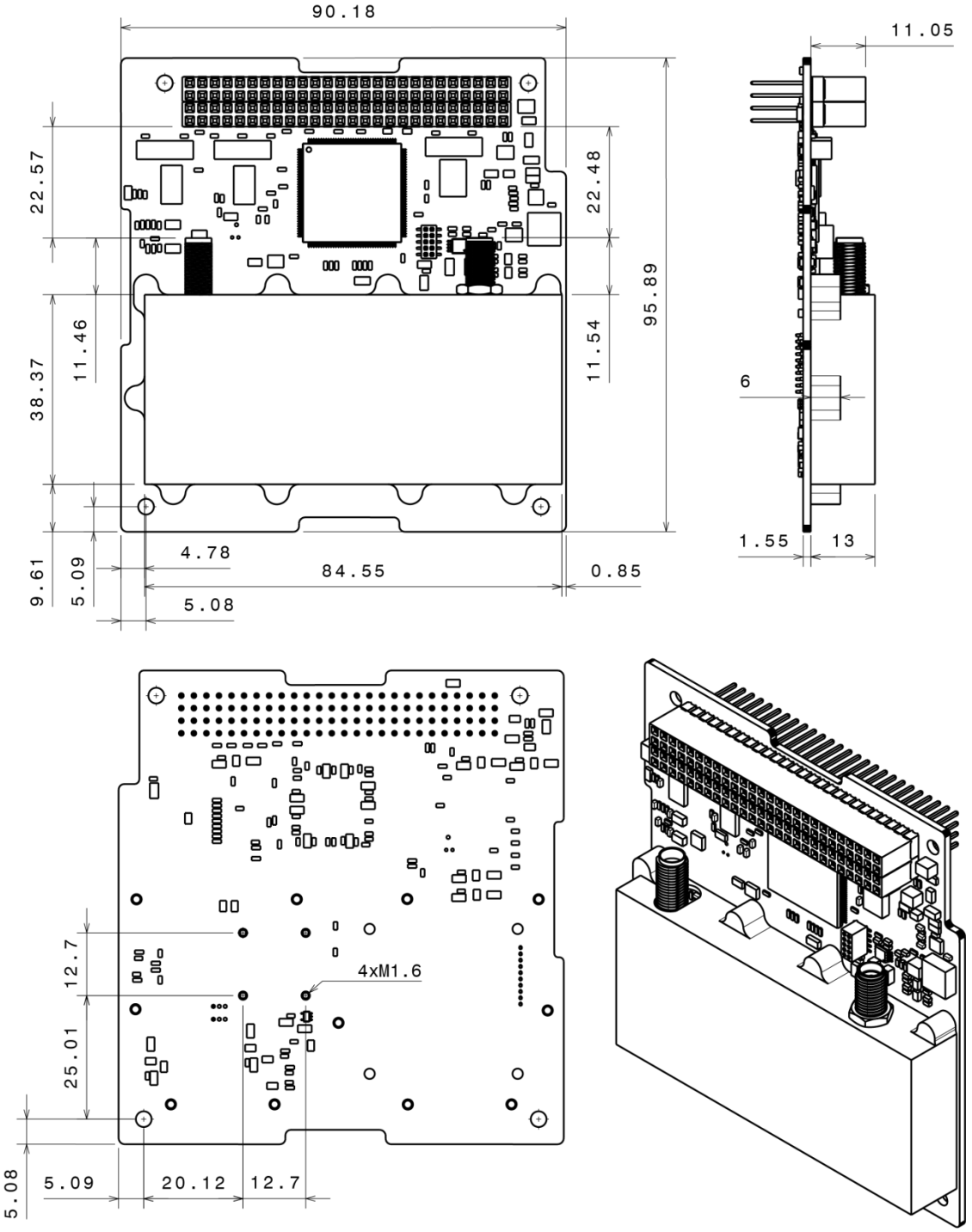

Figure 2: Mechanical diagrams (in mm)

10 Handling and storage

Specific guidelines must be adhered to when handling, transporting and storing the transceiver. Failure to follow these guidelines may result in damage to the unit or degradation in performance.

10.1 Power amplifier protection

Caution must be applied to ensure that an appropriate 50 Ω RF load (at least 5 W rating) is presented to the RF output of the transceiver. Failure to do so could result in permanent damage to the power amplifier unit.

A heat sink must be attached to the underside of the power amplifier to avoid damage at high RF transmit powers.

10.2 ESD protection

The transceiver incorporates static sensitive devices and care should be taken when handling the module. Under no circumstances should the transceiver be handled without appropriate electrostatic protection. The transceiver should only be handled in a static dissipative environment.

10.3 General handling

The transceiver has been designed to withstand satellite flight conditions but care must still be taken when handling the hardware.

- Do not drop the hardware
- All work must be done in a clean room environment
- Keep all metal objects away from the module to prevent accidental short circuiting
- Gloves should be worn when handing flight hardware
- Anti-static procedures should be followed at all times

10.4 Storage and shipping

The transceiver is shipped in anti-static packaging. When storing the transceiver it should be placed in an anti-static package and preferably stored in a hard protective case.

11 System operation

11.1 System overview

After power up the transceiver is immediately ready to receive and transmit data. All telemetry, commands and data are requested or issued via I^2C. A detailed description of the I^2C registers is provided in Section 12.4. The transceiver includes an I^2C inactivity beacon and if enabled will beacon (transmit) a packet, depending on which mode it is in, after a configurable period of inactivity on the I^2C bus. This is detailed in Section 12.3.5.

11.2 Board telemetry

Board telemetry data is acquired using the sensors illustrated in Figure 3. These are all accessible via the relevant I^2C register. Board telemetry is updated once per second. The following board telemetry is made available:

- 3.3 V current,
- 3.3 V voltage,
- 5 V current,
- 5 V voltage,
- SMPS temperature,
- PA temperature,
- RSSI,
- Forward and reverse transmitter power.

The SMPS and PA temperature sensors are located close to the respective components they monitor, namely the SMPS and PA ICs. Both the SMPS and PA are only active during a transmit, therefore temperature should be monitored during this period.

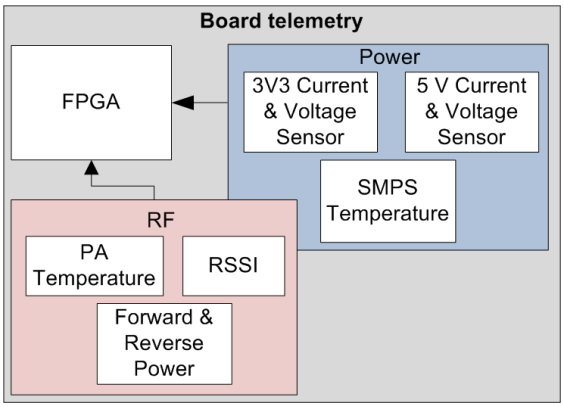

Figure 3: Board telemetry

12 Interfaces

12.1 Mechanical interfaces

12.1.1 Heat sink interface

Provision is made for a heat sink interface on the underside of the PCB. The RF enclosure provides four threaded pillars as depicted on the mechanical diagram which allow for M1.6 screws to fasten a heat sink to the unit. The thread in the pillars is approximately 3.2 mm deep. A simple L–shaped heat sink that attaches to the inside of the satellite structure is suggested. CHO-THERM® may be used between the board and the heat sink for improved thermal conductivity.

12.2 Hardware interfaces

12.2.1 CSK header connections

Figure 4 illustrates the connections that are made available at the CSK header. Broken lines indicate optional connections. The only non-optional connection to the header (excluding power signals) is I^2C. Optional connections that are provided on the header include DTMF signals, a transmit ready (TR) signal, transmit empty (TE), receive ready (RR), FPGA reset and the received baseband audio. The optional connections can be selected at the time of production and should be selected according to application and performance requirements. Should the optional functionality not be required it will not be made available at the header (there will be no physical connection). An explanation of the various connections is detailed later within this document. All signal voltage levels are 3.0 V LVCMOS. The AUDIO RX signal is the analogue demodulated baseband audio from the receiver. Note that should this signal be required that it is AC coupled meaning any DC offset would need to be recreated on the subsystem making use of the audio.

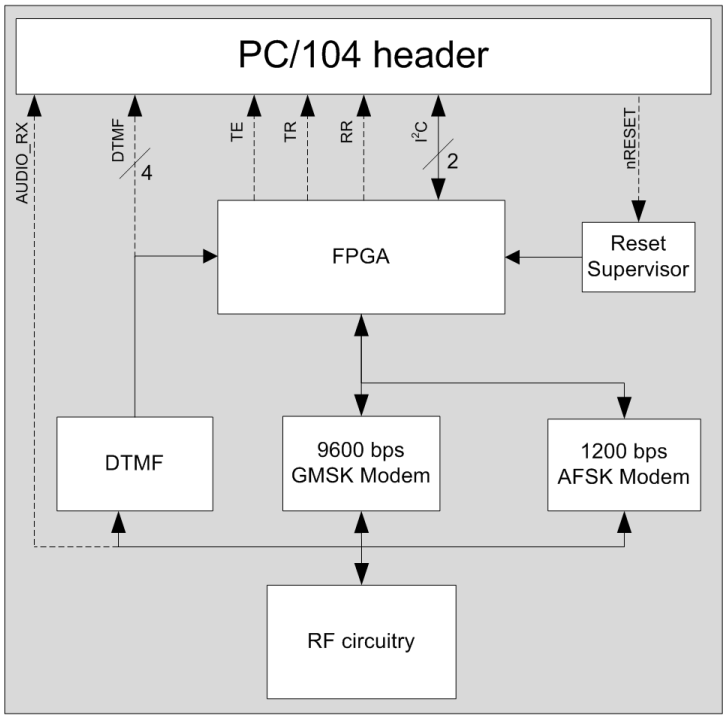

Figure 4: Block diagram of the CSK header connections. Broken lines indicate optional connections

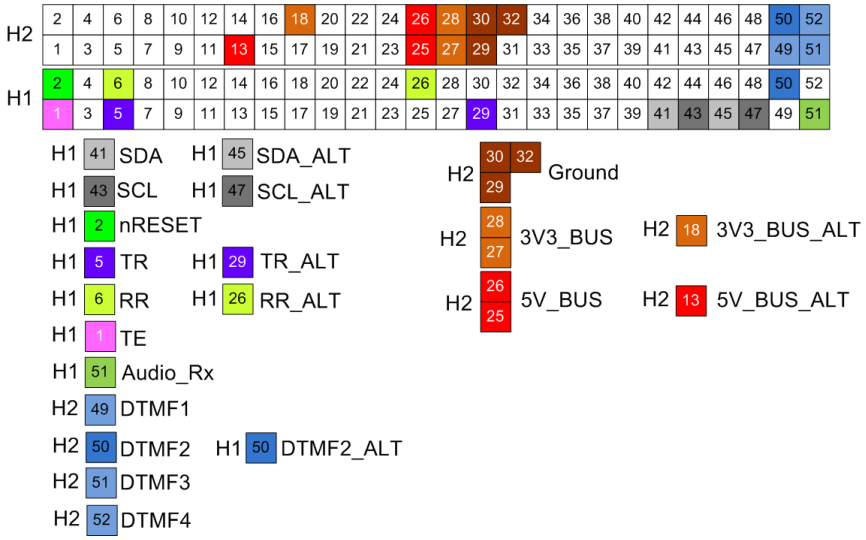

Figure 5: PC/104 header pinouts

Table 1: CSK connector pinouts

Signal name	Primary pin(s)	Alternate pin(s)	I/O type	Description	Optional
SDA	H1.41	H1.45	Bidirectional	I^2C serial data	No
SCL	H1.43	H1.47	Input	I^2C serial clock	No
nRESET	H1.2		Input	FPGA reset (active low)	Yes
TR	H1.5	H1.29	Output	Transmit ready	Yes
RR	H1.6	H1.26	Output	Receive ready	Yes
TE	H1.1		Output	Transmit empty	Yes
AUDIO_RX	H1.51		Output	Receiver baseband audio	Yes
DTMF1	H2.49		Output	Decoded DTMF signal 1	Yes
DTMF2	H2.50	H1.50	Output	Decoded DTMF signal 2	Yes
DTMF3	H2.51		Output	Decoded DTMF signal 3	Yes
DTMF4	H2.52		Output	Decoded DTMF signal 4	Yes
5V_BUS	H2.25, H2.26	H2.13	Power	5 V supply	No
3V3_BUS	H2.27, H2.28	H2.18	Power	3.3 V supply	No
GND	H2.29, H2.30, H2.32		Power	Power ground	No

12.2.2 FPGA reset

A reset signal is provided to the header that will allow an external subsystem such as an OBC to reset the FPGA to a known good state. This is an optional signal. Alternatively cycling the power of the radio or using the soft reset register will also place the FPGA into a known good state.

12.2.3 RF connectors

50 Ω SMA connectors will be used for RF receive and transmit. When connecting to the transceiver a right angle SMA connector should be used. When not transmitting into an antenna, ensure that an appropriate RF load is connected to prevent damaging the transmitter.

12.3 Software interfaces

12.3.1 AX.25

The AX.25 operates in a connectionless mode (Unnumbered Information (UI) frames). If on receipt a packet fails the CRC it will be dropped. The format of the AX.25 packet is illustrated in Table 2. It contains a fixed 16-byte header with a source (SRC), destination (DST) and SSID for each packet. The SRC and DST fields can be selected at time of production. An example of the DST field is "EARTH" and SRC field is "SPACE". The data field can be anything from 1 byte to 256 bytes long. This is followed by the two-byte (16-bit) CRC.

Table 2: AX.25 packet format example. Column data values in hex. Values in brackets denote number of bytes per field

DST (6)	SSID (1)	SRC (6)	SSID (1)	Control (1)	PID (1)	Data (1-256)	FCS (2)
8a, 82, a4, a8, 90, 40	e0	a6, a0, 82, 86, 8a, 40	61	03	f0	...	...

12.3.2 Transparent Mode (Transmit only)

The transceiver can also operate in transparent mode (for transmit only). This is essentially a pass-through of the data directly to the modems, no protocol is implemented as this feature allows an OBC to implement its own. This feature is configurable via the transparent mode I^2C register. Additionally, a CCSDS 1/2 rate convolutional encoder K=7 (171 octal, 133 octal) can be enabled to encode the data. This feature is also configured in the transparent mode I^2C register. Do *not* implement the simple protocol framing method illustrated in Table 3 for transparent mode. The data is transmitted without any manipulation.

12.3.3 I^2C operation

All data, telecommands and telemetry are communicated via I^2C. The default I^2C address is 0x25, but can be configured according to user specifications at time of production. Issuing a telecommand (writing data) has the following procedure. The first byte written to the I^2C points to the address of the register, and the following bytes write the value to the register. Reading telemetry follows a similar approach, firstly a byte is written to point to the correct register followed by a read transaction to return the value. Consecutive read transactions automatically increment the read pointer, except for a few registers.

12.3.4 Operation

On power-up the transceiver is ready to receive and transmit data. It will boot up with the default settings for the modem, RF power setting, etc. As soon as data is available in the transmit buffer it is

sent. Received data is also buffered to be retrieved over I^{2}C. The transceiver is optimally tuned for a 2 MHz band around the selected centre frequency (best receiver sensitivity and transmit power).

12.3.4.1 Transmit in AX.25 mode

Data to be transmitted is sent via an I^{2}C command. The format of the I^{2}C instruction will include the pointer to the data register followed by the data itself. The data must also follow a particular format. A simple protocol is implemented (Table 3) consisting of a two-byte preamble with the byte sequence 0x1A, 0xCF, followed by a single byte containing the length of the data, followed by the data itself and finally a checksum byte. The checksum is a summation of the values of the data bytes ignoring overflow. The length byte can indicate a data field length up to 256 bytes. In order to do this a value of 0 in the length field represents a data field length of 1, and 255 a data field length of 256 bytes respectively.

Table 3: Simple protocol for transmit data. Values in brackets indicate number of bytes

Preamble (2)		Length (1)	Data (1-256)	Checksum (1)
0x1A	0xCF	0x..	{ 0x..; ... ; 0x.. }	0x..

All of this information (preamble, length, data and checksum) is buffered in the transmit buffer. The size of the transmit buffer has been set to 4 kB (4096 bytes). Before writing data to the radio, a transmit buffer check should be performed to check the status of the buffer to see whether there is space for the data. A buffer status telemetry channel is provided to give an indication of the number of free byte slots available in the buffer. Data can be added to the buffer as long as there is space and should preferably be done as complete packets. This means that a number of smaller packets may be written to the buffer. Writes to the buffer when it is full are ignored. As the FPGA packages the AX.25 packet, the data in the buffer is searched sequentially for the preamble after which the number of bytes stipulated in the length field are packaged as AX.25 data. AX.25 data only includes bytes in the data field of the simple protocol. Data will only be packaged as AX.25 data if the simple protocol checksum passes.

A transmit ready (TR) flag is provided to the PC/104 header as a hard signal as well as via an I^{2}C telemetry channel as a soft signal. The hard TR signal should provide a performance advantage as opposed to polling the I^{2}C telemetry channel since it can be used to interrupt an OBC. The TR flag will become active once the number of bytes in the buffer drops below a predefined threshold indicating more data can be added to the buffer. The threshold trigger for the TR flag has been configured to 260 bytes. A transmit empty (TE) flag is also provided to the PC/104 header to indicate when the transmit buffer is empty. The TE signal is logic high when the transmit buffer is empty.

12.3.4.2 Transmit in transparent mode

In transparent mode the simple protocol mentioned above must not be implemented. Data is transmitted as soon as it is buffered. Sync bytes are transmitted while the RF circuitry is being powered or while there is no data in the buffer. If the transmit buffer is not continuously supplied with data the transmitter will automatically turn off after one second.

12.3.4.3 Sync bytes

Each individual AX.25 packet or the first packet of a sequence of AX.25 packets are preceded by a period of transmitting sync bytes. The minimum number of sync bytes preceding a transmission is configurable in a telecommand register. The hex value of the sync byte is 0x55. The purpose of the sync period is to provide the ground (receive) segment an opportunity to perform clock recovery from the signal and synchronise with the transmitter. A similar procedure should be observed when sending telecommands from the ground. Each AX.25 packet also includes a configurable number of AX.25 flags. The value of the AX.25 flag is 0x7E. If there are a number of AX.25 packets buffered in order to be transmitted then only the first packet will be preceded by sync bytes. Each AX.25 packet is however preceded by the configured number of AX.25 flags and terminated with a single flag. Sync bytes are transmitted while there is no data in the transmit buffer and the PTT is still keyed. Once the last packet has been sent and there is no more data in the buffer then PTT will be released.

12.3.4.4 Receive

On receiving telecommands from the ground, if the received AX.25 packet passes the CRC then the AX.25 data field is extracted, the simple protocol header and tail added and then buffered in the receive buffer. Each AX.25 packet must be preceded by at least one flag and terminated with at least one flag. Single flag sharing between packets is not supported. The size of the receive buffer is 4 kB (4096 bytes). As soon as data is available, the RR flag will become active, indicating data is ready to be retrieved. The RR flag is made available as an optional hard signal to the PC/104 header as well as a telemetry channel accessible over I^2C. The hard RR signal should provide a performance advantage as opposed to polling the I^2C telemetry channel since it can be used to interrupt an OBC. An additional I^2C telemetry channel must then be read to indicate how many bytes should be retrieved from the receive buffer. A value of zero for this telemetry channel indicates there is no data available. Any reads from the receive buffer when there is no data available will return a value of 0xff.

12.3.4.5 Full-duplex operation

The radio operates in full-duplex mode with the available configurable modes listed in Table 4. These modes are selectable as an I^2C command. If a reset occurs, then the default mode will be selected. A default mode can be requested at time of production.

Table 4: List of configurable modulation schemes and data rates for downlink/uplink

Configuration mode	Downlink / Uplink	Modulation scheme	Data rate (bps)
1 (default)	Downlink	GMSK	9600
	Uplink	AFSK	1200
2	Downlink	AFSK	1200
	Uplink	GMSK	9600
3	Downlink	GMSK	9600
	Uplink	GMSK	9600

12.3.5 Inactivity beacon

After a period of inactivity on the I^2C bus, configurable between 1 and 7 minutes, a Watchdog timer will overflow resulting in the transmission of a beacon message. The format of the data transmitted depends on the current state of the transmit register. If the transceiver is in AX.25 mode then the data will be formatted as an AX.25 packet. If transparent mode is selected then the raw data will get transmitted, possibly with encoding if that is selected. Another timer can be configured to set the period of delay between consecutive beacons, configurable between 10 and 127 seconds. The beacon message consists of local subsystem telemetry and a configurable 128 volatile bytes for user data. Any I^2C bus activity will reset the Watchdog and beacon operation. The beacon is enabled by default at time of production. It can be enabled/disabled through an I^2C command, however if a reset occurs then the default setting will return. The beacon does not perform any battery voltage measurements to determine whether it should stop beaconing.

The format of the transmitted beacon is presented in Table 5. A detailed description of the beacon I^2C registers can be found in Section 12.4. Registers are available to write, clear and enable the beacon, as well as to configure the timeout period.

Table 5: Inactivity beacon telemetry format

Telemetry	Bytes
Rx packet counter	2
RSSI	2
SMPS temperature	1
PA temperature	1
3V3 Current	2
3V3 Voltage	2
5 V Current	2
5 V Voltage	2
Custom message	128

12.3.6 DTMF backdoor

A DTMF backdoor has been implemented as a means to provide low level commands to the PC/104 connector via the transceiver in the event that ordinary communications are not responding or as a simple, direct command. Typical applications could allow an OBC to reset a subsystem.

The output of the DTMF receiver is provided directly to the PC/104 connector allowing another subsystem, such as an OBC, to interpret the low level decoded signals and perform a function. The current output of the DTMF receiver is also mimicked in a register on the FPGA that is accessible over I^2C. The decoded signals output by the DTMF receiver for a given tone are represented in Table 6.

Take note that the DTMF receiver will latch the digital representation of the last tone pair received and only until a new tone arrives will the latched output change. Since the outputs remain fixed (latched), two same tones must not be sent consecutively .i.e. if two 7's are sent consecutively the

outputs from the DTMF receiver will not change as the digital representation of the tone is the same.

Table 6: Tone decoding

Digit	DTMF4	DTMF3	DTMF2	DTMF1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

12.3.7 Forward and reverse power

Included in the I^2C telemetry is the inclusion of forward and reverse power registers. These registers allow for the calculation of the forward and reverse RF transmit power as well as return loss. This telemetry will provide an indication of the match between the transmitter and the antenna.

12.4 I²C registers

Address	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	r/w	Register group
00 h	-	-	-	-	-	-	CONF1	CONF0	r/w	Modem config.
01 h	D7	D6	D5	D4	D3	D2	D1	D0	r/w	AX.25 TxDelay
02 h	D7	D6	D5	D4	D3	D2	D1	D0	r/w	Sync bytes
03 h	D7	D6	D5	D4	D3	D2	D1	D0	w	Tx Data
04 h	-	-	-	-	-	-	BCNCLR	BCNEN	r/w	Beacon control
05 h	D7	D6	D5	D4	D3	D2	D1	D0	w	Beacon data
06 h	-	-	-	-	-	-	PWR1	PWR0	r/w	PA power
07 h	-	-	-	-	-	-	D9	D8	r/w	Rx frequency offset (UB)
08 h	D7	D6	D5	D4	D3	D2	D1	D0	r/w	Rx frequency offset (LB)
09 h	-	-	-	-	-	-	-	D8	r/w	Tx frequency offset (UB)
0A h	D7	D6	D5	D4	D3	D2	D1	D0	r/w	Tx frequency offset (LB)
0B h	-	-	-	-	-	D2	D1	D0	r/w	I²C timeout
0C h		D6	D5	D4	D3	D2	D1	D0	r/w	Recurring timeout
0D h	-	-	-	-	-	DB	LED1	LED0	r/w	Debug
0E h	-	-	-	-	-	-	-	nRST	w	Reset
0F h	-	-	-	-	-	-	-	-	-	Reserved
10 h	-	-	-	-	CONV	SCRAMRX	SCRAMTX	TRANS	r/w	Transparent
11 h	-	-	-	D12	D11	D10	D9	D8	r/w	Almost Empty Threshold UB
12 h	D7	D6	D5	D4	D3	D2	D1	D0	r/w	Almost Empty Threshold LB
19 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Firmware version
1A h	-	-	-	-	-	-	RR	TR	r	Ready signals
1B h	D15	D14	D13	D12	D11	D10	D9	D8	r	Rx buffer count (UB)
1C h	D7	D6	D5	D4	D3	D2	D1	D0	r	Rx buffer count (LB)
1D h	D7	D6	D5	D4	D3	D2	D1	D0	r	Rx data
1E h	D15	D14	D13	D12	D11	D10	D9	D8	r	Tx buffer free slots (UB)
1F h	D7	D6	D5	D4	D3	D2	D1	D0	r	Tx buffer free slots (LB)
20 h	-	-	-	-	-	-	-	-	-	Reserved
21 h	D15	D14	D13	D12	D11	D10	D9	D8	r	Rx CRC fail counter (UB)
22 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Rx CRC fail counter (LB)
23 h	D15	D14	D13	D12	D11	D10	D9	D8	r	Rx packet counter (UB)
24 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Rx packet counter (LB)
25 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Rx fail full counter

26 h	D15	D14	D13	D12	D11	D10	D9	D8	r	Tx buffer overruns (UB)
27 h	D7	D6	D5	D4	D3	D2	D1	D0	r	Tx buffer overruns (LB)
28 h	-	-	-	-	-	-	TXL	RXL	r	Frequency lock
29 h	CNT4	CNT3	CNT2	CNT1	DTMF4	DTMF3	DTMF2	DTMF1	r	DTMF
2A h	-	-	-	-	D11	D10	D9	D8	r	RSSI (UB)
2B h	D7	D6	D5	D4	D3	D2	D1	D0	r	RSSI (LB)
2C h	T7	T6	T5	T4	T3	T2	T1	T0	r	SMPS temperature
2D h	T7	T6	T5	T4	T3	T2	T1	T0	r	PA temperature
2E h	D15	D14	D13	D12	D11	D10	D9	D8	r	3.3 V Current (UB)
2F h	D7	D6	D5	D4	D3	D2	D1	D0	r	3.3 V Current (LB)
30 h	-	-	-	D12	D11	D10	D9	D8	r	3.3 V Voltage (UB)
31 h	D7	D6	D5	D4	D3	D2	D1	D0	r	3.3 V Voltage (LB)
32 h	D15	D14	D13	D12	D11	D10	D9	D8	r	5 V Current (UB)
33 h	D7	D6	D5	D4	D3	D2	D1	D0	r	5 V Current (LB)
34h	-	-	-	D12	D11	D10	D9	D8	r	5 V Voltage (UB)
35 h	D7	D6	D5	D4	D3	D2	D1	D0	r	5 V Voltage (LB)

12.4.1 Register 0x00: Modem configuration register

Configure the uplink and downlink modulation scheme. Default is 1.

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	CONF1	CONF0

CONF1	CONF0	
0	1	9600 bps GMSK downlink, 1200 bps AFSK uplink
1	0	1200 bps AFSK downlink, 9600 bps GMSK uplink
1	1	9600 bps GMSK downlink and uplink

12.4.2 Register 0x01: AX.25 TxDelay register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Configure the AX.25 TxDelay value. Range is from 1–255 (Default is 20). Transmits configured number of AX.25 flag bytes (0x7E) ahead of each packet.

12.4.3 Register 0x02: Sync bytes register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Configure the sync byte value. Range is from 1–255 (Default is 20). Ensures at least configured number of sync bytes (0x55) are transmitted when first keying the PTT. Refer to Section 12.3.4.3.

12.4.4 Register 0x03: Tx data register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

D7	D6	D5	D4	D3	D2	D1	D0

Data to be transmitted. Writes to this register do not auto-increment the pointer address.

12.4.5 Register 0x04: Beacon control register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	BCNCLR	BCNEN

BCNCLR: Write a '1' to clear the custom beacon data. This register bit is automatically cleared.

BCNEN: Write a '1' to enable the beacon. '0' to disable. Will revert to default after a reset.

12.4.6 Register 0x05: Beacon data register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Write data for the custom beacon portion. Limited to 128 bytes. Writes to this register do not auto-increment the pointer address.

12.4.7 Register 0x06: PA power level register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PWR1	PWR0

Configure the transmit power level. Default is 0 (27 dBm).

PWR1	PWR0	
0	0	27 dBm (0.5 W)
0	1	30 dBm (1 W)
1	0	33 dBm (2 W)

12.4.8 Register 0x07 & 0x08: Rx frequency offset register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	-	-	-	-	-	-	D9	D8
0x08	D7	D6	D5	D4	D3	D2	D1	D0

This register allows the user to select an alternative receive frequency in the band specified. The default frequency is configured to the requested receive frequency and will default to this after power up or after a reset. There are 800 steps allowing for a configurable frequency range from 140 MHz to 150 MHz. Increments are in 12.5 kHz steps. If the register value has not been altered or the FPGA has been reset, reading the offset register value will return 0. Caution should be applied when configuring this register to ensure that it is not incorrectly set resulting in loss of communication.

Use the following formula to calculate the desired offset frequency:

$$offset = \left(\frac{fdesired - 140}{12.5}\right) \times 1000$$

e.g. A desired receive frequency of 145 MHz can be calculated as follows:

$$offset = \left(\frac{145 - 140}{12.5}\right) \times 1000 = 400$$

12.4.9 Register 0x09 & 0x0A: Tx frequency offset register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	-	-	-	-	-	-	-	D8
0x0A	D7	D6	D5	D4	D3	D2	D1	D0

This register allows the user to select an alternative transmit frequency in the band specified. The default frequency is configured to the requested transmit frequency and will default to this after power up or after a reset. There are 400 steps allowing for a configurable frequency range from 430 MHz to 440 MHz. Increments are in 25 kHz steps. If the register value has not been altered or the FPGA has been reset, reading the offset register value will return 0. Caution should be applied when configuring this register to ensure that it is not incorrectly set resulting in loss of communication.

Use the following formula to calculate the desired offset frequency:

$$offset = \left(\frac{fdesired - 430}{25}\right) \times 1000$$

e.g. A desired transmit frequency of 436 MHz can be calculated as follows:

$$offset = \left(\frac{436 - 430}{25}\right) \times 1000 = 240$$

12.4.10 Register 0x0B: Initial I²C timeout register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	D2	D1	D0

Configure the beacon's initial I^2C timeout. Range is from 1–7 (minutes). Default is 3 minutes.

12.4.11 Register 0x0C: Recurring I²C timeout register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	D6	D5	D4	D3	D2	D1	D0

Configure the beacon's recurring I^2C timeout. Range is from 10–127 (seconds). Default is 30 seconds.

12.4.12 Register 0x0D: Debug register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	DB	LED1	LED0

Two LEDs are made available for debugging. Writing a '1' to the register bit activates the corresponding LED. Write a '0' to deactivate. If the DB bit is set to a '1' then the LEDs will display the lock status of the transmit and receive synthesizers. LED0 (Bit 0) will indicate the lock status of the transmit. LED1 (Bit 1) will indicate the lock status of the receive.

12.4.13 Register 0x0E: Reset register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	nRST

Writing a '0' to this register will cause a soft reset of the FPGA logic, placing it into a known good state. This will reset all registers to their default values.

12.4.14 Register 0x10: Transparent mode register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

-	-	-	-	CONV	SCRAMRX	SCRAMTX	TRANS

Writing a '1' to TRANS enables the transparent mode; '0' indicates the transceiver is operating in AX.25 mode. Writing a '1' to CONV enables the convolutional encoder; this can only be used in conjunction with TRANS mode and must be disabled for AX.25 mode. SCRAMRX should always be enabled; always write a '1' to this bit. Write a '1' to SCRAMTX in order to operate in AX.25 mode; otherwise write a '0' for TRANS mode. By default this register has a value of 6 (dec).

12.4.15 Register 0x11 & 0x12: Almost empty threshold

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x11	-	-	-	D12	D11	D10	D9	D8
0x12	D7	D6	D5	D4	D3	D2	D1	D0

This register allows the transmit ready (TR) threshold to be defined. By default it is configured to 260. The TR signal will be active high when the data in the transmit buffer drops below this threshold.

12.4.16 Register 0x19: Firmware version register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

This register is a BCD encoded value. Bits 7:4 represent the Major number, whilst bits 3:0 represent the Minor number. A firmware version of 1.5 has a Major number equal to 1, and a Minor number equal to 5, 0x15 in hex.

12.4.17 Register 0x1A: Ready signals register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	RR	TR

The transmit ready (TR) and receive ready (RR) signals register provides an indication as to when data can be written or read from their respective buffers. These are identical to the TR and RR hard signals made available to the PC/104 header if requested at manufacture, although as a pollable register. The RR signal has its bit set if data is available to be read from the receive buffer. The TR signal has its bit set if data in the transmit buffer drops below a threshold value of 260 bytes of the 4 kB buffer. Reads from this register do not auto-increment the pointer address.

12.4.18 Register 0x1B & 0x1C: Rx buffer count register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1B	D15	D14	D13	D12	D11	D10	D9	D8
0x1C	D7	D6	D5	D4	D3	D2	D1	D0

The receive buffer count register indicates the number of bytes to be read from the receive buffer. This register consists of two bytes, an upper and lower byte. A returned value of 0 indicates that there is no data to be read. Reads from this register do not auto-increment past the register's address boundary. Once the lower byte has been read it will point back to the upper byte's address.

12.4.19 Register 0x1D: Rx data register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

This register returns the data from the received data buffer. Received AX.25 packet data will be encapsulated using the simple protocol method (Table 3). If there is no data available in the receive buffer and a read request is performed then a value of '0xff' will be returned. Reads from this register do not auto-increment the pointer address.

12.4.20 Register 0x1E & 0x1F: Tx buffer free slots register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E	D15	D14	D13	D12	D11	D10	D9	D8
0x1F	D7	D6	D5	D4	D3	D2	D1	D0

This register provides an indication of the number of free slots in the transmit buffer. This register could be referenced before adding additional data to the transmit buffer. Reads from this register do not auto-increment past the register's address boundary. Once the lower byte has been read it will point back to the upper byte's address.

12.4.21 Register 0x21 & 0x22: Rx CRC fail counter register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x21	D15	D14	D13	D12	D11	D10	D9	D8
0x22	D7	D6	D5	D4	D3	D2	D1	D0

This register returns the number of AX.25 packets that have been dropped as a result of the AX.25 frame check sequence (FCS) failing. i.e. There was a mismatch between the 16-bit FCS received and the FCS value calculated. This is a two-byte register consisting of an upper and lower byte. Once this counter reaches its maximum value it will overflow and start counting from zero again.

12.4.22 Register 0x23 & 0x24: Rx packet counter register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x23	D15	D14	D13	D12	D11	D10	D9	D8
0x24	D7	D6	D5	D4	D3	D2	D1	D0

The packet received counter increments by one each time an AX.25 packet is successfully received meaning the FCS calculation checks out. Once this counter reaches its maximum value it will overflow and start counting from zero again.

12.4.23 Register 0x25: Rx fail full counter register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

This register returns the number of AX.25 packets that were dropped as a result of there being insufficient space in the receive buffer. A space check is performed before adding any data to the receive buffer. If this type of failure is occurring then the received packet telemetry needs to be monitored more frequently and the receive buffer data read. Once this counter reaches its maximum value it will overflow and start counting from zero again.

12.4.24 Register 0x26 & 0x27: Tx buffer overrun register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x26	D15	D14	D13	D12	D11	D10	D9	D8
0x27	D7	D6	D5	D4	D3	D2	D1	D0

The transmit buffer overrun register increments by one each time a byte is written to the transmit buffer when there are no free slots available. Any data added to the transmit buffer while it is full

will be dropped. If this type of error is occurring then care must be taken as to when new data is added to the transmit buffer.

12.4.25 Register 0x28: Frequency lock register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	TXL	RXL

This register contains the frequency lock detect signals for both the transmitter (TXL) and receiver (RXL). A value of '1' indicates that a lock was achieved. The transmit lock detect holds its value from the most recent transmit. The TXL value will indicate '0' until a transmit occurs. Data will not be transmitted if a lock is not achieved. The RXL will indicate the current (real-time) lock status of the receiver. At power up the receiver will immediately try to achieve lock and should therefore always return a value of '1'.

12.4.26 Register 0x29: DTMF register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT4	CNT3	CNT2	CNT1	DTMF4	DTMF3	DTMF2	DTMF1

Bits 3:0 indicate a '1' in the relevant bit if the corresponding DTMF tone is received and decoded (see Table 6). These values will be held until another tone is decoded. The bits 7:4 represent a counter; each time a new tone is received the bit field 3:0 is updated and the counter incremented. The counter rolls over when the maximum value is reached. Note that in the event of a power cycle of the transceiver that due to capacitance the DTMF hardware may hold its current latched value. A power cycle of at least a second is recommended.

12.4.27 Register 0x2A & 0x2B: RSSI

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2A	-	-	-	-	D11	D10	D9	D8
0x2B	D7	D6	D5	D4	D3	D2	D1	D0

The RSSI is a 12-bit value returned over two bytes as indicated above. The RSSI telemetry provides an indication of the current received signal strength. This telemetry should typically be captured when a signal is being received from the ground. Table 7 provides an indication of the RF level given the output voltage. The higher the received voltage the better the RF signal being received. Note that this is a noisy telemetry channel unless a carrier signal is present.

Table 7: RSSI output voltage

RF level	Min	Typ	Max	Unit
–118 dBm	-	0.3	0.8	V
–68 dBm	0.7	1.1	1.8	V
–23 dBm	1.2	1.8	2.5	V

$$RSSI = value\ (dec) \times \frac{3}{4096}\ [V]$$

12.4.28 Register 0x2C: SMPS temperature register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

T7	T6	T5	T4	T3	T2	T1	T0

The SMPS temperature register contains the temperature reading of the most recent conversion. T7 is a signed bit. Negative values are returned in two's complement. The data format for the temperature sensor is illustrated in Table 8.

$$Temperature = [T7:T0]\ [°C]$$

Table 8: Temperature sensor data format

Temperature (°C)	Digital output (Binary)	Hex
127	0111 1111	7F
50	0011 0010	32
25	0001 1001	19
0	0000 0000	00
-25	1110 0111	E7

12.4.29 Register 0x2D: PA temperature register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T7	T6	T5	T4	T3	T2	T1	T0

The PA temperature register contains the temperature reading of the most recent conversion. T7 is a signed bit. Negative values are returned in two's complement. The data format for the temperature sensor is illustrated in Table 8.

$$Temperature = [T7:T0]\ [°C]$$

12.4.30 Register 0x2E & 0x2F: 3.3 V Current register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2E	D15	D14	D13	D12	D11	D10	D9	D8
0x2F	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent reading from the 3.3 V current sensor. It returns a signed value with D15 being the signed bit. Negative values are returned in two's complement.

$$Current = value\ (dec)\ \times\ 3 \times 10^{-6}\ [A]$$

12.4.31 Register 0x30 & 0x31: 3.3 V Voltage register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x30	-	-	-	D12	D11	D10	D9	D8
0x31	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent reading of the bus voltage on the 3.3 V supply.

$$Voltage = value\ (dec)\ \times\ 4 \times 10^{-3}\ [V]$$

12.4.32 Register 0x32 & 0x33: 5 V Current register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x32	D15	D14	D13	D12	D11	D10	D9	D8

0x33	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent reading from the 5 V current sensor. It returns a signed value with D15 being the signed bit. Negative values are returned in two's complement.

$$Current = value\ (dec) \times\ 62 \times 10^{-6}\ [A]$$

12.4.33 Register 0x34 & 0x35: 5 V Voltage register

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x34	-	-	-	D12	D11	D10	D9	D8
0x35	D7	D6	D5	D4	D3	D2	D1	D0

This register contains the most recent reading of the bus voltage on the 5 V supply.

$$Voltage = value\ (dec)\ \times\ 4 \times 10^{-3}\ [V]$$

12.4.34 Register 0x36 & 0x37: PA forward power

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x36	-	-	-	-	D11	D10	D9	D8
0x37	D7	D6	D5	D4	D3	D2	D1	D0

This register contains a 12-bit value for the PA forward power. First this value must be converted into voltage using the following equation:

$$x = value\ (dec)\ \times \frac{3}{4096}\ [V]$$

This value needs to be substituted into the equation below in order to acquire the *coupled forward power* value.

$$y = -68838x^6 + 228000x^5 - 308831x^4 + 218934x^3 - 85741x^2 + 17660x - 1511.8\ [dB]$$

The *actual forward power* can be calculated by adding 32.5 dBm to the result of y.

12.4.35 Register 0x38 & 0x39 PA reverse power

Addr.	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x38	-	-	-	-	D11	D10	D9	D8
0x39	D7	D6	D5	D4	D3	D2	D1	D0

This register contains a 12-bit value for the PA reverse power. First this value must be converted into voltage using the following equation:

$$x = value\ (dec)\ \times \frac{3}{4096}\ [V]$$

This value needs to be substituted into the equation below in order to acquire the *coupled reverse power* value.

$$y = -68838x^6 + 228000x^5 - 308831x^4 + 218934x^3 - 85741x^2 + 17660x - 1511.8\ [dB]$$

The *actual reverse power* can be calculated by adding 32.5 dBm to the result of y.

The *return loss* (in dB) can be calculated by subtracting the *actual reverse power* from the *actual forward power*.

13 Operating procedures

13.1 Transmit procedure

The following registers should be checked occasionally to verify the correct parameters are configured. Note that if a reset occurs the register parameters will default to their original settings.

- Modem config (12.4.1)
- AX.25 TxDelay (12.4.2)
- Sync bytes (12.4.3)
- PA power (12.4.7)
- Tx Synth offset (12.4.9)

The procedure to follow when writing data to be transmitted is as follows:

- *Ensure the data is in the correct format:*
  If in AX.25 mode, check that the format of the data sent to the transceiver matches the format illustrated in Table 3. In transparent mode this framing method must not be used.
- *Check if there is space in the transmit buffer:*
  There are a few ways of checking. Check if the TR signal (either hard signal going to the PC/104 header or the TR bit of the *Ready signals* register (12.4.17)) is active OR the *Tx buffer free slots* telemetry channel (12.4.20) can be polled. Neither of these I^2C telemetry channels are auto-incrementing channels meaning an initial I^2C write to the register address is required but subsequent I^2C read requests (according to the byte boundary of the relevant register) may continuously be issued. If the TR signal is active that indicates that there is less than the threshold number of bytes in the transmit buffer.
- *Send the data to the transceiver:*
  The data is sent to the *Tx data register* (12.4.4). In AX.25 mode the data field is extracted, incorporated into the AX.25 protocol and transmitted. In transparent mode the data is transmitted as is except if the convolutional encoder is enabled.

13.2 Receive procedure

The following registers should be checked occasionally to verify the correct parameters are configured. Note that if a reset occurs the register parameters will default to their original settings.

- Modem config (12.4.1)
- Rx Synth offset (12.4.8)
- Synth lock RXL bit (12.4.25)

The receive synthesizer attempts to achieve lock as soon as power is applied to the board and remains locked. If for any reason the receiver loses lock the transceiver will not be able to receive

data. Attempt to reconfigure the Rx synth offset register or follow the reset procedure (13.4) to attempt to rectify the problem.

The procedure to follow when reading received data from the transceiver is as follows:

- *Check if data is available in the receive register:* There are a few ways of checking. Check if the RR signal (either hard signal going to the PC/104 header or the RR bit of the *Ready signals* register (12.4.17)) is active OR the *Rx buffer count* telemetry channel (12.4.18) can be polled. Neither of these I^2C telemetry channels are auto-incrementing channels meaning an initial I^2C write to the register address is required but subsequent I^2C read requests (according to the byte boundary of the relevant register) may continuously be issued. If the RR signal is high it indicates that there is at least one byte in the receive buffer. A value of 0 returned from the Rx buffer count register indicates that there is no data available to be read.
- *Get the number of bytes to read:* Request telemetry from the Rx buffer count channel (12.4.18). This register indicates the number of bytes to be read. A value of 0 returned indicates that there is no data available to be read.
- *Read the data:* Point to the *Rx data* register (12.4.19) and read the required number of bytes. Data is returned in the format illustrated in Table 3. Reading from the register when there is no data available returns 0xFF.

13.3 Configuring the beacon

The procedure to configure the AX.25 inactivity beacon is as follows:

- Configure the initial *I^2C timeout* register (12.4.10).
- Configure the *Recurring I^2C timeout* register (12.4.11).
- Optionally write custom data (max 128 bytes) to the *Beacon data* register (12.4.6).
- Enable the beacon by setting the BCNEN bit of the *Beacon control* register (12.4.5).

In order to clear the custom data portion of the beacon the BCNCLR bit of the Beacon control register (12.4.5) must be set.

13.4 Resetting the FPGA

This reset procedure refers to resetting the FPGA on the transceiver and not a board wide power cycle. Resetting the FPGA will place the logic into a known good state and will revert all registers to default values.

There are several ways to reset the FPGA, including:

- Power cycling the transceiver board (3.3 V and 5 V).
- Pulling the PC/104 nRESET pin low (Table 1), then releasing it.
- Writing a '0' to the nRST bit of *Reset* register (12.4.13).

14 Operating examples

These examples present a finite number of ways to operate the hardware. For alternatives to the operating procedures listed below see Section 13.

14.1 Transmit example

This example uses the 9600 bps modem to transmit three bytes. The soft transmit ready (TR) signal is polled to determine whether more data can be added to the transmit buffer.

- Step 1: Write 0x0001 to point to the Modem config register and configure the downlink to 9600 bps GMSK and the uplink to 1200 bps AFSK.
- Step 2: Write 0x1A to point to the Ready signals register.
- Step 3: Read back one byte. If the TR (bit 0) is equal to one then continue onto the next step otherwise repeat this step.
- Step 4: Write 0x03 to point to the Tx data register.
- Step 5: Write 0x1ACF0201020306. This data is formatted using the simple protocol framing method (not used in transparent mode). Data bytes transmitted are 0x01, 0x02, 0x03.

14.2 Receive example

This example uses the 1200 bps modem to receive data. The soft receive ready (RR) signal is polled to determine whether data is available to be read from the receive buffer.

- Step 1: Write 0x0001 to point to the Modem config register and configure the uplink to 1200 bps AFSK and the downlink to 9600 bps GMSK.
- Step 2: Write 0x1A to point to the Ready signals register.
- Step 3: Read back one byte. If the RR (bit 1) is equal to one then continue onto the next step otherwise repeat this step.
- Step 4: Write 0x1B to point to the Rx buffer count register.
- Step 5: Read back two bytes. This will return the number of bytes to read from the receive register.
- Step 6: Write 0x1D to point to the Rx data register.
- Step 7: Read back the number of bytes returned by the Rx buffer count register. This data will be returned in the simple protocol format.

14.3 Inactivity beacon configuration example

This example configures the timeouts and enables the beacon with data.

- Step 1: Write 0x0B02 to point to the I^2C timeout register and configure it for 2 minutes.
- Step 2: Write 0x0C14 to point to the Recurring timeout register and configure it to 20 seconds.
- Step 3: Write 0x0402 to point to the Beacon control register and clear the beacon contents.
- Step 4: Write 0x05[..] to point to the beacon data register and write data to the register. Max 128 bytes.
- Step 5: Write 0x0401 to point to the beacon control register and enable the beacon.