CS6135 VLSI Physical Design Automation
Homework 1: P&R Tool

Name:賴琮翰

Student ID:112062542

Date:2023/9/27

壹、Comparison Table

Clock Period: 10 Core Utilization: 0.7

	(congestion-driven, timing-driven)					
	(L, off)	**(L, on)**	**(M, off)**	**(M, on)**	**(H, off)**	**(H, on)**
Slack	0.304	0.321	0.402	0.554	0.402	0.553
Total Wire Length (um)	110904.28	103962.63	110082.99	103126.47	110082.99	103126.47

表格解釋：透過以上表格可以觀察到在相同的 congestion-driven effort 下，當開啟 timing-driven placement 時，無論是 Slack 或是 Total Wire Length 兩項數據均優於未開啟此選項，我認為原因是 timing-driven placement 會傾向於將同屬 critical path 上的元件擺放在附近，這使得這些 critical path 的 delay 與 setup time 可以減少，因此固定 clock 周期時 Slack 也就相對增加，另外，Tool 也會盡可能地減少這些元件之間的 Wire Length 以降低 delay。

貳、Different between Congestion driven Placement and Timing-driven Placement

- Timing-driven Placement

  Timing-driven placement 目標為讓 critical path 上的 block 更為靠近，來降低他們之間的 wire length，進而縮短 RC delay 以滿足 setup time。

- Congestion-driven Placement

  Congestion-driven placement 考量到之後在 routing 時 cell 上的 track 數量有限，若有太多的 route 需要經過同一區域，則 track 會不夠用，此時有些 route 會需要繞開這些發生 congestion 的區域，這會導致這些 route 的 delay 增加，若 congestion 過於嚴重更有可能會沒辦法找出 detailed routing。因此，congestion-driven placement 的目標是讓元件擺放位置後，routing 的 congestion 程度降低。

參、Why we insert filler cells?

在這次作業裡，我們添加的 filler cell 應該是屬於 standard filler cell。其不具備有邏輯上的功能，但他仍然會有一般 cell 的 layer，例如 NWell，以及 VDD、GND 等腳位。在 standard cell design 中，當完成 placement and routing 步驟後，通常 layout 還會剩下一些 standard cell 之間的空隙，這是因為考慮到 timing 及 congestion 等因素，把所有 cell 緊密排列是不太現實的。這些空隙可能會導致 layout 無法通過 DRC，比如說 NWell minimum spacing not met，有了 filler cell 就可以將 NWell 連接起來以滿足 design rule，除此之外，filler cell 也可以保證 VDD 和 GND 的連線不中斷。

肆、Best Result

- Clock Period: 6
- Total Area of Chip: 15731.453 (um^2)
- Total Wire Length: 110407.8350 (um)
- Slack: 0.012

- Congestion-driven effort and timing-driven on/off setting: low/on
- Core utilization: 0.65

```
Analysis View: generic_view
Other End Arrival Time          0.000
- Setup                         0.172
+ Phase Shift                   6.000
= Required Time                 5.828
- Arrival Time                  5.816
= Slack Time                    0.012
```

圖一、Timing.rpt Slack 數據

```
============================
Floorplan/Placement Information
============================
Total area of Standard cells: 13732.516 um^2
Total area of Standard cells(Subtracting Physical Cells): 10008.516 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 13732.516 um^2
Total area of Chip: 15731.453 um^2
```

圖二、Summary.rpt Area 數據

```
============================
Wire Length Distribution
============================
Total metal1 wire length: 2326.9900 um
Total metal2 wire length: 28911.1250 um
Total metal3 wire length: 43293.8700 um
Total metal4 wire length: 20206.4700 um
Total metal5 wire length: 8586.0800 um
Total metal6 wire length: 7083.3000 um
Total wire length: 110407.8350 um
```

圖三、Summary.rpt Wire Length 數據

```
VERIFY DRC ..... Sub-Area: {63.720 0.000 126.540 62.640} 2 of 4  Thread : 1
VERIFY DRC ..... Sub-Area: {0.000 62.640 63.720 124.320} 3 of 4  Thread : 1
VERIFY DRC ..... Thread : 3 finished.
VERIFY DRC ..... Sub-Area: {63.720 62.640 126.540 124.320} 4 of 4  Thread : 1
VERIFY DRC ..... Thread : 1 finished.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.2  ELAPSED TIME: 2.00  MEM: 288.1M) ***
```

圖四、Drc.rpt design rule

```
floorPlan -coreMarginsBy die -site FreePDK45_38x28_10R_NP_162NW_34O -r 1.0 0.65 4.0 4.0 4.0 4.0
```

圖五、core utilization

```
setPlaceMode -congEffort low -timingDriven 1
```

圖六、congestion effort 及 time driven option

伍、Final Chip Layout