SDRAM Device Operations

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA_0 ~ BA_1	A_n ~ A_{10}/AP	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode		
A_8	A_7	Type
0	0	Mode Register Set
0	1	Reserved
1	0	Reserved
1	1	Reserved

Write Burst Length	
A_9	Length
0	Burst
1	Single Bit

CAS Latency			
A_6	A_5	A_4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Type	
A_3	Type
0	Sequential
1	Interleave

Burst Length				
A_2	A_1	A_0	BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

*** Full Page Length**
16Mb : x16 (256)
64Mb : x4 (1024), x8 (512), x16 (256), x32 (256)
128Mb : x4 (2048), x8 (1024), x16 (512)
256Mb : x4 (2048), x8 (1024), x16 (512)

Note : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

B. POWER UP SEQUENCE

1. Apply power to VDD and VDDQ simultaneously . And start clock.
2. Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
3. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
4. Issue precharge commands for all banks of the devices.
5. Issue 2 or more auto-refresh commands.
6. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

C. BURST SEQUENCE

1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

D. DEVICE OPERATIONS

ADDRESSES of 16Mb

BANK ADDRESSES (BA)

: In case x 16

This SDRAM is organized as two independent banks of 524,288 words x 16 bits memory arrays. The BA input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank select BA is latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A10/AP)

: In case x 16

The 19 address bits are required to decode the 524,288 word locations are multiplexed into 11 address input pins (A_0 ~ A_{10}/AP). The 11 bit row addresses are latched along with $\overline{RAS}$ and BA during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or write command.

ADDRESSES of 64Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 4,194,304 words x 4 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 8

This SDRAM is organized as four independent banks of 2,097,152 words x 8 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 16

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESSES of 64Mb (Continued)

BANK ADDRESSES (BA0 ~ BA1)

: In case x 32

This SDRAM is organized as four independent banks of 524,288 words x 32 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A11)

: In case x 4

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 8

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 16

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

ADDRESS INPUTS (A0 ~ A10)

: In case x 32

The 19 address bits are required to decode the 524,288 word locations are multiplexed into 11 address input pins (A_0 ~ A_{10}). The 11 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

D. DEVICE OPERATIONS (continued)

ADDRESSES of 128Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 8,388,608 words x 4 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 8

This SDRAM is organized as four independent banks of 4,194,304 words x 8 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 16

This SDRAM is organized as four independent banks of 2,097,152 words x 16 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A11)

: In case x 4

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 11 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 8

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 16

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

ADDRESSES of 256Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 16,777,216 words x 4 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 8

This SDRAM is organized as four independent banks of 8,388,608 words x 8 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 16

This SDRAM is organized as four independent banks of 4,194,304 words x 16 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 4

The 24 address bits are required to decode the 16,777,216 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 11 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 8

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 16

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

D. DEVICE OPERATIONS (continued)

ADDRESSES of 512Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 33,554,432 words x 4 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and pre-charge operations.

: In case x 8

This SDRAM is organized as four independent banks of 16,777,216 words x 8 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and pre-charge operations.

: In case x 16

This SDRAM is organized as four independent banks of 8,388,608 words x 16 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and pre-charge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 4

The 25 address bits are required to decode the 33,554,432 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 12 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 8

The 24 address bits are required to decode the 16,777,216 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 11 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 16

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in a valid state (low or high) for the duration of set-up and hold time around positive edge of the clock in order to function well Q perform and I_{CC} specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time are the same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

D. DEVICE OPERATIONS (continued)

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interruptions of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_n and BA_0 ~ BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on the fields of functions. The burst length field uses A_0 ~ A_2, burst type uses A_3, CAS latency (read latency from column address) use A_4 ~ A_6, vendor specific options or test mode use A_7 ~ A_8, A_{10}/AP ~ A_n and BA_0 ~ BA_1. The write burst length is programmed using A_9. A_7 ~ A_8, A_{10}/AP ~ A_n and BA_0 ~ BA_1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated.

The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high, requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed.

D. DEVICE OPERATIONS (continued)

The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

ALL BANKS PRECHARGE

All banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10}/AP after all banks have satisfied t_{RAS}(min) requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge to all the banks, all banks are in idle state.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10}/AP with valid BA_0 ~ BA_1 of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and $\overline{CAS}$ latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}/AP. If burst read or burst write by asserting high on A_{10}/AP, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

AUTO REFRESH

The storage cells of 64Mb, 128Mb and 256Mb SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle).

D. DEVICE OPERATIONS (continued)

The time required to complete the auto refresh operation is specified by t_{RC}(min). The minimum number of clock cycles required can be calculated by driving t_{RC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The 64Mb and 128Mb SDRAM's auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms. The 256Mb SDRAM's auto refresh cycle can be performed once in 7.8us or a burst of 8192 auto refresh cycles once in 64ms.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing are internally generated to reduce power consumption.

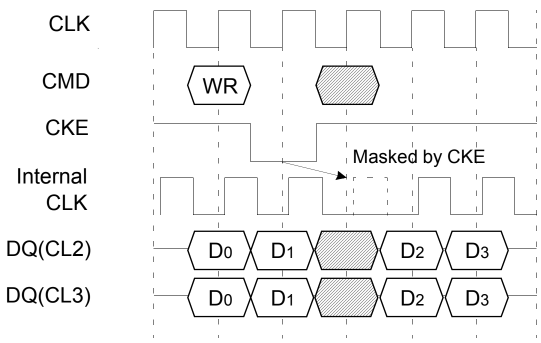
The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including the clock are ignored in order to remain in the self refresh mode.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 8192 auto refresh cycles for 256Mb and burst 4096 auto refresh cycles for 128Mb and 64Mb immediately after exiting in self refresh mode.

E. BASIC FEATURE AND FUNCTION DESCRIPTIONS

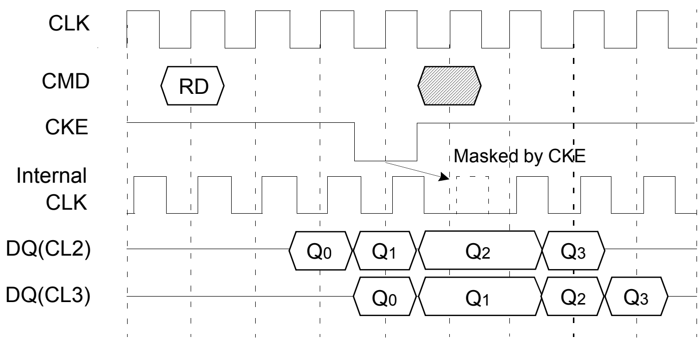
1. CLOCK Suspend

1) Clock Suspended During Write (BL=4)



Not Written

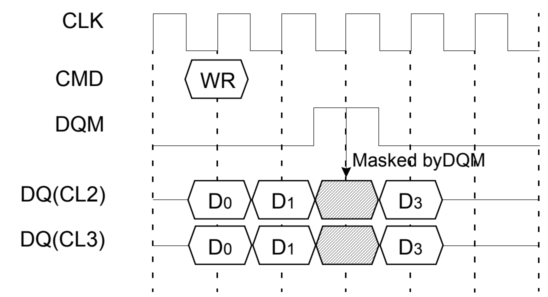
2) Clock Suspended During Read (BL=4)



Suspended Dout

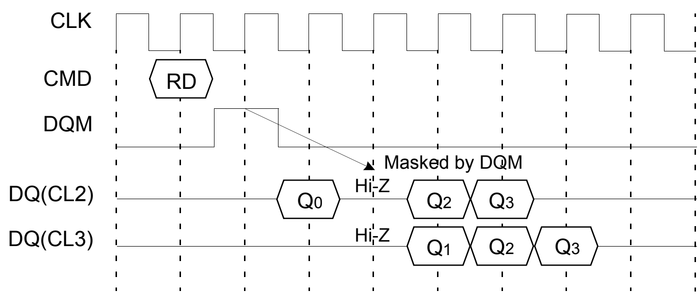
2. DQM Operation

1) Write Mask (BL=4)



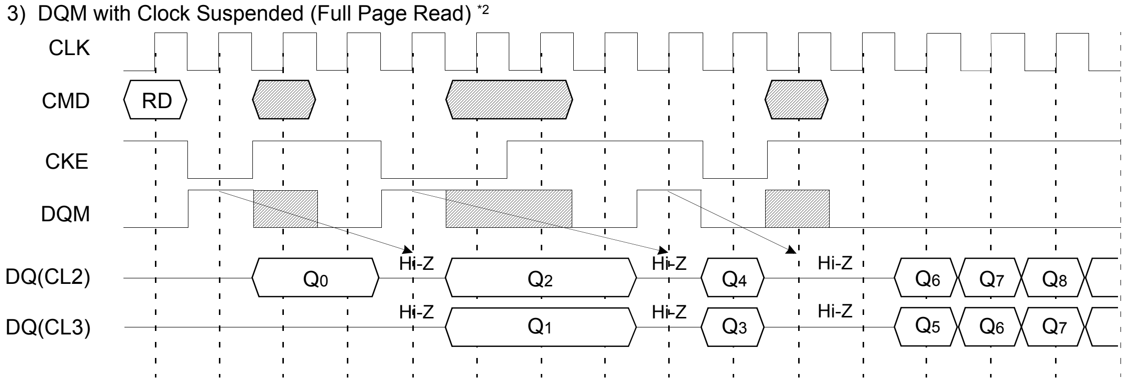
DQM to Data-in Mask = 0

2) Read Mask (BL=4)



DQM to Data-out Mask = 2

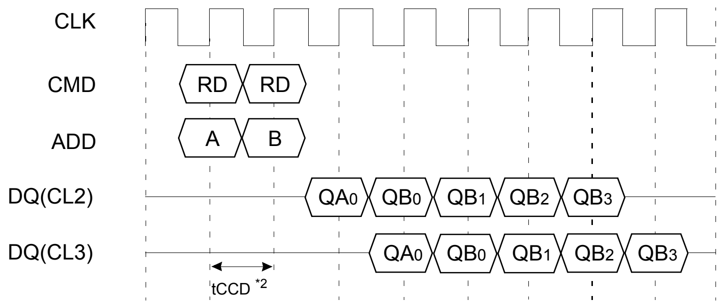
3) DQM with Clock Suspended (Full Page Read) *2



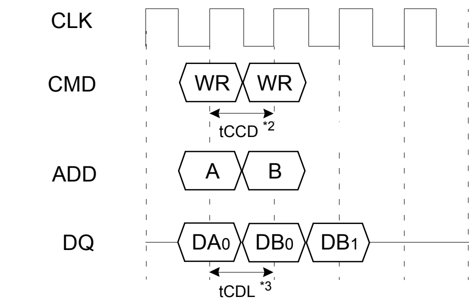
***Note :** 1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

3. $\overline{\text{CAS}}$ Interrupt (I)

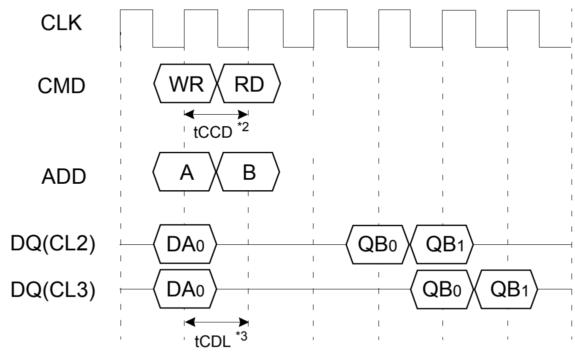
1) Read interrupted by Read (BL=4) *1



2) Write interrupted by Write (BL=2)

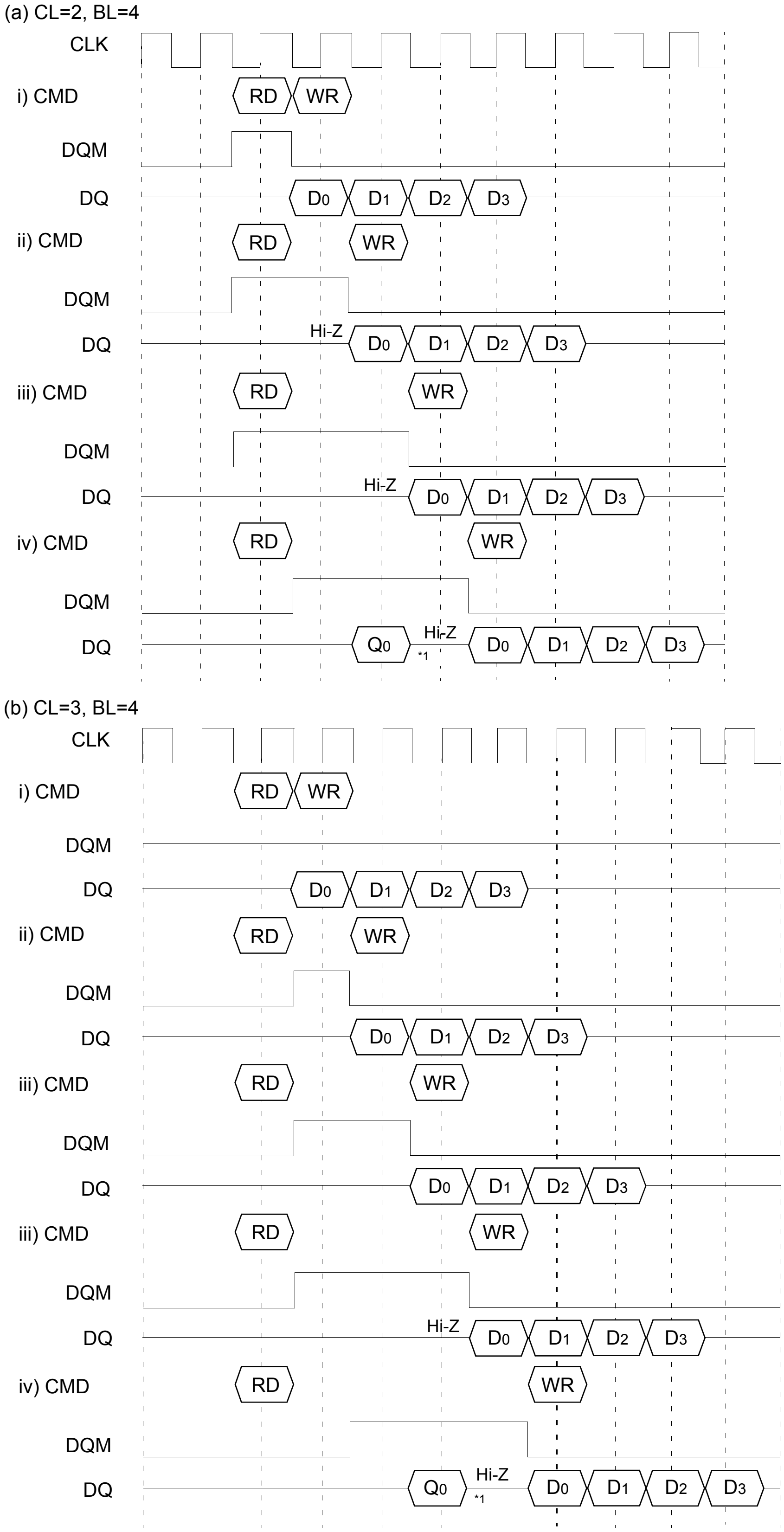


3) Write interrupted by Read (BL=2)



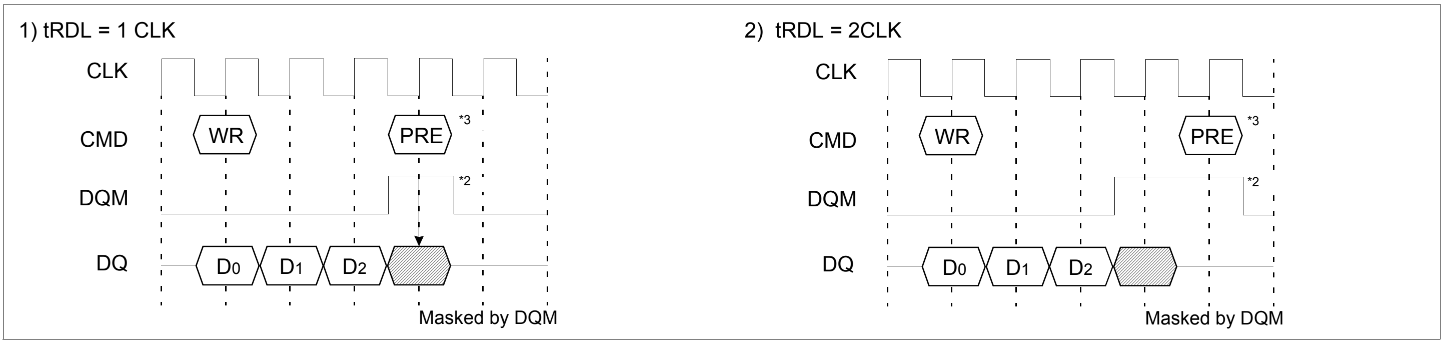
***Note :** 1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
By "$\overline{\text{CAS}}$ Interrupt", to stop burst read/write by $\overline{\text{CAS}}$ access ; read and write.
2. tCCD : $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay. (=1CLK)
3. tCDL : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM



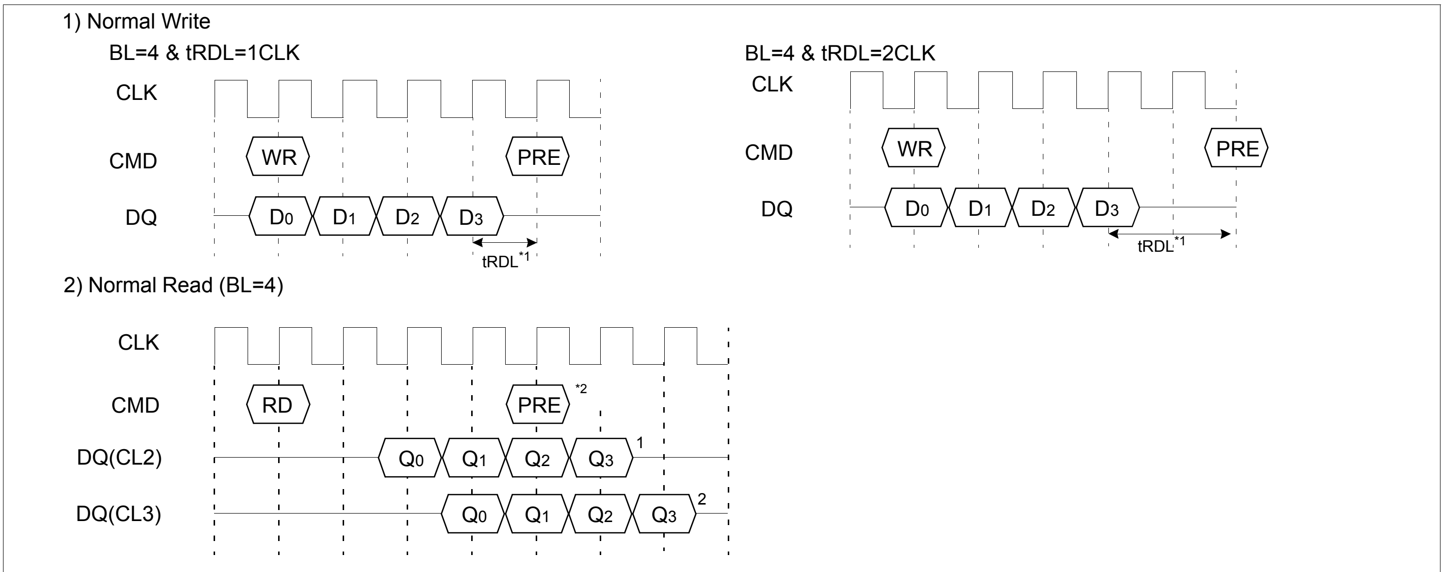
***Note :** 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

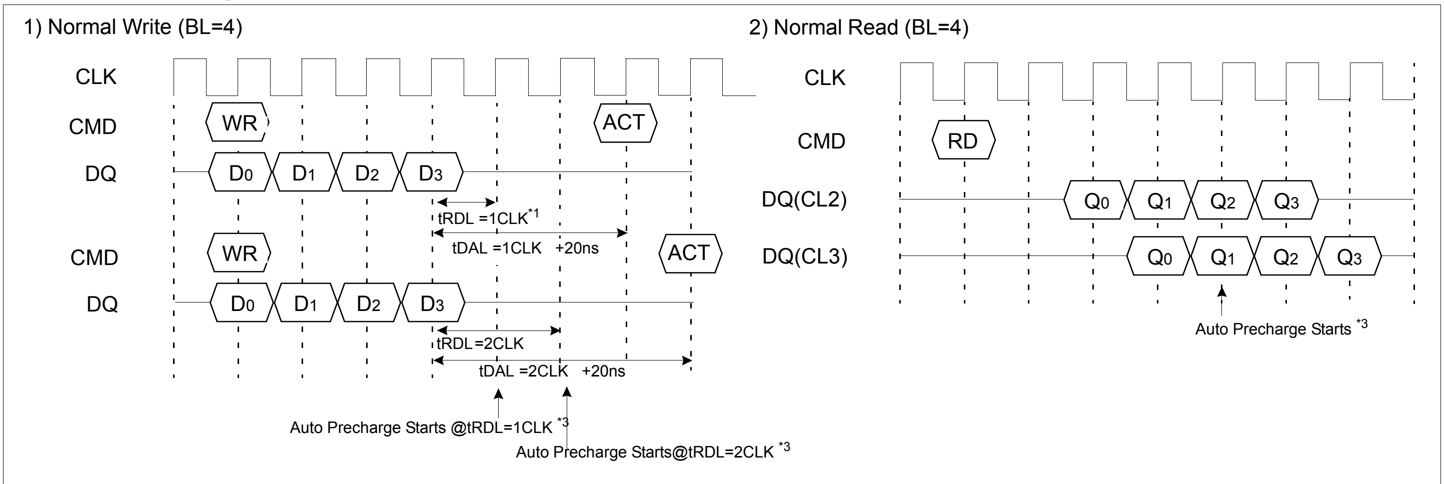


***Note :** 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

6. Precharge



7. Auto Precharge

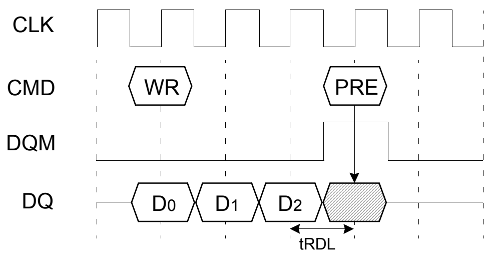


***Note :** 1. SAMSUNG can support tRDL=1CLK and tRDL=2CLK for the memory devices but SAMSUNG recommends tRDL=2 CLK.
In case of tCC< 6ns, tRDL should be only 2CLK.
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same bank is illegal

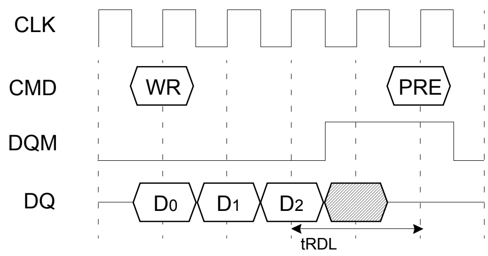
8. Burst Stop & Interrupted by Precharge

1) Normal Write

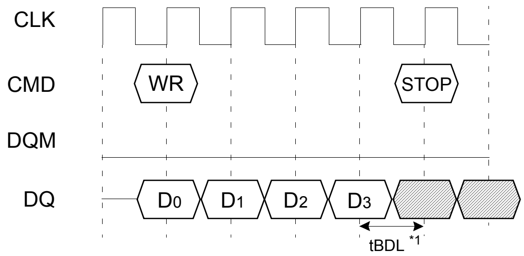
BL=4 & tRDL=1CLK



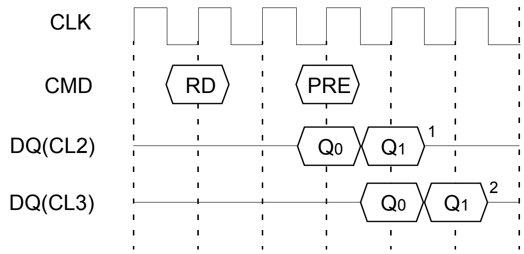
BL=4 & tRDL=2CLK



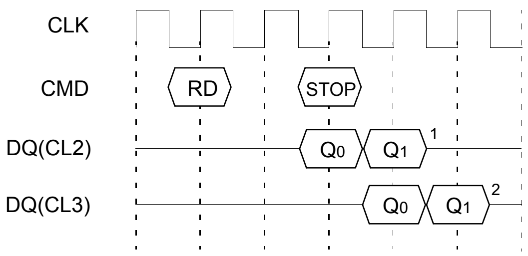
2) Write Burst Stop (BL=8)



3) Read Interrupted by Precharge (BL=4)

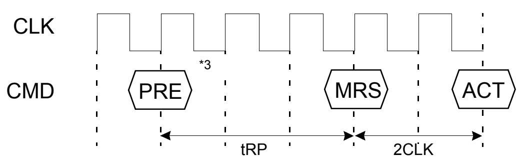


4) Read Burst Stop (BL=4)



9. MRS

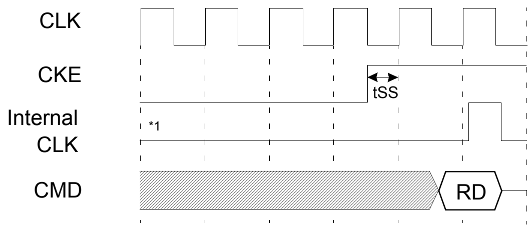
1) Mode Register Set



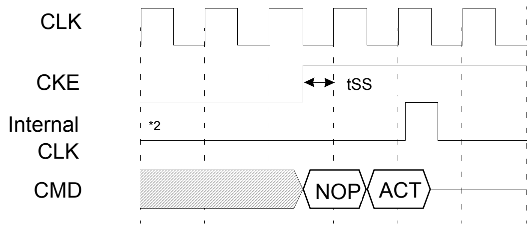
***Note :** 1. tBDL : 1 CLK ; Last data in to burst stop delay.
Read or write burst stop command is valid at every burst length.
2. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectively.
3. PRE : All banks precharge is necessary.
MRS can be issued only at all banks precharge state.

10. Clock Suspend Exit & Power Down Exit

1) Clock Suspend (=Active Power Down) Exit

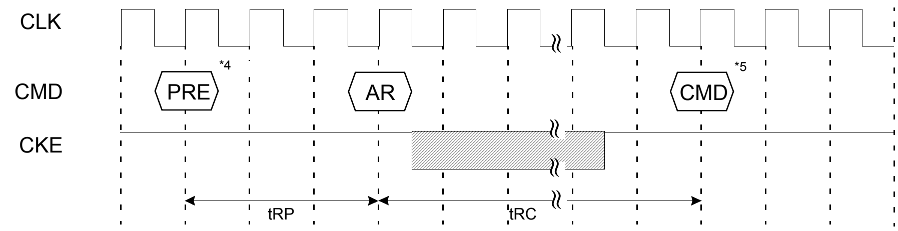


2) Power Down (=Precharge Power Down) Exit

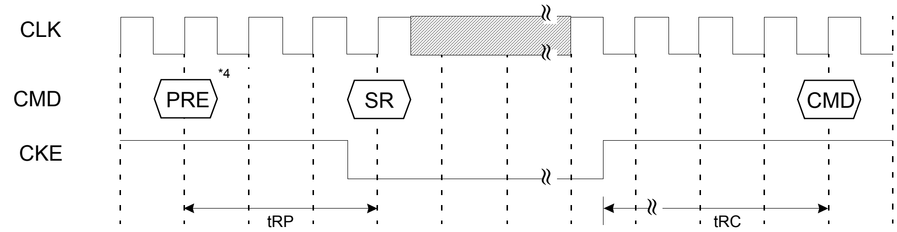


11. Auto Refresh & Self Refresh

1) Auto Refresh



2) Self Refresh Note 6



***Note :** 1. Active power down : one or more banks active state.
2. Precharge power down : all banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after auto refresh command.
During tRC from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, all banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are performed internally.
After self refresh entry, self refresh mode is kept while CKE is low.
During self refresh mode, all inputs except CKE will be don't cared, and outputs will be in Hi-Z state.
For the time interval of tRC from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle (4096 cycles for 64Mb & 128Mb, 8192 cycles for 256Mb) is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". Wrap around mode(infinite burst length) should be stopped by burst stop. $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 2 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A_{10}/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A_{10}/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	H	X	X	NOP --> Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	NOP --> Idle after t_{RP}	4

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	**Note**
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***Note :** 1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	**Note**
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Abbreviations : ABI = All Banks Idle, RA = Row Address

***Note :** 6. CKE low to high transition is asynchronous.
7. CKE low to high transition is asynchronous if restarts internal clock.
A minimum setup time 1CLK + t_{SS} must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the both banks idle state.
9. Must be a legal command.