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# Kinetis SDK v.2.0 API Reference Manual

**NXP Semiconductors**

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# Chapter 1

## Introduction

The Kinetis Software Development Kit (KSDK) 2.0 is a collection of software enablement, for NXP Kinetis Microcontrollers, that includes peripheral drivers, high-level stacks including USB and lwIP, integration with WolfSSL and mbed TLS cryptography libraries, other middleware packages (multicore support and FatFS), and integrated RTOS support for FreeRTOS,  $\mu$ C/OS-II, and  $\mu$ C/OS-III. In addition to the base enablement, the KSDK is augmented with demo applications, driver example projects, and API documentation to help users quickly leverage the support of the Kinetis SDK. The Kinetis Expert (KEx) Web UI is available to provide access to all Kinetis SDK packages. See the *Kinetis SDK v.2.0.0 Release Notes* (document KSDK200RN) and the supported Devices section at [www.nxp.com/ksdk](http://www.nxp.com/ksdk) for details.

The Kinetis SDK is built with the following runtime software components:

- ARM<sup>®</sup> and DSP standard libraries, and CMSIS-compliant device header files which provide direct access to the peripheral registers.
- Open-source peripheral drivers that provide stateless, high-performance, ease-of-use APIs. Communication drivers provide higher-level transactional APIs for a higher-performance option.
- Open-source RTOS wrapper driver built on top of KSDK peripheral drivers and leverage native RTOS services to better comply to the RTOS cases.
- Real time operation systems (RTOS) including FreeRTOS OS,  $\mu$ C/OS-II, and  $\mu$ C/OS-III.
- Stacks and middleware in source or object formats including:
  - A USB device, host, and OTG stack with comprehensive USB class support.
  - CMSIS-DSP, a suite of common signal processing functions.
  - FatFs, a FAT file system for small embedded systems.
  - Encryption software utilizing the mmCAU hardware acceleration.
  - SDMMC, a software component supporting SD Cards and eMMC.
  - mbedTLS, cryptographic SSL/TLS libraries.
  - lwIP, a light-weight TCP/IP stack.
  - WolfSSL, a cryptography and SSL/TLS library.
  - EMV L1 that complies to EMV-v4.3\_Book\_1 specification.
  - DMA Manager, a software component used for managing on-chip DMA channel resources.
  - The Kinetis SDK comes complete with software examples demonstrating the usage of the peripheral drivers, RTOS wrapper drivers, middleware and RTOSes.

All demo applications and driver examples are provided with projects for the following toolchains:

- Atollic TrueSTUDIO
- GNU toolchain for ARM<sup>®</sup> Cortex<sup>®</sup> -M with Cmake build system
- IAR Embedded Workbench
- Keil MDK
- Kinetis Design Studio

The peripheral drivers and RTOS driver wrappers can be used across multiple devices within the Kinetis product family without modification. The configuration items for each driver are encapsulated into C

language data structures. Kinetis device-specific configuration information is provided as part of the KSDK and need not be modified by the user. If necessary, the user is able to modify the peripheral driver and RTOS wrapper driver configuration during runtime. The driver examples demonstrate how to configure the drivers by passing the proper configuration data to the APIs. The Kinetis SDK folder structure is organized to reduce the total number of includes required to compile a project.

Deliverable	Location
Examples	<install_dir>/examples/
Demo Applications	<install_dir>/examples/<board_name>/demo_apps/
Driver Examples	<install_dir>/examples/<board_name>/driver_examples/
Documentation	<install_dir>/doc/
USB Documentation	<install_dir>/doc/usb/
lwIP Documentation	<install_dir>/doc/tcpip/lwip/
Middleware	<install_dir>/middleware/
DMA Manager	<install_dir>/dma_manager_<version>/
FatFS	<install_dir>/middleware/fatfs_<version>/
lwIP TCP/IP	<install_dir>/middleware/lwip_<version>/
MMCAU	<install_dir>/mmcau_<version>/
SD MMC Support	<install_dir>/sdmmc_<version>/
USB Stack	<install_dir>/middleware/usb_<version>/
Drivers	<install_dir>/<device_name>/drivers/
CMSIS Standard ARM Cortex-M Headers, math and DSP Libraries	<install_dir>/<device_name>/CMSIS/
Device Startup and Linker	<install_dir>/<device_name>/<toolchain>/
SDK Utilities	<install_dir>/<device_name>/utilities/
RTOS Kernels	<install_dir>/rtos/

Table 2: KSDK Folder Structure

The rest of this document describes the API references in detail for the peripheral drivers and RTOS wrapper drivers. For the latest version of this and other Kinetis SDK documents, see the [kex.nxp.com/apidoc](http://kex.nxp.com/apidoc).



## Chapter 2

### Driver errors status

- `kStatus_DSPI_Error` = 601
- `kStatus_EDMA_QueueFull` = 5100
- `kStatus_EDMA_Busy` = 5101
- `kStatus_ENET_RxFrameError` = 4000
- `kStatus_ENET_RxFrameFail` = 4001
- `kStatus_ENET_RxFrameEmpty` = 4002
- `kStatus_ENET_TxFrameBusy` = 4003
- `kStatus_ENET_TxFrameFail` = 4004
- `#kStatus_ENET_PtpTsRingFull` = 4005
- `#kStatus_ENET_PtpTsRingEmpty` = 4006
- `kStatus_SAI_TxBusy` = 1900
- `kStatus_SAI_RxBusy` = 1901
- `kStatus_SAI_TxError` = 1902
- `kStatus_SAI_RxError` = 1903
- `kStatus_SAI_QueueFull` = 1904
- `kStatus_SAI_TxIdle` = 1905
- `kStatus_SAI_RxIdle` = 1906
- `kStatus_SMC_StopAbort` = 3900
- `kStatus_NOTIFIER_ErrorNotificationBefore` = 9800
- `kStatus_NOTIFIER_ErrorNotificationAfter` = 9801



## Chapter 3

### Architectural Overview

This chapter provides the architectural overview for the Kinetis Software Development Kit (KSDK). It describes each layer within the architecture and its associated components.

#### Overview

The Kinetis SDK architecture consists of five key components listed below.

1. The ARM Cortex Microcontroller Software Interface Standard (CMSIS) CORE compliance device-specific header files, SOC Header, and CMSIS math/DSP libraries.
2. Peripheral Drivers
3. Real-time Operating Systems (RTOS)
4. Stacks and Middleware that integrate with the Kinetis SDK
5. Demo Applications based on the Kinetis SDK

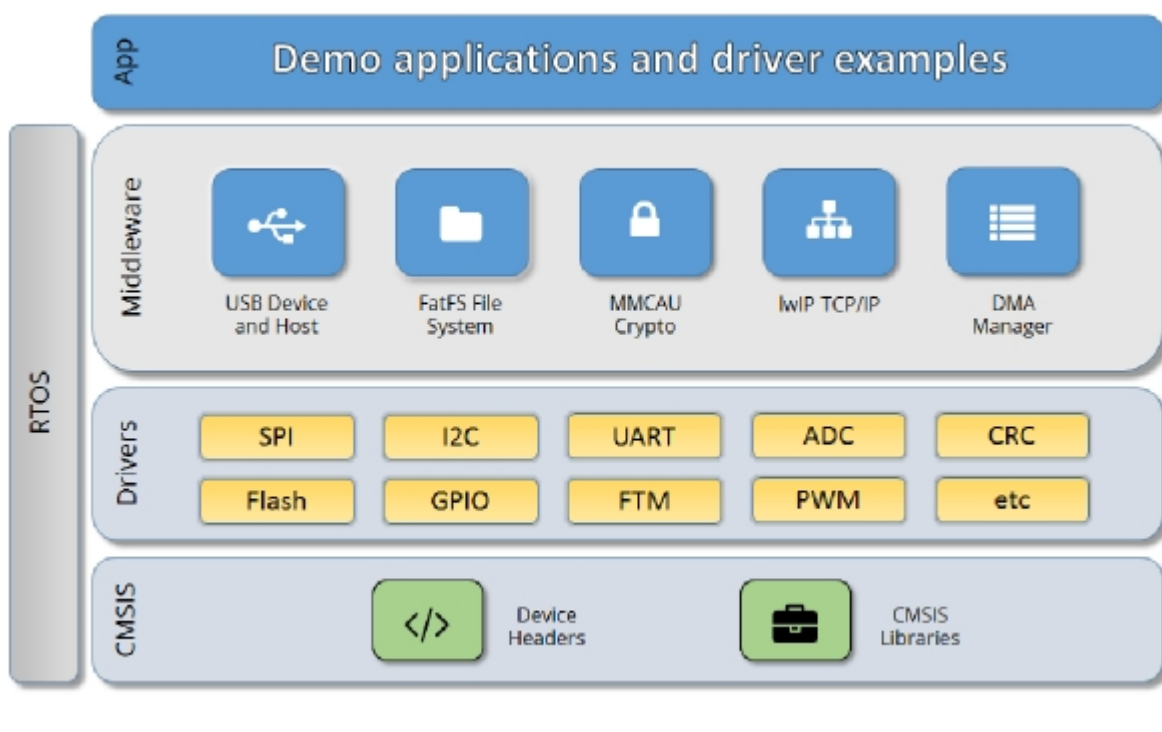


Figure 1: KSDK Block Diagram

#### Kinetis MCU header files

Each supported Kinetis MCU device in the KSDK has an overall System-on Chip (SoC) memory-mapped

header file. This header file contains the memory map and register base address for each peripheral and the IRQ vector table with associated vector numbers. The overall SoC header file provides a access to the peripheral registers through pointers and predefined bit masks. In addition to the overall SoC memory-mapped header file, the KSDK includes a feature header file for each device. The feature header file allows NXP to deliver a single software driver for a given peripheral. The feature file ensures that the driver is properly compiled for the target SOC.

## **CMSIS Support**

Along with the SoC header files and peripheral extension header files, the KSDK also includes common CMSIS header files for the ARM Cortex-M core and the math and DSP libraries from the latest CMSIS release. The CMSIS DSP library source code is also included for reference.

## **KSDK Peripheral Drivers**

The KSDK peripheral drivers mainly consist of low-level functional APIs for the Kinetis MCU product family on-chip peripherals and also of high-level transactional APIs for some bus drivers/DMA driver/e-DMA driver to quickly enable the peripherals and perform transfers.

All KSDK peripheral drivers only depend on the CMSIS headers, device feature files, `fsl_common.h`, and `fsl_clock.h` files so that users can easily pull selected drivers and their dependencies into projects. With the exception of the clock/power-relevant peripherals, each peripheral has its own driver. Peripheral drivers handle the peripheral clock gating/ungating inside the drivers during initialization and deinitialization respectively.

Low-level functional APIs provide common peripheral functionality, abstracting the hardware peripheral register accesses into a set of stateless basic functional operations. These APIs primarily focus on the control, configuration, and function of basic peripheral operations. The APIs hide the register access details and various MCU peripheral instantiation differences so that the application can be abstracted from the low-level hardware details. The API prototypes are intentionally similar to help ensure easy portability across supported KSDK devices.

Transactional APIs provide a quick method for customers to utilize higher-level functionality of the peripherals. The transactional APIs utilize interrupts and perform asynchronous operations without user intervention. Transactional APIs operate on high-level logic that requires data storage for internal operation context handling. However, the Peripheral Drivers do not allocate this memory space. Rather, the user passes in the memory to the driver for internal driver operation. Transactional APIs ensure the NVIC is enabled properly inside the drivers. The transactional APIs do not meet all customer needs, but provide a baseline for development of custom user APIs.

Note that the transactional drivers never disable an NVIC after use. This is due to the shared nature of interrupt vectors on Kinetis devices. It's up to the user to ensure that NVIC interrupts are properly disabled after usage is complete.

## **Interrupt handling for transactional APIs**

A double weak mechanism is introduced for drivers with transactional API. The double weak indicates two levels of weak vector entries. See the examples below:

```
PUBWEAK SPI0_IRQHandler
PUBWEAK SPI0_DriverIRQHandler
SPI0_IRQHandler
```

```
LDR    R0, =SPI0_DriverIRQHandler
BX     R0
```

The first level of the weak implementation are the functions defined in the vector table. In the devices/(<DEVICE\_NAME>)/(<TOOLCHAIN>)/startup\_(<DEVICE\_NAME>).S file, the implementation of the first layer weak function calls the second layer of weak function. The implementation of the second layer weak function (ex. SPI0\_DriverIRQHandler) jumps to itself (B .). The KSDK drivers with transactional APIs provide the reimplement of the second layer function inside of the peripheral driver. If the KSDK drivers with transactional APIs are linked into the image, the SPI0\_DriverIRQHandler is replaced with the function implemented in the KSDK SPI driver.

The reason for implementing the double weak functions is to provide a better user experience when using the transactional APIs. For drivers with a transactional function, call the transactional APIs and the drivers complete the interrupt-driven flow. Users are not required to redefine the vector entries out of the box. At the same time, if users are not satisfied by the second layer weak function implemented in the KSDK drivers, users can redefine the first layer weak function and implement their own interrupt handler functions to suit their implementation.

The limitation of the double weak mechanism is that it cannot be used for peripherals that share the same vector entry. For this use case, redefine the first layer weak function to enable the desired peripheral interrupt functionality. For example, if the MCU's UART0 and UART1 share the same vector entry, redefine the UART0\_UART1\_IRQHandler according to the use case requirements.

## Feature Header Files

The peripheral drivers are designed to be reusable regardless of the peripheral functional differences from one Kinetis MCU device to another. An overall Peripheral Feature Header File is provided for the KSDK-supported MCU device to define the features or configuration differences for each Kinetis sub-family device.

## Application

See the *Getting Started with Kinetis SDK (KSDK) v2.0* document (KSDK20GSUG).



## Chapter 4

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## Chapter 5

# ADC16: 16-bit SAR Analog-to-Digital Converter Driver

### 5.1 Overview

The KSDK provides a peripheral driver for the 16-bit SAR Analog-to-Digital Converter (ADC16) module of Kinetis devices.

### 5.2 Typical use case

#### 5.2.1 Polling Configuration

```
adc16_config_t adc16ConfigStruct;
adc16_channel_config_t adc16ChannelConfigStruct;

ADC16_Init(DEMO_ADC16_INSTANCE);
ADC16_GetDefaultConfig(&adc16ConfigStruct);
ADC16_Configure(DEMO_ADC16_INSTANCE, &adc16ConfigStruct);
ADC16_EnableHardwareTrigger(DEMO_ADC16_INSTANCE, false);
#if defined(FSL_FEATURE_ADC16_HAS_CALIBRATION) && FSL_FEATURE_ADC16_HAS_CALIBRATION
if (kStatus_Success == ADC16_DoAutoCalibration(DEMO_ADC16_INSTANCE))
{
    PRINTF("ADC16_DoAutoCalibration() Done.\r\n");
}
else
{
    PRINTF("ADC16_DoAutoCalibration() Failed.\r\n");
}
#endif // FSL_FEATURE_ADC16_HAS_CALIBRATION

adc16ChannelConfigStruct.channelNumber = DEMO_ADC16_USER_CHANNEL;
adc16ChannelConfigStruct.enableInterruptOnConversionCompleted =
    false;
#if defined(FSL_FEATURE_ADC16_HAS_DIFF_MODE) && FSL_FEATURE_ADC16_HAS_DIFF_MODE
adc16ChannelConfigStruct.enabledDifferentialConversion = false;
#endif // FSL_FEATURE_ADC16_HAS_DIFF_MODE

while(1)
{
    GETCHAR(); // Input any key in terminal console.
    ADC16_ChannelConfigure(DEMO_ADC16_INSTANCE, DEMO_ADC16_CHANNEL_GROUP, &adc16ChannelConfigStruct);
    while (kADC16_ChannelConversionDoneFlag !=
        ADC16_ChannelGetStatusFlags(DEMO_ADC16_INSTANCE, DEMO_ADC16_CHANNEL_GROUP))
    {
    }
    PRINTF("ADC Value: %d\r\n", ADC16_ChannelGetConversionValue(DEMO_ADC16_INSTANCE,
        DEMO_ADC16_CHANNEL_GROUP));
}
```

#### 5.2.2 Interrupt Configuration

```
volatile bool g_Adc16ConversionDoneFlag = false;
volatile uint32_t g_Adc16ConversionValue;
volatile uint32_t g_Adc16InterruptCount = 0U;
```

## Typical use case

```
// ...

adc16_config_t adc16ConfigStruct;
adc16_channel_config_t adc16ChannelConfigStruct;

ADC16_Init (DEMO_ADC16_INSTANCE);
ADC16_GetDefaultConfig(&adc16ConfigStruct);
ADC16_Configure(DEMO_ADC16_INSTANCE, &adc16ConfigStruct);
ADC16_EnableHardwareTrigger(DEMO_ADC16_INSTANCE, false);
#if defined(FSL_FEATURE_ADC16_HAS_CALIBRATION) && FSL_FEATURE_ADC16_HAS_CALIBRATION
    if (ADC16_DoAutoCalibration(DEMO_ADC16_INSTANCE))
    {
        PRINTF("ADC16_DoAutoCalibration() Done.\r\n");
    }
    else
    {
        PRINTF("ADC16_DoAutoCalibration() Failed.\r\n");
    }
#endif // FSL_FEATURE_ADC16_HAS_CALIBRATION

adc16ChannelConfigStruct.channelNumber = DEMO_ADC16_USER_CHANNEL;
adc16ChannelConfigStruct.enableInterruptOnConversionCompleted =
    true; // Enable the interrupt.
#if defined(FSL_FEATURE_ADC16_HAS_DIFF_MODE) && FSL_FEATURE_ADC16_HAS_DIFF_MODE
    adc16ChannelConfigStruct.enableDifferentialConversion = false;
#endif // FSL_FEATURE_ADC16_HAS_DIFF_MODE

while(1)
{
    GETCHAR(); // Input a key in the terminal console.
    g_Adc16ConversionDoneFlag = false;
    ADC16_ChannelConfigure(DEMO_ADC16_INSTANCE, DEMO_ADC16_CHANNEL_GROUP, &adc16ChannelConfigStruct);
    while (!g_Adc16ConversionDoneFlag)
    {
    }
    PRINTF("ADC Value: %d\r\n", g_Adc16ConversionValue);
    PRINTF("ADC Interrupt Count: %d\r\n", g_Adc16InterruptCount);
}

// ...

void DEMO_ADC16_IRQHandler(void)
{
    g_Adc16ConversionDoneFlag = true;
    // Read the conversion result to clear the conversion completed flag.
    g_Adc16ConversionValue = ADC16_ChannelConversionValue(DEMO_ADC16_INSTANCE, DEMO_ADC16_CHANNEL_GROUP);
    g_Adc16InterruptCount++;
}
```

## Data Structures

- struct [adc16\\_config\\_t](#)  
*ADC16 converter configuration. [More...](#)*
- struct [adc16\\_hardware\\_compare\\_config\\_t](#)  
*ADC16 Hardware comparison configuration. [More...](#)*
- struct [adc16\\_channel\\_config\\_t](#)  
*ADC16 channel conversion configuration. [More...](#)*

## Enumerations

- enum [\\_adc16\\_channel\\_status\\_flags](#) { [kADC16\\_ChannelConversionDoneFlag](#) = [ADC\\_SC1\\_COCO\\_MASK](#) }

- Channel status flags.*
  - enum `_adc16_status_flags` {  
`kADC16_ActiveFlag` = `ADC_SC2_ADACT_MASK`,  
`kADC16_CalibrationFailedFlag` = `ADC_SC3_CALF_MASK` }
  - Converter status flags.*
  - enum `adc16_channel_mux_mode_t` {  
`kADC16_ChannelMuxA` = `0U`,  
`kADC16_ChannelMuxB` = `1U` }
  - Channel multiplexer mode for each channel.*
  - enum `adc16_clock_divider_t` {  
`kADC16_ClockDivider1` = `0U`,  
`kADC16_ClockDivider2` = `1U`,  
`kADC16_ClockDivider4` = `2U`,  
`kADC16_ClockDivider8` = `3U` }
  - Clock divider for the converter.*
  - enum `adc16_resolution_t` {  
`kADC16_Resolution8or9Bit` = `0U`,  
`kADC16_Resolution12or13Bit` = `1U`,  
`kADC16_Resolution10or11Bit` = `2U`,  
`kADC16_ResolutionSE8Bit` = `kADC16_Resolution8or9Bit`,  
`kADC16_ResolutionSE12Bit` = `kADC16_Resolution12or13Bit`,  
`kADC16_ResolutionSE10Bit` = `kADC16_Resolution10or11Bit`,  
`kADC16_ResolutionDF9Bit` = `kADC16_Resolution8or9Bit`,  
`kADC16_ResolutionDF13Bit` = `kADC16_Resolution12or13Bit`,  
`kADC16_ResolutionDF11Bit` = `kADC16_Resolution10or11Bit`,  
`kADC16_Resolution16Bit` = `3U`,  
`kADC16_ResolutionSE16Bit` = `kADC16_Resolution16Bit`,  
`kADC16_ResolutionDF16Bit` = `kADC16_Resolution16Bit` }
  - Converter's resolution.*
  - enum `adc16_clock_source_t` {  
`kADC16_ClockSourceAlt0` = `0U`,  
`kADC16_ClockSourceAlt1` = `1U`,  
`kADC16_ClockSourceAlt2` = `2U`,  
`kADC16_ClockSourceAlt3` = `3U`,  
`kADC16_ClockSourceAsynchronousClock` = `kADC16_ClockSourceAlt3` }
  - Clock source.*
  - enum `adc16_long_sample_mode_t` {  
`kADC16_LongSampleCycle24` = `0U`,  
`kADC16_LongSampleCycle16` = `1U`,  
`kADC16_LongSampleCycle10` = `2U`,  
`kADC16_LongSampleCycle6` = `3U`,  
`kADC16_LongSampleDisabled` = `4U` }
  - Long sample mode.*
  - enum `adc16_reference_voltage_source_t` {  
`kADC16_ReferenceVoltageSourceVref` = `0U`,  
`kADC16_ReferenceVoltageSourceValt` = `1U` }

## Typical use case

- Reference voltage source.*
  - enum [adc16\\_hardware\\_average\\_mode\\_t](#) {  
    [kADC16\\_HardwareAverageCount4](#) = 0U,  
    [kADC16\\_HardwareAverageCount8](#) = 1U,  
    [kADC16\\_HardwareAverageCount16](#) = 2U,  
    [kADC16\\_HardwareAverageCount32](#) = 3U,  
    [kADC16\\_HardwareAverageDisabled](#) = 4U }
- Hardware average mode.*
  - enum [adc16\\_hardware\\_compare\\_mode\\_t](#) {  
    [kADC16\\_HardwareCompareMode0](#) = 0U,  
    [kADC16\\_HardwareCompareMode1](#) = 1U,  
    [kADC16\\_HardwareCompareMode2](#) = 2U,  
    [kADC16\\_HardwareCompareMode3](#) = 3U }
- Hardware compare mode.*

## Driver version

- #define [FSL\\_ADC16\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 0, 0))  
*ADC16 driver version 2.0.0.*

## Initialization

- void [ADC16\\_Init](#) (ADC\_Type \*base, const [adc16\\_config\\_t](#) \*config)  
*Initializes the ADC16 module.*
- void [ADC16\\_Deinit](#) (ADC\_Type \*base)  
*De-initializes the ADC16 module.*
- void [ADC16\\_GetDefaultConfig](#) ([adc16\\_config\\_t](#) \*config)  
*Gets an available pre-defined settings for the converter's configuration.*
- status\_t [ADC16\\_DoAutoCalibration](#) (ADC\_Type \*base)  
*Automates the hardware calibration.*
- static void [ADC16\\_SetOffsetValue](#) (ADC\_Type \*base, int16\_t value)  
*Sets the offset value for the conversion result.*

## Advanced Features

- static void [ADC16\\_EnableDMA](#) (ADC\_Type \*base, bool enable)  
*Enables generating the DMA trigger when the conversion is complete.*
- static void [ADC16\\_EnableHardwareTrigger](#) (ADC\_Type \*base, bool enable)  
*Enables the hardware trigger mode.*
- void [ADC16\\_SetChannelMuxMode](#) (ADC\_Type \*base, [adc16\\_channel\\_mux\\_mode\\_t](#) mode)  
*Sets the channel mux mode.*
- void [ADC16\\_SetHardwareCompareConfig](#) (ADC\_Type \*base, const [adc16\\_hardware\\_compare\\_config\\_t](#) \*config)  
*Configures the hardware compare mode.*
- void [ADC16\\_SetHardwareAverage](#) (ADC\_Type \*base, [adc16\\_hardware\\_average\\_mode\\_t](#) mode)  
*Sets the hardware average mode.*
- uint32\_t [ADC16\\_GetStatusFlags](#) (ADC\_Type \*base)  
*Gets the status flags of the converter.*
- void [ADC16\\_ClearStatusFlags](#) (ADC\_Type \*base, uint32\_t mask)  
*Clears the status flags of the converter.*

## Conversion Channel

- void [ADC16\\_SetChannelConfig](#) (ADC\_Type \*base, uint32\_t channelGroup, const [adc16\\_channel\\_config\\_t](#) \*config)  
*Configures the conversion channel.*
- static uint32\_t [ADC16\\_GetChannelConversionValue](#) (ADC\_Type \*base, uint32\_t channelGroup)  
*Gets the conversion value.*
- uint32\_t [ADC16\\_GetChannelStatusFlags](#) (ADC\_Type \*base, uint32\_t channelGroup)  
*Gets the status flags of channel.*

## 5.3 Data Structure Documentation

### 5.3.1 struct adc16\_config\_t

#### Data Fields

- [adc16\\_reference\\_voltage\\_source\\_t](#) referenceVoltageSource  
*Select the reference voltage source.*
- [adc16\\_clock\\_source\\_t](#) clockSource  
*Select the input clock source to converter.*
- bool [enableAsynchronousClock](#)  
*Enable the asynchronous clock output.*
- [adc16\\_clock\\_divider\\_t](#) clockDivider  
*Select the divider of input clock source.*
- [adc16\\_resolution\\_t](#) resolution  
*Select the sample resolution mode.*
- [adc16\\_long\\_sample\\_mode\\_t](#) longSampleMode  
*Select the long sample mode.*
- bool [enableHighSpeed](#)  
*Enable the high-speed mode.*
- bool [enableLowPower](#)  
*Enable low power.*
- bool [enableContinuousConversion](#)  
*Enable continuous conversion mode.*

## Data Structure Documentation

### 5.3.1.0.0.1 Field Documentation

5.3.1.0.0.1.1 `adc16_reference_voltage_source_t` `adc16_config_t::referenceVoltageSource`

5.3.1.0.0.1.2 `adc16_clock_source_t` `adc16_config_t::clockSource`

5.3.1.0.0.1.3 `bool` `adc16_config_t::enableAsynchronousClock`

5.3.1.0.0.1.4 `adc16_clock_divider_t` `adc16_config_t::clockDivider`

5.3.1.0.0.1.5 `adc16_resolution_t` `adc16_config_t::resolution`

5.3.1.0.0.1.6 `adc16_long_sample_mode_t` `adc16_config_t::longSampleMode`

5.3.1.0.0.1.7 `bool` `adc16_config_t::enableHighSpeed`

5.3.1.0.0.1.8 `bool` `adc16_config_t::enableLowPower`

5.3.1.0.0.1.9 `bool` `adc16_config_t::enableContinuousConversion`

### 5.3.2 struct `adc16_hardware_compare_config_t`

#### Data Fields

- [adc16\\_hardware\\_compare\\_mode\\_t](#) `hardwareCompareMode`  
*Select the hardware compare mode.*
- `int16_t` [value1](#)  
*Setting value1 for hardware compare mode.*
- `int16_t` [value2](#)  
*Setting value2 for hardware compare mode.*

### 5.3.2.0.0.2 Field Documentation

5.3.2.0.0.2.1 `adc16_hardware_compare_mode_t` `adc16_hardware_compare_config_t::hardwareCompareMode`

See "`adc16_hardware_compare_mode_t`".

5.3.2.0.0.2.2 `int16_t` `adc16_hardware_compare_config_t::value1`

5.3.2.0.0.2.3 `int16_t` `adc16_hardware_compare_config_t::value2`

### 5.3.3 struct `adc16_channel_config_t`

#### Data Fields

- `uint32_t` [channelNumber](#)  
*Setting the conversion channel number.*
- `bool` [enableInterruptOnConversionCompleted](#)

- *Generate an interrupt request once the conversion is completed.*  
 • bool [enableDifferentialConversion](#)  
*Using Differential sample mode.*

### 5.3.3.0.0.3 Field Documentation

#### 5.3.3.0.0.3.1 uint32\_t adc16\_channel\_config\_t::channelNumber

The available range is 0-31. See channel connection information for each chip in Reference Manual document.

#### 5.3.3.0.0.3.2 bool adc16\_channel\_config\_t::enableInterruptOnConversionCompleted

#### 5.3.3.0.0.3.3 bool adc16\_channel\_config\_t::enableDifferentialConversion

## 5.4 Macro Definition Documentation

### 5.4.1 #define FSL\_ADC16\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 0))

## 5.5 Enumeration Type Documentation

### 5.5.1 enum \_adc16\_channel\_status\_flags

Enumerator

*kADC16\_ChannelConversionDoneFlag* Conversion done.

### 5.5.2 enum \_adc16\_status\_flags

Enumerator

*kADC16\_ActiveFlag* Converter is active.

*kADC16\_CalibrationFailedFlag* Calibration is failed.

### 5.5.3 enum adc16\_channel\_mux\_mode\_t

For some ADC16 channels, there are two pin selections in channel multiplexer. For example, ADC0\_SE4a and ADC0\_SE4b are the different channels that share the same channel number.

Enumerator

*kADC16\_ChannelMuxA* For channel with channel mux a.

*kADC16\_ChannelMuxB* For channel with channel mux b.

### 5.5.4 enum adc16\_clock\_divider\_t

Enumerator

- kADC16\_ClockDivider1* For divider 1 from the input clock to the module.
- kADC16\_ClockDivider2* For divider 2 from the input clock to the module.
- kADC16\_ClockDivider4* For divider 4 from the input clock to the module.
- kADC16\_ClockDivider8* For divider 8 from the input clock to the module.

### 5.5.5 enum adc16\_resolution\_t

Enumerator

- kADC16\_Resolution8or9Bit* Single End 8-bit or Differential Sample 9-bit.
- kADC16\_Resolution12or13Bit* Single End 12-bit or Differential Sample 13-bit.
- kADC16\_Resolution10or11Bit* Single End 10-bit or Differential Sample 11-bit.
- kADC16\_ResolutionSE8Bit* Single End 8-bit.
- kADC16\_ResolutionSE12Bit* Single End 12-bit.
- kADC16\_ResolutionSE10Bit* Single End 10-bit.
- kADC16\_ResolutionDF9Bit* Differential Sample 9-bit.
- kADC16\_ResolutionDF13Bit* Differential Sample 13-bit.
- kADC16\_ResolutionDF11Bit* Differential Sample 11-bit.
- kADC16\_Resolution16Bit* Single End 16-bit or Differential Sample 16-bit.
- kADC16\_ResolutionSE16Bit* Single End 16-bit.
- kADC16\_ResolutionDF16Bit* Differential Sample 16-bit.

### 5.5.6 enum adc16\_clock\_source\_t

Enumerator

- kADC16\_ClockSourceAlt0* Selection 0 of the clock source.
- kADC16\_ClockSourceAlt1* Selection 1 of the clock source.
- kADC16\_ClockSourceAlt2* Selection 2 of the clock source.
- kADC16\_ClockSourceAlt3* Selection 3 of the clock source.
- kADC16\_ClockSourceAsynchronousClock* Using internal asynchronous clock.

### 5.5.7 enum adc16\_long\_sample\_mode\_t

Enumerator

- kADC16\_LongSampleCycle24* 20 extra ADCK cycles, 24 ADCK cycles total.
- kADC16\_LongSampleCycle16* 12 extra ADCK cycles, 16 ADCK cycles total.



***kADC16\_LongSampleCycle10*** 6 extra ADCK cycles, 10 ADCK cycles total.

***kADC16\_LongSampleCycle6*** 2 extra ADCK cycles, 6 ADCK cycles total.

***kADC16\_LongSampleDisabled*** Disable the long sample feature.

### 5.5.8 enum adc16\_reference\_voltage\_source\_t

Enumerator

***kADC16\_ReferenceVoltageSourceVref*** For external pins pair of VrefH and VrefL.

***kADC16\_ReferenceVoltageSourceValt*** For alternate reference pair of ValtH and ValtL.

### 5.5.9 enum adc16\_hardware\_average\_mode\_t

Enumerator

***kADC16\_HardwareAverageCount4*** For hardware average with 4 samples.

***kADC16\_HardwareAverageCount8*** For hardware average with 8 samples.

***kADC16\_HardwareAverageCount16*** For hardware average with 16 samples.

***kADC16\_HardwareAverageCount32*** For hardware average with 32 samples.

***kADC16\_HardwareAverageDisabled*** Disable the hardware average feature.

### 5.5.10 enum adc16\_hardware\_compare\_mode\_t

Enumerator

***kADC16\_HardwareCompareMode0***  $x < \text{value1}$ .

***kADC16\_HardwareCompareMode1***  $x > \text{value1}$ .

***kADC16\_HardwareCompareMode2*** if  $\text{value1} \leq \text{value2}$ , then  $x < \text{value1} \parallel x > \text{value2}$ ; else,  $\text{value1} > x > \text{value2}$ .

***kADC16\_HardwareCompareMode3*** if  $\text{value1} \leq \text{value2}$ , then  $\text{value1} \leq x \leq \text{value2}$ ; else  $x > \text{value1} \parallel x \leq \text{value2}$ .

## 5.6 Function Documentation

### 5.6.1 void ADC16\_Init ( ADC\_Type \* *base*, const adc16\_config\_t \* *config* )

## Function Documentation

### Parameters

<i>base</i>	ADC16 peripheral base address.
<i>config</i>	Pointer to configuration structure. See "adc16_config_t".

### 5.6.2 void ADC16\_Deinit ( ADC\_Type \* *base* )

#### Parameters

<i>base</i>	ADC16 peripheral base address.
-------------	--------------------------------

### 5.6.3 void ADC16\_GetDefaultConfig ( adc16\_config\_t \* *config* )

This function initializes the converter configuration structure with available settings. The default values are as follows.

```
* config->referenceVoltageSource = kADC16_ReferenceVoltageSourceVref
* ;
* config->clockSource = kADC16_ClockSourceAsynchronousClock
* ;
* config->enableAsynchronousClock = true;
* config->clockDivider = kADC16_ClockDivider8;
* config->resolution = kADC16_ResolutionSE12Bit;
* config->longSampleMode = kADC16_LongSampleDisabled;
* config->enableHighSpeed = false;
* config->enableLowPower = false;
* config->enableContinuousConversion = false;
*
```

#### Parameters

<i>config</i>	Pointer to the configuration structure.
---------------	---

### 5.6.4 status\_t ADC16\_DoAutoCalibration ( ADC\_Type \* *base* )

This auto calibration helps to adjust the plus/minus side gain automatically. Execute the calibration before using the converter. Note that the hardware trigger should be used during the calibration.

## Parameters

<i>base</i>	ADC16 peripheral base address.
-------------	--------------------------------

## Returns

Execution status.

## Return values

<i>kStatus_Success</i>	Calibration is done successfully.
<i>kStatus_Fail</i>	Calibration has failed.

### 5.6.5 static void ADC16\_SetOffsetValue ( ADC\_Type \* *base*, int16\_t *value* ) [inline], [static]

This offset value takes effect on the conversion result. If the offset value is not zero, the reading result is subtracted by it. Note, the hardware calibration fills the offset value automatically.

## Parameters

<i>base</i>	ADC16 peripheral base address.
<i>value</i>	Setting offset value.

### 5.6.6 static void ADC16\_EnableDMA ( ADC\_Type \* *base*, bool *enable* ) [inline], [static]

## Parameters

<i>base</i>	ADC16 peripheral base address.
<i>enable</i>	Switcher of the DMA feature. "true" means enabled, "false" means not enabled.

### 5.6.7 static void ADC16\_EnableHardwareTrigger ( ADC\_Type \* *base*, bool *enable* ) [inline], [static]

## Function Documentation

### Parameters

<i>base</i>	ADC16 peripheral base address.
<i>enable</i>	Switcher of the hardware trigger feature. "true" means enabled, "false" means not enabled.

### 5.6.8 void ADC16\_SetChannelMuxMode ( ADC\_Type \* *base*, adc16\_channel\_mux\_mode\_t *mode* )

Some sample pins share the same channel index. The channel mux mode decides which pin is used for an indicated channel.

### Parameters

<i>base</i>	ADC16 peripheral base address.
<i>mode</i>	Setting channel mux mode. See "adc16_channel_mux_mode_t".

### 5.6.9 void ADC16\_SetHardwareCompareConfig ( ADC\_Type \* *base*, const adc16\_hardware\_compare\_config\_t \* *config* )

The hardware compare mode provides a way to process the conversion result automatically by using hardware. Only the result in the compare range is available. To compare the range, see "adc16\_hardware\_compare\_mode\_t" or the appropriate reference manual for more information.

### Parameters

<i>base</i>	ADC16 peripheral base address.
<i>config</i>	Pointer to the "adc16_hardware_compare_config_t" structure. Passing "NULL" disables the feature.

### 5.6.10 void ADC16\_SetHardwareAverage ( ADC\_Type \* *base*, adc16\_hardware\_average\_mode\_t *mode* )

The hardware average mode provides a way to process the conversion result automatically by using hardware. The multiple conversion results are accumulated and averaged internally making them easier to read.

## Parameters

<i>base</i>	ADC16 peripheral base address.
<i>mode</i>	Setting the hardware average mode. See "adc16_hardware_average_mode_t".

**5.6.11 uint32\_t ADC16\_GetStatusFlags ( ADC\_Type \* *base* )**

## Parameters

<i>base</i>	ADC16 peripheral base address.
-------------	--------------------------------

## Returns

Flags' mask if indicated flags are asserted. See "\_adc16\_status\_flags".

**5.6.12 void ADC16\_ClearStatusFlags ( ADC\_Type \* *base*, uint32\_t *mask* )**

## Parameters

<i>base</i>	ADC16 peripheral base address.
<i>mask</i>	Mask value for the cleared flags. See "_adc16_status_flags".

**5.6.13 void ADC16\_SetChannelConfig ( ADC\_Type \* *base*, uint32\_t *channelGroup*, const adc16\_channel\_config\_t \* *config* )**

This operation triggers the conversion when in software trigger mode. When in hardware trigger mode, this API configures the channel while the external trigger source helps to trigger the conversion.

Note that the "Channel Group" has a detailed description. To allow sequential conversions of the ADC to be triggered by internal peripherals, the ADC has more than one group of status and control registers, one for each conversion. The channel group parameter indicates which group of registers are used, for example, channel group 0 is for Group A registers and channel group 1 is for Group B registers. The channel groups are used in a "ping-pong" approach to control the ADC operation. At any point, only one of the channel groups is actively controlling ADC conversions. The channel group 0 is used for both software and hardware trigger modes. Channel group 1 and greater indicates multiple channel group registers for use only in hardware trigger mode. See the chip configuration information in the appropriate MCU reference manual for the number of SC1n registers (channel groups) specific to this device. Channel group 1 or greater are not used for software trigger operation. Therefore, writing to these channel groups does not initiate a new conversion. Updating the channel group 0 while a different channel group is

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## Function Documentation

actively controlling a conversion is allowed and vice versa. Writing any of the channel group registers while that specific channel group is actively controlling a conversion aborts the current conversion.

## Parameters

<i>base</i>	ADC16 peripheral base address.
<i>channelGroup</i>	Channel group index.
<i>config</i>	Pointer to the "adc16_channel_config_t" structure for the conversion channel.

#### 5.6.14 static uint32\_t ADC16\_GetChannelConversionValue ( ADC\_Type \* *base*, uint32\_t *channelGroup* ) [inline], [static]

## Parameters

<i>base</i>	ADC16 peripheral base address.
<i>channelGroup</i>	Channel group index.

## Returns

Conversion value.

#### 5.6.15 uint32\_t ADC16\_GetChannelStatusFlags ( ADC\_Type \* *base*, uint32\_t *channelGroup* )

## Parameters

<i>base</i>	ADC16 peripheral base address.
<i>channelGroup</i>	Channel group index.

## Returns

Flags' mask if indicated flags are asserted. See "\_adc16\_channel\_status\_flags".





## Chapter 6

# CMP: Analog Comparator Driver

### 6.1 Overview

The KSDK provides a peripheral driver for the Analog Comparator (CMP) module of Kinetis devices.

The CMP driver is a basic comparator with advanced features. The APIs for the basic comparator enable the CMP to compare the two voltages of the two input channels and create the output of the comparator result. The APIs for advanced features can be used as the plug-in functions based on the basic comparator. They can process the comparator's output with hardware support.

### 6.2 Typical use case

#### 6.2.1 Polling Configuration

```
int main(void)
{
    cmp_config_t mCmpConfigStruct;
    cmp_dac_config_t mCmpDacConfigStruct;

    // ...

    // Configures the comparator.
    CMP_Init(DEMO_CMP_INSTANCE);
    CMP_GetDefaultConfig(&mCmpConfigStruct);
    CMP_Configure(DEMO_CMP_INSTANCE, &mCmpConfigStruct);

    // Configures the DAC channel.
    mCmpDacConfigStruct.referenceVoltageSource =
        kCMP_VrefSourceVin2; // VCC.
    mCmpDacConfigStruct.DACValue = 32U; // Half voltage of logic high-level.
    CMP_SetDACConfig(DEMO_CMP_INSTANCE, &mCmpDacConfigStruct);
    CMP_SetInputChannels(DEMO_CMP_INSTANCE, DEMO_CMP_USER_CHANNEL, DEMO_CMP_DAC_CHANNEL);

    while (1)
    {
        if (0U != (kCMP_OutputAssertEventFlag &
            CMP_GetStatusFlags(DEMO_CMP_INSTANCE)))
        {
            // Do something.
        }
        else
        {
            // Do something.
        }
    }
}
```

#### 6.2.2 Interrupt Configuration

```
volatile uint32_t g_CmpFlags = 0U;
```

## Typical use case

```
// ...

void DEMO_CMP_IRQ_HANDLER_FUNC(void)
{
    g_CmpFlags = CMP_GetStatusFlags(DEMO_CMP_INSTANCE);
    CMP_ClearStatusFlags(DEMO_CMP_INSTANCE, kCMP_OutputRisingEventFlag |
        kCMP_OutputFallingEventFlag);
    if (0U != (g_CmpFlags & kCMP_OutputRisingEventFlag))
    {
        // Do something.
    }
    else if (0U != (g_CmpFlags & kCMP_OutputFallingEventFlag))
    {
        // Do something.
    }
}

int main(void)
{
    cmp_config_t mCmpConfigStruct;
    cmp_dac_config_t mCmpDacConfigStruct;

    // ...
    EnableIRQ(DEMO_CMP_IRQ_ID);
    // ...

    // Configures the comparator.
    CMP_Init(DEMO_CMP_INSTANCE);
    CMP_GetDefaultConfig(&mCmpConfigStruct);
    CMP_Configure(DEMO_CMP_INSTANCE, &mCmpConfigStruct);

    // Configures the DAC channel.
    mCmpDacConfigStruct.referenceVoltageSource =
        kCMP_VrefSourceVin2; // VCC.
    mCmpDacConfigStruct.DACValue = 32U; // Half voltage of logic high-level.
    CMP_SetDACConfig(DEMO_CMP_INSTANCE, &mCmpDacConfigStruct);
    CMP_SetInputChannels(DEMO_CMP_INSTANCE, DEMO_CMP_USER_CHANNEL, DEMO_CMP_DAC_CHANNEL
        );

    // Enables the output rising and falling interrupts.
    CMP_EnableInterrupts(DEMO_CMP_INSTANCE,
        kCMP_OutputRisingInterruptEnable |
        kCMP_OutputFallingInterruptEnable);

    while (1)
    {
    }
}
```

## Data Structures

- struct `cmp_config_t`  
*Configures the comparator. [More...](#)*
- struct `cmp_filter_config_t`  
*Configures the filter. [More...](#)*
- struct `cmp_dac_config_t`  
*Configures the internal DAC. [More...](#)*

## Enumerations

- enum `_cmp_interrupt_enable` {  
    `kCMP_OutputRisingInterruptEnable` = `CMP_SCR_IER_MASK`,  
    `kCMP_OutputFallingInterruptEnable` = `CMP_SCR_IEF_MASK` }

- *Interrupt enable/disable mask.*  
enum `_cmp_status_flags` {  
    `kCMP_OutputRisingEventFlag` = `CMP_SCR_CFR_MASK`,  
    `kCMP_OutputFallingEventFlag` = `CMP_SCR_CFF_MASK`,  
    `kCMP_OutputAssertEventFlag` = `CMP_SCR_COUT_MASK` }
- *Status flags' mask.*  
enum `cmp_hysteresis_mode_t` {  
    `kCMP_HysteresisLevel0` = `0U`,  
    `kCMP_HysteresisLevel1` = `1U`,  
    `kCMP_HysteresisLevel2` = `2U`,  
    `kCMP_HysteresisLevel3` = `3U` }
- *CMP Hysteresis mode.*  
enum `cmp_reference_voltage_source_t` {  
    `kCMP_VrefSourceVin1` = `0U`,  
    `kCMP_VrefSourceVin2` = `1U` }
- *CMP Voltage Reference source.*

## Driver version

- #define `FSL_CMP_DRIVER_VERSION` (`MAKE_VERSION`(2, 0, 0))  
    *CMP driver version 2.0.0.*

## Initialization

- void `CMP_Init` (`CMP_Type` \*base, const `cmp_config_t` \*config)  
    *Initializes the CMP.*
- void `CMP_Deinit` (`CMP_Type` \*base)  
    *De-initializes the CMP module.*
- static void `CMP_Enable` (`CMP_Type` \*base, bool enable)  
    *Enables/disables the CMP module.*
- void `CMP_GetDefaultConfig` (`cmp_config_t` \*config)  
    *Initializes the CMP user configuration structure.*
- void `CMP_SetInputChannels` (`CMP_Type` \*base, uint8\_t positiveChannel, uint8\_t negativeChannel)  
    *Sets the input channels for the comparator.*

## Advanced Features

- void `CMP_EnableDMA` (`CMP_Type` \*base, bool enable)  
    *Enables/disables the DMA request for rising/falling events.*
- static void `CMP_EnableWindowMode` (`CMP_Type` \*base, bool enable)  
    *Enables/disables the window mode.*
- static void `CMP_EnablePassThroughMode` (`CMP_Type` \*base, bool enable)  
    *Enables/disables the pass through mode.*
- void `CMP_SetFilterConfig` (`CMP_Type` \*base, const `cmp_filter_config_t` \*config)  
    *Configures the filter.*
- void `CMP_SetDACConfig` (`CMP_Type` \*base, const `cmp_dac_config_t` \*config)  
    *Configures the internal DAC.*
- void `CMP_EnableInterrupts` (`CMP_Type` \*base, uint32\_t mask)  
    *Enables the interrupts.*

## Data Structure Documentation

- void [CMP\\_DisableInterrupts](#) (CMP\_Type \*base, uint32\_t mask)  
*Disables the interrupts.*

## Results

- uint32\_t [CMP\\_GetStatusFlags](#) (CMP\_Type \*base)  
*Gets the status flags.*
- void [CMP\\_ClearStatusFlags](#) (CMP\_Type \*base, uint32\_t mask)  
*Clears the status flags.*

## 6.3 Data Structure Documentation

### 6.3.1 struct cmp\_config\_t

#### Data Fields

- bool [enableCmp](#)  
*Enable the CMP module.*
- [cmp\\_hysteresis\\_mode\\_t](#) [hysteresisMode](#)  
*CMP Hysteresis mode.*
- bool [enableHighSpeed](#)  
*Enable High-speed (HS) comparison mode.*
- bool [enableInvertOutput](#)  
*Enable the inverted comparator output.*
- bool [useUnfilteredOutput](#)  
*Set the compare output(COUT) to equal COUTA(true) or COUT(false).*
- bool [enablePinOut](#)  
*The comparator output is available on the associated pin.*
- bool [enableTriggerMode](#)  
*Enable the trigger mode.*

#### 6.3.1.0.0.4 Field Documentation

6.3.1.0.0.4.1 `bool cmp_config_t::enableCmp`

6.3.1.0.0.4.2 `cmp_hysteresis_mode_t cmp_config_t::hysteresisMode`

6.3.1.0.0.4.3 `bool cmp_config_t::enableHighSpeed`

6.3.1.0.0.4.4 `bool cmp_config_t::enableInvertOutput`

6.3.1.0.0.4.5 `bool cmp_config_t::useUnfilteredOutput`

6.3.1.0.0.4.6 `bool cmp_config_t::enablePinOut`

6.3.1.0.0.4.7 `bool cmp_config_t::enableTriggerMode`

#### 6.3.2 struct `cmp_filter_config_t`

##### Data Fields

- `bool enableSample`  
*Using the external SAMPLE as a sampling clock input or using a divided bus clock.*
- `uint8_t filterCount`  
*Filter Sample Count.*
- `uint8_t filterPeriod`  
*Filter Sample Period.*

#### 6.3.2.0.0.5 Field Documentation

6.3.2.0.0.5.1 `bool cmp_filter_config_t::enableSample`

6.3.2.0.0.5.2 `uint8_t cmp_filter_config_t::filterCount`

Available range is 1-7; 0 disables the filter.

6.3.2.0.0.5.3 `uint8_t cmp_filter_config_t::filterPeriod`

The divider to the bus clock. Available range is 0-255.

#### 6.3.3 struct `cmp_dac_config_t`

##### Data Fields

- `cmp_reference_voltage_source_t referenceVoltageSource`  
*Supply voltage reference source.*
- `uint8_t DACValue`  
*Value for the DAC Output Voltage.*

## Enumeration Type Documentation

### 6.3.3.0.0.6 Field Documentation

6.3.3.0.0.6.1 `cmp_reference_voltage_source_t cmp_dac_config_t::referenceVoltageSource`

6.3.3.0.0.6.2 `uint8_t cmp_dac_config_t::DACValue`

Available range is 0-63.

## 6.4 Macro Definition Documentation

6.4.1 `#define FSL_CMP_DRIVER_VERSION (MAKE_VERSION(2, 0, 0))`

## 6.5 Enumeration Type Documentation

### 6.5.1 `enum _cmp_interrupt_enable`

Enumerator

***kCMP\_OutputRisingInterruptEnable*** Comparator interrupt enable rising.

***kCMP\_OutputFallingInterruptEnable*** Comparator interrupt enable falling.

### 6.5.2 `enum _cmp_status_flags`

Enumerator

***kCMP\_OutputRisingEventFlag*** Rising-edge on the comparison output has occurred.

***kCMP\_OutputFallingEventFlag*** Falling-edge on the comparison output has occurred.

***kCMP\_OutputAssertEventFlag*** Return the current value of the analog comparator output.

### 6.5.3 `enum cmp_hysteresis_mode_t`

Enumerator

***kCMP\_HysteresisLevel0*** Hysteresis level 0.

***kCMP\_HysteresisLevel1*** Hysteresis level 1.

***kCMP\_HysteresisLevel2*** Hysteresis level 2.

***kCMP\_HysteresisLevel3*** Hysteresis level 3.

### 6.5.4 `enum cmp_reference_voltage_source_t`

Enumerator

***kCMP\_VrefSourceVin1*** Vin1 is selected as a resistor ladder network supply reference Vin.

***kCMP\_VrefSourceVin2*** Vin2 is selected as a resistor ladder network supply reference Vin.

## 6.6 Function Documentation

### 6.6.1 void CMP\_Init ( CMP\_Type \* *base*, const cmp\_config\_t \* *config* )

This function initializes the CMP module. The operations included are as follows.

- Enabling the clock for CMP module.
- Configuring the comparator.
- Enabling the CMP module. Note that for some devices, multiple CMP instances share the same clock gate. In this case, to enable the clock for any instance enables all CMPs. See the appropriate MCU reference manual for the clock assignment of the CMP.

Parameters

<i>base</i>	CMP peripheral base address.
<i>config</i>	Pointer to the configuration structure.

### 6.6.2 void CMP\_Deinit ( CMP\_Type \* *base* )

This function de-initializes the CMP module. The operations included are as follows.

- Disabling the CMP module.
- Disabling the clock for CMP module.

This function disables the clock for the CMP. Note that for some devices, multiple CMP instances share the same clock gate. In this case, before disabling the clock for the CMP, ensure that all the CMP instances are not used.

Parameters

<i>base</i>	CMP peripheral base address.
-------------	------------------------------

### 6.6.3 static void CMP\_Enable ( CMP\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	CMP peripheral base address.
<i>enable</i>	Enables or disables the module.

## Function Documentation

### 6.6.4 void CMP\_GetDefaultConfig ( cmp\_config\_t \* *config* )

This function initializes the user configuration structure to these default values.

```
* config->enableCmp          = true;
* config->hysteresisMode     = kCMP_HysteresisLevel0;
* config->enableHighSpeed    = false;
* config->enableInvertOutput = false;
* config->useUnfilteredOutput = false;
* config->enablePinOut       = false;
* config->enableTriggerMode  = false;
*
```

#### Parameters

<i>config</i>	Pointer to the configuration structure.
---------------	---

### 6.6.5 void CMP\_SetInputChannels ( CMP\_Type \* *base*, uint8\_t *positiveChannel*, uint8\_t *negativeChannel* )

This function sets the input channels for the comparator. Note that two input channels cannot be set the same way in the application. When the user selects the same input from the analog mux to the positive and negative port, the comparator is disabled automatically.

#### Parameters

<i>base</i>	CMP peripheral base address.
<i>positive-Channel</i>	Positive side input channel number. Available range is 0-7.
<i>negative-Channel</i>	Negative side input channel number. Available range is 0-7.

### 6.6.6 void CMP\_EnableDMA ( CMP\_Type \* *base*, bool *enable* )

This function enables/disables the DMA request for rising/falling events. Either event triggers the generation of the DMA request from CMP if the DMA feature is enabled. Both events are ignored for generating the DMA request from the CMP if the DMA is disabled.

#### Parameters

<i>base</i>	CMP peripheral base address.
<i>enable</i>	Enables or disables the feature.



**6.6.7** `static void CMP_EnableWindowMode ( CMP_Type * base, bool enable )`  
`[inline], [static]`

## Function Documentation

### Parameters

<i>base</i>	CMP peripheral base address.
<i>enable</i>	Enables or disables the feature.

**6.6.8 static void CMP\_EnablePassThroughMode ( CMP\_Type \* *base*, bool *enable* ) [inline], [static]**

### Parameters

<i>base</i>	CMP peripheral base address.
<i>enable</i>	Enables or disables the feature.

**6.6.9 void CMP\_SetFilterConfig ( CMP\_Type \* *base*, const cmp\_filter\_config\_t \* *config* )**

### Parameters

<i>base</i>	CMP peripheral base address.
<i>config</i>	Pointer to the configuration structure.

**6.6.10 void CMP\_SetDACConfig ( CMP\_Type \* *base*, const cmp\_dac\_config\_t \* *config* )**

### Parameters

<i>base</i>	CMP peripheral base address.
<i>config</i>	Pointer to the configuration structure. "NULL" disables the feature.

**6.6.11 void CMP\_EnableInterrupts ( CMP\_Type \* *base*, uint32\_t *mask* )**

## Parameters

<i>base</i>	CMP peripheral base address.
<i>mask</i>	Mask value for interrupts. See "_cmp_interrupt_enable".

**6.6.12 void CMP\_DisableInterrupts ( CMP\_Type \* *base*, uint32\_t *mask* )**

## Parameters

<i>base</i>	CMP peripheral base address.
<i>mask</i>	Mask value for interrupts. See "_cmp_interrupt_enable".

**6.6.13 uint32\_t CMP\_GetStatusFlags ( CMP\_Type \* *base* )**

## Parameters

<i>base</i>	CMP peripheral base address.
-------------	------------------------------

## Returns

Mask value for the asserted flags. See "\_cmp\_status\_flags".

**6.6.14 void CMP\_ClearStatusFlags ( CMP\_Type \* *base*, uint32\_t *mask* )**

## Parameters

<i>base</i>	CMP peripheral base address.
<i>mask</i>	Mask value for the flags. See "_cmp_status_flags".



## Chapter 7

# CMT: Carrier Modulator Transmitter Driver

### 7.1 Overview

The carrier modulator transmitter (CMT) module provides the means to generate the protocol timing and carrier signals for a side variety of encoding schemes. The CMT incorporates hardware to off-load the critical and/or lengthy timing requirements associated with signal generation from the CPU. The KSDK provides a driver for the CMT module of the Kinetis devices.

### 7.2 Clock formulas

The CMT module has internal clock dividers. It was originally designed to be based on an 8 MHz bus clock that can be divided by 1, 2, 4, or 8 according to the specification. To be compatible with a higher bus frequency, the primary prescaler (PPS) was developed to receive a higher frequency and generate a clock enable signal called an intermediate frequency (IF). The IF must be approximately equal to 8 MHz and works as a clock enable to the secondary prescaler. For the PPS, the prescaler is selected according to the bus clock to generate an intermediate clock approximate to 8 MHz and is selected as  $(\text{bus\_clock\_hz}/8000000)$ . The secondary prescaler is the "cmtDivider". The clocks for the CMT module are listed below.

1. CMT clock frequency =  $\text{bus\_clock\_Hz} / (\text{bus\_clock\_Hz} / 8000000) / \text{cmtDivider}$
2. CMT carrier and generator frequency =  $\text{CMT clock frequency} / (\text{highCount1} + \text{lowCount1})$   
(In FSK mode, the second frequency =  $\text{CMT clock frequency} / (\text{highCount2} + \text{lowCount2})$ )
3. CMT infrared output signal frequency
  - a. In Time and Baseband mode  
CMT IRO signal mark time =  $(\text{markCount} + 1) / (\text{CMT clock frequency} / 8)$   
CMT IRO signal space time =  $\text{spaceCount} / (\text{CMT clock frequency} / 8)$
  - b. In FSK mode  
CMT IRO signal mark time =  $(\text{markCount} + 1) / \text{CMT carrier and generator frequency}$   
CMT IRO signal space time =  $\text{spaceCount} / \text{CMT carrier and generator frequency}$

### 7.3 Typical use case

This is an example code to initialize data.

```
cmt_config_t config;
cmt_modulate_config_t modulateConfig;
uint32_t busClock;

// Gets the bus clock for the CMT module.
busClock = CLOCK_GetFreq(kCLOCK_BusClk);

CMT_GetDefaultConfig(&config);

// Interrupts is enabled to change the modulate mark and space count.
config.isInterruptEnabled = true;
```

## Typical use case

```
CMT_Init(CMT, &config, busClock);

// Prepares the modulate configuration for a use case.
modulateConfig.highCount1 = ...;
modulateConfig.lowCount1 = ...;
modulateConfig.markCount = ...;
modulateConfig.spaceCount = ...;

// Sets the time mode.
CMT_SetMode(CMT, kCMT_TimeMode, &modulateConfig);
```

This is an example IRQ handler to change the mark and space count to complete data modulation.

```
// The data length has been transmitted.
uint32_t g_CmtDataBitLen;

void CMT_IRQHandler(void)
{
    if (CMT_GetStatusFlags(CMT))
    {
        if (g_CmtDataBitLen <= CMT_TEST_DATA_BITS)
        {
            // LSB.
            if (data & ((uint32_t)0x01 << g_CmtDataBitLen))
            {
                CMT_SetModulateMarkSpace(CMT, g_CmtModDataOneMarkCount,
                    g_CmtModDataOneSpaceCount);
            }
            else
            {
                CMT_SetModulateMarkSpace(CMT, g_CmtModDataZeroMarkCount,
                    g_CmtModDataZeroSpaceCount);
            }
        }
    }
}
```

## Data Structures

- struct `cmt_modulate_config_t`  
*CMT carrier generator and modulator configuration structure. [More...](#)*
- struct `cmt_config_t`  
*CMT basic configuration structure. [More...](#)*

## Enumerations

- enum `cmt_mode_t` {  
    `kCMT_DirectIROCtl` = 0x00U,  
    `kCMT_TimeMode` = 0x01U,  
    `kCMT_FSKMode` = 0x05U,  
    `kCMT_BasebandMode` = 0x09U }  
*The modes of CMT.*
- enum `cmt_primary_clkdiv_t` {

```

kCMT_PrimaryClkDiv1 = 0U,
kCMT_PrimaryClkDiv2 = 1U,
kCMT_PrimaryClkDiv3 = 2U,
kCMT_PrimaryClkDiv4 = 3U,
kCMT_PrimaryClkDiv5 = 4U,
kCMT_PrimaryClkDiv6 = 5U,
kCMT_PrimaryClkDiv7 = 6U,
kCMT_PrimaryClkDiv8 = 7U,
kCMT_PrimaryClkDiv9 = 8U,
kCMT_PrimaryClkDiv10 = 9U,
kCMT_PrimaryClkDiv11 = 10U,
kCMT_PrimaryClkDiv12 = 11U,
kCMT_PrimaryClkDiv13 = 12U,
kCMT_PrimaryClkDiv14 = 13U,
kCMT_PrimaryClkDiv15 = 14U,
kCMT_PrimaryClkDiv16 = 15U }

```

*The CMT clock divide primary prescaler.*

- enum `cmt_second_clkdiv_t` {  
`kCMT_SecondClkDiv1` = 0U,  
`kCMT_SecondClkDiv2` = 1U,  
`kCMT_SecondClkDiv4` = 2U,  
`kCMT_SecondClkDiv8` = 3U }

*The CMT clock divide secondary prescaler.*

- enum `cmt_infrared_output_polarity_t` {  
`kCMT_IROActiveLow` = 0U,  
`kCMT_IROActiveHigh` = 1U }

*The CMT infrared output polarity.*

- enum `cmt_infrared_output_state_t` {  
`kCMT_IROCtrlLow` = 0U,  
`kCMT_IROCtrlHigh` = 1U }

*The CMT infrared output signal state control.*

- enum `_cmt_interrupt_enable` { `kCMT_EndOfCycleInterruptEnable` = CMT\_MSC\_EOCIE\_MASK  
}

*CMT interrupt configuration structure, default settings all disabled.*

## Driver version

- #define `FSL_CMT_DRIVER_VERSION` (MAKE\_VERSION(2, 0, 1))  
*CMT driver version 2.0.1.*

## Initialization and deinitialization

- void `CMT_GetDefaultConfig` (`cmt_config_t` \*config)  
*Gets the CMT default configuration structure.*
- void `CMT_Init` (CMT\_Type \*base, const `cmt_config_t` \*config, uint32\_t busClock\_Hz)  
*Initializes the CMT module.*
- void `CMT_Deinit` (CMT\_Type \*base)

*Disables the CMT module and gate control.*

### Basic Control Operations

- void [CMT\\_SetMode](#) (CMT\_Type \*base, [cmt\\_mode\\_t](#) mode, [cmt\\_modulate\\_config\\_t](#) \*modulate-Config)  
*Selects the mode for CMT.*
- [cmt\\_mode\\_t](#) [CMT\\_GetMode](#) (CMT\_Type \*base)  
*Gets the mode of the CMT module.*
- uint32\_t [CMT\\_GetCMTFrequency](#) (CMT\_Type \*base, uint32\_t busClock\_Hz)  
*Gets the actual CMT clock frequency.*
- static void [CMT\\_SetCarrirGenerateCountOne](#) (CMT\_Type \*base, uint32\_t highCount, uint32\_t lowCount)  
*Sets the primary data set for the CMT carrier generator counter.*
- static void [CMT\\_SetCarrirGenerateCountTwo](#) (CMT\_Type \*base, uint32\_t highCount, uint32\_t lowCount)  
*Sets the secondary data set for the CMT carrier generator counter.*
- void [CMT\\_SetModulateMarkSpace](#) (CMT\_Type \*base, uint32\_t markCount, uint32\_t spaceCount)  
*Sets the modulation mark and space time period for the CMT modulator.*
- static void [CMT\\_EnableExtendedSpace](#) (CMT\_Type \*base, bool enable)  
*Enables or disables the extended space operation.*
- void [CMT\\_SetIroState](#) (CMT\_Type \*base, [cmt\\_infrared\\_output\\_state\\_t](#) state)  
*Sets the IRO (infrared output) signal state.*
- static void [CMT\\_EnableInterrupts](#) (CMT\_Type \*base, uint32\_t mask)  
*Enables the CMT interrupt.*
- static void [CMT\\_DisableInterrupts](#) (CMT\_Type \*base, uint32\_t mask)  
*Disables the CMT interrupt.*
- static uint32\_t [CMT\\_GetStatusFlags](#) (CMT\_Type \*base)  
*Gets the end of the cycle status flag.*

## 7.4 Data Structure Documentation

### 7.4.1 struct cmt\_modulate\_config\_t

#### Data Fields

- uint8\_t [highCount1](#)  
*The high-time for carrier generator first register.*
- uint8\_t [lowCount1](#)  
*The low-time for carrier generator first register.*
- uint8\_t [highCount2](#)  
*The high-time for carrier generator second register for FSK mode.*
- uint8\_t [lowCount2](#)  
*The low-time for carrier generator second register for FSK mode.*
- uint16\_t [markCount](#)  
*The mark time for the modulator gate.*
- uint16\_t [spaceCount](#)  
*The space time for the modulator gate.*



#### 7.4.1.0.0.7 Field Documentation

7.4.1.0.0.7.1 `uint8_t cmt_modulate_config_t::highCount1`

7.4.1.0.0.7.2 `uint8_t cmt_modulate_config_t::lowCount1`

7.4.1.0.0.7.3 `uint8_t cmt_modulate_config_t::highCount2`

7.4.1.0.0.7.4 `uint8_t cmt_modulate_config_t::lowCount2`

7.4.1.0.0.7.5 `uint16_t cmt_modulate_config_t::markCount`

7.4.1.0.0.7.6 `uint16_t cmt_modulate_config_t::spaceCount`

### 7.4.2 struct `cmt_config_t`

#### Data Fields

- `bool isInterruptEnabled`  
*Timer interrupt 0-disable, 1-enable.*
- `bool isIroEnabled`  
*The IRO output 0-disabled, 1-enabled.*
- `cmt_infrared_output_polarity_t iroPolarity`  
*The IRO polarity.*
- `cmt_second_clkdiv_t divider`  
*The CMT clock divide prescaler.*

#### 7.4.2.0.0.8 Field Documentation

7.4.2.0.0.8.1 `bool cmt_config_t::isInterruptEnabled`

7.4.2.0.0.8.2 `bool cmt_config_t::isIroEnabled`

7.4.2.0.0.8.3 `cmt_infrared_output_polarity_t cmt_config_t::iroPolarity`

7.4.2.0.0.8.4 `cmt_second_clkdiv_t cmt_config_t::divider`

## 7.5 Macro Definition Documentation

7.5.1 `#define FSL_CMT_DRIVER_VERSION (MAKE_VERSION(2, 0, 1))`

## 7.6 Enumeration Type Documentation

### 7.6.1 enum `cmt_mode_t`

Enumerator

***kCMT\_DirectIROCtl*** Carrier modulator is disabled and the IRO signal is directly in software control.

***kCMT\_TimeMode*** Carrier modulator is enabled in time mode.

## Enumeration Type Documentation

***kCMT\_FSKMode*** Carrier modulator is enabled in FSK mode.

***kCMT\_BasebandMode*** Carrier modulator is enabled in baseband mode.

### 7.6.2 enum cmt\_primary\_clkdiv\_t

The primary clock divider is used to divider the bus clock to get the intermediate frequency to approximately equal to 8 MHZ. When the bus clock is 8 MHZ, set primary prescaler to "kCMT\_PrimaryClkDiv1".

Enumerator

<b><i>kCMT_PrimaryClkDiv1</i></b>	The intermediate frequency is the bus clock divided by 1.
<b><i>kCMT_PrimaryClkDiv2</i></b>	The intermediate frequency is the bus clock divided by 2.
<b><i>kCMT_PrimaryClkDiv3</i></b>	The intermediate frequency is the bus clock divided by 3.
<b><i>kCMT_PrimaryClkDiv4</i></b>	The intermediate frequency is the bus clock divided by 4.
<b><i>kCMT_PrimaryClkDiv5</i></b>	The intermediate frequency is the bus clock divided by 5.
<b><i>kCMT_PrimaryClkDiv6</i></b>	The intermediate frequency is the bus clock divided by 6.
<b><i>kCMT_PrimaryClkDiv7</i></b>	The intermediate frequency is the bus clock divided by 7.
<b><i>kCMT_PrimaryClkDiv8</i></b>	The intermediate frequency is the bus clock divided by 8.
<b><i>kCMT_PrimaryClkDiv9</i></b>	The intermediate frequency is the bus clock divided by 9.
<b><i>kCMT_PrimaryClkDiv10</i></b>	The intermediate frequency is the bus clock divided by 10.
<b><i>kCMT_PrimaryClkDiv11</i></b>	The intermediate frequency is the bus clock divided by 11.
<b><i>kCMT_PrimaryClkDiv12</i></b>	The intermediate frequency is the bus clock divided by 12.
<b><i>kCMT_PrimaryClkDiv13</i></b>	The intermediate frequency is the bus clock divided by 13.
<b><i>kCMT_PrimaryClkDiv14</i></b>	The intermediate frequency is the bus clock divided by 14.
<b><i>kCMT_PrimaryClkDiv15</i></b>	The intermediate frequency is the bus clock divided by 15.
<b><i>kCMT_PrimaryClkDiv16</i></b>	The intermediate frequency is the bus clock divided by 16.

### 7.6.3 enum cmt\_second\_clkdiv\_t

The second prescaler can be used to divide the 8 MHZ CMT clock by 1, 2, 4, or 8 according to the specification.

Enumerator

<b><i>kCMT_SecondClkDiv1</i></b>	The CMT clock is the intermediate frequency frequency divided by 1.
<b><i>kCMT_SecondClkDiv2</i></b>	The CMT clock is the intermediate frequency frequency divided by 2.
<b><i>kCMT_SecondClkDiv4</i></b>	The CMT clock is the intermediate frequency frequency divided by 4.
<b><i>kCMT_SecondClkDiv8</i></b>	The CMT clock is the intermediate frequency frequency divided by 8.

### 7.6.4 enum cmt\_infrared\_output\_polarity\_t

Enumerator

***kCMT\_IROActiveLow*** The CMT infrared output signal polarity is active-low.

***kCMT\_IROActiveHigh*** The CMT infrared output signal polarity is active-high.

### 7.6.5 enum cmt\_infrared\_output\_state\_t

Enumerator

***kCMT\_IROCtrlLow*** The CMT Infrared output signal state is controlled to low.

***kCMT\_IROCtrlHigh*** The CMT Infrared output signal state is controlled to high.

### 7.6.6 enum \_cmt\_interrupt\_enable

This structure contains the settings for all of the CMT interrupt configurations.

Enumerator

***kCMT\_EndOfCycleInterruptEnable*** CMT end of cycle interrupt.

## 7.7 Function Documentation

### 7.7.1 void CMT\_GetDefaultConfig ( cmt\_config\_t \* config )

This API gets the default configuration structure for the [CMT\\_Init\(\)](#). Use the initialized structure unchanged in [CMT\\_Init\(\)](#) or modify fields of the structure before calling the [CMT\\_Init\(\)](#).

Parameters

<i>config</i>	The CMT configuration structure pointer.
---------------	--

### 7.7.2 void CMT\_Init ( CMT\_Type \* base, const cmt\_config\_t \* config, uint32\_t busClock\_Hz )

This function ungates the module clock and sets the CMT internal clock, interrupt, and infrared output signal for the CMT module.

## Function Documentation

### Parameters

<i>base</i>	CMT peripheral base address.
<i>config</i>	The CMT basic configuration structure.
<i>busClock_Hz</i>	The CMT module input clock - bus clock frequency.

### 7.7.3 void CMT\_Deinit ( CMT\_Type \* *base* )

This function disables CMT modulator, interrupts, and gates the CMT clock control. CMT\_Init must be called to use the CMT again.

### Parameters

<i>base</i>	CMT peripheral base address.
-------------	------------------------------

### 7.7.4 void CMT\_SetMode ( CMT\_Type \* *base*, cmt\_mode\_t *mode*, cmt\_modulate\_config\_t \* *modulateConfig* )

### Parameters

<i>base</i>	CMT peripheral base address.
<i>mode</i>	The CMT feature mode enumeration. See "cmt_mode_t".
<i>modulate-Config</i>	The carrier generation and modulator configuration.

### 7.7.5 cmt\_mode\_t CMT\_GetMode ( CMT\_Type \* *base* )

### Parameters

<i>base</i>	CMT peripheral base address.
-------------	------------------------------

### Returns

The CMT mode. kCMT\_DirectIROctl Carrier modulator is disabled; the IRO signal is directly in software control. kCMT\_TimeMode Carrier modulator is enabled in time mode. kCMT\_FSKMode Carrier modulator is enabled in FSK mode. kCMT\_BasebandMode Carrier modulator is enabled in baseband mode.

7.7.6 `uint32_t CMT_GetCMTFrequency ( CMT_Type * base, uint32_t busClock_Hz )`

## Function Documentation

### Parameters

<i>base</i>	CMT peripheral base address.
<i>busClock_Hz</i>	CMT module input clock - bus clock frequency.

### Returns

The CMT clock frequency.

### 7.7.7 static void CMT\_SetCarrirGenerateCountOne ( CMT\_Type \* *base*, uint32\_t *highCount*, uint32\_t *lowCount* ) [inline], [static]

This function sets the high-time and low-time of the primary data set for the CMT carrier generator counter to control the period and the duty cycle of the output carrier signal. If the CMT clock period is  $T_{cmt}$ , the period of the carrier generator signal equals  $(highCount + lowCount) * T_{cmt}$ . The duty cycle equals to  $highCount / (highCount + lowCount)$ .

### Parameters

<i>base</i>	CMT peripheral base address.
<i>highCount</i>	The number of CMT clocks for carrier generator signal high time, integer in the range of 1 ~ 0xFF.
<i>lowCount</i>	The number of CMT clocks for carrier generator signal low time, integer in the range of 1 ~ 0xFF.

### 7.7.8 static void CMT\_SetCarrirGenerateCountTwo ( CMT\_Type \* *base*, uint32\_t *highCount*, uint32\_t *lowCount* ) [inline], [static]

This function is used for FSK mode setting the high-time and low-time of the secondary data set CMT carrier generator counter to control the period and the duty cycle of the output carrier signal. If the CMT clock period is  $T_{cmt}$ , the period of the carrier generator signal equals  $(highCount + lowCount) * T_{cmt}$ . The duty cycle equals  $highCount / (highCount + lowCount)$ .

### Parameters

<i>base</i>	CMT peripheral base address.
-------------	------------------------------

<i>highCount</i>	The number of CMT clocks for carrier generator signal high time, integer in the range of 1 ~ 0xFF.
<i>lowCount</i>	The number of CMT clocks for carrier generator signal low time, integer in the range of 1 ~ 0xFF.

### 7.7.9 void CMT\_SetModulateMarkSpace ( CMT\_Type \* *base*, uint32\_t *markCount*, uint32\_t *spaceCount* )

This function sets the mark time period of the CMT modulator counter to control the mark time of the output modulated signal from the carrier generator output signal. If the CMT clock frequency is  $F_{cmt}$  and the carrier out signal frequency is  $f_{cg}$ :

- In Time and Baseband mode: The mark period of the generated signal equals  $(markCount + 1) / (F_{cmt}/8)$ . The space period of the generated signal equals  $spaceCount / (F_{cmt}/8)$ .
- In FSK mode: The mark period of the generated signal equals  $(markCount + 1)/f_{cg}$ . The space period of the generated signal equals  $spaceCount / f_{cg}$ .

Parameters

<i>base</i>	Base address for current CMT instance.
<i>markCount</i>	The number of clock period for CMT modulator signal mark period, in the range of 0 ~ 0xFFFF.
<i>spaceCount</i>	The number of clock period for CMT modulator signal space period, in the range of the 0 ~ 0xFFFF.

### 7.7.10 static void CMT\_EnableExtendedSpace ( CMT\_Type \* *base*, bool *enable* ) [inline], [static]

This function is used to make the space period longer for time, baseband, and FSK modes.

Parameters

<i>base</i>	CMT peripheral base address.
<i>enable</i>	True enable the extended space, false disable the extended space.

---

## Function Documentation

### 7.7.11 void CMT\_SetIroState ( CMT\_Type \* *base*, cmt\_infrared\_output\_state\_t *state* )

Changes the states of the IRO signal when the kCMT\_DirectIROMode mode is set and the IRO signal is enabled.



## Parameters

<i>base</i>	CMT peripheral base address.
<i>state</i>	The control of the IRO signal. See "cmt_infrared_output_state_t"

### 7.7.12 static void CMT\_EnableInterrupts ( CMT\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the CMT interrupts according to the provided mask if enabled. The CMT only has the end of the cycle interrupt - an interrupt occurs at the end of the modulator cycle. This interrupt provides a means for the user to reload the new mark/space values into the CMT modulator data registers and verify the modulator mark and space. For example, to enable the end of cycle, do the following.

```
* CMT_EnableInterrupts(CMT,
* kCMT_EndOfCycleInterruptEnable);
*
```

## Parameters

<i>base</i>	CMT peripheral base address.
<i>mask</i>	The interrupts to enable. Logical OR of <a href="#">_cmt_interrupt_enable</a> .

### 7.7.13 static void CMT\_DisableInterrupts ( CMT\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function disables the CMT interrupts according to the provided maskIf enabled. The CMT only has the end of the cycle interrupt. For example, to disable the end of cycle, do the following.

```
* CMT_DisableInterrupts(CMT,
* kCMT_EndOfCycleInterruptEnable);
*
```

## Parameters

<i>base</i>	CMT peripheral base address.
<i>mask</i>	The interrupts to enable. Logical OR of <a href="#">_cmt_interrupt_enable</a> .

### 7.7.14 static uint32\_t CMT\_GetStatusFlags ( CMT\_Type \* *base* ) [inline], [static]

The flag is set:

## Function Documentation

- When the modulator is not currently active and carrier and modulator are set to start the initial CMT transmission.
- At the end of each modulation cycle when the counter is reloaded and the carrier and modulator are enabled.

Parameters

<i>base</i>	CMT peripheral base address.
-------------	------------------------------

Returns

Current status of the end of cycle status flag

- non-zero: End-of-cycle has occurred.
- zero: End-of-cycle has not yet occurred since the flag last cleared.

## Chapter 8

# CRC: Cyclic Redundancy Check Driver

### 8.1 Overview

The Kinetis SDK provides the Peripheral driver for the Cyclic Redundancy Check (CRC) module of Kinetis devices.

The cyclic redundancy check (CRC) module generates 16/32-bit CRC code for error detection. The CRC module also provides a programmable polynomial, seed, and other parameters required to implement a 16-bit or 32-bit CRC standard.

### 8.2 CRC Driver Initialization and Configuration

[CRC\\_Init\(\)](#) function enables the clock gate for the CRC module in the Kinetis SIM module and fully (re-)configures the CRC module according to the configuration structure. The seed member of the configuration structure is the initial checksum for which new data can be added to. When starting a new checksum computation, the seed is set to the initial checksum per the CRC protocol specification. For continued checksum operation, the seed is set to the intermediate checksum value as obtained from previous calls to [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) function. After calling the [CRC\\_Init\(\)](#), one or multiple [CRC\\_WriteData\(\)](#) calls follow to update the checksum with data and [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) follow to read the result. The `crcResult` member of the configuration structure determines whether the [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) return value is a final checksum or an intermediate checksum. The [CRC\\_Init\(\)](#) function can be called as many times as required allowing for runtime changes of the CRC protocol.

[CRC\\_GetDefaultConfig\(\)](#) function can be used to set the module configuration structure with parameters for CRC-16/CCIT-FALSE protocol.

### 8.3 CRC Write Data

The [CRC\\_WriteData\(\)](#) function adds data to the CRC. Internally, it tries to use 32-bit reads and writes for all aligned data in the user buffer and 8-bit reads and writes for all unaligned data in the user buffer. This function can update the CRC with user-supplied data chunks of an arbitrary size, so one can update the CRC byte by byte or with all bytes at once. Prior to calling the CRC configuration function [CRC\\_Init\(\)](#) fully specifies the CRC module configuration for the [CRC\\_WriteData\(\)](#) call.

### 8.4 CRC Get Checksum

The [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) function reads the CRC module data register. Depending on the prior CRC module usage, the return value is either an intermediate checksum or the final checksum. For example, for 16-bit CRCs the following call sequences can be used.

[CRC\\_Init\(\)](#) / [CRC\\_WriteData\(\)](#) / [CRC\\_Get16bitResult\(\)](#) to get the final checksum.

[CRC\\_Init\(\)](#) / [CRC\\_WriteData\(\)](#) / ... / [CRC\\_WriteData\(\)](#) / [CRC\\_Get16bitResult\(\)](#) to get the final checksum.

## CRC Driver Examples

[CRC\\_Init\(\)](#) / [CRC\\_WriteData\(\)](#) / [CRC\\_Get16bitResult\(\)](#) to get an intermediate checksum.

[CRC\\_Init\(\)](#) / [CRC\\_WriteData\(\)](#) / ... / [CRC\\_WriteData\(\)](#) / [CRC\\_Get16bitResult\(\)](#) to get an intermediate checksum.

### 8.5 Comments about API usage in RTOS

If multiple RTOS tasks share the CRC module to compute checksums with different data and/or protocols, the following needs to be implemented by the user.

The triplets

[CRC\\_Init\(\)](#) / [CRC\\_WriteData\(\)](#) / [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#)

The triplets are protected by the RTOS mutex to protect the CRC module against concurrent accesses from different tasks. This is an example.

```
CRC_Module_RTOS_Mutex_Lock;  
CRC_Init();  
CRC_WriteData();  
CRC_Get16bitResult();  
CRC_Module_RTOS_Mutex_Unlock;
```

### 8.6 Comments about API usage in interrupt handler

All APIs can be used from an interrupt handler although an interrupt latency of equal and lower priority interrupts increases. The user must protect against concurrent accesses from different interrupt handlers and/or tasks.

## 8.7 CRC Driver Examples

### 8.7.1 Simple examples

This is an example with the default CRC-16/CCIT-FALSE protocol.

```
crc_config_t config;  
CRC_Type *base;  
uint8_t data[] = {0x00, 0x01, 0x02, 0x03, 0x04};  
uint16_t checksum;  
  
base = CRC0;  
CRC_GetDefaultConfig(base, &config); /* default gives CRC-16/CCIT-FALSE */  
CRC_Init(base, &config);  
CRC_WriteData(base, data, sizeof(data));  
checksum = CRC_Get16bitResult(base);
```

This is an example with the CRC-32 protocol configuration.

```
crc_config_t config;  
uint32_t checksum;  
  
config.polynomial = 0x04C11DB7u;  
config.seed = 0xFFFFFFFFu;  
config.crcBits = kCrcBits32;  
config.reflectIn = true;
```

```

config.reflectOut = true;
config.complementChecksum = true;
config.crcResult = kCrcFinalChecksum;

CRC_Init(base, &config);
/* example: update by 1 byte at time */
while (dataSize)
{
    uint8_t c = GetCharacter();
    CRC_WriteData(base, &c, 1);
    dataSize--;
}
checksum = CRC_Get32bitResult(base);

```

## 8.7.2 Advanced examples

Assuming there are three tasks/threads, each using the CRC module to compute checksums of a different protocol, with context switches.

First, prepare the three CRC module initialization functions for three different protocols CRC-16 (ARC), CRC-16/CCIT-FALSE, and CRC-32. The table below lists the individual protocol specifications. See also <http://reveng.sourceforge.net/crc-catalogue/>.

	CRC-16/CCIT-FALSE	CRC-16	CRC-32
<b>Width</b>	16 bits	16 bits	32 bits
<b>Polynomial</b>	0x1021	0x8005	0x04C11DB7
<b>Initial seed</b>	0xFFFF	0x0000	0xFFFFFFFF
<b>Complement checksum</b>	No	No	Yes
<b>Reflect In</b>	No	Yes	Yes
<b>Reflect Out</b>	No	Yes	Yes

These are the corresponding initialization functions.

```

void InitCrc16_CCIT(CRC_Type *base, uint32_t seed, bool isLast)
{
    crc_config_t config;

    config.polynomial = 0x1021;
    config.seed = seed;
    config.reflectIn = false;
    config.reflectOut = false;
    config.complementChecksum = false;
    config.crcBits = kCrcBits16;
    config.crcResult = isLast?kCrcFinalChecksum:
        kCrcIntermediateChecksum;

    CRC_Init(base, &config);
}

void InitCrc16(CRC_Type *base, uint32_t seed, bool isLast)
{
    crc_config_t config;

```

## CRC Driver Examples

```
    config.polynomial = 0x8005;
    config.seed = seed;
    config.reflectIn = true;
    config.reflectOut = true;
    config.complementChecksum = false;
    config.crcBits = kCrcBits16;
    config.crcResult = isLast?kCrcFinalChecksum:
        kCrcIntermediateChecksum;

    CRC_Init(base, &config);
}

void InitCrc32(CRC_Type *base, uint32_t seed, bool isLast)
{
    crc_config_t config;

    config.polynomial = 0x04C11DB7U;
    config.seed = seed;
    config.reflectIn = true;
    config.reflectOut = true;
    config.complementChecksum = true;
    config.crcBits = kCrcBits32;
    config.crcResult = isLast?kCrcFinalChecksum:
        kCrcIntermediateChecksum;

    CRC_Init(base, &config);
}
```

The following context switches show a possible API usage.

```
uint16_t checksumCrc16;
uint32_t checksumCrc32;
uint16_t checksumCrc16Ccit;

checksumCrc16 = 0x0;
checksumCrc32 = 0xFFFFFFFFU;
checksumCrc16Ccit = 0xFFFFU;

/* Task A bytes[0-3] */
InitCrc16(base, checksumCrc16, false);
CRC_WriteData(base, &data[0], 4);
checksumCrc16 = CRC_Get16bitResult(base);

/* Task B bytes[0-3] */
InitCrc16_CCIT(base, checksumCrc16Ccit, false);
CRC_WriteData(base, &data[0], 4);
checksumCrc16Ccit = CRC_Get16bitResult(base);

/* Task C 4 bytes[0-3] */
InitCrc32(base, checksumCrc32, false);
CRC_WriteData(base, &data[0], 4);
checksumCrc32 = CRC_Get32bitResult(base);

/* Task B add final 5 bytes[4-8] */
InitCrc16_CCIT(base, checksumCrc16Ccit, true);
CRC_WriteData(base, &data[4], 5);
checksumCrc16Ccit = CRC_Get16bitResult(base);

/* Task C 3 bytes[4-6] */
InitCrc32(base, checksumCrc32, false);
CRC_WriteData(base, &data[4], 3);
checksumCrc32 = CRC_Get32bitResult(base);

/* Task A 3 bytes[4-6] */
InitCrc16(base, checksumCrc16, false);
```

```

CRC_WriteData(base, &data[4], 3);
checksumCrc16 = CRC_Get16bitResult(base);

/* Task C add final 2 bytes[7-8] */
InitCrc32(base, checksumCrc32, true);
CRC_WriteData(base, &data[7], 2);
checksumCrc32 = CRC_Get32bitResult(base);

/* Task A add final 2 bytes[7-8] */
InitCrc16(base, checksumCrc16, true);
CRC_WriteData(base, &data[7], 2);
checksumCrc16 = CRC_Get16bitResult(base);

```

## Data Structures

- struct `crc_config_t`  
CRC protocol configuration. [More...](#)

## Macros

- #define `CRC_DRIVER_USE_CRC16_CCIT_FALSE_AS_DEFAULT` 1  
Default configuration structure filled by `CRC_GetDefaultConfig()`.

## Enumerations

- enum `crc_bits_t` {  
    `kCrcBits16` = 0U,  
    `kCrcBits32` = 1U }  
    CRC bit width.
- enum `crc_result_t` {  
    `kCrcFinalChecksum` = 0U,  
    `kCrcIntermediateChecksum` = 1U }  
    CRC result type.

## Functions

- void `CRC_Init` (CRC\_Type \*base, const `crc_config_t` \*config)  
    Enables and configures the CRC peripheral module.
- static void `CRC_Deinit` (CRC\_Type \*base)  
    Disables the CRC peripheral module.
- void `CRC_GetDefaultConfig` (`crc_config_t` \*config)  
    Loads default values to the CRC protocol configuration structure.
- void `CRC_WriteData` (CRC\_Type \*base, const uint8\_t \*data, size\_t dataSize)  
    Writes data to the CRC module.
- uint32\_t `CRC_Get32bitResult` (CRC\_Type \*base)  
    Reads the 32-bit checksum from the CRC module.
- uint16\_t `CRC_Get16bitResult` (CRC\_Type \*base)  
    Reads a 16-bit checksum from the CRC module.

## Driver version

- #define `FSL_CRC_DRIVER_VERSION` (`MAKE_VERSION`(2, 0, 1))  
    CRC driver version.

## Macro Definition Documentation

## 8.8 Data Structure Documentation

### 8.8.1 struct crc\_config\_t

This structure holds the configuration for the CRC protocol.

#### Data Fields

- uint32\_t [polynomial](#)  
*CRC Polynomial, MSBit first.*
- uint32\_t [seed](#)  
*Starting checksum value.*
- bool [reflectIn](#)  
*Reflect bits on input.*
- bool [reflectOut](#)  
*Reflect bits on output.*
- bool [complementChecksum](#)  
*True if the result shall be complement of the actual checksum.*
- [crc\\_bits\\_t](#) [crcBits](#)  
*Selects 16- or 32- bit CRC protocol.*
- [crc\\_result\\_t](#) [crcResult](#)  
*Selects final or intermediate checksum return from [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#)*

#### 8.8.1.0.0.9 Field Documentation

##### 8.8.1.0.0.9.1 uint32\_t crc\_config\_t::polynomial

Example polynomial: 0x1021 = 1\_0000\_0010\_0001 =  $x^{12} + x^5 + 1$

##### 8.8.1.0.0.9.2 bool crc\_config\_t::reflectIn

##### 8.8.1.0.0.9.3 bool crc\_config\_t::reflectOut

##### 8.8.1.0.0.9.4 bool crc\_config\_t::complementChecksum

##### 8.8.1.0.0.9.5 crc\_bits\_t crc\_config\_t::crcBits

## 8.9 Macro Definition Documentation

### 8.9.1 #define FSL\_CRC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

Version 2.0.1.

Current version: 2.0.1

Change log:

- Version 2.0.1
  - move DATA and DATALL macro definition from header file to source file



### 8.9.2 #define CRC\_DRIVER\_USE\_CRC16\_CCIT\_FALSE\_AS\_DEFAULT 1

Use CRC16-CCIT-FALSE as default.

## 8.10 Enumeration Type Documentation

### 8.10.1 enum crc\_bits\_t

Enumerator

***kCrcBits16*** Generate 16-bit CRC code.

***kCrcBits32*** Generate 32-bit CRC code.

### 8.10.2 enum crc\_result\_t

Enumerator

***kCrcFinalChecksum*** CRC data register read value is the final checksum. Reflect out and final xor protocol features are applied.

***kCrcIntermediateChecksum*** CRC data register read value is intermediate checksum (raw value). Reflect out and final xor protocol feature are not applied. Intermediate checksum can be used as a seed for [CRC\\_Init\(\)](#) to continue adding data to this checksum.

## 8.11 Function Documentation

### 8.11.1 void CRC\_Init ( CRC\_Type \* *base*, const crc\_config\_t \* *config* )

This function enables the clock gate in the Kinetis SIM module for the CRC peripheral. It also configures the CRC module and starts a checksum computation by writing the seed.

Parameters

<i>base</i>	CRC peripheral address.
<i>config</i>	CRC module configuration structure.

### 8.11.2 static void CRC\_Deinit ( CRC\_Type \* *base* ) [inline], [static]

This function disables the clock gate in the Kinetis SIM module for the CRC peripheral.

## Function Documentation

### Parameters

<i>base</i>	CRC peripheral address.
-------------	-------------------------

### 8.11.3 void CRC\_GetDefaultConfig ( crc\_config\_t \* *config* )

Loads default values to the CRC protocol configuration structure. The default values are as follows.

```
* config->polynomial = 0x1021;
* config->seed = 0xFFFF;
* config->reflectIn = false;
* config->reflectOut = false;
* config->complementChecksum = false;
* config->crcBits = kCrcBits16;
* config->crcResult = kCrcFinalChecksum;
*
```

### Parameters

<i>config</i>	CRC protocol configuration structure.
---------------	---------------------------------------

### 8.11.4 void CRC\_WriteData ( CRC\_Type \* *base*, const uint8\_t \* *data*, size\_t *dataSize* )

Writes input data buffer bytes to the CRC data register. The configured type of transpose is applied.

### Parameters

<i>base</i>	CRC peripheral address.
<i>data</i>	Input data stream, MSByte in data[0].
<i>dataSize</i>	Size in bytes of the input data buffer.

### 8.11.5 uint32\_t CRC\_Get32bitResult ( CRC\_Type \* *base* )

Reads the CRC data register (either an intermediate or the final checksum). The configured type of transpose and complement is applied.

## Parameters

<i>base</i>	CRC peripheral address.
-------------	-------------------------

## Returns

An intermediate or the final 32-bit checksum, after configured transpose and complement operations.

**8.11.6 uint16\_t CRC\_Get16bitResult ( CRC\_Type \* *base* )**

Reads the CRC data register (either an intermediate or the final checksum). The configured type of transpose and complement is applied.

## Parameters

<i>base</i>	CRC peripheral address.
-------------	-------------------------

## Returns

An intermediate or the final 16-bit checksum, after configured transpose and complement operations.



## Chapter 9

# DAC: Digital-to-Analog Converter Driver

### 9.1 Overview

The KSDK provides a peripheral driver for the Digital-to-Analog Converter (DAC) module of Kinetis devices.

The DAC driver includes a basic DAC module (converter) and a DAC buffer.

The basic DAC module supports operations unique to the DAC converter in each DAC instance. The APIs in this part are used in the initialization phase, which enables the DAC module in the application. The APIs enable/disable the clock, enable/disable the module, and configure the converter. Call the initial APIs to prepare the DAC module for the application. The DAC buffer operates the DAC hardware buffer. The DAC module supports a hardware buffer to keep a group of DAC values to be converted. This feature supports updating the DAC output value automatically by triggering the buffer read pointer to move in the buffer. Use the APIs to configure the hardware buffer's trigger mode, watermark, work mode, and use size. Additionally, the APIs operate the DMA, interrupts, flags, the pointer (the index of the buffer), item values, and so on.

Note that the most functional features are designed for the DAC hardware buffer.

### 9.2 Typical use case

#### 9.2.1 Working as a basic DAC without the hardware buffer feature

```
// ...

// Configures the DAC.
DAC_GetDefaultConfig(&dacConfigStruct);
DAC_Init(DEMO_DAC_INSTANCE, &dacConfigStruct);
DAC_Enable(DEMO_DAC_INSTANCE, true);
DAC_SetBufferReadPointer(DEMO_DAC_INSTANCE, 0U);

// ...

DAC_SetBufferValue(DEMO_DAC_INSTANCE, 0U, dacValue);
```

#### 9.2.2 Working with the hardware buffer

```
// ...

EnableIRQ(DEMO_DAC_IRQ_ID);

// ...

// Configures the DAC.
DAC_GetDefaultConfig(&dacConfigStruct);
DAC_Init(DEMO_DAC_INSTANCE, &dacConfigStruct);
DAC_Enable(DEMO_DAC_INSTANCE, true);
```

## Typical use case

```
// Configures the DAC buffer.
DAC_GetDefaultBufferConfig(&dacBufferConfigStruct);
DAC_SetBufferConfig(DEMO_DAC_INSTANCE, &dacBufferConfigStruct);
DAC_SetBufferReadPointer(DEMO_DAC_INSTANCE, 0U); // Make sure the read pointer
to the start.
for (index = 0U, dacValue = 0; index < DEMO_DAC_USED_BUFFER_SIZE; index++, dacValue += (0xFFFU /
DEMO_DAC_USED_BUFFER_SIZE))
{
    DAC_SetBufferValue(DEMO_DAC_INSTANCE, index, dacValue);
}
// Clears flags.
#if defined(FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION) && FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION
g_DacBufferWatermarkInterruptFlag = false;
#endif // FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION
g_DacBufferReadPointerTopPositionInterruptFlag = false;
g_DacBufferReadPointerBottomPositionInterruptFlag = false;

// Enables interrupts.
mask = 0U;
#if defined(FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION) && FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION
mask |= kDAC_BufferWatermarkInterruptEnable;
#endif // FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION
mask |= kDAC_BufferReadPointerTopInterruptEnable |
        kDAC_BufferReadPointerBottomInterruptEnable;
DAC_EnableBuffer(DEMO_DAC_INSTANCE, true);
DAC_EnableBufferInterrupts(DEMO_DAC_INSTANCE, mask);

// ISR for the DAC interrupt.
void DEMO_DAC_IRQ_HANDLER_FUNC(void)
{
    uint32_t flags = DAC_GetBufferStatusFlags(DEMO_DAC_INSTANCE);

    #if defined(FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION) && FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION
    if (kDAC_BufferWatermarkFlag == (
        kDAC_BufferWatermarkFlag & flags))
    {
        g_DacBufferWatermarkInterruptFlag = true;
    }
    #endif // FSL_FEATURE_DAC_HAS_WATERMARK_DETECTION
    if (kDAC_BufferReadPointerTopPositionFlag == (
        kDAC_BufferReadPointerTopPositionFlag & flags))
    {
        g_DacBufferReadPointerTopPositionInterruptFlag = true;
    }
    if (kDAC_BufferReadPointerBottomPositionFlag == (
        kDAC_BufferReadPointerBottomPositionFlag & flags))
    {
        g_DacBufferReadPointerBottomPositionInterruptFlag = true;
    }
    DAC_ClearBufferStatusFlags(DEMO_DAC_INSTANCE, flags); /* Clear flags. */
}
```

## Data Structures

- struct [dac\\_config\\_t](#)  
DAC module configuration. [More...](#)
- struct [dac\\_buffer\\_config\\_t](#)  
DAC buffer configuration. [More...](#)

## Enumerations

- enum `_dac_buffer_status_flags` {  
`kDAC_BufferWatermarkFlag` = `DAC_SR_DACBFWMF_MASK`,  
`kDAC_BufferReadPointerTopPositionFlag` = `DAC_SR_DACBFRPTF_MASK`,  
`kDAC_BufferReadPointerBottomPositionFlag` = `DAC_SR_DACBFRPBF_MASK` }  
*DAC buffer flags.*
- enum `_dac_buffer_interrupt_enable` {  
`kDAC_BufferWatermarkInterruptEnable` = `DAC_C0_DACBWIEN_MASK`,  
`kDAC_BufferReadPointerTopInterruptEnable` = `DAC_C0_DACBTIEN_MASK`,  
`kDAC_BufferReadPointerBottomInterruptEnable` = `DAC_C0_DACBBIEN_MASK` }  
*DAC buffer interrupts.*
- enum `dac_reference_voltage_source_t` {  
`kDAC_ReferenceVoltageSourceVref1` = 0U,  
`kDAC_ReferenceVoltageSourceVref2` = 1U }  
*DAC reference voltage source.*
- enum `dac_buffer_trigger_mode_t` {  
`kDAC_BufferTriggerByHardwareMode` = 0U,  
`kDAC_BufferTriggerBySoftwareMode` = 1U }  
*DAC buffer trigger mode.*
- enum `dac_buffer_watermark_t` {  
`kDAC_BufferWatermark1Word` = 0U,  
`kDAC_BufferWatermark2Word` = 1U,  
`kDAC_BufferWatermark3Word` = 2U,  
`kDAC_BufferWatermark4Word` = 3U }  
*DAC buffer watermark.*
- enum `dac_buffer_work_mode_t` {  
`kDAC_BufferWorkAsNormalMode` = 0U,  
`kDAC_BufferWorkAsSwingMode`,  
`kDAC_BufferWorkAsOneTimeScanMode` }  
*DAC buffer work mode.*

## Driver version

- #define `FSL_DAC_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 1)`)  
*DAC driver version 2.0.1.*

## Initialization

- void `DAC_Init` (`DAC_Type *base`, const `dac_config_t *config`)  
*Initializes the DAC module.*
- void `DAC_Deinit` (`DAC_Type *base`)  
*De-initializes the DAC module.*
- void `DAC_GetDefaultConfig` (`dac_config_t *config`)  
*Initializes the DAC user configuration structure.*
- static void `DAC_Enable` (`DAC_Type *base`, bool enable)  
*Enables the DAC module.*

### Buffer

- static void [DAC\\_EnableBuffer](#) (DAC\_Type \*base, bool enable)  
*Enables the DAC buffer.*
- void [DAC\\_SetBufferConfig](#) (DAC\_Type \*base, const [dac\\_buffer\\_config\\_t](#) \*config)  
*Configures the CMP buffer.*
- void [DAC\\_GetDefaultBufferConfig](#) ([dac\\_buffer\\_config\\_t](#) \*config)  
*Initializes the DAC buffer configuration structure.*
- static void [DAC\\_EnableBufferDMA](#) (DAC\_Type \*base, bool enable)  
*Enables the DMA for DAC buffer.*
- void [DAC\\_SetBufferValue](#) (DAC\_Type \*base, uint8\_t index, uint16\_t value)  
*Sets the value for items in the buffer.*
- static void [DAC\\_DoSoftwareTriggerBuffer](#) (DAC\_Type \*base)  
*Triggers the buffer using software and updates the read pointer of the DAC buffer.*
- static uint8\_t [DAC\\_GetBufferReadPointer](#) (DAC\_Type \*base)  
*Gets the current read pointer of the DAC buffer.*
- void [DAC\\_SetBufferReadPointer](#) (DAC\_Type \*base, uint8\_t index)  
*Sets the current read pointer of the DAC buffer.*
- void [DAC\\_EnableBufferInterrupts](#) (DAC\_Type \*base, uint32\_t mask)  
*Enables interrupts for the DAC buffer.*
- void [DAC\\_DisableBufferInterrupts](#) (DAC\_Type \*base, uint32\_t mask)  
*Disables interrupts for the DAC buffer.*
- uint32\_t [DAC\\_GetBufferStatusFlags](#) (DAC\_Type \*base)  
*Gets the flags of events for the DAC buffer.*
- void [DAC\\_ClearBufferStatusFlags](#) (DAC\_Type \*base, uint32\_t mask)  
*Clears the flags of events for the DAC buffer.*

## 9.3 Data Structure Documentation

### 9.3.1 struct [dac\\_config\\_t](#)

#### Data Fields

- [dac\\_reference\\_voltage\\_source\\_t](#) [referenceVoltageSource](#)  
*Select the DAC reference voltage source.*
- bool [enableLowPowerMode](#)  
*Enable the low-power mode.*

#### 9.3.1.0.0.10 Field Documentation

9.3.1.0.0.10.1 [dac\\_reference\\_voltage\\_source\\_t](#) [dac\\_config\\_t::referenceVoltageSource](#)

9.3.1.0.0.10.2 [bool](#) [dac\\_config\\_t::enableLowPowerMode](#)

### 9.3.2 struct [dac\\_buffer\\_config\\_t](#)

#### Data Fields

- [dac\\_buffer\\_trigger\\_mode\\_t](#) [triggerMode](#)  
*Select the buffer's trigger mode.*



- `dac_buffer_watermark_t watermark`  
*Select the buffer's watermark.*
- `dac_buffer_work_mode_t workMode`  
*Select the buffer's work mode.*
- `uint8_t upperLimit`  
*Set the upper limit for the buffer index.*

### 9.3.2.0.0.11 Field Documentation

9.3.2.0.0.11.1 `dac_buffer_trigger_mode_t dac_buffer_config_t::triggerMode`

9.3.2.0.0.11.2 `dac_buffer_watermark_t dac_buffer_config_t::watermark`

9.3.2.0.0.11.3 `dac_buffer_work_mode_t dac_buffer_config_t::workMode`

9.3.2.0.0.11.4 `uint8_t dac_buffer_config_t::upperLimit`

Normally, 0-15 is available for a buffer with 16 items.

## 9.4 Macro Definition Documentation

9.4.1 `#define FSL_DAC_DRIVER_VERSION (MAKE_VERSION(2, 0, 1))`

## 9.5 Enumeration Type Documentation

### 9.5.1 `enum _dac_buffer_status_flags`

Enumerator

***kDAC\_BufferWatermarkFlag*** DAC Buffer Watermark Flag.

***kDAC\_BufferReadPointerTopPositionFlag*** DAC Buffer Read Pointer Top Position Flag.

***kDAC\_BufferReadPointerBottomPositionFlag*** DAC Buffer Read Pointer Bottom Position Flag.

### 9.5.2 `enum _dac_buffer_interrupt_enable`

Enumerator

***kDAC\_BufferWatermarkInterruptEnable*** DAC Buffer Watermark Interrupt Enable.

***kDAC\_BufferReadPointerTopInterruptEnable*** DAC Buffer Read Pointer Top Flag Interrupt Enable.

***kDAC\_BufferReadPointerBottomInterruptEnable*** DAC Buffer Read Pointer Bottom Flag Interrupt Enable.

### 9.5.3 enum dac\_reference\_voltage\_source\_t

Enumerator

*kDAC\_ReferenceVoltageSourceVref1* The DAC selects DACREF\_1 as the reference voltage.

*kDAC\_ReferenceVoltageSourceVref2* The DAC selects DACREF\_2 as the reference voltage.

### 9.5.4 enum dac\_buffer\_trigger\_mode\_t

Enumerator

*kDAC\_BufferTriggerByHardwareMode* The DAC hardware trigger is selected.

*kDAC\_BufferTriggerBySoftwareMode* The DAC software trigger is selected.

### 9.5.5 enum dac\_buffer\_watermark\_t

Enumerator

*kDAC\_BufferWatermark1Word* 1 word away from the upper limit.

*kDAC\_BufferWatermark2Word* 2 words away from the upper limit.

*kDAC\_BufferWatermark3Word* 3 words away from the upper limit.

*kDAC\_BufferWatermark4Word* 4 words away from the upper limit.

### 9.5.6 enum dac\_buffer\_work\_mode\_t

Enumerator

*kDAC\_BufferWorkAsNormalMode* Normal mode.

*kDAC\_BufferWorkAsSwingMode* Swing mode.

*kDAC\_BufferWorkAsOneTimeScanMode* One-Time Scan mode.

## 9.6 Function Documentation

### 9.6.1 void DAC\_Init ( DAC\_Type \* *base*, const dac\_config\_t \* *config* )

This function initializes the DAC module including the following operations.

- Enabling the clock for DAC module.
- Configuring the DAC converter with a user configuration.
- Enabling the DAC module.

## Parameters

<i>base</i>	DAC peripheral base address.
<i>config</i>	Pointer to the configuration structure. See "dac_config_t".

**9.6.2 void DAC\_Deinit ( DAC\_Type \* *base* )**

This function de-initializes the DAC module including the following operations.

- Disabling the DAC module.
- Disabling the clock for the DAC module.

## Parameters

<i>base</i>	DAC peripheral base address.
-------------	------------------------------

**9.6.3 void DAC\_GetDefaultConfig ( dac\_config\_t \* *config* )**

This function initializes the user configuration structure to a default value. The default values are as follows.

```
* config->referenceVoltageSource = kDAC_ReferenceVoltageSourceVref2;
* config->enableLowPowerMode = false;
*
```

## Parameters

<i>config</i>	Pointer to the configuration structure. See "dac_config_t".
---------------	---

**9.6.4 static void DAC\_Enable ( DAC\_Type \* *base*, bool *enable* ) [inline],  
[static]**

## Parameters

<i>base</i>	DAC peripheral base address.
-------------	------------------------------

## Function Documentation

<i>enable</i>	Enables or disables the feature.
---------------	----------------------------------

### 9.6.5 static void DAC\_EnableBuffer ( DAC\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	DAC peripheral base address.
<i>enable</i>	Enables or disables the feature.

### 9.6.6 void DAC\_SetBufferConfig ( DAC\_Type \* *base*, const dac\_buffer\_config\_t \* *config* )

Parameters

<i>base</i>	DAC peripheral base address.
<i>config</i>	Pointer to the configuration structure. See "dac_buffer_config_t".

### 9.6.7 void DAC\_GetDefaultBufferConfig ( dac\_buffer\_config\_t \* *config* )

This function initializes the DAC buffer configuration structure to default values. The default values are as follows.

```
* config->triggerMode = kDAC_BufferTriggerBySoftwareMode;  
* config->watermark   = kDAC_BufferWatermark1Word;  
* config->workMode    = kDAC_BufferWorkAsNormalMode;  
* config->upperLimit  = DAC_DATL_COUNT - 1U;  
*
```

Parameters

<i>config</i>	Pointer to the configuration structure. See "dac_buffer_config_t".
---------------	--

### 9.6.8 static void DAC\_EnableBufferDMA ( DAC\_Type \* *base*, bool *enable* ) [inline], [static]

## Parameters

<i>base</i>	DAC peripheral base address.
<i>enable</i>	Enables or disables the feature.

**9.6.9 void DAC\_SetBufferValue ( DAC\_Type \* *base*, uint8\_t *index*, uint16\_t *value* )**

## Parameters

<i>base</i>	DAC peripheral base address.
<i>index</i>	Setting the index for items in the buffer. The available index should not exceed the size of the DAC buffer.
<i>value</i>	Setting the value for items in the buffer. 12-bits are available.

**9.6.10 static void DAC\_DoSoftwareTriggerBuffer ( DAC\_Type \* *base* ) [inline], [static]**

This function triggers the function using software. The read pointer of the DAC buffer is updated with one step after this function is called. Changing the read pointer depends on the buffer's work mode.

## Parameters

<i>base</i>	DAC peripheral base address.
-------------	------------------------------

**9.6.11 static uint8\_t DAC\_GetBufferReadPointer ( DAC\_Type \* *base* ) [inline], [static]**

This function gets the current read pointer of the DAC buffer. The current output value depends on the item indexed by the read pointer. It is updated either by a software trigger or a hardware trigger.

## Parameters

<i>base</i>	DAC peripheral base address.
-------------	------------------------------

## Returns

The current read pointer of the DAC buffer.

## Function Documentation

### 9.6.12 void DAC\_SetBufferReadPointer ( DAC\_Type \* *base*, uint8\_t *index* )

This function sets the current read pointer of the DAC buffer. The current output value depends on the item indexed by the read pointer. It is updated either by a software trigger or a hardware trigger. After the read pointer changes, the DAC output value also changes.

Parameters

<i>base</i>	DAC peripheral base address.
<i>index</i>	Setting an index value for the pointer.

### 9.6.13 void DAC\_EnableBufferInterrupts ( DAC\_Type \* *base*, uint32\_t *mask* )

Parameters

<i>base</i>	DAC peripheral base address.
<i>mask</i>	Mask value for interrupts. See "_dac_buffer_interrupt_enable".

### 9.6.14 void DAC\_DisableBufferInterrupts ( DAC\_Type \* *base*, uint32\_t *mask* )

Parameters

<i>base</i>	DAC peripheral base address.
<i>mask</i>	Mask value for interrupts. See "_dac_buffer_interrupt_enable".

### 9.6.15 uint32\_t DAC\_GetBufferStatusFlags ( DAC\_Type \* *base* )

Parameters

<i>base</i>	DAC peripheral base address.
-------------	------------------------------

Returns

Mask value for the asserted flags. See "\_dac\_buffer\_status\_flags".

### 9.6.16 void DAC\_ClearBufferStatusFlags ( DAC\_Type \* *base*, uint32\_t *mask* )

## Parameters

<i>base</i>	DAC peripheral base address.
<i>mask</i>	Mask value for flags. See "_dac_buffer_status_flags_t".





## Chapter 10

# DMAMUX: Direct Memory Access Multiplexer Driver

### 10.1 Overview

The KSDK provides a peripheral driver for the Direct Memory Access Multiplexer (DMAMUX) of Kinetis devices.

### 10.2 Typical use case

#### 10.2.1 DMAMUX Operation

```
DMAMUX_Init(DMAMUX0);
DMAMUX_SetSource(DMAMUX0, channel, source);
DMAMUX_EnableChannel(DMAMUX0, channel);
...
DMAMUX_DisableChannel(DMAMUX, channel);
DMAMUX_Deinit(DMAMUX0);
```

#### Driver version

- #define `FSL_DMAMUX_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 2)`)  
*DMAMUX driver version 2.0.2.*

#### DMAMUX Initialization and de-initialization

- void `DMAMUX_Init` (DMAMUX\_Type \*base)  
*Initializes the DMAMUX peripheral.*
- void `DMAMUX_Deinit` (DMAMUX\_Type \*base)  
*Deinitializes the DMAMUX peripheral.*

#### DMAMUX Channel Operation

- static void `DMAMUX_EnableChannel` (DMAMUX\_Type \*base, uint32\_t channel)  
*Enables the DMAMUX channel.*
- static void `DMAMUX_DisableChannel` (DMAMUX\_Type \*base, uint32\_t channel)  
*Disables the DMAMUX channel.*
- static void `DMAMUX_SetSource` (DMAMUX\_Type \*base, uint32\_t channel, uint32\_t source)  
*Configures the DMAMUX channel source.*
- static void `DMAMUX_EnablePeriodTrigger` (DMAMUX\_Type \*base, uint32\_t channel)  
*Enables the DMAMUX period trigger.*
- static void `DMAMUX_DisablePeriodTrigger` (DMAMUX\_Type \*base, uint32\_t channel)  
*Disables the DMAMUX period trigger.*

### 10.3 Macro Definition Documentation

#### 10.3.1 #define `FSL_DMAMUX_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 2)`)

### 10.4 Function Documentation

#### 10.4.1 void DMAMUX\_Init ( DMAMUX\_Type \* *base* )

This function ungates the DMAMUX clock.

## Parameters

<i>base</i>	DMAMUX peripheral base address.
-------------	---------------------------------

**10.4.2 void DMAMUX\_Deinit ( DMAMUX\_Type \* *base* )**

This function gates the DMAMUX clock.

## Parameters

<i>base</i>	DMAMUX peripheral base address.
-------------	---------------------------------

**10.4.3 static void DMAMUX\_EnableChannel ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function enables the DMAMUX channel.

## Parameters

<i>base</i>	DMAMUX peripheral base address.
<i>channel</i>	DMAMUX channel number.

**10.4.4 static void DMAMUX\_DisableChannel ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function disables the DMAMUX channel.

## Note

The user must disable the DMAMUX channel before configuring it.

## Parameters

<i>base</i>	DMAMUX peripheral base address.
-------------	---------------------------------

## Function Documentation

<i>channel</i>	DMAMUX channel number.
----------------	------------------------

**10.4.5 static void DMAMUX\_SetSource ( DMAMUX\_Type \* *base*, uint32\_t *channel*, uint32\_t *source* ) [inline], [static]**

Parameters

<i>base</i>	DMAMUX peripheral base address.
<i>channel</i>	DMAMUX channel number.
<i>source</i>	Channel source, which is used to trigger the DMA transfer.

**10.4.6 static void DMAMUX\_EnablePeriodTrigger ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function enables the DMAMUX period trigger feature.

Parameters

<i>base</i>	DMAMUX peripheral base address.
<i>channel</i>	DMAMUX channel number.

**10.4.7 static void DMAMUX\_DisablePeriodTrigger ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function disables the DMAMUX period trigger.

Parameters

<i>base</i>	DMAMUX peripheral base address.
<i>channel</i>	DMAMUX channel number.



## Chapter 11

### DSPI: Serial Peripheral Interface Driver

#### 11.1 Overview

The KSDK provides a peripheral driver for the Serial Peripheral Interface (SPI) module of Kinetis devices.

#### Modules

- [DSPI DMA Driver](#)
- [DSPI Driver](#)
- [DSPI FreeRTOS Driver](#)
- [DSPI eDMA Driver](#)
- [DSPI  \$\mu\$ COS/II Driver](#)
- [DSPI  \$\mu\$ COS/III Driver](#)

## DSPI Driver

### 11.2 DSPI Driver

#### 11.2.1 Overview

This section describes the programming interface of the DSPI Peripheral driver. The DSPI driver configures the DSPI module and provides the functional and transactional interfaces to build the DSPI application.

#### 11.2.2 Typical use case

##### 11.2.2.1 Master Operation

```
dsppi_master_handle_t g_m_handle; //global variable
dsppi_master_config_t masterConfig;
masterConfig.whichCtar = kDSPI_Ctar0;
masterConfig.ctarConfig.baudRate = baudrate;
masterConfig.ctarConfig.bitsPerFrame = 8;
masterConfig.ctarConfig.cpol = kDSPI_ClockPolarityActiveHigh;
masterConfig.ctarConfig.cpha = kDSPI_ClockPhaseFirstEdge;
masterConfig.ctarConfig.direction = kDSPI_MsbFirst;
masterConfig.ctarConfig.pcsToSckDelayInNanoSec = 1000000000 /
    baudrate ;
masterConfig.ctarConfig.lastSckToPcsDelayInNanoSec = 1000000000 /
    baudrate ;
masterConfig.ctarConfig.betweenTransferDelayInNanoSec = 1000000000 /
    baudrate ;
masterConfig.whichPcs = kDSPI_Pcs0;
masterConfig.pcsActiveHighOrLow = kDSPI_PcsActiveLow;
masterConfig.enableContinuousSCK = false;
masterConfig.enableRxFifoOverWrite = false;
masterConfig.enableModifiedTimingFormat = false;
masterConfig.samplePoint = kDSPI_SckToSin0Clock;
DSPI_MasterInit(base, &masterConfig, srcClock_Hz);

//srcClock_Hz = CLOCK_GetFreq(XXX);
DSPI_MasterInit(base, &masterConfig, srcClock_Hz);

DSPI_MasterTransferCreateHandle(base, &g_m_handle, NULL, NULL);

masterXfer.txData = masterSendBuffer;
masterXfer.rxData = masterReceiveBuffer;
masterXfer.dataSize = transfer_dataSize;
masterXfer.configFlags = kDSPI_MasterCtar0 | kDSPI_MasterPcs0 ;
DSPI_MasterTransferBlocking(base, &g_m_handle, &masterXfer);
```

##### 11.2.2.2 Slave Operation

```
dsppi_slave_handle_t g_s_handle; //global variable
/*Slave config*/
slaveConfig.whichCtar = kDSPI_Ctar0;
slaveConfig.ctarConfig.bitsPerFrame = 8;
slaveConfig.ctarConfig.cpol = kDSPI_ClockPolarityActiveHigh;
slaveConfig.ctarConfig.cpha = kDSPI_ClockPhaseFirstEdge;
```

```

slaveConfig.enableContinuousSCK      = false;
slaveConfig.enableRxFifoOverWrite    = false;
slaveConfig.enableModifiedTimingFormat = false;
slaveConfig.samplePoint              = kDSPI_SckToSin0Clock;
DSPI_SlaveInit(base, &slaveConfig);

slaveXfer.txData      = slaveSendBuffer0;
slaveXfer.rxData      = slaveReceiveBuffer0;
slaveXfer.dataSize    = transfer_dataSize;
slaveXfer.configFlags = kDSPI_SlaveCtar0;

bool isTransferCompleted = false;
DSPI_SlaveTransferCreateHandle(base, &g_s_handle, DSPI_SlaveUserCallback, &
    isTransferCompleted);

DSPI_SlaveTransferNonBlocking(&g_s_handle, &slaveXfer);

//void DSPI_SlaveUserCallback(SPI_Type *base, dspi_slave_handle_t *handle, status_t status, void
//    *isTransferCompleted)
//{
//    if (status == kStatus_Success)
//    {
//        __NOP();
//    }
//    else if (status == kStatus_DSPI_Error)
//    {
//        __NOP();
//    }
//}
//
//*((bool *)isTransferCompleted) = true;
//
//    PRINTF("This is DSPI slave call back . \r\n");
//}

```

## Data Structures

- struct [dspi\\_command\\_data\\_config\\_t](#)  
DSPI master command data configuration used for the SPIx\_PUSHR. [More...](#)
- struct [dspi\\_master\\_ctar\\_config\\_t](#)  
DSPI master ctar configuration structure. [More...](#)
- struct [dspi\\_master\\_config\\_t](#)  
DSPI master configuration structure. [More...](#)
- struct [dspi\\_slave\\_ctar\\_config\\_t](#)  
DSPI slave ctar configuration structure. [More...](#)
- struct [dspi\\_slave\\_config\\_t](#)  
DSPI slave configuration structure. [More...](#)
- struct [dspi\\_transfer\\_t](#)  
DSPI master/slave transfer structure. [More...](#)
- struct [dspi\\_master\\_handle\\_t](#)  
DSPI master transfer handle structure used for transactional API. [More...](#)
- struct [dspi\\_slave\\_handle\\_t](#)  
DSPI slave transfer handle structure used for the transactional API. [More...](#)

## Macros

- #define [DSPI\\_DUMMY\\_DATA](#) (0x00U)

## DSPI Driver

- DSPI dummy data if there is no Tx data.*
- #define [DSPI\\_MASTER\\_CTAR\\_SHIFT](#) (0U)  
*DSPI master CTAR shift macro; used internally.*
- #define [DSPI\\_MASTER\\_CTAR\\_MASK](#) (0x0FU)  
*DSPI master CTAR mask macro; used internally.*
- #define [DSPI\\_MASTER\\_PCS\\_SHIFT](#) (4U)  
*DSPI master PCS shift macro; used internally.*
- #define [DSPI\\_MASTER\\_PCS\\_MASK](#) (0xF0U)  
*DSPI master PCS mask macro; used internally.*
- #define [DSPI\\_SLAVE\\_CTAR\\_SHIFT](#) (0U)  
*DSPI slave CTAR shift macro; used internally.*
- #define [DSPI\\_SLAVE\\_CTAR\\_MASK](#) (0x07U)  
*DSPI slave CTAR mask macro; used internally.*

## Typedefs

- typedef void(\* [dspi\\_master\\_transfer\\_callback\\_t](#) )(SPI\_Type \*base, dspi\_master\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*
- typedef void(\* [dspi\\_slave\\_transfer\\_callback\\_t](#) )(SPI\_Type \*base, dspi\_slave\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*

## Enumerations

- enum [\\_dspi\\_status](#) {  
    [kStatus\\_DSPI\\_Busy](#) = MAKE\_STATUS(kStatusGroup\_DSPI, 0),  
    [kStatus\\_DSPI\\_Error](#) = MAKE\_STATUS(kStatusGroup\_DSPI, 1),  
    [kStatus\\_DSPI\\_Idle](#) = MAKE\_STATUS(kStatusGroup\_DSPI, 2),  
    [kStatus\\_DSPI\\_OutOfRange](#) = MAKE\_STATUS(kStatusGroup\_DSPI, 3) }  
*Status for the DSPI driver.*
- enum [\\_dspi\\_flags](#) {  
    [kDSPI\\_TxCompleteFlag](#) = SPI\_SR\_TCF\_MASK,  
    [kDSPI\\_EndOfQueueFlag](#) = SPI\_SR\_EOQF\_MASK,  
    [kDSPI\\_TxFifoUnderflowFlag](#) = SPI\_SR\_TFUF\_MASK,  
    [kDSPI\\_TxFifoFillRequestFlag](#) = SPI\_SR\_TFFF\_MASK,  
    [kDSPI\\_RxFifoOverflowFlag](#) = SPI\_SR\_RFOF\_MASK,  
    [kDSPI\\_RxFifoDrainRequestFlag](#) = SPI\_SR\_RFDF\_MASK,  
    [kDSPI\\_TxAndRxStatusFlag](#) = SPI\_SR\_TXRXS\_MASK,  
    [kDSPI\\_AllStatusFlag](#) }  
*DSPI status flags in SPIx\_SR register.*
- enum [\\_dspi\\_interrupt\\_enable](#) {



```

kDSPI_TxCompleteInterruptEnable = SPI_RSER_TCF_RE_MASK,
kDSPI_EndOfQueueInterruptEnable = SPI_RSER_EOQF_RE_MASK,
kDSPI_TxFifoUnderflowInterruptEnable = SPI_RSER_TFUF_RE_MASK,
kDSPI_TxFifoFillRequestInterruptEnable = SPI_RSER_TFFF_RE_MASK,
kDSPI_RxFifoOverflowInterruptEnable = SPI_RSER_RFOF_RE_MASK,
kDSPI_RxFifoDrainRequestInterruptEnable = SPI_RSER_RFDF_RE_MASK,
kDSPI_AllInterruptEnable }

```

*DSPI interrupt source.*

- enum `_dspi_dma_enable` {  
`kDSPI_TxDmaEnable` = (SPI\_RSER\_TFFF\_RE\_MASK | SPI\_RSER\_TFFF\_DIRS\_MASK),  
`kDSPI_RxDmaEnable` = (SPI\_RSER\_RFDF\_RE\_MASK | SPI\_RSER\_RFDF\_DIRS\_MASK) }

*DSPI DMA source.*

- enum `dspi_master_slave_mode_t` {  
`kDSPI_Master` = 1U,  
`kDSPI_Slave` = 0U }

*DSPI master or slave mode configuration.*

- enum `dspi_master_sample_point_t` {  
`kDSPI_SckToSin0Clock` = 0U,  
`kDSPI_SckToSin1Clock` = 1U,  
`kDSPI_SckToSin2Clock` = 2U }

*DSPI Sample Point: Controls when the DSPI master samples SIN in the Modified Transfer Format.*

- enum `dspi_which_pcs_t` {  
`kDSPI_Pcs0` = 1U << 0,  
`kDSPI_Pcs1` = 1U << 1,  
`kDSPI_Pcs2` = 1U << 2,  
`kDSPI_Pcs3` = 1U << 3,  
`kDSPI_Pcs4` = 1U << 4,  
`kDSPI_Pcs5` = 1U << 5 }

*DSPI Peripheral Chip Select (Pcs) configuration (which Pcs to configure).*

- enum `dspi_pcs_polarity_config_t` {  
`kDSPI_PcsActiveHigh` = 0U,  
`kDSPI_PcsActiveLow` = 1U }

*DSPI Peripheral Chip Select (Pcs) Polarity configuration.*

- enum `_dspi_pcs_polarity` {  
`kDSPI_Pcs0ActiveLow` = 1U << 0,  
`kDSPI_Pcs1ActiveLow` = 1U << 1,  
`kDSPI_Pcs2ActiveLow` = 1U << 2,  
`kDSPI_Pcs3ActiveLow` = 1U << 3,  
`kDSPI_Pcs4ActiveLow` = 1U << 4,  
`kDSPI_Pcs5ActiveLow` = 1U << 5,  
`kDSPI_PcsAllActiveLow` = 0xFFU }

*DSPI Peripheral Chip Select (Pcs) Polarity.*

- enum `dspi_clock_polarity_t` {  
`kDSPI_ClockPolarityActiveHigh` = 0U,  
`kDSPI_ClockPolarityActiveLow` = 1U }

*DSPI clock polarity configuration for a given CTAR.*

- enum `dspi_clock_phase_t` {

```
kDSPI_ClockPhaseFirstEdge = 0U,  
kDSPI_ClockPhaseSecondEdge = 1U }
```

*DSPI clock phase configuration for a given CTAR.*

- enum `dspi_shift_direction_t` {  
    kDSPI\_MsbFirst = 0U,  
    kDSPI\_LsbFirst = 1U }

*DSPI data shifter direction options for a given CTAR.*

- enum `dspi_delay_type_t` {  
    kDSPI\_PcsToSck = 1U,  
    kDSPI\_LastSckToPcs,  
    kDSPI\_BetweenTransfer }

*DSPI delay type selection.*

- enum `dspi_ctar_selection_t` {  
    kDSPI\_Ctar0 = 0U,  
    kDSPI\_Ctar1 = 1U,  
    kDSPI\_Ctar2 = 2U,  
    kDSPI\_Ctar3 = 3U,  
    kDSPI\_Ctar4 = 4U,  
    kDSPI\_Ctar5 = 5U,  
    kDSPI\_Ctar6 = 6U,  
    kDSPI\_Ctar7 = 7U }

*DSPI Clock and Transfer Attributes Register (CTAR) selection.*

- enum `_dspi_transfer_config_flag_for_master` {  
    kDSPI\_MasterCtar0 = 0U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterCtar1 = 1U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterCtar2 = 2U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterCtar3 = 3U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterCtar4 = 4U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterCtar5 = 5U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterCtar6 = 6U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterCtar7 = 7U << DSPI\_MASTER\_CTAR\_SHIFT,  
    kDSPI\_MasterPcs0 = 0U << DSPI\_MASTER\_PCS\_SHIFT,  
    kDSPI\_MasterPcs1 = 1U << DSPI\_MASTER\_PCS\_SHIFT,  
    kDSPI\_MasterPcs2 = 2U << DSPI\_MASTER\_PCS\_SHIFT,  
    kDSPI\_MasterPcs3 = 3U << DSPI\_MASTER\_PCS\_SHIFT,  
    kDSPI\_MasterPcs4 = 4U << DSPI\_MASTER\_PCS\_SHIFT,  
    kDSPI\_MasterPcs5 = 5U << DSPI\_MASTER\_PCS\_SHIFT,  
    kDSPI\_MasterPcsContinuous = 1U << 20,  
    kDSPI\_MasterActiveAfterTransfer = 1U << 21 }

*Use this enumeration for the DSPI master transfer configFlags.*

- enum `_dspi_transfer_config_flag_for_slave` { kDSPI\_SlaveCtar0 = 0U << DSPI\_SLAVE\_CTAR\_SHIFT }

*Use this enumeration for the DSPI slave transfer configFlags.*

- enum `_dspi_transfer_state` {  
    kDSPI\_Idle = 0x0U,  
    kDSPI\_Busy,

`kDSPI_Error }`

*DSPI transfer state, which is used for DSPI transactional API state machine.*

## Driver version

- #define `FSL_DSPI_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 3)`)  
*DSPI driver version 2.1.3.*

## Initialization and deinitialization

- void `DSPI_MasterInit` (`SPI_Type *base`, const `dspi_master_config_t *masterConfig`, `uint32_t srcClock_Hz`)  
*Initializes the DSPI master.*
- void `DSPI_MasterGetDefaultConfig` (`dspi_master_config_t *masterConfig`)  
*Sets the `dspi_master_config_t` structure to default values.*
- void `DSPI_SlaveInit` (`SPI_Type *base`, const `dspi_slave_config_t *slaveConfig`)  
*DSPI slave configuration.*
- void `DSPI_SlaveGetDefaultConfig` (`dspi_slave_config_t *slaveConfig`)  
*Sets the `dspi_slave_config_t` structure to a default value.*
- void `DSPI_Deinit` (`SPI_Type *base`)  
*De-initializes the DSPI peripheral.*
- static void `DSPI_Enable` (`SPI_Type *base`, bool enable)  
*Enables the DSPI peripheral and sets the MCR MDIS to 0.*

## Status

- static `uint32_t DSPI_GetStatusFlags` (`SPI_Type *base`)  
*Gets the DSPI status flag state.*
- static void `DSPI_ClearStatusFlags` (`SPI_Type *base`, `uint32_t statusFlags`)  
*Clears the DSPI status flag.*

## Interrupts

- void `DSPI_EnableInterrupts` (`SPI_Type *base`, `uint32_t mask`)  
*Enables the DSPI interrupts.*
- static void `DSPI_DisableInterrupts` (`SPI_Type *base`, `uint32_t mask`)  
*Disables the DSPI interrupts.*

## DMA Control

- static void `DSPI_EnableDMA` (`SPI_Type *base`, `uint32_t mask`)  
*Enables the DSPI DMA request.*
- static void `DSPI_DisableDMA` (`SPI_Type *base`, `uint32_t mask`)  
*Disables the DSPI DMA request.*

## DSPI Driver

- static uint32\_t [DSPI\\_MasterGetTxRegisterAddress](#) (SPI\_Type \*base)  
*Gets the DSPI master PUSHR data register address for the DMA operation.*
- static uint32\_t [DSPI\\_SlaveGetTxRegisterAddress](#) (SPI\_Type \*base)  
*Gets the DSPI slave PUSHR data register address for the DMA operation.*
- static uint32\_t [DSPI\\_GetRxRegisterAddress](#) (SPI\_Type \*base)  
*Gets the DSPI POPR data register address for the DMA operation.*

## Bus Operations

- static void [DSPI\\_SetMasterSlaveMode](#) (SPI\_Type \*base, [dspi\\_master\\_slave\\_mode\\_t](#) mode)  
*Configures the DSPI for master or slave.*
- static bool [DSPI\\_IsMaster](#) (SPI\_Type \*base)  
*Returns whether the DSPI module is in master mode.*
- static void [DSPI\\_StartTransfer](#) (SPI\_Type \*base)  
*Starts the DSPI transfers and clears HALT bit in MCR.*
- static void [DSPI\\_StopTransfer](#) (SPI\_Type \*base)  
*Stops DSPI transfers and sets the HALT bit in MCR.*
- static void [DSPI\\_SetFifoEnable](#) (SPI\_Type \*base, bool enableTxFifo, bool enableRxFifo)  
*Enables or disables the DSPI FIFOs.*
- static void [DSPI\\_FlushFifo](#) (SPI\_Type \*base, bool flushTxFifo, bool flushRxFifo)  
*Flushes the DSPI FIFOs.*
- static void [DSPI\\_SetAllPcsPolarity](#) (SPI\_Type \*base, uint32\_t mask)  
*Configures the DSPI peripheral chip select polarity simultaneously.*
- uint32\_t [DSPI\\_MasterSetBaudRate](#) (SPI\_Type \*base, [dspi\\_ctar\\_selection\\_t](#) whichCtar, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Sets the DSPI baud rate in bits per second.*
- void [DSPI\\_MasterSetDelayScaler](#) (SPI\_Type \*base, [dspi\\_ctar\\_selection\\_t](#) whichCtar, uint32\_t prescaler, uint32\_t scaler, [dspi\\_delay\\_type\\_t](#) whichDelay)  
*Manually configures the delay prescaler and scaler for a particular CTAR.*
- uint32\_t [DSPI\\_MasterSetDelayTimes](#) (SPI\_Type \*base, [dspi\\_ctar\\_selection\\_t](#) whichCtar, [dspi\\_delay\\_type\\_t](#) whichDelay, uint32\_t srcClock\_Hz, uint32\_t delayTimeInNanoSec)  
*Calculates the delay prescaler and scaler based on the desired delay input in nanoseconds.*
- static void [DSPI\\_MasterWriteData](#) (SPI\_Type \*base, [dspi\\_command\\_data\\_config\\_t](#) \*command, uint16\_t data)  
*Writes data into the data buffer for master mode.*
- void [DSPI\\_GetDefaultDataCommandConfig](#) ([dspi\\_command\\_data\\_config\\_t](#) \*command)  
*Sets the [dspi\\_command\\_data\\_config\\_t](#) structure to default values.*
- void [DSPI\\_MasterWriteDataBlocking](#) (SPI\_Type \*base, [dspi\\_command\\_data\\_config\\_t](#) \*command, uint16\_t data)  
*Writes data into the data buffer master mode and waits till complete to return.*
- static uint32\_t [DSPI\\_MasterGetFormattedCommand](#) ([dspi\\_command\\_data\\_config\\_t](#) \*command)  
*Returns the DSPI command word formatted to the PUSHR data register bit field.*
- void [DSPI\\_MasterWriteCommandDataBlocking](#) (SPI\_Type \*base, uint32\_t data)  
*Writes a 32-bit data word (16-bit command appended with 16-bit data) into the data buffer master mode and waits till complete to return.*
- static void [DSPI\\_SlaveWriteData](#) (SPI\_Type \*base, uint32\_t data)  
*Writes data into the data buffer in slave mode.*
- void [DSPI\\_SlaveWriteDataBlocking](#) (SPI\_Type \*base, uint32\_t data)  
*Writes data into the data buffer in slave mode, waits till data was transmitted, and returns.*

- static uint32\_t [DSPI\\_ReadData](#) (SPI\_Type \*base)  
*Reads data from the data buffer.*

## Transactional

- void [DSPI\\_MasterTransferCreateHandle](#) (SPI\_Type \*base, dspi\_master\_handle\_t \*handle, [dspi\\_master\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the DSPI master handle.*
- status\_t [DSPI\\_MasterTransferBlocking](#) (SPI\_Type \*base, [dspi\\_transfer\\_t](#) \*transfer)  
*DSPI master transfer data using polling.*
- status\_t [DSPI\\_MasterTransferNonBlocking](#) (SPI\_Type \*base, dspi\_master\_handle\_t \*handle, [dspi\\_transfer\\_t](#) \*transfer)  
*DSPI master transfer data using interrupts.*
- status\_t [DSPI\\_MasterTransferGetCount](#) (SPI\_Type \*base, dspi\_master\_handle\_t \*handle, size\_t \*count)  
*Gets the master transfer count.*
- void [DSPI\\_MasterTransferAbort](#) (SPI\_Type \*base, dspi\_master\_handle\_t \*handle)  
*DSPI master aborts a transfer using an interrupt.*
- void [DSPI\\_MasterTransferHandleIRQ](#) (SPI\_Type \*base, dspi\_master\_handle\_t \*handle)  
*DSPI Master IRQ handler function.*
- void [DSPI\\_SlaveTransferCreateHandle](#) (SPI\_Type \*base, dspi\_slave\_handle\_t \*handle, [dspi\\_slave\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the DSPI slave handle.*
- status\_t [DSPI\\_SlaveTransferNonBlocking](#) (SPI\_Type \*base, dspi\_slave\_handle\_t \*handle, [dspi\\_transfer\\_t](#) \*transfer)  
*DSPI slave transfers data using an interrupt.*
- status\_t [DSPI\\_SlaveTransferGetCount](#) (SPI\_Type \*base, dspi\_slave\_handle\_t \*handle, size\_t \*count)  
*Gets the slave transfer count.*
- void [DSPI\\_SlaveTransferAbort](#) (SPI\_Type \*base, dspi\_slave\_handle\_t \*handle)  
*DSPI slave aborts a transfer using an interrupt.*
- void [DSPI\\_SlaveTransferHandleIRQ](#) (SPI\_Type \*base, dspi\_slave\_handle\_t \*handle)  
*DSPI Master IRQ handler function.*

## 11.2.3 Data Structure Documentation

### 11.2.3.1 struct dspi\_command\_data\_config\_t

#### Data Fields

- bool [isPcsContinuous](#)  
*Option to enable the continuous assertion of the chip select between transfers.*
- [dspi\\_ctar\\_selection\\_t](#) [whichCtar](#)  
*The desired Clock and Transfer Attributes Register (CTAR) to use for CTAS.*
- [dspi\\_which\\_pcs\\_t](#) [whichPcs](#)  
*The desired PCS signal to use for the data transfer.*
- bool [isEndOfQueue](#)

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- Signals that the current transfer is the last in the queue.
- bool [clearTransferCount](#)  
Clears the SPI Transfer Counter (SPI\_TCNT) before transmission starts.

### 11.2.3.1.0.12 Field Documentation

11.2.3.1.0.12.1 bool [dspi\\_command\\_data\\_config\\_t::isPcsContinuous](#)

11.2.3.1.0.12.2 [dspi\\_ctar\\_selection\\_t](#) [dspi\\_command\\_data\\_config\\_t::whichCtar](#)

11.2.3.1.0.12.3 [dspi\\_which\\_pcs\\_t](#) [dspi\\_command\\_data\\_config\\_t::whichPcs](#)

11.2.3.1.0.12.4 bool [dspi\\_command\\_data\\_config\\_t::isEndOfQueue](#)

11.2.3.1.0.12.5 bool [dspi\\_command\\_data\\_config\\_t::clearTransferCount](#)

### 11.2.3.2 struct [dspi\\_master\\_ctar\\_config\\_t](#)

#### Data Fields

- uint32\_t [baudRate](#)  
Baud Rate for DSPI.
- uint32\_t [bitsPerFrame](#)  
Bits per frame, minimum 4, maximum 16.
- [dspi\\_clock\\_polarity\\_t](#) [cpol](#)  
Clock polarity.
- [dspi\\_clock\\_phase\\_t](#) [cpha](#)  
Clock phase.
- [dspi\\_shift\\_direction\\_t](#) [direction](#)  
MSB or LSB data shift direction.
- uint32\_t [pcsToSckDelayInNanoSec](#)  
PCS to SCK delay time in nanoseconds; setting to 0 sets the minimum delay.
- uint32\_t [lastSckToPcsDelayInNanoSec](#)  
The last SCK to PCS delay time in nanoseconds; setting to 0 sets the minimum delay.
- uint32\_t [betweenTransferDelayInNanoSec](#)  
After the SCK delay time in nanoseconds; setting to 0 sets the minimum delay.

### 11.2.3.2.0.13 Field Documentation

11.2.3.2.0.13.1 `uint32_t dspi_master_ctar_config_t::baudRate`

11.2.3.2.0.13.2 `uint32_t dspi_master_ctar_config_t::bitsPerFrame`

11.2.3.2.0.13.3 `dspi_clock_polarity_t dspi_master_ctar_config_t::cpol`

11.2.3.2.0.13.4 `dspi_clock_phase_t dspi_master_ctar_config_t::cpha`

11.2.3.2.0.13.5 `dspi_shift_direction_t dspi_master_ctar_config_t::direction`

11.2.3.2.0.13.6 `uint32_t dspi_master_ctar_config_t::pcsToSckDelayInNanoSec`

It also sets the boundary value if out of range.

11.2.3.2.0.13.7 `uint32_t dspi_master_ctar_config_t::lastSckToPcsDelayInNanoSec`

It also sets the boundary value if out of range.

11.2.3.2.0.13.8 `uint32_t dspi_master_ctar_config_t::betweenTransferDelayInNanoSec`

It also sets the boundary value if out of range.

### 11.2.3.3 struct dspi\_master\_config\_t

#### Data Fields

- [dspi\\_ctar\\_selection\\_t whichCtar](#)  
*The desired CTAR to use.*
- [dspi\\_master\\_ctar\\_config\\_t ctarConfig](#)  
*Set the ctarConfig to the desired CTAR.*
- [dspi\\_which\\_pcs\\_t whichPcs](#)  
*The desired Peripheral Chip Select (pcs).*
- [dspi\\_pcs\\_polarity\\_config\\_t pcsActiveHighOrLow](#)  
*The desired PCS active high or low.*
- `bool enableContinuousSCK`  
*CONT\_SCKE, continuous SCK enable.*
- `bool enableRxFifoOverWrite`  
*ROOE, receive FIFO overflow overwrite enable.*
- `bool enableModifiedTimingFormat`  
*Enables a modified transfer format to be used if true.*
- [dspi\\_master\\_sample\\_point\\_t samplePoint](#)  
*Controls when the module master samples SIN in the Modified Transfer Format.*

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### 11.2.3.3.0.14 Field Documentation

11.2.3.3.0.14.1 `dspi_ctar_selection_t dspi_master_config_t::whichCtar`

11.2.3.3.0.14.2 `dspi_master_ctar_config_t dspi_master_config_t::ctarConfig`

11.2.3.3.0.14.3 `dspi_which_pcs_t dspi_master_config_t::whichPcs`

11.2.3.3.0.14.4 `dspi_pcs_polarity_config_t dspi_master_config_t::pcsActiveHighOrLow`

11.2.3.3.0.14.5 `bool dspi_master_config_t::enableContinuousSCK`

Note that the continuous SCK is only supported for CPHA = 1.

11.2.3.3.0.14.6 `bool dspi_master_config_t::enableRxFifoOverWrite`

If ROOE = 0, the incoming data is ignored and the data from the transfer that generated the overflow is also ignored. If ROOE = 1, the incoming data is shifted to the shift register.

11.2.3.3.0.14.7 `bool dspi_master_config_t::enableModifiedTimingFormat`

11.2.3.3.0.14.8 `dspi_master_sample_point_t dspi_master_config_t::samplePoint`

It's valid only when CPHA=0.

### 11.2.3.4 struct `dspi_slave_ctar_config_t`

#### Data Fields

- `uint32_t bitsPerFrame`  
*Bits per frame, minimum 4, maximum 16.*
- `dspi_clock_polarity_t cpol`  
*Clock polarity.*
- `dspi_clock_phase_t cpha`  
*Clock phase.*

### 11.2.3.4.0.15 Field Documentation

11.2.3.4.0.15.1 `uint32_t dspi_slave_ctar_config_t::bitsPerFrame`

11.2.3.4.0.15.2 `dspi_clock_polarity_t dspi_slave_ctar_config_t::cpol`

11.2.3.4.0.15.3 `dspi_clock_phase_t dspi_slave_ctar_config_t::cpha`

Slave only supports MSB and does not support LSB.



### 11.2.3.5 struct dsp\_slave\_config\_t

#### Data Fields

- [dsp\\_ctar\\_selection\\_t](#) `whichCtar`  
*The desired CTAR to use.*
- [dsp\\_slave\\_ctar\\_config\\_t](#) `ctarConfig`  
*Set the ctarConfig to the desired CTAR.*
- `bool` [enableContinuousSCK](#)  
*CONT\_SCKE, continuous SCK enable.*
- `bool` [enableRxFifoOverWrite](#)  
*ROOE, receive FIFO overflow overwrite enable.*
- `bool` [enableModifiedTimingFormat](#)  
*Enables a modified transfer format to be used if true.*
- [dsp\\_master\\_sample\\_point\\_t](#) `samplePoint`  
*Controls when the module master samples SIN in the Modified Transfer Format.*

#### 11.2.3.5.0.16 Field Documentation

**11.2.3.5.0.16.1 `dsp_ctar_selection_t dsp_slave_config_t::whichCtar`**

**11.2.3.5.0.16.2 `dsp_slave_ctar_config_t dsp_slave_config_t::ctarConfig`**

**11.2.3.5.0.16.3 `bool dsp_slave_config_t::enableContinuousSCK`**

Note that the continuous SCK is only supported for CPHA = 1.

**11.2.3.5.0.16.4 `bool dsp_slave_config_t::enableRxFifoOverWrite`**

If ROOE = 0, the incoming data is ignored and the data from the transfer that generated the overflow is also ignored. If ROOE = 1, the incoming data is shifted to the shift register.

**11.2.3.5.0.16.5 `bool dsp_slave_config_t::enableModifiedTimingFormat`**

**11.2.3.5.0.16.6 `dsp_master_sample_point_t dsp_slave_config_t::samplePoint`**

It's valid only when CPHA=0.

### 11.2.3.6 struct dsp\_transfer\_t

#### Data Fields

- `uint8_t *` [txData](#)  
*Send buffer.*
- `uint8_t *` [rxData](#)  
*Receive buffer.*
- `volatile size_t` [dataSize](#)  
*Transfer bytes.*
- `uint32_t` [configFlags](#)  
*Transfer transfer configuration flags; set from `_dsp_transfer_config_flag_for_master` if the transfer is*

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*used for master or \_dspi\_transfer\_config\_flag\_for\_slave enumeration if the transfer is used for slave.*

### 11.2.3.6.0.17 Field Documentation

**11.2.3.6.0.17.1** `uint8_t* dspi_transfer_t::txData`

**11.2.3.6.0.17.2** `uint8_t* dspi_transfer_t::rxData`

**11.2.3.6.0.17.3** `volatile size_t dspi_transfer_t::dataSize`

**11.2.3.6.0.17.4** `uint32_t dspi_transfer_t::configFlags`

### 11.2.3.7 struct \_dspi\_master\_handle

Forward declaration of the `_dspi_master_handle` typedefs.

### Data Fields

- `uint32_t bitsPerFrame`  
*The desired number of bits per frame.*
- `volatile uint32_t command`  
*The desired data command.*
- `volatile uint32_t lastCommand`  
*The desired last data command.*
- `uint8_t fifoSize`  
*FIFO dataSize.*
- `volatile bool isPcsActiveAfterTransfer`  
*Indicates whether the PCS signal is active after the last frame transfer.*
- `volatile bool isThereExtraByte`  
*Indicates whether there are extra bytes.*
- `uint8_t *volatile txData`  
*Send buffer.*
- `uint8_t *volatile rxData`  
*Receive buffer.*
- `volatile size_t remainingSendByteCount`  
*A number of bytes remaining to send.*
- `volatile size_t remainingReceiveByteCount`  
*A number of bytes remaining to receive.*
- `size_t totalByteCount`  
*A number of transfer bytes.*
- `volatile uint8_t state`  
*DSPI transfer state, see \_dspi\_transfer\_state.*
- `dspi_master_transfer_callback_t callback`  
*Completion callback.*
- `void * userData`  
*Callback user data.*

### 11.2.3.7.0.18 Field Documentation

- 11.2.3.7.0.18.1 `uint32_t dspi_master_handle_t::bitsPerFrame`
  - 11.2.3.7.0.18.2 `volatile uint32_t dspi_master_handle_t::command`
  - 11.2.3.7.0.18.3 `volatile uint32_t dspi_master_handle_t::lastCommand`
  - 11.2.3.7.0.18.4 `uint8_t dspi_master_handle_t::fifoSize`
  - 11.2.3.7.0.18.5 `volatile bool dspi_master_handle_t::isPcsActiveAfterTransfer`
  - 11.2.3.7.0.18.6 `volatile bool dspi_master_handle_t::isThereExtraByte`
  - 11.2.3.7.0.18.7 `uint8_t* volatile dspi_master_handle_t::txData`
  - 11.2.3.7.0.18.8 `uint8_t* volatile dspi_master_handle_t::rxData`
  - 11.2.3.7.0.18.9 `volatile size_t dspi_master_handle_t::remainingSendByteCount`
  - 11.2.3.7.0.18.10 `volatile size_t dspi_master_handle_t::remainingReceiveByteCount`
  - 11.2.3.7.0.18.11 `volatile uint8_t dspi_master_handle_t::state`
  - 11.2.3.7.0.18.12 `dspi_master_transfer_callback_t dspi_master_handle_t::callback`
  - 11.2.3.7.0.18.13 `void* dspi_master_handle_t::userData`
- ### 11.2.3.8 struct \_dspi\_slave\_handle

Forward declaration of the [\\_dspi\\_slave\\_handle](#) typedefs.

### Data Fields

- `uint32_t bitsPerFrame`  
*The desired number of bits per frame.*
- `volatile bool isThereExtraByte`  
*Indicates whether there are extra bytes.*
- `uint8_t *volatile txData`  
*Send buffer.*
- `uint8_t *volatile rxData`  
*Receive buffer.*
- `volatile size_t remainingSendByteCount`  
*A number of bytes remaining to send.*
- `volatile size_t remainingReceiveByteCount`  
*A number of bytes remaining to receive.*
- `size_t totalByteCount`  
*A number of transfer bytes.*
- `volatile uint8_t state`  
*DSPI transfer state.*

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- volatile uint32\_t **errorCount**  
*Error count for slave transfer.*
- **dspi\_slave\_transfer\_callback\_t** callback  
*Completion callback.*
- void \* **userData**  
*Callback user data.*

### 11.2.3.8.0.19 Field Documentation

- 11.2.3.8.0.19.1 **uint32\_t dspi\_slave\_handle\_t::bitsPerFrame**
- 11.2.3.8.0.19.2 **volatile bool dspi\_slave\_handle\_t::isThereExtraByte**
- 11.2.3.8.0.19.3 **uint8\_t\* volatile dspi\_slave\_handle\_t::txData**
- 11.2.3.8.0.19.4 **uint8\_t\* volatile dspi\_slave\_handle\_t::rxData**
- 11.2.3.8.0.19.5 **volatile size\_t dspi\_slave\_handle\_t::remainingSendByteCount**
- 11.2.3.8.0.19.6 **volatile size\_t dspi\_slave\_handle\_t::remainingReceiveByteCount**
- 11.2.3.8.0.19.7 **volatile uint8\_t dspi\_slave\_handle\_t::state**
- 11.2.3.8.0.19.8 **volatile uint32\_t dspi\_slave\_handle\_t::errorCount**
- 11.2.3.8.0.19.9 **dspi\_slave\_transfer\_callback\_t dspi\_slave\_handle\_t::callback**
- 11.2.3.8.0.19.10 **void\* dspi\_slave\_handle\_t::userData**

### 11.2.4 Macro Definition Documentation

11.2.4.1 **#define FSL\_DSPI\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 3))**

11.2.4.2 **#define DSPI\_DUMMY\_DATA (0x00U)**

Dummy data used for Tx if there is no txData.

**11.2.4.3   #define DSPI\_MASTER\_CTAR\_SHIFT (0U)**

**11.2.4.4   #define DSPI\_MASTER\_CTAR\_MASK (0x0FU)**

**11.2.4.5   #define DSPI\_MASTER\_PCS\_SHIFT (4U)**

**11.2.4.6   #define DSPI\_MASTER\_PCS\_MASK (0xF0U)**

**11.2.4.7   #define DSPI\_SLAVE\_CTAR\_SHIFT (0U)**

**11.2.4.8   #define DSPI\_SLAVE\_CTAR\_MASK (0x07U)**

## **11.2.5   Typedef Documentation**

**11.2.5.1   typedef void(\* dspi\_master\_transfer\_callback\_t)(SPI\_Type \*base,  
                  dspi\_master\_handle\_t \*handle, status\_t status, void \*userData)**

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### Parameters

<i>base</i>	DSPI peripheral address.
<i>handle</i>	Pointer to the handle for the DSPI master.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

### 11.2.5.2 typedef void(\* dspi\_slave\_transfer\_callback\_t)(SPI\_Type \*base, dspi\_slave\_handle\_t \*handle, status\_t status, void \*userData)

### Parameters

<i>base</i>	DSPI peripheral address.
<i>handle</i>	Pointer to the handle for the DSPI slave.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

## 11.2.6 Enumeration Type Documentation

### 11.2.6.1 enum \_dspi\_status

#### Enumerator

*kStatus\_DSPI\_Busy* DSPI transfer is busy.  
*kStatus\_DSPI\_Error* DSPI driver error.  
*kStatus\_DSPI\_Idle* DSPI is idle.  
*kStatus\_DSPI\_OutOfRange* DSPI transfer out of range.

### 11.2.6.2 enum \_dspi\_flags

#### Enumerator

*kDSPI\_TxCompleteFlag* Transfer Complete Flag.  
*kDSPI\_EndOfQueueFlag* End of Queue Flag.  
*kDSPI\_TxFifoUnderflowFlag* Transmit FIFO Underflow Flag.  
*kDSPI\_TxFifoFillRequestFlag* Transmit FIFO Fill Flag.  
*kDSPI\_RxFifoOverflowFlag* Receive FIFO Overflow Flag.  
*kDSPI\_RxFifoDrainRequestFlag* Receive FIFO Drain Flag.  
*kDSPI\_TxAndRxStatusFlag* The module is in Stopped/Running state.  
*kDSPI\_AllStatusFlag* All statuses above.

### 11.2.6.3 enum \_dspi\_interrupt\_enable

Enumerator

*kDSPI\_TxCompleteInterruptEnable* TCF interrupt enable.  
*kDSPI\_EndOfQueueInterruptEnable* EOQF interrupt enable.  
*kDSPI\_TxFifoUnderflowInterruptEnable* TFUF interrupt enable.  
*kDSPI\_TxFifoFillRequestInterruptEnable* TFFF interrupt enable, DMA disable.  
*kDSPI\_RxFifoOverflowInterruptEnable* RFOF interrupt enable.  
*kDSPI\_RxFifoDrainRequestInterruptEnable* RFDF interrupt enable, DMA disable.  
*kDSPI\_AllInterruptEnable* All above interrupts enable.

### 11.2.6.4 enum \_dspi\_dma\_enable

Enumerator

*kDSPI\_TxDmaEnable* TFFF flag generates DMA requests. No Tx interrupt request.  
*kDSPI\_RxDmaEnable* RFDF flag generates DMA requests. No Rx interrupt request.

### 11.2.6.5 enum dspi\_master\_slave\_mode\_t

Enumerator

*kDSPI\_Master* DSPI peripheral operates in master mode.  
*kDSPI\_Slave* DSPI peripheral operates in slave mode.

### 11.2.6.6 enum dspi\_master\_sample\_point\_t

This field is valid only when the CPHA bit in the CTAR register is 0.

Enumerator

*kDSPI\_SckToSin0Clock* 0 system clocks between SCK edge and SIN sample.  
*kDSPI\_SckToSin1Clock* 1 system clock between SCK edge and SIN sample.  
*kDSPI\_SckToSin2Clock* 2 system clocks between SCK edge and SIN sample.

### 11.2.6.7 enum dspi\_which\_pcs\_t

Enumerator

*kDSPI\_Pcs0* Pcs[0].  
*kDSPI\_Pcs1* Pcs[1].  
*kDSPI\_Pcs2* Pcs[2].

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*kDSPI\_Pcs3* Pcs[3].  
*kDSPI\_Pcs4* Pcs[4].  
*kDSPI\_Pcs5* Pcs[5].

### 11.2.6.8 enum dspi\_pcs\_polarity\_config\_t

Enumerator

*kDSPI\_PcsActiveHigh* Pcs Active High (idles low).  
*kDSPI\_PcsActiveLow* Pcs Active Low (idles high).

### 11.2.6.9 enum \_dspi\_pcs\_polarity

Enumerator

*kDSPI\_Pcs0ActiveLow* Pcs0 Active Low (idles high).  
*kDSPI\_Pcs1ActiveLow* Pcs1 Active Low (idles high).  
*kDSPI\_Pcs2ActiveLow* Pcs2 Active Low (idles high).  
*kDSPI\_Pcs3ActiveLow* Pcs3 Active Low (idles high).  
*kDSPI\_Pcs4ActiveLow* Pcs4 Active Low (idles high).  
*kDSPI\_Pcs5ActiveLow* Pcs5 Active Low (idles high).  
*kDSPI\_PcsAllActiveLow* Pcs0 to Pcs5 Active Low (idles high).

### 11.2.6.10 enum dspi\_clock\_polarity\_t

Enumerator

*kDSPI\_ClockPolarityActiveHigh* CPOL=0. Active-high DSPI clock (idles low).  
*kDSPI\_ClockPolarityActiveLow* CPOL=1. Active-low DSPI clock (idles high).

### 11.2.6.11 enum dspi\_clock\_phase\_t

Enumerator

*kDSPI\_ClockPhaseFirstEdge* CPHA=0. Data is captured on the leading edge of the SCK and changed on the following edge.  
*kDSPI\_ClockPhaseSecondEdge* CPHA=1. Data is changed on the leading edge of the SCK and captured on the following edge.



### 11.2.6.12 enum dspi\_shift\_direction\_t

Enumerator

***kDSPI\_MsbFirst*** Data transfers start with most significant bit.

***kDSPI\_LsbFirst*** Data transfers start with least significant bit. Shifting out of LSB is not supported for slave

### 11.2.6.13 enum dspi\_delay\_type\_t

Enumerator

***kDSPI\_PcsToSck*** Pcs-to-SCK delay.

***kDSPI\_LastSckToPcs*** The last SCK edge to Pcs delay.

***kDSPI\_BetweenTransfer*** Delay between transfers.

### 11.2.6.14 enum dspi\_ctar\_selection\_t

Enumerator

***kDSPI\_Ctar0*** CTAR0 selection option for master or slave mode; note that CTAR0 and CTAR0\_SLAVE are the same register address.

***kDSPI\_Ctar1*** CTAR1 selection option for master mode only.

***kDSPI\_Ctar2*** CTAR2 selection option for master mode only; note that some devices do not support CTAR2.

***kDSPI\_Ctar3*** CTAR3 selection option for master mode only; note that some devices do not support CTAR3.

***kDSPI\_Ctar4*** CTAR4 selection option for master mode only; note that some devices do not support CTAR4.

***kDSPI\_Ctar5*** CTAR5 selection option for master mode only; note that some devices do not support CTAR5.

***kDSPI\_Ctar6*** CTAR6 selection option for master mode only; note that some devices do not support CTAR6.

***kDSPI\_Ctar7*** CTAR7 selection option for master mode only; note that some devices do not support CTAR7.

### 11.2.6.15 enum \_dspi\_transfer\_config\_flag\_for\_master

Enumerator

***kDSPI\_MasterCtar0*** DSPI master transfer use CTAR0 setting.

***kDSPI\_MasterCtar1*** DSPI master transfer use CTAR1 setting.

***kDSPI\_MasterCtar2*** DSPI master transfer use CTAR2 setting.

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***kDSPI\_MasterCtar3*** DSPI master transfer use CTAR3 setting.  
***kDSPI\_MasterCtar4*** DSPI master transfer use CTAR4 setting.  
***kDSPI\_MasterCtar5*** DSPI master transfer use CTAR5 setting.  
***kDSPI\_MasterCtar6*** DSPI master transfer use CTAR6 setting.  
***kDSPI\_MasterCtar7*** DSPI master transfer use CTAR7 setting.  
***kDSPI\_MasterPcs0*** DSPI master transfer use PCS0 signal.  
***kDSPI\_MasterPcs1*** DSPI master transfer use PCS1 signal.  
***kDSPI\_MasterPcs2*** DSPI master transfer use PCS2 signal.  
***kDSPI\_MasterPcs3*** DSPI master transfer use PCS3 signal.  
***kDSPI\_MasterPcs4*** DSPI master transfer use PCS4 signal.  
***kDSPI\_MasterPcs5*** DSPI master transfer use PCS5 signal.  
***kDSPI\_MasterPcsContinuous*** Indicates whether the PCS signal is continuous.  
***kDSPI\_MasterActiveAfterTransfer*** Indicates whether the PCS signal is active after the last frame transfer.

### 11.2.6.16 enum \_dspi\_transfer\_config\_flag\_for\_slave

Enumerator

***kDSPI\_SlaveCtar0*** DSPI slave transfer use CTAR0 setting. DSPI slave can only use PCS0.

### 11.2.6.17 enum \_dspi\_transfer\_state

Enumerator

***kDSPI\_Idle*** Nothing in the transmitter/receiver.  
***kDSPI\_Busy*** Transfer queue is not finished.  
***kDSPI\_Error*** Transfer error.

## 11.2.7 Function Documentation

### 11.2.7.1 void DSPI\_MasterInit ( SPI\_Type \* base, const dspi\_master\_config\_t \* masterConfig, uint32\_t srcClock\_Hz )

This function initializes the DSPI master configuration. This is an example use case.

```
* dspi_master_config_t masterConfig;  
* masterConfig.whichCtar = kDSPI_Ctar0;  
* masterConfig.ctarConfig.baudRate = 500000000U;  
* masterConfig.ctarConfig.bitsPerFrame = 8;  
* masterConfig.ctarConfig.cpol =  
*   kDSPI_ClockPolarityActiveHigh;  
* masterConfig.ctarConfig.cpha =  
*   kDSPI_ClockPhaseFirstEdge;  
* masterConfig.ctarConfig.direction =
```

```

    kDSPI_MsbFirst;
*   masterConfig.ctarConfig.pcsToSckDelayInNanoSec      = 1000000000U /
    masterConfig.ctarConfig.baudRate ;
*   masterConfig.ctarConfig.lastSckToPcsDelayInNanoSec  = 1000000000U
    / masterConfig.ctarConfig.baudRate ;
*   masterConfig.ctarConfig.betweenTransferDelayInNanoSec =
    1000000000U / masterConfig.ctarConfig.baudRate ;
*   masterConfig.whichPcs                               = kDSPI_Pcs0;
*   masterConfig.pcsActiveHighOrLow                     =
    kDSPI_PcsActiveLow;
*   masterConfig.enableContinuousSCK                   = false;
*   masterConfig.enableRxFifoOverWrite                 = false;
*   masterConfig.enableModifiedTimingFormat            = false;
*   masterConfig.samplePoint                           =
    kDSPI_SckToSin0Clock;
*   DSPI_MasterInit(base, &masterConfig, srcClock_Hz);
*

```

#### Parameters

<i>base</i>	DSPI peripheral address.
<i>masterConfig</i>	Pointer to the structure <a href="#">dspi_master_config_t</a> .
<i>srcClock_Hz</i>	Module source input clock in Hertz.

#### 11.2.7.2 void DSPI\_MasterGetDefaultConfig ( dspi\_master\_config\_t \* *masterConfig* )

The purpose of this API is to get the configuration structure initialized for the [DSPI\\_MasterInit\(\)](#). Users may use the initialized structure unchanged in the [DSPI\\_MasterInit\(\)](#) or modify the structure before calling the [DSPI\\_MasterInit\(\)](#). Example:

```

*   dspi_master_config_t masterConfig;
*   DSPI_MasterGetDefaultConfig(&masterConfig);
*

```

#### Parameters

<i>masterConfig</i>	pointer to <a href="#">dspi_master_config_t</a> structure
---------------------	---

#### 11.2.7.3 void DSPI\_SlaveInit ( SPI\_Type \* *base*, const dspi\_slave\_config\_t \* *slaveConfig* )

This function initializes the DSPI slave configuration. This is an example use case.

```

*   dspi_slave_config_t slaveConfig;
*   slaveConfig->whichCtar          = kDSPI_Ctar0;
*   slaveConfig->ctarConfig.bitsPerFrame = 8;
*   slaveConfig->ctarConfig.cpol      =
    kDSPI_ClockPolarityActiveHigh;
*   slaveConfig->ctarConfig.cpha      =
    kDSPI_ClockPhaseFirstEdge;
*   slaveConfig->enableContinuousSCK = false;

```

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```
* slaveConfig->enableRxFifoOverWrite    = false;
* slaveConfig->enableModifiedTimingFormat = false;
* slaveConfig->samplePoint               = kDSPI_SckToSin0Clock;
*   DSPI_SlaveInit(base, &slaveConfig);
*
```

### Parameters

<i>base</i>	DSPI peripheral address.
<i>slaveConfig</i>	Pointer to the structure <a href="#">dspi_master_config_t</a> .

#### 11.2.7.4 void DSPI\_SlaveGetDefaultConfig ( dspi\_slave\_config\_t \* *slaveConfig* )

The purpose of this API is to get the configuration structure initialized for the [DSPI\\_SlaveInit\(\)](#). Users may use the initialized structure unchanged in the [DSPI\\_SlaveInit\(\)](#) or modify the structure before calling the [DSPI\\_SlaveInit\(\)](#). This is an example.

```
* dspi_slave_config_t slaveConfig;
* DSPI_SlaveGetDefaultConfig(&slaveConfig);
*
```

### Parameters

<i>slaveConfig</i>	Pointer to the <a href="#">dspi_slave_config_t</a> structure.
--------------------	---

#### 11.2.7.5 void DSPI\_Deinit ( SPI\_Type \* *base* )

Call this API to disable the DSPI clock.

### Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

#### 11.2.7.6 static void DSPI\_Enable ( SPI\_Type \* *base*, bool *enable* ) [inline], [static]

### Parameters

---

<i>base</i>	DSPI peripheral address.
<i>enable</i>	Pass true to enable module, false to disable module.

#### 11.2.7.7 static uint32\_t DSPI\_GetStatusFlags ( SPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

Returns

DSPI status (in SR register).

#### 11.2.7.8 static void DSPI\_ClearStatusFlags ( SPI\_Type \* *base*, uint32\_t *statusFlags* ) [inline], [static]

This function clears the desired status bit by using a write-1-to-clear. The user passes in the base and the desired status bit to clear. The list of status bits is defined in the `dspi_status_and_interrupt_request_t`. The function uses these bit positions in its algorithm to clear the desired flag state. This is an example.

```
* DSPI_ClearStatusFlags (base, kDSPI_TxCompleteFlag |
    kDSPI_EndOfQueueFlag);
*
```

Parameters

<i>base</i>	DSPI peripheral address.
<i>statusFlags</i>	The status flag used from the type <code>dspi_flags</code> .

< The status flags are cleared by writing 1 (w1c).

#### 11.2.7.9 void DSPI\_EnableInterrupts ( SPI\_Type \* *base*, uint32\_t *mask* )

This function configures the various interrupt masks of the DSPI. The parameters are a base and an interrupt mask. Note, for Tx Fill and Rx FIFO drain requests, enable the interrupt request and disable the DMA request.

```
* DSPI_EnableInterrupts (base,
    kDSPI_TxCompleteInterruptEnable |
    kDSPI_EndOfQueueInterruptEnable );
*
```

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### Parameters

<i>base</i>	DSPI peripheral address.
<i>mask</i>	The interrupt mask; use the enum <code>_dspi_interrupt_enable</code> .

#### 11.2.7.10 `static void DSPI_DisableInterrupts ( SPI_Type * base, uint32_t mask ) [inline], [static]`

```
* DSPI_DisableInterrupts(base,  
    kDSPI_TxCompleteInterruptEnable |  
    kDSPI_EndOfQueueInterruptEnable );  
*
```

### Parameters

<i>base</i>	DSPI peripheral address.
<i>mask</i>	The interrupt mask; use the enum <code>_dspi_interrupt_enable</code> .

#### 11.2.7.11 `static void DSPI_EnableDMA ( SPI_Type * base, uint32_t mask ) [inline], [static]`

This function configures the Rx and Tx DMA mask of the DSPI. The parameters are a base and a DMA mask.

```
* DSPI_EnableDMA(base, kDSPI_TxDmaEnable |  
    kDSPI_RxDmaEnable);  
*
```

### Parameters

<i>base</i>	DSPI peripheral address.
<i>mask</i>	The interrupt mask; use the enum <code>dspi_dma_enable</code> .

#### 11.2.7.12 `static void DSPI_DisableDMA ( SPI_Type * base, uint32_t mask ) [inline], [static]`

This function configures the Rx and Tx DMA mask of the DSPI. The parameters are a base and a DMA mask.

```
* SPI_DisableDMA(base, kDSPI_TxDmaEnable | kDSPI_RxDmaEnable);  
*
```

## Parameters

<i>base</i>	DSPI peripheral address.
<i>mask</i>	The interrupt mask; use the enum <code>dspi_dma_enable</code> .

#### 11.2.7.13 **static uint32\_t DSPI\_MasterGetTxRegisterAddress ( SPI\_Type \* *base* )** **[inline], [static]**

This function gets the DSPI master PUSHHR data register address because this value is needed for the DMA operation.

## Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

## Returns

The DSPI master PUSHHR data register address.

#### 11.2.7.14 **static uint32\_t DSPI\_SlaveGetTxRegisterAddress ( SPI\_Type \* *base* )** **[inline], [static]**

This function gets the DSPI slave PUSHHR data register address as this value is needed for the DMA operation.

## Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

## Returns

The DSPI slave PUSHHR data register address.

#### 11.2.7.15 **static uint32\_t DSPI\_GetRxRegisterAddress ( SPI\_Type \* *base* )** **[inline],** **[static]**

This function gets the DSPI POPR data register address as this value is needed for the DMA operation.

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### Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

### Returns

The DSPI POPR data register address.

**11.2.7.16 static void DSPI\_SetMasterSlaveMode ( SPI\_Type \* *base*,  
dspi\_master\_slave\_mode\_t *mode* ) [inline], [static]**

### Parameters

<i>base</i>	DSPI peripheral address.
<i>mode</i>	Mode setting (master or slave) of type dspi_master_slave_mode_t.

**11.2.7.17 static bool DSPI\_IsMaster ( SPI\_Type \* *base* ) [inline], [static]**

### Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

### Returns

Returns true if the module is in master mode or false if the module is in slave mode.

**11.2.7.18 static void DSPI\_StartTransfer ( SPI\_Type \* *base* ) [inline], [static]**

This function sets the module to start data transfer in either master or slave mode.

### Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

**11.2.7.19 static void DSPI\_StopTransfer ( SPI\_Type \* *base* ) [inline], [static]**

This function stops data transfers in either master or slave modes.



## Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

#### 11.2.7.20 static void DSPI\_SetFifoEnable ( SPI\_Type \* *base*, bool *enableTxFifo*, bool *enableRxFifo* ) [inline], [static]

This function allows the caller to disable/enable the Tx and Rx FIFOs independently. Note that to disable, pass in a logic 0 (false) for the particular FIFO configuration. To enable, pass in a logic 1 (true).

## Parameters

<i>base</i>	DSPI peripheral address.
<i>enableTxFifo</i>	Disables (false) the TX FIFO; Otherwise, enables (true) the TX FIFO
<i>enableRxFifo</i>	Disables (false) the RX FIFO; Otherwise, enables (true) the RX FIFO

#### 11.2.7.21 static void DSPI\_FlushFifo ( SPI\_Type \* *base*, bool *flushTxFifo*, bool *flushRxFifo* ) [inline], [static]

## Parameters

<i>base</i>	DSPI peripheral address.
<i>flushTxFifo</i>	Flushes (true) the Tx FIFO; Otherwise, does not flush (false) the Tx FIFO
<i>flushRxFifo</i>	Flushes (true) the Rx FIFO; Otherwise, does not flush (false) the Rx FIFO

#### 11.2.7.22 static void DSPI\_SetAllPcsPolarity ( SPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

For example, PCS0 and PCS1 are set to active low and other PCS is set to active high. Note that the number of PCSs is specific to the device.

```
* DSPI_SetAllPcsPolarity(base, kDSPI_Pcs0ActiveLow |
    kDSPI_Pcs1ActiveLow);
```

## Parameters

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<i>base</i>	DSPI peripheral address.
<i>mask</i>	The PCS polarity mask; use the enum <code>_dspi_pcs_polarity</code> .

### 11.2.7.23 `uint32_t DSPI_MasterSetBaudRate ( SPI_Type * base, dspi_ctar_selection_t whichCtar, uint32_t baudRate_Bps, uint32_t srcClock_Hz )`

This function takes in the desired `baudRate_Bps` (baud rate) and calculates the nearest possible baud rate without exceeding the desired baud rate, and returns the calculated baud rate in bits-per-second. It requires that the caller also provide the frequency of the module source clock (in Hertz).

#### Parameters

<i>base</i>	DSPI peripheral address.
<i>whichCtar</i>	The desired Clock and Transfer Attributes Register (CTAR) of the type <code>dspi_ctar_selection_t</code>
<i>baudRate_Bps</i>	The desired baud rate in bits per second
<i>srcClock_Hz</i>	Module source input clock in Hertz

#### Returns

The actual calculated baud rate

### 11.2.7.24 `void DSPI_MasterSetDelayScaler ( SPI_Type * base, dspi_ctar_selection_t whichCtar, uint32_t prescaler, uint32_t scaler, dspi_delay_type_t whichDelay )`

This function configures the PCS to SCK delay pre-scalar (PcsSCK) and scalar (CSSCK), after SCK delay pre-scalar (PASC) and scalar (ASC), and the delay after transfer pre-scalar (PDT) and scalar (DT).

These delay names are available in the type `dspi_delay_type_t`.

The user passes the delay to the configuration along with the prescaler and scaler value. This allows the user to directly set the prescaler/scaler values if pre-calculated or to manually increment either value.

#### Parameters

<i>base</i>	DSPI peripheral address.
<i>whichCtar</i>	The desired Clock and Transfer Attributes Register (CTAR) of type <code>dspi_ctar_selection_t</code> .

<i>prescaler</i>	The prescaler delay value (can be an integer 0, 1, 2, or 3).
<i>scaler</i>	The scaler delay value (can be any integer between 0 to 15).
<i>whichDelay</i>	The desired delay to configure; must be of type <code>dsapi_delay_type_t</code>

#### 11.2.7.25 `uint32_t DSPI_MasterSetDelayTimes ( SPI_Type * base, dsapi_ctar_selection_t whichCtar, dsapi_delay_type_t whichDelay, uint32_t srcClock_Hz, uint32_t delayTimeInNanoSec )`

This function calculates the values for the following. PCS to SCK delay pre-scalar (PCSSCK) and scalar (CSSCK), or After SCK delay pre-scalar (PASC) and scalar (ASC), or Delay after transfer pre-scalar (PDT) and scalar (DT).

These delay names are available in the type `dsapi_delay_type_t`.

The user passes which delay to configure along with the desired delay value in nanoseconds. The function calculates the values needed for the prescaler and scaler. Note that returning the calculated delay as an exact delay match may not be possible. In this case, the closest match is calculated without going below the desired delay value input. It is possible to input a very large delay value that exceeds the capability of the part, in which case the maximum supported delay is returned. The higher-level peripheral driver alerts the user of an out of range delay input.

Parameters

<i>base</i>	DSPI peripheral address.
<i>whichCtar</i>	The desired Clock and Transfer Attributes Register (CTAR) of type <code>dsapi_ctar_selection_t</code> .
<i>whichDelay</i>	The desired delay to configure, must be of type <code>dsapi_delay_type_t</code>
<i>srcClock_Hz</i>	Module source input clock in Hertz
<i>delayTimeInNanoSec</i>	The desired delay value in nanoseconds.

Returns

The actual calculated delay value.

#### 11.2.7.26 `static void DSPI_MasterWriteData ( SPI_Type * base, dsapi_command_data_config_t * command, uint16_t data ) [inline], [static]`

In master mode, the 16-bit data is appended to the 16-bit command info. The command portion provides characteristics of the data, such as the optional continuous chip select operation between transfers, the

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desired Clock and Transfer Attributes register to use for the associated SPI frame, the desired PCS signal to use for the data transfer, whether the current transfer is the last in the queue, and whether to clear the transfer count (normally needed when sending the first frame of a data packet). This is an example.

```
* dspi_command_data_config_t commandConfig;  
* commandConfig.isPcsContinuous = true;  
* commandConfig.whichCtar = kDSPICTar0;  
* commandConfig.whichPcs = kDSPIPcs0;  
* commandConfig.clearTransferCount = false;  
* commandConfig.isEndOfQueue = false;  
* DSPI_MasterWriteData(base, &commandConfig, dataWord);
```

### Parameters

<i>base</i>	DSPI peripheral address.
<i>command</i>	Pointer to the command structure.
<i>data</i>	The data word to be sent.

#### 11.2.7.27 void DSPI\_GetDefaultDataCommandConfig ( dspi\_command\_data\_config\_t \* *command* )

The purpose of this API is to get the configuration structure initialized for use in the DSPI\_MasterWrite\_xx(). Users may use the initialized structure unchanged in the DSPI\_MasterWrite\_xx() or modify the structure before calling the DSPI\_MasterWrite\_xx(). This is an example.

```
* dspi_command_data_config_t command;  
* DSPI_GetDefaultDataCommandConfig(&command);  
*
```

### Parameters

<i>command</i>	Pointer to the <a href="#">dspi_command_data_config_t</a> structure.
----------------	--

#### 11.2.7.28 void DSPI\_MasterWriteDataBlocking ( SPI\_Type \* *base*, dspi\_command\_data\_config\_t \* *command*, uint16\_t *data* )

In master mode, the 16-bit data is appended to the 16-bit command info. The command portion provides characteristics of the data, such as the optional continuous chip select operation between transfers, the desired Clock and Transfer Attributes register to use for the associated SPI frame, the desired PCS signal to use for the data transfer, whether the current transfer is the last in the queue, and whether to clear the transfer count (normally needed when sending the first frame of a data packet). This is an example.

```
* dspi_command_config_t commandConfig;  
* commandConfig.isPcsContinuous = true;  
* commandConfig.whichCtar = kDSPICTar0;
```

```

* commandConfig.whichPcs = kDSPIPCsl;
* commandConfig.clearTransferCount = false;
* commandConfig.isEndOfQueue = false;
* DSPI_MasterWriteDataBlocking(base, &commandConfig, dataWord);
*

```

Note that this function does not return until after the transmit is complete. Also note that the DSPI must be enabled and running to transmit data (MCR[MDIS] & [HALT] = 0). Because the SPI is a synchronous protocol, the received data is available when the transmit completes.

Parameters

<i>base</i>	DSPI peripheral address.
<i>command</i>	Pointer to the command structure.
<i>data</i>	The data word to be sent.

#### 11.2.7.29 static uint32\_t DSPI\_MasterGetFormattedCommand ( dspi\_command\_data\_config\_t \* *command* ) [inline], [static]

This function allows the caller to pass in the data command structure and returns the command word formatted according to the DSPI PUSH register bit field placement. The user can then "OR" the returned command word with the desired data to send and use the function DSPI\_HAL\_WriteCommandDataMastermode or DSPI\_HAL\_WriteCommandDataMastermodeBlocking to write the entire 32-bit command data word to the PUSH register. This helps improve performance in cases where the command structure is constant. For example, the user calls this function before starting a transfer to generate the command word. When they are ready to transmit the data, they OR this formatted command word with the desired data to transmit. This process increases transmit performance when compared to calling send functions, such as DSPI\_HAL\_WriteDataMastermode, which format the command word each time a data word is to be sent.

Parameters

<i>command</i>	Pointer to the command structure.
----------------	-----------------------------------

Returns

The command word formatted to the PUSH register data register bit field.

#### 11.2.7.30 void DSPI\_MasterWriteCommandDataBlocking ( SPI\_Type \* *base*, uint32\_t *data* )

In this function, the user must append the 16-bit data to the 16-bit command information and then provide the total 32-bit word as the data to send. The command portion provides characteristics of the data, such as the optional continuous chip select operation between transfers, the desired Clock and Transfer Attributes

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register to use for the associated SPI frame, the desired PCS signal to use for the data transfer, whether the current transfer is the last in the queue, and whether to clear the transfer count (normally needed when sending the first frame of a data packet). The user is responsible for appending this command with the data to send. This is an example:

```
* dataWord = <16-bit command> | <16-bit data>;  
* DSPI_MasterWriteCommandDataBlocking(base, dataWord);  
*
```

Note that this function does not return until after the transmit is complete. Also note that the DSPI must be enabled and running to transmit data (MCR[MDIS] & [HALT] = 0). Because the SPI is a synchronous protocol, the received data is available when the transmit completes.

For a blocking polling transfer, see methods below. Option 1: uint32\_t command\_to\_send = DSPI\_MasterGetFormattedCommand(&command); uint32\_t data0 = command\_to\_send | data\_need\_to\_send\_0; uint32\_t data1 = command\_to\_send | data\_need\_to\_send\_1; uint32\_t data2 = command\_to\_send | data\_need\_to\_send\_2;

```
DSPI_MasterWriteCommandDataBlocking(base,data0); DSPI_MasterWriteCommandDataBlocking(base,data1);  
DSPI_MasterWriteCommandDataBlocking(base,data2);
```

Option 2: DSPI\_MasterWriteDataBlocking(base,&command,data\_need\_to\_send\_0); DSPI\_MasterWriteDataBlocking(base,&command,data\_need\_to\_send\_1); DSPI\_MasterWriteDataBlocking(base,&command,data\_need\_to\_send\_2);

### Parameters

<i>base</i>	DSPI peripheral address.
<i>data</i>	The data word (command and data combined) to be sent.

### 11.2.7.31 static void DSPI\_SlaveWriteData ( SPI\_Type \* *base*, uint32\_t *data* ) [inline], [static]

In slave mode, up to 16-bit words may be written.

### Parameters

<i>base</i>	DSPI peripheral address.
<i>data</i>	The data to send.

### 11.2.7.32 void DSPI\_SlaveWriteDataBlocking ( SPI\_Type \* *base*, uint32\_t *data* )

In slave mode, up to 16-bit words may be written. The function first clears the transmit complete flag, writes data into data register, and finally waits until the data is transmitted.

## Parameters

<i>base</i>	DSPI peripheral address.
<i>data</i>	The data to send.

**11.2.7.33 static uint32\_t DSPI\_ReadData ( SPI\_Type \* *base* ) [inline], [static]**

## Parameters

<i>base</i>	DSPI peripheral address.
-------------	--------------------------

## Returns

The data from the read data buffer.

**11.2.7.34 void DSPI\_MasterTransferCreateHandle ( SPI\_Type \* *base*, dspimaster\_handle\_t \* *handle*, dspimaster\_transfer\_callback\_t *callback*, void \* *userData* )**

This function initializes the DSPI handle, which can be used for other DSPI transactional APIs. Usually, for a specified DSPI instance, call this API once to get the initialized handle.

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	DSPI handle pointer to dspimaster_handle_t.
<i>callback</i>	DSPI callback.
<i>userData</i>	Callback function parameter.

**11.2.7.35 status\_t DSPI\_MasterTransferBlocking ( SPI\_Type \* *base*, dspitransfer\_t \* *transfer* )**

This function transfers data using polling. This is a blocking function, which does not return until all transfers have been completed.

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### Parameters

<i>base</i>	DSPI peripheral base address.
<i>transfer</i>	Pointer to the <a href="#">dspi_transfer_t</a> structure.

### Returns

status of `status_t`.

#### 11.2.7.36 `status_t DSPI_MasterTransferNonBlocking ( SPI_Type * base, dspi_master_handle_t * handle, dspi_transfer_t * transfer )`

This function transfers data using interrupts. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

### Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the <code>dspi_master_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	Pointer to the <a href="#">dspi_transfer_t</a> structure.

### Returns

status of `status_t`.

#### 11.2.7.37 `status_t DSPI_MasterTransferGetCount ( SPI_Type * base, dspi_master_handle_t * handle, size_t * count )`

This function gets the master transfer count.

### Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the <code>dspi_master_handle_t</code> structure which stores the transfer state.
<i>count</i>	The number of bytes transferred by using the non-blocking transaction.

### Returns

status of `status_t`.



**11.2.7.38** void DSPI\_MasterTransferAbort ( SPI\_Type \* *base*, dspi\_master\_handle\_t \* *handle* )

This function aborts a transfer using an interrupt.

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### Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the <code>dspi_master_handle_t</code> structure which stores the transfer state.

#### 11.2.7.39 void DSPI\_MasterTransferHandleIRQ ( SPI\_Type \* *base*, dspi\_master\_handle\_t \* *handle* )

This function processes the DSPI transmit and receive IRQ.

### Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the <code>dspi_master_handle_t</code> structure which stores the transfer state.

#### 11.2.7.40 void DSPI\_SlaveTransferCreateHandle ( SPI\_Type \* *base*, dspi\_slave\_handle\_t \* *handle*, dspi\_slave\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the DSPI handle, which can be used for other DSPI transactional APIs. Usually, for a specified DSPI instance, call this API once to get the initialized handle.

### Parameters

<i>handle</i>	DSPI handle pointer to the <code>dspi_slave_handle_t</code> .
<i>base</i>	DSPI peripheral base address.
<i>callback</i>	DSPI callback.
<i>userData</i>	Callback function parameter.

#### 11.2.7.41 status\_t DSPI\_SlaveTransferNonBlocking ( SPI\_Type \* *base*, dspi\_slave\_handle\_t \* *handle*, dspi\_transfer\_t \* *transfer* )

This function transfers data using an interrupt. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

### Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the <code>dspi_slave_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	Pointer to the <a href="#">dspi_transfer_t</a> structure.

Returns

status of status\_t.

**11.2.7.42 status\_t DSPI\_SlaveTransferGetCount ( SPI\_Type \* *base*, dspi\_slave\_handle\_t \* *handle*, size\_t \* *count* )**

This function gets the slave transfer count.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the dspi_master_handle_t structure which stores the transfer state.
<i>count</i>	The number of bytes transferred by using the non-blocking transaction.

Returns

status of status\_t.

**11.2.7.43 void DSPI\_SlaveTransferAbort ( SPI\_Type \* *base*, dspi\_slave\_handle\_t \* *handle* )**

This function aborts a transfer using an interrupt.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the dspi_slave_handle_t structure which stores the transfer state.

**11.2.7.44 void DSPI\_SlaveTransferHandleIRQ ( SPI\_Type \* *base*, dspi\_slave\_handle\_t \* *handle* )**

This function processes the DSPI transmit and receive IRQ.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the dspi_slave_handle_t structure which stores the transfer state.

### 11.3 DSPI DMA Driver

#### 11.3.1 Overview

This section describes the programming interface of the DSPI Peripheral driver. The DSPI driver configures DSPI module and provides the functional and transactional interfaces to build the DSPI application.

#### Data Structures

- struct [dspi\\_master\\_dma\\_handle\\_t](#)  
*DSPI master DMA transfer handle structure used for transactional API. [More...](#)*
- struct [dspi\\_slave\\_dma\\_handle\\_t](#)  
*DSPI slave DMA transfer handle structure used for transactional API. [More...](#)*

#### Typedefs

- typedef void(\* [dspi\\_master\\_dma\\_transfer\\_callback\\_t](#))(SPI\_Type \*base, dspi\_master\_dma\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*
- typedef void(\* [dspi\\_slave\\_dma\\_transfer\\_callback\\_t](#))(SPI\_Type \*base, dspi\_slave\_dma\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*

#### Functions

- void [DSPI\\_MasterTransferCreateHandleDMA](#) (SPI\_Type \*base, dspi\_master\_dma\_handle\_t \*handle, [dspi\\_master\\_dma\\_transfer\\_callback\\_t](#) callback, void \*userData, dma\_handle\_t \*dmaRxRegToRxDataHandle, dma\_handle\_t \*dmaTxDataToIntermediaryHandle, dma\_handle\_t \*dmaIntermediaryToTxRegHandle)  
*Initializes the DSPI master DMA handle.*
- status\_t [DSPI\\_MasterTransferDMA](#) (SPI\_Type \*base, dspi\_master\_dma\_handle\_t \*handle, [dspi\\_transfer\\_t](#) \*transfer)  
*DSPI master transfers data using DMA.*
- void [DSPI\\_MasterTransferAbortDMA](#) (SPI\_Type \*base, dspi\_master\_dma\_handle\_t \*handle)  
*DSPI master aborts a transfer which is using DMA.*
- status\_t [DSPI\\_MasterTransferGetCountDMA](#) (SPI\_Type \*base, dspi\_master\_dma\_handle\_t \*handle, size\_t \*count)  
*Gets the master DMA transfer remaining bytes.*
- void [DSPI\\_SlaveTransferCreateHandleDMA](#) (SPI\_Type \*base, dspi\_slave\_dma\_handle\_t \*handle, [dspi\\_slave\\_dma\\_transfer\\_callback\\_t](#) callback, void \*userData, dma\_handle\_t \*dmaRxRegToRxDataHandle, dma\_handle\_t \*dmaTxDataToTxRegHandle)  
*Initializes the DSPI slave DMA handle.*
- status\_t [DSPI\\_SlaveTransferDMA](#) (SPI\_Type \*base, dspi\_slave\_dma\_handle\_t \*handle, [dspi\\_transfer\\_t](#) \*transfer)  
*DSPI slave transfers data using DMA.*

- void [DSPI\\_SlaveTransferAbortDMA](#) (SPI\_Type \*base, dsp\_slave\_dma\_handle\_t \*handle)  
*DSPI slave aborts a transfer which is using DMA.*
- status\_t [DSPI\\_SlaveTransferGetCountDMA](#) (SPI\_Type \*base, dsp\_slave\_dma\_handle\_t \*handle, size\_t \*count)  
*Gets the slave DMA transfer remaining bytes.*

## 11.3.2 Data Structure Documentation

### 11.3.2.1 struct \_dsp\_master\_dma\_handle

Forward declaration of the DSPI DMA master handle typedefs.

#### Data Fields

- uint32\_t [bitsPerFrame](#)  
*The desired number of bits per frame.*
- volatile uint32\_t [command](#)  
*The desired data command.*
- volatile uint32\_t [lastCommand](#)  
*The desired last data command.*
- uint8\_t [fifoSize](#)  
*FIFO dataSize.*
- volatile bool [isPcsActiveAfterTransfer](#)  
*Indicates whether the PCS signal keeps active after the last frame transfer.*
- volatile bool [isThereExtraByte](#)  
*Indicates whether there is an extra byte.*
- uint8\_t \*volatile [txData](#)  
*Send buffer.*
- uint8\_t \*volatile [rxData](#)  
*Receive buffer.*
- volatile size\_t [remainingSendByteCount](#)  
*A number of bytes remaining to send.*
- volatile size\_t [remainingReceiveByteCount](#)  
*A number of bytes remaining to receive.*
- size\_t [totalByteCount](#)  
*A number of transfer bytes.*
- uint32\_t [rxBuffIfNull](#)  
*Used if there is not rxData for DMA purpose.*
- uint32\_t [txBuffIfNull](#)  
*Used if there is not txData for DMA purpose.*
- volatile uint8\_t [state](#)  
*DSPI transfer state, see [\\_dsp\\_transfer\\_state](#).*
- [dsp\\_master\\_dma\\_transfer\\_callback\\_t](#) [callback](#)  
*Completion callback.*
- void \* [userData](#)  
*Callback user data.*
- dma\_handle\_t \* [dmaRxRegToRxDataHandle](#)  
*dma\_handle\_t handle point used for RxReg to RxData buff*

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- `dma_handle_t * dmaTxDataToIntermediaryHandle`  
*dma\_handle\_t handle point used for TxData to Intermediary*
- `dma_handle_t * dmaIntermediaryToTxRegHandle`  
*dma\_handle\_t handle point used for Intermediary to TxReg*

### 11.3.2.1.0.20 Field Documentation

- 11.3.2.1.0.20.1 `uint32_t dspi_master_dma_handle_t::bitsPerFrame`
- 11.3.2.1.0.20.2 `volatile uint32_t dspi_master_dma_handle_t::command`
- 11.3.2.1.0.20.3 `volatile uint32_t dspi_master_dma_handle_t::lastCommand`
- 11.3.2.1.0.20.4 `uint8_t dspi_master_dma_handle_t::fifoSize`
- 11.3.2.1.0.20.5 `volatile bool dspi_master_dma_handle_t::isPcsActiveAfterTransfer`
- 11.3.2.1.0.20.6 `volatile bool dspi_master_dma_handle_t::isThereExtraByte`
- 11.3.2.1.0.20.7 `uint8_t* volatile dspi_master_dma_handle_t::txData`
- 11.3.2.1.0.20.8 `uint8_t* volatile dspi_master_dma_handle_t::rxData`
- 11.3.2.1.0.20.9 `volatile size_t dspi_master_dma_handle_t::remainingSendByteCount`
- 11.3.2.1.0.20.10 `volatile size_t dspi_master_dma_handle_t::remainingReceiveByteCount`
- 11.3.2.1.0.20.11 `uint32_t dspi_master_dma_handle_t::rxBuffIfNull`
- 11.3.2.1.0.20.12 `uint32_t dspi_master_dma_handle_t::txBuffIfNull`
- 11.3.2.1.0.20.13 `volatile uint8_t dspi_master_dma_handle_t::state`
- 11.3.2.1.0.20.14 `dspi_master_dma_transfer_callback_t dspi_master_dma_handle_t::callback`
- 11.3.2.1.0.20.15 `void* dspi_master_dma_handle_t::userData`

### 11.3.2.2 struct \_dspi\_slave\_dma\_handle

Forward declaration of the DSPI DMA slave handle typedefs.

### Data Fields

- `uint32_t bitsPerFrame`  
*Desired number of bits per frame.*
- `volatile bool isThereExtraByte`  
*Indicates whether there is an extra byte.*
- `uint8_t *volatile txData`  
*A send buffer.*
- `uint8_t *volatile rxData`

- *A receive buffer.*
- volatile size\_t [remainingSendByteCount](#)  
*A number of bytes remaining to send.*
- volatile size\_t [remainingReceiveByteCount](#)  
*A number of bytes remaining to receive.*
- size\_t [totalByteCount](#)  
*A number of transfer bytes.*
- uint32\_t [rxBuffIfNull](#)  
*Used if there is not rxData for DMA purpose.*
- uint32\_t [txBuffIfNull](#)  
*Used if there is not txData for DMA purpose.*
- uint32\_t [txLastData](#)  
*Used if there is an extra byte when 16 bits per frame for DMA purpose.*
- volatile uint8\_t [state](#)  
*DSPI transfer state.*
- uint32\_t [errorCount](#)  
*Error count for the slave transfer.*
- [dsp\\_slave\\_dma\\_transfer\\_callback\\_t](#) callback  
*Completion callback.*
- void \* [userData](#)  
*Callback user data.*
- dma\_handle\_t \* [dmaRxRegToRxDataHandle](#)  
*dma\_handle\_t handle point used for RxReg to RxData buff*
- dma\_handle\_t \* [dmaTxDataToTxRegHandle](#)  
*dma\_handle\_t handle point used for TxData to TxReg*

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### 11.3.2.2.0.21 Field Documentation

- 11.3.2.2.0.21.1 `uint32_t dspi_slave_dma_handle_t::bitsPerFrame`
- 11.3.2.2.0.21.2 `volatile bool dspi_slave_dma_handle_t::isThereExtraByte`
- 11.3.2.2.0.21.3 `uint8_t* volatile dspi_slave_dma_handle_t::txData`
- 11.3.2.2.0.21.4 `uint8_t* volatile dspi_slave_dma_handle_t::rxData`
- 11.3.2.2.0.21.5 `volatile size_t dspi_slave_dma_handle_t::remainingSendByteCount`
- 11.3.2.2.0.21.6 `volatile size_t dspi_slave_dma_handle_t::remainingReceiveByteCount`
- 11.3.2.2.0.21.7 `uint32_t dspi_slave_dma_handle_t::rxBuffIfNull`
- 11.3.2.2.0.21.8 `uint32_t dspi_slave_dma_handle_t::txBuffIfNull`
- 11.3.2.2.0.21.9 `uint32_t dspi_slave_dma_handle_t::txLastData`
- 11.3.2.2.0.21.10 `volatile uint8_t dspi_slave_dma_handle_t::state`
- 11.3.2.2.0.21.11 `uint32_t dspi_slave_dma_handle_t::errorCount`
- 11.3.2.2.0.21.12 `dspi_slave_dma_transfer_callback_t dspi_slave_dma_handle_t::callback`
- 11.3.2.2.0.21.13 `void* dspi_slave_dma_handle_t::userData`

### 11.3.3 Typedef Documentation

- 11.3.3.1 `typedef void(* dspi_master_dma_transfer_callback_t)(SPI_Type *base, dspi_master_dma_handle_t *handle, status_t status, void *userData)`



## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the handle for the DSPI master.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

### 11.3.3.2 typedef void(\* dspi\_slave\_dma\_transfer\_callback\_t)(SPI\_Type \*base, dspi\_slave\_dma\_handle\_t \*handle, status\_t status, void \*userData)

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	Pointer to the handle for the DSPI slave.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

## 11.3.4 Function Documentation

### 11.3.4.1 void DSPI\_MasterTransferCreateHandleDMA ( SPI\_Type \* base, dspi\_master\_dma\_handle\_t \* handle, dspi\_master\_dma\_transfer\_callback\_t callback, void \* userData, dma\_handle\_t \* dmaRxRegToRxDataHandle, dma\_handle\_t \* dmaTxDataToIntermediaryHandle, dma\_handle\_t \* dmaIntermediaryToTxRegHandle )

This function initializes the DSPI DMA handle which can be used for other DSPI transactional APIs. Usually, for a specified DSPI instance, call this API once to get the initialized handle.

Note that DSPI DMA has a separated (Rx and Tx as two sources) or shared (Rx and Tx is the same source) DMA request source. (1) For a separated DMA request source, enable and set the Rx DMAMUX source for dmaRxRegToRxDataHandle and Tx DMAMUX source for dmaIntermediaryToTxRegHandle. (2) For a shared DMA request source, enable and set the Rx/Rx DMAMUX source for dmaRxRegToRxDataHandle.

## Parameters

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<i>base</i>	DSPI peripheral base address.
<i>handle</i>	DSPI handle pointer to <code>dspi_master_dma_handle_t</code> .
<i>callback</i>	DSPI callback.
<i>userData</i>	A callback function parameter.
<i>dmaRxRegTo-RxDataHandle</i>	<code>dmaRxRegToRxDataHandle</code> pointer to <code>dma_handle_t</code> .
<i>dmaTxDataTo-Intermediary-Handle</i>	<code>dmaTxDataToIntermediaryHandle</code> pointer to <code>dma_handle_t</code> .
<i>dma-Intermediary-ToTxReg-Handle</i>	<code>dmaIntermediaryToTxRegHandle</code> pointer to <code>dma_handle_t</code> .

### 11.3.4.2 **status\_t DSPI\_MasterTransferDMA ( SPI\_Type \* *base*, dspi\_master\_dma\_handle\_t \* *handle*, dspi\_transfer\_t \* *transfer* )**

This function transfers data using DMA. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note that the master DMA transfer does not support the `transfer_size` of 1 when the `bitsPerFrame` is greater than 8.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_master_dma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	A pointer to the <a href="#">dspi_transfer_t</a> structure.

Returns

status of `status_t`.

### 11.3.4.3 **void DSPI\_MasterTransferAbortDMA ( SPI\_Type \* *base*, dspi\_master\_dma\_handle\_t \* *handle* )**

This function aborts a transfer which is using DMA.

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_master_dma_handle_t</code> structure which stores the transfer state.

#### 11.3.4.4 **status\_t DSPI\_MasterTransferGetCountDMA ( SPI\_Type \* *base*, dspi\_master\_dma\_handle\_t \* *handle*, size\_t \* *count* )**

This function gets the master DMA transfer remaining bytes.

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_master_dma_handle_t</code> structure which stores the transfer state.
<i>count</i>	A number of bytes transferred by the non-blocking transaction.

## Returns

status of `status_t`.

#### 11.3.4.5 **void DSPI\_SlaveTransferCreateHandleDMA ( SPI\_Type \* *base*, dspi\_slave\_dma\_handle\_t \* *handle*, dspi\_slave\_dma\_transfer\_callback\_t *callback*, void \* *userData*, dma\_handle\_t \* *dmaRxRegToRxDataHandle*, dma\_handle\_t \* *dmaTxDataToTxRegHandle* )**

This function initializes the DSPI DMA handle which can be used for other DSPI transactional APIs. Usually, for a specified DSPI instance, call this API once to get the initialized handle.

Note that DSPI DMA has a separated (Rx and Tx as two sources) or shared (Rx and Tx is the same source) DMA request source. (1) For a separated DMA request source, enable and set the Rx DMAMUX source for `dmaRxRegToRxDataHandle` and Tx DMAMUX source for `dmaTxDataToTxRegHandle`. (2) For a shared DMA request source, enable and set the Rx/Rx DMAMUX source for `dmaRxRegToRxDataHandle`.

## Parameters

<i>base</i>	DSPI peripheral base address.
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<i>handle</i>	DSPI handle pointer to <code>dspi_slave_dma_handle_t</code> .
<i>callback</i>	DSPI callback.
<i>userData</i>	A callback function parameter.
<i>dmaRxRegTo-RxDataHandle</i>	<code>dmaRxRegToRxDataHandle</code> pointer to <code>dma_handle_t</code> .
<i>dmaTxDataTo-TxRegHandle</i>	<code>dmaTxDataToTxRegHandle</code> pointer to <code>dma_handle_t</code> .

### 11.3.4.6 `status_t DSPI_SlaveTransferDMA ( SPI_Type * base, dspi_slave_dma_handle_t * handle, dspi_transfer_t * transfer )`

This function transfers data using DMA. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note that the slave DMA transfer does not support the `transfer_size` of 1 when the `bitsPerFrame` is greater than eight.

#### Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_slave_dma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	A pointer to the <a href="#">dspi_transfer_t</a> structure.

#### Returns

status of `status_t`.

### 11.3.4.7 `void DSPI_SlaveTransferAbortDMA ( SPI_Type * base, dspi_slave_dma_handle_t * handle )`

This function aborts a transfer which is using DMA.

#### Parameters

<i>base</i>	DSPI peripheral base address.
-------------	-------------------------------

<i>handle</i>	A pointer to the <code>dspi_slave_dma_handle_t</code> structure which stores the transfer state.
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#### 11.3.4.8 `status_t DSPI_SlaveTransferGetCountDMA ( SPI_Type * base, dspi_slave_dma_handle_t * handle, size_t * count )`

This function gets the slave DMA transfer remaining bytes.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_slave_dma_handle_t</code> structure which stores the transfer state.
<i>count</i>	A number of bytes transferred by the non-blocking transaction.

Returns

status of `status_t`.

### 11.4 DSPI eDMA Driver

#### 11.4.1 Overview

This section describes the programming interface of the DSPI Peripheral driver. The DSPI driver configures DSPI module and provides the functional and transactional interfaces to build the DSPI application.

#### Data Structures

- struct [dspi\\_master\\_edma\\_handle\\_t](#)  
*DSPI master eDMA transfer handle structure used for the transactional API. [More...](#)*
- struct [dspi\\_slave\\_edma\\_handle\\_t](#)  
*DSPI slave eDMA transfer handle structure used for the transactional API. [More...](#)*

#### Typedefs

- typedef void(\* [dspi\\_master\\_edma\\_transfer\\_callback\\_t](#) )(SPI\_Type \*base, dspi\_master\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*
- typedef void(\* [dspi\\_slave\\_edma\\_transfer\\_callback\\_t](#) )(SPI\_Type \*base, dspi\_slave\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*

#### Functions

- void [DSPI\\_MasterTransferCreateHandleEDMA](#) (SPI\_Type \*base, dspi\_master\_edma\_handle\_t \*handle, [dspi\\_master\\_edma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*edmaRxRegToRxDataHandle, [edma\\_handle\\_t](#) \*edmaTxDataToIntermediaryHandle, [edma\\_handle\\_t](#) \*edmaIntermediaryToTxRegHandle)  
*Initializes the DSPI master eDMA handle.*
- status\_t [DSPI\\_MasterTransferEDMA](#) (SPI\_Type \*base, dspi\_master\_edma\_handle\_t \*handle, [dspi\\_transfer\\_t](#) \*transfer)  
*DSPI master transfer data using eDMA.*
- void [DSPI\\_MasterTransferAbortEDMA](#) (SPI\_Type \*base, dspi\_master\_edma\_handle\_t \*handle)  
*DSPI master aborts a transfer which is using eDMA.*
- status\_t [DSPI\\_MasterTransferGetCountEDMA](#) (SPI\_Type \*base, dspi\_master\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets the master eDMA transfer count.*
- void [DSPI\\_SlaveTransferCreateHandleEDMA](#) (SPI\_Type \*base, dspi\_slave\_edma\_handle\_t \*handle, [dspi\\_slave\\_edma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*edmaRxRegToRxDataHandle, [edma\\_handle\\_t](#) \*edmaTxDataToTxRegHandle)  
*Initializes the DSPI slave eDMA handle.*
- status\_t [DSPI\\_SlaveTransferEDMA](#) (SPI\_Type \*base, dspi\_slave\_edma\_handle\_t \*handle, [dspi\\_transfer\\_t](#) \*transfer)  
*DSPI slave transfer data using eDMA.*

- void [DSPI\\_SlaveTransferAbortEDMA](#) (SPI\_Type \*base, dsp\_slave\_edma\_handle\_t \*handle)  
*DSPI slave aborts a transfer which is using eDMA.*
- status\_t [DSPI\\_SlaveTransferGetCountEDMA](#) (SPI\_Type \*base, dsp\_slave\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets the slave eDMA transfer count.*

## 11.4.2 Data Structure Documentation

### 11.4.2.1 struct \_dsp\_master\_edma\_handle

Forward declaration of the DSPI eDMA master handle typedefs.

#### Data Fields

- uint32\_t [bitsPerFrame](#)  
*The desired number of bits per frame.*
- volatile uint32\_t [command](#)  
*The desired data command.*
- volatile uint32\_t [lastCommand](#)  
*The desired last data command.*
- uint8\_t [fifoSize](#)  
*FIFO dataSize.*
- volatile bool [isPcsActiveAfterTransfer](#)  
*Indicates whether the PCS signal keeps active after the last frame transfer.*
- uint8\_t [nbytes](#)  
*eDMA minor byte transfer count initially configured.*
- volatile uint8\_t [state](#)  
*DSPI transfer state , \_dsp\_transfer\_state.*
- uint8\_t \*volatile [txData](#)  
*Send buffer.*
- uint8\_t \*volatile [rxData](#)  
*Receive buffer.*
- volatile size\_t [remainingSendByteCount](#)  
*A number of bytes remaining to send.*
- volatile size\_t [remainingReceiveByteCount](#)  
*A number of bytes remaining to receive.*
- size\_t [totalByteCount](#)  
*A number of transfer bytes.*
- uint32\_t [rxBuffIfNull](#)  
*Used if there is not rxData for DMA purpose.*
- uint32\_t [txBuffIfNull](#)  
*Used if there is not txData for DMA purpose.*
- [dsp\\_master\\_edma\\_transfer\\_callback\\_t](#) [callback](#)  
*Completion callback.*
- void \* [userData](#)  
*Callback user data.*
- [edma\\_handle\\_t](#) \* [edmaRxRegToRxDataHandle](#)  
*edma\_handle\_t handle point used for RxReg to RxData buff*

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- [edma\\_handle\\_t \\* edmaTxDataToIntermediaryHandle](#)  
*edma\_handle\_t handle point used for TxData to Intermediary*
- [edma\\_handle\\_t \\* edmaIntermediaryToTxRegHandle](#)  
*edma\_handle\_t handle point used for Intermediary to TxReg*
- [edma\\_tcd\\_t dsppiSoftwareTCD](#) [2]  
*SoftwareTCD , internal used.*

### 11.4.2.1.0.22 Field Documentation

- 11.4.2.1.0.22.1 `uint32_t dsppi_master_edma_handle_t::bitsPerFrame`
- 11.4.2.1.0.22.2 `volatile uint32_t dsppi_master_edma_handle_t::command`
- 11.4.2.1.0.22.3 `volatile uint32_t dsppi_master_edma_handle_t::lastCommand`
- 11.4.2.1.0.22.4 `uint8_t dsppi_master_edma_handle_t::fifoSize`
- 11.4.2.1.0.22.5 `volatile bool dsppi_master_edma_handle_t::isPcsActiveAfterTransfer`
- 11.4.2.1.0.22.6 `uint8_t dsppi_master_edma_handle_t::nbytes`
- 11.4.2.1.0.22.7 `volatile uint8_t dsppi_master_edma_handle_t::state`
- 11.4.2.1.0.22.8 `uint8_t* volatile dsppi_master_edma_handle_t::txData`
- 11.4.2.1.0.22.9 `uint8_t* volatile dsppi_master_edma_handle_t::rxData`
- 11.4.2.1.0.22.10 `volatile size_t dsppi_master_edma_handle_t::remainingSendByteCount`
- 11.4.2.1.0.22.11 `volatile size_t dsppi_master_edma_handle_t::remainingReceiveByteCount`
- 11.4.2.1.0.22.12 `uint32_t dsppi_master_edma_handle_t::rxBuffIfNull`
- 11.4.2.1.0.22.13 `uint32_t dsppi_master_edma_handle_t::txBuffIfNull`
- 11.4.2.1.0.22.14 `dsppi_master_edma_transfer_callback_t dsppi_master_edma_handle_t::callback`
- 11.4.2.1.0.22.15 `void* dsppi_master_edma_handle_t::userData`

### 11.4.2.2 struct \_dsppi\_slave\_edma\_handle

Forward declaration of the DSPI eDMA slave handle typedefs.

### Data Fields

- `uint32_t bitsPerFrame`  
*The desired number of bits per frame.*
- `uint8_t *volatile txData`  
*Send buffer.*
- `uint8_t *volatile rxData`



- *Receive buffer.*
- volatile size\_t [remainingSendByteCount](#)  
*A number of bytes remaining to send.*
- volatile size\_t [remainingReceiveByteCount](#)  
*A number of bytes remaining to receive.*
- size\_t [totalByteCount](#)  
*A number of transfer bytes.*
- uint32\_t [rxBuffIfNull](#)  
*Used if there is not rxData for DMA purpose.*
- uint32\_t [txBuffIfNull](#)  
*Used if there is not txData for DMA purpose.*
- uint32\_t [txLastData](#)  
*Used if there is an extra byte when 16bits per frame for DMA purpose.*
- uint8\_t [nbytes](#)  
*eDMA minor byte transfer count initially configured.*
- volatile uint8\_t [state](#)  
*DSPI transfer state.*
- [dsp\\_slave\\_edma\\_transfer\\_callback\\_t](#) [callback](#)  
*Completion callback.*
- void \* [userData](#)  
*Callback user data.*
- [edma\\_handle\\_t](#) \* [edmaRxRegToRxDataHandle](#)  
*edma\_handle\_t handle point used for RxReg to RxData buff*
- [edma\\_handle\\_t](#) \* [edmaTxDataToTxRegHandle](#)  
*edma\_handle\_t handle point used for TxData to TxReg*

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### 11.4.2.2.0.23 Field Documentation

- 11.4.2.2.0.23.1 `uint32_t dspi_slave_edma_handle_t::bitsPerFrame`
- 11.4.2.2.0.23.2 `uint8_t* volatile dspi_slave_edma_handle_t::txData`
- 11.4.2.2.0.23.3 `uint8_t* volatile dspi_slave_edma_handle_t::rxData`
- 11.4.2.2.0.23.4 `volatile size_t dspi_slave_edma_handle_t::remainingSendByteCount`
- 11.4.2.2.0.23.5 `volatile size_t dspi_slave_edma_handle_t::remainingReceiveByteCount`
- 11.4.2.2.0.23.6 `uint32_t dspi_slave_edma_handle_t::rxBuffIfNull`
- 11.4.2.2.0.23.7 `uint32_t dspi_slave_edma_handle_t::txBuffIfNull`
- 11.4.2.2.0.23.8 `uint32_t dspi_slave_edma_handle_t::txLastData`
- 11.4.2.2.0.23.9 `uint8_t dspi_slave_edma_handle_t::nbytes`
- 11.4.2.2.0.23.10 `volatile uint8_t dspi_slave_edma_handle_t::state`
- 11.4.2.2.0.23.11 `dspi_slave_edma_transfer_callback_t dspi_slave_edma_handle_t::callback`
- 11.4.2.2.0.23.12 `void* dspi_slave_edma_handle_t::userData`

### 11.4.3 Typedef Documentation

- 11.4.3.1 `typedef void(* dspi_master_edma_transfer_callback_t)(SPI_Type *base, dspi_master_edma_handle_t *handle, status_t status, void *userData)`

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the handle for the DSPI master.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	An arbitrary pointer-dataSized value passed from the application.

#### 11.4.3.2 **typedef void(\* dspi\_slave\_edma\_transfer\_callback\_t)(SPI\_Type \*base, dspi\_slave\_edma\_handle\_t \*handle, status\_t status, void \*userData)**

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the handle for the DSPI slave.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	An arbitrary pointer-dataSized value passed from the application.

### 11.4.4 Function Documentation

#### 11.4.4.1 **void DSPI\_MasterTransferCreateHandleEDMA ( SPI\_Type \* base, dspi\_master\_edma\_handle\_t \* handle, dspi\_master\_edma\_transfer\_callback\_t callback, void \* userData, edma\_handle\_t \* edmaRxRegToRxDataHandle, edma\_handle\_t \* edmaTxDataToIntermediaryHandle, edma\_handle\_t \* edmaIntermediaryToTxRegHandle )**

This function initializes the DSPI eDMA handle which can be used for other DSPI transactional APIs. Usually, for a specified DSPI instance, call this API once to get the initialized handle.

Note that DSPI eDMA has separated (RX and TX as two sources) or shared (RX and TX are the same source) DMA request source. (1) For the separated DMA request source, enable and set the RX DMAMUX source for edmaRxRegToRxDataHandle and TX DMAMUX source for edmaIntermediaryToTxRegHandle. (2) For the shared DMA request source, enable and set the RX/RX DMAMUX source for the edmaRxRegToRxDataHandle.

## Parameters

---

## DSPI eDMA Driver

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	DSPI handle pointer to <code>dspi_master_edma_handle_t</code> .
<i>callback</i>	DSPI callback.
<i>userData</i>	A callback function parameter.
<i>edmaRxRegTo-RxDataHandle</i>	<code>edmaRxRegToRxDataHandle</code> pointer to <a href="#">edma_handle_t</a> .
<i>edmaTxData-To-Intermediary-Handle</i>	<code>edmaTxDataToIntermediaryHandle</code> pointer to <a href="#">edma_handle_t</a> .
<i>edma-Intermediary-ToTxReg-Handle</i>	<code>edmaIntermediaryToTxRegHandle</code> pointer to <a href="#">edma_handle_t</a> .

**11.4.4.2** `status_t DSPI_MasterTransferEDMA ( SPI_Type * base, dspi-  
_master_edma_handle_t * handle, dspi_transfer_t * transfer  
)`

This function transfers data using eDMA. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_master_edma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	A pointer to the <a href="#">dspi_transfer_t</a> structure.

Returns

status of `status_t`.

**11.4.4.3** `void DSPI_MasterTransferAbortEDMA ( SPI_Type * base,  
dspi_master_edma_handle_t * handle )`

This function aborts a transfer which is using eDMA.

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_master_edma_handle_t</code> structure which stores the transfer state.

#### 11.4.4.4 **status\_t DSPI\_MasterTransferGetCountEDMA ( SPI\_Type \* *base*, dspi\_master\_edma\_handle\_t \* *handle*, size\_t \* *count* )**

This function gets the master eDMA transfer count.

## Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_master_edma_handle_t</code> structure which stores the transfer state.
<i>count</i>	A number of bytes transferred by the non-blocking transaction.

## Returns

status of `status_t`.

#### 11.4.4.5 **void DSPI\_SlaveTransferCreateHandleEDMA ( SPI\_Type \* *base*, dspi\_slave\_edma\_handle\_t \* *handle*, dspi\_slave\_edma\_transfer\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *edmaRxRegToRxDataHandle*, edma\_handle\_t \* *edmaTxDataToTxRegHandle* )**

This function initializes the DSPI eDMA handle which can be used for other DSPI transactional APIs. Usually, for a specified DSPI instance, call this API once to get the initialized handle.

Note that DSPI eDMA has separated (RN and TX in 2 sources) or shared (RX and TX are the same source) DMA request source. (1)For the separated DMA request source, enable and set the RX DMAMUX source for `edmaRxRegToRxDataHandle` and TX DMAMUX source for `edmaTxDataToTxRegHandle`. (2)For the shared DMA request source, enable and set the RX/RX DMAMUX source for the `edmaRxRegToRxDataHandle`.

## Parameters

<i>base</i>	DSPI peripheral base address.
-------------	-------------------------------

## DSPI eDMA Driver

<i>handle</i>	DSPI handle pointer to <code>dspi_slave_edma_handle_t</code> .
<i>callback</i>	DSPI callback.
<i>userData</i>	A callback function parameter.
<i>edmaRxRegTo-RxDataHandle</i>	<code>edmaRxRegToRxDataHandle</code> pointer to <a href="#">edma_handle_t</a> .
<i>edmaTxData-ToTxReg-Handle</i>	<code>edmaTxDataToTxRegHandle</code> pointer to <a href="#">edma_handle_t</a> .

### 11.4.4.6 `status_t DSPI_SlaveTransferEDMA ( SPI_Type * base, dspi_slave_edma_handle_t * handle, dspi_transfer_t * transfer )`

This function transfers data using eDMA. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called. Note that the slave eDMA transfer doesn't support `transfer_size` is 1 when the `bitsPerFrame` is greater than eight.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_slave_edma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	A pointer to the <a href="#">dspi_transfer_t</a> structure.

Returns

status of `status_t`.

### 11.4.4.7 `void DSPI_SlaveTransferAbortEDMA ( SPI_Type * base, dspi_slave_edma_handle_t * handle )`

This function aborts a transfer which is using eDMA.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the <code>dspi_slave_edma_handle_t</code> structure which stores the transfer state.

#### 11.4.4.8 **status\_t DSPI\_SlaveTransferGetCountEDMA ( SPI\_Type \* *base*, dspi\_slave\_edma\_handle\_t \* *handle*, size\_t \* *count* )**

This function gets the slave eDMA transfer count.

Parameters

<i>base</i>	DSPI peripheral base address.
<i>handle</i>	A pointer to the dspi_slave_edma_handle_t structure which stores the transfer state.
<i>count</i>	A number of bytes transferred so far by the non-blocking transaction.

Returns

status of status\_t.

### 11.5 DSPI FreeRTOS Driver

#### 11.5.1 Overview

#### DSPI RTOS Operation

- status\_t **DSPI\_RTOS\_Init** (dsapi\_rtos\_handle\_t \*handle, SPI\_Type \*base, const dsapi\_master\_config\_t \*masterConfig, uint32\_t srcClock\_Hz)  
*Initializes the DSPI.*
- status\_t **DSPI\_RTOS\_Deinit** (dsapi\_rtos\_handle\_t \*handle)  
*Deinitializes the DSPI.*
- status\_t **DSPI\_RTOS\_Transfer** (dsapi\_rtos\_handle\_t \*handle, dsapi\_transfer\_t \*transfer)  
*Performs the SPI transfer.*

#### 11.5.2 Function Documentation

##### 11.5.2.1 status\_t DSPI\_RTOS\_Init ( dsapi\_rtos\_handle\_t \* handle, SPI\_Type \* base, const dsapi\_master\_config\_t \* masterConfig, uint32\_t srcClock\_Hz )

This function initializes the DSPI module and the related RTOS context.

Parameters

<i>handle</i>	The RTOS DSPI handle, the pointer to an allocated space for RTOS context.
<i>base</i>	The pointer base address of the DSPI instance to initialize.
<i>masterConfig</i>	A configuration structure to set-up the DSPI in master mode.
<i>srcClock_Hz</i>	A frequency of the input clock of the DSPI module.

Returns

status of the operation.

##### 11.5.2.2 status\_t DSPI\_RTOS\_Deinit ( dsapi\_rtos\_handle\_t \* handle )

This function deinitializes the DSPI module and the related RTOS context.

Parameters



<i>handle</i>	The RTOS DSPI handle.
---------------	-----------------------

#### 11.5.2.3 **status\_t DSPI\_RTOS\_Transfer ( dspi\_rtos\_handle\_t \* *handle*, dspi\_transfer\_t \* *transfer* )**

This function performs the SPI transfer according to the data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS DSPI handle.
<i>transfer</i>	A structure specifying the transfer parameters.

Returns

status of the operation.

### 11.6 DSPI $\mu$ COS/II Driver

#### 11.6.1 Overview

#### DSPI RTOS Operation

- status\_t **DSPI\_RTOS\_Init** (dsapi\_rtos\_handle\_t \*handle, SPI\_Type \*base, const dsapi\_master\_config\_t \*masterConfig, uint32\_t srcClock\_Hz)  
*Initializes the DSPI.*
- status\_t **DSPI\_RTOS\_Deinit** (dsapi\_rtos\_handle\_t \*handle)  
*Deinitializes the DSPI.*
- status\_t **DSPI\_RTOS\_Transfer** (dsapi\_rtos\_handle\_t \*handle, dsapi\_transfer\_t \*transfer)  
*Performs the SPI transfer.*

#### 11.6.2 Function Documentation

##### 11.6.2.1 status\_t DSPI\_RTOS\_Init ( dsapi\_rtos\_handle\_t \* *handle*, SPI\_Type \* *base*, const dsapi\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

This function initializes the DSPI module and the related RTOS context.

Parameters

<i>handle</i>	The RTOS DSPI handle, the pointer to an allocated space for RTOS context.
<i>base</i>	The pointer base address of the DSPI instance to initialize.
<i>masterConfig</i>	A configuration structure to set-up the DSPI in master mode.
<i>srcClock_Hz</i>	A frequency of the input clock of the DSPI module.

Returns

status of the operation.

##### 11.6.2.2 status\_t DSPI\_RTOS\_Deinit ( dsapi\_rtos\_handle\_t \* *handle* )

This function deinitializes the DSPI module and the related RTOS context.

Parameters

<i>handle</i>	The RTOS DSPI handle.
---------------	-----------------------

### 11.6.2.3 **status\_t DSPI\_RTOS\_Transfer ( dspi\_rtos\_handle\_t \* *handle*, dspi\_transfer\_t \* *transfer* )**

This function performs the SPI transfer according to the data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS DSPI handle.
<i>transfer</i>	A structure specifying the transfer parameters.

Returns

status of the operation.

### 11.7 DSPI $\mu$ COS/III Driver

#### 11.7.1 Overview

#### DSPI RTOS Operation

- status\_t **DSPI\_RTOS\_Init** (dsapi\_rtos\_handle\_t \*handle, SPI\_Type \*base, const dsapi\_master\_config\_t \*masterConfig, uint32\_t srcClock\_Hz)  
*Initializes the DSPI.*
- status\_t **DSPI\_RTOS\_Deinit** (dsapi\_rtos\_handle\_t \*handle)  
*Deinitializes the DSPI.*
- status\_t **DSPI\_RTOS\_Transfer** (dsapi\_rtos\_handle\_t \*handle, dsapi\_transfer\_t \*transfer)  
*Performs the SPI transfer.*

#### 11.7.2 Function Documentation

##### 11.7.2.1 status\_t DSPI\_RTOS\_Init ( dsapi\_rtos\_handle\_t \* *handle*, SPI\_Type \* *base*, const dsapi\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

This function initializes the DSPI module and the related RTOS context.

Parameters

<i>handle</i>	The RTOS DSPI handle, the pointer to an allocated space for RTOS context.
<i>base</i>	The pointer base address of the DSPI instance to initialize.
<i>masterConfig</i>	A configuration structure to set-up the DSPI in master mode.
<i>srcClock_Hz</i>	A frequency of the input clock of the DSPI module.

Returns

status of the operation.

##### 11.7.2.2 status\_t DSPI\_RTOS\_Deinit ( dsapi\_rtos\_handle\_t \* *handle* )

This function deinitializes the DSPI module and the related RTOS context.

Parameters

<i>handle</i>	The RTOS DSPI handle.
---------------	-----------------------

### 11.7.2.3 **status\_t DSPI\_RTOS\_Transfer ( dspi\_rtos\_handle\_t \* *handle*, dspi\_transfer\_t \* *transfer* )**

This function performs the SPI transfer according to the data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS DSPI handle.
<i>transfer</i>	A structure specifying the transfer parameters.

Returns

status of the operation.



## Chapter 12

# eDMA: Enhanced Direct Memory Access (eDMA) Controller Driver

## 12.1 Overview

The KSDK provides a peripheral driver for the enhanced Direct Memory Access (eDMA) of Kinetis devices.

## 12.2 Typical use case

### 12.2.1 eDMA Operation

```
edma_transfer_config_t transferConfig;
edma_config_t userConfig;
uint32_t transferDone = false;

EDMA_GetDefaultConfig(&userConfig);
EDMA_Init(DMA0, &userConfig);
EDMA_CreateHandle(&g_EDMA_Handle, DMA0, channel);
EDMA_SetCallback(&g_EDMA_Handle, EDMA_Callback, &transferDone);
EDMA_PrepareTransfer(&transferConfig, srcAddr, srcWidth, destAddr, destWidth,
                    bytesEachRequest, transferBytes, kEDMA_MemoryToMemory);
EDMA_SubmitTransfer(&g_EDMA_Handle, &transferConfig, true);
EDMA_StartTransfer(&g_EDMA_Handle);
/* Waits for the eDMA transfer to finish */
while (transferDone != true);
```

## Data Structures

- struct [edma\\_config\\_t](#)  
*eDMA global configuration structure. [More...](#)*
- struct [edma\\_transfer\\_config\\_t](#)  
*eDMA transfer configuration [More...](#)*
- struct [edma\\_channel\\_preemption\\_config\\_t](#)  
*eDMA channel priority configuration [More...](#)*
- struct [edma\\_minor\\_offset\\_config\\_t](#)  
*eDMA minor offset configuration [More...](#)*
- struct [edma\\_tcd\\_t](#)  
*eDMA TCD. [More...](#)*
- struct [edma\\_handle\\_t](#)  
*eDMA transfer handle structure [More...](#)*

## Macros

- #define [DMA\\_DCHPRI\\_INDEX](#)(channel) (((channel) & ~0x03U) | (3 - ((channel)&0x03U)))  
*Compute the offset unit from DCHPRI3.*
- #define [DMA\\_DCHPRIn](#)(base, channel) ((volatile uint8\_t \*)&(base->DCHPRI3))[[DMA\\_DCHPRI\\_INDEX](#)(channel)]  
*Get the pointer of DCHPRIn.*

## Typical use case

## Typedefs

- typedef void(\* [edma\\_callback](#) )(struct \_edma\_handle \*handle, void \*userData, bool transferDone, uint32\_t tcDs)  
*Define callback function for eDMA.*

## Enumerations

- enum [edma\\_transfer\\_size\\_t](#) {  
    [kEDMA\\_TransferSize1Bytes](#) = 0x0U,  
    [kEDMA\\_TransferSize2Bytes](#) = 0x1U,  
    [kEDMA\\_TransferSize4Bytes](#) = 0x2U,  
    [kEDMA\\_TransferSize16Bytes](#) = 0x4U,  
    [kEDMA\\_TransferSize32Bytes](#) = 0x5U }  
*eDMA transfer configuration*
- enum [edma\\_modulo\\_t](#) {



```

kEDMA_ModuloDisable = 0x0U,
kEDMA_Modulo2bytes,
kEDMA_Modulo4bytes,
kEDMA_Modulo8bytes,
kEDMA_Modulo16bytes,
kEDMA_Modulo32bytes,
kEDMA_Modulo64bytes,
kEDMA_Modulo128bytes,
kEDMA_Modulo256bytes,
kEDMA_Modulo512bytes,
kEDMA_Modulo1Kbytes,
kEDMA_Modulo2Kbytes,
kEDMA_Modulo4Kbytes,
kEDMA_Modulo8Kbytes,
kEDMA_Modulo16Kbytes,
kEDMA_Modulo32Kbytes,
kEDMA_Modulo64Kbytes,
kEDMA_Modulo128Kbytes,
kEDMA_Modulo256Kbytes,
kEDMA_Modulo512Kbytes,
kEDMA_Modulo1Mbytes,
kEDMA_Modulo2Mbytes,
kEDMA_Modulo4Mbytes,
kEDMA_Modulo8Mbytes,
kEDMA_Modulo16Mbytes,
kEDMA_Modulo32Mbytes,
kEDMA_Modulo64Mbytes,
kEDMA_Modulo128Mbytes,
kEDMA_Modulo256Mbytes,
kEDMA_Modulo512Mbytes,
kEDMA_Modulo1Gbytes,
kEDMA_Modulo2Gbytes }
    eDMA modulo configuration
• enum edma_bandwidth_t {
    kEDMA_BandwidthStallNone = 0x0U,
    kEDMA_BandwidthStall4Cycle = 0x2U,
    kEDMA_BandwidthStall8Cycle = 0x3U }
    Bandwidth control.
• enum edma_channel_link_type_t {
    kEDMA_LinkNone = 0x0U,
    kEDMA_MinorLink,
    kEDMA_MajorLink }
    Channel link type.
• enum _edma_channel_status_flags {

```

## Typical use case

- ```
kEDMA_DoneFlag = 0x1U,  
kEDMA_ErrorFlag = 0x2U,  
kEDMA_InterruptFlag = 0x4U }
```
- eDMA channel status flags.*
- enum `_edma_error_status_flags` {  
    kEDMA\_DestinationBusErrorFlag = DMA\_ES\_DBE\_MASK,  
    kEDMA\_SourceBusErrorFlag = DMA\_ES\_SBE\_MASK,  
    kEDMA\_ScatterGatherErrorFlag = DMA\_ES\_SGE\_MASK,  
    kEDMA\_NbytesErrorFlag = DMA\_ES\_NCE\_MASK,  
    kEDMA\_DestinationOffsetErrorFlag = DMA\_ES\_DOE\_MASK,  
    kEDMA\_DestinationAddressErrorFlag = DMA\_ES\_DAE\_MASK,  
    kEDMA\_SourceOffsetErrorFlag = DMA\_ES\_SOE\_MASK,  
    kEDMA\_SourceAddressErrorFlag = DMA\_ES\_SAE\_MASK,  
    kEDMA\_ErrorChannelFlag = DMA\_ES\_ERRCHN\_MASK,  
    kEDMA\_ChannelPriorityErrorFlag = DMA\_ES\_CPE\_MASK,  
    kEDMA\_TransferCanceledFlag = DMA\_ES\_ECX\_MASK,  
    kEDMA\_GroupPriorityErrorFlag = DMA\_ES\_GPE\_MASK,  
    kEDMA\_ValidFlag = DMA\_ES\_VLD\_MASK }
- eDMA channel error status flags.*
- enum `edma_interrupt_enable_t` {  
    kEDMA\_ErrorInterruptEnable = 0x1U,  
    kEDMA\_MajorInterruptEnable = DMA\_CSR\_INTMAJOR\_MASK,  
    kEDMA\_HalfInterruptEnable = DMA\_CSR\_INTHALF\_MASK }
- eDMA interrupt source*
- enum `edma_transfer_type_t` {  
    kEDMA\_MemoryToMemory = 0x0U,  
    kEDMA\_PeripheralToMemory,  
    kEDMA\_MemoryToPeripheral }
- eDMA transfer type*
- enum `_edma_transfer_status` {  
    kStatus\_EDMA\_QueueFull = MAKE\_STATUS(kStatusGroup\_EDMA, 0),  
    kStatus\_EDMA\_Busy = MAKE\_STATUS(kStatusGroup\_EDMA, 1) }
- eDMA transfer status*

## Driver version

- #define `FSL_EDMA_DRIVER_VERSION` (`MAKE_VERSION`(2, 1, 1))  
*eDMA driver version*

## eDMA initialization and de-initialization

- void `EDMA_Init` (DMA\_Type \*base, const `edma_config_t` \*config)  
*Initializes the eDMA peripheral.*
- void `EDMA_Deinit` (DMA\_Type \*base)  
*Deinitializes the eDMA peripheral.*
- void `EDMA_GetDefaultConfig` (`edma_config_t` \*config)  
*Gets the eDMA default configuration structure.*

## eDMA Channel Operation

- void [EDMA\\_ResetChannel](#) (DMA\_Type \*base, uint32\_t channel)  
*Sets all TCD registers to default values.*
- void [EDMA\\_SetTransferConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_transfer\\_config\\_t](#) \*config, [edma\\_tcd\\_t](#) \*nextTcd)  
*Configures the eDMA transfer attribute.*
- void [EDMA\\_SetMinorOffsetConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_minor\\_offset\\_config\\_t](#) \*config)  
*Configures the eDMA minor offset feature.*
- static void [EDMA\\_SetChannelPreemptionConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_channel\\_preemption\\_config\\_t](#) \*config)  
*Configures the eDMA channel preemption feature.*
- void [EDMA\\_SetChannelLink](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_channel\\_link\\_type\\_t](#) type, uint32\_t linkedChannel)  
*Sets the channel link for the eDMA transfer.*
- void [EDMA\\_SetBandWidth](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_bandwidth\\_t](#) bandWidth)  
*Sets the bandwidth for the eDMA transfer.*
- void [EDMA\\_SetModulo](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_modulo\\_t](#) srcModulo, [edma\\_modulo\\_t](#) destModulo)  
*Sets the source modulo and the destination modulo for the eDMA transfer.*
- static void [EDMA\\_EnableAsyncRequest](#) (DMA\_Type \*base, uint32\_t channel, bool enable)  
*Enables an async request for the eDMA transfer.*
- static void [EDMA\\_EnableAutoStopRequest](#) (DMA\_Type \*base, uint32\_t channel, bool enable)  
*Enables an auto stop request for the eDMA transfer.*
- void [EDMA\\_EnableChannelInterrupts](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Enables the interrupt source for the eDMA transfer.*
- void [EDMA\\_DisableChannelInterrupts](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Disables the interrupt source for the eDMA transfer.*

## eDMA TCD Operation

- void [EDMA\\_TcdReset](#) ([edma\\_tcd\\_t](#) \*tcd)  
*Sets all fields to default values for the TCD structure.*
- void [EDMA\\_TcdSetTransferConfig](#) ([edma\\_tcd\\_t](#) \*tcd, const [edma\\_transfer\\_config\\_t](#) \*config, [edma\\_tcd\\_t](#) \*nextTcd)  
*Configures the eDMA TCD transfer attribute.*
- void [EDMA\\_TcdSetMinorOffsetConfig](#) ([edma\\_tcd\\_t](#) \*tcd, const [edma\\_minor\\_offset\\_config\\_t](#) \*config)  
*Configures the eDMA TCD minor offset feature.*
- void [EDMA\\_TcdSetChannelLink](#) ([edma\\_tcd\\_t](#) \*tcd, [edma\\_channel\\_link\\_type\\_t](#) type, uint32\_t linkedChannel)  
*Sets the channel link for the eDMA TCD.*
- static void [EDMA\\_TcdSetBandWidth](#) ([edma\\_tcd\\_t](#) \*tcd, [edma\\_bandwidth\\_t](#) bandWidth)  
*Sets the bandwidth for the eDMA TCD.*
- void [EDMA\\_TcdSetModulo](#) ([edma\\_tcd\\_t](#) \*tcd, [edma\\_modulo\\_t](#) srcModulo, [edma\\_modulo\\_t](#) destModulo)  
*Sets the source modulo and the destination modulo for the eDMA TCD.*
- static void [EDMA\\_TcdEnableAutoStopRequest](#) ([edma\\_tcd\\_t](#) \*tcd, bool enable)  
*Sets the auto stop request for the eDMA TCD.*

## Typical use case

- void [EDMA\\_TcdEnableInterrupts](#) ([edma\\_tcd\\_t](#) \*tcd, uint32\_t mask)  
*Enables the interrupt source for the eDMA TCD.*
- void [EDMA\\_TcdDisableInterrupts](#) ([edma\\_tcd\\_t](#) \*tcd, uint32\_t mask)  
*Disables the interrupt source for the eDMA TCD.*

## eDMA Channel Transfer Operation

- static void [EDMA\\_EnableChannelRequest](#) ([DMA\\_Type](#) \*base, uint32\_t channel)  
*Enables the eDMA hardware channel request.*
- static void [EDMA\\_DisableChannelRequest](#) ([DMA\\_Type](#) \*base, uint32\_t channel)  
*Disables the eDMA hardware channel request.*
- static void [EDMA\\_TriggerChannelStart](#) ([DMA\\_Type](#) \*base, uint32\_t channel)  
*Starts the eDMA transfer by using the software trigger.*

## eDMA Channel Status Operation

- uint32\_t [EDMA\\_GetRemainingMajorLoopCount](#) ([DMA\\_Type](#) \*base, uint32\_t channel)  
*Gets the remaining major loop count from the eDMA current channel TCD.*
- static uint32\_t [EDMA\\_GetErrorStatusFlags](#) ([DMA\\_Type](#) \*base)  
*Gets the eDMA channel error status flags.*
- uint32\_t [EDMA\\_GetChannelStatusFlags](#) ([DMA\\_Type](#) \*base, uint32\_t channel)  
*Gets the eDMA channel status flags.*
- void [EDMA\\_ClearChannelStatusFlags](#) ([DMA\\_Type](#) \*base, uint32\_t channel, uint32\_t mask)  
*Clears the eDMA channel status flags.*

## eDMA Transactional Operation

- void [EDMA\\_CreateHandle](#) ([edma\\_handle\\_t](#) \*handle, [DMA\\_Type](#) \*base, uint32\_t channel)  
*Creates the eDMA handle.*
- void [EDMA\\_InstallTCDMemory](#) ([edma\\_handle\\_t](#) \*handle, [edma\\_tcd\\_t](#) \*tcdPool, uint32\_t tcdSize)  
*Installs the TCDs memory pool into the eDMA handle.*
- void [EDMA\\_SetCallback](#) ([edma\\_handle\\_t](#) \*handle, [edma\\_callback](#) callback, void \*userData)  
*Installs a callback function for the eDMA transfer.*
- void [EDMA\\_PrepareTransfer](#) ([edma\\_transfer\\_config\\_t](#) \*config, void \*srcAddr, uint32\_t srcWidth, void \*destAddr, uint32\_t destWidth, uint32\_t bytesEachRequest, uint32\_t transferBytes, [edma\\_transfer\\_type\\_t](#) type)  
*Prepares the eDMA transfer structure.*
- status\_t [EDMA\\_SubmitTransfer](#) ([edma\\_handle\\_t](#) \*handle, const [edma\\_transfer\\_config\\_t](#) \*config)  
*Submits the eDMA transfer request.*
- void [EDMA\\_StartTransfer](#) ([edma\\_handle\\_t](#) \*handle)  
*eDMA starts transfer.*
- void [EDMA\\_StopTransfer](#) ([edma\\_handle\\_t](#) \*handle)  
*eDMA stops transfer.*
- void [EDMA\\_AbortTransfer](#) ([edma\\_handle\\_t](#) \*handle)  
*eDMA aborts transfer.*
- void [EDMA\\_HandleIRQ](#) ([edma\\_handle\\_t](#) \*handle)  
*eDMA IRQ handler for the current major loop transfer completion.*

## 12.3 Data Structure Documentation

### 12.3.1 struct edma\_config\_t

#### Data Fields

- bool [enableContinuousLinkMode](#)  
*Enable (true) continuous link mode.*
- bool [enableHaltOnError](#)  
*Enable (true) transfer halt on error.*
- bool [enableRoundRobinArbitration](#)  
*Enable (true) round robin channel arbitration method or fixed priority arbitration is used for channel selection.*
- bool [enableDebugMode](#)  
*Enable(true) eDMA debug mode.*

#### 12.3.1.0.0.24 Field Documentation

##### 12.3.1.0.0.24.1 bool edma\_config\_t::enableContinuousLinkMode

Upon minor loop completion, the channel activates again if that channel has a minor loop channel link enabled and the link channel is itself.

##### 12.3.1.0.0.24.2 bool edma\_config\_t::enableHaltOnError

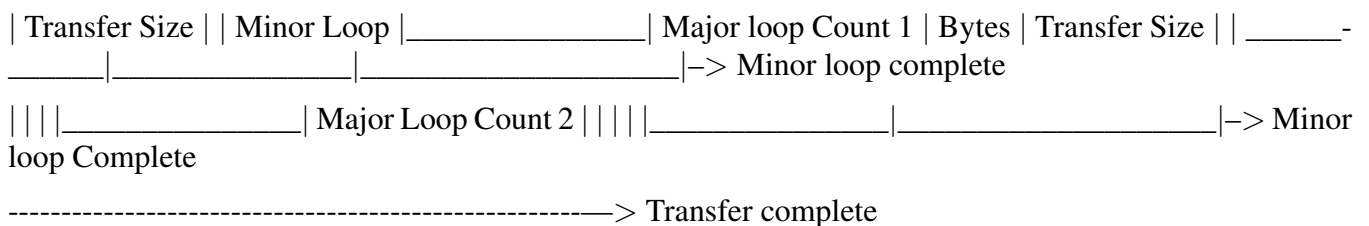
Any error causes the HALT bit to set. Subsequently, all service requests are ignored until the HALT bit is cleared.

##### 12.3.1.0.0.24.3 bool edma\_config\_t::enableDebugMode

When in debug mode, the eDMA stalls the start of a new channel. Executing channels are allowed to complete.

### 12.3.2 struct edma\_transfer\_config\_t

This structure configures the source/destination transfer attribute. This figure shows the eDMA's transfer model:



### Data Fields

- `uint32_t srcAddr`  
*Source data address.*
- `uint32_t destAddr`  
*Destination data address.*
- `edma_transfer_size_t srcTransferSize`  
*Source data transfer size.*
- `edma_transfer_size_t destTransferSize`  
*Destination data transfer size.*
- `int16_t srcOffset`  
*Sign-extended offset applied to the current source address to form the next-state value as each source read is completed.*
- `int16_t destOffset`  
*Sign-extended offset applied to the current destination address to form the next-state value as each destination write is completed.*
- `uint32_t minorLoopBytes`  
*Bytes to transfer in a minor loop.*
- `uint32_t majorLoopCounts`  
*Major loop iteration count.*

#### 12.3.2.0.0.25 Field Documentation

12.3.2.0.0.25.1 `uint32_t edma_transfer_config_t::srcAddr`

12.3.2.0.0.25.2 `uint32_t edma_transfer_config_t::destAddr`

12.3.2.0.0.25.3 `edma_transfer_size_t edma_transfer_config_t::srcTransferSize`

12.3.2.0.0.25.4 `edma_transfer_size_t edma_transfer_config_t::destTransferSize`

12.3.2.0.0.25.5 `int16_t edma_transfer_config_t::srcOffset`

12.3.2.0.0.25.6 `int16_t edma_transfer_config_t::destOffset`

12.3.2.0.0.25.7 `uint32_t edma_transfer_config_t::majorLoopCounts`

### 12.3.3 `struct edma_channel_Preemption_config_t`

#### Data Fields

- `bool enableChannelPreemption`  
*If true: a channel can be suspended by other channel with higher priority.*
- `bool enablePreemptAbility`  
*If true: a channel can suspend other channel with low priority.*
- `uint8_t channelPriority`  
*Channel priority.*

### 12.3.4 struct edma\_minor\_offset\_config\_t

#### Data Fields

- bool [enableSrcMinorOffset](#)  
*Enable(true) or Disable(false) source minor loop offset.*
- bool [enableDestMinorOffset](#)  
*Enable(true) or Disable(false) destination minor loop offset.*
- uint32\_t [minorOffset](#)  
*Offset for a minor loop mapping.*

#### 12.3.4.0.0.26 Field Documentation

12.3.4.0.0.26.1 bool edma\_minor\_offset\_config\_t::enableSrcMinorOffset

12.3.4.0.0.26.2 bool edma\_minor\_offset\_config\_t::enableDestMinorOffset

12.3.4.0.0.26.3 uint32\_t edma\_minor\_offset\_config\_t::minorOffset

### 12.3.5 struct edma\_tcd\_t

This structure is same as TCD register which is described in reference manual, and is used to configure the scatter/gather feature as a next hardware TCD.

#### Data Fields

- \_\_IO uint32\_t [SADDR](#)  
*SADDR register, used to save source address.*
- \_\_IO uint16\_t [SOFF](#)  
*SOFF register, save offset bytes every transfer.*
- \_\_IO uint16\_t [ATTR](#)  
*ATTR register, source/destination transfer size and modulo.*
- \_\_IO uint32\_t [NBYTES](#)  
*Nbytes register, minor loop length in bytes.*
- \_\_IO uint32\_t [SLAST](#)  
*SLAST register.*
- \_\_IO uint32\_t [DADDR](#)  
*DADDR register, used for destination address.*
- \_\_IO uint16\_t [DOFF](#)  
*DOFF register, used for destination offset.*
- \_\_IO uint16\_t [CITER](#)  
*CITER register, current minor loop numbers, for unfinished minor loop.*
- \_\_IO uint32\_t [DLAST\\_SGA](#)  
*DLASTSGA register, next stcd address used in scatter-gather mode.*
- \_\_IO uint16\_t [CSR](#)  
*CSR register, for TCD control status.*
- \_\_IO uint16\_t [BITER](#)  
*BITER register, begin minor loop count.*

## Data Structure Documentation

### 12.3.5.0.0.27 Field Documentation

12.3.5.0.0.27.1 `__IO uint16_t edma_tcd_t::CITER`

12.3.5.0.0.27.2 `__IO uint16_t edma_tcd_t::BITER`

### 12.3.6 struct edma\_handle\_t

#### Data Fields

- `edma_callback callback`  
*Callback function for major count exhausted.*
- `void * userData`  
*Callback function parameter.*
- `DMA_Type * base`  
*eDMA peripheral base address.*
- `edma_tcd_t * tcdPool`  
*Pointer to memory stored TCDs.*
- `uint8_t channel`  
*eDMA channel number.*
- `volatile int8_t header`  
*The first TCD index.*
- `volatile int8_t tail`  
*The last TCD index.*
- `volatile int8_t tcdUsed`  
*The number of used TCD slots.*
- `volatile int8_t tcdSize`  
*The total number of TCD slots in the queue.*
- `uint8_t flags`  
*The status of the current channel.*

### 12.3.6.0.0.28 Field Documentation

12.3.6.0.0.28.1 `edma_callback edma_handle_t::callback`

12.3.6.0.0.28.2 `void* edma_handle_t::userData`

12.3.6.0.0.28.3 `DMA_Type* edma_handle_t::base`

12.3.6.0.0.28.4 `edma_tcd_t* edma_handle_t::tcdPool`

12.3.6.0.0.28.5 `uint8_t edma_handle_t::channel`

12.3.6.0.0.28.6 `volatile int8_t edma_handle_t::header`

Should point to the next TCD to be loaded into the eDMA engine.

12.3.6.0.0.28.7 `volatile int8_t edma_handle_t::tail`

Should point to the next TCD to be stored into the memory pool.



**12.3.6.0.0.28.8 volatile int8\_t edma\_handle\_t::tcdUsed**

Should reflect the number of TCDs can be used/loaded in the memory.

**12.3.6.0.0.28.9 volatile int8\_t edma\_handle\_t::tcdSize****12.3.6.0.0.28.10 uint8\_t edma\_handle\_t::flags****12.4 Macro Definition Documentation****12.4.1 #define FSL\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))**

Version 2.1.1.

**12.5 Typedef Documentation****12.5.1 typedef void(\* edma\_callback)(struct \_edma\_handle \*handle, void \*userData, bool transferDone, uint32\_t tcds)****12.6 Enumeration Type Documentation****12.6.1 enum edma\_transfer\_size\_t**

Enumerator

*kEDMA\_TransferSize1Bytes* Source/Destination data transfer size is 1 byte every time.  
*kEDMA\_TransferSize2Bytes* Source/Destination data transfer size is 2 bytes every time.  
*kEDMA\_TransferSize4Bytes* Source/Destination data transfer size is 4 bytes every time.  
*kEDMA\_TransferSize16Bytes* Source/Destination data transfer size is 16 bytes every time.  
*kEDMA\_TransferSize32Bytes* Source/Destination data transfer size is 32 bytes every time.

**12.6.2 enum edma\_modulo\_t**

Enumerator

*kEDMA\_ModuloDisable* Disable modulo.  
*kEDMA\_Modulo2bytes* Circular buffer size is 2 bytes.  
*kEDMA\_Modulo4bytes* Circular buffer size is 4 bytes.  
*kEDMA\_Modulo8bytes* Circular buffer size is 8 bytes.  
*kEDMA\_Modulo16bytes* Circular buffer size is 16 bytes.  
*kEDMA\_Modulo32bytes* Circular buffer size is 32 bytes.  
*kEDMA\_Modulo64bytes* Circular buffer size is 64 bytes.  
*kEDMA\_Modulo128bytes* Circular buffer size is 128 bytes.  
*kEDMA\_Modulo256bytes* Circular buffer size is 256 bytes.  
*kEDMA\_Modulo512bytes* Circular buffer size is 512 bytes.  
*kEDMA\_Modulo1Kbytes* Circular buffer size is 1 K bytes.

## Enumeration Type Documentation

*kEDMA\_Modulo2Kbytes* Circular buffer size is 2 K bytes.  
*kEDMA\_Modulo4Kbytes* Circular buffer size is 4 K bytes.  
*kEDMA\_Modulo8Kbytes* Circular buffer size is 8 K bytes.  
*kEDMA\_Modulo16Kbytes* Circular buffer size is 16 K bytes.  
*kEDMA\_Modulo32Kbytes* Circular buffer size is 32 K bytes.  
*kEDMA\_Modulo64Kbytes* Circular buffer size is 64 K bytes.  
*kEDMA\_Modulo128Kbytes* Circular buffer size is 128 K bytes.  
*kEDMA\_Modulo256Kbytes* Circular buffer size is 256 K bytes.  
*kEDMA\_Modulo512Kbytes* Circular buffer size is 512 K bytes.  
*kEDMA\_Modulo1Mbytes* Circular buffer size is 1 M bytes.  
*kEDMA\_Modulo2Mbytes* Circular buffer size is 2 M bytes.  
*kEDMA\_Modulo4Mbytes* Circular buffer size is 4 M bytes.  
*kEDMA\_Modulo8Mbytes* Circular buffer size is 8 M bytes.  
*kEDMA\_Modulo16Mbytes* Circular buffer size is 16 M bytes.  
*kEDMA\_Modulo32Mbytes* Circular buffer size is 32 M bytes.  
*kEDMA\_Modulo64Mbytes* Circular buffer size is 64 M bytes.  
*kEDMA\_Modulo128Mbytes* Circular buffer size is 128 M bytes.  
*kEDMA\_Modulo256Mbytes* Circular buffer size is 256 M bytes.  
*kEDMA\_Modulo512Mbytes* Circular buffer size is 512 M bytes.  
*kEDMA\_Modulo1Gbytes* Circular buffer size is 1 G bytes.  
*kEDMA\_Modulo2Gbytes* Circular buffer size is 2 G bytes.

### 12.6.3 enum edma\_bandwidth\_t

Enumerator

*kEDMA\_BandwidthStallNone* No eDMA engine stalls.  
*kEDMA\_BandwidthStall4Cycle* eDMA engine stalls for 4 cycles after each read/write.  
*kEDMA\_BandwidthStall8Cycle* eDMA engine stalls for 8 cycles after each read/write.

### 12.6.4 enum edma\_channel\_link\_type\_t

Enumerator

*kEDMA\_LinkNone* No channel link.  
*kEDMA\_MinorLink* Channel link after each minor loop.  
*kEDMA\_MajorLink* Channel link while major loop count exhausted.

### 12.6.5 enum \_edma\_channel\_status\_flags

Enumerator

*kEDMA\_DoneFlag* DONE flag, set while transfer finished, CITER value exhausted.

***kEDMA\_ErrorFlag*** eDMA error flag, an error occurred in a transfer

***kEDMA\_InterruptFlag*** eDMA interrupt flag, set while an interrupt occurred of this channel

### 12.6.6 enum \_edma\_error\_status\_flags

Enumerator

***kEDMA\_DestinationBusErrorFlag*** Bus error on destination address.

***kEDMA\_SourceBusErrorFlag*** Bus error on the source address.

***kEDMA\_ScatterGatherErrorFlag*** Error on the Scatter/Gather address, not 32byte aligned.

***kEDMA\_NbytesErrorFlag*** NBYTES/CITER configuration error.

***kEDMA\_DestinationOffsetErrorFlag*** Destination offset not aligned with destination size.

***kEDMA\_DestinationAddressErrorFlag*** Destination address not aligned with destination size.

***kEDMA\_SourceOffsetErrorFlag*** Source offset not aligned with source size.

***kEDMA\_SourceAddressErrorFlag*** Source address not aligned with source size.

***kEDMA\_ErrorChannelFlag*** Error channel number of the cancelled channel number.

***kEDMA\_ChannelPriorityErrorFlag*** Channel priority is not unique.

***kEDMA\_TransferCanceledFlag*** Transfer cancelled.

***kEDMA\_GroupPriorityErrorFlag*** Group priority is not unique.

***kEDMA\_ValidFlag*** No error occurred, this bit is 0. Otherwise, it is 1.

### 12.6.7 enum edma\_interrupt\_enable\_t

Enumerator

***kEDMA\_ErrorInterruptEnable*** Enable interrupt while channel error occurs.

***kEDMA\_MajorInterruptEnable*** Enable interrupt while major count exhausted.

***kEDMA\_HalfInterruptEnable*** Enable interrupt while major count to half value.

### 12.6.8 enum edma\_transfer\_type\_t

Enumerator

***kEDMA\_MemoryToMemory*** Transfer from memory to memory.

***kEDMA\_PeripheralToMemory*** Transfer from peripheral to memory.

***kEDMA\_MemoryToPeripheral*** Transfer from memory to peripheral.

## Function Documentation

### 12.6.9 enum \_edma\_transfer\_status

Enumerator

*kStatus\_EDMA\_QueueFull* TCD queue is full.

*kStatus\_EDMA\_Busy* Channel is busy and can't handle the transfer request.

## 12.7 Function Documentation

### 12.7.1 void EDMA\_Init ( DMA\_Type \* *base*, const edma\_config\_t \* *config* )

This function ungates the eDMA clock and configures the eDMA peripheral according to the configuration structure.

Parameters

|               |                                                                |
|---------------|----------------------------------------------------------------|
| <i>base</i>   | eDMA peripheral base address.                                  |
| <i>config</i> | A pointer to the configuration structure, see "edma_config_t". |

Note

This function enables the minor loop map feature.

### 12.7.2 void EDMA\_Deinit ( DMA\_Type \* *base* )

This function gates the eDMA clock.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | eDMA peripheral base address. |
|-------------|-------------------------------|

### 12.7.3 void EDMA\_GetDefaultConfig ( edma\_config\_t \* *config* )

This function sets the configuration structure to default values. The default configuration is set to the following values.

```
* config.enableContinuousLinkMode = false;  
* config.enableHaltOnError = true;  
* config.enableRoundRobinArbitration = false;  
* config.enableDebugMode = false;  
*
```

## Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>config</i> | A pointer to the eDMA configuration structure. |
|---------------|------------------------------------------------|

### 12.7.4 void EDMA\_ResetChannel ( DMA\_Type \* *base*, uint32\_t *channel* )

This function sets TCD registers for this channel to default values.

## Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

## Note

This function must not be called while the channel transfer is ongoing or it causes unpredictable results.

This function enables the auto stop request feature.

### 12.7.5 void EDMA\_SetTransferConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_transfer\_config\_t \* *config*, edma\_tcd\_t \* *nextTcd* )

This function configures the transfer attribute, including source address, destination address, transfer size, address offset, and so on. It also configures the scatter gather feature if the user supplies the TCD address.

Example:

```
* edma_transfer_t config;
* edma_tcd_t tcd;
* config.srcAddr = ..;
* config.destAddr = ..;
* ...
* EDMA_SetTransferConfig(DMA0, channel, &config, &stcd);
*
```

## Parameters

|                |                                                                                               |
|----------------|-----------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                 |
| <i>channel</i> | eDMA channel number.                                                                          |
| <i>config</i>  | Pointer to eDMA transfer configuration structure.                                             |
| <i>nextTcd</i> | Point to TCD structure. It can be NULL if users do not want to enable scatter/gather feature. |

## Function Documentation

### Note

If nextTcd is not NULL, it means scatter gather feature is enabled and DREQ bit is cleared in the previous transfer configuration, which is set in the eDMA\_ResetChannel.

### 12.7.6 void EDMA\_SetMinorOffsetConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_minor\_offset\_config\_t \* *config* )

The minor offset means that the signed-extended value is added to the source address or destination address after each minor loop.

#### Parameters

|                |                                                        |
|----------------|--------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                          |
| <i>channel</i> | eDMA channel number.                                   |
| <i>config</i>  | A pointer to the minor offset configuration structure. |

### 12.7.7 static void EDMA\_SetChannelPreemptionConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_channel\_Preemption\_config\_t \* *config* ) [inline], [static]

This function configures the channel preemption attribute and the priority of the channel.

#### Parameters

|                |                                                              |
|----------------|--------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                |
| <i>channel</i> | eDMA channel number                                          |
| <i>config</i>  | A pointer to the channel preemption configuration structure. |

### 12.7.8 void EDMA\_SetChannelLink ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_channel\_link\_type\_t *type*, uint32\_t *linkedChannel* )

This function configures either the minor link or the major link mode. The minor link means that the channel link is triggered every time CITER decreases by 1. The major link means that the channel link is triggered when the CITER is exhausted.

## Parameters

|                      |                                                                                                                                                                                  |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>          | eDMA peripheral base address.                                                                                                                                                    |
| <i>channel</i>       | eDMA channel number.                                                                                                                                                             |
| <i>type</i>          | A channel link type, which can be one of the following: <ul style="list-style-type: none"> <li>• kEDMA_LinkNone</li> <li>• kEDMA_MinorLink</li> <li>• kEDMA_MajorLink</li> </ul> |
| <i>linkedChannel</i> | The linked channel number.                                                                                                                                                       |

## Note

Users should ensure that DONE flag is cleared before calling this interface, or the configuration is invalid.

### 12.7.9 void EDMA\_SetBandWidth ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_bandwidth\_t *bandWidth* )

Because the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. The bandwidth forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch.

## Parameters

|                  |                                                                                                                                                                                                               |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>      | eDMA peripheral base address.                                                                                                                                                                                 |
| <i>channel</i>   | eDMA channel number.                                                                                                                                                                                          |
| <i>bandWidth</i> | A bandwidth setting, which can be one of the following: <ul style="list-style-type: none"> <li>• kEDMABandwidthStallNone</li> <li>• kEDMABandwidthStall4Cycle</li> <li>• kEDMABandwidthStall8Cycle</li> </ul> |

### 12.7.10 void EDMA\_SetModulo ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_modulo\_t *srcModulo*, edma\_modulo\_t *destModulo* )

This function defines a specific address range specified to be the value after (SADDR + SOFF)/(DADDR + DOFF) calculation is performed or the original register value. It provides the ability to implement a circular data queue easily.

## Function Documentation

### Parameters

|                   |                               |
|-------------------|-------------------------------|
| <i>base</i>       | eDMA peripheral base address. |
| <i>channel</i>    | eDMA channel number.          |
| <i>srcModulo</i>  | A source modulo value.        |
| <i>destModulo</i> | A destination modulo value.   |

**12.7.11 static void EDMA\_EnableAsyncRequest ( DMA\_Type \* *base*, uint32\_t *channel*, bool *enable* ) [inline], [static]**

### Parameters

|                |                                                  |
|----------------|--------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                    |
| <i>channel</i> | eDMA channel number.                             |
| <i>enable</i>  | The command to enable (true) or disable (false). |

**12.7.12 static void EDMA\_EnableAutoStopRequest ( DMA\_Type \* *base*, uint32\_t *channel*, bool *enable* ) [inline], [static]**

If enabling the auto stop request, the eDMA hardware automatically disables the hardware channel request.

### Parameters

|                |                                                  |
|----------------|--------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                    |
| <i>channel</i> | eDMA channel number.                             |
| <i>enable</i>  | The command to enable (true) or disable (false). |

**12.7.13 void EDMA\_EnableChannelInterrupts ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )**

### Parameters

|                |                                                                                                     |
|----------------|-----------------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                       |
| <i>channel</i> | eDMA channel number.                                                                                |
| <i>mask</i>    | The mask of interrupt source to be set. Users need to use the defined edma_interrupt-enable_t type. |



**12.7.14** void EDMA\_DisableChannelInterrupts ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )

## Function Documentation

### Parameters

|                |                                                                                                        |
|----------------|--------------------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                          |
| <i>channel</i> | eDMA channel number.                                                                                   |
| <i>mask</i>    | The mask of the interrupt source to be set. Use the defined <code>edma_interrupt_enable_t</code> type. |

### 12.7.15 void EDMA\_TcdReset ( edma\_tcd\_t \* *tcd* )

This function sets all fields for this TCD structure to default value.

### Parameters

|            |                               |
|------------|-------------------------------|
| <i>tcd</i> | Pointer to the TCD structure. |
|------------|-------------------------------|

### Note

This function enables the auto stop request feature.

### 12.7.16 void EDMA\_TcdSetTransferConfig ( edma\_tcd\_t \* *tcd*, const edma\_transfer\_config\_t \* *config*, edma\_tcd\_t \* *nextTcd* )

The TCD is a transfer control descriptor. The content of the TCD is the same as the hardware TCD registers. The STCD is used in the scatter-gather mode. This function configures the TCD transfer attribute, including source address, destination address, transfer size, address offset, and so on. It also configures the scatter gather feature if the user supplies the next TCD address. Example:

```
*  edma_transfer_t config = {
*  ...
*  }
*  edma_tcd_t tcd __aligned(32);
*  edma_tcd_t nextTcd __aligned(32);
*  EDMA_TcdSetTransferConfig(&tcd, &config, &nextTcd);
*
```

### Parameters

|                |                                                                                                          |
|----------------|----------------------------------------------------------------------------------------------------------|
| <i>tcd</i>     | Pointer to the TCD structure.                                                                            |
| <i>config</i>  | Pointer to eDMA transfer configuration structure.                                                        |
| <i>nextTcd</i> | Pointer to the next TCD structure. It can be NULL if users do not want to enable scatter/gather feature. |

## Note

TCD address should be 32 bytes aligned or it causes an eDMA error.

If the nextTcd is not NULL, the scatter gather feature is enabled and DREQ bit is cleared in the previous transfer configuration, which is set in the EDMA\_TcdReset.

### 12.7.17 void EDMA\_TcdSetMinorOffsetConfig ( edma\_tcd\_t \* *tcd*, const edma\_minor\_offset\_config\_t \* *config* )

A minor offset is a signed-extended value added to the source address or a destination address after each minor loop.

## Parameters

|               |                                                        |
|---------------|--------------------------------------------------------|
| <i>tcd</i>    | A point to the TCD structure.                          |
| <i>config</i> | A pointer to the minor offset configuration structure. |

### 12.7.18 void EDMA\_TcdSetChannelLink ( edma\_tcd\_t \* *tcd*, edma\_channel\_link\_type\_t *type*, uint32\_t *linkedChannel* )

This function configures either a minor link or a major link. The minor link means the channel link is triggered every time CITER decreases by 1. The major link means that the channel link is triggered when the CITER is exhausted.

## Function Documentation

### Note

Users should ensure that DONE flag is cleared before calling this interface, or the configuration is invalid.

### Parameters

|                      |                                                                                                                                                           |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>tcd</i>           | Point to the TCD structure.                                                                                                                               |
| <i>type</i>          | Channel link type, it can be one of: <ul style="list-style-type: none"><li>• kEDMA_LinkNone</li><li>• kEDMA_MinorLink</li><li>• kEDMA_MajorLink</li></ul> |
| <i>linkedChannel</i> | The linked channel number.                                                                                                                                |

### 12.7.19 static void EDMA\_TcdSetBandWidth ( edma\_tcd\_t \* *tcd*, edma\_bandwidth\_t *bandWidth* ) [inline], [static]

Because the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. The bandwidth forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch.

### Parameters

|                  |                                                                                                                                                                                                           |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>tcd</i>       | A pointer to the TCD structure.                                                                                                                                                                           |
| <i>bandWidth</i> | A bandwidth setting, which can be one of the following: <ul style="list-style-type: none"><li>• kEDMABandwidthStallNone</li><li>• kEDMABandwidthStall4Cycle</li><li>• kEDMABandwidthStall8Cycle</li></ul> |

### 12.7.20 void EDMA\_TcdSetModulo ( edma\_tcd\_t \* *tcd*, edma\_modulo\_t *srcModulo*, edma\_modulo\_t *destModulo* )

This function defines a specific address range specified to be the value after (SADDR + SOFF)/(DADDR + DOFF) calculation is performed or the original register value. It provides the ability to implement a circular data queue easily.

## Parameters

|                   |                                 |
|-------------------|---------------------------------|
| <i>tcd</i>        | A pointer to the TCD structure. |
| <i>srcModulo</i>  | A source modulo value.          |
| <i>destModulo</i> | A destination modulo value.     |

### 12.7.21 static void EDMA\_TcdEnableAutoStopRequest ( edma\_tcd\_t \* *tcd*, bool *enable* ) [inline], [static]

If enabling the auto stop request, the eDMA hardware automatically disables the hardware channel request.

## Parameters

|               |                                                  |
|---------------|--------------------------------------------------|
| <i>tcd</i>    | A pointer to the TCD structure.                  |
| <i>enable</i> | The command to enable (true) or disable (false). |

### 12.7.22 void EDMA\_TcdEnableInterrupts ( edma\_tcd\_t \* *tcd*, uint32\_t *mask* )

## Parameters

|             |                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------|
| <i>tcd</i>  | Point to the TCD structure.                                                                         |
| <i>mask</i> | The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type. |

### 12.7.23 void EDMA\_TcdDisableInterrupts ( edma\_tcd\_t \* *tcd*, uint32\_t *mask* )

## Parameters

|             |                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------|
| <i>tcd</i>  | Point to the TCD structure.                                                                         |
| <i>mask</i> | The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type. |

### 12.7.24 static void EDMA\_EnableChannelRequest ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function enables the hardware channel request.

## Function Documentation

### Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

### 12.7.25 static void EDMA\_DisableChannelRequest ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function disables the hardware channel request.

### Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

### 12.7.26 static void EDMA\_TriggerChannelStart ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function starts a minor loop transfer.

### Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

### 12.7.27 uint32\_t EDMA\_GetRemainingMajorLoopCount ( DMA\_Type \* *base*, uint32\_t *channel* )

This function checks the TCD (Task Control Descriptor) status for a specified eDMA channel and returns the the number of major loop count that has not finished.

### Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

### Returns

Major loop count which has not been transferred yet for the current TCD.

## Note

1. This function can only be used to get unfinished major loop count of transfer without the next TCD, or it might be inaccuracy.
1. The unfinished/remaining transfer bytes cannot be obtained directly from registers while the channel is running. Because to calculate the remaining bytes, the initial NBYTES configured in DMA\_TCDn\_NBYTES\_MLNO register is needed while the eDMA IP does not support getting it while a channel is active. In another word, the NBYTES value reading is always the actual (decrementing) NBYTES value the dma\_engine is working with while a channel is running. Consequently, to get the remaining transfer bytes, a software-saved initial value of NBYTES (for example copied before enabling the channel) is needed. The formula to calculate it is shown below:  $\text{RemainingBytes} = \text{RemainingMajorLoopCount} * \text{NBYTES}(\text{initially configured})$

### 12.7.28 static uint32\_t EDMA\_GetErrorStatusFlags ( DMA\_Type \* *base* ) [inline], [static]

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | eDMA peripheral base address. |
|-------------|-------------------------------|

## Returns

The mask of error status flags. Users need to use the `_edma_error_status_flags` type to decode the return variables.

### 12.7.29 uint32\_t EDMA\_GetChannelStatusFlags ( DMA\_Type \* *base*, uint32\_t *channel* )

## Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

## Returns

The mask of channel status flags. Users need to use the `_edma_channel_status_flags` type to decode the return variables.

### 12.7.30 void EDMA\_ClearChannelStatusFlags ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )

## Function Documentation

### Parameters

|                |                                                                                                                       |
|----------------|-----------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                                         |
| <i>channel</i> | eDMA channel number.                                                                                                  |
| <i>mask</i>    | The mask of channel status to be cleared. Users need to use the defined <code>_edma_channel_status_flags</code> type. |

### 12.7.31 void EDMA\_CreateHandle ( edma\_handle\_t \* *handle*, DMA\_Type \* *base*, uint32\_t *channel* )

This function is called if using the transactional API for eDMA. This function initializes the internal state of the eDMA handle.

### Parameters

|                |                                                                               |
|----------------|-------------------------------------------------------------------------------|
| <i>handle</i>  | eDMA handle pointer. The eDMA handle stores callback function and parameters. |
| <i>base</i>    | eDMA peripheral base address.                                                 |
| <i>channel</i> | eDMA channel number.                                                          |

### 12.7.32 void EDMA\_InstallTCDDMemory ( edma\_handle\_t \* *handle*, edma\_tcd\_t \* *tcdPool*, uint32\_t *tcdSize* )

This function is called after the EDMA\_CreateHandle to use scatter/gather feature.

### Parameters

|                |                                                           |
|----------------|-----------------------------------------------------------|
| <i>handle</i>  | eDMA handle pointer.                                      |
| <i>tcdPool</i> | A memory pool to store TCDs. It must be 32 bytes aligned. |
| <i>tcdSize</i> | The number of TCD slots.                                  |

### 12.7.33 void EDMA\_SetCallback ( edma\_handle\_t \* *handle*, edma\_callback *callback*, void \* *userData* )

This callback is called in the eDMA IRQ handler. Use the callback to do something after the current major loop transfer completes.



## Parameters

|                 |                                        |
|-----------------|----------------------------------------|
| <i>handle</i>   | eDMA handle pointer.                   |
| <i>callback</i> | eDMA callback function pointer.        |
| <i>userData</i> | A parameter for the callback function. |

**12.7.34 void EDMA\_PrepareTransfer ( edma\_transfer\_config\_t \* *config*, void \* *srcAddr*, uint32\_t *srcWidth*, void \* *destAddr*, uint32\_t *destWidth*, uint32\_t *bytesEachRequest*, uint32\_t *transferBytes*, edma\_transfer\_type\_t *type* )**

This function prepares the transfer configuration structure according to the user input.

## Parameters

|                         |                                                           |
|-------------------------|-----------------------------------------------------------|
| <i>config</i>           | The user configuration structure of type edma_transfer_t. |
| <i>srcAddr</i>          | eDMA transfer source address.                             |
| <i>srcWidth</i>         | eDMA transfer source address width(bytes).                |
| <i>destAddr</i>         | eDMA transfer destination address.                        |
| <i>destWidth</i>        | eDMA transfer destination address width(bytes).           |
| <i>bytesEachRequest</i> | eDMA transfer bytes per channel request.                  |
| <i>transferBytes</i>    | eDMA transfer bytes to be transferred.                    |
| <i>type</i>             | eDMA transfer type.                                       |

## Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error (SAE).

**12.7.35 status\_t EDMA\_SubmitTransfer ( edma\_handle\_t \* *handle*, const edma\_transfer\_config\_t \* *config* )**

This function submits the eDMA transfer request according to the transfer configuration structure. If submitting the transfer request repeatedly, this function packs an unprocessed request as a TCD and enables scatter/gather feature to process it in the next time.

## Function Documentation

### Parameters

|               |                                                   |
|---------------|---------------------------------------------------|
| <i>handle</i> | eDMA handle pointer.                              |
| <i>config</i> | Pointer to eDMA transfer configuration structure. |

### Return values

|                                |                                                                     |
|--------------------------------|---------------------------------------------------------------------|
| <i>kStatus_EDMA_Success</i>    | It means submit transfer request succeed.                           |
| <i>kStatus_EDMA_Queue-Full</i> | It means TCD queue is full. Submit transfer request is not allowed. |
| <i>kStatus_EDMA_Busy</i>       | It means the given channel is busy, need to submit request later.   |

### 12.7.36 void EDMA\_StartTransfer ( edma\_handle\_t \* *handle* )

This function enables the channel request. Users can call this function after submitting the transfer request or before submitting the transfer request.

#### Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | eDMA handle pointer. |
|---------------|----------------------|

### 12.7.37 void EDMA\_StopTransfer ( edma\_handle\_t \* *handle* )

This function disables the channel request to pause the transfer. Users can call [EDMA\\_StartTransfer\(\)](#) again to resume the transfer.

#### Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | eDMA handle pointer. |
|---------------|----------------------|

### 12.7.38 void EDMA\_AbortTransfer ( edma\_handle\_t \* *handle* )

This function disables the channel request and clear transfer status bits. Users can submit another transfer after calling this API.

## Parameters

|               |                     |
|---------------|---------------------|
| <i>handle</i> | DMA handle pointer. |
|---------------|---------------------|

**12.7.39 void EDMA\_HandleIRQ ( edma\_handle\_t \* *handle* )**

This function clears the channel major interrupt flag and calls the callback function if it is not NULL.

Note: For the case using TCD queue, when the major iteration count is exhausted, additional operations are performed. These include the final address adjustments and reloading of the BITER field into the CITER. Assertion of an optional interrupt request also occurs at this time, as does a possible fetch of a new TCD from memory using the scatter/gather address pointer included in the descriptor (if scatter/gather is enabled).

For instance, when the time interrupt of TCD[0] happens, the TCD[1] has already been loaded into the eDMA engine. As sga and sga\_index are calculated based on the DLAST\_SGA bitfield lies in the TCD\_CSR register, the sga\_index in this case should be 2 (DLAST\_SGA of TCD[1] stores the address of TCD[2]). Thus, the "tcdUsed" updated should be (tcdUsed - 2U) which indicates the number of TCDs can be loaded in the memory pool (because TCD[0] and TCD[1] have been loaded into the eDMA engine at this point already.).

For the last two continuous ISRs in a scatter/gather process, they both load the last TCD (The last ISR does not load a new TCD) from the memory pool to the eDMA engine when major loop completes. Therefore, ensure that the header and tcdUsed updated are identical for them. tcdUsed are both 0 in this case as no TCD to be loaded.

See the "eDMA basic data flow" in the eDMA Functional description part of the Reference Manual for further details.

## Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | eDMA handle pointer. |
|---------------|----------------------|



## Chapter 13

# ENET: Ethernet MAC Driver

### 13.1 Overview

The KSDK provides a peripheral driver for the 10/100 Mbps Ethernet MAC (ENET) module of Kinetis devices.

The MII interface is the interface connected with MAC and PHY. the Serial management interface - MII management interface should be set before any access to the external PHY chip register. Call [ENET\\_SetSMI\(\)](#) to initialize MII management interface. Use [ENET\\_StartSMIRead\(\)](#), [ENET\\_StartSMIWrite\(\)](#), and [ENET\\_ReadSMIData\(\)](#) to read/write to PHY registers. This function group sets up the MII and serial management SMI interface, gets data from the SMI interface, and starts the SMI read and write command. Use [ENET\\_SetMII\(\)](#) to configure the MII before successfully getting data from the external PHY.

This group sets/gets the ENET mac address and the multicast group address filter. [ENET\\_AddMulticastGroup\(\)](#) should be called to add the ENET MAC to the multicast group. The IEEE 1588 feature requires receiving the PTP message.

For ENET receive, the [ENET\\_GetRxFrameSize\(\)](#) function must be called to get the received data size. Then, call the [ENET\\_ReadFrame\(\)](#) function to get the received data. If the received error occurs, call the [ENET\\_GetRxErrBeforeReadFrame\(\)](#) function after [ENET\\_GetRxFrameSize\(\)](#) and before [ENET\\_ReadFrame\(\)](#) functions to get the detailed error information.

For ENET transmit, call the [ENET\\_SendFrame\(\)](#) function to send the data out. The transmit data error information is only accessible for the IEEE 1588 enhanced buffer descriptor mode. When the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` is defined, the [ENET\\_GetTxErrAfterSendFrame\(\)](#) can be used to get the detail transmit error information. The transmit error information can only be updated by uDMA after the data is transmitted. The [ENET\\_GetTxErrAfterSendFrame\(\)](#) function is recommended to be called on the transmit interrupt handler.

This function group configures the PTP IEEE 1588 feature, starts/stops/gets/sets/adjusts the PTP IEEE 1588 timer, gets the receive/transmit frame timestamp, and PTP IEEE 1588 timer channel feature setting.

The [ENET\\_Ptp1588Configure\(\)](#) function must be called when the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` is defined and the IEEE 1588 feature is required. The [ENET\\_GetRxFrameTime\(\)](#) and [ENET\\_GetTxFrameTime\(\)](#) functions are called by the PTP stack to get the timestamp captured by the ENET driver.

### 13.2 Typical use case

#### 13.2.1 ENET Initialization, receive, and transmit operations

For the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` undefined use case, use the legacy type buffer descriptor transmit/receive the frame as follows.

## Typical use case

```
enet_config_t config;
uint32_t length = 0;
uint32_t sysClock;
uint32_t phyAddr = 0;
bool link = false;
phy_speed_t speed;
phy_duplex_t duplex;
enet_status_t result;
enet_data_error_stats_t eErrorStatic;
// Prepares the buffer configuration.
enet_buffer_config_t buffCfg =
{
    ENET_RXBD_NUM,
    ENET_TXBD_NUM,
    ENET_BuffSizeAlign(ENET_RXBUFF_SIZE),
    ENET_BuffSizeAlign(ENET_TXBUFF_SIZE),
    &RxBuffDescrip[0], // Prepare buffers
    &TxBuffDescrip[0], // Prepare buffers
    &RxDataBuff[0][0], // Prepare buffers
    &TxDataBuff[0][0], // Prepare buffers
};

sysClock = CLOCK_GetFreq(kCLOCK_CoreSysClk);

// Gets the default configuration.
ENET_GetDefaultConfig(&config);
PHY_Init(EXAMPLE_ENET, 0, sysClock);
// Changes the link status to PHY auto-negotiated link status.
PHY_GetLinkStatus(EXAMPLE_ENET, phyAddr, &link);
if (link)
{
    PHY_GetLinkSpeedDuplex(EXAMPLE_ENET, phyAddr, &speed, &duplex);
    config.miiSpeed = (enet_mii_speed_t)speed;
    config.miiDuplex = (enet_mii_duplex_t)duplex;
}
ENET_Init(EXAMPLE_ENET, &handle, &config, &buffCfg, &macAddr[0], sysClock);
ENET_ActiveRead(EXAMPLE_ENET);

while (1)
{
    // Gets the frame size.
    result = ENET_GetRxFrameSize(&handle, &length);
    // Calls the ENET_ReadFrame when there is a received frame.
    if (length != 0)
    {
        // Receives a valid frame and delivers the receive buffer with the size equal to length.
        uint8_t *data = (uint8_t *)malloc(length);
        ENET_ReadFrame(EXAMPLE_ENET, &handle, data, length);
        // Delivers the data to the upper layer.
        .....
        free(data);
    }
    else if (result == kStatus_ENET_RxFrameErr)
    {
        // Updates the received buffer when an error occurs.
        ENET_GetRxErrBeforeReadFrame(&handle, &eErrStatic);
        // Updates the receive buffer.
        ENET_ReadFrame(EXAMPLE_ENET, &handle, NULL, 0);
    }

    // Sends a multicast frame when the PHY is linked up.
    if (kStatus_Success == PHY_GetLinkStatus(EXAMPLE_ENET, phyAddr, &link))
    {
        if (link)
        {
            ENET_SendFrame(EXAMPLE_ENET, &handle, &frame[0], ENET_DATA_LENGTH);
        }
    }
}
```

```
}

```

For the ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE defined use case, add the PTP IEEE 1588 configuration to enable the PTP IEEE 1588 feature. The initialization occurs as follows.

```
enet_config_t config;
uint32_t length = 0;
uint32_t sysClock;
uint32_t phyAddr = 0;
bool link = false;
phy_speed_t speed;
phy_duplex_t duplex;
enet_status_t result;
enet_data_err_stats_t eErrStatic;
enet_buffer_config_t buffCfg =
{
    ENET_RXBD_NUM,
    ENET_TXBD_NUM,
    ENET_BuffSizeAlign(ENET_RXBUFF_SIZE),
    ENET_BuffSizeAlign(ENET_TXBUFF_SIZE),
    &RxBuffDescrip[0],
    &TxBuffDescrip[0],
    &RxDataBuff[0][0],
    &TxDataBuff[0][0],
};

sysClock = CLOCK_GetFreq(kCLOCK_CoreSysClk);

// Sets the PTP 1588 source.
CLOCK_SetEnetTime0Clock(2);
ptpClock = CLOCK_GetFreq(kCLOCK_Osc0ErClk);
// Prepares the PTP configuration.
enet_ptp_config_t ptpConfig =
{
    ENET_RXBD_NUM,
    ENET_TXBD_NUM,
    &g_rxPtpTsBuff[0],
    &g_txPtpTsBuff[0],
    kENET_PtpTimerChannell1,
    ptpClock,
};

// Gets the default configuration.
ENET_GetDefaultConfig(&config);

PHY_Init(EXAMPLE_ENET, 0, sysClock);
// Changes the link status to PHY auto-negotiated link status.
PHY_GetLinkStatus(EXAMPLE_ENET, phyAddr, &link);
if (link)
{
    PHY_GetLinkSpeedDuplex(EXAMPLE_ENET, phyAddr, &speed, &duplex);
    config.miiSpeed = (enet_mii_speed_t) speed;
    config.miiDuplex = (enet_mii_duplex_t) duplex;
}

ENET_Init(EXAMPLE_ENET, &handle, &config, &buffCfg, &macAddr[0], sysClock);

// Configures the PTP 1588 feature.
ENET_Ptp1588Configure(EXAMPLE_ENET, &handle, &ptpConfig);
// Adds the device to the PTP multicast group.
ENET_AddMulticastGroup(EXAMPLE_ENET, &mGAddr[0]);

ENET_ActiveRead(EXAMPLE_ENET);
```

## Typical use case

## Data Structures

- struct [enet\\_rx\\_bd\\_struct\\_t](#)  
*Defines the receive buffer descriptor structure for the little endian system. [More...](#)*
- struct [enet\\_tx\\_bd\\_struct\\_t](#)  
*Defines the enhanced transmit buffer descriptor structure for the little endian system. [More...](#)*
- struct [enet\\_data\\_error\\_stats\\_t](#)  
*Defines the ENET data error statistic structure. [More...](#)*
- struct [enet\\_buffer\\_config\\_t](#)  
*Defines the receive buffer descriptor configuration structure. [More...](#)*
- struct [enet\\_config\\_t](#)  
*Defines the basic configuration structure for the ENET device. [More...](#)*
- struct [enet\\_handle\\_t](#)  
*Defines the ENET handler structure. [More...](#)*

## Macros

- #define [ENET\\_BUFFDESCRIPTOR\\_RX\\_ERR\\_MASK](#)  
*Defines the receive error status flag mask.*
- #define [ENET\\_FIFO\\_MIN\\_RX\\_FULL](#) 5U  
*ENET minimum receive FIFO full.*
- #define [ENET\\_RX\\_MIN\\_BUFFERSIZE](#) 256U  
*ENET minimum buffer size.*
- #define [ENET\\_BUFF\\_ALIGNMENT](#) 16U  
*Ethernet buffer alignment.*
- #define [ENET\\_PHY\\_MAXADDRESS](#) (ENET\_MMFR\_PA\_MASK >> ENET\_MMFR\_PA\_SHIFT)  
*Defines the PHY address scope for the ENET.*

## Typedefs

- typedef void(\* [enet\\_callback\\_t](#))(ENET\_Type \*base, enet\_handle\_t \*handle, [enet\\_event\\_t](#) event, void \*userData)  
*ENET callback function.*

## Enumerations

- enum [\\_enet\\_status](#) {  
    [kStatus\\_ENET\\_RxFrameError](#) = MAKE\_STATUS(kStatusGroup\_ENET, 0U),  
    [kStatus\\_ENET\\_RxFrameFail](#) = MAKE\_STATUS(kStatusGroup\_ENET, 1U),  
    [kStatus\\_ENET\\_RxFrameEmpty](#) = MAKE\_STATUS(kStatusGroup\_ENET, 2U),  
    [kStatus\\_ENET\\_TxFrameBusy](#),  
    [kStatus\\_ENET\\_TxFrameFail](#) = MAKE\_STATUS(kStatusGroup\_ENET, 4U) }  
*Defines the status return codes for transaction.*
- enum [enet\\_mii\\_mode\\_t](#) {  
    [kENET\\_MiiMode](#) = 0U,  
    [kENET\\_RmiiMode](#) }  
*Defines the RMII or MII mode for data interface between the MAC and the PHY.*



- enum `enet_mii_speed_t` {  
`kENET_MiiSpeed10M` = 0U,  
`kENET_MiiSpeed100M` }  
*Defines the 10 Mbps or 100 Mbps speed for the MII data interface.*
- enum `enet_mii_duplex_t` {  
`kENET_MiiHalfDuplex` = 0U,  
`kENET_MiiFullDuplex` }  
*Defines the half or full duplex for the MII data interface.*
- enum `enet_mii_write_t` {  
`kENET_MiiWriteNoCompliant` = 0U,  
`kENET_MiiWriteValidFrame` }  
*Defines the write operation for the MII management frame.*
- enum `enet_mii_read_t` {  
`kENET_MiiReadValidFrame` = 2U,  
`kENET_MiiReadNoCompliant` = 3U }  
*Defines the read operation for the MII management frame.*
- enum `enet_special_control_flag_t` {  
`kENET_ControlFlowControlEnable` = 0x0001U,  
`kENET_ControlRxPayloadCheckEnable` = 0x0002U,  
`kENET_ControlRxPadRemoveEnable` = 0x0004U,  
`kENET_ControlRxBroadCastRejectEnable` = 0x0008U,  
`kENET_ControlMacAddrInsert` = 0x0010U,  
`kENET_ControlStoreAndFwdDisable` = 0x0020U,  
`kENET_ControlSMIPreambleDisable` = 0x0040U,  
`kENET_ControlPromiscuousEnable` = 0x0080U,  
`kENET_ControlMIILoopEnable` = 0x0100U,  
`kENET_ControlVLANTagEnable` = 0x0200U }  
*Defines a special configuration for ENET MAC controller.*
- enum `enet_interrupt_enable_t` {  
`kENET_BabrInterrupt` = ENET\_EIR\_BABR\_MASK,  
`kENET_BabtInterrupt` = ENET\_EIR\_BABT\_MASK,  
`kENET_GraceStopInterrupt` = ENET\_EIR\_GRA\_MASK,  
`kENET_TxFrameInterrupt` = ENET\_EIR\_TXF\_MASK,  
`kENET_TxBufferInterrupt` = ENET\_EIR\_TXB\_MASK,  
`kENET_RxFrameInterrupt` = ENET\_EIR\_RXF\_MASK,  
`kENET_RxBufferInterrupt` = ENET\_EIR\_RXB\_MASK,  
`kENET_MiiInterrupt` = ENET\_EIR\_MII\_MASK,  
`kENET_EBusERInterrupt` = ENET\_EIR\_EBERR\_MASK,  
`kENET_LateCollisionInterrupt` = ENET\_EIR\_LC\_MASK,  
`kENET_RetryLimitInterrupt` = ENET\_EIR\_RL\_MASK,  
`kENET_UnderrunInterrupt` = ENET\_EIR\_UN\_MASK,  
`kENET_PayloadRxInterrupt` = ENET\_EIR\_PLR\_MASK,  
`kENET_WakeupInterrupt` = ENET\_EIR\_WAKEUP\_MASK }  
*List of interrupts supported by the peripheral.*
- enum `enet_event_t` {

## Typical use case

```
kENET_RxEvent,  
kENET_TxEvent,  
kENET_ErrEvent,  
kENET_WakeUpEvent }
```

*Defines the common interrupt event for callback use.*

- enum `enet_tx_accelerator_t` {  
    `kENET_TxAccelIsShift16Enabled` = `ENET_TACC_SHIFT16_MASK`,  
    `kENET_TxAccelIpCheckEnabled` = `ENET_TACC_IPCHK_MASK`,  
    `kENET_TxAccelProtoCheckEnabled` = `ENET_TACC_PROCHK_MASK` }

*Defines the transmit accelerator configuration.*

- enum `enet_rx_accelerator_t` {  
    `kENET_RxAccelPadRemoveEnabled` = `ENET_RACC_PADREM_MASK`,  
    `kENET_RxAccelIpCheckEnabled` = `ENET_RACC_IPDIS_MASK`,  
    `kENET_RxAccelProtoCheckEnabled` = `ENET_RACC_PRODIS_MASK`,  
    `kENET_RxAccelMacCheckEnabled` = `ENET_RACC_LINEDIS_MASK`,  
    `kENET_RxAccelIsShift16Enabled` = `ENET_RACC_SHIFT16_MASK` }

*Defines the receive accelerator configuration.*

## Driver version

- #define `FSL_ENET_DRIVER_VERSION` (`MAKE_VERSION`(2, 0, 1))  
*Defines the driver version.*

## Control and status region bit masks of the receive buffer descriptor.

- #define `ENET_BUFFDESCRIPTOR_RX_EMPTY_MASK` 0x8000U  
*Empty bit mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_SOFTOWNER1_MASK` 0x4000U  
*Software owner one mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_WRAP_MASK` 0x2000U  
*Next buffer descriptor is the start address.*
- #define `ENET_BUFFDESCRIPTOR_RX_SOFTOWNER2_Mask` 0x1000U  
*Software owner two mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_LAST_MASK` 0x0800U  
*Last BD of the frame mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_MISS_MASK` 0x0100U  
*Received because of the promiscuous mode.*
- #define `ENET_BUFFDESCRIPTOR_RX_BROADCAST_MASK` 0x0080U  
*Broadcast packet mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_MULTICAST_MASK` 0x0040U  
*Multicast packet mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_LENVIOLATE_MASK` 0x0020U  
*Length violation mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_NOOCTET_MASK` 0x0010U  
*Non-octet aligned frame mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_CRC_MASK` 0x0004U  
*CRC error mask.*
- #define `ENET_BUFFDESCRIPTOR_RX_OVERRUN_MASK` 0x0002U  
*FIFO overrun mask.*

- #define `ENET_BUFFDESCRIPTOR_RX_TRUNC_MASK` 0x0001U  
*Frame is truncated mask.*

## Control and status bit masks of the transmit buffer descriptor.

- #define `ENET_BUFFDESCRIPTOR_TX_READY_MASK` 0x8000U  
*Ready bit mask.*
- #define `ENET_BUFFDESCRIPTOR_TX_SOFTOWNER1_MASK` 0x4000U  
*Software owner one mask.*
- #define `ENET_BUFFDESCRIPTOR_TX_WRAP_MASK` 0x2000U  
*Wrap buffer descriptor mask.*
- #define `ENET_BUFFDESCRIPTOR_TX_SOFTOWNER2_MASK` 0x1000U  
*Software owner two mask.*
- #define `ENET_BUFFDESCRIPTOR_TX_LAST_MASK` 0x0800U  
*Last BD of the frame mask.*
- #define `ENET_BUFFDESCRIPTOR_TX_TRANMITCRC_MASK` 0x0400U  
*Transmit CRC mask.*

## Defines the maximum Ethernet frame size.

- #define `ENET_FRAME_MAX_FRAMELEN` 1518U  
*Maximum Ethernet frame size.*
- #define `ENET_FRAME_MAX_VALNFRAMELEN` 1522U  
*Maximum VLAN frame size.*

## Initialization and de-initialization

- void `ENET_GetDefaultConfig` (`enet_config_t` \*config)  
*Gets the ENET default configuration structure.*
- void `ENET_Init` (`ENET_Type` \*base, `enet_handle_t` \*handle, const `enet_config_t` \*config, const `enet_buffer_config_t` \*bufferConfig, `uint8_t` \*macAddr, `uint32_t` srcClock\_Hz)  
*Initializes the ENET module.*
- void `ENET_Deinit` (`ENET_Type` \*base)  
*Deinitializes the ENET module.*
- static void `ENET_Reset` (`ENET_Type` \*base)  
*Resets the ENET module.*

## MII interface operation

- void `ENET_SetMII` (`ENET_Type` \*base, `enet_mii_speed_t` speed, `enet_mii_duplex_t` duplex)  
*Sets the ENET MII speed and duplex.*
- void `ENET_SetSMI` (`ENET_Type` \*base, `uint32_t` srcClock\_Hz, bool isPreambleDisabled)  
*Sets the ENET SMI (serial management interface) - MII management interface.*
- static bool `ENET_GetSMI` (`ENET_Type` \*base)  
*Gets the ENET SMI- MII management interface configuration.*
- static `uint32_t` `ENET_ReadSMIData` (`ENET_Type` \*base)  
*Reads data from the PHY register through an SMI interface.*
- void `ENET_StartSMIRead` (`ENET_Type` \*base, `uint32_t` phyAddr, `uint32_t` phyReg, `enet_mii_read_t` operation)  
*Starts an SMI (Serial Management Interface) read command.*

## Typical use case

- void [ENET\\_StartSMIWrite](#) (ENET\_Type \*base, uint32\_t phyAddr, uint32\_t phyReg, [enet\\_mii\\_write\\_t](#) operation, uint32\_t data)  
*Starts an SMI write command.*

## MAC Address Filter

- void [ENET\\_SetMacAddr](#) (ENET\_Type \*base, uint8\_t \*macAddr)  
*Sets the ENET module Mac address.*
- void [ENET\\_GetMacAddr](#) (ENET\_Type \*base, uint8\_t \*macAddr)  
*Gets the ENET module Mac address.*
- void [ENET\\_AddMulticastGroup](#) (ENET\_Type \*base, uint8\_t \*address)  
*Adds the ENET device to a multicast group.*
- void [ENET\\_LeaveMulticastGroup](#) (ENET\_Type \*base, uint8\_t \*address)  
*Moves the ENET device from a multicast group.*

## Other basic operations

- static void [ENET\\_ActiveRead](#) (ENET\_Type \*base)  
*Activates ENET read or receive.*
- static void [ENET\\_EnableSleepMode](#) (ENET\_Type \*base, bool enable)  
*Enables/disables the MAC to enter sleep mode.*
- static void [ENET\\_GetAccelFunction](#) (ENET\_Type \*base, uint32\_t \*txAccelOption, uint32\_t \*rxAccelOption)  
*Gets ENET transmit and receive accelerator functions from the MAC controller.*

## Interrupts

- static void [ENET\\_EnableInterrupts](#) (ENET\_Type \*base, uint32\_t mask)  
*Enables the ENET interrupt.*
- static void [ENET\\_DisableInterrupts](#) (ENET\_Type \*base, uint32\_t mask)  
*Disables the ENET interrupt.*
- static uint32\_t [ENET\\_GetInterruptStatus](#) (ENET\_Type \*base)  
*Gets the ENET interrupt status flag.*
- static void [ENET\\_ClearInterruptStatus](#) (ENET\_Type \*base, uint32\_t mask)  
*Clears the ENET interrupt events status flag.*

## Transactional operation

- void [ENET\\_SetCallback](#) (enet\_handle\_t \*handle, [enet\\_callback\\_t](#) callback, void \*userData)  
*Sets the callback function.*
- void [ENET\\_GetRxErrBeforeReadFrame](#) (enet\_handle\_t \*handle, [enet\\_data\\_error\\_stats\\_t](#) \*eError-Static)  
*Gets the ENET the error statistics of a received frame.*
- status\_t [ENET\\_GetRxFrameSize](#) (enet\_handle\_t \*handle, uint32\_t \*length)  
*Gets the size of the read frame.*
- status\_t [ENET\\_ReadFrame](#) (ENET\_Type \*base, enet\_handle\_t \*handle, uint8\_t \*data, uint32\_t length)  
*Reads a frame from the ENET device.*
- status\_t [ENET\\_SendFrame](#) (ENET\_Type \*base, enet\_handle\_t \*handle, uint8\_t \*data, uint32\_t length)

- *Transmits an ENET frame.*  
void [ENET\\_TransmitIRQHandler](#) (ENET\_Type \*base, enet\_handle\_t \*handle)
- *The transmit IRQ handler.*  
void [ENET\\_ReceiveIRQHandler](#) (ENET\_Type \*base, enet\_handle\_t \*handle)
- *The receive IRQ handler.*  
void [ENET\\_ErrorIRQHandler](#) (ENET\_Type \*base, enet\_handle\_t \*handle)
- *The error IRQ handler.*

## 13.3 Data Structure Documentation

### 13.3.1 struct enet\_rx\_bd\_struct\_t

#### Data Fields

- uint16\_t [length](#)  
*Buffer descriptor data length.*
- uint16\_t [control](#)  
*Buffer descriptor control and status.*
- uint8\_t \* [buffer](#)  
*Data buffer pointer.*

#### 13.3.1.0.0.29 Field Documentation

13.3.1.0.0.29.1 uint16\_t enet\_rx\_bd\_struct\_t::length

13.3.1.0.0.29.2 uint16\_t enet\_rx\_bd\_struct\_t::control

13.3.1.0.0.29.3 uint8\_t\* enet\_rx\_bd\_struct\_t::buffer

### 13.3.2 struct enet\_tx\_bd\_struct\_t

#### Data Fields

- uint16\_t [length](#)  
*Buffer descriptor data length.*
- uint16\_t [control](#)  
*Buffer descriptor control and status.*
- uint8\_t \* [buffer](#)  
*Data buffer pointer.*

## Data Structure Documentation

### 13.3.2.0.0.30 Field Documentation

13.3.2.0.0.30.1 `uint16_t enet_tx_bd_struct_t::length`

13.3.2.0.0.30.2 `uint16_t enet_tx_bd_struct_t::control`

13.3.2.0.0.30.3 `uint8_t* enet_tx_bd_struct_t::buffer`

### 13.3.3 `struct enet_data_error_stats_t`

#### Data Fields

- `uint32_t statsRxLenGreaterErr`  
*Receive length greater than RCR[MAX\_FL].*
- `uint32_t statsRxAlignErr`  
*Receive non-octet alignment/.*
- `uint32_t statsRxFcsErr`  
*Receive CRC error.*
- `uint32_t statsRxOverRunErr`  
*Receive over run.*
- `uint32_t statsRxTruncateErr`  
*Receive truncate.*

### 13.3.3.0.0.31 Field Documentation

13.3.3.0.0.31.1 `uint32_t enet_data_error_stats_t::statsRxLenGreaterErr`

13.3.3.0.0.31.2 `uint32_t enet_data_error_stats_t::statsRxFcsErr`

13.3.3.0.0.31.3 `uint32_t enet_data_error_stats_t::statsRxOverRunErr`

13.3.3.0.0.31.4 `uint32_t enet_data_error_stats_t::statsRxTruncateErr`

### 13.3.4 `struct enet_buffer_config_t`

Note that for the internal DMA requirements, the buffers have a corresponding alignment requirements.

1. The aligned receive and transmit buffer size must be evenly divisible by 16.
2. The aligned transmit and receive buffer descriptor start address must be at least 64 bit aligned. However, it's recommended to be evenly divisible by 16.
3. The aligned transmit and receive buffer start address must be evenly divisible by 16. Receive buffers should be continuous with the total size equal to "`rxBdNumber * rxBuffSizeAlign`". Transmit buffers should be continuous with the total size equal to "`txBdNumber * txBuffSizeAlign`".

#### Data Fields

- `uint16_t rxBdNumber`  
*Receive buffer descriptor number.*

- uint16\_t [txBdNumber](#)  
*Transmit buffer descriptor number.*
- uint32\_t [rxBuffSizeAlign](#)  
*Aligned receive data buffer size.*
- uint32\_t [txBuffSizeAlign](#)  
*Aligned transmit data buffer size.*
- volatile [enet\\_rx\\_bd\\_struct\\_t](#) \* [rxBdStartAddrAlign](#)  
*Aligned receive buffer descriptor start address.*
- volatile [enet\\_tx\\_bd\\_struct\\_t](#) \* [txBdStartAddrAlign](#)  
*Aligned transmit buffer descriptor start address.*
- uint8\_t \* [rxBufferAlign](#)  
*Receive data buffer start address.*
- uint8\_t \* [txBufferAlign](#)  
*Transmit data buffer start address.*

#### 13.3.4.0.0.32 Field Documentation

13.3.4.0.0.32.1 uint16\_t enet\_buffer\_config\_t::rxBdNumber

13.3.4.0.0.32.2 uint16\_t enet\_buffer\_config\_t::txBdNumber

13.3.4.0.0.32.3 uint32\_t enet\_buffer\_config\_t::rxBuffSizeAlign

13.3.4.0.0.32.4 uint32\_t enet\_buffer\_config\_t::txBuffSizeAlign

13.3.4.0.0.32.5 volatile enet\_rx\_bd\_struct\_t\* enet\_buffer\_config\_t::rxBdStartAddrAlign

13.3.4.0.0.32.6 volatile enet\_tx\_bd\_struct\_t\* enet\_buffer\_config\_t::txBdStartAddrAlign

13.3.4.0.0.32.7 uint8\_t\* enet\_buffer\_config\_t::rxBufferAlign

13.3.4.0.0.32.8 uint8\_t\* enet\_buffer\_config\_t::txBufferAlign

#### 13.3.5 struct enet\_config\_t

Note:

1. macSpecialConfig is used for a special control configuration, a logical OR of "enet\_special\_control\_flag\_t". For a special configuration for MAC, set this parameter to 0.
2. txWatermark is used for a cut-through operation. It is in steps of 64 bytes. 0/1 - 64 bytes written to TX FIFO before transmission of a frame begins. 2 - 128 bytes written to TX FIFO .... 3 - 192 bytes written to TX FIFO .... The maximum of txWatermark is 0x2F - 4032 bytes written to TX FIFO. txWatermark allows minimizing the transmit latency to set the txWatermark to 0 or 1 or for larger bus access latency 3 or larger due to contention for the system bus.
3. rxFifoFullThreshold is similar to the txWatermark for cut-through operation in RX. It is in 64-bit words. The minimum is ENET\_FIFO\_MIN\_RX\_FULL and the maximum is 0xFF. If the end of the frame is stored in FIFO and the frame size is smaller than the txWatermark, the frame is still transmitted. The rule is the same for rxFifoFullThreshold in the receive direction.
4. When "kENET\_ControlFlowControlEnable" is set in the macSpecialConfig, ensure that the pause-

## Data Structure Documentation

Duration, rxFifoEmptyThreshold, and rxFifoStatEmptyThreshold are set for flow control enabled case.

5. When "kENET\_ControlStoreAndFwdDisabled" is set in the macSpecialConfig, ensure that the rxFifoFullThreshold and txFifoWatermark are set for store and forward disable.
6. The rxAccelerConfig and txAccelerConfig default setting with 0 - accelerator are disabled. The "enet\_tx\_accelerator\_t" and "enet\_rx\_accelerator\_t" are recommended to be used to enable the transmit and receive accelerator. After the accelerators are enabled, the store and forward feature should be enabled. As a result, kENET\_ControlStoreAndFwdDisabled should not be set.

## Data Fields

- uint32\_t [macSpecialConfig](#)  
*Mac special configuration.*
- uint32\_t [interrupt](#)  
*Mac interrupt source.*
- uint16\_t [rxMaxFrameLen](#)  
*Receive maximum frame length.*
- [enet\\_mii\\_mode\\_t](#) [miiMode](#)  
*MII mode.*
- [enet\\_mii\\_speed\\_t](#) [miiSpeed](#)  
*MII Speed.*
- [enet\\_mii\\_duplex\\_t](#) [miiDuplex](#)  
*MII duplex.*
- uint8\_t [rxAccelerConfig](#)  
*Receive accelerator, A logical OR of "enet\_rx\_accelerator\_t".*
- uint8\_t [txAccelerConfig](#)  
*Transmit accelerator, A logical OR of "enet\_tx\_accelerator\_t".*
- uint16\_t [pauseDuration](#)  
*For flow control enabled case: Pause duration.*
- uint8\_t [rxFifoEmptyThreshold](#)  
*For flow control enabled case: when RX FIFO level reaches this value, it makes MAC generate XOFF pause frame.*
- uint8\_t [rxFifoStatEmptyThreshold](#)  
*For flow control enabled case: number of frames in the receive FIFO, independent of size, that can be accept.*
- uint8\_t [rxFifoFullThreshold](#)  
*For store and forward disable case, the data required in RX FIFO to notify the MAC receive ready status.*
- uint8\_t [txFifoWatermark](#)  
*For store and forward disable case, the data required in TX FIFO before a frame transmit start.*

### 13.3.5.0.0.33 Field Documentation

#### 13.3.5.0.0.33.1 uint32\_t enet\_config\_t::macSpecialConfig

A logical OR of "enet\_special\_control\_flag\_t".



**13.3.5.0.0.33.2 uint32\_t enet\_config\_t::interrupt**

A logical OR of "enet\_interrupt\_enable\_t".

**13.3.5.0.0.33.3 uint16\_t enet\_config\_t::rxMaxFrameLen****13.3.5.0.0.33.4 enet\_mii\_mode\_t enet\_config\_t::miiMode****13.3.5.0.0.33.5 enet\_mii\_speed\_t enet\_config\_t::miiSpeed****13.3.5.0.0.33.6 enet\_mii\_duplex\_t enet\_config\_t::miiDuplex****13.3.5.0.0.33.7 uint8\_t enet\_config\_t::rxAccelerConfig****13.3.5.0.0.33.8 uint8\_t enet\_config\_t::txAccelerConfig****13.3.5.0.0.33.9 uint16\_t enet\_config\_t::pauseDuration****13.3.5.0.0.33.10 uint8\_t enet\_config\_t::rxFifoEmptyThreshold****13.3.5.0.0.33.11 uint8\_t enet\_config\_t::rxFifoStatEmptyThreshold**

If the limit is reached, reception continues and a pause frame is triggered.

**13.3.5.0.0.33.12 uint8\_t enet\_config\_t::rxFifoFullThreshold****13.3.5.0.0.33.13 uint8\_t enet\_config\_t::txFifoWatermark****13.3.6 struct \_enet\_handle****Data Fields**

- volatile [enet\\_rx\\_bd\\_struct\\_t](#) \* [rxBdBase](#)  
*Receive buffer descriptor base address pointer.*
- volatile [enet\\_rx\\_bd\\_struct\\_t](#) \* [rxBdCurrent](#)  
*The current available receive buffer descriptor pointer.*
- volatile [enet\\_tx\\_bd\\_struct\\_t](#) \* [txBdBase](#)  
*Transmit buffer descriptor base address pointer.*
- volatile [enet\\_tx\\_bd\\_struct\\_t](#) \* [txBdCurrent](#)  
*The current available transmit buffer descriptor pointer.*
- uint32\_t [rxBuffSizeAlign](#)  
*Receive buffer size alignment.*
- uint32\_t [txBuffSizeAlign](#)  
*Transmit buffer size alignment.*
- [enet\\_callback\\_t](#) [callback](#)  
*Callback function.*
- void \* [userData](#)  
*Callback function parameter.*

## Macro Definition Documentation

### 13.3.6.0.0.34 Field Documentation

13.3.6.0.0.34.1 volatile enet\_rx\_bd\_struct\_t\* enet\_handle\_t::rxBdBase

13.3.6.0.0.34.2 volatile enet\_rx\_bd\_struct\_t\* enet\_handle\_t::rxBdCurrent

13.3.6.0.0.34.3 volatile enet\_tx\_bd\_struct\_t\* enet\_handle\_t::txBdBase

13.3.6.0.0.34.4 volatile enet\_tx\_bd\_struct\_t\* enet\_handle\_t::txBdCurrent

13.3.6.0.0.34.5 uint32\_t enet\_handle\_t::rxBuffSizeAlign

13.3.6.0.0.34.6 uint32\_t enet\_handle\_t::txBuffSizeAlign

13.3.6.0.0.34.7 enet\_callback\_t enet\_handle\_t::callback

13.3.6.0.0.34.8 void\* enet\_handle\_t::userData

## 13.4 Macro Definition Documentation

13.4.1 **#define FSL\_ENET\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))**

Version 2.0.1.



- 13.4.2 **#define ENET\_BUFFDESCRIPTOR\_RX\_EMPTY\_MASK 0x8000U**
- 13.4.3 **#define ENET\_BUFFDESCRIPTOR\_RX\_SOFTOWNER1\_MASK 0x4000U**
- 13.4.4 **#define ENET\_BUFFDESCRIPTOR\_RX\_WRAP\_MASK 0x2000U**
- 13.4.5 **#define ENET\_BUFFDESCRIPTOR\_RX\_SOFTOWNER2\_Mask 0x1000U**
- 13.4.6 **#define ENET\_BUFFDESCRIPTOR\_RX\_LAST\_MASK 0x0800U**
- 13.4.7 **#define ENET\_BUFFDESCRIPTOR\_RX\_MISS\_MASK 0x0100U**
- 13.4.8 **#define ENET\_BUFFDESCRIPTOR\_RX\_BROADCAST\_MASK 0x0080U**
- 13.4.9 **#define ENET\_BUFFDESCRIPTOR\_RX\_MULTICAST\_MASK 0x0040U**
- 13.4.10 **#define ENET\_BUFFDESCRIPTOR\_RX\_LENVIOLATE\_MASK 0x0020U**
- 13.4.11 **#define ENET\_BUFFDESCRIPTOR\_RX\_NOOCTET\_MASK 0x0010U**
- 13.4.12 **#define ENET\_BUFFDESCRIPTOR\_RX\_CRC\_MASK 0x0004U**
- 13.4.13 **#define ENET\_BUFFDESCRIPTOR\_RX\_OVERRUN\_MASK 0x0002U**
- 13.4.14 **#define ENET\_BUFFDESCRIPTOR\_RX\_TRUNC\_MASK 0x0001U**
- 13.4.15 **#define ENET\_BUFFDESCRIPTOR\_TX\_READY\_MASK 0x8000U**
- 13.4.16 **#define ENET\_BUFFDESCRIPTOR\_TX\_SOFTOWENER1\_MASK 0x4000U**
- 13.4.17 **#define ENET\_BUFFDESCRIPTOR\_TX\_WRAP\_MASK 0x2000U**
- 13.4.18 **#define ENET\_BUFFDESCRIPTOR\_TX\_SOFTOWENER2\_MASK 0x1000U**
- 13.4.19 **#define ENET\_BUFFDESCRIPTOR\_TX\_LAST\_MASK 0x0800U**
- 13.4.20 **#define ENET\_BUFFDESCRIPTOR\_TX\_TRANMITCRC\_MASK 0x0400U**
- 13.4.21 **#define ENET\_BUFFDESCRIPTOR\_RX\_ERR\_MASK**

```
(ENET_BUFFDESCRIPTOR_RX_TRUNC_MASK |
 ENET_BUFFDESCRIPTOR_RX_OVERRUN_MASK | \
 ENET_BUFFDESCRIPTOR_RX_LENVIOLATE_MASK |
 ENET_BUFFDESCRIPTOR_RX_NOOCTET_MASK |
 ENET_BUFFDESCRIPTOR_RX_CRC_MASK)
```

**13.4.22 #define ENET\_FRAME\_MAX\_FRAMELEN 1518U**

**13.4.23 #define ENET\_FRAME\_MAX\_VALNFRAMELEN 1522U**

**13.4.24 #define ENET\_FIFO\_MIN\_RX\_FULL 5U**

**13.4.25 #define ENET\_RX\_MIN\_BUFFERSIZE 256U**

**13.4.26 #define ENET\_BUFF\_ALIGNMENT 16U**

**13.4.27 #define ENET\_PHY\_MAXADDRESS (ENET\_MMFR\_PA\_MASK >>  
ENET\_MMFR\_PA\_SHIFT)**

## 13.5 Typedef Documentation

**13.5.1 typedef void(\* enet\_callback\_t)(ENET\_Type \*base, enet\_handle\_t \*handle,  
enet\_event\_t event, void \*userData)**

## 13.6 Enumeration Type Documentation

### 13.6.1 enum \_enet\_status

Enumerator

*kStatus\_ENET\_RxFrameError* A frame received but data error happen.  
*kStatus\_ENET\_RxFrameFail* Failed to receive a frame.  
*kStatus\_ENET\_RxFrameEmpty* No frame arrive.  
*kStatus\_ENET\_TxFrameBusy* Transmit buffer descriptors are under process.  
*kStatus\_ENET\_TxFrameFail* Transmit frame fail.

### 13.6.2 enum enet\_mii\_mode\_t

Enumerator

*kENET\_MiiMode* MII mode for data interface.  
*kENET\_RmiiMode* RMII mode for data interface.

## Enumeration Type Documentation

### 13.6.3 enum enet\_mii\_speed\_t

Enumerator

*kENET\_MiiSpeed10M* Speed 10 Mbps.  
*kENET\_MiiSpeed100M* Speed 100 Mbps.

### 13.6.4 enum enet\_mii\_duplex\_t

Enumerator

*kENET\_MiiHalfDuplex* Half duplex mode.  
*kENET\_MiiFullDuplex* Full duplex mode.

### 13.6.5 enum enet\_mii\_write\_t

Enumerator

*kENET\_MiiWriteNoCompliant* Write frame operation, but not MII-compliant.  
*kENET\_MiiWriteValidFrame* Write frame operation for a valid MII management frame.

### 13.6.6 enum enet\_mii\_read\_t

Enumerator

*kENET\_MiiReadValidFrame* Read frame operation for a valid MII management frame.  
*kENET\_MiiReadNoCompliant* Read frame operation, but not MII-compliant.

### 13.6.7 enum enet\_special\_control\_flag\_t

These control flags are provided for special user requirements. Normally, these control flags are unused for ENET initialization. For special requirements, set the flags to macSpecialConfig in the [enet\\_config\\_t](#). The *kENET\_ControlStoreAndFwdDisable* is used to disable the FIFO store and forward. FIFO store and forward means that the FIFO read/send is started when a complete frame is stored in TX/RX FIFO. If this flag is set, configure *rxFifoFullThreshold* and *txFifoWatermark* in the [enet\\_config\\_t](#).

Enumerator

*kENET\_ControlFlowControlEnable* Enable ENET flow control: pause frame.  
*kENET\_ControlRxPayloadCheckEnable* Enable ENET receive payload length check.  
*kENET\_ControlRxPadRemoveEnable* Padding is removed from received frames.

***kENET\_ControlRxBroadCastRejectEnable*** Enable broadcast frame reject.  
***kENET\_ControlMacAddrInsert*** Enable MAC address insert.  
***kENET\_ControlStoreAndFwdDisable*** Enable FIFO store and forward.  
***kENET\_ControlSMIPreambleDisable*** Enable SMI preamble.  
***kENET\_ControlPromiscuousEnable*** Enable promiscuous mode.  
***kENET\_ControlMIILoopEnable*** Enable ENET MII loop back.  
***kENET\_ControlVLANTagEnable*** Enable VLAN tag frame.

### 13.6.8 enum enet\_interrupt\_enable\_t

This enumeration uses one-hot encoding to allow a logical OR of multiple members. Members usually map to interrupt enable bits in one or more peripheral registers.

Enumerator

***kENET\_BabrInterrupt*** Babbling receive error interrupt source.  
***kENET\_BabtInterrupt*** Babbling transmit error interrupt source.  
***kENET\_GraceStopInterrupt*** Graceful stop complete interrupt source.  
***kENET\_TxFrameInterrupt*** TX FRAME interrupt source.  
***kENET\_TxBufferInterrupt*** TX BUFFER interrupt source.  
***kENET\_RxFrameInterrupt*** RX FRAME interrupt source.  
***kENET\_RxBufferInterrupt*** RX BUFFER interrupt source.  
***kENET\_MiiInterrupt*** MII interrupt source.  
***kENET\_EBusERInterrupt*** Ethernet bus error interrupt source.  
***kENET\_LateCollisionInterrupt*** Late collision interrupt source.  
***kENET\_RetryLimitInterrupt*** Collision Retry Limit interrupt source.  
***kENET\_UnderrunInterrupt*** Transmit FIFO underrun interrupt source.  
***kENET\_PayloadRxInterrupt*** Payload Receive interrupt source.  
***kENET\_WakeupInterrupt*** WAKEUP interrupt source.

### 13.6.9 enum enet\_event\_t

Enumerator

***kENET\_RxEvent*** Receive event.  
***kENET\_TxEvent*** Transmit event.  
***kENET\_ErrEvent*** Error event: BABR/BABT/EBERR/LC/RL/UN/PLR .  
***kENET\_WakeUpEvent*** Wake up from sleep mode event.

## Function Documentation

### 13.6.10 enum enet\_tx\_accelerator\_t

Enumerator

*kENET\_TxAccelIsShift16Enabled* Transmit FIFO shift-16.  
*kENET\_TxAccelIpCheckEnabled* Insert IP header checksum.  
*kENET\_TxAccelProtoCheckEnabled* Insert protocol checksum.

### 13.6.11 enum enet\_rx\_accelerator\_t

Enumerator

*kENET\_RxAccelPadRemoveEnabled* Padding removal for short IP frames.  
*kENET\_RxAccelIpCheckEnabled* Discard with wrong IP header checksum.  
*kENET\_RxAccelProtoCheckEnabled* Discard with wrong protocol checksum.  
*kENET\_RxAccelMacCheckEnabled* Discard with Mac layer errors.  
*kENET\_RxAccelIsShift16Enabled* Receive FIFO shift-16.

## 13.7 Function Documentation

### 13.7.1 void ENET\_GetDefaultConfig ( enet\_config\_t \* config )

The purpose of this API is to get the default ENET MAC controller configuration structure for [ENET\\_Init\(\)](#). Users may use the initialized structure unchanged in [ENET\\_Init\(\)](#) or modify fields of the structure before calling [ENET\\_Init\(\)](#). This is an example.

```
enet_config_t config;  
ENET_GetDefaultConfig(&config);
```

Parameters

|               |                                                          |
|---------------|----------------------------------------------------------|
| <i>config</i> | The ENET mac controller configuration structure pointer. |
|---------------|----------------------------------------------------------|

### 13.7.2 void ENET\_Init ( ENET\_Type \* base, enet\_handle\_t \* handle, const enet\_config\_t \* config, const enet\_buffer\_config\_t \* bufferConfig, uint8\_t \* macAddr, uint32\_t srcClock\_Hz )

This function ungates the module clock and initializes it with the ENET configuration.



## Parameters

|                     |                                                                                                                                                                                                                       |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>         | ENET peripheral base address.                                                                                                                                                                                         |
| <i>handle</i>       | ENET handler pointer.                                                                                                                                                                                                 |
| <i>config</i>       | ENET Mac configuration structure pointer. The "enet_config_t" type mac configuration return from ENET_GetDefaultConfig can be used directly. It is also possible to verify the Mac configuration using other methods. |
| <i>bufferConfig</i> | ENET buffer configuration structure pointer. The buffer configuration should be prepared for ENET Initialization.                                                                                                     |
| <i>macAddr</i>      | ENET mac address of the Ethernet device. This Mac address should be provided.                                                                                                                                         |
| <i>srcClock_Hz</i>  | The internal module clock source for MII clock.                                                                                                                                                                       |

## Note

ENET has two buffer descriptors legacy buffer descriptors and enhanced IEEE 1588 buffer descriptors. The legacy descriptor is used by default. To use the IEEE 1588 feature, use the enhanced IEEE 1588 buffer descriptor by defining "ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE" and calling ENET\_Ptp1588Configure() to configure the 1588 feature and related buffers after calling [ENET\\_Init\(\)](#).

### 13.7.3 void ENET\_Deinit ( ENET\_Type \* *base* )

This function gates the module clock, clears ENET interrupts, and disables the ENET module.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### 13.7.4 static void ENET\_Reset ( ENET\_Type \* *base* ) [inline], [static]

This function restores the ENET module to the reset state. Note that this function sets all registers to the reset state. As a result, the ENET module can't work after calling this function.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### 13.7.5 void ENET\_SetMII ( ENET\_Type \* *base*, enet\_mii\_speed\_t *speed*, enet\_mii\_duplex\_t *duplex* )

## Function Documentation

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>speed</i>  | The speed of the RMII mode.   |
| <i>duplex</i> | The duplex of the RMII mode.  |

### 13.7.6 void ENET\_SetSMI ( ENET\_Type \* *base*, uint32\_t *srcClock\_Hz*, bool *isPreambleDisabled* )

### Parameters

|                            |                                                                                                                                                |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>                | ENET peripheral base address.                                                                                                                  |
| <i>srcClock_Hz</i>         | This is the ENET module clock frequency. Normally it's the system clock. See clock distribution.                                               |
| <i>isPreamble-Disabled</i> | The preamble disable flag. <ul style="list-style-type: none"><li>• true Enables the preamble.</li><li>• false Disables the preamble.</li></ul> |

### 13.7.7 static bool ENET\_GetSMI ( ENET\_Type \* *base* ) [inline], [static]

This API is used to get the SMI configuration to check whether the MII management interface has been set.

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### Returns

The SMI setup status true or false.

### 13.7.8 static uint32\_t ENET\_ReadSMIData ( ENET\_Type \* *base* ) [inline], [static]

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

## Returns

The data read from PHY

### 13.7.9 void ENET\_StartSMIRead ( ENET\_Type \* *base*, uint32\_t *phyAddr*, uint32\_t *phyReg*, enet\_mii\_read\_t *operation* )

## Parameters

|                  |                               |
|------------------|-------------------------------|
| <i>base</i>      | ENET peripheral base address. |
| <i>phyAddr</i>   | The PHY address.              |
| <i>phyReg</i>    | The PHY register.             |
| <i>operation</i> | The read operation.           |

### 13.7.10 void ENET\_StartSMIWrite ( ENET\_Type \* *base*, uint32\_t *phyAddr*, uint32\_t *phyReg*, enet\_mii\_write\_t *operation*, uint32\_t *data* )

## Parameters

|                  |                               |
|------------------|-------------------------------|
| <i>base</i>      | ENET peripheral base address. |
| <i>phyAddr</i>   | The PHY address.              |
| <i>phyReg</i>    | The PHY register.             |
| <i>operation</i> | The write operation.          |
| <i>data</i>      | The data written to PHY.      |

### 13.7.11 void ENET\_SetMacAddr ( ENET\_Type \* *base*, uint8\_t \* *macAddr* )

## Function Documentation

### Parameters

|                |                                                                                                   |
|----------------|---------------------------------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                                                     |
| <i>macAddr</i> | The six-byte Mac address pointer. The pointer is allocated by application and input into the API. |

### 13.7.12 void ENET\_GetMacAddr ( ENET\_Type \* *base*, uint8\_t \* *macAddr* )

### Parameters

|                |                                                                                                   |
|----------------|---------------------------------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                                                     |
| <i>macAddr</i> | The six-byte Mac address pointer. The pointer is allocated by application and input into the API. |

### 13.7.13 void ENET\_AddMulticastGroup ( ENET\_Type \* *base*, uint8\_t \* *address* )

### Parameters

|                |                                                                        |
|----------------|------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                          |
| <i>address</i> | The six-byte multicast group address which is provided by application. |

### 13.7.14 void ENET\_LeaveMulticastGroup ( ENET\_Type \* *base*, uint8\_t \* *address* )

### Parameters

|                |                                                                        |
|----------------|------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                          |
| <i>address</i> | The six-byte multicast group address which is provided by application. |

### 13.7.15 static void ENET\_ActiveRead ( ENET\_Type \* *base* ) [inline], [static]

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

## Note

This must be called after the MAC configuration and state are ready. It must be called after the [ENET\\_Init\(\)](#) and [ENET\\_Ptp1588Configure\(\)](#). This should be called when the ENET receive required.

### 13.7.16 static void ENET\_EnableSleepMode ( ENET\_Type \* *base*, bool *enable* ) [inline], [static]

This function is used to set the MAC enter sleep mode. When entering sleep mode, the magic frame wakeup interrupt should be enabled to wake up MAC from the sleep mode and reset it to normal mode.

## Parameters

|               |                                                   |
|---------------|---------------------------------------------------|
| <i>base</i>   | ENET peripheral base address.                     |
| <i>enable</i> | True enable sleep mode, false disable sleep mode. |

### 13.7.17 static void ENET\_GetAccelFunction ( ENET\_Type \* *base*, uint32\_t \* *txAccelOption*, uint32\_t \* *rxAccelOption* ) [inline], [static]

## Parameters

|                      |                                                                                                                                  |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>          | ENET peripheral base address.                                                                                                    |
| <i>txAccelOption</i> | The transmit accelerator option. The "enet_tx_accelerator_t" is recommended as the mask to get the exact the accelerator option. |
| <i>rxAccelOption</i> | The receive accelerator option. The "enet_rx_accelerator_t" is recommended as the mask to get the exact the accelerator option.  |

### 13.7.18 static void ENET\_EnableInterrupts ( ENET\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the ENET interrupt according to the provided mask. The mask is a logical OR of enumeration members. See [enet\\_interrupt\\_enable\\_t](#). For example, to enable the TX frame interrupt and RX frame interrupt, do the following.

## Function Documentation

```
*  ENET_EnableInterrupts (ENET, kENET_TxFrameInterrupt |  
*  kENET_RxFrameInterrupt);
```

## Parameters

|             |                                                                                                              |
|-------------|--------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ENET peripheral base address.                                                                                |
| <i>mask</i> | ENET interrupts to enable. This is a logical OR of the enumeration :: <code>enet_interrupt_enable_t</code> . |

### 13.7.19 static void ENET\_DisableInterrupts ( ENET\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function disables the ENET interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [enet\\_interrupt\\_enable\\_t](#). For example, to disable the TX frame interrupt and RX frame interrupt, do the following.

```
*  ENET_DisableInterrupts(ENET, kENET_TxFrameInterrupt |
*  kENET_RxFrameInterrupt);
```

## Parameters

|             |                                                                                                               |
|-------------|---------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ENET peripheral base address.                                                                                 |
| <i>mask</i> | ENET interrupts to disable. This is a logical OR of the enumeration :: <code>enet_interrupt_enable_t</code> . |

### 13.7.20 static uint32\_t ENET\_GetInterruptStatus ( ENET\_Type \* *base* ) [inline], [static]

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

## Returns

The event status of the interrupt source. This is the logical OR of members of the enumeration :: `enet_interrupt_enable_t`.

### 13.7.21 static void ENET\_ClearInterruptStatus ( ENET\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function clears enabled ENET interrupts according to the provided mask. The mask is a logical OR of enumeration members. See the [enet\\_interrupt\\_enable\\_t](#). For example, to clear the TX frame interrupt and RX frame interrupt, do the following.

## Function Documentation

```
* ENET_ClearInterruptStatus(ENET,  
* kENET_TxFrameInterrupt | kENET_RxFrameInterrupt);  
*
```

### Parameters

|             |                                                                                                                       |
|-------------|-----------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ENET peripheral base address.                                                                                         |
| <i>mask</i> | ENET interrupt source to be cleared. This is the logical OR of members of the enumeration :: enet_interrupt_enable_t. |

### 13.7.22 void ENET\_SetCallback ( enet\_handle\_t \* *handle*, enet\_callback\_t *callback*, void \* *userData* )

This API is provided for the application callback required case when ENET interrupt is enabled. This API should be called after calling ENET\_Init.

### Parameters

|                 |                                                          |
|-----------------|----------------------------------------------------------|
| <i>handle</i>   | ENET handler pointer. Should be provided by application. |
| <i>callback</i> | The ENET callback function.                              |
| <i>userData</i> | The callback function parameter.                         |

### 13.7.23 void ENET\_GetRxErrBeforeReadFrame ( enet\_handle\_t \* *handle*, enet\_data\_error\_stats\_t \* *eErrorStatic* )

This API must be called after the ENET\_GetRxFrameSize and before the [ENET\\_ReadFrame\(\)](#). If the ENET\_GetRxFrameSize returns kStatus\_ENET\_RxFrameError, the ENET\_GetRxErrBeforeReadFrame can be used to get the exact error statistics. This is an example.

```
* status = ENET_GetRxFrameSize(&g_handle, &length);  
* if (status == kStatus_ENET_RxFrameError)  
* {  
*     // Get the error information of the received frame.  
*     ENET_GetRxErrBeforeReadFrame(&g_handle, &eErrStatic);  
*     // update the receive buffer.  
*     ENET_ReadFrame(EXAMPLE_ENET, &g_handle, NULL, 0);  
* }  
*
```



## Parameters

|                     |                                                                                             |
|---------------------|---------------------------------------------------------------------------------------------|
| <i>handle</i>       | The ENET handler structure pointer. This is the same handler pointer used in the ENET_Init. |
| <i>eErrorStatic</i> | The error statistics structure pointer.                                                     |

### 13.7.24 status\_t ENET\_GetRxFrameSize ( enet\_handle\_t \* *handle*, uint32\_t \* *length* )

This function gets a received frame size from the ENET buffer descriptors.

## Note

The FCS of the frame is automatically removed by Mac and the size is the length without the FCS. After calling ENET\_GetRxFrameSize, [ENET\\_ReadFrame\(\)](#) should be called to update the receive buffers. If the result is not "kStatus\_ENET\_RxFrameEmpty".

## Parameters

|               |                                                                                     |
|---------------|-------------------------------------------------------------------------------------|
| <i>handle</i> | The ENET handler structure. This is the same handler pointer used in the ENET_Init. |
| <i>length</i> | The length of the valid frame received.                                             |

## Return values

|                                   |                                                                                                                                      |
|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <i>kStatus_ENET_RxFrame-Empty</i> | No frame received. Should not call ENET_ReadFrame to read frame.                                                                     |
| <i>kStatus_ENET_RxFrame-Error</i> | Data error happens. ENET_ReadFrame should be called with NULL data and NULL length to update the receive buffers.                    |
| <i>kStatus_Success</i>            | Receive a frame Successfully then the ENET_ReadFrame should be called with the right data buffer and the captured data length input. |

### 13.7.25 status\_t ENET\_ReadFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, uint8\_t \* *data*, uint32\_t *length* )

This function reads a frame (both the data and the length) from the ENET buffer descriptors. The ENET\_GetRxFrameSize should be used to get the size of the prepared data buffer. This is an example.

```
*      uint32_t length;
*      enet_handle_t g_handle;
*      //Get the received frame size firstly.
*      status = ENET_GetRxFrameSize(&g_handle, &length);
```

## Function Documentation

```
*      if (length != 0)
*      {
*          //Allocate memory here with the size of "length"
*          uint8_t *data = memory allocate interface;
*          if (!data)
*          {
*              ENET_ReadFrame(ENET, &g_handle, NULL, 0);
*              //Add the console warning log.
*          }
*          else
*          {
*              status = ENET_ReadFrame(ENET, &g_handle, data, length);
*              //Call stack input API to deliver the data to stack
*          }
*      }
*      else if (status == kStatus_ENET_RxFrameError)
*      {
*          //Update the received buffer when a error frame is received.
*          ENET_ReadFrame(ENET, &g_handle, NULL, 0);
*      }
*
```

### Parameters

|               |                                                                                                    |
|---------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>   | ENET peripheral base address.                                                                      |
| <i>handle</i> | The ENET handler structure. This is the same handler pointer used in the ENET_Init.                |
| <i>data</i>   | The data buffer provided by user to store the frame which memory size should be at least "length". |
| <i>length</i> | The size of the data buffer which is still the length of the received frame.                       |

### Returns

The execute status, successful or failure.

### 13.7.26 status\_t ENET\_SendFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, uint8\_t \* *data*, uint32\_t *length* )

#### Note

The CRC is automatically appended to the data. Input the data to send without the CRC.

### Parameters

|               |                                                                                   |
|---------------|-----------------------------------------------------------------------------------|
| <i>base</i>   | ENET peripheral base address.                                                     |
| <i>handle</i> | The ENET handler pointer. This is the same handler pointer used in the ENET_Init. |
| <i>data</i>   | The data buffer provided by user to be send.                                      |
| <i>length</i> | The length of the data to be send.                                                |

Return values

|                                  |                                                                                                                                                                                                                                                |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>kStatus_Success</i>           | Send frame succeed.                                                                                                                                                                                                                            |
| <i>kStatus_ENET_TxFrame-Busy</i> | Transmit buffer descriptor is busy under transmission. The transmit busy happens when the data send rate is over the MAC capacity. The waiting mechanism is recommended to be added after each call return with kStatus-<br>_ENET_TxFrameBusy. |

### 13.7.27 void ENET\_TransmitIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>handle</i> | The ENET handler pointer.     |

### 13.7.28 void ENET\_ReceiveIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>handle</i> | The ENET handler pointer.     |

### 13.7.29 void ENET\_ErrorIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>handle</i> | The ENET handler pointer.     |



## Chapter 14

# EWM: External Watchdog Monitor Driver

### 14.1 Overview

The KSDK provides a peripheral driver for the EWM module of Kinetis devices.

### 14.2 Typical use case

```
ewm_config_t config;
EWM_GetDefaultConfig(&config);
config.enableInterrupt = true;
config.compareLowValue = 0U;
config.compareHighValue = 0xAAU;
NVIC_EnableIRQ(WDOG_EWM_IRQn);
EWM_Init(base, &config);
```

### Data Structures

- struct `ewm_config_t`  
*Describes EWM clock source. [More...](#)*

### Enumerations

- enum `_ewm_interrupt_enable_t` { `kEWM_InterruptEnable` = `EWM_CTRL_INTEN_MASK` }  
*EWM interrupt configuration structure with default settings all disabled.*
- enum `_ewm_status_flags_t` { `kEWM_RunningFlag` = `EWM_CTRL_EWMEN_MASK` }  
*EWM status flags.*

### Driver version

- #define `FSL_EWM_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 1)`)  
*EWM driver version 2.0.1.*

### EWM initialization and de-initialization

- void `EWM_Init` (`EWM_Type *base`, const `ewm_config_t *config`)  
*Initializes the EWM peripheral.*
- void `EWM_Deinit` (`EWM_Type *base`)  
*Deinitializes the EWM peripheral.*
- void `EWM_GetDefaultConfig` (`ewm_config_t *config`)  
*Initializes the EWM configuration structure.*

### EWM functional Operation

- static void `EWM_EnableInterrupts` (`EWM_Type *base`, `uint32_t mask`)  
*Enables the EWM interrupt.*
- static void `EWM_DisableInterrupts` (`EWM_Type *base`, `uint32_t mask`)

## Enumeration Type Documentation

- Disables the EWM interrupt.*
- static uint32\_t [EWM\\_GetStatusFlags](#) (EWM\_Type \*base)  
*Gets all status flags.*
- void [EWM\\_Refresh](#) (EWM\_Type \*base)  
*Serves the EWM.*

## 14.3 Data Structure Documentation

### 14.3.1 struct ewm\_config\_t

Data structure for EWM configuration.

This structure is used to configure the EWM.

#### Data Fields

- bool [enableEwm](#)  
*Enable EWM module.*
- bool [enableEwmInput](#)  
*Enable EWM\_in input.*
- bool [setInputAssertLogic](#)  
*EWM\_in signal assertion state.*
- bool [enableInterrupt](#)  
*Enable EWM interrupt.*
- uint8\_t [compareLowValue](#)  
*Compare low-register value.*
- uint8\_t [compareHighValue](#)  
*Compare high-register value.*

## 14.4 Macro Definition Documentation

### 14.4.1 #define FSL\_EWM\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

## 14.5 Enumeration Type Documentation

### 14.5.1 enum \_ewm\_interrupt\_enable\_t

This structure contains the settings for all of EWM interrupt configurations.

Enumerator

***kEWM\_InterruptEnable*** Enable the EWM to generate an interrupt.

### 14.5.2 enum \_ewm\_status\_flags\_t

This structure contains the constants for the EWM status flags for use in the EWM functions.

## Enumerator

***kEWM\_RunningFlag*** Running flag, set when EWM is enabled.

## 14.6 Function Documentation

### 14.6.1 void EWM\_Init ( EWM\_Type \* *base*, const ewm\_config\_t \* *config* )

This function is used to initialize the EWM. After calling, the EWM runs immediately according to the configuration. Note that, except for the interrupt enable control bit, other control bits and registers are write once after a CPU reset. Modifying them more than once generates a bus transfer error.

This is an example.

```
*  ewm_config_t config;
*  EWM_GetDefaultConfig(&config);
*  config.compareHighValue = 0xAAU;
*  EWM_Init(ewm_base, &config);
*
```

## Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | EWM peripheral base address  |
| <i>config</i> | The configuration of the EWM |

### 14.6.2 void EWM\_Deinit ( EWM\_Type \* *base* )

This function is used to shut down the EWM.

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | EWM peripheral base address |
|-------------|-----------------------------|

### 14.6.3 void EWM\_GetDefaultConfig ( ewm\_config\_t \* *config* )

This function initializes the EWM configuration structure to default values. The default values are as follows.

```
*  ewmConfig->enableEwm = true;
*  ewmConfig->enableEwmInput = false;
*  ewmConfig->setInputAssertLogic = false;
*  ewmConfig->enableInterrupt = false;
*  ewmConfig->ewm_lpo_clock_source_t = kEWM_LpoClockSource0;
*  ewmConfig->prescaler = 0;
*  ewmConfig->compareLowValue = 0;
*  ewmConfig->compareHighValue = 0xFEU;
*
```

## Function Documentation

### Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Pointer to the EWM configuration structure. |
|---------------|---------------------------------------------|

See Also

[ewm\\_config\\_t](#)

### 14.6.4 static void EWM\_EnableInterrupts ( EWM\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the EWM interrupt.

### Parameters

|             |                                                                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | EWM peripheral base address                                                                                                                                         |
| <i>mask</i> | The interrupts to enable The parameter can be combination of the following source if defined <ul style="list-style-type: none"><li>• kEWM_InterruptEnable</li></ul> |

### 14.6.5 static void EWM\_DisableInterrupts ( EWM\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the EWM interrupt.

### Parameters

|             |                                                                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | EWM peripheral base address                                                                                                                                          |
| <i>mask</i> | The interrupts to disable The parameter can be combination of the following source if defined <ul style="list-style-type: none"><li>• kEWM_InterruptEnable</li></ul> |

### 14.6.6 static uint32\_t EWM\_GetStatusFlags ( EWM\_Type \* *base* ) [inline], [static]

This function gets all status flags.

This is an example for getting the running flag.



```

*  uint32_t status;
*  status = EWM_GetStatusFlags(ewm_base) & kEWM_RunningFlag;
*

```

#### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | EWM peripheral base address |
|-------------|-----------------------------|

#### Returns

State of the status flag: asserted (true) or not-asserted (false).

#### See Also

[\\_ewm\\_status\\_flags\\_t](#)

- True: a related status flag has been set.
- False: a related status flag is not set.

### 14.6.7 void EWM\_Refresh ( EWM\_Type \* *base* )

This function resets the EWM counter to zero.

#### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | EWM peripheral base address |
|-------------|-----------------------------|



## Chapter 15

### C90TFS Flash Driver

#### 15.1 Overview

The flash provides the C90TFS Flash driver of Kinetis devices with the C90TFS Flash module inside. The flash driver provides general APIs to handle specific operations on C90TFS/FTFx Flash module. The user can use those APIs directly in the application. In addition, it provides internal functions called by the driver. Although these functions are not meant to be called from the user's application directly, the APIs can still be used.

#### Data Structures

- struct [flash\\_execute\\_in\\_ram\\_function\\_config\\_t](#)  
*Flash execute-in-RAM function information. [More...](#)*
- struct [flash\\_swap\\_state\\_config\\_t](#)  
*Flash Swap information. [More...](#)*
- struct [flash\\_swap\\_ifr\\_field\\_config\\_t](#)  
*Flash Swap IFR fields. [More...](#)*
- union [flash\\_swap\\_ifr\\_field\\_data\\_t](#)  
*Flash Swap IFR field data. [More...](#)*
- union [pflash\\_protection\\_status\\_low\\_t](#)  
*PFlash protection status - low 32bit. [More...](#)*
- struct [pflash\\_protection\\_status\\_t](#)  
*PFlash protection status - full. [More...](#)*
- struct [flash\\_prefetch\\_speculation\\_status\\_t](#)  
*Flash prefetch speculation status. [More...](#)*
- struct [flash\\_protection\\_config\\_t](#)  
*Active flash protection information for the current operation. [More...](#)*
- struct [flash\\_access\\_config\\_t](#)  
*Active flash Execute-Only access information for the current operation. [More...](#)*
- struct [flash\\_operation\\_config\\_t](#)  
*Active flash information for the current operation. [More...](#)*
- struct [flash\\_config\\_t](#)  
*Flash driver state information. [More...](#)*

#### Typedefs

- typedef void(\* [flash\\_callback\\_t](#))(void)  
*A callback type used for the Pflash block.*

#### Enumerations

- enum [flash\\_margin\\_value\\_t](#) {  
    [kFLASH\\_MarginValueNormal](#),  
    [kFLASH\\_MarginValueUser](#),  
    [kFLASH\\_MarginValueFactory](#),

## Overview

`kFLASH_MarginValueInvalid` }

*Enumeration for supported flash margin levels.*

- enum `flash_security_state_t` {  
    `kFLASH_SecurityStateNotSecure`,  
    `kFLASH_SecurityStateBackdoorEnabled`,  
    `kFLASH_SecurityStateBackdoorDisabled` }

*Enumeration for the three possible flash security states.*

- enum `flash_protection_state_t` {  
    `kFLASH_ProtectionStateUnprotected`,  
    `kFLASH_ProtectionStateProtected`,  
    `kFLASH_ProtectionStateMixed` }

*Enumeration for the three possible flash protection levels.*

- enum `flash_execute_only_access_state_t` {  
    `kFLASH_AccessStateUnLimited`,  
    `kFLASH_AccessStateExecuteOnly`,  
    `kFLASH_AccessStateMixed` }

*Enumeration for the three possible flash execute access levels.*

- enum `flash_property_tag_t` {  
    `kFLASH_PropertyPflashSectorSize` = 0x00U,  
    `kFLASH_PropertyPflashTotalSize` = 0x01U,  
    `kFLASH_PropertyPflashBlockSize` = 0x02U,  
    `kFLASH_PropertyPflashBlockCount` = 0x03U,  
    `kFLASH_PropertyPflashBlockBaseAddr` = 0x04U,  
    `kFLASH_PropertyPflashFacSupport` = 0x05U,  
    `kFLASH_PropertyPflashAccessSegmentSize` = 0x06U,  
    `kFLASH_PropertyPflashAccessSegmentCount` = 0x07U,  
    `kFLASH_PropertyFlexRamBlockBaseAddr` = 0x08U,  
    `kFLASH_PropertyFlexRamTotalSize` = 0x09U,  
    `kFLASH_PropertyDflashSectorSize` = 0x10U,  
    `kFLASH_PropertyDflashTotalSize` = 0x11U,  
    `kFLASH_PropertyDflashBlockSize` = 0x12U,  
    `kFLASH_PropertyDflashBlockCount` = 0x13U,  
    `kFLASH_PropertyDflashBlockBaseAddr` = 0x14U,  
    `kFLASH_PropertyEepromTotalSize` = 0x15U,  
    `kFLASH_PropertyFlashMemoryIndex` = 0x20U }

*Enumeration for various flash properties.*

- enum `_flash_execute_in_ram_function_constants` {  
    `kFLASH_ExecuteInRamFunctionMaxSizeInWords` = 16U,  
    `kFLASH_ExecuteInRamFunctionTotalNum` = 2U }

*Constants for execute-in-RAM flash function.*

- enum `flash_read_resource_option_t` {  
    `kFLASH_ResourceOptionFlashIfr`,  
    `kFLASH_ResourceOptionVersionId` = 0x01U }

*Enumeration for the two possible options of flash read resource command.*

- enum `_flash_read_resource_range` {

```

kFLASH_ResourceRangePflashIfrSizeInBytes = 1024U,
kFLASH_ResourceRangeVersionIdSizeInBytes = 8U,
kFLASH_ResourceRangeVersionIdStart = 0x08U,
kFLASH_ResourceRangeVersionIdEnd = 0x0FU,
kFLASH_ResourceRangePflashSwapIfrStart = 0x40000U,
kFLASH_ResourceRangePflashSwapIfrEnd,
kFLASH_ResourceRangeDflashIfrStart = 0x800000U,
kFLASH_ResourceRangeDflashIfrEnd = 0x8003FFU }

```

*Enumeration for the range of special-purpose flash resource.*

- enum flash\_flexram\_function\_option\_t {
 kFLASH\_FlexramFunctionOptionAvailableAsRam = 0xFFU,
 kFLASH\_FlexramFunctionOptionAvailableForEeprom = 0x00U }

*Enumeration for the two possible options of set FlexRAM function command.*

- enum \_flash\_acceleration\_ram\_property

*Enumeration for acceleration RAM property.*

- enum flash\_swap\_function\_option\_t {
 kFLASH\_SwapFunctionOptionEnable = 0x00U,
 kFLASH\_SwapFunctionOptionDisable = 0x01U }

*Enumeration for the possible options of Swap function.*

- enum flash\_swap\_control\_option\_t {
 kFLASH\_SwapControlOptionInitializeSystem = 0x01U,
 kFLASH\_SwapControlOptionSetInUpdateState = 0x02U,
 kFLASH\_SwapControlOptionSetInCompleteState = 0x04U,
 kFLASH\_SwapControlOptionReportStatus = 0x08U,
 kFLASH\_SwapControlOptionDisableSystem = 0x10U }

*Enumeration for the possible options of Swap control commands.*

- enum flash\_swap\_state\_t {
 kFLASH\_SwapStateUninitialized = 0x00U,
 kFLASH\_SwapStateReady = 0x01U,
 kFLASH\_SwapStateUpdate = 0x02U,
 kFLASH\_SwapStateUpdateErased = 0x03U,
 kFLASH\_SwapStateComplete = 0x04U,
 kFLASH\_SwapStateDisabled = 0x05U }

*Enumeration for the possible flash Swap status.*

- enum flash\_swap\_block\_status\_t {
 kFLASH\_SwapBlockStatusLowerHalfProgramBlocksAtZero,
 kFLASH\_SwapBlockStatusUpperHalfProgramBlocksAtZero }

*Enumeration for the possible flash Swap block status*

- enum flash\_partition\_flexram\_load\_option\_t {
 kFLASH\_PartitionFlexramLoadOptionLoadedWithValidEepromData,
 kFLASH\_PartitionFlexramLoadOptionNotLoaded = 0x01U }

*Enumeration for the FlexRAM load during reset option.*

- enum flash\_memory\_index\_t {
 kFLASH\_MemoryIndexPrimaryFlash = 0x00U,
 kFLASH\_MemoryIndexSecondaryFlash = 0x01U }

*Enumeration for the flash memory index.*

- enum flash\_prefetch\_speculation\_option\_t

## Overview

*Enumeration for the two possible options of flash prefetch speculation.*

## Flash version

- enum `_flash_driver_version_constants` {  
    `kFLASH_DriverVersionName` = 'F',  
    `kFLASH_DriverVersionMajor` = 2,  
    `kFLASH_DriverVersionMinor` = 2,  
    `kFLASH_DriverVersionBugfix` = 0 }  
    *Flash driver version for ROM.*
- #define `MAKE_VERSION`(major, minor, bugfix) (((major) << 16) | ((minor) << 8) | (bugfix))  
    *Constructs the version number for drivers.*
- #define `FSL_FLASH_DRIVER_VERSION` (`MAKE_VERSION`(2, 2, 0))  
    *Flash driver version for SDK.*

## Flash configuration

- #define `FLASH_SSD_CONFIG_ENABLE_FLEXNVM_SUPPORT` 1  
    *Indicates whether to support FlexNVM in the Flash driver.*
- #define `FLASH_SSD_IS_FLEXNVM_ENABLED` (`FLASH_SSD_CONFIG_ENABLE_FLEXNVM_SUPPORT` && `FSL_FEATURE_FLASH_HAS_FLEX_NVM`)  
    *Indicates whether the FlexNVM is enabled in the Flash driver.*
- #define `FLASH_SSD_IS_SECONDARY_FLASH_SUPPORTED` (0)  
    *Indicates whether the secondary flash is supported in the Flash driver.*
- #define `FLASH_SSD_SECONDARY_FLASH_HAS_ITS_OWN_PROTECTION_REGISTER` (0)  
    *Indicates whether the secondary flash has its own protection register in flash module.*
- #define `FLASH_SSD_SECONDARY_FLASH_HAS_ITS_OWN_ACCESS_REGISTER` (0)  
    *Indicates whether the secondary flash has its own Execute-Only access register in flash module.*
- #define `FLASH_DRIVER_IS_FLASH_RESIDENT` 1  
    *Flash driver location.*
- #define `FLASH_DRIVER_IS_EXPORTED` 0  
    *Flash Driver Export option.*

## Flash status

- enum `_flash_status` {  
`kStatus_FLASH_Success` = MAKE\_STATUS(kStatusGroupGeneric, 0),  
`kStatus_FLASH_InvalidArgument` = MAKE\_STATUS(kStatusGroupGeneric, 4),  
`kStatus_FLASH_SizeError` = MAKE\_STATUS(kStatusGroupFlashDriver, 0),  
`kStatus_FLASH_AlignmentError`,  
`kStatus_FLASH_AddressError` = MAKE\_STATUS(kStatusGroupFlashDriver, 2),  
`kStatus_FLASH_AccessError`,  
`kStatus_FLASH_ProtectionViolation`,  
`kStatus_FLASH_CommandFailure`,  
`kStatus_FLASH_UnknownProperty` = MAKE\_STATUS(kStatusGroupFlashDriver, 6),  
`kStatus_FLASH_EraseKeyError` = MAKE\_STATUS(kStatusGroupFlashDriver, 7),  
`kStatus_FLASH_RegionExecuteOnly`,  
`kStatus_FLASH_ExecuteInRamFunctionNotReady`,  
`kStatus_FLASH_PartitionStatusUpdateFailure`,  
`kStatus_FLASH_SetFlexramAsEepromError`,  
`kStatus_FLASH_RecoverFlexramAsRamError`,  
`kStatus_FLASH_SetFlexramAsRamError` = MAKE\_STATUS(kStatusGroupFlashDriver, 13),  
`kStatus_FLASH_RecoverFlexramAsEepromError`,  
`kStatus_FLASH_CommandNotSupported` = MAKE\_STATUS(kStatusGroupFlashDriver, 15),  
`kStatus_FLASH_SwapSystemNotInUninitialized`,  
`kStatus_FLASH_SwapIndicatorAddressError`,  
`kStatus_FLASH_ReadOnlyProperty` = MAKE\_STATUS(kStatusGroupFlashDriver, 18),  
`kStatus_FLASH_InvalidPropertyValue`,  
`kStatus_FLASH_InvalidSpeculationOption` }  
*Flash driver status codes.*
- #define `kStatusGroupGeneric` 0  
*Flash driver status group.*
- #define `kStatusGroupFlashDriver` 1
- #define `MAKE_STATUS`(group, code) (((group)\*100) + (code)))  
*Constructs a status code value from a group and a code number.*

## Flash API key

- enum `_flash_driver_api_keys` { `kFLASH_ApiEraseKey` = FOUR\_CHAR\_CODE('k', 'f', 'e', 'k') }  
*Enumeration for Flash driver API keys.*
- #define `FOUR_CHAR_CODE`(a, b, c, d) (((d) << 24) | ((c) << 16) | ((b) << 8) | ((a)))  
*Constructs the four character code for the Flash driver API key.*

## Initialization

- status\_t `FLASH_Init` (flash\_config\_t \*config)  
*Initializes the global flash properties structure members.*
- status\_t `FLASH_SetCallback` (flash\_config\_t \*config, flash\_callback\_t callback)  
*Sets the desired flash callback function.*
- status\_t `FLASH_PrepareExecuteInRamFunctions` (flash\_config\_t \*config)  
*Prepares flash execute-in-RAM functions.*

## Overview

## Erasing

- status\_t [FLASH\\_EraseAll](#) (flash\_config\_t \*config, uint32\_t key)  
*Erases entire flash.*
- status\_t [FLASH\\_Erase](#) (flash\_config\_t \*config, uint32\_t start, uint32\_t lengthInBytes, uint32\_t key)  
*Erases the flash sectors encompassed by parameters passed into function.*
- status\_t [FLASH\\_EraseAllExecuteOnlySegments](#) (flash\_config\_t \*config, uint32\_t key)  
*Erases the entire flash, including protected sectors.*

## Programming

- status\_t [FLASH\\_Program](#) (flash\_config\_t \*config, uint32\_t start, uint32\_t \*src, uint32\_t lengthInBytes)  
*Programs flash with data at locations passed in through parameters.*
- status\_t [FLASH\\_ProgramOnce](#) (flash\_config\_t \*config, uint32\_t index, uint32\_t \*src, uint32\_t lengthInBytes)  
*Programs Program Once Field through parameters.*
- status\_t [FLASH\\_ProgramSection](#) (flash\_config\_t \*config, uint32\_t start, uint32\_t \*src, uint32\_t lengthInBytes)  
*Programs flash with data at locations passed in through parameters via the Program Section command.*
- status\_t [FLASH\\_EepromWrite](#) (flash\_config\_t \*config, uint32\_t start, uint8\_t \*src, uint32\_t lengthInBytes)  
*Programs the EEPROM with data at locations passed in through parameters.*

## Reading

- status\_t [FLASH\\_ReadResource](#) (flash\_config\_t \*config, uint32\_t start, uint32\_t \*dst, uint32\_t lengthInBytes, flash\_read\_resource\_option\_t option)  
*Reads the resource with data at locations passed in through parameters.*
- status\_t [FLASH\\_ReadOnce](#) (flash\_config\_t \*config, uint32\_t index, uint32\_t \*dst, uint32\_t lengthInBytes)  
*Reads the Program Once Field through parameters.*

## Security

- status\_t [FLASH\\_GetSecurityState](#) (flash\_config\_t \*config, flash\_security\_state\_t \*state)  
*Returns the security state via the pointer passed into the function.*
- status\_t [FLASH\\_SecurityBypass](#) (flash\_config\_t \*config, const uint8\_t \*backdoorKey)  
*Allows users to bypass security with a backdoor key.*

## Verification

- status\_t [FLASH\\_VerifyEraseAll](#) (flash\_config\_t \*config, flash\_margin\_value\_t margin)  
*Verifies erasure of the entire flash at a specified margin level.*
- status\_t [FLASH\\_VerifyErase](#) (flash\_config\_t \*config, uint32\_t start, uint32\_t lengthInBytes, flash\_margin\_value\_t margin)  
*Verifies an erasure of the desired flash area at a specified margin level.*
- status\_t [FLASH\\_VerifyProgram](#) (flash\_config\_t \*config, uint32\_t start, uint32\_t lengthInBytes, const uint32\_t \*expectedData, flash\_margin\_value\_t margin, uint32\_t \*failedAddress, uint32\_t \*failedData)



*Verifies programming of the desired flash area at a specified margin level.*

- status\_t **FLASH\_VerifyEraseAllExecuteOnlySegments** (flash\_config\_t \*config, flash\_margin\_value\_t margin)

*Verifies whether the program flash execute-only segments have been erased to the specified read margin level.*

## Protection

- status\_t **FLASH\_IsProtected** (flash\_config\_t \*config, uint32\_t start, uint32\_t lengthInBytes, flash\_protection\_state\_t \*protection\_state)

*Returns the protection state of the desired flash area via the pointer passed into the function.*

- status\_t **FLASH\_IsExecuteOnly** (flash\_config\_t \*config, uint32\_t start, uint32\_t lengthInBytes, flash\_execute\_only\_access\_state\_t \*access\_state)

*Returns the access state of the desired flash area via the pointer passed into the function.*

## Properties

- status\_t **FLASH\_GetProperty** (flash\_config\_t \*config, flash\_property\_tag\_t whichProperty, uint32\_t \*value)

*Returns the desired flash property.*

## FlexRAM

Sets the desired flash property.

Parameters

|                      |                                                                               |
|----------------------|-------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                        |
| <i>whichProperty</i> | The desired property from the list of properties in enum flash_property_tag_t |
| <i>value</i>         | A to set for the desired flash property.                                      |

Return values

|                                           |                                  |
|-------------------------------------------|----------------------------------|
| <i>kStatus_FLASH_Success</i>              | API was executed successfully.   |
| <i>kStatus_FLASH_InvalidArgument</i>      | An invalid argument is provided. |
| <i>kStatus_FLASH_UnknownProperty</i>      | An unknown property tag.         |
| <i>kStatus_FLASH_InvalidPropertyValue</i> | An invalid property value.       |
| <i>kStatus_FLASH_ReadOnlyProperty</i>     | An read-only property tag.       |

- status\_t **FLASH\_SetFlexramFunction** (flash\_config\_t \*config, flash\_flexram\_function\_option\_t option)

*Sets the FlexRAM function command.*

### Swap

- status\_t [FLASH\\_SwapControl](#) ([flash\\_config\\_t](#) \*config, uint32\_t address, [flash\\_swap\\_control\\_option\\_t](#) option, [flash\\_swap\\_state\\_config\\_t](#) \*returnInfo)  
*Configures the Swap function or checks the the swap state of the Flash module.*
- status\_t [FLASH\\_Swap](#) ([flash\\_config\\_t](#) \*config, uint32\_t address, [flash\\_swap\\_function\\_option\\_t](#) option)  
*Swaps the lower half flash with the higher half flash.*

### FlexNVM

- status\_t [FLASH\\_ProgramPartition](#) ([flash\\_config\\_t](#) \*config, [flash\\_partition\\_flexram\\_load\\_option\\_t](#) option, uint32\_t eepromDataSizeCode, uint32\_t flexnvmPartitionCode)  
*Prepares the FlexNVM block for use as data flash, EEPROM backup, or a combination of both and initializes the FlexRAM.*

### Flash Protection Utilities

- status\_t [FLASH\\_PflashSetProtection](#) ([flash\\_config\\_t](#) \*config, [pflash\\_protection\\_status\\_t](#) \*protectStatus)  
*Sets the PFlash Protection to the intended protection status.*
- status\_t [FLASH\\_PflashGetProtection](#) ([flash\\_config\\_t](#) \*config, [pflash\\_protection\\_status\\_t](#) \*protectStatus)  
*Gets the PFlash protection status.*
- status\_t [FLASH\\_DflashSetProtection](#) ([flash\\_config\\_t](#) \*config, uint8\_t protectStatus)  
*Sets the DFlash protection to the intended protection status.*
- status\_t [FLASH\\_DflashGetProtection](#) ([flash\\_config\\_t](#) \*config, uint8\_t \*protectStatus)  
*Gets the DFlash protection status.*
- status\_t [FLASH\\_EepromSetProtection](#) ([flash\\_config\\_t](#) \*config, uint8\_t protectStatus)  
*Sets the EEPROM protection to the intended protection status.*
- status\_t [FLASH\\_EepromGetProtection](#) ([flash\\_config\\_t](#) \*config, uint8\_t \*protectStatus)  
*Gets the DFlash protection status.*

## 15.2 Data Structure Documentation

### 15.2.1 struct flash\_execute\_in\_ram\_function\_config\_t

#### Data Fields

- uint32\_t [activeFunctionCount](#)  
*Number of available execute-in-RAM functions.*
- uint32\_t \* [flashRunCommand](#)  
*Execute-in-RAM function: flash\_run\_command.*
- uint32\_t \* [flashCommonBitOperation](#)  
*Execute-in-RAM function: flash\_common\_bit\_operation.*

**15.2.1.0.0.35 Field Documentation****15.2.1.0.0.35.1** uint32\_t flash\_execute\_in\_ram\_function\_config\_t::activeFunctionCount**15.2.1.0.0.35.2** uint32\_t\* flash\_execute\_in\_ram\_function\_config\_t::flashRunCommand**15.2.1.0.0.35.3** uint32\_t\* flash\_execute\_in\_ram\_function\_config\_t::flashCommonBitOperation**15.2.2 struct flash\_swap\_state\_config\_t****Data Fields**

- [flash\\_swap\\_state\\_t](#) flashSwapState  
*The current Swap system status.*
- [flash\\_swap\\_block\\_status\\_t](#) currentSwapBlockStatus  
*The current Swap block status.*
- [flash\\_swap\\_block\\_status\\_t](#) nextSwapBlockStatus  
*The next Swap block status.*

**15.2.2.0.0.36 Field Documentation****15.2.2.0.0.36.1** flash\_swap\_state\_t flash\_swap\_state\_config\_t::flashSwapState**15.2.2.0.0.36.2** flash\_swap\_block\_status\_t flash\_swap\_state\_config\_t::currentSwapBlockStatus**15.2.2.0.0.36.3** flash\_swap\_block\_status\_t flash\_swap\_state\_config\_t::nextSwapBlockStatus**15.2.3 struct flash\_swap\_ifr\_field\_config\_t****Data Fields**

- uint16\_t [swapIndicatorAddress](#)  
*A Swap indicator address field.*
- uint16\_t [swapEnableWord](#)  
*A Swap enable word field.*
- uint8\_t [reserved0](#) [4]  
*A reserved field.*
- uint8\_t [reserved1](#) [2]  
*A reserved field.*
- uint16\_t [swapDisableWord](#)  
*A Swap disable word field.*
- uint8\_t [reserved2](#) [4]  
*A reserved field.*

## Data Structure Documentation

### 15.2.3.0.0.37 Field Documentation

15.2.3.0.0.37.1 uint16\_t flash\_swap\_ifr\_field\_config\_t::swapIndicatorAddress

15.2.3.0.0.37.2 uint16\_t flash\_swap\_ifr\_field\_config\_t::swapEnableWord

15.2.3.0.0.37.3 uint8\_t flash\_swap\_ifr\_field\_config\_t::reserved0[4]

15.2.3.0.0.37.4 uint8\_t flash\_swap\_ifr\_field\_config\_t::reserved1[2]

15.2.3.0.0.37.5 uint16\_t flash\_swap\_ifr\_field\_config\_t::swapDisableWord

15.2.3.0.0.37.6 uint8\_t flash\_swap\_ifr\_field\_config\_t::reserved2[4]

### 15.2.4 union flash\_swap\_ifr\_field\_data\_t

#### Data Fields

- uint32\_t [flashSwapIfrData](#) [2]  
*A flash Swap IFR field data.*
- [flash\\_swap\\_ifr\\_field\\_config\\_t flashSwapIfrField](#)  
*A flash Swap IFR field structure.*

### 15.2.4.0.0.38 Field Documentation

15.2.4.0.0.38.1 uint32\_t flash\_swap\_ifr\_field\_data\_t::flashSwapIfrData[2]

15.2.4.0.0.38.2 flash\_swap\_ifr\_field\_config\_t flash\_swap\_ifr\_field\_data\_t::flashSwapIfrField

### 15.2.5 union pflash\_protection\_status\_low\_t

#### Data Fields

- uint32\_t [protl32b](#)  
*PROT[31:0].*
- uint8\_t [protsl](#)  
*PROTS[7:0].*
- uint8\_t [protsh](#)  
*PROTS[15:8].*

**15.2.5.0.0.39 Field Documentation****15.2.5.0.0.39.1** uint32\_t pflash\_protection\_status\_low\_t::protl32b**15.2.5.0.0.39.2** uint8\_t pflash\_protection\_status\_low\_t::protsl**15.2.5.0.0.39.3** uint8\_t pflash\_protection\_status\_low\_t::protsh**15.2.6 struct pflash\_protection\_status\_t****Data Fields**

- [pflash\\_protection\\_status\\_low\\_t valueLow32b](#)  
*PROT[31:0] or PROTS[15:0].*

**15.2.6.0.0.40 Field Documentation****15.2.6.0.0.40.1** pflash\_protection\_status\_low\_t pflash\_protection\_status\_t::valueLow32b**15.2.7 struct flash\_prefetch\_speculation\_status\_t****Data Fields**

- [flash\\_prefetch\\_speculation\\_option\\_t instructionOption](#)  
*Instruction speculation.*
- [flash\\_prefetch\\_speculation\\_option\\_t dataOption](#)  
*Data speculation.*

**15.2.7.0.0.41 Field Documentation****15.2.7.0.0.41.1** flash\_prefetch\_speculation\_option\_t flash\_prefetch\_speculation\_status\_t::instructionOption**15.2.7.0.0.41.2** flash\_prefetch\_speculation\_option\_t flash\_prefetch\_speculation\_status\_t::dataOption**15.2.8 struct flash\_protection\_config\_t****Data Fields**

- uint32\_t [regionBase](#)  
*Base address of flash protection region.*
- uint32\_t [regionSize](#)  
*size of flash protection region.*
- uint32\_t [regionCount](#)  
*flash protection region count.*

## Data Structure Documentation

### 15.2.8.0.0.42 Field Documentation

15.2.8.0.0.42.1 uint32\_t flash\_protection\_config\_t::regionBase

15.2.8.0.0.42.2 uint32\_t flash\_protection\_config\_t::regionSize

15.2.8.0.0.42.3 uint32\_t flash\_protection\_config\_t::regionCount

### 15.2.9 struct flash\_access\_config\_t

#### Data Fields

- uint32\_t [SegmentBase](#)  
*Base address of flash Execute-Only segment.*
- uint32\_t [SegmentSize](#)  
*size of flash Execute-Only segment.*
- uint32\_t [SegmentCount](#)  
*flash Execute-Only segment count.*

### 15.2.9.0.0.43 Field Documentation

15.2.9.0.0.43.1 uint32\_t flash\_access\_config\_t::SegmentBase

15.2.9.0.0.43.2 uint32\_t flash\_access\_config\_t::SegmentSize

15.2.9.0.0.43.3 uint32\_t flash\_access\_config\_t::SegmentCount

### 15.2.10 struct flash\_operation\_config\_t

#### Data Fields

- uint32\_t [convertedAddress](#)  
*A converted address for the current flash type.*
- uint32\_t [activeSectorSize](#)  
*A sector size of the current flash type.*
- uint32\_t [activeBlockSize](#)  
*A block size of the current flash type.*
- uint32\_t [blockWriteUnitSize](#)  
*The write unit size.*
- uint32\_t [sectorCmdAddressAligment](#)  
*An erase sector command address alignment.*
- uint32\_t [partCmdAddressAligment](#)  
*A program/verify part command address alignment.*
- 32\_t [resourceCmdAddressAligment](#)  
*A read resource command address alignment.*
- uint32\_t [checkCmdAddressAligment](#)  
*A program check command address alignment.*

**15.2.10.0.0.44 Field Documentation****15.2.10.0.0.44.1** uint32\_t flash\_operation\_config\_t::convertedAddress**15.2.10.0.0.44.2** uint32\_t flash\_operation\_config\_t::activeSectorSize**15.2.10.0.0.44.3** uint32\_t flash\_operation\_config\_t::activeBlockSize**15.2.10.0.0.44.4** uint32\_t flash\_operation\_config\_t::blockWriteUnitSize**15.2.10.0.0.44.5** uint32\_t flash\_operation\_config\_t::sectorCmdAddressAlignent**15.2.10.0.0.44.6** uint32\_t flash\_operation\_config\_t::partCmdAddressAlignent**15.2.10.0.0.44.7** uint32\_t flash\_operation\_config\_t::resourceCmdAddressAlignent**15.2.10.0.0.44.8** uint32\_t flash\_operation\_config\_t::checkCmdAddressAlignent**15.2.11 struct flash\_config\_t**

An instance of this structure is allocated by the user of the flash driver and passed into each of the driver APIs.

**Data Fields**

- uint32\_t [PFlashBlockBase](#)  
*A base address of the first PFlash block.*
- uint32\_t [PFlashTotalSize](#)  
*The size of the combined PFlash block.*
- uint32\_t [PFlashBlockCount](#)  
*A number of PFlash blocks.*
- uint32\_t [PFlashSectorSize](#)  
*The size in bytes of a sector of PFlash.*
- [flash\\_callback\\_t](#) [PFlashCallback](#)  
*The callback function for the flash API.*
- uint32\_t [PFlashAccessSegmentSize](#)  
*A size in bytes of an access segment of PFlash.*
- uint32\_t [PFlashAccessSegmentCount](#)  
*A number of PFlash access segments.*
- uint32\_t \* [flashExecuteInRamFunctionInfo](#)  
*An information structure of the flash execute-in-RAM function.*
- uint32\_t [FlexRAMBlockBase](#)  
*For the FlexNVM device, this is the base address of the FlexRAM For the non-FlexNVM device, this is the base address of the acceleration RAM memory.*
- uint32\_t [FlexRAMTotalSize](#)  
*For the FlexNVM device, this is the size of the FlexRAM For the non-FlexNVM device, this is the size of the acceleration RAM memory.*
- uint32\_t [DFlashBlockBase](#)  
*For the FlexNVM device, this is the base address of the D-Flash memory (FlexNVM memory) For the*

## Macro Definition Documentation

- non-FlexNVM device, this field is unused.*
- uint32\_t [DFlashTotalSize](#)  
*For the FlexNVM device, this is the total size of the FlexNVM memory; For the non-FlexNVM device, this field is unused.*
- uint32\_t [EEPromTotalSize](#)  
*For the FlexNVM device, this is the size in bytes of the EEPROM area which was partitioned from FlexRAM. For the non-FlexNVM device, this field is unused.*
- uint32\_t [FlashMemoryIndex](#)  
*0 - primary flash; 1 - secondary flash*

### 15.2.11.0.0.45 Field Documentation

15.2.11.0.0.45.1 uint32\_t flash\_config\_t::PFlashTotalSize

15.2.11.0.0.45.2 uint32\_t flash\_config\_t::PFlashBlockCount

15.2.11.0.0.45.3 uint32\_t flash\_config\_t::PFlashSectorSize

15.2.11.0.0.45.4 flash\_callback\_t flash\_config\_t::PFlashCallback

15.2.11.0.0.45.5 uint32\_t flash\_config\_t::PFlashAccessSegmentSize

15.2.11.0.0.45.6 uint32\_t flash\_config\_t::PFlashAccessSegmentCount

15.2.11.0.0.45.7 uint32\_t\* flash\_config\_t::flashExecuteInRamFunctionInfo

## 15.3 Macro Definition Documentation

15.3.1 **#define MAKE\_VERSION( *major, minor, bugfix* ) (((major) << 16) | ((minor) << 8) | (bugfix))**

15.3.2 **#define FSL\_FLASH\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 0))**

Version 2.2.0.

15.3.3 **#define FLASH\_SSD\_CONFIG\_ENABLE\_FLEXNVM\_SUPPORT 1**

Enables the FlexNVM support by default.

15.3.4 **#define FLASH\_DRIVER\_IS\_FLASH\_RESIDENT 1**

Used for the flash resident application.



### 15.3.5 #define FLASH\_DRIVER\_IS\_EXPORTED 0

Used for the KSDK application.

### 15.3.6 #define kStatusGroupGeneric 0

### 15.3.7 #define MAKE\_STATUS( group, code ) (((group)\*100) + (code))

### 15.3.8 #define FOUR\_CHAR\_CODE( a, b, c, d ) (((d) << 24) | ((c) << 16) | ((b) << 8) | ((a)))

## 15.4 Enumeration Type Documentation

### 15.4.1 enum \_flash\_driver\_version\_constants

Enumerator

***kFLASH\_DriverVersionName*** Flash driver version name.  
***kFLASH\_DriverVersionMajor*** Major flash driver version.  
***kFLASH\_DriverVersionMinor*** Minor flash driver version.  
***kFLASH\_DriverVersionBugfix*** Bugfix for flash driver version.

### 15.4.2 enum \_flash\_status

Enumerator

***kStatus\_FLASH\_Success*** API is executed successfully.  
***kStatus\_FLASH\_InvalidArgument*** Invalid argument.  
***kStatus\_FLASH\_SizeError*** Error size.  
***kStatus\_FLASH\_AlignmentError*** Parameter is not aligned with the specified baseline.  
***kStatus\_FLASH\_AddressError*** Address is out of range.  
***kStatus\_FLASH\_AccessError*** Invalid instruction codes and out-of bound addresses.  
***kStatus\_FLASH\_ProtectionViolation*** The program/erase operation is requested to execute on protected areas.  
***kStatus\_FLASH\_CommandFailure*** Run-time error during command execution.  
***kStatus\_FLASH\_UnknownProperty*** Unknown property.  
***kStatus\_FLASH\_EraseKeyError*** API erase key is invalid.  
***kStatus\_FLASH\_RegionExecuteOnly*** The current region is execute-only.  
***kStatus\_FLASH\_ExecuteInRamFunctionNotReady*** Execute-in-RAM function is not available.  
***kStatus\_FLASH\_PartitionStatusUpdateFailure*** Failed to update partition status.  
***kStatus\_FLASH\_SetFlexramAsEepromError*** Failed to set FlexRAM as EEPROM.  
***kStatus\_FLASH\_RecoverFlexramAsRamError*** Failed to recover FlexRAM as RAM.  
***kStatus\_FLASH\_SetFlexramAsRamError*** Failed to set FlexRAM as RAM.

## Enumeration Type Documentation

***kStatus\_FLASH\_RecoverFlexramAsEepromError*** Failed to recover FlexRAM as EEPROM.  
***kStatus\_FLASH\_CommandNotSupported*** Flash API is not supported.  
***kStatus\_FLASH\_SwapSystemNotInUninitialized*** Swap system is not in an uninitialized state.  
***kStatus\_FLASH\_SwapIndicatorAddressError*** The swap indicator address is invalid.  
***kStatus\_FLASH\_ReadOnlyProperty*** The flash property is read-only.  
***kStatus\_FLASH\_InvalidPropertyValue*** The flash property value is out of range.  
***kStatus\_FLASH\_InvalidSpeculationOption*** The option of flash prefetch speculation is invalid.

### 15.4.3 enum \_flash\_driver\_api\_keys

#### Note

The resulting value is built with a byte order such that the string being readable in expected order when viewed in a hex editor, if the value is treated as a 32-bit little endian value.

#### Enumerator

***kFLASH\_ApiEraseKey*** Key value used to validate all flash erase APIs.

### 15.4.4 enum flash\_margin\_value\_t

#### Enumerator

***kFLASH\_MarginValueNormal*** Use the 'normal' read level for 1s.  
***kFLASH\_MarginValueUser*** Apply the 'User' margin to the normal read-1 level.  
***kFLASH\_MarginValueFactory*** Apply the 'Factory' margin to the normal read-1 level.  
***kFLASH\_MarginValueInvalid*** Not real margin level, Used to determine the range of valid margin level.

### 15.4.5 enum flash\_security\_state\_t

#### Enumerator

***kFLASH\_SecurityStateNotSecure*** Flash is not secure.  
***kFLASH\_SecurityStateBackdoorEnabled*** Flash backdoor is enabled.  
***kFLASH\_SecurityStateBackdoorDisabled*** Flash backdoor is disabled.

### 15.4.6 enum flash\_protection\_state\_t

Enumerator

***kFLASH\_ProtectionStateUnprotected*** Flash region is not protected.

***kFLASH\_ProtectionStateProtected*** Flash region is protected.

***kFLASH\_ProtectionStateMixed*** Flash is mixed with protected and unprotected region.

### 15.4.7 enum flash\_execute\_only\_access\_state\_t

Enumerator

***kFLASH\_AccessStateUnLimited*** Flash region is unlimited.

***kFLASH\_AccessStateExecuteOnly*** Flash region is execute only.

***kFLASH\_AccessStateMixed*** Flash is mixed with unlimited and execute only region.

### 15.4.8 enum flash\_property\_tag\_t

Enumerator

***kFLASH\_PropertyPflashSectorSize*** Pflash sector size property.

***kFLASH\_PropertyPflashTotalSize*** Pflash total size property.

***kFLASH\_PropertyPflashBlockSize*** Pflash block size property.

***kFLASH\_PropertyPflashBlockCount*** Pflash block count property.

***kFLASH\_PropertyPflashBlockBaseAddr*** Pflash block base address property.

***kFLASH\_PropertyPflashFacSupport*** Pflash fac support property.

***kFLASH\_PropertyPflashAccessSegmentSize*** Pflash access segment size property.

***kFLASH\_PropertyPflashAccessSegmentCount*** Pflash access segment count property.

***kFLASH\_PropertyFlexRamBlockBaseAddr*** FlexRam block base address property.

***kFLASH\_PropertyFlexRamTotalSize*** FlexRam total size property.

***kFLASH\_PropertyDflashSectorSize*** Dflash sector size property.

***kFLASH\_PropertyDflashTotalSize*** Dflash total size property.

***kFLASH\_PropertyDflashBlockSize*** Dflash block size property.

***kFLASH\_PropertyDflashBlockCount*** Dflash block count property.

***kFLASH\_PropertyDflashBlockBaseAddr*** Dflash block base address property.

***kFLASH\_PropertyEepromTotalSize*** EEPROM total size property.

***kFLASH\_PropertyFlashMemoryIndex*** Flash memory index property.

### 15.4.9 enum \_flash\_execute\_in\_ram\_function\_constants

Enumerator

- kFLASH\_ExecuteInRamFunctionMaxSizeInWords*** The maximum size of execute-in-RAM function.
- kFLASH\_ExecuteInRamFunctionTotalNum*** Total number of execute-in-RAM functions.

### 15.4.10 enum flash\_read\_resource\_option\_t

Enumerator

- kFLASH\_ResourceOptionFlashIfr*** Select code for Program flash 0 IFR, Program flash swap 0 IFR, Data flash 0 IFR.
- kFLASH\_ResourceOptionVersionId*** Select code for the version ID.

### 15.4.11 enum \_flash\_read\_resource\_range

Enumerator

- kFLASH\_ResourceRangePflashIfrSizeInBytes*** Pflash IFR size in byte.
- kFLASH\_ResourceRangeVersionIdSizeInBytes*** Version ID IFR size in byte.
- kFLASH\_ResourceRangeVersionIdStart*** Version ID IFR start address.
- kFLASH\_ResourceRangeVersionIdEnd*** Version ID IFR end address.
- kFLASH\_ResourceRangePflashSwapIfrStart*** Pflash swap IFR start address.
- kFLASH\_ResourceRangePflashSwapIfrEnd*** Pflash swap IFR end address.
- kFLASH\_ResourceRangeDflashIfrStart*** Dflash IFR start address.
- kFLASH\_ResourceRangeDflashIfrEnd*** Dflash IFR end address.

### 15.4.12 enum flash\_flexram\_function\_option\_t

Enumerator

- kFLASH\_FlexramFunctionOptionAvailableAsRam*** An option used to make FlexRAM available as RAM.
- kFLASH\_FlexramFunctionOptionAvailableForEeprom*** An option used to make FlexRAM available for EEPROM.

### 15.4.13 enum flash\_swap\_function\_option\_t

Enumerator

- kFLASH\_SwapFunctionOptionEnable*** An option used to enable the Swap function.  
***kFLASH\_SwapFunctionOptionDisable*** An option used to disable the Swap function.

### 15.4.14 enum flash\_swap\_control\_option\_t

Enumerator

- kFLASH\_SwapControlOptionInitializeSystem*** An option used to initialize the Swap system.  
***kFLASH\_SwapControlOptionSetInUpdateState*** An option used to set the Swap in an update state.  
***kFLASH\_SwapControlOptionSetInCompleteState*** An option used to set the Swap in a complete state.  
***kFLASH\_SwapControlOptionReportStatus*** An option used to report the Swap status.  
***kFLASH\_SwapControlOptionDisableSystem*** An option used to disable the Swap status.

### 15.4.15 enum flash\_swap\_state\_t

Enumerator

- kFLASH\_SwapStateUninitialized*** Flash Swap system is in an uninitialized state.  
***kFLASH\_SwapStateReady*** Flash Swap system is in a ready state.  
***kFLASH\_SwapStateUpdate*** Flash Swap system is in an update state.  
***kFLASH\_SwapStateUpdateErased*** Flash Swap system is in an updateErased state.  
***kFLASH\_SwapStateComplete*** Flash Swap system is in a complete state.  
***kFLASH\_SwapStateDisabled*** Flash Swap system is in a disabled state.

### 15.4.16 enum flash\_swap\_block\_status\_t

Enumerator

- kFLASH\_SwapBlockStatusLowerHalfProgramBlocksAtZero*** Swap block status is that lower half program block at zero.  
***kFLASH\_SwapBlockStatusUpperHalfProgramBlocksAtZero*** Swap block status is that upper half program block at zero.

## Function Documentation

### 15.4.17 enum flash\_partition\_flexram\_load\_option\_t

Enumerator

***kFLASH\_PartitionFlexramLoadOptionLoadedWithValidEepromData*** FlexRAM is loaded with valid EEPROM data during reset sequence.

***kFLASH\_PartitionFlexramLoadOptionNotLoaded*** FlexRAM is not loaded during reset sequence.

### 15.4.18 enum flash\_memory\_index\_t

Enumerator

***kFLASH\_MemoryIndexPrimaryFlash*** Current flash memory is primary flash.

***kFLASH\_MemoryIndexSecondaryFlash*** Current flash memory is secondary flash.

## 15.5 Function Documentation

### 15.5.1 status\_t FLASH\_Init ( flash\_config\_t \* config )

This function checks and initializes the Flash module for the other Flash APIs.

Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>config</i> | Pointer to the storage for the driver runtime state. |
|---------------|------------------------------------------------------|

Return values

|                                                   |                                           |
|---------------------------------------------------|-------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.            |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.          |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available. |
| <i>kStatus_FLASH_PartitionStatusUpdateFailure</i> | Failed to update the partition status.    |

### 15.5.2 status\_t FLASH\_SetCallback ( flash\_config\_t \* config, flash\_callback\_t callback )

## Parameters

|                 |                                                      |
|-----------------|------------------------------------------------------|
| <i>config</i>   | Pointer to the storage for the driver runtime state. |
| <i>callback</i> | A callback function to be stored in the driver.      |

## Return values

|                                                       |                                  |
|-------------------------------------------------------|----------------------------------|
| <a href="#"><i>kStatus_FLASH_Success</i></a>          | API was executed successfully.   |
| <a href="#"><i>kStatus_FLASH_Invalid-Argument</i></a> | An invalid argument is provided. |

**15.5.3 status\_t FLASH\_PrepareExecuteInRamFunctions ( flash\_config\_t \* *config* )**

## Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>config</i> | Pointer to the storage for the driver runtime state. |
|---------------|------------------------------------------------------|

## Return values

|                                                       |                                  |
|-------------------------------------------------------|----------------------------------|
| <a href="#"><i>kStatus_FLASH_Success</i></a>          | API was executed successfully.   |
| <a href="#"><i>kStatus_FLASH_Invalid-Argument</i></a> | An invalid argument is provided. |

**15.5.4 status\_t FLASH\_EraseAll ( flash\_config\_t \* *config*, uint32\_t *key* )**

## Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>config</i> | Pointer to the storage for the driver runtime state. |
| <i>key</i>    | A value used to validate all flash erase APIs.       |

## Function Documentation

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_EraseKeyError</i>                | API erase key is invalid.                                               |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during command execution.                                |
| <i>kStatus_FLASH_PartitionStatusUpdateFailure</i> | Failed to update the partition status.                                  |

### 15.5.5 **status\_t FLASH\_Erase ( flash\_config\_t \* config, uint32\_t start, uint32\_t lengthInBytes, uint32\_t key )**

This function erases the appropriate number of flash sectors based on the desired start address and length.

### Parameters

|                      |                                                                                                                                            |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | The pointer to the storage for the driver runtime state.                                                                                   |
| <i>start</i>         | The start address of the desired flash memory to be erased. The start address does not need to be sector-aligned but must be word-aligned. |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words) to be erased. Must be word-aligned.                                                   |
| <i>key</i>           | The value used to validate all flash erase APIs.                                                                                           |



## Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | The parameter is not aligned with the specified baseline.               |
| <i>kStatus_FLASH_AddressError</i>                 | The address is out of range.                                            |
| <i>kStatus_FLASH_EraseKeyError</i>                | The API erase key is invalid.                                           |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.6 **status\_t FLASH\_EraseAllExecuteOnlySegments ( flash\_config\_t \* config, uint32\_t key )**

## Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>config</i> | Pointer to the storage for the driver runtime state. |
| <i>key</i>    | A value used to validate all flash erase APIs.       |

## Function Documentation

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_EraseKeyError</i>                | API erase key is invalid.                                               |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH-ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH-CommandFailure</i>               | Run-time error during command execution.                                |
| <i>kStatus_FLASH-PartitionStatusUpdateFailure</i> | Failed to update the partition status.                                  |

Erases all program flash execute-only segments defined by the FXACC registers.

### Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>config</i> | Pointer to the storage for the driver runtime state. |
| <i>key</i>    | A value used to validate all flash erase APIs.       |

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_EraseKeyError</i>                | API erase key is invalid.                                               |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH-ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH-CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.7 **status\_t FLASH\_Program ( flash\_config\_t \* *config*, uint32\_t *start*, uint32\_t \* *src*, uint32\_t *lengthInBytes* )**

This function programs the flash memory with the desired data for a given flash area as determined by the start address and the length.

## Function Documentation

### Parameters

|                      |                                                                                               |
|----------------------|-----------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                        |
| <i>start</i>         | The start address of the desired flash memory to be programmed. Must be word-aligned.         |
| <i>src</i>           | A pointer to the source buffer of data that is to be programmed into the flash.               |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be programmed. Must be word-aligned. |

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | Parameter is not aligned with the specified baseline.                   |
| <i>kStatus_FLASH_AddressError</i>                 | Address is out of range.                                                |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.8 **status\_t FLASH\_ProgramOnce ( flash\_config\_t \* *config*, uint32\_t *index*, uint32\_t \* *src*, uint32\_t *lengthInBytes* )**

This function programs the Program Once Field with the desired data for a given flash area as determined by the index and length.

### Parameters

|                      |                                                                                               |
|----------------------|-----------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                        |
| <i>index</i>         | The index indicating which area of the Program Once Field to be programmed.                   |
| <i>src</i>           | A pointer to the source buffer of data that is to be programmed into the Program Once Field.  |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be programmed. Must be word-aligned. |

## Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.9 **status\_t FLASH\_ProgramSection ( flash\_config\_t \* *config*, uint32\_t *start*, uint32\_t \* *src*, uint32\_t *lengthInBytes* )**

This function programs the flash memory with the desired data for a given flash area as determined by the start address and length.

## Parameters

|                      |                                                                                               |
|----------------------|-----------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                        |
| <i>start</i>         | The start address of the desired flash memory to be programmed. Must be word-aligned.         |
| <i>src</i>           | A pointer to the source buffer of data that is to be programmed into the flash.               |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be programmed. Must be word-aligned. |

## Function Documentation

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | Parameter is not aligned with specified baseline.                       |
| <i>kStatus_FLASH_AddressError</i>                 | Address is out of range.                                                |
| <i>kStatus_FLASH_SetFlexramAsRamError</i>         | Failed to set flexram as RAM.                                           |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during command execution.                                |
| <i>kStatus_FLASH_RecoverFlexramAsEepromError</i>  | Failed to recover FlexRAM as EEPROM.                                    |

### 15.5.10 **status\_t FLASH\_EepromWrite ( flash\_config\_t \* *config*, uint32\_t *start*, uint8\_t \* *src*, uint32\_t *lengthInBytes* )**

This function programs the emulated EEPROM with the desired data for a given flash area as determined by the start address and length.

### Parameters

|                      |                                                                                               |
|----------------------|-----------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                        |
| <i>start</i>         | The start address of the desired flash memory to be programmed. Must be word-aligned.         |
| <i>src</i>           | A pointer to the source buffer of data that is to be programmed into the flash.               |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be programmed. Must be word-aligned. |

Return values

|                                               |                                                                         |
|-----------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                  | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>          | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AddressError</i>             | Address is out of range.                                                |
| <i>kStatus_FLASH_SetFlexramAsEepromError</i>  | Failed to set flexram as eeprom.                                        |
| <i>kStatus_FLASH_ProtectionViolation</i>      | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_RecoverFlexramAsRamError</i> | Failed to recover the FlexRAM as RAM.                                   |

### 15.5.11 **status\_t FLASH\_ReadResource ( flash\_config\_t \* *config*, uint32\_t *start*, uint32\_t \* *dst*, uint32\_t *lengthInBytes*, flash\_read\_resource\_option\_t *option* )**

This function reads the flash memory with the desired location for a given flash area as determined by the start address and length.

Parameters

|                      |                                                                                         |
|----------------------|-----------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                  |
| <i>start</i>         | The start address of the desired flash memory to be programmed. Must be word-aligned.   |
| <i>dst</i>           | A pointer to the destination buffer of data that is used to store data to be read.      |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be read. Must be word-aligned. |
| <i>option</i>        | The resource option which indicates which area should be read back.                     |

Return values

|                              |                                |
|------------------------------|--------------------------------|
| <i>kStatus_FLASH_Success</i> | API was executed successfully. |
|------------------------------|--------------------------------|

## Function Documentation

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | Parameter is not aligned with the specified baseline.                   |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.12 **status\_t FLASH\_ReadOnce ( flash\_config\_t \* *config*, uint32\_t *index*, uint32\_t \* *dst*, uint32\_t *lengthInBytes* )**

This function reads the read once feild with given index and length.

Parameters

|                      |                                                                                               |
|----------------------|-----------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                        |
| <i>index</i>         | The index indicating the area of program once field to be read.                               |
| <i>dst</i>           | A pointer to the destination buffer of data that is used to store data to be read.            |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be programmed. Must be word-aligned. |

Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |



### 15.5.13 **status\_t FLASH\_GetSecurityState ( flash\_config\_t \* *config*, flash\_security\_state\_t \* *state* )**

This function retrieves the current flash security status, including the security enabling state and the backdoor key enabling state.

Parameters

|               |                                                                       |
|---------------|-----------------------------------------------------------------------|
| <i>config</i> | A pointer to storage for the driver runtime state.                    |
| <i>state</i>  | A pointer to the value returned for the current security status code: |

Return values

|                                                      |                                  |
|------------------------------------------------------|----------------------------------|
| <a href="#"><i>kStatus_FLASH_Success</i></a>         | API was executed successfully.   |
| <a href="#"><i>kStatus_FLASH_InvalidArgument</i></a> | An invalid argument is provided. |

### 15.5.14 **status\_t FLASH\_SecurityBypass ( flash\_config\_t \* *config*, const uint8\_t \* *backdoorKey* )**

If the MCU is in secured state, this function unsecures the MCU by comparing the provided backdoor key with ones in the flash configuration field.

Parameters

|                    |                                                           |
|--------------------|-----------------------------------------------------------|
| <i>config</i>      | A pointer to the storage for the driver runtime state.    |
| <i>backdoorKey</i> | A pointer to the user buffer containing the backdoor key. |

## Function Documentation

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.15 **status\_t FLASH\_VerifyEraseAll ( flash\_config\_t \* *config*, flash\_margin\_value\_t *margin* )**

This function checks whether the flash is erased to the specified read margin level.

### Parameters

|               |                                                        |
|---------------|--------------------------------------------------------|
| <i>config</i> | A pointer to the storage for the driver runtime state. |
| <i>margin</i> | Read margin choice.                                    |

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.16 **status\_t FLASH\_VerifyErase ( flash\_config\_t \* *config*, uint32\_t *start*, uint32\_t *lengthInBytes*, flash\_margin\_value\_t *margin* )**

This function checks the appropriate number of flash sectors based on the desired start address and length to check whether the flash is erased to the specified read margin level.

## Function Documentation

### Parameters

|                      |                                                                                                                                              |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                       |
| <i>start</i>         | The start address of the desired flash memory to be verified. The start address does not need to be sector-aligned but must be word-aligned. |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be verified. Must be word-aligned.                                                  |
| <i>margin</i>        | Read margin choice.                                                                                                                          |

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | Parameter is not aligned with specified baseline.                       |
| <i>kStatus_FLASH_AddressError</i>                 | Address is out of range.                                                |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

**15.5.17 status\_t FLASH\_VerifyProgram ( flash\_config\_t \* *config*, uint32\_t *start*, uint32\_t *lengthInBytes*, const uint32\_t \* *expectedData*, flash\_margin\_value\_t *margin*, uint32\_t \* *failedAddress*, uint32\_t \* *failedData* )**

This function verifies the data programed in the flash memory using the Flash Program Check Command and compares it to the expected data for a given flash area as determined by the start address and length.

## Parameters

|                      |                                                                                                                                                                     |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                                              |
| <i>start</i>         | The start address of the desired flash memory to be verified. Must be word-aligned.                                                                                 |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be verified. Must be word-aligned.                                                                         |
| <i>expectedData</i>  | A pointer to the expected data that is to be verified against.                                                                                                      |
| <i>margin</i>        | Read margin choice.                                                                                                                                                 |
| <i>failedAddress</i> | A pointer to the returned failing address.                                                                                                                          |
| <i>failedData</i>    | A pointer to the returned failing data. Some derivatives do not include failed data as part of the FCCOBx registers. In this case, zeros are returned upon failure. |

## Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | Parameter is not aligned with specified baseline.                       |
| <i>kStatus_FLASH_AddressError</i>                 | Address is out of range.                                                |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

**15.5.18** `status_t FLASH_VerifyEraseAllExecuteOnlySegments ( flash_config_t * config, flash_margin_value_t margin )`

## Function Documentation

### Parameters

|               |                                                        |
|---------------|--------------------------------------------------------|
| <i>config</i> | A pointer to the storage for the driver runtime state. |
| <i>margin</i> | Read margin choice.                                    |

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.19 **status\_t FLASH\_IsProtected ( flash\_config\_t \* *config*, uint32\_t *start*, uint32\_t *lengthInBytes*, flash\_protection\_state\_t \* *protection\_state* )**

This function retrieves the current flash protect status for a given flash area as determined by the start address and length.

### Parameters

|                         |                                                                                                    |
|-------------------------|----------------------------------------------------------------------------------------------------|
| <i>config</i>           | A pointer to the storage for the driver runtime state.                                             |
| <i>start</i>            | The start address of the desired flash memory to be checked. Must be word-aligned.                 |
| <i>lengthInBytes</i>    | The length, given in bytes (not words or long-words) to be checked. Must be word-aligned.          |
| <i>protection_state</i> | A pointer to the value returned for the current protection status code for the desired flash area. |

Return values

|                                      |                                                   |
|--------------------------------------|---------------------------------------------------|
| <i>kStatus_FLASH_Success</i>         | API was executed successfully.                    |
| <i>kStatus_FLASH_InvalidArgument</i> | An invalid argument is provided.                  |
| <i>kStatus_FLASH_AlignmentError</i>  | Parameter is not aligned with specified baseline. |
| <i>kStatus_FLASH_AddressError</i>    | The address is out of range.                      |

### 15.5.20 **status\_t FLASH\_IsExecuteOnly ( flash\_config\_t \* *config*, uint32\_t *start*, uint32\_t *lengthInBytes*, flash\_execute\_only\_access\_state\_t \* *access\_state* )**

This function retrieves the current flash access status for a given flash area as determined by the start address and length.

Parameters

|                      |                                                                                                |
|----------------------|------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                         |
| <i>start</i>         | The start address of the desired flash memory to be checked. Must be word-aligned.             |
| <i>lengthInBytes</i> | The length, given in bytes (not words or long-words), to be checked. Must be word-aligned.     |
| <i>access_state</i>  | A pointer to the value returned for the current access status code for the desired flash area. |

Return values

|                                      |                                                         |
|--------------------------------------|---------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>         | API was executed successfully.                          |
| <i>kStatus_FLASH_InvalidArgument</i> | An invalid argument is provided.                        |
| <i>kStatus_FLASH_AlignmentError</i>  | The parameter is not aligned to the specified baseline. |
| <i>kStatus_FLASH_AddressError</i>    | The address is out of range.                            |

### 15.5.21 **status\_t FLASH\_GetProperty ( flash\_config\_t \* *config*, flash\_property\_tag\_t *whichProperty*, uint32\_t \* *value* )**

## Function Documentation

### Parameters

|                      |                                                                                            |
|----------------------|--------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                     |
| <i>whichProperty</i> | The desired property from the list of properties in enum <code>flash_property_tag_t</code> |
| <i>value</i>         | A pointer to the value returned for the desired flash property.                            |

### Return values

|                                      |                                  |
|--------------------------------------|----------------------------------|
| <i>kStatus_FLASH_Success</i>         | API was executed successfully.   |
| <i>kStatus_FLASH_InvalidArgument</i> | An invalid argument is provided. |
| <i>kStatus_FLASH_UnknownProperty</i> | An unknown property tag.         |

## 15.5.22 `status_t FLASH_SetFlexramFunction ( flash_config_t * config, flash_flexram_function_option_t option )`

### Parameters

|               |                                                        |
|---------------|--------------------------------------------------------|
| <i>config</i> | A pointer to the storage for the driver runtime state. |
| <i>option</i> | The option used to set the work mode of FlexRAM.       |

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |



**15.5.23** `status_t FLASH_SwapControl ( flash_config_t * config, uint32_t address,  
flash_swap_control_option_t option, flash_swap_state_config_t * returnInfo  
)`

## Function Documentation

### Parameters

|                   |                                                                                          |
|-------------------|------------------------------------------------------------------------------------------|
| <i>config</i>     | A pointer to the storage for the driver runtime state.                                   |
| <i>address</i>    | Address used to configure the flash Swap function.                                       |
| <i>option</i>     | The possible option used to configure Flash Swap function or check the flash Swap status |
| <i>returnInfo</i> | A pointer to the data which is used to return the information of flash Swap.             |

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | Parameter is not aligned with specified baseline.                       |
| <i>kStatus_FLASH_SwapIndicatorAddressError</i>    | Swap indicator address is invalid.                                      |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during the command execution.                            |

### 15.5.24 **status\_t FLASH\_Swap ( flash\_config\_t \* *config*, uint32\_t *address*, flash\_swap\_function\_option\_t *option* )**

#### Parameters

|                |                                                        |
|----------------|--------------------------------------------------------|
| <i>config</i>  | A pointer to the storage for the driver runtime state. |
| <i>address</i> | Address used to configure the flash swap function      |

|               |                                                                                               |
|---------------|-----------------------------------------------------------------------------------------------|
| <i>option</i> | The possible option used to configure the Flash Swap function or check the flash Swap status. |
|---------------|-----------------------------------------------------------------------------------------------|

## Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | An invalid argument is provided.                                        |
| <i>kStatus_FLASH_AlignmentError</i>               | Parameter is not aligned with specified baseline.                       |
| <i>kStatus_FLASH_SwapIndicatorAddressError</i>    | Swap indicator address is invalid.                                      |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during command execution.                                |
| <i>kStatus_FLASH_SwapSystemNotInUninitialized</i> | Swap system is not in an uninitialized state.                           |

### 15.5.25 **status\_t FLASH\_ProgramPartition ( flash\_config\_t \* config, flash\_partition\_flexram\_load\_option\_t option, uint32\_t eepromDataSizeCode, uint32\_t flexnvmPartitionCode )**

## Parameters

|                             |                                                                                                                          |
|-----------------------------|--------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>               | Pointer to storage for the driver runtime state.                                                                         |
| <i>option</i>               | The option used to set FlexRAM load behavior during reset.                                                               |
| <i>eepromDataSizeCode</i>   | Determines the amount of FlexRAM used in each of the available EEPROM subsystems.                                        |
| <i>flexnvmPartitionCode</i> | Specifies how to split the FlexNVM block between data flash memory and EEPROM backup memory supporting EEPROM functions. |

## Function Documentation

### Return values

|                                                   |                                                                         |
|---------------------------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_FLASH_Success</i>                      | API was executed successfully.                                          |
| <i>kStatus_FLASH_InvalidArgument</i>              | Invalid argument is provided.                                           |
| <i>kStatus_FLASH_ExecuteInRamFunctionNotReady</i> | Execute-in-RAM function is not available.                               |
| <i>kStatus_FLASH_AccessError</i>                  | Invalid instruction codes and out-of bounds addresses.                  |
| <i>kStatus_FLASH_ProtectionViolation</i>          | The program/erase operation is requested to execute on protected areas. |
| <i>kStatus_FLASH_CommandFailure</i>               | Run-time error during command execution.                                |

### 15.5.26 **status\_t FLASH\_PflashSetProtection ( flash\_config\_t \* *config*, pflash\_protection\_status\_t \* *protectStatus* )**

#### Parameters

|                      |                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to storage for the driver runtime state.                                                                                                                                                                                                                                                                                                                                                                    |
| <i>protectStatus</i> | The expected protect status to set to the PFlash protection register. Each bit is corresponding to protection of 1/32(64) of the total PFlash. The least significant bit is corresponding to the lowest address area of PFlash. The most significant bit is corresponding to the highest address area of PFlash. There are two possible cases as shown below: 0: this area is protected. 1: this area is unprotected. |

### Return values

|                                      |                                          |
|--------------------------------------|------------------------------------------|
| <i>kStatus_FLASH_Success</i>         | API was executed successfully.           |
| <i>kStatus_FLASH_InvalidArgument</i> | An invalid argument is provided.         |
| <i>kStatus_FLASH_CommandFailure</i>  | Run-time error during command execution. |

### 15.5.27 **status\_t FLASH\_PflashGetProtection ( flash\_config\_t \* *config*, pflash\_protection\_status\_t \* *protectStatus* )**

## Parameters

|                      |                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                                                                                                                                                                                                                                                                  |
| <i>protectStatus</i> | Protect status returned by the PFlash IP. Each bit is corresponding to the protection of 1/32(64) of the total PFlash. The least significant bit corresponds to the lowest address area of the PFlash. The most significant bit corresponds to the highest address area of PFlash. There are two possible cases as shown below: 0: this area is protected. 1: this area is unprotected. |

## Return values

|                                      |                                  |
|--------------------------------------|----------------------------------|
| <i>kStatus_FLASH_Success</i>         | API was executed successfully.   |
| <i>kStatus_FLASH_InvalidArgument</i> | An invalid argument is provided. |

### 15.5.28 **status\_t FLASH\_DflashSetProtection ( flash\_config\_t \* *config*, uint8\_t *protectStatus* )**

## Parameters

|                      |                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                                                                                                                                                                                                                                                                                            |
| <i>protectStatus</i> | The expected protect status to set to the DFlash protection register. Each bit corresponds to the protection of the 1/8 of the total DFlash. The least significant bit corresponds to the lowest address area of the DFlash. The most significant bit corresponds to the highest address area of the DFlash. There are two possible cases as shown below: 0: this area is protected. 1: this area is unprotected. |

## Return values

|                                          |                                          |
|------------------------------------------|------------------------------------------|
| <i>kStatus_FLASH_Success</i>             | API was executed successfully.           |
| <i>kStatus_FLASH_InvalidArgument</i>     | An invalid argument is provided.         |
| <i>kStatus_FLASH_CommandNotSupported</i> | Flash API is not supported.              |
| <i>kStatus_FLASH_CommandFailure</i>      | Run-time error during command execution. |

**15.5.29**    **status\_t FLASH\_DflashGetProtection ( flash\_config\_t \* *config*, uint8\_t \* *protectStatus* )**

## Parameters

|                      |                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                                                                                                                                                                                                                                                                            |
| <i>protectStatus</i> | DFlash Protect status returned by the PFlash IP. Each bit corresponds to the protection of the 1/8 of the total DFlash. The least significant bit corresponds to the lowest address area of the DFlash. The most significant bit corresponds to the highest address area of the DFlash, and so on. There are two possible cases as below: 0: this area is protected. 1: this area is unprotected. |

## Return values

|                                          |                                  |
|------------------------------------------|----------------------------------|
| <i>kStatus_FLASH_Success</i>             | API was executed successfully.   |
| <i>kStatus_FLASH_InvalidArgument</i>     | An invalid argument is provided. |
| <i>kStatus_FLASH_CommandNotSupported</i> | Flash API is not supported.      |

### 15.5.30 **status\_t FLASH\_EepromSetProtection ( flash\_config\_t \* *config*, uint8\_t *protectStatus* )**

## Parameters

|                      |                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                                                                                                                                                                                                                                                                                                   |
| <i>protectStatus</i> | The expected protect status to set to the EEPROM protection register. Each bit corresponds to the protection of the 1/8 of the total EEPROM. The least significant bit corresponds to the lowest address area of the EEPROM. The most significant bit corresponds to the highest address area of EEPROM, and so on. There are two possible cases as shown below: 0: this area is protected. 1: this area is unprotected. |

## Return values

|                                          |                                          |
|------------------------------------------|------------------------------------------|
| <i>kStatus_FLASH_Success</i>             | API was executed successfully.           |
| <i>kStatus_FLASH_InvalidArgument</i>     | An invalid argument is provided.         |
| <i>kStatus_FLASH_CommandNotSupported</i> | Flash API is not supported.              |
| <i>kStatus_FLASH_CommandFailure</i>      | Run-time error during command execution. |

**15.5.31** `status_t FLASH_EepromGetProtection ( flash_config_t * config, uint8_t * protectStatus )`



## Parameters

|                      |                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                                                                                                                                                                                                                                                                 |
| <i>protectStatus</i> | DFlash Protect status returned by the PFlash IP. Each bit corresponds to the protection of the 1/8 of the total EEPROM. The least significant bit corresponds to the lowest address area of the EEPROM. The most significant bit corresponds to the highest address area of the EEPROM. There are two possible cases as below: 0: this area is protected. 1: this area is unprotected. |

## Return values

|                                          |                                  |
|------------------------------------------|----------------------------------|
| <i>kStatus_FLASH_Success</i>             | API was executed successfully.   |
| <i>kStatus_FLASH_Invalid-Argument</i>    | An invalid argument is provided. |
| <i>kStatus_FLASH-CommandNotSupported</i> | Flash API is not supported.      |



## Chapter 16

# FlexBus: External Bus Interface Driver

### 16.1 Overview

The KSDK provides a peripheral driver for the Crossbar External Bus Interface (FlexBus) block of Kinetis devices.

A multifunction external bus interface is provided on the device with a basic functionality to interface to slave-only devices. It can be directly connected to the following asynchronous or synchronous devices with little or no additional circuitry.

- External ROMs
- Flash memories
- Programmable logic devices
- Other simple target (slave) devices

For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has up to six general purpose chip-selects, FB\_CS[5:0]. The number of chip selects available depends on the device and its pin configuration.

### 16.2 FlexBus functional operation

To configure the FlexBus driver, use one of the two ways to configure the `flexbus_config_t` structure.

1. Using the `FLEXBUS_GetDefaultConfig()` function.
2. Set parameters in the `flexbus_config_t` structure.

To initialize and configure the FlexBus driver, call the `FLEXBUS_Init()` function and pass a pointer to the `flexbus_config_t` structure.

To de-initialize the FlexBus driver, call the `FLEXBUS_Deinit()` function.

### 16.3 Typical use case and example

This example shows how to write/read to external memory (MRAM) by using the FlexBus module.

```
flexbus_config_t flexbusUserConfig;

FLEXBUS_GetDefaultConfig(&flexbusUserConfig); /* Gets the default configuration. */
/* Configure some parameters when using MRAM */
flexbusUserConfig.waitStates      = 2U;          /* Wait 2 states */
flexbusUserConfig.chipBaseAddress = MRAM_START_ADDRESS; /* MRAM address for using
FlexBus */
flexbusUserConfig.chipBaseAddressMask = 7U;      /* 512 kilobytes memory
size */
FLEXBUS_Init(FB, &flexbusUserConfig); /* Initializes and configures the FlexBus module */

/* Do something */

FLEXBUS_Deinit(FB);
```

## Typical use case and example

### Data Structures

- struct `flexbus_config_t`  
*Configuration structure that the user needs to set. [More...](#)*

### Enumerations

- enum `flexbus_port_size_t` {  
    `kFLEXBUS_4Bytes` = 0x00U,  
    `kFLEXBUS_1Byte` = 0x01U,  
    `kFLEXBUS_2Bytes` = 0x02U }  
*Defines port size for FlexBus peripheral.*
- enum `flexbus_write_address_hold_t` {  
    `kFLEXBUS_Hold1Cycle` = 0x00U,  
    `kFLEXBUS_Hold2Cycles` = 0x01U,  
    `kFLEXBUS_Hold3Cycles` = 0x02U,  
    `kFLEXBUS_Hold4Cycles` = 0x03U }  
*Defines number of cycles to hold address and attributes for FlexBus peripheral.*
- enum `flexbus_read_address_hold_t` {  
    `kFLEXBUS_Hold1Or0Cycles` = 0x00U,  
    `kFLEXBUS_Hold2Or1Cycles` = 0x01U,  
    `kFLEXBUS_Hold3Or2Cycle` = 0x02U,  
    `kFLEXBUS_Hold4Or3Cycle` = 0x03U }  
*Defines number of cycles to hold address and attributes for FlexBus peripheral.*
- enum `flexbus_address_setup_t` {  
    `kFLEXBUS_FirstRisingEdge` = 0x00U,  
    `kFLEXBUS_SecondRisingEdge` = 0x01U,  
    `kFLEXBUS_ThirdRisingEdge` = 0x02U,  
    `kFLEXBUS_FourthRisingEdge` = 0x03U }  
*Address setup for FlexBus peripheral.*
- enum `flexbus_bytelane_shift_t` {  
    `kFLEXBUS_NotShifted` = 0x00U,  
    `kFLEXBUS_Shifted` = 0x01U }  
*Defines byte-lane shift for FlexBus peripheral.*
- enum `flexbus_multiplex_group1_t` {  
    `kFLEXBUS_MultiplexGroup1_FB_ALE` = 0x00U,  
    `kFLEXBUS_MultiplexGroup1_FB_CS1` = 0x01U,  
    `kFLEXBUS_MultiplexGroup1_FB_TS` = 0x02U }  
*Defines multiplex group1 valid signals.*
- enum `flexbus_multiplex_group2_t` {  
    `kFLEXBUS_MultiplexGroup2_FB_CS4` = 0x00U,  
    `kFLEXBUS_MultiplexGroup2_FB_TSI0` = 0x01U,  
    `kFLEXBUS_MultiplexGroup2_FB_BE_31_24` = 0x02U }  
*Defines multiplex group2 valid signals.*
- enum `flexbus_multiplex_group3_t` {  
    `kFLEXBUS_MultiplexGroup3_FB_CS5` = 0x00U,  
    `kFLEXBUS_MultiplexGroup3_FB_TSI1` = 0x01U,  
    `kFLEXBUS_MultiplexGroup3_FB_BE_23_16` = 0x02U }

- *Defines multiplex group3 valid signals.*
- enum `flexbus_multiplex_group4_t` {  
`kFLEXBUS_MultiplexGroup4_FB_TBST` = 0x00U,  
`kFLEXBUS_MultiplexGroup4_FB_CS2` = 0x01U,  
`kFLEXBUS_MultiplexGroup4_FB_BE_15_8` = 0x02U }
- *Defines multiplex group4 valid signals.*
- enum `flexbus_multiplex_group5_t` {  
`kFLEXBUS_MultiplexGroup5_FB_TA` = 0x00U,  
`kFLEXBUS_MultiplexGroup5_FB_CS3` = 0x01U,  
`kFLEXBUS_MultiplexGroup5_FB_BE_7_0` = 0x02U }
- *Defines multiplex group5 valid signals.*

## Driver version

- #define `FSL_FLEXBUS_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 1)`)  
*Version 2.0.1.*

## FlexBus functional operation

- void `FLEXBUS_Init` (`FB_Type *base`, const `flexbus_config_t *config`)  
*Initializes and configures the FlexBus module.*
- void `FLEXBUS_Deinit` (`FB_Type *base`)  
*De-initializes a FlexBus instance.*
- void `FLEXBUS_GetDefaultConfig` (`flexbus_config_t *config`)  
*Initializes the FlexBus configuration structure.*

## 16.4 Data Structure Documentation

### 16.4.1 struct `flexbus_config_t`

#### Data Fields

- uint8\_t `chip`  
*Chip FlexBus for validation.*
- uint8\_t `waitStates`  
*Value of wait states.*
- uint32\_t `chipBaseAddress`  
*Chip base address for using FlexBus.*
- uint32\_t `chipBaseAddressMask`  
*Chip base address mask.*
- bool `writeProtect`  
*Write protected.*
- bool `burstWrite`  
*Burst-Write enable.*
- bool `burstRead`  
*Burst-Read enable.*
- bool `byteEnableMode`  
*Byte-enable mode support.*
- bool `autoAcknowledge`

## Enumeration Type Documentation

- Auto acknowledge setting.*
- bool [extendTransferAddress](#)  
*Extend transfer start/extend address latch enable.*
- bool [secondaryWaitStates](#)  
*Secondary wait states number.*
- [flexbus\\_port\\_size\\_t](#) portSize  
*Port size of transfer.*
- [flexbus\\_bytelane\\_shift\\_t](#) byteLaneShift  
*Byte-lane shift enable.*
- [flexbus\\_write\\_address\\_hold\\_t](#) writeAddressHold  
*Write address hold or deselect option.*
- [flexbus\\_read\\_address\\_hold\\_t](#) readAddressHold  
*Read address hold or deselect option.*
- [flexbus\\_address\\_setup\\_t](#) addressSetup  
*Address setup setting.*
- [flexbus\\_multiplex\\_group1\\_t](#) group1MultiplexControl  
*FlexBus Signal Group 1 Multiplex control.*
- [flexbus\\_multiplex\\_group2\\_t](#) group2MultiplexControl  
*FlexBus Signal Group 2 Multiplex control.*
- [flexbus\\_multiplex\\_group3\\_t](#) group3MultiplexControl  
*FlexBus Signal Group 3 Multiplex control.*
- [flexbus\\_multiplex\\_group4\\_t](#) group4MultiplexControl  
*FlexBus Signal Group 4 Multiplex control.*
- [flexbus\\_multiplex\\_group5\\_t](#) group5MultiplexControl  
*FlexBus Signal Group 5 Multiplex control.*

## 16.5 Macro Definition Documentation

### 16.5.1 #define FSL\_FLEXBUS\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

## 16.6 Enumeration Type Documentation

### 16.6.1 enum flexbus\_port\_size\_t

Enumerator

***kFLEXBUS\_4Bytes*** 32-bit port size  
***kFLEXBUS\_1Byte*** 8-bit port size  
***kFLEXBUS\_2Bytes*** 16-bit port size

### 16.6.2 enum flexbus\_write\_address\_hold\_t

Enumerator

***kFLEXBUS\_Hold1Cycle*** Hold address and attributes one cycles after FB\_CS<sub>n</sub> negates on writes.  
***kFLEXBUS\_Hold2Cycles*** Hold address and attributes two cycles after FB\_CS<sub>n</sub> negates on writes.  
***kFLEXBUS\_Hold3Cycles*** Hold address and attributes three cycles after FB\_CS<sub>n</sub> negates on writes.

***kFLEXBUS\_Hold4Cycles*** Hold address and attributes four cycles after FB\_CS<sub>n</sub> negates on writes.

### 16.6.3 enum flexbus\_read\_address\_hold\_t

Enumerator

***kFLEXBUS\_Hold1Or0Cycles*** Hold address and attributes 1 or 0 cycles on reads.

***kFLEXBUS\_Hold2Or1Cycles*** Hold address and attributes 2 or 1 cycles on reads.

***kFLEXBUS\_Hold3Or2Cycle*** Hold address and attributes 3 or 2 cycles on reads.

***kFLEXBUS\_Hold4Or3Cycle*** Hold address and attributes 4 or 3 cycles on reads.

### 16.6.4 enum flexbus\_address\_setup\_t

Enumerator

***kFLEXBUS\_FirstRisingEdge*** Assert FB\_CS<sub>n</sub> on first rising clock edge after address is asserted.

***kFLEXBUS\_SecondRisingEdge*** Assert FB\_CS<sub>n</sub> on second rising clock edge after address is asserted.

***kFLEXBUS\_ThirdRisingEdge*** Assert FB\_CS<sub>n</sub> on third rising clock edge after address is asserted.

***kFLEXBUS\_FourthRisingEdge*** Assert FB\_CS<sub>n</sub> on fourth rising clock edge after address is asserted.

### 16.6.5 enum flexbus\_bytelane\_shift\_t

Enumerator

***kFLEXBUS\_NotShifted*** Not shifted. Data is left-justified on FB\_AD

***kFLEXBUS\_Shifted*** Shifted. Data is right justified on FB\_AD

### 16.6.6 enum flexbus\_multiplex\_group1\_t

Enumerator

***kFLEXBUS\_MultiplexGroup1\_FB\_ALE*** FB\_ALE.

***kFLEXBUS\_MultiplexGroup1\_FB\_CS1*** FB\_CS1.

***kFLEXBUS\_MultiplexGroup1\_FB\_TS*** FB\_TS.

### 16.6.7 enum flexbus\_multiplex\_group2\_t

Enumerator

*kFLEXBUS\_MultiplexGroup2\_FB\_CS4* FB\_CS4.  
*kFLEXBUS\_MultiplexGroup2\_FB\_TSIZ0* FB\_TSIZ0.  
*kFLEXBUS\_MultiplexGroup2\_FB\_BE\_31\_24* FB\_BE\_31\_24.

### 16.6.8 enum flexbus\_multiplex\_group3\_t

Enumerator

*kFLEXBUS\_MultiplexGroup3\_FB\_CS5* FB\_CS5.  
*kFLEXBUS\_MultiplexGroup3\_FB\_TSIZ1* FB\_TSIZ1.  
*kFLEXBUS\_MultiplexGroup3\_FB\_BE\_23\_16* FB\_BE\_23\_16.

### 16.6.9 enum flexbus\_multiplex\_group4\_t

Enumerator

*kFLEXBUS\_MultiplexGroup4\_FB\_TBST* FB\_TBST.  
*kFLEXBUS\_MultiplexGroup4\_FB\_CS2* FB\_CS2.  
*kFLEXBUS\_MultiplexGroup4\_FB\_BE\_15\_8* FB\_BE\_15\_8.

### 16.6.10 enum flexbus\_multiplex\_group5\_t

Enumerator

*kFLEXBUS\_MultiplexGroup5\_FB\_TA* FB\_TA.  
*kFLEXBUS\_MultiplexGroup5\_FB\_CS3* FB\_CS3.  
*kFLEXBUS\_MultiplexGroup5\_FB\_BE\_7\_0* FB\_BE\_7\_0.

## 16.7 Function Documentation

### 16.7.1 void FLEXBUS\_Init ( FB\_Type \* *base*, const flexbus\_config\_t \* *config* )

This function enables the clock gate for FlexBus module. Only chip 0 is validated and set to known values. Other chips are disabled. Note that in this function, certain parameters, depending on external memories, must be set before using the [FLEXBUS\\_Init\(\)](#) function. This example shows how to set up the `uart_state_t` and the `flexbus_config_t` parameters and how to call the `FLEXBUS_Init` function by passing in these parameters.



```

flexbus_config_t flexbusConfig;
FLEXBUS_GetDefaultConfig(&flexbusConfig);
flexbusConfig.waitStates      = 2U;
flexbusConfig.chipBaseAddress = 0x60000000U;
flexbusConfig.chipBaseAddressMask = 7U;
FLEXBUS_Init(FB, &flexbusConfig);

```

#### Parameters

|               |                                        |
|---------------|----------------------------------------|
| <i>base</i>   | FlexBus peripheral address.            |
| <i>config</i> | Pointer to the configuration structure |

### 16.7.2 void FLEXBUS\_Deinit ( FB\_Type \* *base* )

This function disables the clock gate of the FlexBus module clock.

#### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | FlexBus peripheral address. |
|-------------|-----------------------------|

### 16.7.3 void FLEXBUS\_GetDefaultConfig ( flexbus\_config\_t \* *config* )

This function initializes the FlexBus configuration structure to default value. The default values are.

```

fbConfig->chip                = 0;
fbConfig->writeProtect         = 0;
fbConfig->burstWrite           = 0;
fbConfig->burstRead            = 0;
fbConfig->byteEnableMode       = 0;
fbConfig->autoAcknowledge       = true;
fbConfig->extendTransferAddress = 0;
fbConfig->secondaryWaitStates   = 0;
fbConfig->byteLaneShift         = kFLEXBUS_NotShifted;
fbConfig->writeAddressHold      = kFLEXBUS_Hold1Cycle;
fbConfig->readAddressHold       = kFLEXBUS_Hold1Or0Cycles;
fbConfig->addressSetup          = kFLEXBUS_FirstRisingEdge;
fbConfig->portSize              = kFLEXBUS_1Byte;
fbConfig->group1MultiplexControl = kFLEXBUS_MultiplexGroup1_FB_ALE;
fbConfig->group2MultiplexControl = kFLEXBUS_MultiplexGroup2_FB_CS4 ;
fbConfig->group3MultiplexControl = kFLEXBUS_MultiplexGroup3_FB_CS5;
fbConfig->group4MultiplexControl = kFLEXBUS_MultiplexGroup4_FB_TBST;
fbConfig->group5MultiplexControl = kFLEXBUS_MultiplexGroup5_FB_TA;

```

## Function Documentation

### Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>config</i> | Pointer to the initialization structure. |
|---------------|------------------------------------------|

### See Also

[FLEXBUS\\_Init](#)



## Chapter 17

# FlexCAN: Flex Controller Area Network Driver

### 17.1 Overview

The KSDK provides a peripheral driver for the Flex Controller Area Network (FlexCAN) module of Kinetis devices.

### Modules

- [FlexCAN Driver](#)
- [FlexCAN eDMA Driver](#)

## 17.2 FlexCAN Driver

### 17.2.1 Overview

This section describes the programming interface of the FlexCAN driver. The FlexCAN driver configures FlexCAN module and provides functional and transactional interfaces to build the FlexCAN application.

### 17.2.2 Typical use case

#### 17.2.2.1 Message Buffer Send Operation

```
flexcan_config_t flexcanConfig;
flexcan_frame_t txFrame;

/* Init FlexCAN module. */
FLEXCAN_GetDefaultConfig(&flexcanConfig);
FLEXCAN_Init(EXAMPLE_CAN, &flexcanConfig);

/* Enable FlexCAN module. */
FLEXCAN_Enable(EXAMPLE_CAN, true);

/* Sets up the transmit message buffer. */
FLEXCAN_SetTxMbConfig(EXAMPLE_CAN, TX_MESSAGE_BUFFER_INDEX, true);

/* Prepares the transmit frame for sending. */
txFrame.format = KFLEXCAN_FrameFormatStandard;
txFrame.type = KFLEXCAN_FrameTypeData;
txFrame.id = FLEXCAN_ID_STD(0x123);
txFrame.length = 8;
txFrame.dataWord0 = CAN_WORD0_DATA_BYTE_0(0x11) |
                    CAN_WORD0_DATA_BYTE_1(0x22) |
                    CAN_WORD0_DATA_BYTE_2(0x33) |
                    CAN_WORD0_DATA_BYTE_3(0x44);
txFrame.dataWord1 = CAN_WORD1_DATA_BYTE_4(0x55) |
                    CAN_WORD1_DATA_BYTE_5(0x66) |
                    CAN_WORD1_DATA_BYTE_6(0x77) |
                    CAN_WORD1_DATA_BYTE_7(0x88);

/* Writes a transmit message buffer to send a CAN Message. */
FLEXCAN_WriteTxMb(EXAMPLE_CAN, TX_MESSAGE_BUFFER_INDEX, &txFrame);

/* Waits until the transmit message buffer is empty. */
while (!FLEXCAN_GetMbStatusFlags(EXAMPLE_CAN, 1 << TX_MESSAGE_BUFFER_INDEX));

/* Cleans the transmit message buffer empty status. */
FLEXCAN_ClearMbStatusFlags(EXAMPLE_CAN, 1 << TX_MESSAGE_BUFFER_INDEX);
```

#### 17.2.2.2 Message Buffer Receive Operation

```
flexcan_config_t flexcanConfig;
flexcan_frame_t rxFrame;

/* Initializes the FlexCAN module. */
FLEXCAN_GetDefaultConfig(&flexcanConfig);
FLEXCAN_Init(EXAMPLE_CAN, &flexcanConfig);

/* Enables the FlexCAN module. */
FLEXCAN_Enable(EXAMPLE_CAN, true);

/* Sets up the receive message buffer. */
```

```

mbConfig.format      = KFLEXCAN_FrameFormatStandard;
mbConfig.type        = KFLEXCAN_FrameTypeData;
mbConfig.id          = FLEXCAN_ID_STD(0x123);
FLEXCAN_SetRxMbConfig(EXAMPLE_CAN, RX_MESSAGE_BUFFER_INDEX, &mbConfig, true);

/* Waits until the receive message buffer is full. */
while (!FLEXCAN_GetMbStatusFlags(EXAMPLE_CAN, 1 << RX_MESSAGE_BUFFER_INDEX));

/* Reads the received message from the receive message buffer. */
FLEXCAN_ReadRxMb(EXAMPLE_CAN, RX_MESSAGE_BUFFER_INDEX, &rxFrame);

/* Cleans the receive message buffer full status. */
FLEXCAN_ClearMbStatusFlags(EXAMPLE_CAN, 1 << RX_MESSAGE_BUFFER_INDEX);

```

### 17.2.2.3 Receive FIFO Operation

```

uint32_t rxFifoFilter[] = {FLEXCAN_RX_FIFO_STD_FILTER_TYPE_A(0x321, 0, 0),
                          FLEXCAN_RX_FIFO_STD_FILTER_TYPE_A(0x321, 1, 0),
                          FLEXCAN_RX_FIFO_STD_FILTER_TYPE_A(0x123, 0, 0),
                          FLEXCAN_RX_FIFO_STD_FILTER_TYPE_A(0x123, 1, 0)}
;

flexcan_config_t flexcanConfig;
flexcan_frame_t rxFrame;

/* Initializes the FlexCAN module. */
FLEXCAN_GetDefaultConfig(&flexcanConfig);
FLEXCAN_Init(EXAMPLE_CAN, &flexcanConfig);

/* Enables the FlexCAN module. */
FLEXCAN_Enable(EXAMPLE_CAN, true);

/* Sets up the receive FIFO. */
rxFifoConfig.idFilterTable = rxFifoFilter;
rxFifoConfig.idFilterType  = KFLEXCAN_RxFifoFilterTypeA;
rxFifoConfig.idFilterNum   = sizeof(rxFifoFilter) / sizeof(rxFifoFilter[0]);
rxFifoConfig.priority      = KFLEXCAN_RxFifoPrioHigh;
FLEXCAN_SetRxFifoConfig(EXAMPLE_CAN, &rxFifoConfig, true);

/* Waits until the receive FIFO becomes available. */
while (!FLEXCAN_GetMbStatusFlags(EXAMPLE_CAN, KFLEXCAN_RxFifoFrameAvlFlag));

/* Reads the message from the receive FIFO. */
FLEXCAN_ReadRxFifo(EXAMPLE_CAN, &rxFrame);

/* Cleans the receive FIFO available status. */
FLEXCAN_ClearMbStatusFlags(EXAMPLE_CAN, KFLEXCAN_RxFifoFrameAvlFlag);

```

## Data Structures

- struct `flexcan_frame_t`  
*FlexCAN message frame structure. [More...](#)*
- struct `flexcan_config_t`  
*FlexCAN module configuration structure. [More...](#)*
- struct `flexcan_timing_config_t`  
*FlexCAN protocol timing characteristic configuration structure. [More...](#)*
- struct `flexcan_rx_mb_config_t`  
*FlexCAN Receive Message Buffer configuration structure. [More...](#)*
- struct `flexcan_rx_fifo_config_t`

## FlexCAN Driver

- *FlexCAN Rx FIFO configuration structure. [More...](#)*
- struct `flexcan_mb_transfer_t`  
*FlexCAN Message Buffer transfer. [More...](#)*
- struct `flexcan_fifo_transfer_t`  
*FlexCAN Rx FIFO transfer. [More...](#)*
- struct `flexcan_handle_t`  
*FlexCAN handle structure. [More...](#)*

## Macros

- #define `FLEXCAN_ID_STD(id)` (((uint32\_t)((uint32\_t)(id)) << CAN\_ID\_STD\_SHIFT)) & CAN\_ID\_STD\_MASK)  
*FlexCAN Frame ID helper macro.*
- #define `FLEXCAN_ID_EXT(id)`  
*Extend Frame ID helper macro.*
- #define `FLEXCAN_RX_MB_STD_MASK(id, rtr, ide)`  
*FlexCAN Rx Message Buffer Mask helper macro.*
- #define `FLEXCAN_RX_MB_EXT_MASK(id, rtr, ide)`  
*Extend Rx Message Buffer Mask helper macro.*
- #define `FLEXCAN_RX_FIFO_STD_MASK_TYPE_A(id, rtr, ide)`  
*FlexCAN Rx FIFO Mask helper macro.*
- #define `FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_HIGH(id, rtr, ide)`  
*Standard Rx FIFO Mask helper macro Type B upper part helper macro.*
- #define `FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_LOW(id, rtr, ide)`  
*Standard Rx FIFO Mask helper macro Type B lower part helper macro.*
- #define `FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_HIGH(id)` ((FLEXCAN\_ID\_STD(id) & 0x7F8) << 21)  
*Standard Rx FIFO Mask helper macro Type C upper part helper macro.*
- #define `FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_HIGH(id)` ((FLEXCAN\_ID\_STD(id) & 0x7F8) << 13)  
*Standard Rx FIFO Mask helper macro Type C mid-upper part helper macro.*
- #define `FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_LOW(id)` ((FLEXCAN\_ID\_STD(id) & 0x7F8) << 5)  
*Standard Rx FIFO Mask helper macro Type C mid-lower part helper macro.*
- #define `FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_LOW(id)` ((FLEXCAN\_ID\_STD(id) & 0x7F8) >> 3)  
*Standard Rx FIFO Mask helper macro Type C lower part helper macro.*
- #define `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_A(id, rtr, ide)`  
*Extend Rx FIFO Mask helper macro Type A helper macro.*
- #define `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_HIGH(id, rtr, ide)`  
*Extend Rx FIFO Mask helper macro Type B upper part helper macro.*
- #define `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_LOW(id, rtr, ide)`  
*Extend Rx FIFO Mask helper macro Type B lower part helper macro.*
- #define `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_HIGH(id)` ((FLEXCAN\_ID\_EXT(id) & 0x1FE00000) << 3)  
*Extend Rx FIFO Mask helper macro Type C upper part helper macro.*
- #define `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_HIGH(id)`  
*Extend Rx FIFO Mask helper macro Type C mid-upper part helper macro.*
- #define `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_LOW(id)`

- *Extend Rx FIFO Mask helper macro Type C mid-lower part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_LOW(id)` (((FLEXCAN\_ID\_EXT(id) & 0x1FE00000) >> 21)
- *Extend Rx FIFO Mask helper macro Type C lower part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_STD_FILTER_TYPE_A(id, rtr, ide)` `FLEXCAN_RX_FIFO_STD_MASK_TYPE_A(id, rtr, ide)`
- *FlexCAN Rx FIFO Filter helper macro.*  
 • #define `FLEXCAN_RX_FIFO_STD_FILTER_TYPE_B_HIGH(id, rtr, ide)`
- *Standard Rx FIFO Filter helper macro Type B upper part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_STD_FILTER_TYPE_B_LOW(id, rtr, ide)`
- *Standard Rx FIFO Filter helper macro Type B lower part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_HIGH(id)`
- *Standard Rx FIFO Filter helper macro Type C upper part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_MID_HIGH(id)`
- *Standard Rx FIFO Filter helper macro Type C mid-upper part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_MID_LOW(id)`
- *Standard Rx FIFO Filter helper macro Type C mid-lower part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_LOW(id)` `FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_LOW(id)`
- *Standard Rx FIFO Filter helper macro Type C lower part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_A(id, rtr, ide)` `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_A(id, rtr, ide)`
- *Extend Rx FIFO Filter helper macro Type A helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_B_HIGH(id, rtr, ide)`
- *Extend Rx FIFO Filter helper macro Type B upper part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_B_LOW(id, rtr, ide)`
- *Extend Rx FIFO Filter helper macro Type B lower part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_HIGH(id)` `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_HIGH(id)`
- *Extend Rx FIFO Filter helper macro Type C upper part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_MID_HIGH(id)`
- *Extend Rx FIFO Filter helper macro Type C mid-upper part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_MID_LOW(id)`
- *Extend Rx FIFO Filter helper macro Type C mid-lower part helper macro.*  
 • #define `FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_LOW(id)` `FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_LOW(id)`
- *Extend Rx FIFO Filter helper macro Type C lower part helper macro.*

## Typedefs

- typedef void(\* `flexcan_transfer_callback_t`)(CAN\_Type \*base, flexcan\_handle\_t \*handle, status\_t status, uint32\_t result, void \*userData)  
*FlexCAN transfer callback function.*

## Enumerations

- enum `_flexcan_status` {  
`kStatus_FLEXCAN_TxBusy` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 0),  
`kStatus_FLEXCAN_TxIdle` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 1),  
`kStatus_FLEXCAN_TxSwitchToRx`,  
`kStatus_FLEXCAN_RxBusy` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 3),  
`kStatus_FLEXCAN_RxIdle` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 4),  
`kStatus_FLEXCAN_RxOverflow` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 5),  
`kStatus_FLEXCAN_RxFifoBusy` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 6),  
`kStatus_FLEXCAN_RxFifoIdle` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 7),  
`kStatus_FLEXCAN_RxFifoOverflow` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 8),  
`kStatus_FLEXCAN_RxFifoWarning` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 9),  
`kStatus_FLEXCAN_ErrorStatus` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 10),  
`kStatus_FLEXCAN_UnHandled` = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 11) }  
*FlexCAN transfer status.*
- enum `flexcan_frame_format_t` {  
`kFLEXCAN_FrameFormatStandard` = 0x0U,  
`kFLEXCAN_FrameFormatExtend` = 0x1U }  
*FlexCAN frame format.*
- enum `flexcan_frame_type_t` {  
`kFLEXCAN_FrameTypeData` = 0x0U,  
`kFLEXCAN_FrameTypeRemote` = 0x1U }  
*FlexCAN frame type.*
- enum `flexcan_clock_source_t` {  
`kFLEXCAN_ClkSrcOsc` = 0x0U,  
`kFLEXCAN_ClkSrcPeri` = 0x1U }  
*FlexCAN clock source.*
- enum `flexcan_rx_fifo_filter_type_t` {  
`kFLEXCAN_RxFifoFilterTypeA` = 0x0U,  
`kFLEXCAN_RxFifoFilterTypeB`,  
`kFLEXCAN_RxFifoFilterTypeC`,  
`kFLEXCAN_RxFifoFilterTypeD` = 0x3U }  
*FlexCAN Rx Fifo Filter type.*
- enum `flexcan_rx_fifo_priority_t` {  
`kFLEXCAN_RxFifoPrioLow` = 0x0U,  
`kFLEXCAN_RxFifoPrioHigh` = 0x1U }  
*FlexCAN Rx FIFO priority.*
- enum `_flexcan_interrupt_enable` {  
`kFLEXCAN_BusOffInterruptEnable` = CAN\_CTRL1\_BOFFMSK\_MASK,  
`kFLEXCAN_ErrorInterruptEnable` = CAN\_CTRL1\_ERRMSK\_MASK,  
`kFLEXCAN_RxWarningInterruptEnable` = CAN\_CTRL1\_RWRNMSK\_MASK,  
`kFLEXCAN_TxWarningInterruptEnable` = CAN\_CTRL1\_TWRNMSK\_MASK,  
`kFLEXCAN_WakeUpInterruptEnable` = CAN\_MCR\_WAKMSK\_MASK }  
*FlexCAN interrupt configuration structure, default settings all disabled.*
- enum `_flexcan_flags` {



```

kFLEXCAN_SynchFlag = CAN_ESR1_SYNCH_MASK,
kFLEXCAN_TxWarningIntFlag = CAN_ESR1_TWRNINT_MASK,
kFLEXCAN_RxWarningIntFlag = CAN_ESR1_RWRNINT_MASK,
kFLEXCAN_TxErrorWarningFlag = CAN_ESR1_TXWRN_MASK,
kFLEXCAN_RxErrorWarningFlag = CAN_ESR1_RXWRN_MASK,
kFLEXCAN_IdleFlag = CAN_ESR1_IDLE_MASK,
kFLEXCAN_FaultConfinementFlag = CAN_ESR1_FLTCONF_MASK,
kFLEXCAN_TransmittingFlag = CAN_ESR1_TX_MASK,
kFLEXCAN_ReceivingFlag = CAN_ESR1_RX_MASK,
kFLEXCAN_BusOffIntFlag = CAN_ESR1_BOFFINT_MASK,
kFLEXCAN_ErrorIntFlag = CAN_ESR1_ERRINT_MASK,
kFLEXCAN_WakeUpIntFlag = CAN_ESR1_WAKINT_MASK,
kFLEXCAN_ErrorFlag }

```

*FlexCAN status flags.*

- enum `_flexcan_error_flags` {
 

```

kFLEXCAN_StuffingError = CAN_ESR1_STFERR_MASK,
kFLEXCAN_FormError = CAN_ESR1_FRMERR_MASK,
kFLEXCAN_CrcError = CAN_ESR1_CRCERR_MASK,
kFLEXCAN_AckError = CAN_ESR1_ACKERR_MASK,
kFLEXCAN_Bit0Error = CAN_ESR1_BIT0ERR_MASK,
kFLEXCAN_Bit1Error = CAN_ESR1_BIT1ERR_MASK }

```

*FlexCAN error status flags.*

- enum `_flexcan_rx_fifo_flags` {
 

```

kFLEXCAN_RxFifoOverflowFlag = CAN_IFLAG1_BUF7I_MASK,
kFLEXCAN_RxFifoWarningFlag = CAN_IFLAG1_BUF6I_MASK,
kFLEXCAN_RxFifoFrameAvlFlag = CAN_IFLAG1_BUF5I_MASK }

```

*FlexCAN Rx FIFO status flags.*

## Driver version

- #define `FLEXCAN_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 0)`)  
*FlexCAN driver version 2.1.0.*

## Initialization and deinitialization

- void `FLEXCAN_Init` (`CAN_Type *base`, const `flexcan_config_t *config`, `uint32_t sourceClock_Hz`)  
*Initializes a FlexCAN instance.*
- void `FLEXCAN_Deinit` (`CAN_Type *base`)  
*De-initializes a FlexCAN instance.*
- void `FLEXCAN_GetDefaultConfig` (`flexcan_config_t *config`)  
*Gets the default configuration structure.*

### Configuration.

- void [FLEXCAN\\_SetTimingConfig](#) (CAN\_Type \*base, const [flexcan\\_timing\\_config\\_t](#) \*config)  
*Sets the FlexCAN protocol timing characteristic.*
- void [FLEXCAN\\_SetRxMbGlobalMask](#) (CAN\_Type \*base, uint32\_t mask)  
*Sets the FlexCAN receive message buffer global mask.*
- void [FLEXCAN\\_SetRxFifoGlobalMask](#) (CAN\_Type \*base, uint32\_t mask)  
*Sets the FlexCAN receive FIFO global mask.*
- void [FLEXCAN\\_SetRxIndividualMask](#) (CAN\_Type \*base, uint8\_t maskIdx, uint32\_t mask)  
*Sets the FlexCAN receive individual mask.*
- void [FLEXCAN\\_SetTxMbConfig](#) (CAN\_Type \*base, uint8\_t mbIdx, bool enable)  
*Configures a FlexCAN transmit message buffer.*
- void [FLEXCAN\\_SetRxMbConfig](#) (CAN\_Type \*base, uint8\_t mbIdx, const [flexcan\\_rx\\_mb\\_config\\_t](#) \*config, bool enable)  
*Configures a FlexCAN Receive Message Buffer.*
- void [FLEXCAN\\_SetRxFifoConfig](#) (CAN\_Type \*base, const [flexcan\\_rx\\_fifo\\_config\\_t](#) \*config, bool enable)  
*Configures the FlexCAN Rx FIFO.*

### Status

- static uint32\_t [FLEXCAN\\_GetStatusFlags](#) (CAN\_Type \*base)  
*Gets the FlexCAN module interrupt flags.*
- static void [FLEXCAN\\_ClearStatusFlags](#) (CAN\_Type \*base, uint32\_t mask)  
*Clears status flags with the provided mask.*
- static void [FLEXCAN\\_GetBusErrCount](#) (CAN\_Type \*base, uint8\_t \*txErrBuf, uint8\_t \*rxErrBuf)  
*Gets the FlexCAN Bus Error Counter value.*
- static uint32\_t [FLEXCAN\\_GetMbStatusFlags](#) (CAN\_Type \*base, uint32\_t mask)  
*Gets the FlexCAN Message Buffer interrupt flags.*
- static void [FLEXCAN\\_ClearMbStatusFlags](#) (CAN\_Type \*base, uint32\_t mask)  
*Clears the FlexCAN Message Buffer interrupt flags.*

### Interrupts

- static void [FLEXCAN\\_EnableInterrupts](#) (CAN\_Type \*base, uint32\_t mask)  
*Enables FlexCAN interrupts according to the provided mask.*
- static void [FLEXCAN\\_DisableInterrupts](#) (CAN\_Type \*base, uint32\_t mask)  
*Disables FlexCAN interrupts according to the provided mask.*
- static void [FLEXCAN\\_EnableMbInterrupts](#) (CAN\_Type \*base, uint32\_t mask)  
*Enables FlexCAN Message Buffer interrupts.*
- static void [FLEXCAN\\_DisableMbInterrupts](#) (CAN\_Type \*base, uint32\_t mask)  
*Disables FlexCAN Message Buffer interrupts.*

### Bus Operations

- static void [FLEXCAN\\_Enable](#) (CAN\_Type \*base, bool enable)  
*Enables or disables the FlexCAN module operation.*

- status\_t [FLEXCAN\\_WriteTxMb](#) (CAN\_Type \*base, uint8\_t mbIdx, const flexcan\_frame\_t \*txFrame)  
*Writes a FlexCAN Message to the Transmit Message Buffer.*
- status\_t [FLEXCAN\\_ReadRxMb](#) (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_frame\_t \*rxFrame)  
*Reads a FlexCAN Message from Receive Message Buffer.*
- status\_t [FLEXCAN\\_ReadRxFifo](#) (CAN\_Type \*base, flexcan\_frame\_t \*rxFrame)  
*Reads a FlexCAN Message from Rx FIFO.*

## Transactional

- status\_t [FLEXCAN\\_TransferSendBlocking](#) (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_frame\_t \*txFrame)  
*Performs a polling send transaction on the CAN bus.*
- status\_t [FLEXCAN\\_TransferReceiveBlocking](#) (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_frame\_t \*rxFrame)  
*Performs a polling receive transaction on the CAN bus.*
- status\_t [FLEXCAN\\_TransferReceiveFifoBlocking](#) (CAN\_Type \*base, flexcan\_frame\_t \*rxFrame)  
*Performs a polling receive transaction from Rx FIFO on the CAN bus.*
- void [FLEXCAN\\_TransferCreateHandle](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_transfer\_callback\_t callback, void \*userData)  
*Initializes the FlexCAN handle.*
- status\_t [FLEXCAN\\_TransferSendNonBlocking](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_mb\_transfer\_t \*xfer)  
*Sends a message using IRQ.*
- status\_t [FLEXCAN\\_TransferReceiveNonBlocking](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_mb\_transfer\_t \*xfer)  
*Receives a message using IRQ.*
- status\_t [FLEXCAN\\_TransferReceiveFifoNonBlocking](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_fifo\_transfer\_t \*xfer)  
*Receives a message from Rx FIFO using IRQ.*
- void [FLEXCAN\\_TransferAbortSend](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle, uint8\_t mbIdx)  
*Aborts the interrupt driven message send process.*
- void [FLEXCAN\\_TransferAbortReceive](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle, uint8\_t mbIdx)  
*Aborts the interrupt driven message receive process.*
- void [FLEXCAN\\_TransferAbortReceiveFifo](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle)  
*Aborts the interrupt driven message receive from Rx FIFO process.*
- void [FLEXCAN\\_TransferHandleIRQ](#) (CAN\_Type \*base, flexcan\_handle\_t \*handle)  
*FlexCAN IRQ handle function.*

### 17.2.3 Data Structure Documentation

#### 17.2.3.1 struct flexcan\_frame\_t

##### 17.2.3.1.0.46 Field Documentation

17.2.3.1.0.46.1 uint32\_t flexcan\_frame\_t::timestamp

17.2.3.1.0.46.2 uint32\_t flexcan\_frame\_t::length

17.2.3.1.0.46.3 uint32\_t flexcan\_frame\_t::type

17.2.3.1.0.46.4 uint32\_t flexcan\_frame\_t::format

17.2.3.1.0.46.5 uint32\_t flexcan\_frame\_t::\_\_pad0\_\_

17.2.3.1.0.46.6 uint32\_t flexcan\_frame\_t::idhit

17.2.3.1.0.46.7 uint32\_t flexcan\_frame\_t::id

17.2.3.1.0.46.8 uint32\_t flexcan\_frame\_t::dataWord0

17.2.3.1.0.46.9 uint32\_t flexcan\_frame\_t::dataWord1

17.2.3.1.0.46.10 uint8\_t flexcan\_frame\_t::dataByte3

17.2.3.1.0.46.11 uint8\_t flexcan\_frame\_t::dataByte2

17.2.3.1.0.46.12 uint8\_t flexcan\_frame\_t::dataByte1

17.2.3.1.0.46.13 uint8\_t flexcan\_frame\_t::dataByte0

17.2.3.1.0.46.14 uint8\_t flexcan\_frame\_t::dataByte7

17.2.3.1.0.46.15 uint8\_t flexcan\_frame\_t::dataByte6

17.2.3.1.0.46.16 uint8\_t flexcan\_frame\_t::dataByte5

17.2.3.1.0.46.17 uint8\_t flexcan\_frame\_t::dataByte4

#### 17.2.3.2 struct flexcan\_config\_t

##### Data Fields

- uint32\_t [baudRate](#)  
*FlexCAN baud rate in bps.*
- [flexcan\\_clock\\_source\\_t](#) clkSrc  
*Clock source for FlexCAN Protocol Engine.*
- uint8\_t [maxMbNum](#)  
*The maximum number of Message Buffers used by user.*

- bool [enableLoopBack](#)  
*Enable or Disable Loop Back Self Test Mode.*
- bool [enableSelfWakeup](#)  
*Enable or Disable Self Wakeup Mode.*
- bool [enableIndividMask](#)  
*Enable or Disable Rx Individual Mask.*

#### 17.2.3.2.0.47 Field Documentation

17.2.3.2.0.47.1 `uint32_t flexcan_config_t::baudRate`

17.2.3.2.0.47.2 `flexcan_clock_source_t flexcan_config_t::clkSrc`

17.2.3.2.0.47.3 `uint8_t flexcan_config_t::maxMbNum`

17.2.3.2.0.47.4 `bool flexcan_config_t::enableLoopBack`

17.2.3.2.0.47.5 `bool flexcan_config_t::enableSelfWakeup`

17.2.3.2.0.47.6 `bool flexcan_config_t::enableIndividMask`

#### 17.2.3.3 `struct flexcan_timing_config_t`

##### Data Fields

- `uint8_t` [preDivider](#)  
*Clock Pre-scaler Division Factor.*
- `uint8_t` [rJumpwidth](#)  
*Re-sync Jump Width.*
- `uint8_t` [phaseSeg1](#)  
*Phase Segment 1.*
- `uint8_t` [phaseSeg2](#)  
*Phase Segment 2.*
- `uint8_t` [propSeg](#)  
*Propagation Segment.*

### 17.2.3.3.0.48 Field Documentation

17.2.3.3.0.48.1 `uint8_t flexcan_timing_config_t::preDivider`

17.2.3.3.0.48.2 `uint8_t flexcan_timing_config_t::rJumpwidth`

17.2.3.3.0.48.3 `uint8_t flexcan_timing_config_t::phaseSeg1`

17.2.3.3.0.48.4 `uint8_t flexcan_timing_config_t::phaseSeg2`

17.2.3.3.0.48.5 `uint8_t flexcan_timing_config_t::propSeg`

### 17.2.3.4 `struct flexcan_rx_mb_config_t`

This structure is used as the parameter of `FLEXCAN_SetRxMbConfig()` function. The `FLEXCAN_SetRxMbConfig()` function is used to configure FlexCAN Receive Message Buffer. The function abort previous receiving process, clean the Message Buffer and activate the Rx Message Buffer using given Message Buffer setting.

#### Data Fields

- `uint32_t id`  
*CAN Message Buffer Frame Identifier, should be set using `FLEXCAN_ID_EXT()` or `FLEXCAN_ID_STD()` macro.*
- `flexcan_frame_format_t format`  
*CAN Frame Identifier format(Standard of Extend).*
- `flexcan_frame_type_t type`  
*CAN Frame Type(Data or Remote).*

### 17.2.3.4.0.49 Field Documentation

17.2.3.4.0.49.1 `uint32_t flexcan_rx_mb_config_t::id`

17.2.3.4.0.49.2 `flexcan_frame_format_t flexcan_rx_mb_config_t::format`

17.2.3.4.0.49.3 `flexcan_frame_type_t flexcan_rx_mb_config_t::type`

### 17.2.3.5 `struct flexcan_rx_fifo_config_t`

#### Data Fields

- `uint32_t * idFilterTable`  
*Pointer to the FlexCAN Rx FIFO identifier filter table.*
- `uint8_t idFilterNum`  
*The quantity of filter elements.*
- `flexcan_rx_fifo_filter_type_t idFilterType`  
*The FlexCAN Rx FIFO Filter type.*
- `flexcan_rx_fifo_priority_t priority`  
*The FlexCAN Rx FIFO receive priority.*

**17.2.3.5.0.50 Field Documentation****17.2.3.5.0.50.1** `uint32_t flexcan_rx_fifo_config_t::idFilterTable`**17.2.3.5.0.50.2** `uint8_t flexcan_rx_fifo_config_t::idFilterNum`**17.2.3.5.0.50.3** `flexcan_rx_fifo_filter_type_t flexcan_rx_fifo_config_t::idFilterType`**17.2.3.5.0.50.4** `flexcan_rx_fifo_priority_t flexcan_rx_fifo_config_t::priority`**17.2.3.6 struct flexcan\_mb\_transfer\_t****Data Fields**

- `flexcan_frame_t * frame`  
*The buffer of CAN Message to be transfer.*
- `uint8_t mbIdx`  
*The index of Message buffer used to transfer Message.*

**17.2.3.6.0.51 Field Documentation****17.2.3.6.0.51.1** `flexcan_frame_t * flexcan_mb_transfer_t::frame`**17.2.3.6.0.51.2** `uint8_t flexcan_mb_transfer_t::mbIdx`**17.2.3.7 struct flexcan\_fifo\_transfer\_t****Data Fields**

- `flexcan_frame_t * frame`  
*The buffer of CAN Message to be received from Rx FIFO.*

**17.2.3.7.0.52 Field Documentation****17.2.3.7.0.52.1** `flexcan_frame_t * flexcan_fifo_transfer_t::frame`**17.2.3.8 struct \_flexcan\_handle**

FlexCAN handle structure definition.

**Data Fields**

- `flexcan_transfer_callback_t callback`  
*Callback function.*
- `void * userData`  
*FlexCAN callback function parameter.*
- `flexcan_frame_t *volatile mbFrameBuf [CAN_WORD1_COUNT]`  
*The buffer for received data from Message Buffers.*
- `flexcan_frame_t *volatile rxFifoFrameBuf`  
*The buffer for received data from Rx FIFO.*

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- volatile uint8\_t **mbState** [CAN\_WORD1\_COUNT]  
*Message Buffer transfer state.*
- volatile uint8\_t **rxFifoState**  
*Rx FIFO transfer state.*

### 17.2.3.8.0.53 Field Documentation

17.2.3.8.0.53.1 flexcan\_transfer\_callback\_t flexcan\_handle\_t::callback

17.2.3.8.0.53.2 void\* flexcan\_handle\_t::userData

17.2.3.8.0.53.3 flexcan\_frame\_t\* volatile flexcan\_handle\_t::mbFrameBuf[CAN\_WORD1\_COUNT]

17.2.3.8.0.53.4 flexcan\_frame\_t\* volatile flexcan\_handle\_t::rxFifoFrameBuf

17.2.3.8.0.53.5 volatile uint8\_t flexcan\_handle\_t::mbState[CAN\_WORD1\_COUNT]

17.2.3.8.0.53.6 volatile uint8\_t flexcan\_handle\_t::rxFifoState

### 17.2.4 Macro Definition Documentation

17.2.4.1 #define FLEXCAN\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 0))

17.2.4.2 #define FLEXCAN\_ID\_STD( *id* ) (((uint32\_t)((uint32\_t)(id)) << CAN\_ID\_STD\_SHIFT)) & CAN\_ID\_STD\_MASK)

Standard Frame ID helper macro.

17.2.4.3 #define FLEXCAN\_ID\_EXT( *id* )

Value:

```
((uint32_t)((uint32_t)(id)) << CAN_ID_EXT_SHIFT)) & \
(CAN_ID_EXT_MASK | CAN_ID_STD_MASK)
```

17.2.4.4 #define FLEXCAN\_RX\_MB\_STD\_MASK( *id*, *rtr*, *ide* )

Value:

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
FLEXCAN_ID_STD(id)
```

Standard Rx Message Buffer Mask helper macro.



**17.2.4.5 #define FLEXCAN\_RX\_MB\_EXT\_MASK( *id*, *rtr*, *ide* )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
    FLEXCAN_ID_EXT(id))
```

**17.2.4.6 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A( *id*, *rtr*, *ide* )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
    (FLEXCAN_ID_STD(id) << 1))
```

Standard Rx FIFO Mask helper macro Type A helper macro.

**17.2.4.7 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_HIGH( *id*, *rtr*, *ide* )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
    (FLEXCAN_ID_STD(id) << 16))
```

**17.2.4.8 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_LOW( *id*, *rtr*, *ide* )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 15) | (uint32_t)((uint32_t)(ide) << 14)) | \
    FLEXCAN_ID_STD(id))
```

**17.2.4.9 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_HIGH( *id*  
) ((FLEXCAN\_ID\_STD(id) & 0x7F8) << 21)****17.2.4.10 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_HIGH( *id*  
) ((FLEXCAN\_ID\_STD(id) & 0x7F8) << 13)**

\

**17.2.4.11** `#define FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_LOW( id ) ((FLEXCAN_ID_STD(id) & 0x7F8) << 5)`

**17.2.4.12** `#define FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_LOW( id ) ((FLEXCAN_ID_STD(id) & 0x7F8) >> 3)`

**17.2.4.13** `#define FLEXCAN_RX_FIFO_EXT_MASK_TYPE_A( id, rtr, ide )`

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
(FLEXCAN_ID_EXT(id) << 1)
```

**17.2.4.14** `#define FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_HIGH( id, rtr, ide )`

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
(FLEXCAN_ID_EXT(id) & 0x1FFF8000) << 1)
```

**17.2.4.15** `#define FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_LOW( id, rtr, ide )`

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 15) | (uint32_t)((uint32_t)(ide) << 14)) | \
((FLEXCAN_ID_EXT(id) & 0x1FFF8000) >> 15) \
```

**17.2.4.16** `#define FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_HIGH( id ) ((FLEXCAN_ID_EXT(id) & 0x1FE00000) << 3)`

**17.2.4.17** `#define FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_HIGH( id )`

**Value:**

```
((FLEXCAN_ID_EXT(id) & 0x1FE00000) >> 5) \
```

**17.2.4.18** `#define FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_LOW( id )`

**Value:**

```
((FLEXCAN_ID_EXT(id) & 0x1FE00000) >> 13) \
```

**17.2.4.19** `#define FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_LOW( id  
) ((FLEXCAN_ID_EXT(id) & 0x1FE00000) >> 21)`

**17.2.4.20** `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_A( id, rtr, ide  
) FLEXCAN_RX_FIFO_STD_MASK_TYPE_A(id, rtr, ide)`

Standard Rx FIFO Filter helper macro Type A helper macro.

**17.2.4.21** `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_B_HIGH( id, rtr, ide )`

**Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_HIGH(
    id, rtr, ide) \
```

**17.2.4.22** `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_B_LOW( id, rtr, ide )`

**Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_LOW(
    id, rtr, ide) \
```

**17.2.4.23** `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_HIGH( id )`

**Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_HIGH(
    id) \
```

**17.2.4.24** `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_MID_HIGH( id )`

**Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_HIGH(
    id) \
```

**17.2.4.25** `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_MID_LOW( id )`

**Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_LOW(
    id) \
```

**17.2.4.26** `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_LOW( id  
 ) FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_LOW(id)`

\

**17.2.4.27** `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_A( id, rtr, ide  
 ) FLEXCAN_RX_FIFO_EXT_MASK_TYPE_A(id, rtr, ide)`

**17.2.4.28** `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_B_HIGH( id, rtr, ide )`

**Value:**

`FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_HIGH( id, rtr, ide)` \

**17.2.4.29** `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_B_LOW( id, rtr, ide )`

**Value:**

`FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_LOW( id, rtr, ide)` \

**17.2.4.30** `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_HIGH( id  
 ) FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_HIGH(id)`

\

**17.2.4.31** `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_MID_HIGH( id )`

**Value:**

`FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_HIGH( id)` \

**17.2.4.32** `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_MID_LOW( id )`

**Value:**

`FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_LOW( id)` \

```
17.2.4.33 #define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_LOW( id
           ) FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_LOW(id)
```

## 17.2.5 Typedef Documentation

```
17.2.5.1 typedef void(* flexcan_transfer_callback_t)(CAN_Type *base, flexcan_handle_t
           *handle, status_t status, uint32_t result, void *userData)
```

The FlexCAN transfer callback returns a value from the underlying layer. If the status equals to `kStatus_FLEXCAN_ErrorStatus`, the result parameter is the Content of FlexCAN status register which can be used to get the working status(or error status) of FlexCAN module. If the status equals to other FlexCAN Message Buffer transfer status, the result is the index of Message Buffer that generate transfer event. If the status equals to other FlexCAN Message Buffer transfer status, the result is meaningless and should be Ignored.

## 17.2.6 Enumeration Type Documentation

### 17.2.6.1 enum \_flexcan\_status

Enumerator

*kStatus\_FLEXCAN\_TxBusy* Tx Message Buffer is Busy.  
*kStatus\_FLEXCAN\_TxIdle* Tx Message Buffer is Idle.  
*kStatus\_FLEXCAN\_TxSwitchToRx* Remote Message is send out and Message buffer changed to Receive one.  
*kStatus\_FLEXCAN\_RxBusy* Rx Message Buffer is Busy.  
*kStatus\_FLEXCAN\_RxIdle* Rx Message Buffer is Idle.  
*kStatus\_FLEXCAN\_RxOverflow* Rx Message Buffer is Overflowed.  
*kStatus\_FLEXCAN\_RxFifoBusy* Rx Message FIFO is Busy.  
*kStatus\_FLEXCAN\_RxFifoIdle* Rx Message FIFO is Idle.  
*kStatus\_FLEXCAN\_RxFifoOverflow* Rx Message FIFO is overflowed.  
*kStatus\_FLEXCAN\_RxFifoWarning* Rx Message FIFO is almost overflowed.  
*kStatus\_FLEXCAN\_ErrorStatus* FlexCAN Module Error and Status.  
*kStatus\_FLEXCAN\_UnHandled* UnHadled Interrupt asserted.

### 17.2.6.2 enum flexcan\_frame\_format\_t

Enumerator

*kFLEXCAN\_FrameFormatStandard* Standard frame format attribute.  
*kFLEXCAN\_FrameFormatExtend* Extend frame format attribute.

### 17.2.6.3 enum flexcan\_frame\_type\_t

Enumerator

*kFLEXCAN\_FrameTypeData* Data frame type attribute.

*kFLEXCAN\_FrameTypeRemote* Remote frame type attribute.

### 17.2.6.4 enum flexcan\_clock\_source\_t

Enumerator

*kFLEXCAN\_ClkSrcOsc* FlexCAN Protocol Engine clock from Oscillator.

*kFLEXCAN\_ClkSrcPeri* FlexCAN Protocol Engine clock from Peripheral Clock.

### 17.2.6.5 enum flexcan\_rx\_fifo\_filter\_type\_t

Enumerator

*kFLEXCAN\_RxFifoFilterTypeA* One full ID (standard and extended) per ID Filter element.

*kFLEXCAN\_RxFifoFilterTypeB* Two full standard IDs or two partial 14-bit ID slices per ID Filter Table element.

*kFLEXCAN\_RxFifoFilterTypeC* Four partial 8-bit Standard or extended ID slices per ID Filter Table element.

*kFLEXCAN\_RxFifoFilterTypeD* All frames rejected.

### 17.2.6.6 enum flexcan\_rx\_fifo\_priority\_t

The matching process starts from the Rx MB(or Rx FIFO) with higher priority. If no MB(or Rx FIFO filter) is satisfied, the matching process goes on with the Rx FIFO(or Rx MB) with lower priority.

Enumerator

*kFLEXCAN\_RxFifoPrioLow* Matching process start from Rx Message Buffer first.

*kFLEXCAN\_RxFifoPrioHigh* Matching process start from Rx FIFO first.

### 17.2.6.7 enum \_flexcan\_interrupt\_enable

This structure contains the settings for all of the FlexCAN Module interrupt configurations. Note: FlexCAN Message Buffers and Rx FIFO have their own interrupts.

Enumerator

*kFLEXCAN\_BusOffInterruptEnable* Bus Off interrupt.

***kFLEXCAN\_ErrorInterruptEnable*** Error interrupt.  
***kFLEXCAN\_RxWarningInterruptEnable*** Rx Warning interrupt.  
***kFLEXCAN\_TxWarningInterruptEnable*** Tx Warning interrupt.  
***kFLEXCAN\_WakeUpInterruptEnable*** Wake Up interrupt.

#### 17.2.6.8 enum \_flexcan\_flags

This provides constants for the FlexCAN status flags for use in the FlexCAN functions. Note: The CPU read action clears FLEXCAN\_ErrorFlag, therefore user need to read FLEXCAN\_ErrorFlag and distinguish which error is occur using [\\_flexcan\\_error\\_flags](#) enumerations.

Enumerator

***kFLEXCAN\_SynchFlag*** CAN Synchronization Status.  
***kFLEXCAN\_TxWarningIntFlag*** Tx Warning Interrupt Flag.  
***kFLEXCAN\_RxWarningIntFlag*** Rx Warning Interrupt Flag.  
***kFLEXCAN\_TxErrorWarningFlag*** Tx Error Warning Status.  
***kFLEXCAN\_RxErrorWarningFlag*** Rx Error Warning Status.  
***kFLEXCAN\_IdleFlag*** CAN IDLE Status Flag.  
***kFLEXCAN\_FaultConfinementFlag*** Fault Confinement State Flag.  
***kFLEXCAN\_TransmittingFlag*** FlexCAN In Transmission Status.  
***kFLEXCAN\_ReceivingFlag*** FlexCAN In Reception Status.  
***kFLEXCAN\_BusOffIntFlag*** Bus Off Interrupt Flag.  
***kFLEXCAN\_ErrorIntFlag*** Error Interrupt Flag.  
***kFLEXCAN\_WakeUpIntFlag*** Wake-Up Interrupt Flag.  
***kFLEXCAN\_ErrorFlag*** All FlexCAN Error Status.

#### 17.2.6.9 enum \_flexcan\_error\_flags

The FlexCAN Error Status enumerations is used to report current error of the FlexCAN bus. This enumerations should be used with KFLEXCAN\_ErrorFlag in [\\_flexcan\\_flags](#) enumerations to determine which error is generated.

Enumerator

***kFLEXCAN\_StuffingError*** Stuffing Error.  
***kFLEXCAN\_FormError*** Form Error.  
***kFLEXCAN\_CrcError*** Cyclic Redundancy Check Error.  
***kFLEXCAN\_AckError*** Received no ACK on transmission.  
***kFLEXCAN\_Bit0Error*** Unable to send dominant bit.  
***kFLEXCAN\_Bit1Error*** Unable to send recessive bit.

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### 17.2.6.10 enum \_flexcan\_rx\_fifo\_flags

The FlexCAN Rx FIFO Status enumerations are used to determine the status of the Rx FIFO. Because Rx FIFO occupy the MB0 ~ MB7 (Rx Fifo filter also occupies more Message Buffer space), Rx FIFO status flags are mapped to the corresponding Message Buffer status flags.

Enumerator

***kFLEXCAN\_RxFifoOverflowFlag*** Rx FIFO overflow flag.  
***kFLEXCAN\_RxFifoWarningFlag*** Rx FIFO almost full flag.  
***kFLEXCAN\_RxFifoFrameAvlFlag*** Frames available in Rx FIFO flag.

## 17.2.7 Function Documentation

### 17.2.7.1 void FLEXCAN\_Init ( CAN\_Type \* *base*, const flexcan\_config\_t \* *config*, uint32\_t *sourceClock\_Hz* )

This function initializes the FlexCAN module with user-defined settings. This example shows how to set up the [flexcan\\_config\\_t](#) parameters and how to call the FLEXCAN\_Init function by passing in these parameters.

```
* flexcan_config_t flexcanConfig;  
* flexcanConfig.clkSrc = kFLEXCAN_ClkSrcOsc;  
* flexcanConfig.baudRate = 125000U;  
* flexcanConfig.maxMbNum = 16;  
* flexcanConfig.enableLoopBack = false;  
* flexcanConfig.enableSelfWakeup = false;  
* flexcanConfig.enableIndividMask = false;  
* flexcanConfig.enableDoze = false;  
* FLEXCAN_Init(CAN0, &flexcanConfig, 8000000UL);  
*
```

Parameters

|                       |                                                       |
|-----------------------|-------------------------------------------------------|
| <i>base</i>           | FlexCAN peripheral base address.                      |
| <i>config</i>         | Pointer to the user-defined configuration structure.  |
| <i>sourceClock_Hz</i> | FlexCAN Protocol Engine clock source frequency in Hz. |

### 17.2.7.2 void FLEXCAN\_Deinit ( CAN\_Type \* *base* )

This function disables the FlexCAN module clock and sets all register values to the reset value.



## Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

**17.2.7.3 void FLEXCAN\_GetDefaultConfig ( flexcan\_config\_t \* *config* )**

This function initializes the FlexCAN configuration structure to default values. The default values are as follows. flexcanConfig->clkSrc = KFLEXCAN\_ClkSrcOsc; flexcanConfig->baudRate = 125000U; flexcanConfig->maxMbNum = 16; flexcanConfig->enableLoopBack = false; flexcanConfig->enableSelfWakeup = false; flexcanConfig->enableIndividMask = false; flexcanConfig->enableDoze = false;

## Parameters

|               |                                                 |
|---------------|-------------------------------------------------|
| <i>config</i> | Pointer to the FlexCAN configuration structure. |
|---------------|-------------------------------------------------|

**17.2.7.4 void FLEXCAN\_SetTimingConfig ( CAN\_Type \* *base*, const flexcan\_timing\_config\_t \* *config* )**

This function gives user settings to CAN bus timing characteristic. The function is for an experienced user. For less experienced users, call the [FLEXCAN\\_Init\(\)](#) and fill the baud rate field with a desired value. This provides the default timing characteristics to the module.

Note that calling [FLEXCAN\\_SetTimingConfig\(\)](#) overrides the baud rate set in [FLEXCAN\\_Init\(\)](#).

## Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.               |
| <i>config</i> | Pointer to the timing configuration structure. |

**17.2.7.5 void FLEXCAN\_SetRxMbGlobalMask ( CAN\_Type \* *base*, uint32\_t *mask* )**

This function sets the global mask for the FlexCAN message buffer in a matching process. The configuration is only effective when the Rx individual mask is disabled in the [FLEXCAN\\_Init\(\)](#).

## Parameters

|             |                                      |
|-------------|--------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.     |
| <i>mask</i> | Rx Message Buffer Global Mask value. |

**17.2.7.6 void FLEXCAN\_SetRxFifoGlobalMask ( CAN\_Type \* *base*, uint32\_t *mask* )**

This function sets the global mask for FlexCAN FIFO in a matching process.

## Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
| <i>mask</i> | Rx Fifo Global Mask value.       |

### 17.2.7.7 void FLEXCAN\_SetRxIndividualMask ( CAN\_Type \* *base*, uint8\_t *maskIdx*, uint32\_t *mask* )

This function sets the individual mask for the FlexCAN matching process. The configuration is only effective when the Rx individual mask is enabled in the [FLEXCAN\\_Init\(\)](#). If the Rx FIFO is disabled, the individual mask is applied to the corresponding Message Buffer. If the Rx FIFO is enabled, the individual mask for Rx FIFO occupied Message Buffer is applied to the Rx Filter with the same index. Note that only the first 32 individual masks can be used as the Rx FIFO filter mask.

## Parameters

|                |                                  |
|----------------|----------------------------------|
| <i>base</i>    | FlexCAN peripheral base address. |
| <i>maskIdx</i> | The Index of individual Mask.    |
| <i>mask</i>    | Rx Individual Mask value.        |

### 17.2.7.8 void FLEXCAN\_SetTxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, bool *enable* )

This function aborts the previous transmission, cleans the Message Buffer, and configures it as a Transmit Message Buffer.

## Parameters

|               |                                                                                                                                                                    |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                                                                                                   |
| <i>mbIdx</i>  | The Message Buffer index.                                                                                                                                          |
| <i>enable</i> | Enable/disable Tx Message Buffer. <ul style="list-style-type: none"> <li>• true: Enable Tx Message Buffer.</li> <li>• false: Disable Tx Message Buffer.</li> </ul> |

### 17.2.7.9 void FLEXCAN\_SetRxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_rx\_mb\_config\_t \* *config*, bool *enable* )

This function cleans a FlexCAN build-in Message Buffer and configures it as a Receive Message Buffer.

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### Parameters

|               |                                                                                                                                                                 |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                                                                                                |
| <i>mbIdx</i>  | The Message Buffer index.                                                                                                                                       |
| <i>config</i> | Pointer to the FlexCAN Message Buffer configuration structure.                                                                                                  |
| <i>enable</i> | Enable/disable Rx Message Buffer. <ul style="list-style-type: none"><li>• true: Enable Rx Message Buffer.</li><li>• false: Disable Rx Message Buffer.</li></ul> |

#### 17.2.7.10 void FLEXCAN\_SetRxFifoConfig ( CAN\_Type \* *base*, const flexcan\_rx\_fifo\_config\_t \* *config*, bool *enable* )

This function configures the Rx FIFO with given Rx FIFO configuration.

### Parameters

|               |                                                                                                                                   |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                                                                  |
| <i>config</i> | Pointer to the FlexCAN Rx FIFO configuration structure.                                                                           |
| <i>enable</i> | Enable/disable Rx FIFO. <ul style="list-style-type: none"><li>• true: Enable Rx FIFO.</li><li>• false: Disable Rx FIFO.</li></ul> |

#### 17.2.7.11 static uint32\_t FLEXCAN\_GetStatusFlags ( CAN\_Type \* *base* ) [inline], [static]

This function gets all FlexCAN status flags. The flags are returned as the logical OR value of the enumerators [\\_flexcan\\_flags](#). To check the specific status, compare the return value with enumerators in [\\_flexcan\\_flags](#).

### Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

### Returns

FlexCAN status flags which are ORed by the enumerators in the [\\_flexcan\\_flags](#).

**17.2.7.12** `static void FLEXCAN_ClearStatusFlags ( CAN_Type * base, uint32_t mask )`  
`[inline], [static]`

This function clears the FlexCAN status flags with a provided mask. An automatically cleared flag can't be cleared by this function.

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### Parameters

|             |                                                                                            |
|-------------|--------------------------------------------------------------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.                                                           |
| <i>mask</i> | The status flags to be cleared, it is logical OR value of <a href="#">_flexcan_flags</a> . |

**17.2.7.13** `static void FLEXCAN_GetBusErrCount ( CAN_Type * base, uint8_t * txErrBuf,  
uint8_t * rxErrBuf ) [inline], [static]`

This function gets the FlexCAN Bus Error Counter value for both Tx and Rx direction. These values may be needed in the upper layer error handling.

### Parameters

|                 |                                         |
|-----------------|-----------------------------------------|
| <i>base</i>     | FlexCAN peripheral base address.        |
| <i>txErrBuf</i> | Buffer to store Tx Error Counter value. |
| <i>rxErrBuf</i> | Buffer to store Rx Error Counter value. |

**17.2.7.14** `static uint32_t FLEXCAN_GetMbStatusFlags ( CAN_Type * base, uint32_t mask  
) [inline], [static]`

This function gets the interrupt flags of a given Message Buffers.

### Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

### Returns

The status of given Message Buffers.

**17.2.7.15** `static void FLEXCAN_ClearMbStatusFlags ( CAN_Type * base, uint32_t mask )  
[inline], [static]`

This function clears the interrupt flags of a given Message Buffers.

## Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

#### 17.2.7.16 static void FLEXCAN\_EnableInterrupts ( CAN\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the FlexCAN interrupts according to the provided mask. The mask is a logical OR of enumeration members, see [\\_flexcan\\_interrupt\\_enable](#).

## Parameters

|             |                                                                                     |
|-------------|-------------------------------------------------------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.                                                    |
| <i>mask</i> | The interrupts to enable. Logical OR of <a href="#">_flexcan_interrupt_enable</a> . |

#### 17.2.7.17 static void FLEXCAN\_DisableInterrupts ( CAN\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function disables the FlexCAN interrupts according to the provided mask. The mask is a logical OR of enumeration members, see [\\_flexcan\\_interrupt\\_enable](#).

## Parameters

|             |                                                                                      |
|-------------|--------------------------------------------------------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.                                                     |
| <i>mask</i> | The interrupts to disable. Logical OR of <a href="#">_flexcan_interrupt_enable</a> . |

#### 17.2.7.18 static void FLEXCAN\_EnableMblInterrupts ( CAN\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the interrupts of given Message Buffers.

## Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

**17.2.7.19**   `static void FLEXCAN_DisableMbInterrupts ( CAN_Type * base, uint32_t mask )`  
                  `[inline], [static]`

This function disables the interrupts of given Message Buffers.



## Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

### 17.2.7.20 static void FLEXCAN\_Enable ( CAN\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the FlexCAN module.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexCAN base pointer.             |
| <i>enable</i> | true to enable, false to disable. |

### 17.2.7.21 status\_t FLEXCAN\_WriteTxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_frame\_t \* *txFrame* )

This function writes a CAN Message to the specified Transmit Message Buffer and changes the Message Buffer state to start CAN Message transmit. After that the function returns immediately.

## Parameters

|                |                                          |
|----------------|------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base address.         |
| <i>mbIdx</i>   | The FlexCAN Message Buffer index.        |
| <i>txFrame</i> | Pointer to CAN message frame to be sent. |

## Return values

|                        |                                          |
|------------------------|------------------------------------------|
| <i>kStatus_Success</i> | - Write Tx Message Buffer Successfully.  |
| <i>kStatus_Fail</i>    | - Tx Message Buffer is currently in use. |

### 17.2.7.22 status\_t FLEXCAN\_ReadRxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *rxFrame* )

This function reads a CAN message from a specified Receive Message Buffer. The function fills a receive CAN message frame structure with just received data and activates the Message Buffer again. The function returns immediately.

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### Parameters

|                |                                                       |
|----------------|-------------------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base address.                      |
| <i>mbIdx</i>   | The FlexCAN Message Buffer index.                     |
| <i>rxFrame</i> | Pointer to CAN message frame structure for reception. |

### Return values

|                                    |                                                                           |
|------------------------------------|---------------------------------------------------------------------------|
| <i>kStatus_Success</i>             | - Rx Message Buffer is full and has been read successfully.               |
| <i>kStatus_FLEXCAN_Rx-Overflow</i> | - Rx Message Buffer is already overflowed and has been read successfully. |
| <i>kStatus_Fail</i>                | - Rx Message Buffer is empty.                                             |

#### 17.2.7.23 **status\_t FLEXCAN\_ReadRxFifo ( CAN\_Type \* *base*, flexcan\_frame\_t \* *rxFrame* )**

This function reads a CAN message from the FlexCAN build-in Rx FIFO.

### Parameters

|                |                                                       |
|----------------|-------------------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base address.                      |
| <i>rxFrame</i> | Pointer to CAN message frame structure for reception. |

### Return values

|                        |                                           |
|------------------------|-------------------------------------------|
| <i>kStatus_Success</i> | - Read Message from Rx FIFO successfully. |
| <i>kStatus_Fail</i>    | - Rx FIFO is not enabled.                 |

#### 17.2.7.24 **status\_t FLEXCAN\_TransferSendBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *txFrame* )**

Note that a transfer handle does not need to be created before calling this API.

### Parameters

|                |                                          |
|----------------|------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base pointer.         |
| <i>mbIdx</i>   | The FlexCAN Message Buffer index.        |
| <i>txFrame</i> | Pointer to CAN message frame to be sent. |

Return values

|                        |                                          |
|------------------------|------------------------------------------|
| <i>kStatus_Success</i> | - Write Tx Message Buffer Successfully.  |
| <i>kStatus_Fail</i>    | - Tx Message Buffer is currently in use. |

#### 17.2.7.25 **status\_t FLEXCAN\_TransferReceiveBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *rxFrame* )**

Note that a transfer handle does not need to be created before calling this API.

Parameters

|                |                                                       |
|----------------|-------------------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base pointer.                      |
| <i>mbIdx</i>   | The FlexCAN Message Buffer index.                     |
| <i>rxFrame</i> | Pointer to CAN message frame structure for reception. |

Return values

|                                    |                                                                           |
|------------------------------------|---------------------------------------------------------------------------|
| <i>kStatus_Success</i>             | - Rx Message Buffer is full and has been read successfully.               |
| <i>kStatus_FLEXCAN_Rx-Overflow</i> | - Rx Message Buffer is already overflowed and has been read successfully. |
| <i>kStatus_Fail</i>                | - Rx Message Buffer is empty.                                             |

#### 17.2.7.26 **status\_t FLEXCAN\_TransferReceiveFifoBlocking ( CAN\_Type \* *base*, flexcan\_frame\_t \* *rxFrame* )**

Note that a transfer handle does not need to be created before calling this API.

Parameters

|                |                                                       |
|----------------|-------------------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base pointer.                      |
| <i>rxFrame</i> | Pointer to CAN message frame structure for reception. |

Return values

|                        |                                           |
|------------------------|-------------------------------------------|
| <i>kStatus_Success</i> | - Read Message from Rx FIFO successfully. |
| <i>kStatus_Fail</i>    | - Rx FIFO is not enabled.                 |

**17.2.7.27** void FLEXCAN\_TransferCreateHandle ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the FlexCAN handle, which can be used for other FlexCAN transactional APIs. Usually, for a specified FlexCAN instance, call this API once to get the initialized handle.

## Parameters

|                 |                                         |
|-----------------|-----------------------------------------|
| <i>base</i>     | FlexCAN peripheral base address.        |
| <i>handle</i>   | FlexCAN handle pointer.                 |
| <i>callback</i> | The callback function.                  |
| <i>userData</i> | The parameter of the callback function. |

#### 17.2.7.28 **status\_t FLEXCAN\_TransferSendNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *xfer* )**

This function sends a message using IRQ. This is a non-blocking function, which returns right away. When messages have been sent out, the send callback function is called.

## Parameters

|               |                                                                                            |
|---------------|--------------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                           |
| <i>handle</i> | FlexCAN handle pointer.                                                                    |
| <i>xfer</i>   | FlexCAN Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> . |

## Return values

|                                |                                                       |
|--------------------------------|-------------------------------------------------------|
| <i>kStatus_Success</i>         | Start Tx Message Buffer sending process successfully. |
| <i>kStatus_Fail</i>            | Write Tx Message Buffer failed.                       |
| <i>kStatus_FLEXCAN_Tx-Busy</i> | Tx Message Buffer is in use.                          |

#### 17.2.7.29 **status\_t FLEXCAN\_TransferReceiveNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *xfer* )**

This function receives a message using IRQ. This is non-blocking function, which returns right away. When the message has been received, the receive callback function is called.

## Parameters

|               |                                                                                            |
|---------------|--------------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                           |
| <i>handle</i> | FlexCAN handle pointer.                                                                    |
| <i>xfer</i>   | FlexCAN Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> . |

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### Return values

|                                |                                                           |
|--------------------------------|-----------------------------------------------------------|
| <i>kStatus_Success</i>         | - Start Rx Message Buffer receiving process successfully. |
| <i>kStatus_FLEXCAN_Rx-Busy</i> | - Rx Message Buffer is in use.                            |

### 17.2.7.30 **status\_t FLEXCAN\_TransferReceiveFifoNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_fifo\_transfer\_t \* *xfer* )**

This function receives a message using IRQ. This is a non-blocking function, which returns right away. When all messages have been received, the receive callback function is called.

### Parameters

|               |                                                                                       |
|---------------|---------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                      |
| <i>handle</i> | FlexCAN handle pointer.                                                               |
| <i>xfer</i>   | FlexCAN Rx FIFO transfer structure. See the <a href="#">flexcan_fifo_transfer_t</a> . |

### Return values

|                                    |                                                 |
|------------------------------------|-------------------------------------------------|
| <i>kStatus_Success</i>             | - Start Rx FIFO receiving process successfully. |
| <i>kStatus_FLEXCAN_Rx-FifoBusy</i> | - Rx FIFO is currently in use.                  |

### 17.2.7.31 **void FLEXCAN\_TransferAbortSend ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )**

This function aborts the interrupt driven message send process.

### Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.  |
| <i>handle</i> | FlexCAN handle pointer.           |
| <i>mbIdx</i>  | The FlexCAN Message Buffer index. |

### 17.2.7.32 **void FLEXCAN\_TransferAbortReceive ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )**

This function aborts the interrupt driven message receive process.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.  |
| <i>handle</i> | FlexCAN handle pointer.           |
| <i>mbIdx</i>  | The FlexCAN Message Buffer index. |

### 17.2.7.33 void FLEXCAN\_TransferAbortReceiveFifo ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle* )

This function aborts the interrupt driven message receive from Rx FIFO process.

## Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address. |
| <i>handle</i> | FlexCAN handle pointer.          |

### 17.2.7.34 void FLEXCAN\_TransferHandleIRQ ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle* )

This function handles the FlexCAN Error, the Message Buffer, and the Rx FIFO IRQ request.

## Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address. |
| <i>handle</i> | FlexCAN handle pointer.          |

### 17.3 FlexCAN eDMA Driver

#### 17.3.1 Overview

##### Data Structures

- struct [flexcan\\_edma\\_handle\\_t](#)  
*FlexCAN eDMA handle. [More...](#)*

##### Typedefs

- typedef void(\* [flexcan\\_edma\\_transfer\\_callback\\_t](#) )(CAN\_Type \*base, flexcan\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*FlexCAN transfer callback function.*

##### eDMA transactional

- void [FLEXCAN\\_TransferCreateHandleEDMA](#) (CAN\_Type \*base, flexcan\_edma\_handle\_t \*handle, [flexcan\\_edma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*rxFifoEdmaHandle)  
*Initializes the FlexCAN handle, which is used in transactional functions.*
- status\_t [FLEXCAN\\_TransferReceiveFifoEDMA](#) (CAN\_Type \*base, flexcan\_edma\_handle\_t \*handle, [flexcan\\_fifo\\_transfer\\_t](#) \*xfer)  
*Receives the CAN Message from the Rx FIFO using eDMA.*
- void [FLEXCAN\\_TransferAbortReceiveFifoEDMA](#) (CAN\_Type \*base, flexcan\_edma\_handle\_t \*handle)  
*Aborts the receive process which used eDMA.*

#### 17.3.2 Data Structure Documentation

##### 17.3.2.1 struct \_flexcan\_edma\_handle

##### Data Fields

- [flexcan\\_edma\\_transfer\\_callback\\_t](#) callback  
*Callback function.*
- void \* [userData](#)  
*FlexCAN callback function parameter.*
- [edma\\_handle\\_t](#) \* [rxFifoEdmaHandle](#)  
*The EDMA Rx FIFO channel used.*
- volatile uint8\_t [rxFifoState](#)  
*Rx FIFO transfer state.*



#### 17.3.2.1.0.54 Field Documentation

17.3.2.1.0.54.1 `flexcan_edma_transfer_callback_t flexcan_edma_handle_t::callback`

17.3.2.1.0.54.2 `void* flexcan_edma_handle_t::userData`

17.3.2.1.0.54.3 `edma_handle_t* flexcan_edma_handle_t::rxFifoEdmaHandle`

17.3.2.1.0.54.4 `volatile uint8_t flexcan_edma_handle_t::rxFifoState`

#### 17.3.3 Typedef Documentation

17.3.3.1 `typedef void(* flexcan_edma_transfer_callback_t)(CAN_Type *base,  
flexcan_edma_handle_t *handle, status_t status, void *userData)`

#### 17.3.4 Function Documentation

17.3.4.1 `void FLEXCAN_TransferCreateHandleEDMA ( CAN_Type * base,  
flexcan_edma_handle_t * handle, flexcan_edma_transfer_callback_t callback,  
void * userData, edma_handle_t * rxFifoEdmaHandle )`

## FlexCAN eDMA Driver

### Parameters

|                          |                                                     |
|--------------------------|-----------------------------------------------------|
| <i>base</i>              | FlexCAN peripheral base address.                    |
| <i>handle</i>            | Pointer to flexcan_edma_handle_t structure.         |
| <i>callback</i>          | The callback function.                              |
| <i>userData</i>          | The parameter of the callback function.             |
| <i>rxFifoEdma-Handle</i> | User-requested DMA handle for Rx FIFO DMA transfer. |

### 17.3.4.2 status\_t FLEXCAN\_TransferReceiveFifoEDMA ( CAN\_Type \* *base*, flexcan\_edma\_handle\_t \* *handle*, flexcan\_fifo\_transfer\_t \* *xfer* )

This function receives the CAN Message using eDMA. This is a non-blocking function, which returns right away. After the CAN Message is received, the receive callback function is called.

### Parameters

|               |                                                                                        |
|---------------|----------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                       |
| <i>handle</i> | Pointer to flexcan_edma_handle_t structure.                                            |
| <i>xfer</i>   | FlexCAN Rx FIFO EDMA transfer structure, see <a href="#">flexcan_fifo_transfer_t</a> . |

### Return values

|                                    |                            |
|------------------------------------|----------------------------|
| <i>kStatus_Success</i>             | if succeed, others failed. |
| <i>kStatus_FLEXCAN_Rx-FifoBusy</i> | Previous transfer ongoing. |

### 17.3.4.3 void FLEXCAN\_TransferAbortReceiveFifoEDMA ( CAN\_Type \* *base*, flexcan\_edma\_handle\_t \* *handle* )

This function aborts the receive process which used eDMA.

### Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.            |
| <i>handle</i> | Pointer to flexcan_edma_handle_t structure. |

## Chapter 18

### FTM: FlexTimer Driver

#### 18.1 Overview

The KSDK provides a driver for the FlexTimer Module (FTM) of Kinetis devices.

#### 18.2 Function groups

The FTM driver supports the generation of PWM signals, input capture, dual edge capture, output compare, and quadrature decoder modes. The driver also supports configuring each of the FTM fault inputs.

##### 18.2.1 Initialization and deinitialization

The function [FTM\\_Init\(\)](#) initializes the FTM with specified configurations. The function [FTM\\_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the FTM for the requested register update mode for registers with buffers. It also sets up the FTM's fault operation mode and FTM behavior in the BDM mode.

The function [FTM\\_Deinit\(\)](#) disables the FTM counter and turns off the module clock.

##### 18.2.2 PWM Operations

The function [FTM\\_SetupPwm\(\)](#) sets up FTM channels for the PWM output. The function sets up the PWM signal properties for multiple channels. Each channel has its own duty cycle and level-mode specified. However, the same PWM period and PWM mode is applied to all channels requesting the PWM output. The signal duty cycle is provided as a percentage of the PWM period. Its value should be between 0 and 100 0=inactive signal (0% duty cycle) and 100=always active signal (100% duty cycle).

The function [FTM\\_UpdatePwmDutycycle\(\)](#) updates the PWM signal duty cycle of a particular FTM channel.

The function [FTM\\_UpdateChnlEdgeLevelSelect\(\)](#) updates the level select bits of a particular FTM channel. This can be used to disable the PWM output when making changes to the PWM signal.

##### 18.2.3 Input capture operations

The function [FTM\\_SetupInputCapture\(\)](#) sets up an FTM channel for the input capture. The user can specify the capture edge and a filter value to be used when processing the input signal.

The function [FTM\\_SetupDualEdgeCapture\(\)](#) can be used to measure the pulse width of a signal. A channel pair is used during capture with the input signal coming through a channel n. The user can specify whether

## Register Update

to use one-shot or continuous capture, the capture edge for each channel, and any filter value to be used when processing the input signal.

### 18.2.4 Output compare operations

The function [FTM\\_SetupOutputCompare\(\)](#) sets up an FTM channel for the output comparison. The user can specify the channel output on a successful comparison and a comparison value.

### 18.2.5 Quad decode

The function [FTM\\_SetupQuadDecode\(\)](#) sets up FTM channels 0 and 1 for quad decoding. The user can specify the quad decoding mode, polarity, and filter properties for each input signal.

### 18.2.6 Fault operation

The function [FTM\\_SetupFault\(\)](#) sets up the properties for each fault. The user can specify the fault polarity and whether to use a filter on a fault input. The overall fault filter value and fault control mode are set up during initialization.

## 18.3 Register Update

Some of the FTM registers have buffers. The driver supports various methods to update these registers with the content of the register buffer. The registers can be updated using the PWM synchronized loading or an intermediate point loading. The update mechanism for register with buffers can be specified through the following fields available in the configuration structure.

```
uint32_t pwmSyncMode;  
uint32_t reloadPoints;
```

Multiple PWM synchronization update modes can be used by providing an OR'ed list of options available in the enumeration [ftm\\_pwm\\_sync\\_method\\_t](#) to the `pwmSyncMode` field.

When using an intermediate reload points, the PWM synchronization is not required. Multiple reload points can be used by providing an OR'ed list of options available in the enumeration [ftm\\_reload\\_point\\_t](#) to the `reloadPoints` field.

The driver initialization function sets up the appropriate bits in the FTM module based on the register update options selected.

If software PWM synchronization is used, the below function can be used to initiate a software trigger.

```
FTM_SetSoftwareTrigger(FTM0, true)
```

## 18.4 Typical use case

### 18.4.1 PWM output

Output a PWM signal on two FTM channels with different duty cycles. Periodically update the PWM signal duty cycle.

```
int main(void)
{
    bool brightnessUp = true; /* Indicates whether LEDs are brighter or dimmer. */
    ftm_config_t ftmInfo;
    uint8_t updatedDutycycle = 0U;
    ftm_chnl_pwm_signal_param_t ftmParam[2];

    /* Configures the FTM parameters with frequency 24 kHz */
    ftmParam[0].chnlNumber = (ftm_chnl_t)BOARD_FIRST_FTM_CHANNEL;
    ftmParam[0].level = kFTM_LowTrue;
    ftmParam[0].dutyCyclePercent = 0U;
    ftmParam[0].firstEdgeDelayPercent = 0U;

    ftmParam[1].chnlNumber = (ftm_chnl_t)BOARD_SECOND_FTM_CHANNEL;
    ftmParam[1].level = kFTM_LowTrue;
    ftmParam[1].dutyCyclePercent = 0U;
    ftmParam[1].firstEdgeDelayPercent = 0U;

    FTM_GetDefaultConfig(&ftmInfo);

    /* Initializes the FTM module. */
    FTM_Init(BOARD_FTM_BASEADDR, &ftmInfo);

    FTM_SetupPwm(BOARD_FTM_BASEADDR, ftmParam, 2U,
        kFTM_EdgeAlignedPwm, 24000U, FTM_SOURCE_CLOCK);
    FTM_StartTimer(BOARD_FTM_BASEADDR, kFTM_SystemClock);

    while (1)
    {
        /* Delays to check whether the LED brightness has changed. */
        delay();

        if (brightnessUp)
        {
            /* Increases the duty cycle until it reaches a limited value. */
            if (++updatedDutycycle == 100U)
            {
                brightnessUp = false;
            }
        }
        else
        {
            /* Decreases the duty cycle until it reaches a limited value. */
            if (--updatedDutycycle == 0U)
            {
                brightnessUp = true;
            }
        }

        /* Starts the PWM mode with an updated duty cycle. */
        FTM_UpdatePwmDutycycle(BOARD_FTM_BASEADDR, (
            ftm_chnl_t)BOARD_FIRST_FTM_CHANNEL, kFTM_EdgeAlignedPwm,
            updatedDutycycle);
        FTM_UpdatePwmDutycycle(BOARD_FTM_BASEADDR, (
            ftm_chnl_t)BOARD_SECOND_FTM_CHANNEL, kFTM_EdgeAlignedPwm,
            updatedDutycycle);

        /* Software trigger to update registers. */
        FTM_SetSoftwareTrigger(BOARD_FTM_BASEADDR, true);
    }
}
```

## Typical use case

## Data Structures

- struct `ftm_chnl_pwm_signal_param_t`  
*Options to configure a FTM channel's PWM signal. [More...](#)*
- struct `ftm_dual_edge_capture_param_t`  
*FlexTimer dual edge capture parameters. [More...](#)*
- struct `ftm_phase_params_t`  
*FlexTimer quadrature decode phase parameters. [More...](#)*
- struct `ftm_fault_param_t`  
*Structure is used to hold the parameters to configure a FTM fault. [More...](#)*
- struct `ftm_config_t`  
*FTM configuration structure. [More...](#)*

## Enumerations

- enum `ftm_chnl_t` {  
    `kFTM_Chnl_0` = 0U,  
    `kFTM_Chnl_1`,  
    `kFTM_Chnl_2`,  
    `kFTM_Chnl_3`,  
    `kFTM_Chnl_4`,  
    `kFTM_Chnl_5`,  
    `kFTM_Chnl_6`,  
    `kFTM_Chnl_7` }  
*List of FTM channels.*
- enum `ftm_fault_input_t` {  
    `kFTM_Fault_0` = 0U,  
    `kFTM_Fault_1`,  
    `kFTM_Fault_2`,  
    `kFTM_Fault_3` }  
*List of FTM faults.*
- enum `ftm_pwm_mode_t` {  
    `kFTM_EdgeAlignedPwm` = 0U,  
    `kFTM_CenterAlignedPwm`,  
    `kFTM_CombinedPwm` }  
*FTM PWM operation modes.*
- enum `ftm_pwm_level_select_t` {  
    `kFTM_NoPwmSignal` = 0U,  
    `kFTM_LowTrue`,  
    `kFTM_HighTrue` }  
*FTM PWM output pulse mode: high-true, low-true or no output.*
- enum `ftm_output_compare_mode_t` {  
    `kFTM_NoOutputSignal` = (1U << FTM\_CnSC\_MSA\_SHIFT),  
    `kFTM_ToggleOnMatch` = ((1U << FTM\_CnSC\_MSA\_SHIFT) | (1U << FTM\_CnSC\_ELSA\_SHIFT)),  
    `kFTM_ClearOnMatch` = ((1U << FTM\_CnSC\_MSA\_SHIFT) | (2U << FTM\_CnSC\_ELSA\_SHIFT)),  
    `kFTM_SetOnMatch` = ((1U << FTM\_CnSC\_MSA\_SHIFT) | (3U << FTM\_CnSC\_ELSA\_SHIFT))

T)) }

*FlexTimer output compare mode.*

- enum `ftm_input_capture_edge_t` {  
`kFTM_RisingEdge` = (1U << FTM\_CnSC\_ELSA\_SHIFT),  
`kFTM_FallingEdge` = (2U << FTM\_CnSC\_ELSA\_SHIFT),  
`kFTM_RiseAndFallEdge` = (3U << FTM\_CnSC\_ELSA\_SHIFT) }

*FlexTimer input capture edge.*

- enum `ftm_dual_edge_capture_mode_t` {  
`kFTM_OneShot` = 0U,  
`kFTM_Continuous` = (1U << FTM\_CnSC\_MSA\_SHIFT) }

*FlexTimer dual edge capture modes.*

- enum `ftm_quad_decode_mode_t` {  
`kFTM_QuadPhaseEncode` = 0U,  
`kFTM_QuadCountAndDir` }

*FlexTimer quadrature decode modes.*

- enum `ftm_phase_polarity_t` {  
`kFTM_QuadPhaseNormal` = 0U,  
`kFTM_QuadPhaseInvert` }

*FlexTimer quadrature phase polarities.*

- enum `ftm_deadtime_prescale_t` {  
`kFTM_Deadtime_Prescale_1` = 1U,  
`kFTM_Deadtime_Prescale_4`,  
`kFTM_Deadtime_Prescale_16` }

*FlexTimer pre-scaler factor for the dead time insertion.*

- enum `ftm_clock_source_t` {  
`kFTM_SystemClock` = 1U,  
`kFTM_FixedClock`,  
`kFTM_ExternalClock` }

*FlexTimer clock source selection.*

- enum `ftm_clock_prescale_t` {  
`kFTM_Prescale_Divide_1` = 0U,  
`kFTM_Prescale_Divide_2`,  
`kFTM_Prescale_Divide_4`,  
`kFTM_Prescale_Divide_8`,  
`kFTM_Prescale_Divide_16`,  
`kFTM_Prescale_Divide_32`,  
`kFTM_Prescale_Divide_64`,  
`kFTM_Prescale_Divide_128` }

*FlexTimer pre-scaler factor selection for the clock source.*

- enum `ftm_bdm_mode_t` {  
`kFTM_BdmMode_0` = 0U,  
`kFTM_BdmMode_1`,  
`kFTM_BdmMode_2`,  
`kFTM_BdmMode_3` }

*Options for the FlexTimer behaviour in BDM Mode.*

- enum `ftm_fault_mode_t` {

## Typical use case

```
kFTM_Fault_Disable = 0U,  
kFTM_Fault_EvenChnls,  
kFTM_Fault_AllChnlsMan,  
kFTM_Fault_AllChnlsAuto }
```

*Options for the FTM fault control mode.*

- enum `ftm_external_trigger_t` {  
    kFTM\_Chnl0Trigger = (1U << 4),  
    kFTM\_Chnl1Trigger = (1U << 5),  
    kFTM\_Chnl2Trigger = (1U << 0),  
    kFTM\_Chnl3Trigger = (1U << 1),  
    kFTM\_Chnl4Trigger = (1U << 2),  
    kFTM\_Chnl5Trigger = (1U << 3),  
    kFTM\_Chnl6Trigger,  
    kFTM\_Chnl7Trigger,  
    kFTM\_InitTrigger = (1U << 6),  
    kFTM\_ReloadInitTrigger = (1U << 7) }

*FTM external trigger options.*

- enum `ftm_pwm_sync_method_t` {  
    kFTM\_SoftwareTrigger = FTM\_SYNC\_SWSYNC\_MASK,  
    kFTM\_HardwareTrigger\_0 = FTM\_SYNC\_TRIG0\_MASK,  
    kFTM\_HardwareTrigger\_1 = FTM\_SYNC\_TRIG1\_MASK,  
    kFTM\_HardwareTrigger\_2 = FTM\_SYNC\_TRIG2\_MASK }

*FlexTimer PWM sync options to update registers with buffer.*

- enum `ftm_reload_point_t` {  
    kFTM\_Chnl0Match = (1U << 0),  
    kFTM\_Chnl1Match = (1U << 1),  
    kFTM\_Chnl2Match = (1U << 2),  
    kFTM\_Chnl3Match = (1U << 3),  
    kFTM\_Chnl4Match = (1U << 4),  
    kFTM\_Chnl5Match = (1U << 5),  
    kFTM\_Chnl6Match = (1U << 6),  
    kFTM\_Chnl7Match = (1U << 7),  
    kFTM\_CntMax = (1U << 8),  
    kFTM\_CntMin = (1U << 9),  
    kFTM\_HalfCycMatch = (1U << 10) }

*FTM options available as loading point for register reload.*

- enum `ftm_interrupt_enable_t` {



```

kFTM_Chnl0InterruptEnable = (1U << 0),
kFTM_Chnl1InterruptEnable = (1U << 1),
kFTM_Chnl2InterruptEnable = (1U << 2),
kFTM_Chnl3InterruptEnable = (1U << 3),
kFTM_Chnl4InterruptEnable = (1U << 4),
kFTM_Chnl5InterruptEnable = (1U << 5),
kFTM_Chnl6InterruptEnable = (1U << 6),
kFTM_Chnl7InterruptEnable = (1U << 7),
kFTM_FaultInterruptEnable = (1U << 8),
kFTM_TimeOverflowInterruptEnable = (1U << 9),
kFTM_ReloadInterruptEnable = (1U << 10) }

```

*List of FTM interrupts.*

- enum `ftm_status_flags_t` {
 

```

kFTM_Chnl0Flag = (1U << 0),
kFTM_Chnl1Flag = (1U << 1),
kFTM_Chnl2Flag = (1U << 2),
kFTM_Chnl3Flag = (1U << 3),
kFTM_Chnl4Flag = (1U << 4),
kFTM_Chnl5Flag = (1U << 5),
kFTM_Chnl6Flag = (1U << 6),
kFTM_Chnl7Flag = (1U << 7),
kFTM_FaultFlag = (1U << 8),
kFTM_TimeOverflowFlag = (1U << 9),
kFTM_ChnlTriggerFlag = (1U << 10),
kFTM_ReloadFlag = (1U << 11) }

```

*List of FTM flags.*

- enum `_ftm_quad_decoder_flags` {
 

```

kFTM_QuadDecoderCountingIncreaseFlag = FTM_QDCTRL_QUADIR_MASK,
kFTM_QuadDecoderCountingOverflowOnTopFlag = FTM_QDCTRL_TOFDIR_MASK }

```

*List of FTM Quad Decoder flags.*

## Functions

- void `FTM_SetupFault` (FTM\_Type \*base, `ftm_fault_input_t` faultNumber, const `ftm_fault_param_t` \*faultParams)
 

*Sets up the working of the FTM fault protection.*
- static void `FTM_SetGlobalTimeBaseOutputEnable` (FTM\_Type \*base, bool enable)
 

*Enables or disables the FTM global time base signal generation to other FTMs.*
- static void `FTM_SetOutputMask` (FTM\_Type \*base, `ftm_chnl_t` chnlNumber, bool mask)
 

*Sets the FTM peripheral timer channel output mask.*
- static void `FTM_SetSoftwareTrigger` (FTM\_Type \*base, bool enable)
 

*Enables or disables the FTM software trigger for PWM synchronization.*
- static void `FTM_SetWriteProtection` (FTM\_Type \*base, bool enable)
 

*Enables or disables the FTM write protection.*

## Driver version

- #define `FSL_FTM_DRIVER_VERSION` (`MAKE_VERSION`(2, 0, 2))

## Typical use case

Version 2.0.2.

## Initialization and deinitialization

- status\_t [FTM\\_Init](#) (FTM\_Type \*base, const [ftm\\_config\\_t](#) \*config)  
*Ungates the FTM clock and configures the peripheral for basic operation.*
- void [FTM\\_Deinit](#) (FTM\_Type \*base)  
*Gates the FTM clock.*
- void [FTM\\_GetDefaultConfig](#) ([ftm\\_config\\_t](#) \*config)  
*Fills in the FTM configuration structure with the default settings.*

## Channel mode operations

- status\_t [FTM\\_SetupPwm](#) (FTM\_Type \*base, const [ftm\\_chnl\\_pwm\\_signal\\_param\\_t](#) \*chnlParams, uint8\_t numOfChnls, [ftm\\_pwm\\_mode\\_t](#) mode, uint32\_t pwmFreq\_Hz, uint32\_t srcClock\_Hz)  
*Configures the PWM signal parameters.*
- void [FTM\\_UpdatePwmDutycycle](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlNumber, [ftm\\_pwm\\_mode\\_t](#) currentPwmMode, uint8\_t dutyCyclePercent)  
*Updates the duty cycle of an active PWM signal.*
- void [FTM\\_UpdateChnlEdgeLevelSelect](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlNumber, uint8\_t level)  
*Updates the edge level selection for a channel.*
- void [FTM\\_SetupInputCapture](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlNumber, [ftm\\_input\\_capture\\_edge\\_t](#) captureMode, uint32\_t filterValue)  
*Enables capturing an input signal on the channel using the function parameters.*
- void [FTM\\_SetupOutputCompare](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlNumber, [ftm\\_output\\_compare\\_mode\\_t](#) compareMode, uint32\_t compareValue)  
*Configures the FTM to generate timed pulses.*
- void [FTM\\_SetupDualEdgeCapture](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlPairNumber, const [ftm\\_dual\\_edge\\_capture\\_param\\_t](#) \*edgeParam, uint32\_t filterValue)  
*Configures the dual edge capture mode of the FTM.*

## Interrupt Interface

- void [FTM\\_EnableInterrupts](#) (FTM\_Type \*base, uint32\_t mask)  
*Enables the selected FTM interrupts.*
- void [FTM\\_DisableInterrupts](#) (FTM\_Type \*base, uint32\_t mask)  
*Disables the selected FTM interrupts.*
- uint32\_t [FTM\\_GetEnabledInterrupts](#) (FTM\_Type \*base)  
*Gets the enabled FTM interrupts.*

## Status Interface

- uint32\_t [FTM\\_GetStatusFlags](#) (FTM\_Type \*base)  
*Gets the FTM status flags.*
- void [FTM\\_ClearStatusFlags](#) (FTM\_Type \*base, uint32\_t mask)  
*Clears the FTM status flags.*

## Timer Start and Stop

- static void [FTM\\_StartTimer](#) (FTM\_Type \*base, [ftm\\_clock\\_source\\_t](#) clockSource)

- *Starts the FTM counter.*
- static void [FTM\\_StopTimer](#) (FTM\_Type \*base)
- *Stops the FTM counter.*

## Software output control

- static void [FTM\\_SetSoftwareCtrlEnable](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlNumber, bool value)  
*Enables or disables the channel software output control.*
- static void [FTM\\_SetSoftwareCtrlVal](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlNumber, bool value)  
*Sets the channel software output control value.*

## Channel pair operations

- static void [FTM\\_SetFaultControlEnable](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlPairNumber, bool value)  
*This function enables/disables the fault control in a channel pair.*
- static void [FTM\\_SetDeadTimeEnable](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlPairNumber, bool value)  
*This function enables/disables the dead time insertion in a channel pair.*
- static void [FTM\\_SetComplementaryEnable](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlPairNumber, bool value)  
*This function enables/disables complementary mode in a channel pair.*
- static void [FTM\\_SetInvertEnable](#) (FTM\_Type \*base, [ftm\\_chnl\\_t](#) chnlPairNumber, bool value)  
*This function enables/disables inverting control in a channel pair.*

## Quad Decoder

- void [FTM\\_SetupQuadDecode](#) (FTM\_Type \*base, const [ftm\\_phase\\_params\\_t](#) \*phaseAParams, const [ftm\\_phase\\_params\\_t](#) \*phaseBParams, [ftm\\_quad\\_decode\\_mode\\_t](#) quadMode)  
*Configures the parameters and activates the quadrature decoder mode.*
- static uint32\_t [FTM\\_GetQuadDecoderFlags](#) (FTM\_Type \*base)  
*Gets the FTM Quad Decoder flags.*
- static void [FTM\\_SetQuadDecoderModuloValue](#) (FTM\_Type \*base, uint32\_t startValue, uint32\_t overValue)  
*Sets the modulo values for Quad Decoder.*
- static uint32\_t [FTM\\_GetQuadDecoderCounterValue](#) (FTM\_Type \*base)  
*Gets the current Quad Decoder counter value.*
- static void [FTM\\_ClearQuadDecoderCounterValue](#) (FTM\_Type \*base)  
*Clears the current Quad Decoder counter value.*

## 18.5 Data Structure Documentation

### 18.5.1 struct [ftm\\_chnl\\_pwm\\_signal\\_param\\_t](#)

#### Data Fields

- [ftm\\_chnl\\_t](#) chnlNumber  
*The channel/channel pair number.*
- [ftm\\_pwm\\_level\\_select\\_t](#) level  
*PWM output active level select.*

## Data Structure Documentation

- `uint8_t` [dutyCyclePercent](#)  
*PWM pulse width, value should be between 0 to 100 0 = inactive signal(0% duty cycle)...*
- `uint8_t` [firstEdgeDelayPercent](#)  
*Used only in combined PWM mode to generate an asymmetrical PWM.*

### 18.5.1.0.0.55 Field Documentation

#### 18.5.1.0.0.55.1 `ftm_chnl_t` `ftm_chnl_pwm_signal_param_t::chnlNumber`

In combined mode, this represents the channel pair number.

#### 18.5.1.0.0.55.2 `ftm_pwm_level_select_t` `ftm_chnl_pwm_signal_param_t::level`

#### 18.5.1.0.0.55.3 `uint8_t` `ftm_chnl_pwm_signal_param_t::dutyCyclePercent`

100 = always active signal (100% duty cycle).

#### 18.5.1.0.0.55.4 `uint8_t` `ftm_chnl_pwm_signal_param_t::firstEdgeDelayPercent`

Specifies the delay to the first edge in a PWM period. If unsure leave as 0; Should be specified as a percentage of the PWM period

## 18.5.2 `struct` `ftm_dual_edge_capture_param_t`

### Data Fields

- `ftm_dual_edge_capture_mode_t` `mode`  
*Dual Edge Capture mode.*
- `ftm_input_capture_edge_t` `currChanEdgeMode`  
*Input capture edge select for channel n.*
- `ftm_input_capture_edge_t` `nextChanEdgeMode`  
*Input capture edge select for channel n+1.*

## 18.5.3 `struct` `ftm_phase_params_t`

### Data Fields

- `bool` [enablePhaseFilter](#)  
*True: enable phase filter; false: disable filter.*
- `uint32_t` [phaseFilterVal](#)  
*Filter value, used only if phase filter is enabled.*
- `ftm_phase_polarity_t` `phasePolarity`  
*Phase polarity.*

### 18.5.4 struct ftm\_fault\_param\_t

#### Data Fields

- bool [enableFaultInput](#)  
*True: Fault input is enabled; false: Fault input is disabled.*
- bool [faultLevel](#)  
*True: Fault polarity is active low; in other words, '0' indicates a fault; False: Fault polarity is active high.*
- bool [useFaultFilter](#)  
*True: Use the filtered fault signal; False: Use the direct path from fault input.*

### 18.5.5 struct ftm\_config\_t

This structure holds the configuration settings for the FTM peripheral. To initialize this structure to reasonable defaults, call the [FTM\\_GetDefaultConfig\(\)](#) function and pass a pointer to the configuration structure instance.

The configuration structure can be made constant so as to reside in flash.

#### Data Fields

- [ftm\\_clock\\_prescale\\_t](#) [prescale](#)  
*FTM clock prescale value.*
- [ftm\\_bdm\\_mode\\_t](#) [bdmMode](#)  
*FTM behavior in BDM mode.*
- [uint32\\_t](#) [pwmSyncMode](#)  
*Synchronization methods to use to update buffered registers; Multiple update modes can be used by providing an OR'ed list of options available in enumeration [ftm\\_pwm\\_sync\\_method\\_t](#).*
- [uint32\\_t](#) [reloadPoints](#)  
*FTM reload points; When using this, the PWM synchronization is not required.*
- [ftm\\_fault\\_mode\\_t](#) [faultMode](#)  
*FTM fault control mode.*
- [uint8\\_t](#) [faultFilterValue](#)  
*Fault input filter value.*
- [ftm\\_deadtime\\_prescale\\_t](#) [deadTimePrescale](#)  
*The dead time prescalar value.*
- [uint32\\_t](#) [deadTimeValue](#)  
*The dead time value [deadTimeValue](#)'s available range is 0-1023 when register has DTVALEX, otherwise its available range is 0-63.*
- [uint32\\_t](#) [extTriggers](#)  
*External triggers to enable.*
- [uint8\\_t](#) [chnlInitState](#)  
*Defines the initialization value of the channels in OUTINT register.*
- [uint8\\_t](#) [chnlPolarity](#)  
*Defines the output polarity of the channels in POL register.*
- bool [useGlobalTimeBase](#)  
*True: Use of an external global time base is enabled; False: disabled.*

## Enumeration Type Documentation

### 18.5.5.0.0.56 Field Documentation

#### 18.5.5.0.0.56.1 uint32\_t ftm\_config\_t::pwmSyncMode

#### 18.5.5.0.0.56.2 uint32\_t ftm\_config\_t::reloadPoints

Multiple reload points can be used by providing an OR'ed list of options available in enumeration [ftm\\_reload\\_point\\_t](#).

#### 18.5.5.0.0.56.3 uint32\_t ftm\_config\_t::deadTimeValue

#### 18.5.5.0.0.56.4 uint32\_t ftm\_config\_t::extTriggers

Multiple trigger sources can be enabled by providing an OR'ed list of options available in enumeration [ftm\\_external\\_trigger\\_t](#).

## 18.6 Enumeration Type Documentation

### 18.6.1 enum ftm\_chnl\_t

Note

Actual number of available channels is SoC dependent

Enumerator

- kFTM\_Chnl\_0* FTM channel number 0.
- kFTM\_Chnl\_1* FTM channel number 1.
- kFTM\_Chnl\_2* FTM channel number 2.
- kFTM\_Chnl\_3* FTM channel number 3.
- kFTM\_Chnl\_4* FTM channel number 4.
- kFTM\_Chnl\_5* FTM channel number 5.
- kFTM\_Chnl\_6* FTM channel number 6.
- kFTM\_Chnl\_7* FTM channel number 7.

### 18.6.2 enum ftm\_fault\_input\_t

Enumerator

- kFTM\_Fault\_0* FTM fault 0 input pin.
- kFTM\_Fault\_1* FTM fault 1 input pin.
- kFTM\_Fault\_2* FTM fault 2 input pin.
- kFTM\_Fault\_3* FTM fault 3 input pin.

### 18.6.3 enum ftm\_pwm\_mode\_t

Enumerator

*kFTM\_EdgeAlignedPwm* Edge-aligned PWM.  
*kFTM\_CenterAlignedPwm* Center-aligned PWM.  
*kFTM\_CombinedPwm* Combined PWM.

### 18.6.4 enum ftm\_pwm\_level\_select\_t

Enumerator

*kFTM\_NoPwmSignal* No PWM output on pin.  
*kFTM\_LowTrue* Low true pulses.  
*kFTM\_HighTrue* High true pulses.

### 18.6.5 enum ftm\_output\_compare\_mode\_t

Enumerator

*kFTM\_NoOutputSignal* No channel output when counter reaches CnV.  
*kFTM\_ToggleOnMatch* Toggle output.  
*kFTM\_ClearOnMatch* Clear output.  
*kFTM\_SetOnMatch* Set output.

### 18.6.6 enum ftm\_input\_capture\_edge\_t

Enumerator

*kFTM\_RisingEdge* Capture on rising edge only.  
*kFTM\_FallingEdge* Capture on falling edge only.  
*kFTM\_RiseAndFallEdge* Capture on rising or falling edge.

### 18.6.7 enum ftm\_dual\_edge\_capture\_mode\_t

Enumerator

*kFTM\_OneShot* One-shot capture mode.  
*kFTM\_Continuous* Continuous capture mode.

### 18.6.8 enum ftm\_quad\_decode\_mode\_t

Enumerator

*kFTM\_QuadPhaseEncode* Phase A and Phase B encoding mode.

*kFTM\_QuadCountAndDir* Count and direction encoding mode.

### 18.6.9 enum ftm\_phase\_polarity\_t

Enumerator

*kFTM\_QuadPhaseNormal* Phase input signal is not inverted.

*kFTM\_QuadPhaseInvert* Phase input signal is inverted.

### 18.6.10 enum ftm\_deadtime\_prescale\_t

Enumerator

*kFTM\_Deadtime\_Prescale\_1* Divide by 1.

*kFTM\_Deadtime\_Prescale\_4* Divide by 4.

*kFTM\_Deadtime\_Prescale\_16* Divide by 16.

### 18.6.11 enum ftm\_clock\_source\_t

Enumerator

*kFTM\_SystemClock* System clock selected.

*kFTM\_FixedClock* Fixed frequency clock.

*kFTM\_ExternalClock* External clock.

### 18.6.12 enum ftm\_clock\_prescale\_t

Enumerator

*kFTM\_Prescale\_Divide\_1* Divide by 1.

*kFTM\_Prescale\_Divide\_2* Divide by 2.

*kFTM\_Prescale\_Divide\_4* Divide by 4.

*kFTM\_Prescale\_Divide\_8* Divide by 8.

*kFTM\_Prescale\_Divide\_16* Divide by 16.

*kFTM\_Prescale\_Divide\_32* Divide by 32.

*kFTM\_Prescale\_Divide\_64* Divide by 64.

*kFTM\_Prescale\_Divide\_128* Divide by 128.



### 18.6.13 enum ftm\_bdm\_mode\_t

Enumerator

- kFTM\_BdmMode\_0*** FTM counter stopped, CH(n)F bit can be set, FTM channels in functional mode, writes to MOD,CNTIN and C(n)V registers bypass the register buffers.
- kFTM\_BdmMode\_1*** FTM counter stopped, CH(n)F bit is not set, FTM channels outputs are forced to their safe value , writes to MOD,CNTIN and C(n)V registers bypass the register buffers.
- kFTM\_BdmMode\_2*** FTM counter stopped, CH(n)F bit is not set, FTM channels outputs are frozen when chip enters in BDM mode, writes to MOD,CNTIN and C(n)V registers bypass the register buffers.
- kFTM\_BdmMode\_3*** FTM counter in functional mode, CH(n)F bit can be set, FTM channels in functional mode, writes to MOD,CNTIN and C(n)V registers is in fully functional mode.

### 18.6.14 enum ftm\_fault\_mode\_t

Enumerator

- kFTM\_Fault\_Disable*** Fault control is disabled for all channels.
- kFTM\_Fault\_EvenChnls*** Enabled for even channels only(0,2,4,6) with manual fault clearing.
- kFTM\_Fault\_AllChnlsMan*** Enabled for all channels with manual fault clearing.
- kFTM\_Fault\_AllChnlsAuto*** Enabled for all channels with automatic fault clearing.

### 18.6.15 enum ftm\_external\_trigger\_t

Note

Actual available external trigger sources are SoC-specific

Enumerator

- kFTM\_Chnl0Trigger*** Generate trigger when counter equals chnl 0 CnV reg.
- kFTM\_Chnl1Trigger*** Generate trigger when counter equals chnl 1 CnV reg.
- kFTM\_Chnl2Trigger*** Generate trigger when counter equals chnl 2 CnV reg.
- kFTM\_Chnl3Trigger*** Generate trigger when counter equals chnl 3 CnV reg.
- kFTM\_Chnl4Trigger*** Generate trigger when counter equals chnl 4 CnV reg.
- kFTM\_Chnl5Trigger*** Generate trigger when counter equals chnl 5 CnV reg.
- kFTM\_Chnl6Trigger*** Available on certain SoC's, generate trigger when counter equals chnl 6 CnV reg.
- kFTM\_Chnl7Trigger*** Available on certain SoC's, generate trigger when counter equals chnl 7 CnV reg.
- kFTM\_InitTrigger*** Generate Trigger when counter is updated with CNTIN.
- kFTM\_ReloadInitTrigger*** Available on certain SoC's, trigger on reload point.

### 18.6.16 enum ftm\_pwm\_sync\_method\_t

Enumerator

***kFTM\_SoftwareTrigger*** Software triggers PWM sync.  
***kFTM\_HardwareTrigger\_0*** Hardware trigger 0 causes PWM sync.  
***kFTM\_HardwareTrigger\_1*** Hardware trigger 1 causes PWM sync.  
***kFTM\_HardwareTrigger\_2*** Hardware trigger 2 causes PWM sync.

### 18.6.17 enum ftm\_reload\_point\_t

Note

Actual available reload points are SoC-specific

Enumerator

***kFTM\_Chnl0Match*** Channel 0 match included as a reload point.  
***kFTM\_Chnl1Match*** Channel 1 match included as a reload point.  
***kFTM\_Chnl2Match*** Channel 2 match included as a reload point.  
***kFTM\_Chnl3Match*** Channel 3 match included as a reload point.  
***kFTM\_Chnl4Match*** Channel 4 match included as a reload point.  
***kFTM\_Chnl5Match*** Channel 5 match included as a reload point.  
***kFTM\_Chnl6Match*** Channel 6 match included as a reload point.  
***kFTM\_Chnl7Match*** Channel 7 match included as a reload point.  
***kFTM\_CntMax*** Use in up-down count mode only, reload when counter reaches the maximum value.  
  
***kFTM\_CntMin*** Use in up-down count mode only, reload when counter reaches the minimum value.  
  
***kFTM\_HalfCycMatch*** Available on certain SoC's, half cycle match reload point.

### 18.6.18 enum ftm\_interrupt\_enable\_t

Note

Actual available interrupts are SoC-specific

Enumerator

***kFTM\_Chnl0InterruptEnable*** Channel 0 interrupt.  
***kFTM\_Chnl1InterruptEnable*** Channel 1 interrupt.  
***kFTM\_Chnl2InterruptEnable*** Channel 2 interrupt.  
***kFTM\_Chnl3InterruptEnable*** Channel 3 interrupt.  
***kFTM\_Chnl4InterruptEnable*** Channel 4 interrupt.

*kFTM\_Chnl5InterruptEnable* Channel 5 interrupt.  
*kFTM\_Chnl6InterruptEnable* Channel 6 interrupt.  
*kFTM\_Chnl7InterruptEnable* Channel 7 interrupt.  
*kFTM\_FaultInterruptEnable* Fault interrupt.  
*kFTM\_TimeOverflowInterruptEnable* Time overflow interrupt.  
*kFTM\_ReloadInterruptEnable* Reload interrupt; Available only on certain SoC's.

### 18.6.19 enum ftm\_status\_flags\_t

Note

Actual available flags are SoC-specific

Enumerator

*kFTM\_Chnl0Flag* Channel 0 Flag.  
*kFTM\_Chnl1Flag* Channel 1 Flag.  
*kFTM\_Chnl2Flag* Channel 2 Flag.  
*kFTM\_Chnl3Flag* Channel 3 Flag.  
*kFTM\_Chnl4Flag* Channel 4 Flag.  
*kFTM\_Chnl5Flag* Channel 5 Flag.  
*kFTM\_Chnl6Flag* Channel 6 Flag.  
*kFTM\_Chnl7Flag* Channel 7 Flag.  
*kFTM\_FaultFlag* Fault Flag.  
*kFTM\_TimeOverflowFlag* Time overflow Flag.  
*kFTM\_ChnlTriggerFlag* Channel trigger Flag.  
*kFTM\_ReloadFlag* Reload Flag; Available only on certain SoC's.

### 18.6.20 enum \_ftm\_quad\_decoder\_flags

Enumerator

*kFTM\_QuadDecoderCountingIncreaseFlag* Counting direction is increasing (FTM counter increment), or the direction is decreasing.  
*kFTM\_QuadDecoderCountingOverflowOnTopFlag* Indicates if the TOF bit was set on the top or the bottom of counting.

## 18.7 Function Documentation

### 18.7.1 status\_t FTM\_Init ( FTM\_Type \* *base*, const ftm\_config\_t \* *config* )

Note

This API should be called at the beginning of the application which is using the FTM driver.

## Function Documentation

### Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>base</i>   | FTM peripheral base address                  |
| <i>config</i> | Pointer to the user configuration structure. |

### Returns

kStatus\_Success indicates success; Else indicates failure.

## 18.7.2 void FTM\_Deinit ( FTM\_Type \* *base* )

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | FTM peripheral base address |
|-------------|-----------------------------|

## 18.7.3 void FTM\_GetDefaultConfig ( ftm\_config\_t \* *config* )

The default values are:

```
* config->prescale = kFTM_Prescale_Divide_1;
* config->bdmMode = kFTM_BdmMode_0;
* config->pwmSyncMode = kFTM_SoftwareTrigger;
* config->reloadPoints = 0;
* config->faultMode = kFTM_Fault_Disable;
* config->faultFilterValue = 0;
* config->deadTimePrescale = kFTM_Deadtime_Prescale_1;
* config->deadTimeValue = 0;
* config->extTriggers = 0;
* config->chnlInitState = 0;
* config->chnlPolarity = 0;
* config->useGlobalTimeBase = false;
*
```

### Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>config</i> | Pointer to the user configuration structure. |
|---------------|----------------------------------------------|

## 18.7.4 status\_t FTM\_SetupPwm ( FTM\_Type \* *base*, const ftm\_chnl\_pwm\_signal\_param\_t \* *chnlParams*, uint8\_t *numOfChnls*, ftm\_pwm\_mode\_t *mode*, uint32\_t *pwmFreq\_Hz*, uint32\_t *srcClock\_Hz* )

Call this function to configure the PWM signal period, mode, duty cycle, and edge. Use this function to configure all FTM channels that are used to output a PWM signal.

## Parameters

|                    |                                                                                     |
|--------------------|-------------------------------------------------------------------------------------|
| <i>base</i>        | FTM peripheral base address                                                         |
| <i>chnlParams</i>  | Array of PWM channel parameters to configure the channel(s)                         |
| <i>numOfChnls</i>  | Number of channels to configure; This should be the size of the array passed in     |
| <i>mode</i>        | PWM operation mode, options available in enumeration <a href="#">ftm_pwm_mode_t</a> |
| <i>pwmFreq_Hz</i>  | PWM signal frequency in Hz                                                          |
| <i>srcClock_Hz</i> | FTM counter clock in Hz                                                             |

## Returns

kStatus\_Success if the PWM setup was successful kStatus\_Error on failure

### 18.7.5 void FTM\_UpdatePwmDutycycle ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlNumber*, ftm\_pwm\_mode\_t *currentPwmMode*, uint8\_t *dutyCyclePercent* )

## Parameters

|                          |                                                                                                                                   |
|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>              | FTM peripheral base address                                                                                                       |
| <i>chnlNumber</i>        | The channel/channel pair number. In combined mode, this represents the channel pair number                                        |
| <i>currentPwm-Mode</i>   | The current PWM mode set during PWM setup                                                                                         |
| <i>dutyCycle-Percent</i> | New PWM pulse width; The value should be between 0 to 100 0=inactive signal(0% duty cycle)... 100=active signal (100% duty cycle) |

### 18.7.6 void FTM\_UpdateChnlEdgeLevelSelect ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlNumber*, uint8\_t *level* )

## Parameters

|                   |                                                                                                                                                   |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | FTM peripheral base address                                                                                                                       |
| <i>chnlNumber</i> | The channel number                                                                                                                                |
| <i>level</i>      | The level to be set to the ELSnB:ELSnA field; Valid values are 00, 01, 10, 11. See the Kinetis SoC reference manual for details about this field. |

### 18.7.7 void FTM\_SetupInputCapture ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlNumber*, ftm\_input\_capture\_edge\_t *captureMode*, uint32\_t *filterValue* )

When the edge specified in the *captureMode* argument occurs on the channel, the FTM counter is captured into the CnV register. The user has to read the CnV register separately to get this value. The filter function is disabled if the *filterVal* argument passed in is 0. The filter function is available only for channels 0, 1, 2, 3.

Parameters

|                    |                                                                             |
|--------------------|-----------------------------------------------------------------------------|
| <i>base</i>        | FTM peripheral base address                                                 |
| <i>chnlNumber</i>  | The channel number                                                          |
| <i>captureMode</i> | Specifies which edge to capture                                             |
| <i>filterValue</i> | Filter value, specify 0 to disable filter. Available only for channels 0-3. |

### 18.7.8 void FTM\_SetupOutputCompare ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlNumber*, ftm\_output\_compare\_mode\_t *compareMode*, uint32\_t *compareValue* )

When the FTM counter matches the value of *compareVal* argument (this is written into CnV reg), the channel output is changed based on what is specified in the *compareMode* argument.

Parameters

|                     |                                                                        |
|---------------------|------------------------------------------------------------------------|
| <i>base</i>         | FTM peripheral base address                                            |
| <i>chnlNumber</i>   | The channel number                                                     |
| <i>compareMode</i>  | Action to take on the channel output when the compare condition is met |
| <i>compareValue</i> | Value to be programmed in the CnV register.                            |

### 18.7.9 void FTM\_SetupDualEdgeCapture ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlPairNumber*, const ftm\_dual\_edge\_capture\_param\_t \* *edgeParam*, uint32\_t *filterValue* )

This function sets up the dual edge capture mode on a channel pair. The capture edge for the channel pair and the capture mode (one-shot or continuous) is specified in the parameter argument. The filter function is disabled if the *filterVal* argument passed is zero. The filter function is available only on channels 0 and 2. The user has to read the channel CnV registers separately to get the capture values.

## Parameters

|                        |                                                                                     |
|------------------------|-------------------------------------------------------------------------------------|
| <i>base</i>            | FTM peripheral base address                                                         |
| <i>chnlPair-Number</i> | The FTM channel pair number; options are 0, 1, 2, 3                                 |
| <i>edgeParam</i>       | Sets up the dual edge capture function                                              |
| <i>filterValue</i>     | Filter value, specify 0 to disable filter. Available only for channel pair 0 and 1. |

### 18.7.10 void FTM\_SetupFault ( FTM\_Type \* *base*, ftm\_fault\_input\_t *faultNumber*, const ftm\_fault\_param\_t \* *faultParams* )

FTM can have up to 4 fault inputs. This function sets up fault parameters, fault level, and a filter.

## Parameters

|                    |                                          |
|--------------------|------------------------------------------|
| <i>base</i>        | FTM peripheral base address              |
| <i>faultNumber</i> | FTM fault to configure.                  |
| <i>faultParams</i> | Parameters passed in to set up the fault |

### 18.7.11 void FTM\_EnableInterrupts ( FTM\_Type \* *base*, uint32\_t *mask* )

## Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | FTM peripheral base address                                                                                         |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">ftm_interrupt_enable_t</a> |

### 18.7.12 void FTM\_DisableInterrupts ( FTM\_Type \* *base*, uint32\_t *mask* )

## Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | FTM peripheral base address                                                                                         |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">ftm_interrupt_enable_t</a> |

**18.7.13**    `uint32_t FTM_GetEnabledInterrupts ( FTM_Type * base )`



## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | FTM peripheral base address |
|-------------|-----------------------------|

## Returns

The enabled interrupts. This is the logical OR of members of the enumeration [ftm\\_interrupt\\_enable\\_t](#)

#### 18.7.14 uint32\_t FTM\_GetStatusFlags ( FTM\_Type \* *base* )

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | FTM peripheral base address |
|-------------|-----------------------------|

## Returns

The status flags. This is the logical OR of members of the enumeration [ftm\\_status\\_flags\\_t](#)

#### 18.7.15 void FTM\_ClearStatusFlags ( FTM\_Type \* *base*, uint32\_t *mask* )

## Parameters

|             |                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | FTM peripheral base address                                                                                      |
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">ftm_status_flags_t</a> |

#### 18.7.16 static void FTM\_StartTimer ( FTM\_Type \* *base*, ftm\_clock\_source\_t *clockSource* ) [inline], [static]

## Parameters

|                    |                                                                              |
|--------------------|------------------------------------------------------------------------------|
| <i>base</i>        | FTM peripheral base address                                                  |
| <i>clockSource</i> | FTM clock source; After the clock source is set, the counter starts running. |

#### 18.7.17 static void FTM\_StopTimer ( FTM\_Type \* *base* ) [inline], [static]

## Function Documentation

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | FTM peripheral base address |
|-------------|-----------------------------|

**18.7.18 static void FTM\_SetSoftwareCtrlEnable ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlNumber*, bool *value* ) [inline], [static]**

### Parameters

|                   |                                                                                                                            |
|-------------------|----------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | FTM peripheral base address                                                                                                |
| <i>chnlNumber</i> | Channel to be enabled or disabled                                                                                          |
| <i>value</i>      | true: channel output is affected by software output control false: channel output is unaffected by software output control |

**18.7.19 static void FTM\_SetSoftwareCtrlVal ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlNumber*, bool *value* ) [inline], [static]**

### Parameters

|                   |                               |
|-------------------|-------------------------------|
| <i>base</i>       | FTM peripheral base address.  |
| <i>chnlNumber</i> | Channel to be configured      |
| <i>value</i>      | true to set 1, false to set 0 |

**18.7.20 static void FTM\_SetGlobalTimeBaseOutputEnable ( FTM\_Type \* *base*, bool *enable* ) [inline], [static]**

### Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | FTM peripheral base address      |
| <i>enable</i> | true to enable, false to disable |

**18.7.21 static void FTM\_SetOutputMask ( FTM\_Type \* *base*, ftm\_chnl\_t *chnlNumber*, bool *mask* ) [inline], [static]**

## Parameters

|                   |                                                                        |
|-------------------|------------------------------------------------------------------------|
| <i>base</i>       | FTM peripheral base address                                            |
| <i>chnlNumber</i> | Channel to be configured                                               |
| <i>mask</i>       | true: masked, channel is forced to its inactive state; false: unmasked |

**18.7.22** `static void FTM_SetFaultControlEnable ( FTM_Type * base, ftm_chnl_t chnlPairNumber, bool value ) [inline], [static]`

## Parameters

|                        |                                                                           |
|------------------------|---------------------------------------------------------------------------|
| <i>base</i>            | FTM peripheral base address                                               |
| <i>chnlPair-Number</i> | The FTM channel pair number; options are 0, 1, 2, 3                       |
| <i>value</i>           | true: Enable fault control for this channel pair; false: No fault control |

**18.7.23** `static void FTM_SetDeadTimeEnable ( FTM_Type * base, ftm_chnl_t chnlPairNumber, bool value ) [inline], [static]`

## Parameters

|                        |                                                                           |
|------------------------|---------------------------------------------------------------------------|
| <i>base</i>            | FTM peripheral base address                                               |
| <i>chnlPair-Number</i> | The FTM channel pair number; options are 0, 1, 2, 3                       |
| <i>value</i>           | true: Insert dead time in this channel pair; false: No dead time inserted |

**18.7.24** `static void FTM_SetComplementaryEnable ( FTM_Type * base, ftm_chnl_t chnlPairNumber, bool value ) [inline], [static]`

## Parameters

|                        |                                                                    |
|------------------------|--------------------------------------------------------------------|
| <i>base</i>            | FTM peripheral base address                                        |
| <i>chnlPair-Number</i> | The FTM channel pair number; options are 0, 1, 2, 3                |
| <i>value</i>           | true: enable complementary mode; false: disable complementary mode |

**18.7.25** `static void FTM_SetInvertEnable ( FTM_Type * base, ftm_chnl_t chnlPairNumber, bool value ) [inline], [static]`

## Parameters

|                        |                                                     |
|------------------------|-----------------------------------------------------|
| <i>base</i>            | FTM peripheral base address                         |
| <i>chnlPair-Number</i> | The FTM channel pair number; options are 0, 1, 2, 3 |
| <i>value</i>           | true: enable inverting; false: disable inverting    |

**18.7.26** `void FTM_SetupQuadDecode ( FTM_Type * base, const ftm_phase_params_t * phaseAParams, const ftm_phase_params_t * phaseBParams, ftm_quad_decode_mode_t quadMode )`

## Parameters

|                     |                                                       |
|---------------------|-------------------------------------------------------|
| <i>base</i>         | FTM peripheral base address                           |
| <i>phaseAParams</i> | Phase A configuration parameters                      |
| <i>phaseBParams</i> | Phase B configuration parameters                      |
| <i>quadMode</i>     | Selects encoding mode used in quadrature decoder mode |

**18.7.27** `static uint32_t FTM_GetQuadDecoderFlags ( FTM_Type * base )  
[inline], [static]`

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | FTM peripheral base address. |
|-------------|------------------------------|

## Returns

Flag mask of FTM Quad Decoder, see [\\_ftm\\_quad\\_decoder\\_flags](#).

**18.7.28** `static void FTM_SetQuadDecoderModuloValue ( FTM_Type * base,  
uint32_t startValue, uint32_t overValue ) [inline], [static]`

The modulo values configure the minimum and maximum values that the Quad decoder counter can reach. After the counter goes over, the counter value goes to the other side and decrease/increase again.

## Function Documentation

### Parameters

|                   |                                                |
|-------------------|------------------------------------------------|
| <i>base</i>       | FTM peripheral base address.                   |
| <i>startValue</i> | The low limit value for Quad Decoder counter.  |
| <i>overValue</i>  | The high limit value for Quad Decoder counter. |

**18.7.29** `static uint32_t FTM_GetQuadDecoderCounterValue ( FTM_Type * base )  
[inline], [static]`

### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | FTM peripheral base address. |
|-------------|------------------------------|

### Returns

Current quad Decoder counter value.

**18.7.30** `static void FTM_ClearQuadDecoderCounterValue ( FTM_Type * base )  
[inline], [static]`

The counter is set as the initial value.

### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | FTM peripheral base address. |
|-------------|------------------------------|

**18.7.31** `static void FTM_SetSoftwareTrigger ( FTM_Type * base, bool enable )  
[inline], [static]`

### Parameters

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| <i>base</i>   | FTM peripheral base address                                                 |
| <i>enable</i> | true: software trigger is selected, false: software trigger is not selected |

**18.7.32** `static void FTM_SetWriteProtection ( FTM_Type * base, bool enable )  
[inline], [static]`

## Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | FTM peripheral base address                                            |
| <i>enable</i> | true: Write-protection is enabled, false: Write-protection is disabled |





## Chapter 19

# GPIO: General-Purpose Input/Output Driver

### 19.1 Overview

#### Modules

- [FGPIO Driver](#)
- [GPIO Driver](#)

#### Data Structures

- struct [gpio\\_pin\\_config\\_t](#)  
*The GPIO pin configuration structure. [More...](#)*

#### Enumerations

- enum [gpio\\_pin\\_direction\\_t](#) {  
    [kGPIO\\_DigitalInput](#) = 0U,  
    [kGPIO\\_DigitalOutput](#) = 1U }  
*GPIO direction definition.*

#### Driver version

- #define [FSL\\_GPIO\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 1, 1))  
*GPIO driver version 2.1.1.*

### 19.2 Data Structure Documentation

#### 19.2.1 struct [gpio\\_pin\\_config\\_t](#)

Each pin can only be configured as either an output pin or an input pin at a time. If configured as an input pin, leave the outputConfig unused. Note that in some use cases, the corresponding port property should be configured in advance with the [PORT\\_SetPinConfig\(\)](#).

#### Data Fields

- [gpio\\_pin\\_direction\\_t](#) [pinDirection](#)  
*GPIO direction, input or output.*
- uint8\_t [outputLogic](#)  
*Set a default output logic, which has no use in input.*

## Enumeration Type Documentation

### 19.3 Macro Definition Documentation

#### 19.3.1 #define FSL\_GPIO\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))

### 19.4 Enumeration Type Documentation

#### 19.4.1 enum gpio\_pin\_direction\_t

Enumerator

***kGPIO\_DigitalInput*** Set current pin as digital input.

***kGPIO\_DigitalOutput*** Set current pin as digital output.

## 19.5 GPIO Driver

### 19.5.1 Overview

The KSDK provides a peripheral driver for the General-Purpose Input/Output (GPIO) module of Kinetis devices.

### 19.5.2 Typical use case

#### 19.5.2.1 Output Operation

```
/* Output pin configuration */
gpio_pin_config_t led_config =
{
    kGpioDigitalOutput,
    1,
};
/* Sets the configuration */
GPIO_PinInit(GPIO_LED, LED_PINNUM, &led_config);
```

#### 19.5.2.2 Input Operation

```
/* Input pin configuration */
PORT_SetPinInterruptConfig(BOARD_SW2_PORT, BOARD_SW2_GPIO_PIN,
    kPORT_InterruptFallingEdge);
NVIC_EnableIRQ(BOARD_SW2_IRQ);
gpio_pin_config_t sw1_config =
{
    kGpioDigitalInput,
    0,
};
/* Sets the input pin configuration */
GPIO_PinInit(GPIO_SW1, SW1_PINNUM, &sw1_config);
```

## GPIO Configuration

- void [GPIO\\_PinInit](#) (GPIO\_Type \*base, uint32\_t pin, const [gpio\\_pin\\_config\\_t](#) \*config)  
*Initializes a GPIO pin used by the board.*

## GPIO Output Operations

- static void [GPIO\\_WritePinOutput](#) (GPIO\_Type \*base, uint32\_t pin, uint8\_t output)  
*Sets the output level of the multiple GPIO pins to the logic 1 or 0.*
- static void [GPIO\\_SetPinsOutput](#) (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 1.*
- static void [GPIO\\_ClearPinsOutput](#) (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 0.*
- static void [GPIO\\_TogglePinsOutput](#) (GPIO\_Type \*base, uint32\_t mask)  
*Reverses the current output logic of the multiple GPIO pins.*

## GPIO Driver

### GPIO Input Operations

- static uint32\_t [GPIO\\_ReadPinInput](#) (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current input value of the GPIO port.*

### GPIO Interrupt

- uint32\_t [GPIO\\_GetPinsInterruptFlags](#) (GPIO\_Type \*base)  
*Reads the GPIO port interrupt status flag.*
- void [GPIO\\_ClearPinsInterruptFlags](#) (GPIO\_Type \*base, uint32\_t mask)  
*Clears multiple GPIO pin interrupt status flags.*

## 19.5.3 Function Documentation

### 19.5.3.1 void GPIO\_PinInit ( GPIO\_Type \* *base*, uint32\_t *pin*, const gpio\_pin\_config\_t \* *config* )

To initialize the GPIO, define a pin configuration, as either input or output, in the user file. Then, call the [GPIO\\_PinInit\(\)](#) function.

This is an example to define an input pin or an output pin configuration.

```
* // Define a digital input pin configuration,  
* gpio_pin_config_t config =  
* {  
*     kGPIO_DigitalInput,  
*     0,  
* }  
* //Define a digital output pin configuration,  
* gpio_pin_config_t config =  
* {  
*     kGPIO_DigitalOutput,  
*     0,  
* }  
*
```

#### Parameters

|               |                                                                |
|---------------|----------------------------------------------------------------|
| <i>base</i>   | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.) |
| <i>pin</i>    | GPIO port pin number                                           |
| <i>config</i> | GPIO pin configuration pointer                                 |

### 19.5.3.2 static void GPIO\_WritePinOutput ( GPIO\_Type \* *base*, uint32\_t *pin*, uint8\_t *output* ) [inline], [static]

## Parameters

|               |                                                                                                                                                                                        |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)                                                                                                                         |
| <i>pin</i>    | GPIO pin number                                                                                                                                                                        |
| <i>output</i> | GPIO pin output logic level. <ul style="list-style-type: none"> <li>• 0: corresponding pin output low-logic level.</li> <li>• 1: corresponding pin output high-logic level.</li> </ul> |

### 19.5.3.3 static void GPIO\_SetPinsOutput ( GPIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

## Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.) |
| <i>mask</i> | GPIO pin number macro                                          |

### 19.5.3.4 static void GPIO\_ClearPinsOutput ( GPIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

## Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.) |
| <i>mask</i> | GPIO pin number macro                                          |

### 19.5.3.5 static void GPIO\_TogglePinsOutput ( GPIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

## Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.) |
| <i>mask</i> | GPIO pin number macro                                          |

### 19.5.3.6 static uint32\_t GPIO\_ReadPinInput ( GPIO\_Type \* *base*, uint32\_t *pin* ) [inline], [static]

## GPIO Driver

### Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.) |
| <i>pin</i>  | GPIO pin number                                                |

### Return values

|             |                                                                                                                                                                       |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>GPIO</i> | port input value <ul style="list-style-type: none"><li>• 0: corresponding pin input low-logic level.</li><li>• 1: corresponding pin input high-logic level.</li></ul> |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### 19.5.3.7 uint32\_t GPIO\_GetPinsInterruptFlags ( GPIO\_Type \* *base* )

If a pin is configured to generate the DMA request, the corresponding flag is cleared automatically at the completion of the requested DMA transfer. Otherwise, the flag remains set until a logic one is written to that flag. If configured for a level sensitive interrupt that remains asserted, the flag is set again immediately.

### Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.) |
|-------------|----------------------------------------------------------------|

### Return values

|            |                                                                                                             |
|------------|-------------------------------------------------------------------------------------------------------------|
| <i>The</i> | current GPIO port interrupt status flag, for example, 0x00010001 means the pin 0 and 17 have the interrupt. |
|------------|-------------------------------------------------------------------------------------------------------------|

### 19.5.3.8 void GPIO\_ClearPinsInterruptFlags ( GPIO\_Type \* *base*, uint32\_t *mask* )

### Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.) |
| <i>mask</i> | GPIO pin number macro                                          |

## 19.6 FGPIO Driver

This chapter describes the programming interface of the FGPIO driver. The FGPIO driver configures the FGPIO module and provides a functional interface to build the GPIO application.

### Note

FGPIO (Fast GPIO) is only available in a few MCUs. FGPIO and GPIO share the same peripheral but use different registers. FGPIO is closer to the core than the regular GPIO and it's faster to read and write.

### 19.6.1 Typical use case

#### 19.6.1.1 Output Operation

```
/* Output pin configuration */
gpio_pin_config_t led_config =
{
    kGpioDigitalOutput,
    1,
};
/* Sets the configuration */
FGPIO_PinInit(FGPIO_LED, LED_PINNUM, &led_config);
```

#### 19.6.1.2 Input Operation

```
/* Input pin configuration */
PORT_SetPinInterruptConfig(BOARD_SW2_PORT, BOARD_SW2_FGPIO_PIN,
    kPORT_InterruptFallingEdge);
NVIC_EnableIRQ(BOARD_SW2_IRQ);
gpio_pin_config_t sw1_config =
{
    kGpioDigitalInput,
    0,
};
/* Sets the input pin configuration */
FGPIO_PinInit(FGPIO_SW1, SW1_PINNUM, &sw1_config);
```







## Chapter 20

### I2C: Inter-Integrated Circuit Driver

#### 20.1 Overview

##### Modules

- [I2C DMA Driver](#)
- [I2C Driver](#)
- [I2C FreeRTOS Driver](#)
- [I2C eDMA Driver](#)
- [I2C  \$\mu\$ COS/II Driver](#)
- [I2C  \$\mu\$ COS/III Driver](#)

## I2C Driver

### 20.2 I2C Driver

#### 20.2.1 Overview

The KSDK provides a peripheral driver for the Inter-Integrated Circuit (I2C) module of Kinetis devices.

The I2C driver includes functional APIs and transactional APIs.

Functional APIs target the low-level APIs. Functional APIs can be used for the I2C master/slave initialization/configuration/operation for optimization/customization purpose. Using the functional APIs requires knowing the I2C master peripheral and how to organize functional APIs to meet the application requirements. The I2C functional operation groups provide the functional APIs set.

Transactional APIs target the high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code using the functional APIs or accessing the hardware registers.

Transactional APIs support asynchronous transfer. This means that the functions [I2C\\_MasterTransferNonBlocking\(\)](#) set up the interrupt non-blocking transfer. When the transfer completes, the upper layer is notified through a callback function with the status.

#### 20.2.2 Typical use case

##### 20.2.2.1 Master Operation in functional method

```
i2c_master_config_t masterConfig;
uint8_t status;
status_t result = kStatus_Success;
uint8_t txBuff[BUFFER_SIZE];

/* Gets the default configuration for master. */
I2C_MasterGetDefaultConfig(&masterConfig);

/* Initializes the I2C master. */
I2C_MasterInit(EXAMPLE_I2C_MASTER_BASEADDR, &masterConfig, I2C_MASTER_CLK);

/* Sends a start and a slave address. */
I2C_MasterStart(EXAMPLE_I2C_MASTER_BASEADDR, 7-bit slave address,
    kI2C_Write/kI2C_Read);

/* Waits for the sent out address. */
while(!((status = I2C_GetStatusFlag(EXAMPLE_I2C_MASTER_BASEADDR)) & kI2C_IntPendingFlag))
{
}

if(status & kI2C_ReceiveNakFlag)
{
    return kStatus_I2C_Nak;
}

result = I2C_MasterWriteBlocking(EXAMPLE_I2C_MASTER_BASEADDR, txBuff, BUFFER_SIZE);

if(result)
{
    /* If an error occurs, send STOP. */
}
```

```

    I2C_MasterStop(EXAMPLE_I2C_MASTER_BASEADDR, kI2CStop);
    return result;
}

while(!(I2C_GetStatusFlag(EXAMPLE_I2C_MASTER_BASEADDR) & kI2C_IntPendingFlag))
{
}

/* Wait for all data to be sent out and sends STOP. */
I2C_MasterStop(EXAMPLE_I2C_MASTER_BASEADDR, kI2CStop);

```

### 20.2.2.2 Master Operation in interrupt transactional method

```

i2c_master_handle_t g_m_handle;
volatile bool g_MasterCompletionFlag = false;
i2c_master_config_t masterConfig;
uint8_t status;
status_t result = kStatus_Success;
uint8_t txBuff[BUFFER_SIZE];
i2c_master_transfer_t masterXfer;

static void i2c_master_callback(I2C_Type *base, i2c_master_handle_t *handle, status_t status, void *
    userData)
{
    /* Signal transfer success when received success status. */
    if (status == kStatus_Success)
    {
        g_MasterCompletionFlag = true;
    }
}

/* Gets a default configuration for master. */
I2C_MasterGetDefaultConfig(&masterConfig);

/* Initializes the I2C master. */
I2C_MasterInit(EXAMPLE_I2C_MASTER_BASEADDR, &masterConfig, I2C_MASTER_CLK);

masterXfer.slaveAddress = I2C_MASTER_SLAVE_ADDR_7BIT;
masterXfer.direction = kI2C_Write;
masterXfer.subaddress = NULL;
masterXfer.subaddressSize = 0;
masterXfer.data = txBuff;
masterXfer.dataSize = BUFFER_SIZE;
masterXfer.flags = kI2C_TransferDefaultFlag;

I2C_MasterTransferCreateHandle(EXAMPLE_I2C_MASTER_BASEADDR, &g_m_handle,
    i2c_master_callback, NULL);
I2C_MasterTransferNonBlocking(EXAMPLE_I2C_MASTER_BASEADDR, &g_m_handle, &
    masterXfer);

/* Waits for a transfer to be completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;

```

### 20.2.2.3 Master Operation in DMA transactional method

```

i2c_master_dma_handle_t g_m_dma_handle;
dma_handle_t dmaHandle;
volatile bool g_MasterCompletionFlag = false;
i2c_master_config_t masterConfig;

```

## I2C Driver

```
uint8_t txBuff[BUFFER_SIZE];
i2c_master_transfer_t masterXfer;

static void i2c_master_callback(I2C_Type *base, i2c_master_dma_handle_t *handle, status_t status, void *
    userData)
{
    /* Signal transfer success when received success status. */
    if (status == kStatus_Success)
    {
        g_MasterCompletionFlag = true;
    }
}

/* Gets the default configuration for the master. */
I2C_MasterGetDefaultConfig(&masterConfig);

/* Initializes the I2C master. */
I2C_MasterInit(EXAMPLE_I2C_MASTER_BASEADDR, &masterConfig, I2C_MASTER_CLK);

masterXfer.slaveAddress = I2C_MASTER_SLAVE_ADDR_7BIT;
masterXfer.direction = kI2C_Write;
masterXfer.subaddress = NULL;
masterXfer.subaddressSize = 0;
masterXfer.data = txBuff;
masterXfer.dataSize = BUFFER_SIZE;
masterXfer.flags = kI2C_TransferDefaultFlag;

DMAMGR_RequestChannel((dma_request_source_t)DMA_REQUEST_SRC, 0, &dmaHandle);

I2C_MasterTransferCreateHandleDMA(EXAMPLE_I2C_MASTER_BASEADDR, &
    g_m_dma_handle, i2c_master_callback, NULL, &dmaHandle);
I2C_MasterTransferDMA(EXAMPLE_I2C_MASTER_BASEADDR, &g_m_dma_handle, &masterXfer);

/* Wait for transfer completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;
```

### 20.2.2.4 Slave Operation in functional method

```
i2c_slave_config_t slaveConfig;
uint8_t status;
status_t result = kStatus_Success;

I2C_SlaveGetDefaultConfig(&slaveConfig); /*A default configuration 7-bit
    addressing mode*/
slaveConfig.slaveAddr = 7-bit address
slaveConfig.addressingMode = kI2C_Address7bit/
    kI2C_RangeMatch;
I2C_SlaveInit(EXAMPLE_I2C_SLAVE_BASEADDR, &slaveConfig);

/* Waits for an address match. */
while(!((status = I2C_GetStatusFlag(EXAMPLE_I2C_SLAVE_BASEADDR)) & kI2C_AddressMatchFlag))
{
}

/* A slave transmits; master is reading from the slave. */
if (status & kI2C_TransferDirectionFlag)
{
    result = I2C_SlaveWriteBlocking(EXAMPLE_I2C_SLAVE_BASEADDR);
}
else
{
}
```

```

        I2C_SlaveReadBlocking(EXAMPLE_I2C_SLAVE_BASEADDR);
    }

    return result;

```

### 20.2.2.5 Slave Operation in interrupt transactional method

```

i2c_slave_config_t slaveConfig;
i2c_slave_handle_t g_s_handle;
volatile bool g_SlaveCompletionFlag = false;

static void i2c_slave_callback(I2C_Type *base, i2c_slave_transfer_t *xfer, void *
    userData)
{
    switch (xfer->event)
    {
        /* Transmit request */
        case kI2C_SlaveTransmitEvent:
            /* Update information for transmit process */
            xfer->data = g_slave_buff;
            xfer->dataSize = I2C_DATA_LENGTH;
            break;

        /* Receives request */
        case kI2C_SlaveReceiveEvent:
            /* Update information for received process */
            xfer->data = g_slave_buff;
            xfer->dataSize = I2C_DATA_LENGTH;
            break;

        /* Transfer is done */
        case kI2C_SlaveCompletionEvent:
            g_SlaveCompletionFlag = true;
            break;

        default:
            g_SlaveCompletionFlag = true;
            break;
    }
}

I2C_SlaveGetDefaultConfig(&slaveConfig); /*A default configuration 7-bit
    addressing mode*/
slaveConfig.slaveAddr = 7-bit address
slaveConfig.addressingMode = kI2C_Address7bit/
    kI2C_RangeMatch;

I2C_SlaveInit (EXAMPLE_I2C_SLAVE_BASEADDR, &slaveConfig);

I2C_SlaveTransferCreateHandle (EXAMPLE_I2C_SLAVE_BASEADDR, &g_s_handle,
    i2c_slave_callback, NULL);

I2C_SlaveTransferNonBlocking (EXAMPLE_I2C_SLAVE_BASEADDR, &g_s_handle,
    kI2C_SlaveCompletionEvent);

/* Waits for a transfer to be completed. */
while (!g_SlaveCompletionFlag)
{
}
g_SlaveCompletionFlag = false;

```

### Data Structures

- struct [i2c\\_master\\_config\\_t](#)  
*I2C master user configuration. [More...](#)*
- struct [i2c\\_slave\\_config\\_t](#)  
*I2C slave user configuration. [More...](#)*
- struct [i2c\\_master\\_transfer\\_t](#)  
*I2C master transfer structure. [More...](#)*
- struct [i2c\\_master\\_handle\\_t](#)  
*I2C master handle structure. [More...](#)*
- struct [i2c\\_slave\\_transfer\\_t](#)  
*I2C slave transfer structure. [More...](#)*
- struct [i2c\\_slave\\_handle\\_t](#)  
*I2C slave handle structure. [More...](#)*

### Typedefs

- typedef void(\* [i2c\\_master\\_transfer\\_callback\\_t](#) )(I2C\_Type \*base, i2c\_master\_handle\_t \*handle, status\_t status, void \*userData)  
*I2C master transfer callback typedef.*
- typedef void(\* [i2c\\_slave\\_transfer\\_callback\\_t](#) )(I2C\_Type \*base, [i2c\\_slave\\_transfer\\_t](#) \*xfer, void \*userData)  
*I2C slave transfer callback typedef.*

### Enumerations

- enum [\\_i2c\\_status](#) {  
    [kStatus\\_I2C\\_Busy](#) = MAKE\_STATUS(kStatusGroup\_I2C, 0),  
    [kStatus\\_I2C\\_Idle](#) = MAKE\_STATUS(kStatusGroup\_I2C, 1),  
    [kStatus\\_I2C\\_Nak](#) = MAKE\_STATUS(kStatusGroup\_I2C, 2),  
    [kStatus\\_I2C\\_ArbitrationLost](#) = MAKE\_STATUS(kStatusGroup\_I2C, 3),  
    [kStatus\\_I2C\\_Timeout](#) = MAKE\_STATUS(kStatusGroup\_I2C, 4),  
    [kStatus\\_I2C\\_Addr\\_Nak](#) = MAKE\_STATUS(kStatusGroup\_I2C, 5) }  
*I2C status return codes.*
- enum [\\_i2c\\_flags](#) {  
    [kI2C\\_ReceiveNakFlag](#) = I2C\_S\_RXAK\_MASK,  
    [kI2C\\_IntPendingFlag](#) = I2C\_S\_IICIF\_MASK,  
    [kI2C\\_TransferDirectionFlag](#) = I2C\_S\_SRW\_MASK,  
    [kI2C\\_RangeAddressMatchFlag](#) = I2C\_S\_RAM\_MASK,  
    [kI2C\\_ArbitrationLostFlag](#) = I2C\_S\_ARBL\_MASK,  
    [kI2C\\_BusBusyFlag](#) = I2C\_S\_BUSY\_MASK,  
    [kI2C\\_AddressMatchFlag](#) = I2C\_S\_IAAS\_MASK,  
    [kI2C\\_TransferCompleteFlag](#) = I2C\_S\_TCF\_MASK,  
    [kI2C\\_StopDetectFlag](#) = I2C\_FLT\_STOPF\_MASK << 8,  
    [kI2C\\_StartDetectFlag](#) = I2C\_FLT\_STARTF\_MASK << 8 }  
*I2C peripheral flags.*

- enum `_i2c_interrupt_enable` {  
`kI2C_GlobalInterruptEnable` = `I2C_C1_IICIE_MASK`,  
`kI2C_StartStopDetectInterruptEnable` = `I2C_FLT_SSIE_MASK` }  
*I2C feature interrupt source.*
- enum `i2c_direction_t` {  
`kI2C_Write` = `0x0U`,  
`kI2C_Read` = `0x1U` }  
*The direction of master and slave transfers.*
- enum `i2c_slave_address_mode_t` {  
`kI2C_Address7bit` = `0x0U`,  
`kI2C_RangeMatch` = `0x2U` }  
*Addressing mode.*
- enum `_i2c_master_transfer_flags` {  
`kI2C_TransferDefaultFlag` = `0x0U`,  
`kI2C_TransferNoStartFlag` = `0x1U`,  
`kI2C_TransferRepeatedStartFlag` = `0x2U`,  
`kI2C_TransferNoStopFlag` = `0x4U` }  
*I2C transfer control flag.*
- enum `i2c_slave_transfer_event_t` {  
`kI2C_SlaveAddressMatchEvent` = `0x01U`,  
`kI2C_SlaveTransmitEvent` = `0x02U`,  
`kI2C_SlaveReceiveEvent` = `0x04U`,  
`kI2C_SlaveTransmitAckEvent` = `0x08U`,  
`kI2C_SlaveStartEvent` = `0x10U`,  
`kI2C_SlaveCompletionEvent` = `0x20U`,  
`kI2C_SlaveGeneralCallEvent` = `0x40U`,  
`kI2C_SlaveAllEvents` }  
*Set of events sent to the callback for nonblocking slave transfers.*

## Driver version

- #define `FSL_I2C_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 2)`)  
*I2C driver version 2.0.2.*

## Initialization and deinitialization

- void `I2C_MasterInit` (`I2C_Type *base`, const `i2c_master_config_t *masterConfig`, `uint32_t srcClock_Hz`)  
*Initializes the I2C peripheral.*
- void `I2C_SlaveInit` (`I2C_Type *base`, const `i2c_slave_config_t *slaveConfig`, `uint32_t srcClock_Hz`)  
*Initializes the I2C peripheral.*
- void `I2C_MasterDeinit` (`I2C_Type *base`)  
*De-initializes the I2C master peripheral.*
- void `I2C_SlaveDeinit` (`I2C_Type *base`)

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- *De-initializes the I2C slave peripheral.*
- void [I2C\\_MasterGetDefaultConfig](#) (i2c\_master\_config\_t \*masterConfig)  
*Sets the I2C master configuration structure to default values.*
- void [I2C\\_SlaveGetDefaultConfig](#) (i2c\_slave\_config\_t \*slaveConfig)  
*Sets the I2C slave configuration structure to default values.*
- static void [I2C\\_Enable](#) (I2C\_Type \*base, bool enable)  
*Enables or disables the I2C peripheral operation.*

## Status

- uint32\_t [I2C\\_MasterGetStatusFlags](#) (I2C\_Type \*base)  
*Gets the I2C status flags.*
- static uint32\_t [I2C\\_SlaveGetStatusFlags](#) (I2C\_Type \*base)  
*Gets the I2C status flags.*
- static void [I2C\\_MasterClearStatusFlags](#) (I2C\_Type \*base, uint32\_t statusMask)  
*Clears the I2C status flag state.*
- static void [I2C\\_SlaveClearStatusFlags](#) (I2C\_Type \*base, uint32\_t statusMask)  
*Clears the I2C status flag state.*

## Interrupts

- void [I2C\\_EnableInterrupts](#) (I2C\_Type \*base, uint32\_t mask)  
*Enables I2C interrupt requests.*
- void [I2C\\_DisableInterrupts](#) (I2C\_Type \*base, uint32\_t mask)  
*Disables I2C interrupt requests.*

## DMA Control

- static void [I2C\\_EnableDMA](#) (I2C\_Type \*base, bool enable)  
*Enables/disables the I2C DMA interrupt.*
- static uint32\_t [I2C\\_GetDataRegAddr](#) (I2C\_Type \*base)  
*Gets the I2C tx/rx data register address.*

## Bus Operations

- void [I2C\\_MasterSetBaudRate](#) (I2C\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Sets the I2C master transfer baud rate.*
- status\_t [I2C\\_MasterStart](#) (I2C\_Type \*base, uint8\_t address, i2c\_direction\_t direction)  
*Sends a START on the I2C bus.*
- status\_t [I2C\\_MasterStop](#) (I2C\_Type \*base)  
*Sends a STOP signal on the I2C bus.*
- status\_t [I2C\\_MasterRepeatedStart](#) (I2C\_Type \*base, uint8\_t address, i2c\_direction\_t direction)  
*Sends a REPEATED START on the I2C bus.*
- status\_t [I2C\\_MasterWriteBlocking](#) (I2C\_Type \*base, const uint8\_t \*txBuff, size\_t txSize, uint32\_t flags)  
*Performs a polling send transaction on the I2C bus.*



- status\_t [I2C\\_MasterReadBlocking](#) (I2C\_Type \*base, uint8\_t \*rxBuff, size\_t rxSize, uint32\_t flags)  
*Performs a polling receive transaction on the I2C bus.*
- status\_t [I2C\\_SlaveWriteBlocking](#) (I2C\_Type \*base, const uint8\_t \*txBuff, size\_t txSize)  
*Performs a polling send transaction on the I2C bus.*
- void [I2C\\_SlaveReadBlocking](#) (I2C\_Type \*base, uint8\_t \*rxBuff, size\_t rxSize)  
*Performs a polling receive transaction on the I2C bus.*
- status\_t [I2C\\_MasterTransferBlocking](#) (I2C\_Type \*base, [i2c\\_master\\_transfer\\_t](#) \*xfer)  
*Performs a master polling transfer on the I2C bus.*

## Transactional

- void [I2C\\_MasterTransferCreateHandle](#) (I2C\_Type \*base, i2c\_master\_handle\_t \*handle, [i2c\\_master\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the I2C handle which is used in transactional functions.*
- status\_t [I2C\\_MasterTransferNonBlocking](#) (I2C\_Type \*base, i2c\_master\_handle\_t \*handle, [i2c\\_master\\_transfer\\_t](#) \*xfer)  
*Performs a master interrupt non-blocking transfer on the I2C bus.*
- status\_t [I2C\\_MasterTransferGetCount](#) (I2C\_Type \*base, i2c\_master\_handle\_t \*handle, size\_t \*count)  
*Gets the master transfer status during a interrupt non-blocking transfer.*
- void [I2C\\_MasterTransferAbort](#) (I2C\_Type \*base, i2c\_master\_handle\_t \*handle)  
*Aborts an interrupt non-blocking transfer early.*
- void [I2C\\_MasterTransferHandleIRQ](#) (I2C\_Type \*base, void \*i2cHandle)  
*Master interrupt handler.*
- void [I2C\\_SlaveTransferCreateHandle](#) (I2C\_Type \*base, i2c\_slave\_handle\_t \*handle, [i2c\\_slave\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the I2C handle which is used in transactional functions.*
- status\_t [I2C\\_SlaveTransferNonBlocking](#) (I2C\_Type \*base, i2c\_slave\_handle\_t \*handle, uint32\_t eventMask)  
*Starts accepting slave transfers.*
- void [I2C\\_SlaveTransferAbort](#) (I2C\_Type \*base, i2c\_slave\_handle\_t \*handle)  
*Aborts the slave transfer.*
- status\_t [I2C\\_SlaveTransferGetCount](#) (I2C\_Type \*base, i2c\_slave\_handle\_t \*handle, size\_t \*count)  
*Gets the slave transfer remaining bytes during a interrupt non-blocking transfer.*
- void [I2C\\_SlaveTransferHandleIRQ](#) (I2C\_Type \*base, void \*i2cHandle)  
*Slave interrupt handler.*

## 20.2.3 Data Structure Documentation

### 20.2.3.1 struct i2c\_master\_config\_t

#### Data Fields

- bool [enableMaster](#)  
*Enables the I2C peripheral at initialization time.*
- bool [enableHighDrive](#)  
*Controls the drive capability of the I2C pads.*

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- bool [enableStopHold](#)  
*Controls the stop hold enable.*
- uint32\_t [baudRate\\_Bps](#)  
*Baud rate configuration of I2C peripheral.*
- uint8\_t [glitchFilterWidth](#)  
*Controls the width of the glitch.*

### 20.2.3.1.0.57 Field Documentation

20.2.3.1.0.57.1 bool i2c\_master\_config\_t::enableMaster

20.2.3.1.0.57.2 bool i2c\_master\_config\_t::enableHighDrive

20.2.3.1.0.57.3 bool i2c\_master\_config\_t::enableStopHold

20.2.3.1.0.57.4 uint32\_t i2c\_master\_config\_t::baudRate\_Bps

20.2.3.1.0.57.5 uint8\_t i2c\_master\_config\_t::glitchFilterWidth

### 20.2.3.2 struct i2c\_slave\_config\_t

#### Data Fields

- bool [enableSlave](#)  
*Enables the I2C peripheral at initialization time.*
- bool [enableGeneralCall](#)  
*Enables the general call addressing mode.*
- bool [enableWakeUp](#)  
*Enables/disables waking up MCU from low-power mode.*
- bool [enableHighDrive](#)  
*Controls the drive capability of the I2C pads.*
- bool [enableBaudRateCtl](#)  
*Enables/disables independent slave baud rate on SCL in very fast I2C modes.*
- uint16\_t [slaveAddress](#)  
*A slave address configuration.*
- uint16\_t [upperAddress](#)  
*A maximum boundary slave address used in a range matching mode.*
- [i2c\\_slave\\_address\\_mode\\_t](#) [addressingMode](#)  
*An addressing mode configuration of i2c\_slave\_address\_mode\_config\_t.*
- uint32\_t [sclStopHoldTime\\_ns](#)  
*the delay from the rising edge of SCL (I2C clock) to the rising edge of SDA (I2C data) while SCL is high (stop condition), SDA hold time and SCL start hold time are also configured according to the SCL stop hold time.*

**20.2.3.2.0.58 Field Documentation**

- 20.2.3.2.0.58.1** `bool i2c_slave_config_t::enableSlave`
- 20.2.3.2.0.58.2** `bool i2c_slave_config_t::enableGeneralCall`
- 20.2.3.2.0.58.3** `bool i2c_slave_config_t::enableWakeUp`
- 20.2.3.2.0.58.4** `bool i2c_slave_config_t::enableHighDrive`
- 20.2.3.2.0.58.5** `bool i2c_slave_config_t::enableBaudRateCtl`
- 20.2.3.2.0.58.6** `uint16_t i2c_slave_config_t::slaveAddress`
- 20.2.3.2.0.58.7** `uint16_t i2c_slave_config_t::upperAddress`
- 20.2.3.2.0.58.8** `i2c_slave_address_mode_t i2c_slave_config_t::addressingMode`
- 20.2.3.2.0.58.9** `uint32_t i2c_slave_config_t::sclStopHoldTime_ns`

**20.2.3.3 struct i2c\_master\_transfer\_t****Data Fields**

- `uint32_t flags`  
*A transfer flag which controls the transfer.*
- `uint8_t slaveAddress`  
*7-bit slave address.*
- `i2c_direction_t direction`  
*A transfer direction, read or write.*
- `uint32_t subaddress`  
*A sub address.*
- `uint8_t subaddressSize`  
*A size of the command buffer.*
- `uint8_t *volatile data`  
*A transfer buffer.*
- `volatile size_t dataSize`  
*A transfer size.*

**20.2.3.3.0.59 Field Documentation**

- 20.2.3.3.0.59.1** `uint32_t i2c_master_transfer_t::flags`
- 20.2.3.3.0.59.2** `uint8_t i2c_master_transfer_t::slaveAddress`
- 20.2.3.3.0.59.3** `i2c_direction_t i2c_master_transfer_t::direction`
- 20.2.3.3.0.59.4** `uint32_t i2c_master_transfer_t::subaddress`

Transferred MSB first.

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20.2.3.3.0.59.5 `uint8_t i2c_master_transfer_t::subaddressSize`

20.2.3.3.0.59.6 `uint8_t* volatile i2c_master_transfer_t::data`

20.2.3.3.0.59.7 `volatile size_t i2c_master_transfer_t::dataSize`

### 20.2.3.4 `struct i2c_master_handle`

I2C master handle typedef.

#### Data Fields

- [i2c\\_master\\_transfer\\_t transfer](#)  
*I2C master transfer copy.*
- `size_t` [transferSize](#)  
*Total bytes to be transferred.*
- `uint8_t` [state](#)  
*A transfer state maintained during transfer.*
- [i2c\\_master\\_transfer\\_callback\\_t completionCallback](#)  
*A callback function called when the transfer is finished.*
- `void *` [userData](#)  
*A callback parameter passed to the callback function.*

#### 20.2.3.4.0.60 Field Documentation

20.2.3.4.0.60.1 `i2c_master_transfer_t i2c_master_handle_t::transfer`

20.2.3.4.0.60.2 `size_t i2c_master_handle_t::transferSize`

20.2.3.4.0.60.3 `uint8_t i2c_master_handle_t::state`

20.2.3.4.0.60.4 `i2c_master_transfer_callback_t i2c_master_handle_t::completionCallback`

20.2.3.4.0.60.5 `void* i2c_master_handle_t::userData`

### 20.2.3.5 `struct i2c_slave_transfer_t`

#### Data Fields

- [i2c\\_slave\\_transfer\\_event\\_t event](#)  
*A reason that the callback is invoked.*
- `uint8_t *volatile` [data](#)  
*A transfer buffer.*
- `volatile size_t` [dataSize](#)  
*A transfer size.*
- `status_t` [completionStatus](#)  
*Success or error code describing how the transfer completed.*
- `size_t` [transferredCount](#)  
*A number of bytes actually transferred since the start or since the last repeated start.*

**20.2.3.5.0.61 Field Documentation****20.2.3.5.0.61.1** `i2c_slave_transfer_event_t i2c_slave_transfer_t::event`**20.2.3.5.0.61.2** `uint8_t* volatile i2c_slave_transfer_t::data`**20.2.3.5.0.61.3** `volatile size_t i2c_slave_transfer_t::dataSize`**20.2.3.5.0.61.4** `status_t i2c_slave_transfer_t::completionStatus`

Only applies for [kI2C\\_SlaveCompletionEvent](#).

**20.2.3.5.0.61.5** `size_t i2c_slave_transfer_t::transferredCount`**20.2.3.6 struct \_i2c\_slave\_handle**

I2C slave handle typedef.

**Data Fields**

- volatile bool [isBusy](#)  
*Indicates whether a transfer is busy.*
- [i2c\\_slave\\_transfer\\_t transfer](#)  
*I2C slave transfer copy.*
- uint32\_t [eventMask](#)  
*A mask of enabled events.*
- [i2c\\_slave\\_transfer\\_callback\\_t callback](#)  
*A callback function called at the transfer event.*
- void \* [userData](#)  
*A callback parameter passed to the callback.*

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### 20.2.3.6.0.62 Field Documentation

20.2.3.6.0.62.1 `volatile bool i2c_slave_handle_t::isBusy`

20.2.3.6.0.62.2 `i2c_slave_transfer_t i2c_slave_handle_t::transfer`

20.2.3.6.0.62.3 `uint32_t i2c_slave_handle_t::eventMask`

20.2.3.6.0.62.4 `i2c_slave_transfer_callback_t i2c_slave_handle_t::callback`

20.2.3.6.0.62.5 `void* i2c_slave_handle_t::userData`

### 20.2.4 Macro Definition Documentation

20.2.4.1 `#define FSL_I2C_DRIVER_VERSION (MAKE_VERSION(2, 0, 2))`

### 20.2.5 Typedef Documentation

20.2.5.1 `typedef void(* i2c_master_transfer_callback_t)(I2C_Type *base, i2c_master_handle_t *handle, status_t status, void *userData)`

20.2.5.2 `typedef void(* i2c_slave_transfer_callback_t)(I2C_Type *base, i2c_slave_transfer_t *xfer, void *userData)`

### 20.2.6 Enumeration Type Documentation

#### 20.2.6.1 `enum _i2c_status`

Enumerator

*kStatus\_I2C\_Busy* I2C is busy with current transfer.

*kStatus\_I2C\_Idle* Bus is Idle.

*kStatus\_I2C\_Nak* NAK received during transfer.

*kStatus\_I2C\_ArbitrationLost* Arbitration lost during transfer.

*kStatus\_I2C\_Timeout* Wait event timeout.

*kStatus\_I2C\_Addr\_Nak* NAK received during the address probe.

#### 20.2.6.2 `enum _i2c_flags`

The following status register flags can be cleared:

- [kI2C\\_ArbitrationLostFlag](#)
- [kI2C\\_IntPendingFlag](#)
- [kI2C\\_StartDetectFlag](#)
- [kI2C\\_StopDetectFlag](#)

## Note

These enumerations are meant to be OR'd together to form a bit mask.

## Enumerator

***kI2C\_ReceiveNakFlag*** I2C receive NAK flag.  
***kI2C\_IntPendingFlag*** I2C interrupt pending flag.  
***kI2C\_TransferDirectionFlag*** I2C transfer direction flag.  
***kI2C\_RangeAddressMatchFlag*** I2C range address match flag.  
***kI2C\_ArbitrationLostFlag*** I2C arbitration lost flag.  
***kI2C\_BusBusyFlag*** I2C bus busy flag.  
***kI2C\_AddressMatchFlag*** I2C address match flag.  
***kI2C\_TransferCompleteFlag*** I2C transfer complete flag.  
***kI2C\_StopDetectFlag*** I2C stop detect flag.  
***kI2C\_StartDetectFlag*** I2C start detect flag.

**20.2.6.3 enum \_i2c\_interrupt\_enable**

## Enumerator

***kI2C\_GlobalInterruptEnable*** I2C global interrupt.  
***kI2C\_StartStopDetectInterruptEnable*** I2C start&stop detect interrupt.

**20.2.6.4 enum i2c\_direction\_t**

## Enumerator

***kI2C\_Write*** Master transmits to the slave.  
***kI2C\_Read*** Master receives from the slave.

**20.2.6.5 enum i2c\_slave\_address\_mode\_t**

## Enumerator

***kI2C\_Address7bit*** 7-bit addressing mode.  
***kI2C\_RangeMatch*** Range address match addressing mode.

**20.2.6.6 enum \_i2c\_master\_transfer\_flags**

## Enumerator

***kI2C\_TransferDefaultFlag*** A transfer starts with a start signal, stops with a stop signal.

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***kI2C\_TransferNoStartFlag*** A transfer starts without a start signal.

***kI2C\_TransferRepeatedStartFlag*** A transfer starts with a repeated start signal.

***kI2C\_TransferNoStopFlag*** A transfer ends without a stop signal.

### 20.2.6.7 enum i2c\_slave\_transfer\_event\_t

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to [I2C\\_SlaveTransferNonBlocking\(\)](#) to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

#### Note

These enumerations are meant to be OR'd together to form a bit mask of events.

#### Enumerator

***kI2C\_SlaveAddressMatchEvent*** Received the slave address after a start or repeated start.

***kI2C\_SlaveTransmitEvent*** A callback is requested to provide data to transmit (slave-transmitter role).

***kI2C\_SlaveReceiveEvent*** A callback is requested to provide a buffer in which to place received data (slave-receiver role).

***kI2C\_SlaveTransmitAckEvent*** A callback needs to either transmit an ACK or NACK.

***kI2C\_SlaveStartEvent*** A start/repeated start was detected.

***kI2C\_SlaveCompletionEvent*** A stop was detected or finished transfer, completing the transfer.

***kI2C\_SlaveGeneralCallEvent*** Received the general call address after a start or repeated start.

***kI2C\_SlaveAllEvents*** A bit mask of all available events.

## 20.2.7 Function Documentation

### 20.2.7.1 void I2C\_MasterInit ( I2C\_Type \* *base*, const i2c\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

Call this API to ungate the I2C clock and configure the I2C with master configuration.

#### Note

This API should be called at the beginning of the application. Otherwise, any operation to the I2C module can cause a hard fault because the clock is not enabled. The configuration structure can be custom filled or it can be set with default values by using the [I2C\\_MasterGetDefaultConfig\(\)](#). After calling this API, the master is ready to transfer. This is an example.

```
* i2c_master_config_t config = {  
* .enableMaster = true,  
* .enableStopHold = false,  
* .highDrive = false,  
* .baudRate_Bps = 100000,  
}
```



```

* .glitchFilterWidth = 0
* };
* I2C_MasterInit(I2C0, &config, 12000000U);
*

```

## Parameters

|                     |                                                 |
|---------------------|-------------------------------------------------|
| <i>base</i>         | I2C base pointer                                |
| <i>masterConfig</i> | A pointer to the master configuration structure |
| <i>srcClock_Hz</i>  | I2C peripheral clock frequency in Hz            |

### 20.2.7.2 void I2C\_SlaveInit ( I2C\_Type \* *base*, const i2c\_slave\_config\_t \* *slaveConfig*, uint32\_t *srcClock\_Hz* )

Call this API to ungate the I2C clock and initialize the I2C with the slave configuration.

## Note

This API should be called at the beginning of the application. Otherwise, any operation to the I2C module can cause a hard fault because the clock is not enabled. The configuration structure can partly be set with default values by [I2C\\_SlaveGetDefaultConfig\(\)](#) or it can be custom filled by the user. This is an example.

```

* i2c_slave_config_t config = {
* .enableSlave = true,
* .enableGeneralCall = false,
* .addressingMode = kI2C_Address7bit,
* .slaveAddress = 0x1DU,
* .enableWakeUp = false,
* .enablehighDrive = false,
* .enableBaudRateCtl = false,
* .sclStopHoldTime_ns = 4000
* };
* I2C_SlaveInit(I2C0, &config, 12000000U);
*

```

## Parameters

|                    |                                                |
|--------------------|------------------------------------------------|
| <i>base</i>        | I2C base pointer                               |
| <i>slaveConfig</i> | A pointer to the slave configuration structure |
| <i>srcClock_Hz</i> | I2C peripheral clock frequency in Hz           |

### 20.2.7.3 void I2C\_MasterDeinit ( I2C\_Type \* *base* )

Call this API to gate the I2C clock. The I2C master module can't work unless the I2C\_MasterInit is called.

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### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

#### 20.2.7.4 void I2C\_SlaveDeinit ( I2C\_Type \* *base* )

Calling this API gates the I2C clock. The I2C slave module can't work unless the I2C\_SlaveInit is called to enable the clock.

### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

#### 20.2.7.5 void I2C\_MasterGetDefaultConfig ( i2c\_master\_config\_t \* *masterConfig* )

The purpose of this API is to get the configuration structure initialized for use in the I2C\_MasterConfigure(). Use the initialized structure unchanged in the I2C\_MasterConfigure() or modify the structure before calling the I2C\_MasterConfigure(). This is an example.

```
* i2c_master_config_t config;  
* I2C_MasterGetDefaultConfig(&config);  
*
```

### Parameters

|                     |                                                  |
|---------------------|--------------------------------------------------|
| <i>masterConfig</i> | A pointer to the master configuration structure. |
|---------------------|--------------------------------------------------|

#### 20.2.7.6 void I2C\_SlaveGetDefaultConfig ( i2c\_slave\_config\_t \* *slaveConfig* )

The purpose of this API is to get the configuration structure initialized for use in the I2C\_SlaveConfigure(). Modify fields of the structure before calling the I2C\_SlaveConfigure(). This is an example.

```
* i2c_slave_config_t config;  
* I2C_SlaveGetDefaultConfig(&config);  
*
```

### Parameters

|                    |                                                 |
|--------------------|-------------------------------------------------|
| <i>slaveConfig</i> | A pointer to the slave configuration structure. |
|--------------------|-------------------------------------------------|

#### 20.2.7.7 static void I2C\_Enable ( I2C\_Type \* *base*, bool *enable* ) [inline], [static]

## Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>base</i>   | I2C base pointer                                     |
| <i>enable</i> | Pass true to enable and false to disable the module. |

**20.2.7.8 uint32\_t I2C\_MasterGetStatusFlags ( I2C\_Type \* *base* )**

## Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

## Returns

status flag, use status flag to AND [\\_i2c\\_flags](#) to get the related status.

**20.2.7.9 static uint32\_t I2C\_SlaveGetStatusFlags ( I2C\_Type \* *base* ) [inline], [static]**

## Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

## Returns

status flag, use status flag to AND [\\_i2c\\_flags](#) to get the related status.

**20.2.7.10 static void I2C\_MasterClearStatusFlags ( I2C\_Type \* *base*, uint32\_t *statusMask* ) [inline], [static]**

The following status register flags can be cleared kI2C\_ArbitrationLostFlag and kI2C\_IntPendingFlag.

## Parameters

|                   |                                                                                                                                                                                                                                                                                                                                                   |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | I2C base pointer                                                                                                                                                                                                                                                                                                                                  |
| <i>statusMask</i> | The status flag mask, defined in type <code>i2c_status_flag_t</code> . The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• kI2C_StartDetectFlag (if available)</li> <li>• kI2C_StopDetectFlag (if available)</li> <li>• kI2C_ArbitrationLostFlag</li> <li>• kI2C_IntPendingFlagFlag</li> </ul> |

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**20.2.7.11** `static void I2C_SlaveClearStatusFlags ( I2C_Type * base, uint32_t statusMask  
 ) [inline], [static]`

The following status register flags can be cleared kI2C\_ArbitrationLostFlag and kI2C\_IntPendingFlag

## Parameters

|                   |                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | I2C base pointer                                                                                                                                                                                                                                                                                                                                                                                      |
| <i>statusMask</i> | The status flag mask, defined in type <code>i2c_status_flag_t</code> . The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• <code>kI2C_StartDetectFlag</code> (if available)</li> <li>• <code>kI2C_StopDetectFlag</code> (if available)</li> <li>• <code>kI2C_ArbitrationLostFlag</code></li> <li>• <code>kI2C_IntPendingFlagFlag</code></li> </ul> |

**20.2.7.12 void I2C\_EnableInterrupts ( I2C\_Type \* *base*, uint32\_t *mask* )**

## Parameters

|             |                                                                                                                                                                                                                                                                                                                                 |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | I2C base pointer                                                                                                                                                                                                                                                                                                                |
| <i>mask</i> | interrupt source The parameter can be combination of the following source if defined: <ul style="list-style-type: none"> <li>• <code>kI2C_GlobalInterruptEnable</code></li> <li>• <code>kI2C_StopDetectInterruptEnable/kI2C_StartDetectInterruptEnable</code></li> <li>• <code>kI2C_SdaTimeoutInterruptEnable</code></li> </ul> |

**20.2.7.13 void I2C\_DisableInterrupts ( I2C\_Type \* *base*, uint32\_t *mask* )**

## Parameters

|             |                                                                                                                                                                                                                                                                                                                                 |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | I2C base pointer                                                                                                                                                                                                                                                                                                                |
| <i>mask</i> | interrupt source The parameter can be combination of the following source if defined: <ul style="list-style-type: none"> <li>• <code>kI2C_GlobalInterruptEnable</code></li> <li>• <code>kI2C_StopDetectInterruptEnable/kI2C_StartDetectInterruptEnable</code></li> <li>• <code>kI2C_SdaTimeoutInterruptEnable</code></li> </ul> |

**20.2.7.14 static void I2C\_EnableDMA ( I2C\_Type \* *base*, bool *enable* ) [inline], [static]**

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### Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | I2C base pointer                 |
| <i>enable</i> | true to enable, false to disable |

#### 20.2.7.15 **static uint32\_t I2C\_GetDataRegAddr ( I2C\_Type \* *base* ) [inline], [static]**

This API is used to provide a transfer address for I2C DMA transfer configuration.

### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

### Returns

data register address

#### 20.2.7.16 **void I2C\_MasterSetBaudRate ( I2C\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClock\_Hz* )**

### Parameters

|                     |                            |
|---------------------|----------------------------|
| <i>base</i>         | I2C base pointer           |
| <i>baudRate_Bps</i> | the baud rate value in bps |
| <i>srcClock_Hz</i>  | Source clock               |

#### 20.2.7.17 **status\_t I2C\_MasterStart ( I2C\_Type \* *base*, uint8\_t *address*, i2c\_direction\_t *direction* )**

This function is used to initiate a new master mode transfer by sending the START signal. The slave address is sent following the I2C START signal.

### Parameters

|                  |                                               |
|------------------|-----------------------------------------------|
| <i>base</i>      | I2C peripheral base pointer                   |
| <i>address</i>   | 7-bit slave device address.                   |
| <i>direction</i> | Master transfer directions(transmit/receive). |

Return values

|                         |                                     |
|-------------------------|-------------------------------------|
| <i>kStatus_Success</i>  | Successfully send the start signal. |
| <i>kStatus_I2C_Busy</i> | Current bus is busy.                |

#### 20.2.7.18 **status\_t I2C\_MasterStop ( I2C\_Type \* *base* )**

Return values

|                            |                                    |
|----------------------------|------------------------------------|
| <i>kStatus_Success</i>     | Successfully send the stop signal. |
| <i>kStatus_I2C_Timeout</i> | Send stop signal failed, timeout.  |

#### 20.2.7.19 **status\_t I2C\_MasterRepeatedStart ( I2C\_Type \* *base*, uint8\_t *address*, i2c\_direction\_t *direction* )**

Parameters

|                  |                                               |
|------------------|-----------------------------------------------|
| <i>base</i>      | I2C peripheral base pointer                   |
| <i>address</i>   | 7-bit slave device address.                   |
| <i>direction</i> | Master transfer directions(transmit/receive). |

Return values

|                         |                                                             |
|-------------------------|-------------------------------------------------------------|
| <i>kStatus_Success</i>  | Successfully send the start signal.                         |
| <i>kStatus_I2C_Busy</i> | Current bus is busy but not occupied by current I2C master. |

#### 20.2.7.20 **status\_t I2C\_MasterWriteBlocking ( I2C\_Type \* *base*, const uint8\_t \* *txBuff*, size\_t *txSize*, uint32\_t *flags* )**

Parameters

|               |                                                                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | The I2C peripheral base pointer.                                                                                                                      |
| <i>txBuff</i> | The pointer to the data to be transferred.                                                                                                            |
| <i>txSize</i> | The length in bytes of the data to be transferred.                                                                                                    |
| <i>flags</i>  | Transfer control flag to decide whether need to send a stop, use kI2C_TransferDefaultFlag to issue a stop and kI2C_TransferNoStop to not send a stop. |

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### Return values

|                                     |                                              |
|-------------------------------------|----------------------------------------------|
| <i>kStatus_Success</i>              | Successfully complete the data transmission. |
| <i>kStatus_I2C_Arbitration-Lost</i> | Transfer error, arbitration lost.            |
| <i>kStatus_I2C_Nak</i>              | Transfer error, receive NAK during transfer. |

### 20.2.7.21 **status\_t I2C\_MasterReadBlocking ( I2C\_Type \* *base*, uint8\_t \* *rxBuff*, size\_t *rxSize*, uint32\_t *flags* )**

#### Note

The I2C\_MasterReadBlocking function stops the bus before reading the final byte. Without stopping the bus prior for the final read, the bus issues another read, resulting in garbage data being read into the data register.

#### Parameters

|               |                                                                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base pointer.                                                                                                                          |
| <i>rxBuff</i> | The pointer to the data to store the received data.                                                                                                   |
| <i>rxSize</i> | The length in bytes of the data to be received.                                                                                                       |
| <i>flags</i>  | Transfer control flag to decide whether need to send a stop, use kI2C_TransferDefaultFlag to issue a stop and kI2C_TransferNoStop to not send a stop. |

### Return values

|                            |                                              |
|----------------------------|----------------------------------------------|
| <i>kStatus_Success</i>     | Successfully complete the data transmission. |
| <i>kStatus_I2C_Timeout</i> | Send stop signal failed, timeout.            |

### 20.2.7.22 **status\_t I2C\_SlaveWriteBlocking ( I2C\_Type \* *base*, const uint8\_t \* *txBuff*, size\_t *txSize* )**

#### Parameters

|               |                                                    |
|---------------|----------------------------------------------------|
| <i>base</i>   | The I2C peripheral base pointer.                   |
| <i>txBuff</i> | The pointer to the data to be transferred.         |
| <i>txSize</i> | The length in bytes of the data to be transferred. |



## Return values

|                                     |                                              |
|-------------------------------------|----------------------------------------------|
| <i>kStatus_Success</i>              | Successfully complete the data transmission. |
| <i>kStatus_I2C_Arbitration-Lost</i> | Transfer error, arbitration lost.            |
| <i>kStatus_I2C_Nak</i>              | Transfer error, receive NAK during transfer. |

### 20.2.7.23 void I2C\_SlaveReadBlocking ( I2C\_Type \* *base*, uint8\_t \* *rxBuff*, size\_t *rxSize* )

## Parameters

|               |                                                     |
|---------------|-----------------------------------------------------|
| <i>base</i>   | I2C peripheral base pointer.                        |
| <i>rxBuff</i> | The pointer to the data to store the received data. |
| <i>rxSize</i> | The length in bytes of the data to be received.     |

### 20.2.7.24 status\_t I2C\_MasterTransferBlocking ( I2C\_Type \* *base*, i2c\_master\_transfer\_t \* *xfer* )

## Note

The API does not return until the transfer succeeds or fails due to arbitration lost or receiving a NAK.

## Parameters

|             |                                    |
|-------------|------------------------------------|
| <i>base</i> | I2C peripheral base address.       |
| <i>xfer</i> | Pointer to the transfer structure. |

## Return values

|                                     |                                              |
|-------------------------------------|----------------------------------------------|
| <i>kStatus_Success</i>              | Successfully complete the data transmission. |
| <i>kStatus_I2C_Busy</i>             | Previous transmission still not finished.    |
| <i>kStatus_I2C_Timeout</i>          | Transfer error, wait signal timeout.         |
| <i>kStatus_I2C_Arbitration-Lost</i> | Transfer error, arbitration lost.            |
| <i>kStatus_I2C_Nak</i>              | Transfer error, receive NAK during transfer. |

**20.2.7.25** void I2C\_MasterTransferCreateHandle ( I2C\_Type \* *base*, i2c\_master\_handle\_t \* *handle*, i2c\_master\_transfer\_callback\_t *callback*, void \* *userData* )

## Parameters

|                 |                                                                       |
|-----------------|-----------------------------------------------------------------------|
| <i>base</i>     | I2C base pointer.                                                     |
| <i>handle</i>   | pointer to i2c_master_handle_t structure to store the transfer state. |
| <i>callback</i> | pointer to user callback function.                                    |
| <i>userData</i> | user parameter passed to the callback function.                       |

#### 20.2.7.26 status\_t I2C\_MasterTransferNonBlocking ( I2C\_Type \* *base*, i2c\_master\_handle\_t \* *handle*, i2c\_master\_transfer\_t \* *xfer* )

## Note

Calling the API returns immediately after transfer initiates. The user needs to call I2C\_MasterGetTransferCount to poll the transfer status to check whether the transfer is finished. If the return status is not kStatus\_I2C\_Busy, the transfer is finished.

## Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                         |
| <i>handle</i> | pointer to i2c_master_handle_t structure which stores the transfer state. |
| <i>xfer</i>   | pointer to <a href="#">i2c_master_transfer_t</a> structure.               |

## Return values

|                            |                                           |
|----------------------------|-------------------------------------------|
| <i>kStatus_Success</i>     | Successfully start the data transmission. |
| <i>kStatus_I2C_Busy</i>    | Previous transmission still not finished. |
| <i>kStatus_I2C_Timeout</i> | Transfer error, wait signal timeout.      |

#### 20.2.7.27 status\_t I2C\_MasterTransferGetCount ( I2C\_Type \* *base*, i2c\_master\_handle\_t \* *handle*, size\_t \* *count* )

## Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                         |
| <i>handle</i> | pointer to i2c_master_handle_t structure which stores the transfer state. |
| <i>count</i>  | Number of bytes transferred so far by the non-blocking transaction.       |

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Return values

|                                |                                |
|--------------------------------|--------------------------------|
| <i>kStatus_InvalidArgument</i> | count is Invalid.              |
| <i>kStatus_Success</i>         | Successfully return the count. |

### 20.2.7.28 void I2C\_MasterTransferAbort ( I2C\_Type \* *base*, i2c\_master\_handle\_t \* *handle* )

Note

This API can be called at any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

|               |                                                                          |
|---------------|--------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                        |
| <i>handle</i> | pointer to i2c_master_handle_t structure which stores the transfer state |

### 20.2.7.29 void I2C\_MasterTransferHandleIRQ ( I2C\_Type \* *base*, void \* *i2cHandle* )

Parameters

|                  |                                           |
|------------------|-------------------------------------------|
| <i>base</i>      | I2C base pointer.                         |
| <i>i2cHandle</i> | pointer to i2c_master_handle_t structure. |

### 20.2.7.30 void I2C\_SlaveTransferCreateHandle ( I2C\_Type \* *base*, i2c\_slave\_handle\_t \* *handle*, i2c\_slave\_transfer\_callback\_t *callback*, void \* *userData* )

Parameters

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <i>base</i>     | I2C base pointer.                                                    |
| <i>handle</i>   | pointer to i2c_slave_handle_t structure to store the transfer state. |
| <i>callback</i> | pointer to user callback function.                                   |
| <i>userData</i> | user parameter passed to the callback function.                      |

### 20.2.7.31 **status\_t I2C\_SlaveTransferNonBlocking ( I2C\_Type \* *base*, i2c\_slave\_handle\_t \* *handle*, uint32\_t *eventMask* )**

Call this API after calling the [I2C\\_SlaveInit\(\)](#) and [I2C\\_SlaveTransferCreateHandle\(\)](#) to start processing transactions driven by an I2C master. The slave monitors the I2C bus and passes events to the callback that was passed into the call to [I2C\\_SlaveTransferCreateHandle\(\)](#). The callback is always invoked from the interrupt context.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of [i2c\\_slave\\_transfer\\_event\\_t](#) enumerators for the events you wish to receive. The [kI2C\\_SlaveTransmitEvent](#) and [#kLPI2C\\_SlaveReceiveEvent](#) events are always enabled and do not need to be included in the mask. Alternatively, pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the [kI2C\\_SlaveAllEvents](#) constant is provided as a convenient way to enable all events.

Parameters

|                  |                                                                                                                                                                                                                                                                                                    |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>      | The I2C peripheral base address.                                                                                                                                                                                                                                                                   |
| <i>handle</i>    | Pointer to <a href="#">#i2c_slave_handle_t</a> structure which stores the transfer state.                                                                                                                                                                                                          |
| <i>eventMask</i> | Bit mask formed by OR'ing together <a href="#">i2c_slave_transfer_event_t</a> enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and <a href="#">kI2C_SlaveAllEvents</a> to enable all events. |

Return values

|                                  |                                                           |
|----------------------------------|-----------------------------------------------------------|
| <a href="#">#kStatus_Success</a> | Slave transfers were successfully started.                |
| <a href="#">kStatus_I2C_Busy</a> | Slave transfers have already been started on this handle. |

### 20.2.7.32 **void I2C\_SlaveTransferAbort ( I2C\_Type \* *base*, i2c\_slave\_handle\_t \* *handle* )**

Note

This API can be called at any time to stop slave for handling the bus events.

Parameters

|               |                                                                                          |
|---------------|------------------------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                                        |
| <i>handle</i> | pointer to <a href="#">i2c_slave_handle_t</a> structure which stores the transfer state. |

### 20.2.7.33 **status\_t I2C\_SlaveTransferGetCount ( I2C\_Type \* *base*, i2c\_slave\_handle\_t \* *handle*, size\_t \* *count* )**

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### Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                   |
| <i>handle</i> | pointer to i2c_slave_handle_t structure.                            |
| <i>count</i>  | Number of bytes transferred so far by the non-blocking transaction. |

### Return values

|                                |                                |
|--------------------------------|--------------------------------|
| <i>kStatus_InvalidArgument</i> | count is Invalid.              |
| <i>kStatus_Success</i>         | Successfully return the count. |

### 20.2.7.34 void I2C\_SlaveTransferHandleIRQ ( I2C\_Type \* *base*, void \* *i2cHandle* )

### Parameters

|                  |                                                                         |
|------------------|-------------------------------------------------------------------------|
| <i>base</i>      | I2C base pointer.                                                       |
| <i>i2cHandle</i> | pointer to i2c_slave_handle_t structure which stores the transfer state |

## 20.3 I2C eDMA Driver

### 20.3.1 Overview

#### Data Structures

- struct [i2c\\_master\\_edma\\_handle\\_t](#)  
*I2C master eDMA transfer structure. [More...](#)*

#### Typedefs

- typedef void(\* [i2c\\_master\\_edma\\_transfer\\_callback\\_t](#))(I2C\_Type \*base, i2c\_master\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*I2C master eDMA transfer callback typedef.*

### I2C Block eDMA Transfer Operation

- void [I2C\\_MasterCreateEDMAHandle](#) (I2C\_Type \*base, i2c\_master\_edma\_handle\_t \*handle, [i2c\\_master\\_edma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*edmaHandle)  
*Initializes the I2C handle which is used in transactional functions.*
- status\_t [I2C\\_MasterTransferEDMA](#) (I2C\_Type \*base, i2c\_master\_edma\_handle\_t \*handle, [i2c\\_master\\_transfer\\_t](#) \*xfer)  
*Performs a master eDMA non-blocking transfer on the I2C bus.*
- status\_t [I2C\\_MasterTransferGetCountEDMA](#) (I2C\_Type \*base, i2c\_master\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets a master transfer status during the eDMA non-blocking transfer.*
- void [I2C\\_MasterTransferAbortEDMA](#) (I2C\_Type \*base, i2c\_master\_edma\_handle\_t \*handle)  
*Aborts a master eDMA non-blocking transfer early.*

### 20.3.2 Data Structure Documentation

#### 20.3.2.1 struct [i2c\\_master\\_edma\\_handle](#)

I2C master eDMA handle typedef.

#### Data Fields

- [i2c\\_master\\_transfer\\_t](#) transfer  
*I2C master transfer structure.*
- size\_t [transferSize](#)  
*Total bytes to be transferred.*
- uint8\_t [nbytes](#)  
*eDMA minor byte transfer count initially configured.*
- uint8\_t [state](#)

## I2C eDMA Driver

- I2C master transfer status.*
  - `edma_handle_t * dmaHandle`  
*The eDMA handler used.*
  - `i2c_master_edma_transfer_callback_t completionCallback`  
*A callback function called after the eDMA transfer is finished.*
  - `void * userData`  
*A callback parameter passed to the callback function.*

### 20.3.2.1.0.63 Field Documentation

20.3.2.1.0.63.1 `i2c_master_transfer_t i2c_master_edma_handle_t::transfer`

20.3.2.1.0.63.2 `size_t i2c_master_edma_handle_t::transferSize`

20.3.2.1.0.63.3 `uint8_t i2c_master_edma_handle_t::nbytes`

20.3.2.1.0.63.4 `uint8_t i2c_master_edma_handle_t::state`

20.3.2.1.0.63.5 `edma_handle_t* i2c_master_edma_handle_t::dmaHandle`

20.3.2.1.0.63.6 `i2c_master_edma_transfer_callback_t i2c_master_edma_handle_t::completion-Callback`

20.3.2.1.0.63.7 `void* i2c_master_edma_handle_t::userData`

### 20.3.3 Typedef Documentation

20.3.3.1 `typedef void(* i2c_master_edma_transfer_callback_t)(I2C_Type *base, i2c_master_edma_handle_t *handle, status_t status, void *userData)`

### 20.3.4 Function Documentation

20.3.4.1 `void I2C_MasterCreateEDMAHandle ( I2C_Type * base, i2c_master_edma_handle_t * handle, i2c_master_edma_transfer_callback_t callback, void * userData, edma_handle_t * edmaHandle )`

#### Parameters

|                   |                                                                   |
|-------------------|-------------------------------------------------------------------|
| <i>base</i>       | I2C peripheral base address.                                      |
| <i>handle</i>     | A pointer to the <code>i2c_master_edma_handle_t</code> structure. |
| <i>callback</i>   | A pointer to the user callback function.                          |
| <i>userData</i>   | A user parameter passed to the callback function.                 |
| <i>edmaHandle</i> | eDMA handle pointer.                                              |



**20.3.4.2** `status_t I2C_MasterTransferEDMA ( I2C_Type * base, i2c_-  
master_edma_handle_t * handle, i2c_master_transfer_t * xfer  
)`

## I2C eDMA Driver

### Parameters

|               |                                                                                |
|---------------|--------------------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base address.                                                   |
| <i>handle</i> | A pointer to the <code>i2c_master_edma_handle_t</code> structure.              |
| <i>xfer</i>   | A pointer to the transfer structure of <a href="#">i2c_master_transfer_t</a> . |

### Return values

|                                     |                                                |
|-------------------------------------|------------------------------------------------|
| <i>kStatus_Success</i>              | Successfully completed the data transmission.  |
| <i>kStatus_I2C_Busy</i>             | A previous transmission is still not finished. |
| <i>kStatus_I2C_Timeout</i>          | Transfer error, waits for a signal timeout.    |
| <i>kStatus_I2C_Arbitration-Lost</i> | Transfer error, arbitration lost.              |
| <i>kStatus_I2C_Nak</i>              | Transfer error, receive NAK during transfer.   |

#### 20.3.4.3 `status_t I2C_MasterTransferGetCountEDMA ( I2C_Type * base, i2c_master_edma_handle_t * handle, size_t * count )`

### Parameters

|               |                                                                   |
|---------------|-------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base address.                                      |
| <i>handle</i> | A pointer to the <code>i2c_master_edma_handle_t</code> structure. |
| <i>count</i>  | A number of bytes transferred by the non-blocking transaction.    |

#### 20.3.4.4 `void I2C_MasterTransferAbortEDMA ( I2C_Type * base, i2c_master_edma_handle_t * handle )`

### Parameters

|               |                                                                   |
|---------------|-------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base address.                                      |
| <i>handle</i> | A pointer to the <code>i2c_master_edma_handle_t</code> structure. |

## 20.4 I2C DMA Driver

### 20.4.1 Overview

#### Data Structures

- struct [i2c\\_master\\_dma\\_handle\\_t](#)  
*I2C master DMA transfer structure. [More...](#)*

#### Typedefs

- typedef void(\* [i2c\\_master\\_dma\\_transfer\\_callback\\_t](#))(I2C\_Type \*base, i2c\_master\_dma\_handle\_t \*handle, status\_t status, void \*userData)  
*I2C master DMA transfer callback typedef.*

### I2C Block DMA Transfer Operation

- void [I2C\\_MasterTransferCreateHandleDMA](#) (I2C\_Type \*base, i2c\_master\_dma\_handle\_t \*handle, [i2c\\_master\\_dma\\_transfer\\_callback\\_t](#) callback, void \*userData, dma\_handle\_t \*dmaHandle)  
*Initializes the I2C handle which is used in transactional functions.*
- status\_t [I2C\\_MasterTransferDMA](#) (I2C\_Type \*base, i2c\_master\_dma\_handle\_t \*handle, [i2c\\_master\\_transfer\\_t](#) \*xfer)  
*Performs a master DMA non-blocking transfer on the I2C bus.*
- status\_t [I2C\\_MasterTransferGetCountDMA](#) (I2C\_Type \*base, i2c\_master\_dma\_handle\_t \*handle, size\_t \*count)  
*Gets a master transfer status during a DMA non-blocking transfer.*
- void [I2C\\_MasterTransferAbortDMA](#) (I2C\_Type \*base, i2c\_master\_dma\_handle\_t \*handle)  
*Aborts a master DMA non-blocking transfer early.*

### 20.4.2 Data Structure Documentation

#### 20.4.2.1 struct [i2c\\_master\\_dma\\_handle](#)

I2C master DMA handle typedef.

#### Data Fields

- [i2c\\_master\\_transfer\\_t](#) transfer  
*I2C master transfer struct.*
- size\_t [transferSize](#)  
*Total bytes to be transferred.*
- uint8\_t [state](#)  
*I2C master transfer status.*
- dma\_handle\_t \* [dmaHandle](#)

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*The DMA handler used.*

- [i2c\\_master\\_dma\\_transfer\\_callback\\_t completionCallback](#)  
*A callback function called after the DMA transfer finished.*
- void \* [userData](#)  
*A callback parameter passed to the callback function.*

### 20.4.2.1.0.64 Field Documentation

20.4.2.1.0.64.1 `i2c_master_transfer_t i2c_master_dma_handle_t::transfer`

20.4.2.1.0.64.2 `size_t i2c_master_dma_handle_t::transferSize`

20.4.2.1.0.64.3 `uint8_t i2c_master_dma_handle_t::state`

20.4.2.1.0.64.4 `dma_handle_t* i2c_master_dma_handle_t::dmaHandle`

20.4.2.1.0.64.5 `i2c_master_dma_transfer_callback_t i2c_master_dma_handle_t::completion-  
Callback`

20.4.2.1.0.64.6 `void* i2c_master_dma_handle_t::userData`

### 20.4.3 Typedef Documentation

20.4.3.1 `typedef void(* i2c_master_dma_transfer_callback_t)(I2C_Type *base,  
i2c_master_dma_handle_t *handle, status_t status, void *userData)`

### 20.4.4 Function Documentation

20.4.4.1 `void I2C_MasterTransferCreateHandleDMA ( I2C_Type * base,  
i2c_master_dma_handle_t * handle, i2c_master_dma_transfer_callback_t  
callback, void * userData, dma_handle_t * dmaHandle )`

Parameters

|                  |                                                  |
|------------------|--------------------------------------------------|
| <i>base</i>      | I2C peripheral base address                      |
| <i>handle</i>    | Pointer to the i2c_master_dma_handle_t structure |
| <i>callback</i>  | Pointer to the user callback function            |
| <i>userData</i>  | A user parameter passed to the callback function |
| <i>dmaHandle</i> | DMA handle pointer                               |

20.4.4.2 `status_t I2C_MasterTransferDMA ( I2C_Type * base, i2c_master_dma_handle_t  
* handle, i2c_master_transfer_t * xfer )`

## Parameters

|               |                                                                                  |
|---------------|----------------------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base address                                                      |
| <i>handle</i> | A pointer to the <code>i2c_master_dma_handle_t</code> structure                  |
| <i>xfer</i>   | A pointer to the transfer structure of the <a href="#">i2c_master_transfer_t</a> |

## Return values

|                                     |                                                 |
|-------------------------------------|-------------------------------------------------|
| <i>kStatus_Success</i>              | Successfully completes the data transmission.   |
| <i>kStatus_I2C_Busy</i>             | A previous transmission is still not finished.  |
| <i>kStatus_I2C_Timeout</i>          | A transfer error, waits for the signal timeout. |
| <i>kStatus_I2C_Arbitration-Lost</i> | A transfer error, arbitration lost.             |
| <i>kStatus_I2C_Nak</i>              | A transfer error, receives NAK during transfer. |

#### 20.4.4.3 `status_t I2C_MasterTransferGetCountDMA ( I2C_Type * base, i2c_master_dma_handle_t * handle, size_t * count )`

## Parameters

|               |                                                                       |
|---------------|-----------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base address                                           |
| <i>handle</i> | A pointer to the <code>i2c_master_dma_handle_t</code> structure       |
| <i>count</i>  | A number of bytes transferred so far by the non-blocking transaction. |

#### 20.4.4.4 `void I2C_MasterTransferAbortDMA ( I2C_Type * base, i2c_master_dma_handle_t * handle )`

## Parameters

|               |                                                                  |
|---------------|------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base address                                      |
| <i>handle</i> | A pointer to the <code>i2c_master_dma_handle_t</code> structure. |

### 20.5 I2C FreeRTOS Driver

#### 20.5.1 Overview

#### I2C RTOS Operation

- status\_t [I2C\\_RTOS\\_Init](#) (i2c\_rtos\_handle\_t \*handle, I2C\_Type \*base, const [i2c\\_master\\_config\\_t](#) \*masterConfig, uint32\_t srcClock\_Hz)  
*Initializes I2C.*
- status\_t [I2C\\_RTOS\\_Deinit](#) (i2c\_rtos\_handle\_t \*handle)  
*Deinitializes the I2C.*
- status\_t [I2C\\_RTOS\\_Transfer](#) (i2c\_rtos\_handle\_t \*handle, [i2c\\_master\\_transfer\\_t](#) \*transfer)  
*Performs the I2C transfer.*

#### 20.5.2 Function Documentation

##### 20.5.2.1 status\_t I2C\_RTOS\_Init ( i2c\_rtos\_handle\_t \* *handle*, I2C\_Type \* *base*, const [i2c\\_master\\_config\\_t](#) \* *masterConfig*, uint32\_t *srcClock\_Hz* )

This function initializes the I2C module and the related RTOS context.

Parameters

|                     |                                                                          |
|---------------------|--------------------------------------------------------------------------|
| <i>handle</i>       | The RTOS I2C handle, the pointer to an allocated space for RTOS context. |
| <i>base</i>         | The pointer base address of the I2C instance to initialize.              |
| <i>masterConfig</i> | The configuration structure to set-up I2C in master mode.                |
| <i>srcClock_Hz</i>  | The frequency of an input clock of the I2C module.                       |

Returns

status of the operation.

##### 20.5.2.2 status\_t I2C\_RTOS\_Deinit ( i2c\_rtos\_handle\_t \* *handle* )

This function deinitializes the I2C module and the related RTOS context.

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | The RTOS I2C handle. |
|---------------|----------------------|

**20.5.2.3** `status_t I2C_RTOS_Transfer ( i2c_rtos_handle_t * handle, i2c_master_transfer_t * transfer )`

This function performs the I2C transfer according to the data given in the transfer structure.

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### Parameters

|                 |                                                 |
|-----------------|-------------------------------------------------|
| <i>handle</i>   | The RTOS I2C handle.                            |
| <i>transfer</i> | A structure specifying the transfer parameters. |

### Returns

status of the operation.



## 20.6 I2C $\mu$ COS/II Driver

### 20.6.1 Overview

#### I2C RTOS Operation

- status\_t **I2C\_RTOS\_Init** (i2c\_rtos\_handle\_t \*handle, I2C\_Type \*base, const i2c\_master\_config\_t \*masterConfig, uint32\_t srcClock\_Hz)  
*Initializes the I2C.*
- status\_t **I2C\_RTOS\_Deinit** (i2c\_rtos\_handle\_t \*handle)  
*Deinitializes the I2C.*
- status\_t **I2C\_RTOS\_Transfer** (i2c\_rtos\_handle\_t \*handle, i2c\_master\_transfer\_t \*transfer)  
*Performs the I2C transfer.*

### 20.6.2 Function Documentation

#### 20.6.2.1 status\_t I2C\_RTOS\_Init ( i2c\_rtos\_handle\_t \* *handle*, I2C\_Type \* *base*, const i2c\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

This function initializes the I2C module and the related RTOS context.

Parameters

|                     |                                                                          |
|---------------------|--------------------------------------------------------------------------|
| <i>handle</i>       | The RTOS I2C handle; the pointer to an allocated space for RTOS context. |
| <i>base</i>         | The pointer base address of the I2C instance to initialize.              |
| <i>masterConfig</i> | A configuration structure to set-up the I2C in master mode.              |
| <i>srcClock_Hz</i>  | A frequency of the input clock of the I2C module.                        |

Returns

status of the operation.

#### 20.6.2.2 status\_t I2C\_RTOS\_Deinit ( i2c\_rtos\_handle\_t \* *handle* )

This function deinitializes the I2C module and the related RTOS context.

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | The RTOS I2C handle. |
|---------------|----------------------|

### 20.6.2.3 `status_t I2C_RTOS_Transfer ( i2c_rtos_handle_t * handle, i2c_master_transfer_t * transfer )`

This function performs the I2C transfer according to the data given in the transfer structure.

## Parameters

|                 |                                                 |
|-----------------|-------------------------------------------------|
| <i>handle</i>   | The RTOS I2C handle.                            |
| <i>transfer</i> | A structure specifying the transfer parameters. |

## Returns

status of the operation.

### 20.7 I2C $\mu$ COS/III Driver

#### 20.7.1 Overview

#### I2C RTOS Operation

- status\_t **I2C\_RTOS\_Init** (i2c\_rtos\_handle\_t \*handle, I2C\_Type \*base, const i2c\_master\_config\_t \*masterConfig, uint32\_t srcClock\_Hz)  
*Initializes the I2C.*
- status\_t **I2C\_RTOS\_Deinit** (i2c\_rtos\_handle\_t \*handle)  
*Deinitializes the I2C.*
- status\_t **I2C\_RTOS\_Transfer** (i2c\_rtos\_handle\_t \*handle, i2c\_master\_transfer\_t \*transfer)  
*Performs the I2C transfer.*

#### 20.7.2 Function Documentation

##### 20.7.2.1 status\_t I2C\_RTOS\_Init ( i2c\_rtos\_handle\_t \* *handle*, I2C\_Type \* *base*, const i2c\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

This function initializes the I2C module and the related RTOS context.

Parameters

|                     |                                                                              |
|---------------------|------------------------------------------------------------------------------|
| <i>handle</i>       | The RTOS I2C handle; the pointer to an allocated space for the RTOS context. |
| <i>base</i>         | The pointer base address of the I2C instance to initialize.                  |
| <i>masterConfig</i> | A configuration structure to set-up the I2C in master mode.                  |
| <i>srcClock_Hz</i>  | A frequency of the input clock of the I2C module.                            |

Returns

status of the operation.

##### 20.7.2.2 status\_t I2C\_RTOS\_Deinit ( i2c\_rtos\_handle\_t \* *handle* )

This function deinitializes the I2C module and the related RTOS context.

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | The RTOS I2C handle. |
|---------------|----------------------|

**20.7.2.3** `status_t I2C_RTOS_Transfer ( i2c_rtos_handle_t * handle, i2c_master_transfer_t * transfer )`

This function performs the I2C transfer according to the data given in the transfer structure.

## I2C $\mu$ COS/III Driver

### Parameters

|                 |                                                 |
|-----------------|-------------------------------------------------|
| <i>handle</i>   | The RTOS I2C handle.                            |
| <i>transfer</i> | A structure specifying the transfer parameters. |

### Returns

status of the operation.

## Chapter 21

# LLWU: Low-Leakage Wakeup Unit Driver

### 21.1 Overview

The KSDK provides a peripheral driver for the Low-Leakage Wakeup Unit (LLWU) module of Kinetis devices. The LLWU module allows the user to select external pin sources and internal modules as a wake-up source from low-leakage power modes.

### 21.2 External wakeup pins configurations

Configures the external wakeup pins' working modes, gets, and clears the wake pin flags. External wakeup pins are accessed by the `pinIndex`, which is started from 1. Numbers of the external pins depend on the SoC configuration.

### 21.3 Internal wakeup modules configurations

Enables/disables the internal wakeup modules and gets the module flags. Internal modules are accessed by `moduleIndex`, which is started from 1. Numbers of external pins depend the on SoC configuration.

### 21.4 Digital pin filter for external wakeup pin configurations

Configures the digital pin filter of the external wakeup pins' working modes, gets, and clears the pin filter flags. Digital pin filters are accessed by the `filterIndex`, which is started from 1. Numbers of external pins depend on the SoC configuration.

## Data Structures

- struct `llwu_external_pin_filter_mode_t`  
*An external input pin filter control structure. [More...](#)*

## Enumerations

- enum `llwu_external_pin_mode_t` {  
    `kLLWU_ExternalPinDisable` = 0U,  
    `kLLWU_ExternalPinRisingEdge` = 1U,  
    `kLLWU_ExternalPinFallingEdge` = 2U,  
    `kLLWU_ExternalPinAnyEdge` = 3U }  
*External input pin control modes.*
- enum `llwu_pin_filter_mode_t` {  
    `kLLWU_PinFilterDisable` = 0U,  
    `kLLWU_PinFilterRisingEdge` = 1U,  
    `kLLWU_PinFilterFallingEdge` = 2U,  
    `kLLWU_PinFilterAnyEdge` = 3U }  
*Digital filter control modes.*

## Enumeration Type Documentation

### Driver version

- #define **FSL\_LLWU\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 0, 1))  
*LLWU driver version 2.0.1.*

### Low-Leakage Wakeup Unit Control APIs

- void **LLWU\_SetExternalWakeupPinMode** (LLWU\_Type \*base, uint32\_t pinIndex, **llwu\_external\_pin\_mode\_t** pinMode)  
*Sets the external input pin source mode.*
- bool **LLWU\_GetExternalWakeupPinFlag** (LLWU\_Type \*base, uint32\_t pinIndex)  
*Gets the external wakeup source flag.*
- void **LLWU\_ClearExternalWakeupPinFlag** (LLWU\_Type \*base, uint32\_t pinIndex)  
*Clears the external wakeup source flag.*
- static void **LLWU\_EnableInternalModuleInterruptWakup** (LLWU\_Type \*base, uint32\_t moduleIndex, bool enable)  
*Enables/disables the internal module source.*
- static bool **LLWU\_GetInternalWakeupModuleFlag** (LLWU\_Type \*base, uint32\_t moduleIndex)  
*Gets the external wakeup source flag.*
- void **LLWU\_SetPinFilterMode** (LLWU\_Type \*base, uint32\_t filterIndex, **llwu\_external\_pin\_filter\_mode\_t** filterMode)  
*Sets the pin filter configuration.*
- bool **LLWU\_GetPinFilterFlag** (LLWU\_Type \*base, uint32\_t filterIndex)  
*Gets the pin filter configuration.*
- void **LLWU\_ClearPinFilterFlag** (LLWU\_Type \*base, uint32\_t filterIndex)  
*Clears the pin filter configuration.*

## 21.5 Data Structure Documentation

### 21.5.1 struct llwu\_external\_pin\_filter\_mode\_t

#### Data Fields

- uint32\_t **pinIndex**  
*A pin number.*
- **llwu\_pin\_filter\_mode\_t** filterMode  
*Filter mode.*

## 21.6 Macro Definition Documentation

### 21.6.1 #define FSL\_LLWU\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

## 21.7 Enumeration Type Documentation

### 21.7.1 enum llwu\_external\_pin\_mode\_t

Enumerator

**kLLWU\_ExternalPinDisable** Pin disabled as a wakeup input.



***kLLWU\_ExternalPinRisingEdge*** Pin enabled with the rising edge detection.

***kLLWU\_ExternalPinFallingEdge*** Pin enabled with the falling edge detection.

***kLLWU\_ExternalPinAnyEdge*** Pin enabled with any change detection.

## 21.7.2 enum llwu\_pin\_filter\_mode\_t

Enumerator

***kLLWU\_PinFilterDisable*** Filter disabled.

***kLLWU\_PinFilterRisingEdge*** Filter positive edge detection.

***kLLWU\_PinFilterFallingEdge*** Filter negative edge detection.

***kLLWU\_PinFilterAnyEdge*** Filter any edge detection.

## 21.8 Function Documentation

### 21.8.1 void LLWU\_SetExternalWakeupPinMode ( LLWU\_Type \* *base*, uint32\_t *pinIndex*, llwu\_external\_pin\_mode\_t *pinMode* )

This function sets the external input pin source mode that is used as a wake up source.

Parameters

|                 |                                                                         |
|-----------------|-------------------------------------------------------------------------|
| <i>base</i>     | LLWU peripheral base address.                                           |
| <i>pinIndex</i> | A pin index to be enabled as an external wakeup source starting from 1. |
| <i>pinMode</i>  | A pin configuration mode defined in the llwu_external_pin_modes_t.      |

### 21.8.2 bool LLWU\_GetExternalWakeupPinFlag ( LLWU\_Type \* *base*, uint32\_t *pinIndex* )

This function checks the external pin flag to detect whether the MCU is woken up by the specific pin.

Parameters

|                 |                                   |
|-----------------|-----------------------------------|
| <i>base</i>     | LLWU peripheral base address.     |
| <i>pinIndex</i> | A pin index, which starts from 1. |

Returns

True if the specific pin is a wakeup source.

## Function Documentation

### 21.8.3 void LLWU\_ClearExternalWakeupPinFlag ( LLWU\_Type \* *base*, uint32\_t *pinIndex* )

This function clears the external wakeup source flag for a specific pin.

## Parameters

|                 |                                   |
|-----------------|-----------------------------------|
| <i>base</i>     | LLWU peripheral base address.     |
| <i>pinIndex</i> | A pin index, which starts from 1. |

#### 21.8.4 static void LLWU\_EnableInternalModuleInterruptWakeup ( LLWU\_Type \* *base*, uint32\_t *moduleIndex*, bool *enable* ) [inline], [static]

This function enables/disables the internal module source mode that is used as a wake up source.

## Parameters

|                    |                                                                            |
|--------------------|----------------------------------------------------------------------------|
| <i>base</i>        | LLWU peripheral base address.                                              |
| <i>moduleIndex</i> | A module index to be enabled as an internal wakeup source starting from 1. |
| <i>enable</i>      | An enable or a disable setting                                             |

#### 21.8.5 static bool LLWU\_GetInternalWakeupModuleFlag ( LLWU\_Type \* *base*, uint32\_t *moduleIndex* ) [inline], [static]

This function checks the external pin flag to detect whether the system is woken up by the specific pin.

## Parameters

|                    |                                      |
|--------------------|--------------------------------------|
| <i>base</i>        | LLWU peripheral base address.        |
| <i>moduleIndex</i> | A module index, which starts from 1. |

## Returns

True if the specific pin is a wake up source.

#### 21.8.6 void LLWU\_SetPinFilterMode ( LLWU\_Type \* *base*, uint32\_t *filterIndex*, llwu\_external\_pin\_filter\_mode\_t *filterMode* )

This function sets the pin filter configuration.

## Function Documentation

### Parameters

|                    |                                                                                |
|--------------------|--------------------------------------------------------------------------------|
| <i>base</i>        | LLWU peripheral base address.                                                  |
| <i>filterIndex</i> | A pin filter index used to enable/disable the digital filter, starting from 1. |
| <i>filterMode</i>  | A filter mode configuration                                                    |

### 21.8.7 bool LLWU\_GetPinFilterFlag ( LLWU\_Type \* *base*, uint32\_t *filterIndex* )

This function gets the pin filter flag.

### Parameters

|                    |                                          |
|--------------------|------------------------------------------|
| <i>base</i>        | LLWU peripheral base address.            |
| <i>filterIndex</i> | A pin filter index, which starts from 1. |

### Returns

True if the flag is a source of the existing low-leakage power mode.

### 21.8.8 void LLWU\_ClearPinFilterFlag ( LLWU\_Type \* *base*, uint32\_t *filterIndex* )

This function clears the pin filter flag.

### Parameters

|                    |                                                        |
|--------------------|--------------------------------------------------------|
| <i>base</i>        | LLWU peripheral base address.                          |
| <i>filterIndex</i> | A pin filter index to clear the flag, starting from 1. |

# Chapter 22

## LMEM: Local Memory Controller Cache Control Driver

### 22.1 Overview

The KSDK provides a peripheral driver for the Local Memory Controller Cache Controller module of Kinetis devices.

### 22.2 Descriptions

The LMEM Cache peripheral driver allows the user to enable/disable the cache and to perform cache maintenance operations such as invalidate, push, and clear. These maintenance operations may be performed on the Processor Code (PC) bus or Both Processor Code (PC) and Processor System (PS) bus.

The Kinetis devices contain a Processor Code (PC) bus and a Processor System (PS) bus as follows. The Processor Code (PC) bus - a 32-bit address space bus with low-order addresses (0x0000\_0000 through 0x1FFF\_FFFF) used normally for code access. The Processor System (PS) bus - a 32-bit address space bus with high-order addresses (0x2000\_0000 through 0xFFFF\_FFFF) used normally for data accesses.

Some Kinetic MCU devices have caches available for the PC bus and PS bus, others may only have a PC bus cache, while some do not have PC or PS caches at all. See the appropriate Kinetis reference manual for cache availability.

Cache maintenance operations:

| command |            | description |                                                                 |
|---------|------------|-------------|-----------------------------------------------------------------|
|         | Invalidate |             | U                                                               |
|         | Push       | P           | ush a cache entry if it is valid and modified, then clear the m |
|         | Clear      | P           | ush a cache entry if it is valid                                |

The above cache maintenance operations may be performed on the entire cache or on a line-basis. The peripheral driver API names distinguish between the two using the terms "All" or Line".

### 22.3 Function groups

#### 22.3.1 Local Memory Processor Code Bus Cache Control

The invalidate command can be performed on the entire cache, one line, or multiple lines by calling [LMEM\\_CodeCacheInvalidateAll\(\)](#), [LMEM\\_CodeCacheInvalidateLine\(\)](#), and [LMEM\\_CodeCacheInvalidateMultiLines\(\)](#).

## Function groups

The push command can be performed on the entire cache, one line, or multiple lines by calling [LMEM\\_CodeCachePushAll\(\)](#), [LMEM\\_CodeCachePushLine\(\)](#), and [LMEM\\_CodeCachePushMultiLines\(\)](#).

The clear command can be performed on the entire cache, one line, or multiple lines by calling [LMEM\\_CodeCacheClearAll\(\)](#), [LMEM\\_CodeCacheClearLine\(\)](#), and [LMEM\\_CodeCacheClearMultiLines\(\)](#).

Note that the parameter "address" must be supplied, which indicates the physical address of the line to perform the one line cache maintenance operation. In addition, the length of the number of bytes should be supplied for multiple line operation. The function determines if the length meets or exceeds 1/2 the cache size because the cache contains 2 WAYs, half of the cache is in WAY0 and the other half in WAY1 and if so, performs a cache maintenance "all" operation which is faster than performing the cache maintenance on a line-basis.

Cache Demotion: Cache region demotion - Demoting the cache mode reduces the cache function applied to a memory region from write-back to write-through to non-cacheable. The cache region demote function checks to see if the requested cache mode is higher than or equal to the current cache mode, and if so, returns an error. After a region is demoted, its cache mode can only be raised by a reset, which returns it to its default state. To demote a cache region, call the [LMEM\\_CodeCacheDemoteRegion\(\)](#).

Note that the address region assignment of the 16 subregions is device-specific and is detailed in the Chip Configuration part of the SoC Kinetis reference manual. The LMEM provides typedef enums for each of the 16 regions, starting with "kLMEM\_CacheRegion0" and ending with "kLMEM\_CacheRegion15". The parameter cacheMode is of type `lmem_cache_mode_t`. This provides typedef enums for each of the cache modes, such as "kLMEM\_CacheNonCacheable", "kLMEM\_CacheWriteThrough", and "kLMEM\_CacheWriteBack".

Cache Enable and Disable: The cache enable function enables the PC bus cache and the write buffer. However, before enabling these, the function first performs an invalidate all. Call [LMEM\\_EnableCodeCache\(\)](#) to enable a particular bus cache.

### 22.3.2 Local Memory Processor System Bus Cache Control

The invalidate command can be performed on the entire cache, one line, or multiple lines by calling [LMEM\\_SystemCacheInvalidateAll\(\)](#), [LMEM\\_SystemCacheInvalidateLine\(\)](#), and [LMEM\\_SystemCacheInvalidateMultiLines\(\)](#).

The push command can be performed on the entire cache, one line, or multiple lines by calling [LMEM\\_SystemCachePushAll\(\)](#), [LMEM\\_SystemCachePushLine\(\)](#), and [LMEM\\_SystemCachePushMultiLines\(\)](#).

The clear command can be performed on the entire cache, one line, or multiple lines by calling [LMEM\\_SystemCacheClearAll\(\)](#), [LMEM\\_SystemCacheClearLine\(\)](#), and [LMEM\\_SystemCacheClearMultiLines\(\)](#).

Note that the parameter "address" must be supplied, which indicates the physical address of the line to perform the one line cache maintenance operation. In addition, the length of the number of bytes should be supplied for multiple lines operation. The function determines if the length meets or exceeds 1/2 the cache size because the cache contains 2 WAYs, half of the cache is in WAY0 and the other half in WAY1 and if so, performs a cache maintenance "all" operation which is faster than performing the cache maintenance on a line-basis.

Cache Demotion: Cache region demotion - Demoting the cache mode reduces the cache function applied to a memory region from write-back to write-through to non-cacheable. The cache region demote function checks to see if the requested cache mode is higher than or equal to the current cache mode, and if so, returns an error. After a region is demoted, its cache mode can only be raised by a reset, which returns it to its default state. To demote a cache region, call the `LMEM_SystemCacheDemoteRegion()`.

Note that the address region assignment of the 16 subregions is device-specific and is described in the Chip Configuration part of the Kinetis SoC reference manual. The LMEM provides typedef enumerations for each of the 16 regions, starting with "kLMEM\_CacheRegion0" and ending with "kLMEM\_CacheRegion15". The parameter cacheMode is of type `lmem_cache_mode_t`. This provides typedef enumerations for each of the cache modes, such as "kLMEM\_CacheNonCacheable", "kLMEM\_CacheWriteThrough", and "kLMEM\_CacheWriteBack". Cache Enable and Disable: The cache enable function enables the PS bus cache and the write buffer. However, before enabling these, the function first performs an invalidate all. Call `LMEM_EnableSystemCache()` to enable a particular bus cache.

## Macros

- #define `LMEM_CACHE_LINE_SIZE` (0x10U)  
*Cache line is 16-bytes.*
- #define `LMEM_CACHE_SIZE_ONEWAY` (4096U)  
*Cache size is 4K-bytes one way.*

## Enumerations

- enum `lmem_cache_mode_t` {  
    `kLMEM_NonCacheable` = 0x0U,  
    `kLMEM_CacheWriteThrough` = 0x2U,  
    `kLMEM_CacheWriteBack` = 0x3U }  
*LMEM cache mode options.*
- enum `lmem_cache_region_t` {  
    `kLMEM_CacheRegion15` = 0U,  
    `kLMEM_CacheRegion14`,  
    `kLMEM_CacheRegion13`,  
    `kLMEM_CacheRegion12`,  
    `kLMEM_CacheRegion11`,  
    `kLMEM_CacheRegion10`,  
    `kLMEM_CacheRegion9`,  
    `kLMEM_CacheRegion8`,  
    `kLMEM_CacheRegion7`,  
    `kLMEM_CacheRegion6`,  
    `kLMEM_CacheRegion5`,  
    `kLMEM_CacheRegion4`,  
    `kLMEM_CacheRegion3`,  
    `kLMEM_CacheRegion2`,  
    `kLMEM_CacheRegion1`,  
    `kLMEM_CacheRegion0` }  
*LMEM cache regions.*

## Macro Definition Documentation

- enum `lmem_cache_line_command_t` {  
    `kLMEM_CacheLineSearchReadOrWrite` = 0U,  
    `kLMEM_CacheLineInvalidate`,  
    `kLMEM_CacheLinePush`,  
    `kLMEM_CacheLineClear` }  
    *LMEM cache line command.*

## Driver version

- #define `FSL_LMEM_DRIVER_VERSION` (`MAKE_VERSION`(2, 1, 0))  
    *LMEM controller driver version 2.1.0.*

## Local Memory Processor Code Bus Cache Control

- void `LMEM_EnableCodeCache` (`LMEM_Type` \*base, bool enable)  
    *Enables/disables the processor code bus cache.*
- static void `LMEM_EnableCodeWriteBuffer` (`LMEM_Type` \*base, bool enable)  
    *Enables/disables the processor code bus write buffer.*
- void `LMEM_CodeCacheInvalidateAll` (`LMEM_Type` \*base)  
    *Invalidates the processor code bus cache.*
- void `LMEM_CodeCachePushAll` (`LMEM_Type` \*base)  
    *Pushes all modified lines in the processor code bus cache.*
- void `LMEM_CodeCacheClearAll` (`LMEM_Type` \*base)  
    *Clears the processor code bus cache.*
- void `LMEM_CodeCacheInvalidateLine` (`LMEM_Type` \*base, uint32\_t address)  
    *Invalidates a specific line in the processor code bus cache.*
- void `LMEM_CodeCacheInvalidateMultiLines` (`LMEM_Type` \*base, uint32\_t address, uint32\_t length)  
    *Invalidates multiple lines in the processor code bus cache.*
- void `LMEM_CodeCachePushLine` (`LMEM_Type` \*base, uint32\_t address)  
    *Pushes a specific modified line in the processor code bus cache.*
- void `LMEM_CodeCachePushMultiLines` (`LMEM_Type` \*base, uint32\_t address, uint32\_t length)  
    *Pushes multiple modified lines in the processor code bus cache.*
- void `LMEM_CodeCacheClearLine` (`LMEM_Type` \*base, uint32\_t address)  
    *Clears a specific line in the processor code bus cache.*
- void `LMEM_CodeCacheClearMultiLines` (`LMEM_Type` \*base, uint32\_t address, uint32\_t length)  
    *Clears multiple lines in the processor code bus cache.*
- status\_t `LMEM_CodeCacheDemoteRegion` (`LMEM_Type` \*base, `lmem_cache_region_t` region, `lmem_cache_mode_t` cacheMode)  
    *Demotes the cache mode of a region in processor code bus cache.*

## 22.4 Macro Definition Documentation

22.4.1 #define `FSL_LMEM_DRIVER_VERSION` (`MAKE_VERSION`(2, 1, 0))

22.4.2 #define `LMEM_CACHE_LINE_SIZE` (0x10U)

22.4.3 #define `LMEM_CACHE_SIZE_ONWAY` (4096U)



## 22.5 Enumeration Type Documentation

### 22.5.1 enum lmem\_cache\_mode\_t

Enumerator

***kLMEM\_NonCacheable*** Cache mode: non-cacheable.  
***kLMEM\_CacheWriteThrough*** Cache mode: write-through.  
***kLMEM\_CacheWriteBack*** Cache mode: write-back.

### 22.5.2 enum lmem\_cache\_region\_t

Enumerator

***kLMEM\_CacheRegion15*** Cache Region 15.  
***kLMEM\_CacheRegion14*** Cache Region 14.  
***kLMEM\_CacheRegion13*** Cache Region 13.  
***kLMEM\_CacheRegion12*** Cache Region 12.  
***kLMEM\_CacheRegion11*** Cache Region 11.  
***kLMEM\_CacheRegion10*** Cache Region 10.  
***kLMEM\_CacheRegion9*** Cache Region 9.  
***kLMEM\_CacheRegion8*** Cache Region 8.  
***kLMEM\_CacheRegion7*** Cache Region 7.  
***kLMEM\_CacheRegion6*** Cache Region 6.  
***kLMEM\_CacheRegion5*** Cache Region 5.  
***kLMEM\_CacheRegion4*** Cache Region 4.  
***kLMEM\_CacheRegion3*** Cache Region 3.  
***kLMEM\_CacheRegion2*** Cache Region 2.  
***kLMEM\_CacheRegion1*** Cache Region 1.  
***kLMEM\_CacheRegion0*** Cache Region 0.

### 22.5.3 enum lmem\_cache\_line\_command\_t

Enumerator

***kLMEM\_CacheLineSearchReadOrWrite*** Cache line search and read or write.  
***kLMEM\_CacheLineInvalidate*** Cache line invalidate.  
***kLMEM\_CacheLinePush*** Cache line push.  
***kLMEM\_CacheLineClear*** Cache line clear.

### 22.6 Function Documentation

#### 22.6.1 void LMEM\_EnableCodeCache ( LMEM\_Type \* *base*, bool *enable* )

This function enables/disables the cache. The function first invalidates the entire cache and then enables/disables both the cache and write buffers.

## Parameters

|               |                                                                                           |
|---------------|-------------------------------------------------------------------------------------------|
| <i>base</i>   | LMEM peripheral base address.                                                             |
| <i>enable</i> | The enable or disable flag. true - enable the code cache. false - disable the code cache. |

### 22.6.2 static void LMEM\_EnableCodeWriteBuffer ( LMEM\_Type \* *base*, bool *enable* ) [inline], [static]

## Parameters

|               |                                                                                                                 |
|---------------|-----------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | LMEM peripheral base address.                                                                                   |
| <i>enable</i> | The enable or disable flag. true - enable the code bus write buffer. false - disable the code bus write buffer. |

### 22.6.3 void LMEM\_CodeCacheInvalidateAll ( LMEM\_Type \* *base* )

This function invalidates the cache both ways, which means that it unconditionally clears valid bits and modifies bits of a cache entry.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LMEM peripheral base address. |
|-------------|-------------------------------|

### 22.6.4 void LMEM\_CodeCachePushAll ( LMEM\_Type \* *base* )

This function pushes all modified lines in both ways in the entire cache. It pushes a cache entry if it is valid and modified and clears the modified bit. If the entry is not valid or not modified, leave as is. This action does not clear the valid bit. A cache push is synonymous with a cache flush.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LMEM peripheral base address. |
|-------------|-------------------------------|

### 22.6.5 void LMEM\_CodeCacheClearAll ( LMEM\_Type \* *base* )

This function clears the entire cache and pushes (flushes) and invalidates the operation. Clear - Pushes a cache entry if it is valid and modified, then clears the valid and modified bits. If the entry is not valid or not modified, clear the valid bit.

## Function Documentation

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LMEM peripheral base address. |
|-------------|-------------------------------|

### 22.6.6 void LMEM\_CodeCacheInvalidateLine ( LMEM\_Type \* *base*, uint32\_t *address* )

This function invalidates a specific line in the cache based on the physical address passed in by the user. Invalidate - Unconditionally clears valid and modified bits of a cache entry.

### Parameters

|                |                                                                                                                                         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | LMEM peripheral base address.                                                                                                           |
| <i>address</i> | The physical address of the cache line. Should be 16-byte aligned address. If not, it is changed to the 16-byte aligned memory address. |

### 22.6.7 void LMEM\_CodeCacheInvalidateMultiLines ( LMEM\_Type \* *base*, uint32\_t *address*, uint32\_t *length* )

This function invalidates multiple lines in the cache based on the physical address and length in bytes passed in by the user. If the function detects that the length meets or exceeds half the cache, the function performs an entire cache invalidate function, which is more efficient than invalidating the cache line-by-line. Because the cache consists of two ways and line commands based on the physical address searches both ways, check half the total amount of cache. Invalidate - Unconditionally clear valid and modified bits of a cache entry.

### Parameters

|                |                                                                                                                                         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | LMEM peripheral base address.                                                                                                           |
| <i>address</i> | The physical address of the cache line. Should be 16-byte aligned address. If not, it is changed to the 16-byte aligned memory address. |
| <i>length</i>  | The length in bytes of the total amount of cache lines.                                                                                 |

### 22.6.8 void LMEM\_CodeCachePushLine ( LMEM\_Type \* *base*, uint32\_t *address* )

This function pushes a specific modified line based on the physical address passed in by the user. Push - Push a cache entry if it is valid and modified, then clear the modified bit. If the entry is not valid or not modified, leave as is. This action does not clear the valid bit. A cache push is synonymous with a cache flush.

## Parameters

|                |                                                                                                                                         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | LMEM peripheral base address.                                                                                                           |
| <i>address</i> | The physical address of the cache line. Should be 16-byte aligned address. If not, it is changed to the 16-byte aligned memory address. |

### 22.6.9 void LMEM\_CodeCachePushMultiLines ( LMEM\_Type \* *base*, uint32\_t *address*, uint32\_t *length* )

This function pushes multiple modified lines in the cache based on the physical address and length in bytes passed in by the user. If the function detects that the length meets or exceeds half of the cache, the function performs an cache push function, which is more efficient than pushing the modified lines in the cache line-by-line. Because the cache consists of two ways and line commands based on the physical address searches both ways, check half the total amount of cache. Push - Push a cache entry if it is valid and modified, then clear the modified bit. If the entry is not valid or not modified, leave as is. This action does not clear the valid bit. A cache push is synonymous with a cache flush.

## Parameters

|                |                                                                                                                                         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | LMEM peripheral base address.                                                                                                           |
| <i>address</i> | The physical address of the cache line. Should be 16-byte aligned address. If not, it is changed to the 16-byte aligned memory address. |
| <i>length</i>  | The length in bytes of the total amount of cache lines.                                                                                 |

### 22.6.10 void LMEM\_CodeCacheClearLine ( LMEM\_Type \* *base*, uint32\_t *address* )

This function clears a specific line based on the physical address passed in by the user. Clear - Push a cache entry if it is valid and modified, then clear the valid and modify bits. If entry not valid or not modified, clear the valid bit.

## Parameters

|                |                                                                                                                                         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | LMEM peripheral base address.                                                                                                           |
| <i>address</i> | The physical address of the cache line. Should be 16-byte aligned address. If not, it is changed to the 16-byte aligned memory address. |

### 22.6.11 void LMEM\_CodeCacheClearMultiLines ( LMEM\_Type \* *base*, uint32\_t *address*, uint32\_t *length* )

This function clears multiple lines in the cache based on the physical address and length in bytes passed in by the user. If the function detects that the length meets or exceeds half the total amount of cache, the function performs a cache clear function which is more efficient than clearing the lines in the cache line-by-line. Because the cache consists of two ways and line commands based on the physical address searches both ways, check half the total amount of cache. Clear - Push a cache entry if it is valid and modified, then clear the valid and modify bits. If entry not valid or not modified, clear the valid bit.

Parameters

|                |                                                                                                                                         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | LMEM peripheral base address.                                                                                                           |
| <i>address</i> | The physical address of the cache line. Should be 16-byte aligned address. If not, it is changed to the 16-byte aligned memory address. |
| <i>length</i>  | The length in bytes of the total amount of cache lines.                                                                                 |

### 22.6.12 status\_t LMEM\_CodeCacheDemoteRegion ( LMEM\_Type \* *base*, lmem\_cache\_region\_t *region*, lmem\_cache\_mode\_t *cacheMode* )

This function allows the user to demote the cache mode of a region within the device's memory map. Demoting the cache mode reduces the cache function applied to a memory region from write-back to write-through to non-cacheable. The function checks to see if the requested cache mode is higher than or equal to the current cache mode, and if so, returns an error. After a region is demoted, its cache mode can only be raised by a reset, which returns it to its default state which is the highest cache configure for each region. To maintain cache coherency, changes to the cache mode should be completed while the address space being changed is not being accessed or the cache is disabled. Before a cache mode change, this function completes a cache clear all command to push and invalidate any cache entries that may have changed.

Parameters

|                  |                                                           |
|------------------|-----------------------------------------------------------|
| <i>base</i>      | LMEM peripheral base address.                             |
| <i>region</i>    | The desired region to demote of type lmem_cache_region_t. |
| <i>cacheMode</i> | The new, demoted cache mode of type lmem_cache_mode_t.    |

Returns

The execution result. kStatus\_Success The cache demote operation is successful. kStatus\_Fail The cache demote operation is failure.

## Chapter 23

# LPTMR: Low-Power Timer

### 23.1 Overview

The KSDK provides a driver for the Low-Power Timer (LPTMR) of Kinetis devices.

### 23.2 Function groups

The LPTMR driver supports operating the module as a time counter or as a pulse counter.

#### 23.2.1 Initialization and deinitialization

The function [LPTMR\\_Init\(\)](#) initializes the LPTMR with specified configurations. The function [LPTMR\\_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the LPTMR for a timer or a pulse counter mode. It also sets up the LPTMR's free running mode operation and a clock source.

The function [LPTMR\\_DeInit\(\)](#) disables the LPTMR module and gates the module clock.

#### 23.2.2 Timer period Operations

The function [LPTMR\\_SetTimerPeriod\(\)](#) sets the timer period in units of count. Timers counts from 0 to the count value set here.

The function [LPTMR\\_GetCurrentTimerCount\(\)](#) reads the current timer counting value. This function returns the real-time timer counting value ranging from 0 to a timer period.

The timer period operation function takes the count value in ticks. Call the utility macros provided in the `fsl_common.h` file to convert to microseconds or milliseconds.

#### 23.2.3 Start and Stop timer operations

The function [LPTMR\\_StartTimer\(\)](#) starts the timer counting. After calling this function, the timer counts up to the counter value set earlier by using the [LPTMR\\_SetPeriod\(\)](#) function. Each time the timer reaches the count value and increments, it generates a trigger pulse and sets the timeout interrupt flag. An interrupt is also triggered if the timer interrupt is enabled.

The function [LPTMR\\_StopTimer\(\)](#) stops the timer counting and resets the timer's counter register.

## Typical use case

### 23.2.4 Status

Provides functions to get and clear the LPTMR status.

### 23.2.5 Interrupt

Provides functions to enable/disable LPTMR interrupts and get the currently enabled interrupts.

## 23.3 Typical use case

### 23.3.1 LPTMR tick example

Updates the LPTMR period and toggles an LED periodically.

```
int main(void)
{
    uint32_t currentCounter = 0U;
    lptmr_config_t lptmrConfig;

    LED_INIT();

    /* Board pin, clock, debug console initialization */
    BOARD_InitHardware();

    /* Configures the LPTMR */
    LPTMR_GetDefaultConfig(&lptmrConfig);

    /* Initializes the LPTMR */
    LPTMR_Init(LPTMR0, &lptmrConfig);

    /* Sets the timer period */
    LPTMR_SetTimerPeriod(LPTMR0, USEC_TO_COUNT(1000000U, LPTMR_SOURCE_CLOCK));

    /* Enables a timer interrupt */
    LPTMR_EnableInterrupts(LPTMR0,
        kLPTMR_TimerInterruptEnable);

    /* Enables the NVIC */
    EnableIRQ(LPTMR0_IRQn);

    PRINTF("Low Power Timer Example\r\n");

    /* Starts counting */
    LPTMR_StartTimer(LPTMR0);
    while (1)
    {
        if (currentCounter != lptmrCounter)
        {
            currentCounter = lptmrCounter;
            PRINTF("LPTMR interrupt No.%d \r\n", currentCounter);
        }
    }
}
```

## Data Structures

- struct [lptmr\\_config\\_t](#)  
*LPTMR config structure. [More...](#)*



## Enumerations

- enum `lptmr_pin_select_t` {  
`kLPTMR_PinSelectInput_0` = 0x0U,  
`kLPTMR_PinSelectInput_1` = 0x1U,  
`kLPTMR_PinSelectInput_2` = 0x2U,  
`kLPTMR_PinSelectInput_3` = 0x3U }  
*LPTMR pin selection used in pulse counter mode.*
- enum `lptmr_pin_polarity_t` {  
`kLPTMR_PinPolarityActiveHigh` = 0x0U,  
`kLPTMR_PinPolarityActiveLow` = 0x1U }  
*LPTMR pin polarity used in pulse counter mode.*
- enum `lptmr_timer_mode_t` {  
`kLPTMR_TimerModeTimeCounter` = 0x0U,  
`kLPTMR_TimerModePulseCounter` = 0x1U }  
*LPTMR timer mode selection.*
- enum `lptmr_prescaler_glitch_value_t` {  
`kLPTMR_Prescale_Glitch_0` = 0x0U,  
`kLPTMR_Prescale_Glitch_1` = 0x1U,  
`kLPTMR_Prescale_Glitch_2` = 0x2U,  
`kLPTMR_Prescale_Glitch_3` = 0x3U,  
`kLPTMR_Prescale_Glitch_4` = 0x4U,  
`kLPTMR_Prescale_Glitch_5` = 0x5U,  
`kLPTMR_Prescale_Glitch_6` = 0x6U,  
`kLPTMR_Prescale_Glitch_7` = 0x7U,  
`kLPTMR_Prescale_Glitch_8` = 0x8U,  
`kLPTMR_Prescale_Glitch_9` = 0x9U,  
`kLPTMR_Prescale_Glitch_10` = 0xAU,  
`kLPTMR_Prescale_Glitch_11` = 0xBU,  
`kLPTMR_Prescale_Glitch_12` = 0xCU,  
`kLPTMR_Prescale_Glitch_13` = 0xDU,  
`kLPTMR_Prescale_Glitch_14` = 0xEU,  
`kLPTMR_Prescale_Glitch_15` = 0xFU }  
*LPTMR prescaler/glitch filter values.*
- enum `lptmr_prescaler_clock_select_t` {  
`kLPTMR_PrescalerClock_0` = 0x0U,  
`kLPTMR_PrescalerClock_1` = 0x1U,  
`kLPTMR_PrescalerClock_2` = 0x2U,  
`kLPTMR_PrescalerClock_3` = 0x3U }  
*LPTMR prescaler/glitch filter clock select.*
- enum `lptmr_interrupt_enable_t` { `kLPTMR_TimerInterruptEnable` = `LPTMR_CSR_TIE_MASK` }  
*List of the LPTMR interrupts.*
- enum `lptmr_status_flags_t` { `kLPTMR_TimerCompareFlag` = `LPTMR_CSR_TCF_MASK` }  
*List of the LPTMR status flags.*

## Driver version

- #define `FSL_LPTMR_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 0)`)

Version 2.0.0.

### Initialization and deinitialization

- void [LPTMR\\_Init](#) (LPTMR\_Type \*base, const [lptmr\\_config\\_t](#) \*config)  
*Ungates the LPTMR clock and configures the peripheral for a basic operation.*
- void [LPTMR\\_Deinit](#) (LPTMR\_Type \*base)  
*Gates the LPTMR clock.*
- void [LPTMR\\_GetDefaultConfig](#) ([lptmr\\_config\\_t](#) \*config)  
*Fills in the LPTMR configuration structure with default settings.*

### Interrupt Interface

- static void [LPTMR\\_EnableInterrupts](#) (LPTMR\_Type \*base, uint32\_t mask)  
*Enables the selected LPTMR interrupts.*
- static void [LPTMR\\_DisableInterrupts](#) (LPTMR\_Type \*base, uint32\_t mask)  
*Disables the selected LPTMR interrupts.*
- static uint32\_t [LPTMR\\_GetEnabledInterrupts](#) (LPTMR\_Type \*base)  
*Gets the enabled LPTMR interrupts.*

### Status Interface

- static uint32\_t [LPTMR\\_GetStatusFlags](#) (LPTMR\_Type \*base)  
*Gets the LPTMR status flags.*
- static void [LPTMR\\_ClearStatusFlags](#) (LPTMR\_Type \*base, uint32\_t mask)  
*Clears the LPTMR status flags.*

### Read and write the timer period

- static void [LPTMR\\_SetTimerPeriod](#) (LPTMR\_Type \*base, uint16\_t ticks)  
*Sets the timer period in units of count.*
- static uint16\_t [LPTMR\\_GetCurrentTimerCount](#) (LPTMR\_Type \*base)  
*Reads the current timer counting value.*

### Timer Start and Stop

- static void [LPTMR\\_StartTimer](#) (LPTMR\_Type \*base)  
*Starts the timer.*
- static void [LPTMR\\_StopTimer](#) (LPTMR\_Type \*base)  
*Stops the timer.*

## 23.4 Data Structure Documentation

### 23.4.1 struct [lptmr\\_config\\_t](#)

This structure holds the configuration settings for the LPTMR peripheral. To initialize this structure to reasonable defaults, call the [LPTMR\\_GetDefaultConfig\(\)](#) function and pass a pointer to your configuration structure instance.

The configuration struct can be made constant so it resides in flash.

## Data Fields

- [lptmr\\_timer\\_mode\\_t timerMode](#)  
*Time counter mode or pulse counter mode.*
- [lptmr\\_pin\\_select\\_t pinSelect](#)  
*LPTMR pulse input pin select; used only in pulse counter mode.*
- [lptmr\\_pin\\_polarity\\_t pinPolarity](#)  
*LPTMR pulse input pin polarity; used only in pulse counter mode.*
- bool [enableFreeRunning](#)  
*True: enable free running, counter is reset on overflow False: counter is reset when the compare flag is set.*
- bool [bypassPrescaler](#)  
*True: bypass prescaler; false: use clock from prescaler.*
- [lptmr\\_prescaler\\_clock\\_select\\_t prescalerClockSource](#)  
*LPTMR clock source.*
- [lptmr\\_prescaler\\_glitch\\_value\\_t value](#)  
*Prescaler or glitch filter value.*

## 23.5 Enumeration Type Documentation

### 23.5.1 enum lptmr\_pin\_select\_t

Enumerator

***kLPTMR\_PinSelectInput\_0*** Pulse counter input 0 is selected.  
***kLPTMR\_PinSelectInput\_1*** Pulse counter input 1 is selected.  
***kLPTMR\_PinSelectInput\_2*** Pulse counter input 2 is selected.  
***kLPTMR\_PinSelectInput\_3*** Pulse counter input 3 is selected.

### 23.5.2 enum lptmr\_pin\_polarity\_t

Enumerator

***kLPTMR\_PinPolarityActiveHigh*** Pulse Counter input source is active-high.  
***kLPTMR\_PinPolarityActiveLow*** Pulse Counter input source is active-low.

### 23.5.3 enum lptmr\_timer\_mode\_t

Enumerator

***kLPTMR\_TimerModeTimeCounter*** Time Counter mode.  
***kLPTMR\_TimerModePulseCounter*** Pulse Counter mode.

### 23.5.4 enum lptmr\_prescaler\_glitch\_value\_t

Enumerator

|                                         |                                                                  |
|-----------------------------------------|------------------------------------------------------------------|
| <b><i>kLPTMR_Prescale_Glitch_0</i></b>  | Prescaler divide 2, glitch filter does not support this setting. |
| <b><i>kLPTMR_Prescale_Glitch_1</i></b>  | Prescaler divide 4, glitch filter 2.                             |
| <b><i>kLPTMR_Prescale_Glitch_2</i></b>  | Prescaler divide 8, glitch filter 4.                             |
| <b><i>kLPTMR_Prescale_Glitch_3</i></b>  | Prescaler divide 16, glitch filter 8.                            |
| <b><i>kLPTMR_Prescale_Glitch_4</i></b>  | Prescaler divide 32, glitch filter 16.                           |
| <b><i>kLPTMR_Prescale_Glitch_5</i></b>  | Prescaler divide 64, glitch filter 32.                           |
| <b><i>kLPTMR_Prescale_Glitch_6</i></b>  | Prescaler divide 128, glitch filter 64.                          |
| <b><i>kLPTMR_Prescale_Glitch_7</i></b>  | Prescaler divide 256, glitch filter 128.                         |
| <b><i>kLPTMR_Prescale_Glitch_8</i></b>  | Prescaler divide 512, glitch filter 256.                         |
| <b><i>kLPTMR_Prescale_Glitch_9</i></b>  | Prescaler divide 1024, glitch filter 512.                        |
| <b><i>kLPTMR_Prescale_Glitch_10</i></b> | Prescaler divide 2048 glitch filter 1024.                        |
| <b><i>kLPTMR_Prescale_Glitch_11</i></b> | Prescaler divide 4096, glitch filter 2048.                       |
| <b><i>kLPTMR_Prescale_Glitch_12</i></b> | Prescaler divide 8192, glitch filter 4096.                       |
| <b><i>kLPTMR_Prescale_Glitch_13</i></b> | Prescaler divide 16384, glitch filter 8192.                      |
| <b><i>kLPTMR_Prescale_Glitch_14</i></b> | Prescaler divide 32768, glitch filter 16384.                     |
| <b><i>kLPTMR_Prescale_Glitch_15</i></b> | Prescaler divide 65536, glitch filter 32768.                     |

### 23.5.5 enum lptmr\_prescaler\_clock\_select\_t

Note

Clock connections are SoC-specific

Enumerator

|                                       |                                           |
|---------------------------------------|-------------------------------------------|
| <b><i>kLPTMR_PrescalerClock_0</i></b> | Prescaler/glitch filter clock 0 selected. |
| <b><i>kLPTMR_PrescalerClock_1</i></b> | Prescaler/glitch filter clock 1 selected. |
| <b><i>kLPTMR_PrescalerClock_2</i></b> | Prescaler/glitch filter clock 2 selected. |
| <b><i>kLPTMR_PrescalerClock_3</i></b> | Prescaler/glitch filter clock 3 selected. |

### 23.5.6 enum lptmr\_interrupt\_enable\_t

Enumerator

|                                           |                         |
|-------------------------------------------|-------------------------|
| <b><i>kLPTMR_TimerInterruptEnable</i></b> | Timer interrupt enable. |
|-------------------------------------------|-------------------------|

### 23.5.7 enum lptmr\_status\_flags\_t

Enumerator

***kLPTMR\_TimerCompareFlag*** Timer compare flag.

## 23.6 Function Documentation

### 23.6.1 void LPTMR\_Init ( LPTMR\_Type \* *base*, const lptmr\_config\_t \* *config* )

Note

This API should be called at the beginning of the application using the LPTMR driver.

Parameters

|               |                                                 |
|---------------|-------------------------------------------------|
| <i>base</i>   | LPTMR peripheral base address                   |
| <i>config</i> | A pointer to the LPTMR configuration structure. |

### 23.6.2 void LPTMR\_Deinit ( LPTMR\_Type \* *base* )

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

### 23.6.3 void LPTMR\_GetDefaultConfig ( lptmr\_config\_t \* *config* )

The default values are as follows.

```
* config->timerMode = kLPTMR_TimerModeTimeCounter;
* config->pinSelect = kLPTMR_PinSelectInput_0;
* config->pinPolarity = kLPTMR_PinPolarityActiveHigh;
* config->enableFreeRunning = false;
* config->bypassPrescaler = true;
* config->prescalerClockSource = kLPTMR_PrescalerClock_1;
* config->value = kLPTMR_Prescale_Glitch_0;
*
```

Parameters

|               |                                                 |
|---------------|-------------------------------------------------|
| <i>config</i> | A pointer to the LPTMR configuration structure. |
|---------------|-------------------------------------------------|

### 23.6.4 static void LPTMR\_EnableInterrupts ( LPTMR\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

## Function Documentation

### Parameters

|             |                                                                                                                        |
|-------------|------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPTMR peripheral base address                                                                                          |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">lptmr-_interrupt_enable_t</a> |

**23.6.5 static void LPTMR\_DisableInterrupts ( LPTMR\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

### Parameters

|             |                                                                                                                           |
|-------------|---------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPTMR peripheral base address                                                                                             |
| <i>mask</i> | The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">lptmr-_interrupt_enable_t</a> . |

**23.6.6 static uint32\_t LPTMR\_GetEnabledInterrupts ( LPTMR\_Type \* *base* ) [inline], [static]**

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

### Returns

The enabled interrupts. This is the logical OR of members of the enumeration [lptmr\\_interrupt\\_enable\\_t](#)

**23.6.7 static uint32\_t LPTMR\_GetStatusFlags ( LPTMR\_Type \* *base* ) [inline], [static]**

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

### Returns

The status flags. This is the logical OR of members of the enumeration [lptmr\\_status\\_flags\\_t](#)

**23.6.8** `static void LPTMR_ClearStatusFlags ( LPTMR_Type * base, uint32_t mask  
 ) [inline], [static]`

## Function Documentation

### Parameters

|             |                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPTMR peripheral base address                                                                                        |
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">lptmr_status_flags_t</a> . |

### 23.6.9 static void LPTMR\_SetTimerPeriod ( LPTMR\_Type \* *base*, uint16\_t *ticks* ) [inline], [static]

Timers counts from 0 until it equals the count value set here. The count value is written to the CMR register.

#### Note

1. The TCF flag is set with the CNR equals the count provided here and then increments.
2. Call the utility macros provided in the fsl\_common.h to convert to ticks.

### Parameters

|              |                                                                            |
|--------------|----------------------------------------------------------------------------|
| <i>base</i>  | LPTMR peripheral base address                                              |
| <i>ticks</i> | A timer period in units of ticks, which should be equal or greater than 1. |

### 23.6.10 static uint16\_t LPTMR\_GetCurrentTimerCount ( LPTMR\_Type \* *base* ) [inline], [static]

This function returns the real-time timer counting value in a range from 0 to a timer period.

#### Note

Call the utility macros provided in the fsl\_common.h to convert ticks to usec or msec.

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

### Returns

The current counter value in ticks



### 23.6.11 static void LPTMR\_StartTimer ( LPTMR\_Type \* *base* ) [inline], [static]

After calling this function, the timer counts up to the CMR register value. Each time the timer reaches the CMR value and then increments, it generates a trigger pulse and sets the timeout interrupt flag. An interrupt is also triggered if the timer interrupt is enabled.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

### 23.6.12 static void LPTMR\_StopTimer ( LPTMR\_Type \* *base* ) [inline], [static]

This function stops the timer and resets the timer's counter register.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|





## Chapter 24

### LPUART: Low Power UART Driver

#### 24.1 Overview

##### Modules

- [LPUART DMA Driver](#)
- [LPUART Driver](#)
- [LPUART FreeRTOS Driver](#)
- [LPUART eDMA Driver](#)
- [LPUART  \$\mu\$ COS/II Driver](#)
- [LPUART  \$\mu\$ COS/III Driver](#)

## LPUART Driver

### 24.2 LPUART Driver

#### 24.2.1 Overview

The KSDK provides a peripheral driver for the Low Power UART (LPUART) module of Kinetis devices.

#### 24.2.2 Typical use case

##### 24.2.2.1 LPUART Operation

```
uint8_t ch;
LPUART_GetDefaultConfig(&user_config);
user_config.baudRate = 115200U;
config.enableTx = true;
config.enableRx = true;

LPUART_Init(LPUART1, &user_config, 120000000U);

LPUART_WriteBlocking(LPUART1, txbuff, sizeof(txbuff) - 1);

while(1)
{
    LPUART_ReadBlocking(LPUART1, &ch, 1);
    LPUART_WriteBlocking(LPUART1, &ch, 1);
}
```

## Data Structures

- struct [lpuart\\_config\\_t](#)  
*LPUART configuration structure. [More...](#)*
- struct [lpuart\\_transfer\\_t](#)  
*LPUART transfer structure. [More...](#)*
- struct [lpuart\\_handle\\_t](#)  
*LPUART handle structure. [More...](#)*

## Typedefs

- typedef void(\* [lpuart\\_transfer\\_callback\\_t](#))(LPUART\_Type \*base, lpuart\_handle\_t \*handle, status\_t status, void \*userData)  
*LPUART transfer callback function.*

## Enumerations

- enum `_lpuart_status` {  
`kStatus_LPUART_TxBusy` = MAKE\_STATUS(kStatusGroup\_LPUART, 0),  
`kStatus_LPUART_RxBusy` = MAKE\_STATUS(kStatusGroup\_LPUART, 1),  
`kStatus_LPUART_TxIdle` = MAKE\_STATUS(kStatusGroup\_LPUART, 2),  
`kStatus_LPUART_RxIdle` = MAKE\_STATUS(kStatusGroup\_LPUART, 3),  
`kStatus_LPUART_TxWatermarkTooLarge` = MAKE\_STATUS(kStatusGroup\_LPUART, 4),  
`kStatus_LPUART_RxWatermarkTooLarge` = MAKE\_STATUS(kStatusGroup\_LPUART, 5),  
`kStatus_LPUART_FlagCannotClearManually` = MAKE\_STATUS(kStatusGroup\_LPUART, 6),  
`kStatus_LPUART_Error` = MAKE\_STATUS(kStatusGroup\_LPUART, 7),  
`kStatus_LPUART_RxRingBufferOverflow`,  
`kStatus_LPUART_RxHardwareOverflow` = MAKE\_STATUS(kStatusGroup\_LPUART, 9),  
`kStatus_LPUART_NoiseError` = MAKE\_STATUS(kStatusGroup\_LPUART, 10),  
`kStatus_LPUART_FramingError` = MAKE\_STATUS(kStatusGroup\_LPUART, 11),  
`kStatus_LPUART_ParityError` = MAKE\_STATUS(kStatusGroup\_LPUART, 12),  
`kStatus_LPUART_BaudrateNotSupport` }  
*Error codes for the LPUART driver.*
- enum `lpuart_parity_mode_t` {  
`kLPUART_ParityDisabled` = 0x0U,  
`kLPUART_ParityEven` = 0x2U,  
`kLPUART_ParityOdd` = 0x3U }  
*LPUART parity mode.*
- enum `lpuart_data_bits_t` { `kLPUART_EightDataBits` = 0x0U }  
*LPUART data bits count.*
- enum `lpuart_stop_bit_count_t` {  
`kLPUART_OneStopBit` = 0U,  
`kLPUART_TwoStopBit` = 1U }  
*LPUART stop bit count.*
- enum `_lpuart_interrupt_enable` {  
`kLPUART_LinBreakInterruptEnable` = (LPUART\_BAUD\_LBKDIE\_MASK >> 8),  
`kLPUART_RxActiveEdgeInterruptEnable` = (LPUART\_BAUD\_RXEDGIE\_MASK >> 8),  
`kLPUART_TxDataRegEmptyInterruptEnable` = (LPUART\_CTRL\_TIE\_MASK),  
`kLPUART_TransmissionCompleteInterruptEnable` = (LPUART\_CTRL\_TCIE\_MASK),  
`kLPUART_RxDataRegFullInterruptEnable` = (LPUART\_CTRL\_RIE\_MASK),  
`kLPUART_IdleLineInterruptEnable` = (LPUART\_CTRL\_ILIE\_MASK),  
`kLPUART_RxOverflowInterruptEnable` = (LPUART\_CTRL\_ORIE\_MASK),  
`kLPUART_NoiseErrorInterruptEnable` = (LPUART\_CTRL\_NEIE\_MASK),  
`kLPUART_FramingErrorInterruptEnable` = (LPUART\_CTRL\_FEIE\_MASK),  
`kLPUART_ParityErrorInterruptEnable` = (LPUART\_CTRL\_PEIE\_MASK) }  
*LPUART interrupt configuration structure, default settings all disabled.*
- enum `_lpuart_flags` {

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```
kLPUART_TxDataRegEmptyFlag,  
kLPUART_TransmissionCompleteFlag,  
kLPUART_RxDataRegFullFlag,  
kLPUART_IdleLineFlag = (LPUART_STAT_IDLE_MASK),  
kLPUART_RxOverrunFlag = (LPUART_STAT_OR_MASK),  
kLPUART_NoiseErrorFlag = (LPUART_STAT_NF_MASK),  
kLPUART_FramingErrorFlag,  
kLPUART_ParityErrorFlag = (LPUART_STAT_PF_MASK),  
kLPUART_LinBreakFlag = (LPUART_STAT_LBKDIF_MASK),  
kLPUART_RxActiveEdgeFlag,  
kLPUART_RxActiveFlag,  
kLPUART_DataMatch1Flag = LPUART_STAT_MA1F_MASK,  
kLPUART_DataMatch2Flag = LPUART_STAT_MA2F_MASK,  
kLPUART_NoiseErrorInRxDataRegFlag,  
kLPUART_ParityErrorInRxDataRegFlag }
```

*LPUART status flags.*

## Driver version

- #define **FSL\_LPUART\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 2, 3))  
*LPUART driver version 2.2.1.*

## Initialization and deinitialization

- status\_t **LPUART\_Init** (LPUART\_Type \*base, const **lpuart\_config\_t** \*config, uint32\_t srcClock\_Hz)  
*Initializes an LPUART instance with the user configuration structure and the peripheral clock.*
- void **LPUART\_Deinit** (LPUART\_Type \*base)  
*Deinitializes a LPUART instance.*
- void **LPUART\_GetDefaultConfig** (**lpuart\_config\_t** \*config)  
*Gets the default configuration structure.*
- status\_t **LPUART\_SetBaudRate** (LPUART\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Sets the LPUART instance baudrate.*

## Status

- uint32\_t **LPUART\_GetStatusFlags** (LPUART\_Type \*base)  
*Gets LPUART status flags.*
- status\_t **LPUART\_ClearStatusFlags** (LPUART\_Type \*base, uint32\_t mask)  
*Clears status flags with a provided mask.*

## Interrupts

- void [LPUART\\_EnableInterrupts](#) (LPUART\_Type \*base, uint32\_t mask)  
*Enables LPUART interrupts according to a provided mask.*
- void [LPUART\\_DisableInterrupts](#) (LPUART\_Type \*base, uint32\_t mask)  
*Disables LPUART interrupts according to a provided mask.*
- uint32\_t [LPUART\\_GetEnabledInterrupts](#) (LPUART\_Type \*base)  
*Gets enabled LPUART interrupts.*
- static uint32\_t [LPUART\\_GetDataRegisterAddress](#) (LPUART\_Type \*base)  
*Gets the LPUART data register address.*
- static void [LPUART\\_EnableTxDMA](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART transmitter DMA request.*
- static void [LPUART\\_EnableRxDMA](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART receiver DMA.*

## Bus Operations

- static void [LPUART\\_EnableTx](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART transmitter.*
- static void [LPUART\\_EnableRx](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART receiver.*
- static void [LPUART\\_WriteByte](#) (LPUART\_Type \*base, uint8\_t data)  
*Writes to the transmitter register.*
- static uint8\_t [LPUART\\_ReadByte](#) (LPUART\_Type \*base)  
*Reads the receiver register.*
- void [LPUART\\_WriteBlocking](#) (LPUART\_Type \*base, const uint8\_t \*data, size\_t length)  
*Writes to the transmitter register using a blocking method.*
- status\_t [LPUART\\_ReadBlocking](#) (LPUART\_Type \*base, uint8\_t \*data, size\_t length)  
*Reads the receiver data register using a blocking method.*

## Transactional

- void [LPUART\\_TransferCreateHandle](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, [lpuart\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the LPUART handle.*
- status\_t [LPUART\\_TransferSendNonBlocking](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, [lpuart\\_transfer\\_t](#) \*xfer)  
*Transmits a buffer of data using the interrupt method.*
- void [LPUART\\_TransferStartRingBuffer](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, uint8\_t \*ringBuffer, size\_t ringBufferSize)  
*Sets up the RX ring buffer.*
- void [LPUART\\_TransferStopRingBuffer](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle)  
*Aborts the background transfer and uninstalls the ring buffer.*
- void [LPUART\\_TransferAbortSend](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle)  
*Aborts the interrupt-driven data transmit.*
- status\_t [LPUART\\_TransferGetSendCount](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes that have been written to the LPUART transmitter register.*

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- status\_t [LPUART\\_TransferReceiveNonBlocking](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, lpuart\_transfer\_t \*xfer, size\_t \*receivedBytes)  
*Receives a buffer of data using the interrupt method.*
- void [LPUART\\_TransferAbortReceive](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle)  
*Aborts the interrupt-driven data receiving.*
- status\_t [LPUART\\_TransferGetReceiveCount](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes that have been received.*
- void [LPUART\\_TransferHandleIRQ](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle)  
*LPUART IRQ handle function.*
- void [LPUART\\_TransferHandleErrorIRQ](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle)  
*LPUART Error IRQ handle function.*

### 24.2.3 Data Structure Documentation

#### 24.2.3.1 struct lpuart\_config\_t

##### Data Fields

- uint32\_t [baudRate\\_Bps](#)  
*LPUART baud rate.*
- lpuart\_parity\_mode\_t [parityMode](#)  
*Parity mode, disabled (default), even, odd.*
- lpuart\_data\_bits\_t [dataBitsCount](#)  
*Data bits count, eight (default), seven.*
- bool [isMsb](#)  
*Data bits order, LSB (default), MSB.*
- lpuart\_stop\_bit\_count\_t [stopBitCount](#)  
*Number of stop bits, 1 stop bit (default) or 2 stop bits.*
- bool [enableTx](#)  
*Enable TX.*
- bool [enableRx](#)  
*Enable RX.*

#### 24.2.3.2 struct lpuart\_transfer\_t

##### Data Fields

- uint8\_t \* [data](#)  
*The buffer of data to be transfer.*
- size\_t [dataSize](#)  
*The byte count to be transfer.*



### 24.2.3.2.0.65 Field Documentation

24.2.3.2.0.65.1 `uint8_t* lpuart_transfer_t::data`

24.2.3.2.0.65.2 `size_t lpuart_transfer_t::dataSize`

### 24.2.3.3 `struct _lpuart_handle`

#### Data Fields

- `uint8_t *volatile txData`  
*Address of remaining data to send.*
- `volatile size_t txDataSize`  
*Size of the remaining data to send.*
- `size_t txDataSizeAll`  
*Size of the data to send out.*
- `uint8_t *volatile rxData`  
*Address of remaining data to receive.*
- `volatile size_t rxDataSize`  
*Size of the remaining data to receive.*
- `size_t rxDataSizeAll`  
*Size of the data to receive.*
- `uint8_t * rxRingBuffer`  
*Start address of the receiver ring buffer.*
- `size_t rxRingBufferSize`  
*Size of the ring buffer.*
- `volatile uint16_t rxRingBufferHead`  
*Index for the driver to store received data into ring buffer.*
- `volatile uint16_t rxRingBufferTail`  
*Index for the user to get data from the ring buffer.*
- `lpuart_transfer_callback_t callback`  
*Callback function.*
- `void * userData`  
*LPUART callback function parameter.*
- `volatile uint8_t txState`  
*TX transfer state.*
- `volatile uint8_t rxState`  
*RX transfer state.*

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### 24.2.3.3.0.66 Field Documentation

- 24.2.3.3.0.66.1 `uint8_t* volatile lpuart_handle_t::txData`
- 24.2.3.3.0.66.2 `volatile size_t lpuart_handle_t::txDataSize`
- 24.2.3.3.0.66.3 `size_t lpuart_handle_t::txDataSizeAll`
- 24.2.3.3.0.66.4 `uint8_t* volatile lpuart_handle_t::rxData`
- 24.2.3.3.0.66.5 `volatile size_t lpuart_handle_t::rxDataSize`
- 24.2.3.3.0.66.6 `size_t lpuart_handle_t::rxDataSizeAll`
- 24.2.3.3.0.66.7 `uint8_t* lpuart_handle_t::rxRingBuffer`
- 24.2.3.3.0.66.8 `size_t lpuart_handle_t::rxRingBufferSize`
- 24.2.3.3.0.66.9 `volatile uint16_t lpuart_handle_t::rxRingBufferHead`
- 24.2.3.3.0.66.10 `volatile uint16_t lpuart_handle_t::rxRingBufferTail`
- 24.2.3.3.0.66.11 `lpuart_transfer_callback_t lpuart_handle_t::callback`
- 24.2.3.3.0.66.12 `void* lpuart_handle_t::userData`
- 24.2.3.3.0.66.13 `volatile uint8_t lpuart_handle_t::txState`
- 24.2.3.3.0.66.14 `volatile uint8_t lpuart_handle_t::rxState`

### 24.2.4 Macro Definition Documentation

- 24.2.4.1 `#define FSL_LPUART_DRIVER_VERSION (MAKE_VERSION(2, 2, 3))`

### 24.2.5 Typedef Documentation

- 24.2.5.1 `typedef void(* lpuart_transfer_callback_t)(LPUART_Type *base, lpuart_handle_t *handle, status_t status, void *userData)`

### 24.2.6 Enumeration Type Documentation

#### 24.2.6.1 `enum _lpuart_status`

Enumerator

- kStatus\_LPUART\_TxBusy* TX busy.
- kStatus\_LPUART\_RxBusy* RX busy.
- kStatus\_LPUART\_TxIdle* LPUART transmitter is idle.

*kStatus\_LPUART\_RxIdle* LPUART receiver is idle.  
*kStatus\_LPUART\_TxWatermarkTooLarge* TX FIFO watermark too large.  
*kStatus\_LPUART\_RxWatermarkTooLarge* RX FIFO watermark too large.  
*kStatus\_LPUART\_FlagCannotClearManually* Some flag can't manually clear.  
*kStatus\_LPUART\_Error* Error happens on LPUART.  
*kStatus\_LPUART\_RxRingBufferOverflow* LPUART RX software ring buffer overrun.  
*kStatus\_LPUART\_RxHardwareOverflow* LPUART RX receiver overrun.  
*kStatus\_LPUART\_NoiseError* LPUART noise error.  
*kStatus\_LPUART\_FramingError* LPUART framing error.  
*kStatus\_LPUART\_ParityError* LPUART parity error.  
*kStatus\_LPUART\_BaudrateNotSupport* Baudrate is not support in current clock source.

#### 24.2.6.2 enum lpuart\_parity\_mode\_t

Enumerator

*kLPUART\_ParityDisabled* Parity disabled.  
*kLPUART\_ParityEven* Parity enabled, type even, bit setting: PE|PT = 10.  
*kLPUART\_ParityOdd* Parity enabled, type odd, bit setting: PE|PT = 11.

#### 24.2.6.3 enum lpuart\_data\_bits\_t

Enumerator

*kLPUART\_EightDataBits* Eight data bit.

#### 24.2.6.4 enum lpuart\_stop\_bit\_count\_t

Enumerator

*kLPUART\_OneStopBit* One stop bit.  
*kLPUART\_TwoStopBit* Two stop bits.

#### 24.2.6.5 enum \_lpuart\_interrupt\_enable

This structure contains the settings for all LPUART interrupt configurations.

Enumerator

*kLPUART\_LinBreakInterruptEnable* LIN break detect.  
*kLPUART\_RxActiveEdgeInterruptEnable* Receive Active Edge.  
*kLPUART\_TxDataRegEmptyInterruptEnable* Transmit data register empty.

***kLPUART\_TransmissionCompleteInterruptEnable*** Transmission complete.  
***kLPUART\_RxDataRegFullInterruptEnable*** Receiver data register full.  
***kLPUART\_IdleLineInterruptEnable*** Idle line.  
***kLPUART\_RxOverrunInterruptEnable*** Receiver Overrun.  
***kLPUART\_NoiseErrorInterruptEnable*** Noise error flag.  
***kLPUART\_FramingErrorInterruptEnable*** Framing error flag.  
***kLPUART\_ParityErrorInterruptEnable*** Parity error flag.

### 24.2.6.6 enum \_lpuart\_flags

This provides constants for the LPUART status flags for use in the LPUART functions.

Enumerator

***kLPUART\_TxDataRegEmptyFlag*** Transmit data register empty flag, sets when transmit buffer is empty.  
***kLPUART\_TransmissionCompleteFlag*** Transmission complete flag, sets when transmission activity complete.  
***kLPUART\_RxDataRegFullFlag*** Receive data register full flag, sets when the receive data buffer is full.  
***kLPUART\_IdleLineFlag*** Idle line detect flag, sets when idle line detected.  
***kLPUART\_RxOverrunFlag*** Receive Overrun, sets when new data is received before data is read from receive register.  
***kLPUART\_NoiseErrorFlag*** Receive takes 3 samples of each received bit. If any of these samples differ, noise flag sets  
***kLPUART\_FramingErrorFlag*** Frame error flag, sets if logic 0 was detected where stop bit expected.  
***kLPUART\_ParityErrorFlag*** If parity enabled, sets upon parity error detection.  
***kLPUART\_LinBreakFlag*** LIN break detect interrupt flag, sets when LIN break char detected and LIN circuit enabled.  
***kLPUART\_RxActiveEdgeFlag*** Receive pin active edge interrupt flag, sets when active edge detected.  
***kLPUART\_RxActiveFlag*** Receiver Active Flag (RAF), sets at beginning of valid start bit.  
***kLPUART\_DataMatch1Flag*** The next character to be read from LPUART\_DATA matches MA1.  
***kLPUART\_DataMatch2Flag*** The next character to be read from LPUART\_DATA matches MA2.  
***kLPUART\_NoiseErrorInRxDataRegFlag*** NOISY bit, sets if noise detected in current data word.  
***kLPUART\_ParityErrorInRxDataRegFlag*** PARITYE bit, sets if noise detected in current data word.

## 24.2.7 Function Documentation

### 24.2.7.1 `status_t LPUART_Init ( LPUART_Type * base, const lpuart_config_t * config, uint32_t srcClock_Hz )`

This function configures the LPUART module with user-defined settings. Call the [LPUART\\_GetDefaultConfig\(\)](#) function to configure the configuration structure and get the default configuration. The example below shows how to use this API to configure the LPUART.

```
* lpuart_config_t lpuartConfig;
* lpuartConfig.baudRate_Bps = 115200U;
* lpuartConfig.parityMode = kLPUART_ParityDisabled;
* lpuartConfig.dataBitsCount = kLPUART_EightDataBits;
* lpuartConfig.isMsb = false;
* lpuartConfig.stopBitCount = kLPUART_OneStopBit;
* lpuartConfig.txFifoWatermark = 0;
* lpuartConfig.rxFifoWatermark = 1;
* LPUART_Init(LPUART1, &lpuartConfig, 20000000U);
*
```

#### Parameters

|                    |                                                    |
|--------------------|----------------------------------------------------|
| <i>base</i>        | LPUART peripheral base address.                    |
| <i>config</i>      | Pointer to a user-defined configuration structure. |
| <i>srcClock_Hz</i> | LPUART clock source frequency in HZ.               |

#### Return values

|                                           |                                                  |
|-------------------------------------------|--------------------------------------------------|
| <i>kStatus_LPUART_-BaudrateNotSupport</i> | Baudrate is not support in current clock source. |
| <i>kStatus_Success</i>                    | LPUART initialize succeed                        |

### 24.2.7.2 `void LPUART_Deinit ( LPUART_Type * base )`

This function waits for transmit to complete, disables TX and RX, and disables the LPUART clock.

#### Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

### 24.2.7.3 `void LPUART_GetDefaultConfig ( lpuart_config_t * config )`

This function initializes the LPUART configuration structure to a default value. The default values are:  
: lpuartConfig->baudRate\_Bps = 115200U; lpuartConfig->parityMode = kLPUART\_ParityDisabled;

---

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```
lpuartConfig->dataBitsCount = kLPUART_EightDataBits; lpuartConfig->isMsb = false; lpuartConfig->stopBitCount = kLPUART_OneStopBit; lpuartConfig->txFifoWatermark = 0; lpuartConfig->rxFifoWatermark = 1; lpuartConfig->enableTx = false; lpuartConfig->enableRx = false;
```

## Parameters

|               |                                       |
|---------------|---------------------------------------|
| <i>config</i> | Pointer to a configuration structure. |
|---------------|---------------------------------------|

#### 24.2.7.4 status\_t LPUART\_SetBaudRate ( LPUART\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClock\_Hz* )

This function configures the LPUART module baudrate. This function is used to update the LPUART module baudrate after the LPUART module is initialized by the LPUART\_Init.

```
* LPUART_SetBaudRate(LPUART1, 115200U, 200000000U);
*
```

## Parameters

|                     |                                      |
|---------------------|--------------------------------------|
| <i>base</i>         | LPUART peripheral base address.      |
| <i>baudRate_Bps</i> | LPUART baudrate to be set.           |
| <i>srcClock_Hz</i>  | LPUART clock source frequency in HZ. |

## Return values

|                                           |                                                        |
|-------------------------------------------|--------------------------------------------------------|
| <i>kStatus_LPUART_-BaudrateNotSupport</i> | Baudrate is not supported in the current clock source. |
| <i>kStatus_Success</i>                    | Set baudrate succeeded.                                |

#### 24.2.7.5 uint32\_t LPUART\_GetStatusFlags ( LPUART\_Type \* *base* )

This function gets all LPUART status flags. The flags are returned as the logical OR value of the enumerators [\\_lpuart\\_flags](#). To check for a specific status, compare the return value with enumerators in the [\\_lpuart\\_flags](#). For example, to check whether the TX is empty:

```
* if (kLPUART_TxDataRegEmptyFlag &
*    LPUART_GetStatusFlags(LPUART1))
* {
*     ...
* }
*
```

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### Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

### Returns

LPUART status flags which are ORed by the enumerators in the `_lpuart_flags`.

#### 24.2.7.6 `status_t LPUART_ClearStatusFlags ( LPUART_Type * base, uint32_t mask )`

This function clears LPUART status flags with a provided mask. Automatically cleared flags can't be cleared by this function. Flags that can only be cleared or set by hardware are: `kLPUART_TxDataRegEmptyFlag`, `kLPUART_TransmissionCompleteFlag`, `kLPUART_RxDataRegFullFlag`, `kLPUART_RxActiveFlag`, `kLPUART_NoiseErrorInRxDataRegFlag`, `kLPUART_ParityErrorInRxDataRegFlag`, `kLPUART_TxFifoEmptyFlag`, `kLPUART_RxFifoEmptyFlag`. Note: This API should be called when the Tx/Rx is idle, otherwise it takes no effects.

### Parameters

|             |                                                                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPUART peripheral base address.                                                                                                                     |
| <i>mask</i> | the status flags to be cleared. The user can use the enumerators in the <code>_lpuart_status_flag_t</code> to do the OR operation and get the mask. |

### Returns

0 succeed, others failed.

### Return values

|                                               |                                                                                         |
|-----------------------------------------------|-----------------------------------------------------------------------------------------|
| <i>kStatus_LPUART_FlagCannotClearManually</i> | The flag can't be cleared by this function but it is cleared automatically by hardware. |
| <i>kStatus_Success</i>                        | Status in the mask are cleared.                                                         |

#### 24.2.7.7 `void LPUART_EnableInterrupts ( LPUART_Type * base, uint32_t mask )`

This function enables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See the [\\_lpuart\\_interrupt\\_enable](#). This example shows how to enable TX empty interrupt and RX full interrupt:

```
* LPUART_EnableInterrupts(LPUART1,  
* kLPUART_TxDataRegEmptyInterruptEnable |  
* kLPUART_RxDataRegFullInterruptEnable);
```



## Parameters

|             |                                                                                  |
|-------------|----------------------------------------------------------------------------------|
| <i>base</i> | LPUART peripheral base address.                                                  |
| <i>mask</i> | The interrupts to enable. Logical OR of <a href="#">_uart_interrupt_enable</a> . |

#### 24.2.7.8 void LPUART\_DisableInterrupts ( LPUART\_Type \* *base*, uint32\_t *mask* )

This function disables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See [\\_lpuart\\_interrupt\\_enable](#). This example shows how to disable the TX empty interrupt and RX full interrupt:

```
*  LPUART_DisableInterrupts(LPUART1,
*  kLPUART_TxDataRegEmptyInterruptEnable |
*  kLPUART_RxDataRegFullInterruptEnable);
*
```

## Parameters

|             |                                                                                     |
|-------------|-------------------------------------------------------------------------------------|
| <i>base</i> | LPUART peripheral base address.                                                     |
| <i>mask</i> | The interrupts to disable. Logical OR of <a href="#">_lpuart_interrupt_enable</a> . |

#### 24.2.7.9 uint32\_t LPUART\_GetEnabledInterrupts ( LPUART\_Type \* *base* )

This function gets the enabled LPUART interrupts. The enabled interrupts are returned as the logical OR value of the enumerators [\\_lpuart\\_interrupt\\_enable](#). To check a specific interrupt enable status, compare the return value with enumerators in [\\_lpuart\\_interrupt\\_enable](#). For example, to check whether the TX empty interrupt is enabled:

```
*  uint32_t enabledInterrupts = LPUART_GetEnabledInterrupts(LPUART1);
*
*  if (kLPUART_TxDataRegEmptyInterruptEnable & enabledInterrupts)
*  {
*      ...
*  }
*
```

## Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

## Returns

LPUART interrupt flags which are logical OR of the enumerators in [\\_lpuart\\_interrupt\\_enable](#).

**24.2.7.10** `static uint32_t LPUART_GetDataRegisterAddress ( LPUART_Type * base )`  
`[inline], [static]`

This function returns the LPUART data register address, which is mainly used by the DMA/eDMA.

## Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

## Returns

LPUART data register addresses which are used both by the transmitter and receiver.

#### 24.2.7.11 static void LPUART\_EnableTxDMA ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the transmit data register empty flag, STAT[TDRE], to generate DMA requests.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

#### 24.2.7.12 static void LPUART\_EnableRxDMA ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the receiver data register full flag, STAT[RDRF], to generate DMA requests.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

#### 24.2.7.13 static void LPUART\_EnableTx ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the LPUART transmitter.

## Parameters

---

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|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

### 24.2.7.14 static void LPUART\_EnableRx ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the LPUART receiver.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

### 24.2.7.15 static void LPUART\_WriteByte ( LPUART\_Type \* *base*, uint8\_t *data* ) [inline], [static]

This function writes data to the transmitter register directly. The upper layer must ensure that the TX register is empty or that the TX FIFO has room before calling this function.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
| <i>data</i> | Data write to the TX register.  |

### 24.2.7.16 static uint8\_t LPUART\_ReadByte ( LPUART\_Type \* *base* ) [inline], [static]

This function reads data from the receiver register directly. The upper layer must ensure that the receiver register is full or that the RX FIFO has data before calling this function.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

Data read from data register.

### 24.2.7.17 void LPUART\_WriteBlocking ( LPUART\_Type \* *base*, const uint8\_t \* *data*, size\_t *length* )

This function polls the transmitter register, waits for the register to be empty or for TX FIFO to have room, and writes data to the transmitter buffer.

#### Note

This function does not check whether all data has been sent out to the bus. Before disabling the transmitter, check the kLPUART\_TransmissionCompleteFlag to ensure that the transmit is finished.

#### Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | LPUART peripheral base address.     |
| <i>data</i>   | Start address of the data to write. |
| <i>length</i> | Size of the data to write.          |

### 24.2.7.18 status\_t LPUART\_ReadBlocking ( LPUART\_Type \* *base*, uint8\_t \* *data*, size\_t *length* )

This function polls the receiver register, waits for the receiver register full or receiver FIFO has data, and reads data from the TX register.

#### Parameters

|               |                                                         |
|---------------|---------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                         |
| <i>data</i>   | Start address of the buffer to store the received data. |
| <i>length</i> | Size of the buffer.                                     |

#### Return values

|                                          |                                                 |
|------------------------------------------|-------------------------------------------------|
| <i>kStatus_LPUART_Rx-HardwareOverrun</i> | Receiver overrun happened while receiving data. |
| <i>kStatus_LPUART_Noise-Error</i>        | Noise error happened while receiving data.      |
| <i>kStatus_LPUART_-FramingError</i>      | Framing error happened while receiving data.    |
| <i>kStatus_LPUART_Parity-Error</i>       | Parity error happened while receiving data.     |
| <i>kStatus_Success</i>                   | Successfully received all data.                 |

## LPUART Driver

### 24.2.7.19 void LPUART\_TransferCreateHandle ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle*, lpuart\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the LPUART handle, which can be used for other LPUART transactional APIs. Usually, for a specified LPUART instance, call this API once to get the initialized handle.

The LPUART driver supports the "background" receiving, which means that user can set up an RX ring buffer optionally. Data received is stored into the ring buffer even when the user doesn't call the [LPUART\\_TransferReceiveNonBlocking\(\)](#) API. If there is already data received in the ring buffer, the user can get the received data from the ring buffer directly. The ring buffer is disabled if passing NULL as *ringBuffer*.

Parameters

|                 |                                 |
|-----------------|---------------------------------|
| <i>base</i>     | LPUART peripheral base address. |
| <i>handle</i>   | LPUART handle pointer.          |
| <i>callback</i> | Callback function.              |
| <i>userData</i> | User data.                      |

### 24.2.7.20 status\_t LPUART\_TransferSendNonBlocking ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle*, lpuart\_transfer\_t \* *xfer* )

This function send data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data written to the transmitter register. When all data is written to the TX register in the ISR, the LPUART driver calls the callback function and passes the [kStatus\\_LPUART\\_TxIdle](#) as status parameter.

Note

The [kStatus\\_LPUART\\_TxIdle](#) is passed to the upper layer when all data are written to the TX register. However, there is no check to ensure that all the data sent out. Before disabling the T-X, check the [kLPUART\\_TransmissionCompleteFlag](#) to ensure that the transmit is finished.

Parameters

|               |                                                                    |
|---------------|--------------------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                                    |
| <i>handle</i> | LPUART handle pointer.                                             |
| <i>xfer</i>   | LPUART transfer structure, see <a href="#">lpuart_transfer_t</a> . |

## Return values

|                                |                                                                                    |
|--------------------------------|------------------------------------------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully start the data transmission.                                          |
| <i>kStatus_LPUART_TxBusy</i>   | Previous transmission still not finished, data not all written to the TX register. |
| <i>kStatus_InvalidArgument</i> | Invalid argument.                                                                  |

#### 24.2.7.21 void LPUART\_TransferStartRingBuffer ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle*, uint8\_t \* *ringBuffer*, size\_t *ringBufferSize* )

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received is stored into the ring buffer even when the user doesn't call the [UART\\_TransferReceiveNonBlocking\(\)](#) API. If there is already data received in the ring buffer, the user can get the received data from the ring buffer directly.

## Note

When using RX ring buffer, one byte is reserved for internal use. In other words, if *ringBufferSize* is 32, then only 31 bytes are used for saving data.

## Parameters

|                       |                                                                                              |
|-----------------------|----------------------------------------------------------------------------------------------|
| <i>base</i>           | LPUART peripheral base address.                                                              |
| <i>handle</i>         | LPUART handle pointer.                                                                       |
| <i>ringBuffer</i>     | Start address of ring buffer for background receiving. Pass NULL to disable the ring buffer. |
| <i>ringBufferSize</i> | size of the ring buffer.                                                                     |

#### 24.2.7.22 void LPUART\_TransferStopRingBuffer ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle* )

This function aborts the background transfer and uninstalls the ring buffer.

## Parameters

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|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

### 24.2.7.23 void LPUART\_TransferAbortSend ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle* )

This function aborts the interrupt driven data sending. The user can get the remainBytes to find out how many bytes are not sent out.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

### 24.2.7.24 status\_t LPUART\_TransferGetSendCount ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle*, uint32\_t \* *count* )

This function gets the number of bytes that have been written to LPUART TX register by an interrupt method.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Send bytes count.               |

Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No send in progress.                                        |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

### 24.2.7.25 status\_t LPUART\_TransferReceiveNonBlocking ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle*, lpuart\_transfer\_t \* *xfer*, size\_t \* *receivedBytes* )

This function receives data using an interrupt method. This is a non-blocking function which returns without waiting to ensure that all data are received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter `receivedBytes` shows how many bytes are copied from the ring buffer. After copying, if the data in the ring buffer is not enough for read, the receive request is saved



by the LPUART driver. When the new data arrives, the receive request is serviced first. When all data is received, the LPUART driver notifies the upper layer through a callback function and passes a status parameter `kStatus_UART_RxIdle`. For example, the upper layer needs 10 bytes but there are only 5 bytes in ring buffer. The 5 bytes are copied to `xfer->data`, which returns with the parameter `receivedBytes` set to 5. For the remaining 5 bytes, the newly arrived data is saved from `xfer->data[5]`. When 5 bytes are received, the LPUART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to `xfer->data`. When all data is received, the upper layer is notified.

Parameters

|                      |                                                                  |
|----------------------|------------------------------------------------------------------|
| <i>base</i>          | LPUART peripheral base address.                                  |
| <i>handle</i>        | LPUART handle pointer.                                           |
| <i>xfer</i>          | LPUART transfer structure, see <a href="#">uart_transfer_t</a> . |
| <i>receivedBytes</i> | Bytes received from the ring buffer directly.                    |

Return values

|                                |                                                          |
|--------------------------------|----------------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully queue the transfer into the transmit queue. |
| <i>kStatus_LPUART_Rx-Busy</i>  | Previous receive request is not finished.                |
| <i>kStatus_InvalidArgument</i> | Invalid argument.                                        |

#### 24.2.7.26 void LPUART\_TransferAbortReceive ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle* )

This function aborts the interrupt-driven data receiving. The user can get the `remainBytes` to find out how many bytes not received yet.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

#### 24.2.7.27 status\_t LPUART\_TransferGetReceiveCount ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle*, uint32\_t \* *count* )

This function gets the number of bytes that have been received.

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### Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Receive bytes count.            |

### Return values

|                                     |                                               |
|-------------------------------------|-----------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No receive in progress.                       |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                         |
| <i>kStatus_Success</i>              | Get successfully through the parameter count; |

#### 24.2.7.28 void LPUART\_TransferHandleIRQ ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle* )

This function handles the LPUART transmit and receive IRQ request.

### Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

#### 24.2.7.29 void LPUART\_TransferHandleErrorIRQ ( LPUART\_Type \* *base*, lpuart\_handle\_t \* *handle* )

This function handles the LPUART error IRQ request.

### Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

## 24.3 LPUART DMA Driver

### 24.3.1 Overview

#### Data Structures

- struct [lpuart\\_dma\\_handle\\_t](#)  
*LPUART DMA handle. [More...](#)*

#### Typedefs

- typedef void(\* [lpuart\\_dma\\_transfer\\_callback\\_t](#) )(LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle, status\_t status, void \*userData)  
*LPUART transfer callback function.*

#### EDMA transactional

- void [LPUART\\_TransferCreateHandleDMA](#) (LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle, [lpuart\\_dma\\_transfer\\_callback\\_t](#) callback, void \*userData, dma\_handle\_t \*txDmaHandle, dma\_handle\_t \*rxDmaHandle)  
*Initializes the LPUART handle which is used in transactional functions.*
- status\_t [LPUART\\_TransferSendDMA](#) (LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle, [lpuart\\_transfer\\_t](#) \*xfer)  
*Sends data using DMA.*
- status\_t [LPUART\\_TransferReceiveDMA](#) (LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle, [lpuart\\_transfer\\_t](#) \*xfer)  
*Receives data using DMA.*
- void [LPUART\\_TransferAbortSendDMA](#) (LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle)  
*Aborts the sent data using DMA.*
- void [LPUART\\_TransferAbortReceiveDMA](#) (LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle)  
*Aborts the received data using DMA.*
- status\_t [LPUART\\_TransferGetSendCountDMA](#) (LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes written to the LPUART TX register.*
- status\_t [LPUART\\_TransferGetReceiveCountDMA](#) (LPUART\_Type \*base, lpuart\_dma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of received bytes.*

### 24.3.2 Data Structure Documentation

#### 24.3.2.1 struct [lpuart\\_dma\\_handle](#)

##### Data Fields

- [lpuart\\_dma\\_transfer\\_callback\\_t](#) callback

## LPUART DMA Driver

- Callback function.*
  - void \* [userData](#)  
*LPUART callback function parameter.*
- size\_t [rxDataSizeAll](#)  
*Size of the data to receive.*
- size\_t [txDataSizeAll](#)  
*Size of the data to send out.*
- dma\_handle\_t \* [txDmaHandle](#)  
*The DMA TX channel used.*
- dma\_handle\_t \* [rxDmaHandle](#)  
*The DMA RX channel used.*
- volatile uint8\_t [txState](#)  
*TX transfer state.*
- volatile uint8\_t [rxState](#)  
*RX transfer state.*

### 24.3.2.1.0.67 Field Documentation

24.3.2.1.0.67.1 `lpuart_dma_transfer_callback_t lpuart_dma_handle_t::callback`

24.3.2.1.0.67.2 `void* lpuart_dma_handle_t::userData`

24.3.2.1.0.67.3 `size_t lpuart_dma_handle_t::rxDataSizeAll`

24.3.2.1.0.67.4 `size_t lpuart_dma_handle_t::txDataSizeAll`

24.3.2.1.0.67.5 `dma_handle_t* lpuart_dma_handle_t::txDmaHandle`

24.3.2.1.0.67.6 `dma_handle_t* lpuart_dma_handle_t::rxDmaHandle`

24.3.2.1.0.67.7 `volatile uint8_t lpuart_dma_handle_t::txState`

### 24.3.3 Typedef Documentation

24.3.3.1 `typedef void(* lpuart_dma_transfer_callback_t)(LPUART_Type *base,  
lpuart_dma_handle_t *handle, status_t status, void *userData)`

### 24.3.4 Function Documentation

24.3.4.1 `void LPUART_TransferCreateHandleDMA ( LPUART_Type * base,  
lpuart_dma_handle_t * handle, lpuart_dma_transfer_callback_t callback, void *  
userData, dma_handle_t * txDmaHandle, dma_handle_t * rxDmaHandle )`

## Parameters

|                    |                                                        |
|--------------------|--------------------------------------------------------|
| <i>base</i>        | LPUART peripheral base address.                        |
| <i>handle</i>      | Pointer to <code>lpuart_dma_handle_t</code> structure. |
| <i>callback</i>    | Callback function.                                     |
| <i>userData</i>    | User data.                                             |
| <i>txDmaHandle</i> | User-requested DMA handle for TX DMA transfer.         |
| <i>rxDmaHandle</i> | User-requested DMA handle for RX DMA transfer.         |

#### 24.3.4.2 **status\_t LPUART\_TransferSendDMA ( LPUART\_Type \* *base*, lpuart\_dma\_handle\_t \* *handle*, lpuart\_transfer\_t \* *xfer* )**

This function sends data using DMA. This is a non-blocking function, which returns right away. When all data is sent, the send callback function is called.

## Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                                        |
| <i>handle</i> | LPUART handle pointer.                                                 |
| <i>xfer</i>   | LPUART DMA transfer structure. See <a href="#">lpuart_transfer_t</a> . |

## Return values

|                                |                             |
|--------------------------------|-----------------------------|
| <i>kStatus_Success</i>         | if succeed, others failed.  |
| <i>kStatus_LPUART_TxBusy</i>   | Previous transfer on going. |
| <i>kStatus_InvalidArgument</i> | Invalid argument.           |

#### 24.3.4.3 **status\_t LPUART\_TransferReceiveDMA ( LPUART\_Type \* *base*, lpuart\_dma\_handle\_t \* *handle*, lpuart\_transfer\_t \* *xfer* )**

This function receives data using DMA. This is a non-blocking function, which returns right away. When all data is received, the receive callback function is called.

## Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                                        |
| <i>handle</i> | Pointer to <code>lpuart_dma_handle_t</code> structure.                 |
| <i>xfer</i>   | LPUART DMA transfer structure. See <a href="#">lpuart_transfer_t</a> . |

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Return values

|                                |                             |
|--------------------------------|-----------------------------|
| <i>kStatus_Success</i>         | if succeed, others failed.  |
| <i>kStatus_LPUART_Rx-Busy</i>  | Previous transfer on going. |
| <i>kStatus_InvalidArgument</i> | Invalid argument.           |

### 24.3.4.4 void LPUART\_TransferAbortSendDMA ( LPUART\_Type \* *base*, lpuart\_dma\_handle\_t \* *handle* )

This function aborts send data using DMA.

Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>base</i>   | LPUART peripheral base address           |
| <i>handle</i> | Pointer to lpuart_dma_handle_t structure |

### 24.3.4.5 void LPUART\_TransferAbortReceiveDMA ( LPUART\_Type \* *base*, lpuart\_dma\_handle\_t \* *handle* )

This function aborts the received data using DMA.

Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>base</i>   | LPUART peripheral base address           |
| <i>handle</i> | Pointer to lpuart_dma_handle_t structure |

### 24.3.4.6 status\_t LPUART\_TransferGetSendCountDMA ( LPUART\_Type \* *base*, lpuart\_dma\_handle\_t \* *handle*, uint32\_t \* *count* )

This function gets the number of bytes that have been written to LPUART TX register by DMA.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Send bytes count.               |

Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No send in progress.                                        |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

#### 24.3.4.7 **status\_t LPUART\_TransferGetReceiveCountDMA ( LPUART\_Type \* *base*, lpuart\_dma\_handle\_t \* *handle*, uint32\_t \* *count* )**

This function gets the number of received bytes.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Receive bytes count.            |

Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No receive in progress.                                     |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

### 24.4 LPUART eDMA Driver

#### 24.4.1 Overview

#### Data Structures

- struct [lpuart\\_edma\\_handle\\_t](#)  
*LPUART eDMA handle. [More...](#)*

#### Typedefs

- typedef void(\* [lpuart\\_edma\\_transfer\\_callback\\_t](#) )(LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*LPUART transfer callback function.*

#### eDMA transactional

- void [LPUART\\_TransferCreateHandleEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, [lpuart\\_edma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*txEdmaHandle, [edma\\_handle\\_t](#) \*rxEdmaHandle)  
*Initializes the LPUART handle which is used in transactional functions.*
- status\_t [LPUART\\_SendEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, [lpuart\\_transfer\\_t](#) \*xfer)  
*Sends data using eDMA.*
- status\_t [LPUART\\_ReceiveEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, [lpuart\\_transfer\\_t](#) \*xfer)  
*Receives data using eDMA.*
- void [LPUART\\_TransferAbortSendEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle)  
*Aborts the sent data using eDMA.*
- void [LPUART\\_TransferAbortReceiveEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle)  
*Aborts the received data using eDMA.*
- status\_t [LPUART\\_TransferGetSendCountEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes written to the LPUART TX register.*
- status\_t [LPUART\\_TransferGetReceiveCountEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of received bytes.*



## 24.4.2 Data Structure Documentation

### 24.4.2.1 struct \_lpuart\_edma\_handle

#### Data Fields

- [lpuart\\_edma\\_transfer\\_callback\\_t](#) [callback](#)  
*Callback function.*
- void \* [userData](#)  
*LPUART callback function parameter.*
- size\_t [rxDataSizeAll](#)  
*Size of the data to receive.*
- size\_t [txDataSizeAll](#)  
*Size of the data to send out.*
- [edma\\_handle\\_t](#) \* [txEdmaHandle](#)  
*The eDMA TX channel used.*
- [edma\\_handle\\_t](#) \* [rxEdmaHandle](#)  
*The eDMA RX channel used.*
- uint8\_t [nbytes](#)  
*eDMA minor byte transfer count initially configured.*
- volatile uint8\_t [txState](#)  
*TX transfer state.*
- volatile uint8\_t [rxState](#)  
*RX transfer state.*

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### 24.4.2.1.0.68 Field Documentation

24.4.2.1.0.68.1 `lpuart_edma_transfer_callback_t lpuart_edma_handle_t::callback`

24.4.2.1.0.68.2 `void* lpuart_edma_handle_t::userData`

24.4.2.1.0.68.3 `size_t lpuart_edma_handle_t::rxDataSizeAll`

24.4.2.1.0.68.4 `size_t lpuart_edma_handle_t::txDataSizeAll`

24.4.2.1.0.68.5 `edma_handle_t* lpuart_edma_handle_t::txEdmaHandle`

24.4.2.1.0.68.6 `edma_handle_t* lpuart_edma_handle_t::rxEdmaHandle`

24.4.2.1.0.68.7 `uint8_t lpuart_edma_handle_t::nbytes`

24.4.2.1.0.68.8 `volatile uint8_t lpuart_edma_handle_t::txState`

### 24.4.3 Typedef Documentation

24.4.3.1 `typedef void(* lpuart_edma_transfer_callback_t)(LPUART_Type *base,  
lpuart_edma_handle_t *handle, status_t status, void *userData)`

### 24.4.4 Function Documentation

24.4.4.1 `void LPUART_TransferCreateHandleEDMA ( LPUART_Type * base,  
lpuart_edma_handle_t * handle, lpuart_edma_transfer_callback_t callback, void  
* userData, edma_handle_t * txEdmaHandle, edma_handle_t * rxEdmaHandle )`

## Parameters

|                     |                                                         |
|---------------------|---------------------------------------------------------|
| <i>base</i>         | LPUART peripheral base address.                         |
| <i>handle</i>       | Pointer to <code>lpuart_edma_handle_t</code> structure. |
| <i>callback</i>     | Callback function.                                      |
| <i>userData</i>     | User data.                                              |
| <i>txEdmaHandle</i> | User requested DMA handle for TX DMA transfer.          |
| <i>rxEdmaHandle</i> | User requested DMA handle for RX DMA transfer.          |

#### 24.4.4.2 **status\_t LPUART\_SendEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle*, lpuart\_transfer\_t \* *xfer* )**

This function sends data using eDMA. This is a non-blocking function, which returns right away. When all data is sent, the send callback function is called.

## Parameters

|               |                                                                         |
|---------------|-------------------------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                                         |
| <i>handle</i> | LPUART handle pointer.                                                  |
| <i>xfer</i>   | LPUART eDMA transfer structure. See <a href="#">lpuart_transfer_t</a> . |

## Return values

|                                |                             |
|--------------------------------|-----------------------------|
| <i>kStatus_Success</i>         | if succeed, others failed.  |
| <i>kStatus_LPUART_TxBusy</i>   | Previous transfer on going. |
| <i>kStatus_InvalidArgument</i> | Invalid argument.           |

#### 24.4.4.3 **status\_t LPUART\_ReceiveEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle*, lpuart\_transfer\_t \* *xfer* )**

This function receives data using eDMA. This is non-blocking function, which returns right away. When all data is received, the receive callback function is called.

## Parameters

|               |                                                                         |
|---------------|-------------------------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                                         |
| <i>handle</i> | Pointer to <code>lpuart_edma_handle_t</code> structure.                 |
| <i>xfer</i>   | LPUART eDMA transfer structure, see <a href="#">lpuart_transfer_t</a> . |

## LPUART eDMA Driver

Return values

|                                |                            |
|--------------------------------|----------------------------|
| <i>kStatus_Success</i>         | if succeed, others fail.   |
| <i>kStatus_LPUART_Rx-Busy</i>  | Previous transfer ongoing. |
| <i>kStatus_InvalidArgument</i> | Invalid argument.          |

### 24.4.4.4 void LPUART\_TransferAbortSendEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle* )

This function aborts the sent data using eDMA.

Parameters

|               |                                            |
|---------------|--------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.            |
| <i>handle</i> | Pointer to lpuart_edma_handle_t structure. |

### 24.4.4.5 void LPUART\_TransferAbortReceiveEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle* )

This function aborts the received data using eDMA.

Parameters

|               |                                            |
|---------------|--------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.            |
| <i>handle</i> | Pointer to lpuart_edma_handle_t structure. |

### 24.4.4.6 status\_t LPUART\_TransferGetSendCountEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle*, uint32\_t \* *count* )

This function gets the number of bytes written to the LPUART TX register by DMA.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Send bytes count.               |

Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No send in progress.                                        |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

#### 24.4.4.7 **status\_t LPUART\_TransferGetReceiveCountEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle*, uint32\_t \* *count* )**

This function gets the number of received bytes.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Receive bytes count.            |

Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No receive in progress.                                     |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

### 24.5 LPUART $\mu$ COS/II Driver

#### 24.5.1 Overview

##### Data Structures

- struct [lpuart\\_rtos\\_config\\_t](#)  
*LPUART RTOS configuration structure. [More...](#)*

##### LPUART RTOS Operation

- int [LPUART\\_RTOS\\_Init](#) (lpuart\_rtos\_handle\_t \*handle, lpuart\_handle\_t \*t\_handle, const [lpuart\\_rtos\\_config\\_t](#) \*cfg)  
*Initializes an LPUART instance for operation in RTOS.*
- int [LPUART\\_RTOS\\_Deinit](#) (lpuart\_rtos\_handle\_t \*handle)  
*Deinitializes an LPUART instance for operation.*

##### LPUART transactional Operation

- int [LPUART\\_RTOS\\_Send](#) (lpuart\_rtos\_handle\_t \*handle, const uint8\_t \*buffer, uint32\_t length)  
*Sends data in the background.*
- int [LPUART\\_RTOS\\_Receive](#) (lpuart\_rtos\_handle\_t \*handle, uint8\_t \*buffer, uint32\_t length, size\_t \*received)  
*Receives data.*

#### 24.5.2 Data Structure Documentation

##### 24.5.2.1 struct lpuart\_rtos\_config\_t

###### Data Fields

- LPUART\_Type \* [base](#)  
*UART base address.*
- uint32\_t [srcclk](#)  
*UART source clock in Hz.*
- uint32\_t [baudrate](#)  
*Desired communication speed.*
- [lpuart\\_parity\\_mode\\_t](#) [parity](#)  
*Parity setting.*
- [lpuart\\_stop\\_bit\\_count\\_t](#) [stopbits](#)  
*Number of stop bits to use.*
- uint8\_t \* [buffer](#)  
*Buffer for background reception.*
- uint32\_t [buffer\\_size](#)  
*Size of buffer for background reception.*

### 24.5.3 Function Documentation

24.5.3.1 `int LPUART_RTOS_Init ( lpuart_rtos_handle_t * handle, lpuart_handle_t * t_handle, const lpuart_rtos_config_t * cfg )`

## LPUART $\mu$ COS/II Driver

### Parameters

|                        |                                                                                      |
|------------------------|--------------------------------------------------------------------------------------|
| <i>handle</i>          | The RTOS LPUART handle, the pointer to an allocated space for RTOS context.          |
| <i>lpuart_t_handle</i> | The pointer to an allocated space to store the transactional layer internal state.   |
| <i>cfg</i>             | The pointer to the parameters required to configure the LPUART after initialization. |

### Returns

0 succeed, others failed

#### 24.5.3.2 int LPUART\_RTOS\_Deinit ( lpuart\_rtos\_handle\_t \* *handle* )

This function deinitializes the LPUART module, sets all register values to the reset value, and releases the resources.

### Parameters

|               |                         |
|---------------|-------------------------|
| <i>handle</i> | The RTOS LPUART handle. |
|---------------|-------------------------|

#### 24.5.3.3 int LPUART\_RTOS\_Send ( lpuart\_rtos\_handle\_t \* *handle*, const uint8\_t \* *buffer*, uint32\_t *length* )

This function sends data. It is a synchronous API. If the hardware buffer is full, the task is in the blocked state.

### Parameters

|               |                                |
|---------------|--------------------------------|
| <i>handle</i> | The RTOS LPUART handle.        |
| <i>buffer</i> | The pointer to buffer to send. |
| <i>length</i> | The number of bytes to send.   |

#### 24.5.3.4 int LPUART\_RTOS\_Receive ( lpuart\_rtos\_handle\_t \* *handle*, uint8\_t \* *buffer*, uint32\_t *length*, size\_t \* *received* )

This function receives data from LPUART. It is a synchronous API. If any data is immediately available it is returned immediately and the number of bytes received.



## Parameters

|                 |                                                                                  |
|-----------------|----------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS LPUART handle.                                                          |
| <i>buffer</i>   | The pointer to buffer where to write received data.                              |
| <i>length</i>   | The number of bytes to receive.                                                  |
| <i>received</i> | The pointer to a variable of size_t where the number of received data is filled. |

### 24.6 LPUART $\mu$ COS/III Driver

#### 24.6.1 Overview

##### Data Structures

- struct [lpuart\\_rtos\\_config\\_t](#)  
*LPUART RTOS configuration structure. [More...](#)*

##### LPUART RTOS Operation

- int [LPUART\\_RTOS\\_Init](#) (lpuart\_rtos\_handle\_t \*handle, lpuart\_handle\_t \*t\_handle, const [lpuart\\_rtos\\_config\\_t](#) \*cfg)  
*Initializes an LPUART instance for operation in RTOS.*
- int [LPUART\\_RTOS\\_Deinit](#) (lpuart\_rtos\_handle\_t \*handle)  
*Deinitializes an LPUART instance for operation.*

##### LPUART transactional Operation

- int [LPUART\\_RTOS\\_Send](#) (lpuart\_rtos\_handle\_t \*handle, const uint8\_t \*buffer, uint32\_t length)  
*Sends data in the background.*
- int [LPUART\\_RTOS\\_Receive](#) (lpuart\_rtos\_handle\_t \*handle, uint8\_t \*buffer, uint32\_t length, size\_t \*received)  
*Receives data.*

#### 24.6.2 Data Structure Documentation

##### 24.6.2.1 struct lpuart\_rtos\_config\_t

###### Data Fields

- LPUART\_Type \* [base](#)  
*UART base address.*
- uint32\_t [srcclk](#)  
*UART source clock in Hz.*
- uint32\_t [baudrate](#)  
*Desired communication speed.*
- [lpuart\\_parity\\_mode\\_t](#) [parity](#)  
*Parity setting.*
- [lpuart\\_stop\\_bit\\_count\\_t](#) [stopbits](#)  
*Number of stop bits to use.*
- uint8\_t \* [buffer](#)  
*Buffer for background reception.*
- uint32\_t [buffer\\_size](#)  
*Size of buffer for background reception.*

### 24.6.3 Function Documentation

24.6.3.1 int LPUART\_RTOS\_Init ( lpuart\_rtos\_handle\_t \* *handle*, lpuart\_handle\_t \* *t\_handle*, const lpuart\_rtos\_config\_t \* *cfg* )

## LPUART $\mu$ COS/III Driver

### Parameters

|                        |                                                                                      |
|------------------------|--------------------------------------------------------------------------------------|
| <i>handle</i>          | The RTOS LPUART handle, the pointer to allocated space for RTOS context.             |
| <i>lpuart_t_handle</i> | The pointer to allocated space where to store transactional layer internal state.    |
| <i>cfg</i>             | The pointer to the parameters required to configure the LPUART after initialization. |

### Returns

0 succeed, others failed

#### 24.6.3.2 int LPUART\_RTOS\_Deinit ( lpuart\_rtos\_handle\_t \* *handle* )

This function deinitializes the LPUART module, set all register value to reset value and releases the resources.

### Parameters

|               |                         |
|---------------|-------------------------|
| <i>handle</i> | The RTOS LPUART handle. |
|---------------|-------------------------|

#### 24.6.3.3 int LPUART\_RTOS\_Send ( lpuart\_rtos\_handle\_t \* *handle*, const uint8\_t \* *buffer*, uint32\_t *length* )

This function sends data. It is synchronous API. If the HW buffer is full, the task is in the blocked state.

### Parameters

|               |                                |
|---------------|--------------------------------|
| <i>handle</i> | The RTOS LPUART handle.        |
| <i>buffer</i> | The pointer to buffer to send. |
| <i>length</i> | The number of bytes to send.   |

#### 24.6.3.4 int LPUART\_RTOS\_Receive ( lpuart\_rtos\_handle\_t \* *handle*, uint8\_t \* *buffer*, uint32\_t *length*, size\_t \* *received* )

It is a synchronous API.

This function receives data from LPUART. If any data is immediately available it will be returned immediately and the number of bytes received.

## Parameters

|                 |                                                                                     |
|-----------------|-------------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS LPUART handle.                                                             |
| <i>buffer</i>   | The pointer to buffer where to write received data.                                 |
| <i>length</i>   | The number of bytes to receive.                                                     |
| <i>received</i> | The pointer to variable of size_t where the number of received data will be filled. |

## 24.7 LPUART FreeRTOS Driver

### 24.7.1 Overview

#### Data Structures

- struct [lpuart\\_rtos\\_config\\_t](#)  
*LPUART RTOS configuration structure. [More...](#)*

#### LPUART RTOS Operation

- int [LPUART\\_RTOS\\_Init](#) (lpuart\_rtos\_handle\_t \*handle, lpuart\_handle\_t \*t\_handle, const [lpuart\\_rtos\\_config\\_t](#) \*cfg)  
*Initializes an LPUART instance for operation in RTOS.*
- int [LPUART\\_RTOS\\_Deinit](#) (lpuart\_rtos\_handle\_t \*handle)  
*Deinitializes an LPUART instance for operation.*

#### LPUART transactional Operation

- int [LPUART\\_RTOS\\_Send](#) (lpuart\_rtos\_handle\_t \*handle, const uint8\_t \*buffer, uint32\_t length)  
*Sends data in the background.*
- int [LPUART\\_RTOS\\_Receive](#) (lpuart\_rtos\_handle\_t \*handle, uint8\_t \*buffer, uint32\_t length, size\_t \*received)  
*Receives data.*

### 24.7.2 Data Structure Documentation

#### 24.7.2.1 struct lpuart\_rtos\_config\_t

##### Data Fields

- LPUART\_Type \* [base](#)  
*UART base address.*
- uint32\_t [srcclk](#)  
*UART source clock in Hz.*
- uint32\_t [baudrate](#)  
*Desired communication speed.*
- [lpuart\\_parity\\_mode\\_t](#) [parity](#)  
*Parity setting.*
- [lpuart\\_stop\\_bit\\_count\\_t](#) [stopbits](#)  
*Number of stop bits to use.*
- uint8\_t \* [buffer](#)  
*Buffer for background reception.*
- uint32\_t [buffer\\_size](#)  
*Size of buffer for background reception.*

### 24.7.3 Function Documentation

24.7.3.1 `int LPUART_RTOS_Init ( lpuart_rtos_handle_t * handle, lpuart_handle_t * t_handle, const lpuart_rtos_config_t * cfg )`

## LPUART FreeRTOS Driver

### Parameters

|                 |                                                                                      |
|-----------------|--------------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS LPUART handle, the pointer to an allocated space for RTOS context.          |
| <i>t_handle</i> | The pointer to an allocated space to store the transactional layer internal state.   |
| <i>cfg</i>      | The pointer to the parameters required to configure the LPUART after initialization. |

### Returns

0 succeed, others failed

#### 24.7.3.2 int LPUART\_RTOS\_Deinit ( lpuart\_rtos\_handle\_t \* *handle* )

This function deinitializes the LPUART module, sets all register value to the reset value, and releases the resources.

### Parameters

|               |                         |
|---------------|-------------------------|
| <i>handle</i> | The RTOS LPUART handle. |
|---------------|-------------------------|

#### 24.7.3.3 int LPUART\_RTOS\_Send ( lpuart\_rtos\_handle\_t \* *handle*, const uint8\_t \* *buffer*, uint32\_t *length* )

This function sends data. It is an synchronous API. If the hardware buffer is full, the task is in the blocked state.

### Parameters

|               |                                |
|---------------|--------------------------------|
| <i>handle</i> | The RTOS LPUART handle.        |
| <i>buffer</i> | The pointer to buffer to send. |
| <i>length</i> | The number of bytes to send.   |

#### 24.7.3.4 int LPUART\_RTOS\_Receive ( lpuart\_rtos\_handle\_t \* *handle*, uint8\_t \* *buffer*, uint32\_t *length*, size\_t \* *received* )

This function receives data from LPUART. It is an synchronous API. If any data is immediately available it is returned immediately and the number of bytes received.



### Parameters

|                 |                                                                                  |
|-----------------|----------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS LPUART handle.                                                          |
| <i>buffer</i>   | The pointer to buffer where to write received data.                              |
| <i>length</i>   | The number of bytes to receive.                                                  |
| <i>received</i> | The pointer to a variable of size_t where the number of received data is filled. |



## Chapter 25

# MPU: Memory Protection Unit

### 25.1 Overview

The MPU driver provides hardware access control for all memory references generated in the device. Use the MPU driver to program the region descriptors that define memory spaces and their access rights. After initialization, the MPU concurrently monitors the system bus transactions and evaluates their appropriateness.

### 25.2 Initialization and Deinitialization

To initialize the MPU module, call the [MPU\\_Init\(\)](#) function and provide the user configuration data structure. This function sets the configuration of the MPU module automatically and enables the MPU module.

Note that the configuration start address, end address, the region valid value, and the debugger's access permission for the MPU region 0 cannot be changed.

This is an example code to configure the MPU driver.

```
// Defines the MPU memory access permission configuration structure . //
mpu_rwxrights_master_access_control_t mpuRwxAccessRightsMasters =
{
    kMPU_SupervisorReadWriteExecute,
    kMPU_UserNoAccessRights,
    kMPU_IdentifierDisable,
    kMPU_SupervisorEqualToUsermode,
    kMPU_UserNoAccessRights,
    kMPU_IdentifierDisable,
    kMPU_SupervisorEqualToUsermode,
    kMPU_UserNoAccessRights,
    kMPU_IdentifierDisable,
    kMPU_SupervisorEqualToUsermode,
    kMPU_UserNoAccessRights,
    kMPU_IdentifierDisable
}
mpu_rwxrights_master_access_control_t mpuRwAccessRightsMasters =
{
    false,
    false,
    false,
    false,
    false,
    false,
    false,
    false,
    false
};

// Defines the MPU region configuration structure. //
mpu_region_config_t mpuRegionConfig =
{
    0,
    0x0,
    0xffffffff,
    mpuRwxAccessRightsMasters,
    mpuRwAccessRightsMasters,
```

## Basic Control Operations

```
    0,  
    0  
};  
  
// Defines the MPU user configuration structure. //  
mpu_config_t mpuUserConfig =  
{  
    mpuRegionConfig,  
    NULL  
};  
  
// Initializes the MPU region 0. //  
MPU_Init(MPU, &mpuUserConfig);
```

## 25.3 Basic Control Operations

MPU can be enabled/disabled for the entire memory protection region by calling the [MPU\\_Enable\(\)](#) function. To save the power for any unused special regions when the entire memory protection region is disabled, call the [MPU\\_RegionEnable\(\)](#).

After MPU initialization, the [MPU\\_SetRegionLowMasterAccessRights\(\)](#) and [MPU\\_SetRegionHighMasterAccessRights\(\)](#) can be used to change the access rights for special master ports and for special region numbers. The [MPU\\_SetRegionConfig](#) can be used to set the whole region with the start/end address with access rights.

The [MPU\\_GetHardwareInfo\(\)](#) API is provided to get the hardware information for the device. The [MPU\\_GetSlavePortErrorStatus\(\)](#) API is provided to get the error status of a special slave port. When an error happens in this port, the [MPU\\_GetDetailErrorAccessInfo\(\)](#) API is provided to get the detailed error information.

## Data Structures

- struct [mpu\\_hardware\\_info\\_t](#)  
*MPU hardware basic information. [More...](#)*
- struct [mpu\\_access\\_err\\_info\\_t](#)  
*MPU detail error access information. [More...](#)*
- struct [mpu\\_rwxrights\\_master\\_access\\_control\\_t](#)  
*MPU read/write/execute rights control for bus master 0 ~ 3. [More...](#)*
- struct [mpu\\_rwrights\\_master\\_access\\_control\\_t](#)  
*MPU read/write access control for bus master 4 ~ 7. [More...](#)*
- struct [mpu\\_region\\_config\\_t](#)  
*MPU region configuration structure. [More...](#)*
- struct [mpu\\_config\\_t](#)  
*The configuration structure for the MPU initialization. [More...](#)*

## Macros

- #define [MPU\\_REGION\\_RWXRIGHTS\\_MASTER\\_SHIFT](#)(n) (n \* 6)  
*MPU the bit shift for masters with privilege rights: read write and execute.*
- #define [MPU\\_REGION\\_RWXRIGHTS\\_MASTER\\_MASK](#)(n) (0x1Fu << MPU\_REGION\_RWXRIGHTS\_MASTER\_SHIFT(n))  
*MPU masters with read, write and execute rights bit mask.*
- #define [MPU\\_REGION\\_RWXRIGHTS\\_MASTER\\_WIDTH](#) 5

- *MPU masters with read, write and execute rights bit width.*  
 • #define `MPU_REGION_RWXRIGHTS_MASTER(n, x)` (((uint32\_t)((uint32\_t)(x)) << `MPU_REGION_RWXRIGHTS_MASTER_SHIFT(n)`)) & `MPU_REGION_RWXRIGHTS_MASTER_MASK(n)`
- *MPU masters with read, write and execute rights priority setting.*  
 • #define `MPU_REGION_RWXRIGHTS_MASTER_PE_SHIFT(n)` (n \* 6 + `MPU_REGION_RWXRIGHTS_MASTER_WIDTH`)
- *MPU masters with read, write and execute rights process enable bit shift.*  
 • #define `MPU_REGION_RWXRIGHTS_MASTER_PE_MASK(n)` (0x1u << `MPU_REGION_RWXRIGHTS_MASTER_PE_SHIFT(n)`)
- *MPU masters with read, write and execute rights process enable bit mask.*  
 • #define `MPU_REGION_RWXRIGHTS_MASTER_PE(n, x)` (((uint32\_t)((uint32\_t)(x)) << `MPU_REGION_RWXRIGHTS_MASTER_PE_SHIFT(n)`)) & `MPU_REGION_RWXRIGHTS_MASTER_PE_MASK(n)`
- *MPU masters with read, write and execute rights process enable setting.*  
 • #define `MPU_REGION_RWRIGHTS_MASTER_SHIFT(n)` ((n - `FSL_FEATURE_MPU_PRIVILEGED_RIGHTS_MASTER_COUNT`) \* 2 + 24)
- *MPU masters with normal read write permission bit shift.*  
 • #define `MPU_REGION_RWRIGHTS_MASTER_MASK(n)` (0x3u << `MPU_REGION_RWRIGHTS_MASTER_SHIFT(n)`)
- *MPU masters with normal read write rights bit mask.*  
 • #define `MPU_REGION_RWRIGHTS_MASTER(n, x)` (((uint32\_t)((uint32\_t)(x)) << `MPU_REGION_RWRIGHTS_MASTER_SHIFT(n)`)) & `MPU_REGION_RWRIGHTS_MASTER_MASK(n)`
- *MPU masters with normal read write rights priority setting.*  
 • #define `MPU_SLAVE_PORT_NUM` (4u)
- *the Slave port numbers.*  
 • #define `MPU_PRIVILEGED_RIGHTS_MASTER_MAX_INDEX` (3)
- *define the maximum index of master with privileged rights.*

## Enumerations

- enum `mpu_region_total_num_t` {  
   `kMPU_8Regions` = 0x0U,  
   `kMPU_12Regions` = 0x1U,  
   `kMPU_16Regions` = 0x2U }  
   *Describes the number of MPU regions.*
- enum `mpu_slave_t` {  
   `kMPU_Slave0` = 0U,  
   `kMPU_Slave1` = 1U,  
   `kMPU_Slave2` = 2U,  
   `kMPU_Slave3` = 3U,  
   `kMPU_Slave4` = 4U }  
   *MPU slave port number.*
- enum `mpu_err_access_control_t` {  
   `kMPU_NoRegionHit` = 0U,  
   `kMPU_NoneOverlappRegion` = 1U,  
   `kMPU_OverlappRegion` = 2U }

## Basic Control Operations

- MPU error access control detail.*
  - enum `mpu_err_access_type_t` {  
    `kMPU_ErrTypeRead` = 0U,  
    `kMPU_ErrTypeWrite` = 1U }
- MPU error access type.*
  - enum `mpu_err_attributes_t` {  
    `kMPU_InstructionAccessInUserMode` = 0U,  
    `kMPU_DataAccessInUserMode` = 1U,  
    `kMPU_InstructionAccessInSupervisorMode` = 2U,  
    `kMPU_DataAccessInSupervisorMode` = 3U }
- MPU access error attributes.*
  - enum `mpu_supervisor_access_rights_t` {  
    `kMPU_SupervisorReadWriteExecute` = 0U,  
    `kMPU_SupervisorReadExecute` = 1U,  
    `kMPU_SupervisorReadWrite` = 2U,  
    `kMPU_SupervisorEqualToUsermode` = 3U }
- MPU access rights in supervisor mode for bus master 0 ~ 3.*
  - enum `mpu_user_access_rights_t` {  
    `kMPU_UserNoAccessRights` = 0U,  
    `kMPU_UserExecute` = 1U,  
    `kMPU_UserWrite` = 2U,  
    `kMPU_UserWriteExecute` = 3U,  
    `kMPU_UserRead` = 4U,  
    `kMPU_UserReadExecute` = 5U,  
    `kMPU_UserReadWrite` = 6U,  
    `kMPU_UserReadWriteExecute` = 7U }
- MPU access rights in user mode for bus master 0 ~ 3.*

## Driver version

- #define `FSL_MPU_DRIVER_VERSION` (`MAKE_VERSION`(2, 1, 1))  
*MPU driver version 2.1.0.*

## Initialization and deinitialization

- void `MPU_Init` (MPU\_Type \*base, const `mpu_config_t` \*config)  
*Initializes the MPU with the user configuration structure.*
- void `MPU_Deinit` (MPU\_Type \*base)  
*Deinitializes the MPU regions.*

## Basic Control Operations

- static void `MPU_Enable` (MPU\_Type \*base, bool enable)  
*Enables/disables the MPU globally.*
- static void `MPU_RegionEnable` (MPU\_Type \*base, uint32\_t number, bool enable)  
*Enables/disables the MPU for a special region.*
- void `MPU_GetHardwareInfo` (MPU\_Type \*base, `mpu_hardware_info_t` \*hardwareInform)  
*Gets the MPU basic hardware information.*

- void [MPU\\_SetRegionConfig](#) (MPU\_Type \*base, const [mpu\\_region\\_config\\_t](#) \*regionConfig)  
*Sets the MPU region.*
- void [MPU\\_SetRegionAddr](#) (MPU\_Type \*base, uint32\_t regionNum, uint32\_t startAddr, uint32\_t endAddr)  
*Sets the region start and end address.*
- void [MPU\\_SetRegionRwxMasterAccessRights](#) (MPU\_Type \*base, uint32\_t regionNum, uint32\_t masterNum, const [mpu\\_rwxrights\\_master\\_access\\_control\\_t](#) \*accessRights)  
*Sets the MPU region access rights for masters with read, write, and execute rights.*
- void [MPU\\_SetRegionRwMasterAccessRights](#) (MPU\_Type \*base, uint32\_t regionNum, uint32\_t masterNum, const [mpu\\_rwxrights\\_master\\_access\\_control\\_t](#) \*accessRights)  
*Sets the MPU region access rights for masters with read and write rights.*
- bool [MPU\\_GetSlavePortErrorStatus](#) (MPU\_Type \*base, [mpu\\_slave\\_t](#) slaveNum)  
*Gets the numbers of slave ports where errors occur.*
- void [MPU\\_GetDetailErrorAccessInfo](#) (MPU\_Type \*base, [mpu\\_slave\\_t](#) slaveNum, [mpu\\_access\\_err\\_info\\_t](#) \*errInform)  
*Gets the MPU detailed error access information.*

## 25.4 Data Structure Documentation

### 25.4.1 struct mpu\_hardware\_info\_t

#### Data Fields

- uint8\_t [hardwareRevisionLevel](#)  
*Specifies the MPU's hardware and definition reversion level.*
- uint8\_t [slavePortsNumbers](#)  
*Specifies the number of slave ports connected to MPU.*
- [mpu\\_region\\_total\\_num\\_t](#) [regionsNumbers](#)  
*Indicates the number of region descriptors implemented.*

#### 25.4.1.0.0.69 Field Documentation

25.4.1.0.0.69.1 uint8\_t mpu\_hardware\_info\_t::hardwareRevisionLevel

25.4.1.0.0.69.2 uint8\_t mpu\_hardware\_info\_t::slavePortsNumbers

25.4.1.0.0.69.3 mpu\_region\_total\_num\_t mpu\_hardware\_info\_t::regionsNumbers

### 25.4.2 struct mpu\_access\_err\_info\_t

#### Data Fields

- uint32\_t [master](#)  
*Access error master.*
- [mpu\\_err\\_attributes\\_t](#) [attributes](#)  
*Access error attributes.*
- [mpu\\_err\\_access\\_type\\_t](#) [accessType](#)  
*Access error type.*
- [mpu\\_err\\_access\\_control\\_t](#) [accessControl](#)

## Data Structure Documentation

- *Access error control.*  
uint32\_t [address](#)
- *Access error address.*  
uint8\_t [processorIdentification](#)
- *Access error processor identification.*

### 25.4.2.0.0.70 Field Documentation

25.4.2.0.0.70.1 uint32\_t mpu\_access\_err\_info\_t::master

25.4.2.0.0.70.2 mpu\_err\_attributes\_t mpu\_access\_err\_info\_t::attributes

25.4.2.0.0.70.3 mpu\_err\_access\_type\_t mpu\_access\_err\_info\_t::accessType

25.4.2.0.0.70.4 mpu\_err\_access\_control\_t mpu\_access\_err\_info\_t::accessControl

25.4.2.0.0.70.5 uint32\_t mpu\_access\_err\_info\_t::address

25.4.2.0.0.70.6 uint8\_t mpu\_access\_err\_info\_t::processorIdentification

### 25.4.3 struct mpu\_rwxrights\_master\_access\_control\_t

#### Data Fields

- [mpu\\_supervisor\\_access\\_rights\\_t](#) superAccessRights  
*Master access rights in supervisor mode.*
- [mpu\\_user\\_access\\_rights\\_t](#) userAccessRights  
*Master access rights in user mode.*
- bool [processIdentifierEnable](#)  
*Enables or disables process identifier.*

### 25.4.3.0.0.71 Field Documentation

25.4.3.0.0.71.1 mpu\_supervisor\_access\_rights\_t mpu\_rwxrights\_master\_access\_control\_t::superAccessRights

25.4.3.0.0.71.2 mpu\_user\_access\_rights\_t mpu\_rwxrights\_master\_access\_control\_t::userAccessRights

25.4.3.0.0.71.3 bool mpu\_rwxrights\_master\_access\_control\_t::processIdentifierEnable

### 25.4.4 struct mpu\_rwrights\_master\_access\_control\_t

#### Data Fields

- bool [writeEnable](#)  
*Enables or disables write permission.*
- bool [readEnable](#)  
*Enables or disables read permission.*



**25.4.4.0.0.72 Field Documentation****25.4.4.0.0.72.1** `bool mpu_rwrights_master_access_control_t::writeEnable`**25.4.4.0.0.72.2** `bool mpu_rwrights_master_access_control_t::readEnable`**25.4.5 struct mpu\_region\_config\_t**

This structure is used to configure the regionNum region. The accessRights1[0] ~ accessRights1[3] are used to configure the bus master 0 ~ 3 with the privilege rights setting. The accessRights2[0] ~ accessRights2[3] are used to configure the high master 4 ~ 7 with the normal read write permission. The master port assignment is the chip configuration. Normally, the core is the master 0, debugger is the master 1. Note that the MPU assigns a priority scheme where the debugger is treated as the highest priority master followed by the core and then all the remaining masters. MPU protection does not allow writes from the core to affect the "regionNum 0" start and end address nor the permissions associated with the debugger. It can only write the permission fields associated with the other masters. This protection guarantees that the debugger always has access to the entire address space and those rights can't be changed by the core or any other bus master. Prepare the region configuration when regionNum is 0.

**Data Fields**

- `uint32_t regionNum`  
*MPU region number, range form 0 ~ FSL\_FEATURE\_MPU\_DESCRIPTOR\_COUNT - 1.*
- `uint32_t startAddress`  
*Memory region start address.*
- `uint32_t endAddress`  
*Memory region end address.*
- `mpu_rwxrights_master_access_control_t accessRights1 [4]`  
*Masters with read, write and execute rights setting.*
- `mpu_rwrights_master_access_control_t accessRights2 [4]`  
*Masters with normal read write rights setting.*
- `uint8_t processIdentifier`  
*Process identifier used when "processIdentifierEnable" set with true.*
- `uint8_t processIdMask`  
*Process identifier mask.*

**25.4.5.0.0.73 Field Documentation****25.4.5.0.0.73.1** `uint32_t mpu_region_config_t::regionNum`**25.4.5.0.0.73.2** `uint32_t mpu_region_config_t::startAddress`

Note: bit0 ~ bit4 always be marked as 0 by MPU. The actual start address is 0-modulo-32 byte address.

**25.4.5.0.0.73.3** `uint32_t mpu_region_config_t::endAddress`

Note: bit0 ~ bit4 always be marked as 1 by MPU. The actual end address is 31-modulo-32 byte address.

## Data Structure Documentation

**25.4.5.0.0.73.4** `mpu_rwxrights_master_access_control_t mpu_region_config_t::accessRights1[4]`

**25.4.5.0.0.73.5** `mpu_rwrights_master_access_control_t mpu_region_config_t::accessRights2[4]`

**25.4.5.0.0.73.6** `uint8_t mpu_region_config_t::processIdentifier`

**25.4.5.0.0.73.7** `uint8_t mpu_region_config_t::processIdMask`

The setting bit will ignore the same bit in process identifier.

### 25.4.6 struct mpu\_config\_t

This structure is used when calling the MPU\_Init function.

#### Data Fields

- [mpu\\_region\\_config\\_t regionConfig](#)  
*Region access permission.*
- `struct _mpu_config * next`  
*Pointer to the next structure.*

#### 25.4.6.0.0.74 Field Documentation

**25.4.6.0.0.74.1** `mpu_region_config_t mpu_config_t::regionConfig`

**25.4.6.0.0.74.2** `struct _mpu_config* mpu_config_t::next`

## 25.5 Macro Definition Documentation

25.5.1 **#define FSL\_MPU\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))**

25.5.2 **#define MPU\_REGION\_RWXRIGHTS\_MASTER\_SHIFT( *n* ) ( *n* \* 6 )**

25.5.3 **#define MPU\_REGION\_RWXRIGHTS\_MASTER\_MASK( *n* ) (0x1Fu << MPU\_REGION\_RWXRIGHTS\_MASTER\_SHIFT(*n*))**

25.5.4 **#define MPU\_REGION\_RWXRIGHTS\_MASTER\_WIDTH 5**

25.5.5 **#define MPU\_REGION\_RWXRIGHTS\_MASTER( *n*, *x* ) (((uint32\_t)(((uint32\_t)(x)) << MPU\_REGION\_RWXRIGHTS\_MASTER\_SHIFT(*n*))) & MPU\_REGION\_RWXRIGHTS\_MASTER\_MASK(*n*))**

25.5.6 **#define MPU\_REGION\_RWXRIGHTS\_MASTER\_PE\_SHIFT( *n* ) ( *n* \* 6 + MPU\_REGION\_RWXRIGHTS\_MASTER\_WIDTH )**

25.5.7 **#define MPU\_REGION\_RWXRIGHTS\_MASTER\_PE\_MASK( *n* ) (0x1u << MPU\_REGION\_RWXRIGHTS\_MASTER\_PE\_SHIFT(*n*))**

25.5.8 **#define MPU\_REGION\_RWXRIGHTS\_MASTER\_PE( *n*, *x* ) (((uint32\_t)(((uint32\_t)(x)) << MPU\_REGION\_RWXRIGHTS\_MASTER\_PE\_SHIFT(*n*))) & MPU\_REGION\_RWXRIGHTS\_MASTER\_PE\_MASK(*n*))**

25.5.9 **#define MPU\_REGION\_RWRIGHTS\_MASTER\_SHIFT( *n* ) ((*n* - FSL\_FEATURE\_MPU\_PRIVILEGED\_RIGHTS\_MASTER\_COUNT) \* 2 + 24)**

25.5.10 **#define MPU\_REGION\_RWRIGHTS\_MASTER\_MASK( *n* ) (0x3u << MPU\_REGION\_RWRIGHTS\_MASTER\_SHIFT(*n*))**

25.5.11 **#define MPU\_REGION\_RWRIGHTS\_MASTER( *n*, *x* ) (((uint32\_t)(((uint32\_t)(x)) << MPU\_REGION\_RWRIGHTS\_MASTER\_SHIFT(*n*))) & MPU\_REGION\_RWRIGHTS\_MASTER\_MASK(*n*))**

25.5.12 **#define MPU\_SLAVE\_PORT\_NUM (4u)**

25.5.13 **#define MPU\_PRIVILEGED\_RIGHTS\_MASTER\_MAX\_INDEX (3)**

### 25.6 Enumeration Type Documentation

#### 25.6.1 enum mpu\_region\_total\_num\_t

Enumerator

*kMPU\_8Regions* MPU supports 8 regions.  
*kMPU\_12Regions* MPU supports 12 regions.  
*kMPU\_16Regions* MPU supports 16 regions.

#### 25.6.2 enum mpu\_slave\_t

Enumerator

*kMPU\_Slave0* MPU slave port 0.  
*kMPU\_Slave1* MPU slave port 1.  
*kMPU\_Slave2* MPU slave port 2.  
*kMPU\_Slave3* MPU slave port 3.  
*kMPU\_Slave4* MPU slave port 4.

#### 25.6.3 enum mpu\_err\_access\_control\_t

Enumerator

*kMPU\_NoRegionHit* No region hit error.  
*kMPU\_NoneOverlappRegion* Access single region error.  
*kMPU\_OverlappRegion* Access overlapping region error.

#### 25.6.4 enum mpu\_err\_access\_type\_t

Enumerator

*kMPU\_ErrTypeRead* MPU error access type — read.  
*kMPU\_ErrTypeWrite* MPU error access type — write.

#### 25.6.5 enum mpu\_err\_attributes\_t

Enumerator

*kMPU\_InstructionAccessInUserMode* Access instruction error in user mode.  
*kMPU\_DataAccessInUserMode* Access data error in user mode.  
*kMPU\_InstructionAccessInSupervisorMode* Access instruction error in supervisor mode.  
*kMPU\_DataAccessInSupervisorMode* Access data error in supervisor mode.

### 25.6.6 enum mpu\_supervisor\_access\_rights\_t

Enumerator

***kMPU\_SupervisorReadWriteExecute*** Read write and execute operations are allowed in supervisor mode.

***kMPU\_SupervisorReadExecute*** Read and execute operations are allowed in supervisor mode.

***kMPU\_SupervisorReadWrite*** Read write operations are allowed in supervisor mode.

***kMPU\_SupervisorEqualToUsermode*** Access permission equal to user mode.

### 25.6.7 enum mpu\_user\_access\_rights\_t

Enumerator

***kMPU\_UserNoAccessRights*** No access allowed in user mode.

***kMPU\_UserExecute*** Execute operation is allowed in user mode.

***kMPU\_UserWrite*** Write operation is allowed in user mode.

***kMPU\_UserWriteExecute*** Write and execute operations are allowed in user mode.

***kMPU\_UserRead*** Read is allowed in user mode.

***kMPU\_UserReadExecute*** Read and execute operations are allowed in user mode.

***kMPU\_UserReadWrite*** Read and write operations are allowed in user mode.

***kMPU\_UserReadWriteExecute*** Read write and execute operations are allowed in user mode.

## 25.7 Function Documentation

### 25.7.1 void MPU\_Init ( MPU\_Type \* *base*, const mpu\_config\_t \* *config* )

This function configures the MPU module with the user-defined configuration.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | MPU peripheral base address.                |
| <i>config</i> | The pointer to the configuration structure. |

### 25.7.2 void MPU\_Deinit ( MPU\_Type \* *base* )

Parameters

## Function Documentation

|             |                              |
|-------------|------------------------------|
| <i>base</i> | MPU peripheral base address. |
|-------------|------------------------------|

### 25.7.3 static void MPU\_Enable ( MPU\_Type \* *base*, bool *enable* ) [inline], [static]

Call this API to enable or disable the MPU module.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | MPU peripheral base address.        |
| <i>enable</i> | True enable MPU, false disable MPU. |

### 25.7.4 static void MPU\_RegionEnable ( MPU\_Type \* *base*, uint32\_t *number*, bool *enable* ) [inline], [static]

When MPU is enabled, call this API to disable an unused region of an enabled MPU. Call this API to minimize the power dissipation.

Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>base</i>   | MPU peripheral base address.                                              |
| <i>number</i> | MPU region number.                                                        |
| <i>enable</i> | True enable the special region MPU, false disable the special region MPU. |

### 25.7.5 void MPU\_GetHardwareInfo ( MPU\_Type \* *base*, mpu\_hardware\_info\_t \* *hardwareInform* )

Parameters

|                        |                                                                                   |
|------------------------|-----------------------------------------------------------------------------------|
| <i>base</i>            | MPU peripheral base address.                                                      |
| <i>hardware-Inform</i> | The pointer to the MPU hardware information structure. See "mpu_hardware_info_t". |

### 25.7.6 void MPU\_SetRegionConfig ( MPU\_Type \* *base*, const mpu\_region\_config\_t \* *regionConfig* )

Note: Due to the MPU protection, the region number 0 does not allow writes from core to affect the start and end address nor the permissions associated with the debugger. It can only write the permission fields associated with the other masters.

Parameters

|                     |                                                                                 |
|---------------------|---------------------------------------------------------------------------------|
| <i>base</i>         | MPU peripheral base address.                                                    |
| <i>regionConfig</i> | The pointer to the MPU user configuration structure. See "mpu_region_config_t". |

### 25.7.7 void MPU\_SetRegionAddr ( MPU\_Type \* *base*, uint32\_t *regionNum*, uint32\_t *startAddr*, uint32\_t *endAddr* )

Memory region start address. Note: bit0 ~ bit4 is always marked as 0 by MPU. The actual start address by MPU is 0-modulo-32 byte address. Memory region end address. Note: bit0 ~ bit4 always be marked as 1 by MPU. The end address used by the MPU is 31-modulo-32 byte address. Note: Due to the MPU protection, the startAddr and endAddr can't be changed by the core when regionNum is 0.

Parameters

|                  |                                                                                 |
|------------------|---------------------------------------------------------------------------------|
| <i>base</i>      | MPU peripheral base address.                                                    |
| <i>regionNum</i> | MPU region number. The range is from 0 to FSL_FEATURE_MPU_DESCRIPTOR_COUNT - 1. |
| <i>startAddr</i> | Region start address.                                                           |
| <i>endAddr</i>   | Region end address.                                                             |

### 25.7.8 void MPU\_SetRegionRwxMasterAccessRights ( MPU\_Type \* *base*, uint32\_t *regionNum*, uint32\_t *masterNum*, const mpu\_rwxrights\_master\_access\_control\_t \* *accessRights* )

The MPU access rights depend on two board classifications of bus masters. The privilege rights masters and the normal rights masters. The privilege rights masters have the read, write, and execute access rights. Except the normal read and write rights, the execute rights are also allowed for these masters. The privilege rights masters normally range from bus masters 0 - 3. However, the maximum master number is device-specific. See the "MPU\_PRIVILEGED\_RIGHTS\_MASTER\_MAX\_INDEX". The normal rights masters access rights control see "MPU\_SetRegionRwMasterAccessRights()".

## Function Documentation

### Parameters

|                     |                                                                                                  |
|---------------------|--------------------------------------------------------------------------------------------------|
| <i>base</i>         | MPU peripheral base address.                                                                     |
| <i>regionNum</i>    | MPU region number. Should range from 0 to FSL_FEATURE_MPU_DESCRIPTOR_COUNT - 1.                  |
| <i>masterNum</i>    | MPU bus master number. Should range from 0 to MPU_PRIVILEGED_RIGHTS_MASTER_MAX_INDEX.            |
| <i>accessRights</i> | The pointer to the MPU access rights configuration. See "mpu_rwxrights_master_access_control_t". |

**25.7.9 void MPU\_SetRegionRwMasterAccessRights ( MPU\_Type \* *base*, uint32\_t *regionNum*, uint32\_t *masterNum*, const mpu\_rwrights\_master\_access\_control\_t \* *accessRights* )**

The MPU access rights depend on two board classifications of bus masters. The privilege rights masters and the normal rights masters. The normal rights masters only have the read and write access permissions. The privilege rights access control see "MPU\_SetRegionRwxMasterAccessRights".

### Parameters

|                     |                                                                                                                                |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>         | MPU peripheral base address.                                                                                                   |
| <i>regionNum</i>    | MPU region number. The range is from 0 to FSL_FEATURE_MPU_DESCRIPTOR_COUNT - 1.                                                |
| <i>masterNum</i>    | MPU bus master number. Should range from FSL_FEATURE_MPU_PRIVILEGED_RIGHTS_MASTER_COUNT to ~ FSL_FEATURE_MPU_MASTER_MAX_INDEX. |
| <i>accessRights</i> | The pointer to the MPU access rights configuration. See "mpu_rwrights_master_access_control_t".                                |

**25.7.10 bool MPU\_GetSlavePortErrorStatus ( MPU\_Type \* *base*, mpu\_slave\_t *slaveNum* )**

### Parameters

|                 |                              |
|-----------------|------------------------------|
| <i>base</i>     | MPU peripheral base address. |
| <i>slaveNum</i> | MPU slave port number.       |



## Returns

The slave ports error status. true - error happens in this slave port. false - error didn't happen in this slave port.

**25.7.11 void MPU\_GetDetailErrorAccessInfo ( MPU\_Type \* *base*, mpu\_slave\_t *slaveNum*, mpu\_access\_err\_info\_t \* *errInform* )**

## Parameters

|                  |                                                                               |
|------------------|-------------------------------------------------------------------------------|
| <i>base</i>      | MPU peripheral base address.                                                  |
| <i>slaveNum</i>  | MPU slave port number.                                                        |
| <i>errInform</i> | The pointer to the MPU access error information. See "mpu_access_err_info_t". |



## Chapter 26

# PDB: Programmable Delay Block

### 26.1 Overview

The KSDK provides a peripheral driver for the Programmable Delay Block (PDB) module of Kinetis devices.

The PDB driver includes a basic PDB counter, trigger generators for ADC, DAC, and pulse-out.

The basic PDB counter can be used as a general programmable timer with an interrupt. The counter increases automatically with the divided clock signal after it is triggered to start by an external trigger input or the software trigger. There are "milestones" for the output trigger event. When the counter is equal to any of these "milestones", the corresponding trigger is generated and sent out to other modules. These "milestones" are for the following events.

- Counter delay interrupt, which is the interrupt for the PDB module
- ADC pre-trigger to trigger the ADC conversion
- DAC interval trigger to trigger the DAC buffer and move the buffer read pointer
- Pulse-out triggers to generate a single of rising and falling edges, which can be assembled to a window.

The "milestone" values have a flexible load mode. To call the APIs to set these value is equivalent to writing data to their buffer. The loading event occurs as the load mode describes. This design ensures that all "milestones" can be updated at the same time.

### 26.2 Typical use case

#### 26.2.1 Working as basic PDB counter with a PDB interrupt.

```
int main(void)
{
    // ...
    EnableIRQ(DEMO_PDB_IRQ_ID);

    // ...
    // Configures the PDB counter.
    PDB_GetDefaultConfig(&pdbConfigStruct);
    PDB_Init(DEMO_PDB_INSTANCE, &pdbConfigStruct);

    // Configures the delay interrupt.
    PDB_SetModulusValue(DEMO_PDB_INSTANCE, 1000U);
    PDB_SetCounterDelayValue(DEMO_PDB_INSTANCE, 1000U); // The available delay
    value is less than or equal to the modulus value.
    PDB_EnableInterrupts(DEMO_PDB_INSTANCE,
        kPDB_DelayInterruptEnable);
    PDB_DoLoadValues(DEMO_PDB_INSTANCE);

    while (1)
    {
        // ...
        g_PdbDelayInterruptFlag = false;
    }
}
```

## Typical use case

```
PDB_DoSoftwareTrigger (DEMO_PDB_INSTANCE);
while (!g_PdbDelayInterruptFlag)
{
}
}

void DEMO_PDB_IRQ_HANDLER_FUNC(void)
{
    // ...
    g_PdbDelayInterruptFlag = true;
    PDB_ClearStatusFlags (DEMO_PDB_INSTANCE,
        kPDB_DelayEventFlag);
}
```

### 26.2.2 Working with an additional trigger. The ADC trigger is used as an example.

```
void DEMO_PDB_IRQ_HANDLER_FUNC(void)
{
    PDB_ClearStatusFlags (DEMO_PDB_INSTANCE,
        kPDB_DelayEventFlag);
    g_PdbDelayInterruptCounter++;
    g_PdbDelayInterruptFlag = true;
}

void DEMO_PDB_InitADC(void)
{
    adc16_config_t adc16ConfigStruct;
    adc16_channel_config_t adc16ChannelConfigStruct;

    ADC16_GetDefaultConfig(&adc16ConfigStruct);
    ADC16_Init (DEMO_PDB_ADC_INSTANCE, &adc16ConfigStruct);
#if defined(FSL_FEATURE_ADC16_HAS_CALIBRATION) && FSL_FEATURE_ADC16_HAS_CALIBRATION
    ADC16_EnableHardwareTrigger (DEMO_PDB_ADC_INSTANCE, false);
    ADC16_DoAutoCalibration (DEMO_PDB_ADC_INSTANCE);
#endif /* FSL_FEATURE_ADC16_HAS_CALIBRATION */
    ADC16_EnableHardwareTrigger (DEMO_PDB_ADC_INSTANCE, true);

    adc16ChannelConfigStruct.channelNumber = DEMO_PDB_ADC_USER_CHANNEL;
    adc16ChannelConfigStruct.enableInterruptOnConversionCompleted =
        true; /* Enable the interrupt. */
#if defined(FSL_FEATURE_ADC16_HAS_DIFF_MODE) && FSL_FEATURE_ADC16_HAS_DIFF_MODE
    adc16ChannelConfigStruct.enabledDifferentialConversion = false;
#endif /* FSL_FEATURE_ADC16_HAS_DIFF_MODE */
    ADC16_SetChannelConfig (DEMO_PDB_ADC_INSTANCE, DEMO_PDB_ADC_CHANNEL_GROUP, &
        adc16ChannelConfigStruct);
}

void DEMO_PDB_ADC_IRQ_HANDLER_FUNCTION(void)
{
    uint32_t tmp32;

    tmp32 = ADC16_GetChannelConversionValue (DEMO_PDB_ADC_INSTANCE,
        DEMO_PDB_ADC_CHANNEL_GROUP); /* Read to clear COCO flag. */
    g_AdcInterruptCounter++;
    g_AdcInterruptFlag = true;
}

int main(void)
{
    // ...

    EnableIRQ (DEMO_PDB_IRQ_ID);
    EnableIRQ (DEMO_PDB_ADC_IRQ_ID);
}
```

```

// ...

// Configures the PDB counter.
PDB_GetDefaultConfig(&pdbConfigStruct);
PDB_Init(DEMO_PDB_INSTANCE, &pdbConfigStruct);

// Configures the delay interrupt.
PDB_SetModulusValue(DEMO_PDB_INSTANCE, 1000U);
PDB_SetCounterDelayValue(DEMO_PDB_INSTANCE, 1000U); // The available delay
value is less than or equal to the modulus value.
PDB_EnableInterrupts(DEMO_PDB_INSTANCE,
    kPDB_DelayInterruptEnable);

// Configures the ADC pre-trigger.
pdbAdcPreTriggerConfigStruct.enablePreTriggerMask = 1U << DEMO_PDB_ADC_PRETRIGGER_CHANNEL;
pdbAdcPreTriggerConfigStruct.enableOutputMask = 1U << DEMO_PDB_ADC_PRETRIGGER_CHANNEL;
pdbAdcPreTriggerConfigStruct.enableBackToBackOperationMask = 0U;
PDB_SetADCPreTriggerConfig(DEMO_PDB_INSTANCE, DEMO_PDB_ADC_TRIGGER_CHANNEL, &
    pdbAdcPreTriggerConfigStruct);
PDB_SetADCPreTriggerDelayValue(DEMO_PDB_INSTANCE,
    DEMO_PDB_ADC_TRIGGER_CHANNEL, DEMO_PDB_ADC_PRETRIGGER_CHANNEL, 200U);
// The available pre-trigger delay value is less than or equal to the modulus
value.

PDB_DoLoadValues(DEMO_PDB_INSTANCE);

// Configures the ADC.
DEMO_PDB_InitADC();

while (1)
{
    g_PdbDelayInterruptFlag = false;
    g_AdcInterruptFlag = false;
    PDB_DoSoftwareTrigger(DEMO_PDB_INSTANCE);
    while ((!g_PdbDelayInterruptFlag) || (!g_AdcInterruptFlag))
    {
        // ...
    }
}

```

## Data Structures

- struct [pdb\\_config\\_t](#)  
*PDB module configuration. [More...](#)*
- struct [pdb\\_adc\\_pretrigger\\_config\\_t](#)  
*PDB ADC Pre-trigger configuration. [More...](#)*
- struct [pdb\\_dac\\_trigger\\_config\\_t](#)  
*PDB DAC trigger configuration. [More...](#)*

## Enumerations

- enum [\\_pdb\\_status\\_flags](#) {  
    [kPDB\\_LoadOKFlag](#) = PDB\_SC\_LDOK\_MASK,  
    [kPDB\\_DelayEventFlag](#) = PDB\_SC\_PDBIF\_MASK }  
*PDB flags.*
- enum [\\_pdb\\_adc\\_pretrigger\\_flags](#) {  
    [kPDB\\_ADCPreTriggerChannel0Flag](#) = PDB\_S\_CF(1U << 0),  
    [kPDB\\_ADCPreTriggerChannel1Flag](#) = PDB\_S\_CF(1U << 1),  
    [kPDB\\_ADCPreTriggerChannel0ErrorFlag](#) = PDB\_S\_ERR(1U << 0),

## Typical use case

```
kPDB_ADCPreTriggerChannel1ErrorFlag = PDB_S_ERR(1U << 1) }
```

*PDB ADC PreTrigger channel flags.*

- enum `_pdb_interrupt_enable` {  
    `kPDB_SequenceErrorInterruptEnable` = `PDB_SC_PDBEIE_MASK`,  
    `kPDB_DelayInterruptEnable` = `PDB_SC_PDBIE_MASK` }

*PDB buffer interrupts.*

- enum `pdb_load_value_mode_t` {  
    `kPDB_LoadValueImmediately` = 0U,  
    `kPDB_LoadValueOnCounterOverflow` = 1U,  
    `kPDB_LoadValueOnTriggerInput` = 2U,  
    `kPDB_LoadValueOnCounterOverflowOrTriggerInput` = 3U }

*PDB load value mode.*

- enum `pdb_prescaler_divider_t` {  
    `kPDB_PrescalerDivider1` = 0U,  
    `kPDB_PrescalerDivider2` = 1U,  
    `kPDB_PrescalerDivider4` = 2U,  
    `kPDB_PrescalerDivider8` = 3U,  
    `kPDB_PrescalerDivider16` = 4U,  
    `kPDB_PrescalerDivider32` = 5U,  
    `kPDB_PrescalerDivider64` = 6U,  
    `kPDB_PrescalerDivider128` = 7U }

*Prescaler divider.*

- enum `pdb_divider_multiplication_factor_t` {  
    `kPDB_DividerMultiplicationFactor1` = 0U,  
    `kPDB_DividerMultiplicationFactor10` = 1U,  
    `kPDB_DividerMultiplicationFactor20` = 2U,  
    `kPDB_DividerMultiplicationFactor40` = 3U }

*Multiplication factor select for prescaler.*

- enum `pdb_trigger_input_source_t` {  
    `kPDB_TriggerInput0` = 0U,  
    `kPDB_TriggerInput1` = 1U,  
    `kPDB_TriggerInput2` = 2U,  
    `kPDB_TriggerInput3` = 3U,  
    `kPDB_TriggerInput4` = 4U,  
    `kPDB_TriggerInput5` = 5U,  
    `kPDB_TriggerInput6` = 6U,  
    `kPDB_TriggerInput7` = 7U,  
    `kPDB_TriggerInput8` = 8U,  
    `kPDB_TriggerInput9` = 9U,  
    `kPDB_TriggerInput10` = 10U,  
    `kPDB_TriggerInput11` = 11U,  
    `kPDB_TriggerInput12` = 12U,  
    `kPDB_TriggerInput13` = 13U,  
    `kPDB_TriggerInput14` = 14U,  
    `kPDB_TriggerSoftware` = 15U }

*Trigger input source.*

## Driver version

- #define **FSL\_PDB\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 0, 1))  
*PDB driver version 2.0.1.*

## Initialization

- void **PDB\_Init** (PDB\_Type \*base, const **pdb\_config\_t** \*config)  
*Initializes the PDB module.*
- void **PDB\_Deinit** (PDB\_Type \*base)  
*De-initializes the PDB module.*
- void **PDB\_GetDefaultConfig** (**pdb\_config\_t** \*config)  
*Initializes the PDB user configuration structure.*
- static void **PDB\_Enable** (PDB\_Type \*base, bool enable)  
*Enables the PDB module.*

## Basic Counter

- static void **PDB\_DoSoftwareTrigger** (PDB\_Type \*base)  
*Triggers the PDB counter by software.*
- static void **PDB\_DoLoadValues** (PDB\_Type \*base)  
*Loads the counter values.*
- static void **PDB\_EnableDMA** (PDB\_Type \*base, bool enable)  
*Enables the DMA for the PDB module.*
- static void **PDB\_EnableInterrupts** (PDB\_Type \*base, uint32\_t mask)  
*Enables the interrupts for the PDB module.*
- static void **PDB\_DisableInterrupts** (PDB\_Type \*base, uint32\_t mask)  
*Disables the interrupts for the PDB module.*
- static uint32\_t **PDB\_GetStatusFlags** (PDB\_Type \*base)  
*Gets the status flags of the PDB module.*
- static void **PDB\_ClearStatusFlags** (PDB\_Type \*base, uint32\_t mask)  
*Clears the status flags of the PDB module.*
- static void **PDB\_SetModulusValue** (PDB\_Type \*base, uint32\_t value)  
*Specifies the counter period.*
- static uint32\_t **PDB\_GetCounterValue** (PDB\_Type \*base)  
*Gets the PDB counter's current value.*
- static void **PDB\_SetCounterDelayValue** (PDB\_Type \*base, uint32\_t value)  
*Sets the value for the PDB counter delay event.*

## ADC Pre-trigger

- static void **PDB\_SetADCPreTriggerConfig** (PDB\_Type \*base, uint32\_t channel, **pdb\_adc\_pretrigger\_config\_t** \*config)  
*Configures the ADC pre-trigger in the PDB module.*
- static void **PDB\_SetADCPreTriggerDelayValue** (PDB\_Type \*base, uint32\_t channel, uint32\_t pre-Channel, uint32\_t value)  
*Sets the value for the ADC pre-trigger delay event.*
- static uint32\_t **PDB\_GetADCPreTriggerStatusFlags** (PDB\_Type \*base, uint32\_t channel)  
*Gets the ADC pre-trigger's status flags.*
- static void **PDB\_ClearADCPreTriggerStatusFlags** (PDB\_Type \*base, uint32\_t channel, uint32\_t mask)

## Data Structure Documentation

*Clears the ADC pre-trigger status flags.*

### DAC Interval Trigger

- void [PDB\\_SetDACTriggerConfig](#) (PDB\_Type \*base, uint32\_t channel, [pdb\\_dac\\_trigger\\_config\\_t](#) \*config)  
*Configures the DAC trigger in the PDB module.*
- static void [PDB\\_SetDACTriggerIntervalValue](#) (PDB\_Type \*base, uint32\_t channel, uint32\_t value)  
*Sets the value for the DAC interval event.*

### Pulse-Out Trigger

- static void [PDB\\_EnablePulseOutTrigger](#) (PDB\_Type \*base, uint32\_t channelMask, bool enable)  
*Enables the pulse out trigger channels.*
- static void [PDB\\_SetPulseOutTriggerDelayValue](#) (PDB\_Type \*base, uint32\_t channel, uint32\_t value1, uint32\_t value2)  
*Sets event values for the pulse out trigger.*

## 26.3 Data Structure Documentation

### 26.3.1 struct [pdb\\_config\\_t](#)

#### Data Fields

- [pdb\\_load\\_value\\_mode\\_t](#) loadValueMode  
*Select the load value mode.*
- [pdb\\_prescaler\\_divider\\_t](#) prescalerDivider  
*Select the prescaler divider.*
- [pdb\\_divider\\_multiplication\\_factor\\_t](#) dividerMultiplicationFactor  
*Multiplication factor select for prescaler.*
- [pdb\\_trigger\\_input\\_source\\_t](#) triggerInputSource  
*Select the trigger input source.*
- bool [enableContinuousMode](#)  
*Enable the PDB operation in Continuous mode.*



**26.3.1.0.0.75 Field Documentation****26.3.1.0.0.75.1** `pdb_load_value_mode_t` `pdb_config_t::loadValueMode`**26.3.1.0.0.75.2** `pdb_prescaler_divider_t` `pdb_config_t::prescalerDivider`**26.3.1.0.0.75.3** `pdb_divider_multiplication_factor_t` `pdb_config_t::dividerMultiplicationFactor`**26.3.1.0.0.75.4** `pdb_trigger_input_source_t` `pdb_config_t::triggerInputSource`**26.3.1.0.0.75.5** `bool` `pdb_config_t::enableContinuousMode`**26.3.2 struct `pdb_adc_pretrigger_config_t`****Data Fields**

- `uint32_t` [enablePreTriggerMask](#)  
*PDB Channel Pre-trigger Enable.*
- `uint32_t` [enableOutputMask](#)  
*PDB Channel Pre-trigger Output Select.*
- `uint32_t` [enableBackToBackOperationMask](#)  
*PDB Channel pre-trigger Back-to-Back Operation Enable.*

**26.3.2.0.0.76 Field Documentation****26.3.2.0.0.76.1** `uint32_t` `pdb_adc_pretrigger_config_t::enablePreTriggerMask`**26.3.2.0.0.76.2** `uint32_t` `pdb_adc_pretrigger_config_t::enableOutputMask`

PDB channel's corresponding pre-trigger asserts when the counter reaches the channel delay register.

**26.3.2.0.0.76.3** `uint32_t` `pdb_adc_pretrigger_config_t::enableBackToBackOperationMask`

Back-to-back operation enables the ADC conversions complete to trigger the next PDB channel pre-trigger and trigger output, so that the ADC conversions can be triggered on next set of configuration and results registers.

**26.3.3 struct `pdb_dac_trigger_config_t`****Data Fields**

- `bool` [enableExternalTriggerInput](#)  
*Enables the external trigger for DAC interval counter.*
- `bool` [enableIntervalTrigger](#)  
*Enables the DAC interval trigger.*

## Enumeration Type Documentation

### 26.3.3.0.0.77 Field Documentation

26.3.3.0.0.77.1 bool pdb\_dac\_trigger\_config\_t::enableExternalTriggerInput

26.3.3.0.0.77.2 bool pdb\_dac\_trigger\_config\_t::enableIntervalTrigger

## 26.4 Macro Definition Documentation

26.4.1 #define FSL\_PDB\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

## 26.5 Enumeration Type Documentation

### 26.5.1 enum \_pdb\_status\_flags

Enumerator

***kPDB\_LoadOKFlag*** This flag is automatically cleared when the values in buffers are loaded into the internal registers after the LDOK bit is set or the PDBEN is cleared.

***kPDB\_DelayEventFlag*** PDB timer delay event flag.

### 26.5.2 enum \_pdb\_adc\_pretrigger\_flags

Enumerator

***kPDB\_ADCPreTriggerChannel0Flag*** Pre-trigger 0 flag.

***kPDB\_ADCPreTriggerChannel1Flag*** Pre-trigger 1 flag.

***kPDB\_ADCPreTriggerChannel0ErrorFlag*** Pre-trigger 0 Error.

***kPDB\_ADCPreTriggerChannel1ErrorFlag*** Pre-trigger 1 Error.

### 26.5.3 enum \_pdb\_interrupt\_enable

Enumerator

***kPDB\_SequenceErrorInterruptEnable*** PDB sequence error interrupt enable.

***kPDB\_DelayInterruptEnable*** PDB delay interrupt enable.

### 26.5.4 enum pdb\_load\_value\_mode\_t

Selects the mode to load the internal values after doing the load operation (write 1 to PDBx\_SC[LDOK]). These values are for the following operations.

- PDB counter (PDBx\_MOD, PDBx\_IDLY)
- ADC trigger (PDBx\_CHnDLYm)

- DAC trigger (PDBx\_DACINTx)
- CMP trigger (PDBx\_POyDLY)

Enumerator

***kPDB\_LoadValueImmediately*** Load immediately after 1 is written to LDOK.

***kPDB\_LoadValueOnCounterOverflow*** Load when the PDB counter overflows (reaches the MOD register value).

***kPDB\_LoadValueOnTriggerInput*** Load a trigger input event is detected.

***kPDB\_LoadValueOnCounterOverflowOrTriggerInput*** Load either when the PDB counter overflows or a trigger input is detected.

### 26.5.5 enum pdb\_prescaler\_divider\_t

Counting uses the peripheral clock divided by multiplication factor selected by times of MULT.

Enumerator

***kPDB\_PrescalerDivider1*** Divider x1.

***kPDB\_PrescalerDivider2*** Divider x2.

***kPDB\_PrescalerDivider4*** Divider x4.

***kPDB\_PrescalerDivider8*** Divider x8.

***kPDB\_PrescalerDivider16*** Divider x16.

***kPDB\_PrescalerDivider32*** Divider x32.

***kPDB\_PrescalerDivider64*** Divider x64.

***kPDB\_PrescalerDivider128*** Divider x128.

### 26.5.6 enum pdb\_divider\_multiplication\_factor\_t

Selects the multiplication factor of the prescaler divider for the counter clock.

Enumerator

***kPDB\_DividerMultiplicationFactor1*** Multiplication factor is 1.

***kPDB\_DividerMultiplicationFactor10*** Multiplication factor is 10.

***kPDB\_DividerMultiplicationFactor20*** Multiplication factor is 20.

***kPDB\_DividerMultiplicationFactor40*** Multiplication factor is 40.

### 26.5.7 enum pdb\_trigger\_input\_source\_t

Selects the trigger input source for the PDB. The trigger input source can be internal or external (EXTRG pin), or the software trigger. See chip configuration details for the actual PDB input trigger connections.

## Function Documentation

### Enumerator

***kPDB\_TriggerInput0*** Trigger-In 0.  
***kPDB\_TriggerInput1*** Trigger-In 1.  
***kPDB\_TriggerInput2*** Trigger-In 2.  
***kPDB\_TriggerInput3*** Trigger-In 3.  
***kPDB\_TriggerInput4*** Trigger-In 4.  
***kPDB\_TriggerInput5*** Trigger-In 5.  
***kPDB\_TriggerInput6*** Trigger-In 6.  
***kPDB\_TriggerInput7*** Trigger-In 7.  
***kPDB\_TriggerInput8*** Trigger-In 8.  
***kPDB\_TriggerInput9*** Trigger-In 9.  
***kPDB\_TriggerInput10*** Trigger-In 10.  
***kPDB\_TriggerInput11*** Trigger-In 11.  
***kPDB\_TriggerInput12*** Trigger-In 12.  
***kPDB\_TriggerInput13*** Trigger-In 13.  
***kPDB\_TriggerInput14*** Trigger-In 14.  
***kPDB\_TriggerSoftware*** Trigger-In 15, software trigger.

## 26.6 Function Documentation

### 26.6.1 void PDB\_Init ( PDB\_Type \* *base*, const pdb\_config\_t \* *config* )

This function initializes the PDB module. The operations included are as follows.

- Enable the clock for PDB instance.
- Configure the PDB module.
- Enable the PDB module.

#### Parameters

|               |                                                             |
|---------------|-------------------------------------------------------------|
| <i>base</i>   | PDB peripheral base address.                                |
| <i>config</i> | Pointer to the configuration structure. See "pdb_config_t". |

### 26.6.2 void PDB\_Deinit ( PDB\_Type \* *base* )

#### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PDB peripheral base address. |
|-------------|------------------------------|

### 26.6.3 void PDB\_GetDefaultConfig ( pdb\_config\_t \* *config* )

This function initializes the user configuration structure to a default value. The default values are as follows.

```
* config->loadValueMode = kPDB_LoadValueImmediately;
* config->prescalerDivider = kPDB_PrescalerDivider1;
* config->dividerMultiplicationFactor = kPDB_DividerMultiplicationFactor1
* ;
* config->triggerInputSource = kPDB_TriggerSoftware;
* config->enableContinuousMode = false;
*
```

Parameters

|               |                                                         |
|---------------|---------------------------------------------------------|
| <i>config</i> | Pointer to configuration structure. See "pdb_config_t". |
|---------------|---------------------------------------------------------|

### 26.6.4 static void PDB\_Enable ( PDB\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | PDB peripheral base address. |
| <i>enable</i> | Enable the module or not.    |

### 26.6.5 static void PDB\_DoSoftwareTrigger ( PDB\_Type \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PDB peripheral base address. |
|-------------|------------------------------|

### 26.6.6 static void PDB\_DoLoadValues ( PDB\_Type \* *base* ) [inline], [static]

This function loads the counter values from the internal buffer. See "pdb\_load\_value\_mode\_t" about PDB's load mode.

## Function Documentation

### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PDB peripheral base address. |
|-------------|------------------------------|

**26.6.7 static void PDB\_EnableDMA ( PDB\_Type \* *base*, bool *enable* ) [inline], [static]**

### Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | PDB peripheral base address. |
| <i>enable</i> | Enable the feature or not.   |

**26.6.8 static void PDB\_EnableInterrupts ( PDB\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

### Parameters

|             |                                                         |
|-------------|---------------------------------------------------------|
| <i>base</i> | PDB peripheral base address.                            |
| <i>mask</i> | Mask value for interrupts. See "_pdb_interrupt_enable". |

**26.6.9 static void PDB\_DisableInterrupts ( PDB\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

### Parameters

|             |                                                         |
|-------------|---------------------------------------------------------|
| <i>base</i> | PDB peripheral base address.                            |
| <i>mask</i> | Mask value for interrupts. See "_pdb_interrupt_enable". |

**26.6.10 static uint32\_t PDB\_GetStatusFlags ( PDB\_Type \* *base* ) [inline], [static]**

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PDB peripheral base address. |
|-------------|------------------------------|

## Returns

Mask value for asserted flags. See "\_pdb\_status\_flags".

**26.6.11 static void PDB\_ClearStatusFlags ( PDB\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

## Parameters

|             |                                               |
|-------------|-----------------------------------------------|
| <i>base</i> | PDB peripheral base address.                  |
| <i>mask</i> | Mask value of flags. See "_pdb_status_flags". |

**26.6.12 static void PDB\_SetModulusValue ( PDB\_Type \* *base*, uint32\_t *value* ) [inline], [static]**

## Parameters

|              |                                                     |
|--------------|-----------------------------------------------------|
| <i>base</i>  | PDB peripheral base address.                        |
| <i>value</i> | Setting value for the modulus. 16-bit is available. |

**26.6.13 static uint32\_t PDB\_GetCounterValue ( PDB\_Type \* *base* ) [inline], [static]**

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PDB peripheral base address. |
|-------------|------------------------------|

## Returns

PDB counter's current value.

**26.6.14 static void PDB\_SetCounterDelayValue ( PDB\_Type \* *base*, uint32\_t *value* ) [inline], [static]**

## Function Documentation

### Parameters

|              |                                                                 |
|--------------|-----------------------------------------------------------------|
| <i>base</i>  | PDB peripheral base address.                                    |
| <i>value</i> | Setting value for PDB counter delay event. 16-bit is available. |

**26.6.15 static void PDB\_SetADCPreTriggerConfig ( PDB\_Type \* *base*, uint32\_t *channel*, pdb\_adc\_pretrigger\_config\_t \* *config* ) [inline], [static]**

### Parameters

|                |                                                                            |
|----------------|----------------------------------------------------------------------------|
| <i>base</i>    | PDB peripheral base address.                                               |
| <i>channel</i> | Channel index for ADC instance.                                            |
| <i>config</i>  | Pointer to the configuration structure. See "pdb_adc_pretrigger_config_t". |

**26.6.16 static void PDB\_SetADCPreTriggerDelayValue ( PDB\_Type \* *base*, uint32\_t *channel*, uint32\_t *preChannel*, uint32\_t *value* ) [inline], [static]**

This function sets the value for ADC pre-trigger delay event. It specifies the delay value for the channel's corresponding pre-trigger. The pre-trigger asserts when the PDB counter is equal to the set value.

### Parameters

|                   |                                                                     |
|-------------------|---------------------------------------------------------------------|
| <i>base</i>       | PDB peripheral base address.                                        |
| <i>channel</i>    | Channel index for ADC instance.                                     |
| <i>preChannel</i> | Channel group index for ADC instance.                               |
| <i>value</i>      | Setting value for ADC pre-trigger delay event. 16-bit is available. |

**26.6.17 static uint32\_t PDB\_GetADCPreTriggerStatusFlags ( PDB\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

### Parameters

|                |                                 |
|----------------|---------------------------------|
| <i>base</i>    | PDB peripheral base address.    |
| <i>channel</i> | Channel index for ADC instance. |



## Returns

Mask value for asserted flags. See "\_pdb\_adc\_pretrigger\_flags".

**26.6.18 static void PDB\_ClearADCPreTriggerStatusFlags ( PDB\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* ) [inline], [static]**

## Parameters

|                |                                                        |
|----------------|--------------------------------------------------------|
| <i>base</i>    | PDB peripheral base address.                           |
| <i>channel</i> | Channel index for ADC instance.                        |
| <i>mask</i>    | Mask value for flags. See "_pdb_adc_pretrigger_flags". |

**26.6.19 void PDB\_SetDACTriggerConfig ( PDB\_Type \* *base*, uint32\_t *channel*, pdb\_dac\_trigger\_config\_t \* *config* )**

## Parameters

|                |                                                                         |
|----------------|-------------------------------------------------------------------------|
| <i>base</i>    | PDB peripheral base address.                                            |
| <i>channel</i> | Channel index for DAC instance.                                         |
| <i>config</i>  | Pointer to the configuration structure. See "pdb_dac_trigger_config_t". |

**26.6.20 static void PDB\_SetDACTriggerIntervalValue ( PDB\_Type \* *base*, uint32\_t *channel*, uint32\_t *value* ) [inline], [static]**

This function sets the value for DAC interval event. DAC interval trigger triggers the DAC module to update the buffer when the DAC interval counter is equal to the set value.

## Parameters

|                |                                           |
|----------------|-------------------------------------------|
| <i>base</i>    | PDB peripheral base address.              |
| <i>channel</i> | Channel index for DAC instance.           |
| <i>value</i>   | Setting value for the DAC interval event. |

**26.6.21 static void PDB\_EnablePulseOutTrigger ( PDB\_Type \* *base*, uint32\_t *channelMask*, bool *enable* ) [inline], [static]**

## Function Documentation

### Parameters

|                    |                                                            |
|--------------------|------------------------------------------------------------|
| <i>base</i>        | PDB peripheral base address.                               |
| <i>channelMask</i> | Channel mask value for multiple pulse out trigger channel. |
| <i>enable</i>      | Whether the feature is enabled or not.                     |

### 26.6.22 static void PDB\_SetPulseOutTriggerDelayValue ( PDB\_Type \* *base*, uint32\_t *channel*, uint32\_t *value1*, uint32\_t *value2* ) [inline], [static]

This function is used to set event values for the pulse output trigger. These pulse output trigger delay values specify the delay for the PDB Pulse-out. Pulse-out goes high when the PDB counter is equal to the pulse output high value (*value1*). Pulse-out goes low when the PDB counter is equal to the pulse output low value (*value2*).

### Parameters

|                |                                              |
|----------------|----------------------------------------------|
| <i>base</i>    | PDB peripheral base address.                 |
| <i>channel</i> | Channel index for pulse out trigger channel. |
| <i>value1</i>  | Setting value for pulse out high.            |
| <i>value2</i>  | Setting value for pulse out low.             |

## Chapter 27

### PIT: Periodic Interrupt Timer

#### 27.1 Overview

The KSDK provides a driver for the Periodic Interrupt Timer (PIT) of Kinetis devices.

#### 27.2 Function groups

The PIT driver supports operating the module as a time counter.

##### 27.2.1 Initialization and deinitialization

The function `PIT_Init()` initializes the PIT with specified configurations. The function `PIT_GetDefaultConfig()` gets the default configurations. The initialization function configures the PIT operation in debug mode.

The function `PIT_SetTimerChainMode()` configures the chain mode operation of each PIT channel.

The function `PIT_Deinit()` disables the PIT timers and disables the module clock.

##### 27.2.2 Timer period Operations

The function `PITR_SetTimerPeriod()` sets the timer period in units of count. Timers begin counting down from the value set by this function until it reaches 0.

The function `PIT_GetCurrentTimerCount()` reads the current timer counting value. This function returns the real-time timer counting value, in a range from 0 to a timer period.

The timer period operation functions takes the count value in ticks. Users can call the utility macros provided in `fsl_common.h` to convert to microseconds or milliseconds.

##### 27.2.3 Start and Stop timer operations

The function `PIT_StartTimer()` starts the timer counting. After calling this function, the timer loads the period value set earlier via the `PIT_SetPeriod()` function and starts counting down to 0. When the timer reaches 0, it generates a trigger pulse and sets the timeout interrupt flag.

The function `PIT_StopTimer()` stops the timer counting.

## Typical use case

### 27.2.4 Status

Provides functions to get and clear the PIT status.

### 27.2.5 Interrupt

Provides functions to enable/disable PIT interrupts and get current enabled interrupts.

## 27.3 Typical use case

### 27.3.1 PIT tick example

Updates the PIT period and toggles an LED periodically.

```
int main(void)
{
    /* Structure of initialize PIT */
    pit_config_t pitConfig;

    /* Initialize and enable LED */
    LED_INIT();

    /* Board pin, clock, debug console init */
    BOARD_InitHardware();

    PIT_GetDefaultConfig(&pitConfig);

    /* Init pit module */
    PIT_Init(PIT, &pitConfig);

    /* Set timer period for channel 0 */
    PIT_SetTimerPeriod(PIT, kPIT_Chnl_0, USEC_TO_COUNT(1000000U,
        PIT_SOURCE_CLOCK));

    /* Enable timer interrupts for channel 0 */
    PIT_EnableInterrupts(PIT, kPIT_Chnl_0,
        kPIT_TimerInterruptEnable);

    /* Enable at the NVIC */
    EnableIRQ(PIT_IRQ_ID);

    /* Start channel 0 */
    PRINTF("\r\nStarting channel No.0 ...");
    PIT_StartTimer(PIT, kPIT_Chnl_0);

    while (true)
    {
        /* Check whether occur interrupt and toggle LED */
        if (true == pitIsrFlag)
        {
            PRINTF("\r\n Channel No.0 interrupt is occurred !");
            LED_TOGGLE();
            pitIsrFlag = false;
        }
    }
}
```

## Data Structures

- struct [pit\\_config\\_t](#)  
*PIT configuration structure. [More...](#)*

## Enumerations

- enum [pit\\_chnl\\_t](#) {  
  [kPIT\\_Chnl\\_0](#) = 0U,  
  [kPIT\\_Chnl\\_1](#),  
  [kPIT\\_Chnl\\_2](#),  
  [kPIT\\_Chnl\\_3](#) }  
*List of PIT channels.*
- enum [pit\\_interrupt\\_enable\\_t](#) { [kPIT\\_TimerInterruptEnable](#) = [PIT\\_TCTRL\\_TIE\\_MASK](#) }  
*List of PIT interrupts.*
- enum [pit\\_status\\_flags\\_t](#) { [kPIT\\_TimerFlag](#) = [PIT\\_TFLG\\_TIF\\_MASK](#) }  
*List of PIT status flags.*

## Functions

- [uint64\\_t PIT\\_GetLifetimeTimerCount](#) ([PIT\\_Type](#) \*base)  
*Reads the current lifetime counter value.*

## Driver version

- #define [FSL\\_PIT\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 0, 0))  
*Version 2.0.0.*

## Initialization and deinitialization

- void [PIT\\_Init](#) ([PIT\\_Type](#) \*base, const [pit\\_config\\_t](#) \*config)  
*Un-gates the PIT clock, enables the PIT module, and configures the peripheral for basic operations.*
- void [PIT\\_Deinit](#) ([PIT\\_Type](#) \*base)  
*Gates the PIT clock and disables the PIT module.*
- static void [PIT\\_GetDefaultConfig](#) ([pit\\_config\\_t](#) \*config)  
*Fills in the PIT configuration structure with the default settings.*
- static void [PIT\\_SetTimerChainMode](#) ([PIT\\_Type](#) \*base, [pit\\_chnl\\_t](#) channel, bool enable)  
*Enables or disables chaining a timer with the previous timer.*

## Interrupt Interface

- static void [PIT\\_EnableInterrupts](#) ([PIT\\_Type](#) \*base, [pit\\_chnl\\_t](#) channel, [uint32\\_t](#) mask)  
*Enables the selected PIT interrupts.*
- static void [PIT\\_DisableInterrupts](#) ([PIT\\_Type](#) \*base, [pit\\_chnl\\_t](#) channel, [uint32\\_t](#) mask)  
*Disables the selected PIT interrupts.*
- static [uint32\\_t](#) [PIT\\_GetEnabledInterrupts](#) ([PIT\\_Type](#) \*base, [pit\\_chnl\\_t](#) channel)  
*Gets the enabled PIT interrupts.*

## Enumeration Type Documentation

### Status Interface

- static uint32\_t [PIT\\_GetStatusFlags](#) (PIT\_Type \*base, [pit\\_chnl\\_t](#) channel)  
*Gets the PIT status flags.*
- static void [PIT\\_ClearStatusFlags](#) (PIT\_Type \*base, [pit\\_chnl\\_t](#) channel, uint32\_t mask)  
*Clears the PIT status flags.*

### Read and Write the timer period

- static void [PIT\\_SetTimerPeriod](#) (PIT\_Type \*base, [pit\\_chnl\\_t](#) channel, uint32\_t count)  
*Sets the timer period in units of count.*
- static uint32\_t [PIT\\_GetCurrentTimerCount](#) (PIT\_Type \*base, [pit\\_chnl\\_t](#) channel)  
*Reads the current timer counting value.*

### Timer Start and Stop

- static void [PIT\\_StartTimer](#) (PIT\_Type \*base, [pit\\_chnl\\_t](#) channel)  
*Starts the timer counting.*
- static void [PIT\\_StopTimer](#) (PIT\_Type \*base, [pit\\_chnl\\_t](#) channel)  
*Stops the timer counting.*

## 27.4 Data Structure Documentation

### 27.4.1 struct pit\_config\_t

This structure holds the configuration settings for the PIT peripheral. To initialize this structure to reasonable defaults, call the [PIT\\_GetDefaultConfig\(\)](#) function and pass a pointer to your config structure instance.

The configuration structure can be made constant so it resides in flash.

### Data Fields

- bool [enableRunInDebug](#)  
*true: Timers run in debug mode; false: Timers stop in debug mode*

## 27.5 Enumeration Type Documentation

### 27.5.1 enum pit\_chnl\_t

Note

Actual number of available channels is SoC dependent

Enumerator

- kPIT\_Chnl\_0* PIT channel number 0.
- kPIT\_Chnl\_1* PIT channel number 1.

*kPIT\_Chnl\_2* PIT channel number 2.

*kPIT\_Chnl\_3* PIT channel number 3.

### 27.5.2 enum pit\_interrupt\_enable\_t

Enumerator

*kPIT\_TimerInterruptEnable* Timer interrupt enable.

### 27.5.3 enum pit\_status\_flags\_t

Enumerator

*kPIT\_TimerFlag* Timer flag.

## 27.6 Function Documentation

### 27.6.1 void PIT\_Init ( PIT\_Type \* *base*, const pit\_config\_t \* *config* )

Note

This API should be called at the beginning of the application using the PIT driver.

Parameters

|               |                                            |
|---------------|--------------------------------------------|
| <i>base</i>   | PIT peripheral base address                |
| <i>config</i> | Pointer to the user's PIT config structure |

### 27.6.2 void PIT\_Deinit ( PIT\_Type \* *base* )

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PIT peripheral base address |
|-------------|-----------------------------|

### 27.6.3 static void PIT\_GetDefaultConfig ( pit\_config\_t \* *config* ) [inline], [static]

The default values are as follows.

```
* config->enableRunInDebug = false;
*
```

## Function Documentation

### Parameters

|               |                                        |
|---------------|----------------------------------------|
| <i>config</i> | Pointer to the onfiguration structure. |
|---------------|----------------------------------------|

#### 27.6.4 static void PIT\_SetTimerChainMode ( PIT\_Type \* *base*, pit\_chnl\_t *channel*, bool *enable* ) [inline], [static]

When a timer has a chain mode enabled, it only counts after the previous timer has expired. If the timer n-1 has counted down to 0, counter n decrements the value by one. Each timer is 32-bits, which allows the developers to chain timers together and form a longer timer (64-bits and larger). The first timer (timer 0) can't be chained to any other timer.

### Parameters

|                |                                                                                                                                |
|----------------|--------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | PIT peripheral base address                                                                                                    |
| <i>channel</i> | Timer channel number which is chained with the previous timer                                                                  |
| <i>enable</i>  | Enable or disable chain. true: Current timer is chained with the previous timer. false: Timer doesn't chain with other timers. |

#### 27.6.5 static void PIT\_EnableInterrupts ( PIT\_Type \* *base*, pit\_chnl\_t *channel*, uint32\_t *mask* ) [inline], [static]

### Parameters

|                |                                                                                                                     |
|----------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | PIT peripheral base address                                                                                         |
| <i>channel</i> | Timer channel number                                                                                                |
| <i>mask</i>    | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">pit_interrupt_enable_t</a> |

#### 27.6.6 static void PIT\_DisableInterrupts ( PIT\_Type \* *base*, pit\_chnl\_t *channel*, uint32\_t *mask* ) [inline], [static]

### Parameters

|                |                                                                                                                      |
|----------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | PIT peripheral base address                                                                                          |
| <i>channel</i> | Timer channel number                                                                                                 |
| <i>mask</i>    | The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">pit_interrupt_enable_t</a> |



### 27.6.7 `static uint32_t PIT_GetEnabledInterrupts ( PIT_Type * base, pit_chnl_t channel ) [inline], [static]`

Parameters

|                |                             |
|----------------|-----------------------------|
| <i>base</i>    | PIT peripheral base address |
| <i>channel</i> | Timer channel number        |

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [pit\\_interrupt\\_enable\\_t](#)

### 27.6.8 `static uint32_t PIT_GetStatusFlags ( PIT_Type * base, pit_chnl_t channel ) [inline], [static]`

Parameters

|                |                             |
|----------------|-----------------------------|
| <i>base</i>    | PIT peripheral base address |
| <i>channel</i> | Timer channel number        |

Returns

The status flags. This is the logical OR of members of the enumeration [pit\\_status\\_flags\\_t](#)

### 27.6.9 `static void PIT_ClearStatusFlags ( PIT_Type * base, pit_chnl_t channel, uint32_t mask ) [inline], [static]`

Parameters

|                |                             |
|----------------|-----------------------------|
| <i>base</i>    | PIT peripheral base address |
| <i>channel</i> | Timer channel number        |

## Function Documentation

|             |                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------|
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">pit_status_flags_t</a> |
|-------------|------------------------------------------------------------------------------------------------------------------|

### 27.6.10 static void PIT\_SetTimerPeriod ( PIT\_Type \* *base*, pit\_chnl\_t *channel*, uint32\_t *count* ) [inline], [static]

Timers begin counting from the value set by this function until it reaches 0, then it generates an interrupt and load this register value again. Writing a new value to this register does not restart the timer. Instead, the value is loaded after the timer expires.

#### Note

Users can call the utility macros provided in `fsl_common.h` to convert to ticks.

#### Parameters

|                |                                |
|----------------|--------------------------------|
| <i>base</i>    | PIT peripheral base address    |
| <i>channel</i> | Timer channel number           |
| <i>count</i>   | Timer period in units of ticks |

### 27.6.11 static uint32\_t PIT\_GetCurrentTimerCount ( PIT\_Type \* *base*, pit\_chnl\_t *channel* ) [inline], [static]

This function returns the real-time timer counting value, in a range from 0 to a timer period.

#### Note

Users can call the utility macros provided in `fsl_common.h` to convert ticks to usec or msec.

#### Parameters

|                |                             |
|----------------|-----------------------------|
| <i>base</i>    | PIT peripheral base address |
| <i>channel</i> | Timer channel number        |

#### Returns

Current timer counting value in ticks

**27.6.12** `static void PIT_StartTimer ( PIT_Type * base, pit_chnl_t channel )`  
`[inline], [static]`

After calling this function, timers load period value, count down to 0 and then load the respective start value again. Each time a timer reaches 0, it generates a trigger pulse and sets the timeout interrupt flag.

## Function Documentation

### Parameters

|                |                             |
|----------------|-----------------------------|
| <i>base</i>    | PIT peripheral base address |
| <i>channel</i> | Timer channel number.       |

### 27.6.13 static void PIT\_StopTimer ( PIT\_Type \* *base*, pit\_chnl\_t *channel* ) [inline], [static]

This function stops every timer counting. Timers reload their periods respectively after the next time they call the PIT\_DRV\_StartTimer.

### Parameters

|                |                             |
|----------------|-----------------------------|
| <i>base</i>    | PIT peripheral base address |
| <i>channel</i> | Timer channel number.       |

### 27.6.14 uint64\_t PIT\_GetLifetimeTimerCount ( PIT\_Type \* *base* )

The lifetime timer is a 64-bit timer which chains timer 0 and timer 1 together. Timer 0 and 1 are chained by calling the PIT\_SetTimerChainMode before using this timer. The period of lifetime timer is equal to the "period of timer 0 \* period of timer 1". For the 64-bit value, the higher 32-bit has the value of timer 1, and the lower 32-bit has the value of timer 0.

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PIT peripheral base address |
|-------------|-----------------------------|

### Returns

Current lifetime timer value

## Chapter 28

# PMC: Power Management Controller

### 28.1 Overview

The KSDK provides a Peripheral driver for the Power Management Controller (PMC) module of Kinetis devices. The PMC module contains internal voltage regulator, power on reset, low-voltage detect system, and high-voltage detect system.

### Data Structures

- struct [pmc\\_low\\_volt\\_detect\\_config\\_t](#)  
*Low-voltage Detect Configuration Structure. [More...](#)*
- struct [pmc\\_low\\_volt\\_warning\\_config\\_t](#)  
*Low-voltage Warning Configuration Structure. [More...](#)*
- struct [pmc\\_bandgap\\_buffer\\_config\\_t](#)  
*Bandgap Buffer configuration. [More...](#)*

### Enumerations

- enum [pmc\\_low\\_volt\\_detect\\_volt\\_select\\_t](#) {  
    [kPMC\\_LowVoltDetectLowTrip](#) = 0U,  
    [kPMC\\_LowVoltDetectHighTrip](#) = 1U }  
*Low-voltage Detect Voltage Select.*
- enum [pmc\\_low\\_volt\\_warning\\_volt\\_select\\_t](#) {  
    [kPMC\\_LowVoltWarningLowTrip](#) = 0U,  
    [kPMC\\_LowVoltWarningMid1Trip](#) = 1U,  
    [kPMC\\_LowVoltWarningMid2Trip](#) = 2U,  
    [kPMC\\_LowVoltWarningHighTrip](#) = 3U }  
*Low-voltage Warning Voltage Select.*

### Driver version

- #define [FSL\\_PMC\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 0, 0))  
*PMC driver version.*

### Power Management Controller Control APIs

- void [PMC\\_ConfigureLowVoltDetect](#) (PMC\_Type \*base, const [pmc\\_low\\_volt\\_detect\\_config\\_t](#) \*config)  
*Configures the low-voltage detect setting.*
- static bool [PMC\\_GetLowVoltDetectFlag](#) (PMC\_Type \*base)  
*Gets the Low-voltage Detect Flag status.*
- static void [PMC\\_ClearLowVoltDetectFlag](#) (PMC\_Type \*base)  
*Acknowledges clearing the Low-voltage Detect flag.*

## Data Structure Documentation

- void [PMC\\_ConfigureLowVoltWarning](#) (PMC\_Type \*base, const [pmc\\_low\\_volt\\_warning\\_config\\_t](#) \*config)  
*Configures the low-voltage warning setting.*
- static bool [PMC\\_GetLowVoltWarningFlag](#) (PMC\_Type \*base)  
*Gets the Low-voltage Warning Flag status.*
- static void [PMC\\_ClearLowVoltWarningFlag](#) (PMC\_Type \*base)  
*Acknowledges the Low-voltage Warning flag.*
- void [PMC\\_ConfigureBandgapBuffer](#) (PMC\_Type \*base, const [pmc\\_bandgap\\_buffer\\_config\\_t](#) \*config)  
*Configures the PMC bandgap.*
- static bool [PMC\\_GetPeriphIOIsolationFlag](#) (PMC\_Type \*base)  
*Gets the acknowledge Peripherals and I/O pads isolation flag.*
- static void [PMC\\_ClearPeriphIOIsolationFlag](#) (PMC\_Type \*base)  
*Acknowledges the isolation flag to Peripherals and I/O pads.*
- static bool [PMC\\_IsRegulatorInRunRegulation](#) (PMC\_Type \*base)  
*Gets the regulator regulation status.*

## 28.2 Data Structure Documentation

### 28.2.1 struct pmc\_low\_volt\_detect\_config\_t

#### Data Fields

- bool [enableInt](#)  
*Enable interrupt when Low-voltage detect.*
- bool [enableReset](#)  
*Enable system reset when Low-voltage detect.*
- [pmc\\_low\\_volt\\_detect\\_volt\\_select\\_t](#) [voltSelect](#)  
*Low-voltage detect trip point voltage selection.*

### 28.2.2 struct pmc\_low\_volt\_warning\_config\_t

#### Data Fields

- bool [enableInt](#)  
*Enable interrupt when low-voltage warning.*
- [pmc\\_low\\_volt\\_warning\\_volt\\_select\\_t](#) [voltSelect](#)  
*Low-voltage warning trip point voltage selection.*

### 28.2.3 struct pmc\_bandgap\_buffer\_config\_t

#### Data Fields

- bool [enable](#)  
*Enable bandgap buffer.*
- bool [enableInLowPowerMode](#)

*Enable bandgap buffer in low-power mode.*

### 28.2.3.0.0.78 Field Documentation

**28.2.3.0.0.78.1** `bool pmc_bandgap_buffer_config_t::enable`

**28.2.3.0.0.78.2** `bool pmc_bandgap_buffer_config_t::enableInLowPowerMode`

## 28.3 Macro Definition Documentation

**28.3.1** `#define FSL_PMC_DRIVER_VERSION (MAKE_VERSION(2, 0, 0))`

Version 2.0.0.

## 28.4 Enumeration Type Documentation

**28.4.1** `enum pmc_low_volt_detect_volt_select_t`

Enumerator

*kPMC\_LowVoltDetectLowTrip* Low-trip point selected (VLVD = VLVDL )  
*kPMC\_LowVoltDetectHighTrip* High-trip point selected (VLVD = VLVDH )

**28.4.2** `enum pmc_low_volt_warning_volt_select_t`

Enumerator

*kPMC\_LowVoltWarningLowTrip* Low-trip point selected (VLVW = VLVW1)  
*kPMC\_LowVoltWarningMid1Trip* Mid 1 trip point selected (VLVW = VLVW2)  
*kPMC\_LowVoltWarningMid2Trip* Mid 2 trip point selected (VLVW = VLVW3)  
*kPMC\_LowVoltWarningHighTrip* High-trip point selected (VLVW = VLVW4)

## 28.5 Function Documentation

**28.5.1** `void PMC_ConfigureLowVoltDetect ( PMC_Type * base, const pmc_low_volt_detect_config_t * config )`

This function configures the low-voltage detect setting, including the trip point voltage setting, enables or disables the interrupt, enables or disables the system reset.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | PMC peripheral base address.                |
| <i>config</i> | Low-voltage detect configuration structure. |

### 28.5.2 static bool PMC\_GetLowVoltDetectFlag ( PMC\_Type \* *base* ) [inline], [static]

This function reads the current LVDF status. If it returns 1, a low-voltage event is detected.



## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PMC peripheral base address. |
|-------------|------------------------------|

## Returns

Current low-voltage detect flag

- true: Low-voltage detected
- false: Low-voltage not detected

### 28.5.3 static void PMC\_ClearLowVoltDetectFlag ( PMC\_Type \* *base* ) [inline], [static]

This function acknowledges the low-voltage detection errors (write 1 to clear LVDF).

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PMC peripheral base address. |
|-------------|------------------------------|

### 28.5.4 void PMC\_ConfigureLowVoltWarning ( PMC\_Type \* *base*, const *pmc\_low\_volt\_warning\_config\_t* \* *config* )

This function configures the low-voltage warning setting, including the trip point voltage setting and enabling or disabling the interrupt.

## Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>base</i>   | PMC peripheral base address.                 |
| <i>config</i> | Low-voltage warning configuration structure. |

### 28.5.5 static bool PMC\_GetLowVoltWarningFlag ( PMC\_Type \* *base* ) [inline], [static]

This function polls the current LVWF status. When 1 is returned, it indicates a low-voltage warning event. LVWF is set when V Supply transitions below the trip point or after reset and V Supply is already below the V LVW.

## Function Documentation

### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PMC peripheral base address. |
|-------------|------------------------------|

### Returns

Current LVWF status

- true: Low-voltage Warning Flag is set.
- false: the Low-voltage Warning does not happen.

### 28.5.6 static void PMC\_ClearLowVoltWarningFlag ( PMC\_Type \* *base* ) [inline], [static]

This function acknowledges the low voltage warning errors (write 1 to clear LVWF).

### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PMC peripheral base address. |
|-------------|------------------------------|

### 28.5.7 void PMC\_ConfigureBandgapBuffer ( PMC\_Type \* *base*, const pmc\_bandgap\_buffer\_config\_t \* *config* )

This function configures the PMC bandgap, including the drive select and behavior in low-power mode.

### Parameters

|               |                                        |
|---------------|----------------------------------------|
| <i>base</i>   | PMC peripheral base address.           |
| <i>config</i> | Pointer to the configuration structure |

### 28.5.8 static bool PMC\_GetPeriphIOIsolationFlag ( PMC\_Type \* *base* ) [inline], [static]

This function reads the Acknowledge Isolation setting that indicates whether certain peripherals and the I/O pads are in a latched state as a result of having been in the VLLS mode.

## Parameters

|             |                                        |
|-------------|----------------------------------------|
| <i>base</i> | PMC peripheral base address.           |
| <i>base</i> | Base address for current PMC instance. |

## Returns

ACK isolation 0 - Peripherals and I/O pads are in a normal run state. 1 - Certain peripherals and I/O pads are in an isolated and latched state.

### 28.5.9 static void PMC\_ClearPeriphIOIsolationFlag ( PMC\_Type \* *base* ) [inline], [static]

This function clears the ACK Isolation flag. Writing one to this setting when it is set releases the I/O pads and certain peripherals to their normal run mode state.

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PMC peripheral base address. |
|-------------|------------------------------|

### 28.5.10 static bool PMC\_IsRegulatorInRunRegulation ( PMC\_Type \* *base* ) [inline], [static]

This function returns the regulator to run a regulation status. It provides the current status of the internal voltage regulator.

## Parameters

|             |                                        |
|-------------|----------------------------------------|
| <i>base</i> | PMC peripheral base address.           |
| <i>base</i> | Base address for current PMC instance. |

## Returns

Regulation status 0 - Regulator is in a stop regulation or in transition to/from the regulation. 1 - Regulator is in a run regulation.



## Chapter 29

# PORT: Port Control and Interrupts

### 29.1 Overview

The KSDK provides a driver for the Port Control and Interrupts (PORT) module of Kinetis devices.

### 29.2 Typical configuration use case

#### 29.2.1 Input PORT configuration

```
/* Input pin PORT configuration */
port_pin_config_t config = {
    kPORT_PullUp,
    kPORT_FastSlewRate,
    kPORT_PassiveFilterDisable,
    kPORT_OpenDrainDisable,
    kPORT_LowDriveStrength,
    kPORT_MuxAsGpio,
    kPORT_UnLockRegister,
};
/* Sets the configuration */
PORT_SetPinConfig(PORTA, 4, &config);
```

#### 29.2.2 I2C PORT Configuration

```
/* I2C pin PORT configuration */
port_pin_config_t config = {
    kPORT_PullUp,
    kPORT_FastSlewRate,
    kPORT_PassiveFilterDisable,
    kPORT_OpenDrainEnable,
    kPORT_LowDriveStrength,
    kPORT_MuxAlt5,
    kPORT_UnLockRegister,
};
PORT_SetPinConfig(PORTE, 24u, &config);
PORT_SetPinConfig(PORTE, 25u, &config);
```

### Data Structures

- struct [port\\_digital\\_filter\\_config\\_t](#)  
*PORT digital filter feature configuration definition. [More...](#)*
- struct [port\\_pin\\_config\\_t](#)  
*PORT pin configuration structure. [More...](#)*

### Enumerations

- enum [\\_port\\_pull](#) {  
    [kPORT\\_PullDisable](#) = 0U,  
    [kPORT\\_PullDown](#) = 2U,

## Typical configuration use case

`kPORT_PullUp = 3U }`

*Internal resistor pull feature selection.*

- enum `_port_slew_rate` {  
    `kPORT_FastSlewRate = 0U`,  
    `kPORT_SlowSlewRate = 1U` }

*Slew rate selection.*

- enum `_port_open_drain_enable` {  
    `kPORT_OpenDrainDisable = 0U`,  
    `kPORT_OpenDrainEnable = 1U` }

*Open Drain feature enable/disable.*

- enum `_port_passive_filter_enable` {  
    `kPORT_PassiveFilterDisable = 0U`,  
    `kPORT_PassiveFilterEnable = 1U` }

*Passive filter feature enable/disable.*

- enum `_port_drive_strength` {  
    `kPORT_LowDriveStrength = 0U`,  
    `kPORT_HighDriveStrength = 1U` }

*Configures the drive strength.*

- enum `_port_lock_register` {  
    `kPORT_UnlockRegister = 0U`,  
    `kPORT_LockRegister = 1U` }

*Unlock/lock the pin control register field[15:0].*

- enum `port_mux_t` {  
    `kPORT_PinDisabledOrAnalog = 0U`,  
    `kPORT_MuxAsGpio = 1U`,  
    `kPORT_MuxAlt2 = 2U`,  
    `kPORT_MuxAlt3 = 3U`,  
    `kPORT_MuxAlt4 = 4U`,  
    `kPORT_MuxAlt5 = 5U`,  
    `kPORT_MuxAlt6 = 6U`,  
    `kPORT_MuxAlt7 = 7U`,  
    `kPORT_MuxAlt8 = 8U`,  
    `kPORT_MuxAlt9 = 9U`,  
    `kPORT_MuxAlt10 = 10U`,  
    `kPORT_MuxAlt11 = 11U`,  
    `kPORT_MuxAlt12 = 12U`,  
    `kPORT_MuxAlt13 = 13U`,  
    `kPORT_MuxAlt14 = 14U`,  
    `kPORT_MuxAlt15 = 15U` }

*Pin mux selection.*

- enum `port_interrupt_t` {

```

kPORT_InterruptOrDMADisabled = 0x0U,
kPORT_DMARisingEdge = 0x1U,
kPORT_DMAFallingEdge = 0x2U,
kPORT_DMAEitherEdge = 0x3U,
kPORT_InterruptLogicZero = 0x8U,
kPORT_InterruptRisingEdge = 0x9U,
kPORT_InterruptFallingEdge = 0xAU,
kPORT_InterruptEitherEdge = 0xBU,
kPORT_InterruptLogicOne = 0xCU }
    Configures the interrupt generation condition.
• enum port_digital_filter_clock_source_t {
    kPORT_BusClock = 0U,
    kPORT_LpoClock = 1U }
    Digital filter clock source selection.

```

## Driver version

- #define FSL\_PORT\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 2))  
Version 2.0.2.

## Configuration

- static void PORT\_SetPinConfig (PORT\_Type \*base, uint32\_t pin, const port\_pin\_config\_t \*config)  
*Sets the port PCR register.*
- static void PORT\_SetMultiplePinsConfig (PORT\_Type \*base, uint32\_t mask, const port\_pin\_config\_t \*config)  
*Sets the port PCR register for multiple pins.*
- static void PORT\_SetPinMux (PORT\_Type \*base, uint32\_t pin, port\_mux\_t mux)  
*Configures the pin muxing.*
- static void PORT\_EnablePinsDigitalFilter (PORT\_Type \*base, uint32\_t mask, bool enable)  
*Enables the digital filter in one port, each bit of the 32-bit register represents one pin.*
- static void PORT\_SetDigitalFilterConfig (PORT\_Type \*base, const port\_digital\_filter\_config\_t \*config)  
*Sets the digital filter in one port, each bit of the 32-bit register represents one pin.*

## Interrupt

- static void PORT\_SetPinInterruptConfig (PORT\_Type \*base, uint32\_t pin, port\_interrupt\_t config)  
*Configures the port pin interrupt/DMA request.*
- static uint32\_t PORT\_GetPinsInterruptFlags (PORT\_Type \*base)  
*Reads the whole port status flag.*
- static void PORT\_ClearPinsInterruptFlags (PORT\_Type \*base, uint32\_t mask)  
*Clears the multiple pin interrupt status flag.*

## Enumeration Type Documentation

### 29.3 Data Structure Documentation

#### 29.3.1 struct port\_digital\_filter\_config\_t

##### Data Fields

- uint32\_t [digitalFilterWidth](#)  
*Set digital filter width.*
- [port\\_digital\\_filter\\_clock\\_source\\_t](#) clockSource  
*Set digital filter clockSource.*

#### 29.3.2 struct port\_pin\_config\_t

##### Data Fields

- uint16\_t [pullSelect](#): 2  
*No-pull/pull-down/pull-up select.*
- uint16\_t [slewRate](#): 1  
*Fast/slow slew rate Configure.*
- uint16\_t [passiveFilterEnable](#): 1  
*Passive filter enable/disable.*
- uint16\_t [openDrainEnable](#): 1  
*Open drain enable/disable.*
- uint16\_t [driveStrength](#): 1  
*Fast/slow drive strength configure.*
- uint16\_t [mux](#): 3  
*Pin mux Configure.*
- uint16\_t [lockRegister](#): 1  
*Lock/unlock the PCR field[15:0].*

### 29.4 Macro Definition Documentation

#### 29.4.1 #define FSL\_PORT\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 2))

### 29.5 Enumeration Type Documentation

#### 29.5.1 enum \_port\_pull

Enumerator

***kPORT\_PullDisable*** Internal pull-up/down resistor is disabled.  
***kPORT\_PullDown*** Internal pull-down resistor is enabled.  
***kPORT\_PullUp*** Internal pull-up resistor is enabled.



### 29.5.2 enum \_port\_slew\_rate

Enumerator

- kPORT\_FastSlewRate* Fast slew rate is configured.
- kPORT\_SlowSlewRate* Slow slew rate is configured.

### 29.5.3 enum \_port\_open\_drain\_enable

Enumerator

- kPORT\_OpenDrainDisable* Open drain output is disabled.
- kPORT\_OpenDrainEnable* Open drain output is enabled.

### 29.5.4 enum \_port\_passive\_filter\_enable

Enumerator

- kPORT\_PassiveFilterDisable* Passive input filter is disabled.
- kPORT\_PassiveFilterEnable* Passive input filter is enabled.

### 29.5.5 enum \_port\_drive\_strength

Enumerator

- kPORT\_LowDriveStrength* Low-drive strength is configured.
- kPORT\_HighDriveStrength* High-drive strength is configured.

### 29.5.6 enum \_port\_lock\_register

Enumerator

- kPORT\_UnlockRegister* Pin Control Register fields [15:0] are not locked.
- kPORT\_LockRegister* Pin Control Register fields [15:0] are locked.

### 29.5.7 enum port\_mux\_t

Enumerator

- kPORT\_PinDisabledOrAnalog* Corresponding pin is disabled, but is used as an analog pin.

## Function Documentation

*kPORT\_MuxAsGpio* Corresponding pin is configured as GPIO.  
*kPORT\_MuxAlt2* Chip-specific.  
*kPORT\_MuxAlt3* Chip-specific.  
*kPORT\_MuxAlt4* Chip-specific.  
*kPORT\_MuxAlt5* Chip-specific.  
*kPORT\_MuxAlt6* Chip-specific.  
*kPORT\_MuxAlt7* Chip-specific.  
*kPORT\_MuxAlt8* Chip-specific.  
*kPORT\_MuxAlt9* Chip-specific.  
*kPORT\_MuxAlt10* Chip-specific.  
*kPORT\_MuxAlt11* Chip-specific.  
*kPORT\_MuxAlt12* Chip-specific.  
*kPORT\_MuxAlt13* Chip-specific.  
*kPORT\_MuxAlt14* Chip-specific.  
*kPORT\_MuxAlt15* Chip-specific.

### 29.5.8 enum port\_interrupt\_t

Enumerator

*kPORT\_InterruptOrDMADisabled* Interrupt/DMA request is disabled.  
*kPORT\_DMARisingEdge* DMA request on rising edge.  
*kPORT\_DMAFallingEdge* DMA request on falling edge.  
*kPORT\_DMAEitherEdge* DMA request on either edge.  
*kPORT\_InterruptLogicZero* Interrupt when logic zero.  
*kPORT\_InterruptRisingEdge* Interrupt on rising edge.  
*kPORT\_InterruptFallingEdge* Interrupt on falling edge.  
*kPORT\_InterruptEitherEdge* Interrupt on either edge.  
*kPORT\_InterruptLogicOne* Interrupt when logic one.

### 29.5.9 enum port\_digital\_filter\_clock\_source\_t

Enumerator

*kPORT\_BusClock* Digital filters are clocked by the bus clock.  
*kPORT\_LpoClock* Digital filters are clocked by the 1 kHz LPO clock.

## 29.6 Function Documentation

**29.6.1 static void PORT\_SetPinConfig ( PORT\_Type \* *base*, uint32\_t *pin*, const port\_pin\_config\_t \* *config* ) [inline], [static]**

This is an example to define an input pin or output pin PCR configuration.

```

* // Define a digital input pin PCR configuration
* port_pin_config_t config = {
*     kPORT_PullUp,
*     kPORT_FastSlewRate,
*     kPORT_PassiveFilterDisable,
*     kPORT_OpenDrainDisable,
*     kPORT_LowDriveStrength,
*     kPORT_MuxAsGpio,
*     kPORT_UnLockRegister,
* };
*

```

## Parameters

|               |                                            |
|---------------|--------------------------------------------|
| <i>base</i>   | PORT peripheral base pointer.              |
| <i>pin</i>    | PORT pin number.                           |
| <i>config</i> | PORT PCR register configuration structure. |

### 29.6.2 static void PORT\_SetMultiplePinsConfig ( PORT\_Type \* *base*, uint32\_t *mask*, const port\_pin\_config\_t \* *config* ) [inline], [static]

This is an example to define input pins or output pins PCR configuration.

```

* // Define a digital input pin PCR configuration
* port_pin_config_t config = {
*     kPORT_PullUp ,
*     kPORT_PullEnable,
*     kPORT_FastSlewRate,
*     kPORT_PassiveFilterDisable,
*     kPORT_OpenDrainDisable,
*     kPORT_LowDriveStrength,
*     kPORT_MuxAsGpio,
*     kPORT_UnlockRegister,
* };
*

```

## Parameters

|               |                                            |
|---------------|--------------------------------------------|
| <i>base</i>   | PORT peripheral base pointer.              |
| <i>mask</i>   | PORT pin number macro.                     |
| <i>config</i> | PORT PCR register configuration structure. |

### 29.6.3 static void PORT\_SetPinMux ( PORT\_Type \* *base*, uint32\_t *pin*, port\_mux\_t *mux* ) [inline], [static]

## Function Documentation

### Parameters

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PORT peripheral base pointer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <i>pin</i>  | PORT pin number.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <i>mux</i>  | pin muxing slot selection. <ul style="list-style-type: none"><li>• <a href="#">kPORT_PinDisabledOrAnalog</a>: Pin disabled or work in analog function.</li><li>• <a href="#">kPORT_MuxAsGpio</a> : Set as GPIO.</li><li>• <a href="#">kPORT_MuxAlt2</a> : chip-specific.</li><li>• <a href="#">kPORT_MuxAlt3</a> : chip-specific.</li><li>• <a href="#">kPORT_MuxAlt4</a> : chip-specific.</li><li>• <a href="#">kPORT_MuxAlt5</a> : chip-specific.</li><li>• <a href="#">kPORT_MuxAlt6</a> : chip-specific.</li><li>• <a href="#">kPORT_MuxAlt7</a> : chip-specific. : This function is NOT recommended to use together with the <code>PORT_SetPinsConfig</code>, because the <code>PORT_SetPinsConfig</code> need to configure the pin mux anyway (Otherwise the pin mux is reset to zero : <code>kPORT_PinDisabledOrAnalog</code>). This function is recommended to use to reset the pin mux</li></ul> |

### 29.6.4 static void PORT\_EnablePinsDigitalFilter ( PORT\_Type \* *base*, uint32\_t *mask*, bool *enable* ) [inline], [static]

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | PORT peripheral base pointer. |
| <i>mask</i> | PORT pin number macro.        |

### 29.6.5 static void PORT\_SetDigitalFilterConfig ( PORT\_Type \* *base*, const port\_digital\_filter\_config\_t \* *config* ) [inline], [static]

### Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>base</i>   | PORT peripheral base pointer.                |
| <i>config</i> | PORT digital filter configuration structure. |

### 29.6.6 static void PORT\_SetPinInterruptConfig ( PORT\_Type \* *base*, uint32\_t *pin*, port\_interrupt\_t *config* ) [inline], [static]

## Parameters

|               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | PORT peripheral base pointer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <i>pin</i>    | PORT pin number.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <i>config</i> | PORT pin interrupt configuration. <ul style="list-style-type: none"> <li>• <a href="#">kPORT_InterruptOrDMADisabled</a>: Interrupt/DMA request disabled.</li> <li>• <a href="#">kPORT_DMARisingEdge</a>: DMA request on rising edge(if the DMA requests exit).</li> <li>• <a href="#">kPORT_DMAFallingEdge</a>: DMA request on falling edge(if the DMA requests exit).</li> <li>• <a href="#">kPORT_DMAEitherEdge</a>: DMA request on either edge(if the DMA requests exit).</li> <li>• <a href="#">#kPORT_FlagRisingEdge</a>: Flag sets on rising edge(if the Flag states exit).</li> <li>• <a href="#">#kPORT_FlagFallingEdge</a>: Flag sets on falling edge(if the Flag states exit).</li> <li>• <a href="#">#kPORT_FlagEitherEdge</a>: Flag sets on either edge(if the Flag states exit).</li> <li>• <a href="#">kPORT_InterruptLogicZero</a>: Interrupt when logic zero.</li> <li>• <a href="#">kPORT_InterruptRisingEdge</a>: Interrupt on rising edge.</li> <li>• <a href="#">kPORT_InterruptFallingEdge</a>: Interrupt on falling edge.</li> <li>• <a href="#">kPORT_InterruptEitherEdge</a>: Interrupt on either edge.</li> <li>• <a href="#">kPORT_InterruptLogicOne</a>: Interrupt when logic one.</li> <li>• <a href="#">#kPORT_ActiveHighTriggerOutputEnable</a>: Enable active high-trigger output (if the trigger states exit).</li> <li>• <a href="#">#kPORT_ActiveLowTriggerOutputEnable</a>: Enable active low-trigger output (if the trigger states exit).</li> </ul> |

### 29.6.7 static uint32\_t PORT\_GetPinsInterruptFlags ( PORT\_Type \* *base* ) [inline], [static]

If a pin is configured to generate the DMA request, the corresponding flag is cleared automatically at the completion of the requested DMA transfer. Otherwise, the flag remains set until a logic one is written to that flag. If configured for a level sensitive interrupt that remains asserted, the flag is set again immediately.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | PORT peripheral base pointer. |
|-------------|-------------------------------|

## Returns

Current port interrupt status flags, for example, 0x00010001 means the pin 0 and 16 have the interrupt.

**29.6.8** `static void PORT_ClearPinsInterruptFlags ( PORT_Type * base, uint32_t mask ) [inline], [static]`

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | PORT peripheral base pointer. |
| <i>mask</i> | PORT pin number macro.        |





## Chapter 30

# RCM: Reset Control Module Driver

### 30.1 Overview

The KSDK provides a Peripheral driver for the Reset Control Module (RCM) module of Kinetis devices.

### Data Structures

- struct [rcm\\_reset\\_pin\\_filter\\_config\\_t](#)  
*Reset pin filter configuration. [More...](#)*

### Enumerations

- enum [rcm\\_reset\\_source\\_t](#) {  
    [kRCM\\_SourceWakeup](#) = RCM\_SRS0\_WAKEUP\_MASK,  
    [kRCM\\_SourceLvd](#) = RCM\_SRS0\_LVD\_MASK,  
    [kRCM\\_SourceLoc](#) = RCM\_SRS0\_LOC\_MASK,  
    [kRCM\\_SourceLol](#) = RCM\_SRS0\_LOL\_MASK,  
    [kRCM\\_SourceWdog](#) = RCM\_SRS0\_WDOG\_MASK,  
    [kRCM\\_SourcePin](#) = RCM\_SRS0\_PIN\_MASK,  
    [kRCM\\_SourcePor](#) = RCM\_SRS0\_POR\_MASK,  
    [kRCM\\_SourceJtag](#) = RCM\_SRS1\_JTAG\_MASK << 8U,  
    [kRCM\\_SourceLockup](#) = RCM\_SRS1\_LOCKUP\_MASK << 8U,  
    [kRCM\\_SourceSw](#) = RCM\_SRS1\_SW\_MASK << 8U,  
    [kRCM\\_SourceMdma](#) = RCM\_SRS1\_MDM\_AP\_MASK << 8U,  
    [kRCM\\_SourceEzpt](#) = RCM\_SRS1\_EZPT\_MASK << 8U,  
    [kRCM\\_SourceSackerr](#) = RCM\_SRS1\_SACKERR\_MASK << 8U }  
    *System Reset Source Name definitions.*
- enum [rcm\\_run\\_wait\\_filter\\_mode\\_t](#) {  
    [kRCM\\_FilterDisable](#) = 0U,  
    [kRCM\\_FilterBusClock](#) = 1U,  
    [kRCM\\_FilterLpoClock](#) = 2U }  
    *Reset pin filter select in Run and Wait modes.*

### Driver version

- #define [FSL\\_RCM\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 0, 1))  
    *RCM driver version 2.0.1.*

### Reset Control Module APIs

- static uint32\_t [RCM\\_GetPreviousResetSources](#) (RCM\_Type \*base)  
    *Gets the reset source status which caused a previous reset.*

## Enumeration Type Documentation

- static uint32\_t [RCM\\_GetStickyResetSources](#) (RCM\_Type \*base)  
*Gets the sticky reset source status.*
- static void [RCM\\_ClearStickyResetSources](#) (RCM\_Type \*base, uint32\_t sourceMasks)  
*Clears the sticky reset source status.*
- void [RCM\\_ConfigureResetPinFilter](#) (RCM\_Type \*base, const [rcm\\_reset\\_pin\\_filter\\_config\\_t](#) \*config)  
*Configures the reset pin filter.*
- static bool [RCM\\_GetEasyPortModePinStatus](#) (RCM\_Type \*base)  
*Gets the EZP\_MS\_B pin assert status.*

## 30.2 Data Structure Documentation

### 30.2.1 struct rcm\_reset\_pin\_filter\_config\_t

#### Data Fields

- bool [enableFilterInStop](#)  
*Reset pin filter select in stop mode.*
- [rcm\\_run\\_wait\\_filter\\_mode\\_t](#) [filterInRunWait](#)  
*Reset pin filter in run/wait mode.*
- uint8\_t [busClockFilterCount](#)  
*Reset pin bus clock filter width.*

#### 30.2.1.0.0.79 Field Documentation

30.2.1.0.0.79.1 bool [rcm\\_reset\\_pin\\_filter\\_config\\_t::enableFilterInStop](#)

30.2.1.0.0.79.2 [rcm\\_run\\_wait\\_filter\\_mode\\_t](#) [rcm\\_reset\\_pin\\_filter\\_config\\_t::filterInRunWait](#)

30.2.1.0.0.79.3 uint8\_t [rcm\\_reset\\_pin\\_filter\\_config\\_t::busClockFilterCount](#)

## 30.3 Macro Definition Documentation

30.3.1 #define [FSL\\_RCM\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 0, 1))

## 30.4 Enumeration Type Documentation

### 30.4.1 enum rcm\_reset\_source\_t

#### Enumerator

*kRCM\_SourceWakeup* Low-leakage wakeup reset.  
*kRCM\_SourceLvd* Low-voltage detect reset.  
*kRCM\_SourceLoc* Loss of clock reset.  
*kRCM\_SourceLol* Loss of lock reset.  
*kRCM\_SourceWdog* Watchdog reset.  
*kRCM\_SourcePin* External pin reset.  
*kRCM\_SourcePor* Power on reset.  
*kRCM\_SourceJtag* JTAG generated reset.

*kRCM\_SourceLockup* Core lock up reset.  
*kRCM\_SourceSw* Software reset.  
*kRCM\_SourceMdmmap* MDM-AP system reset.  
*kRCM\_SourceEzpt* EzPort reset.  
*kRCM\_SourceSackerr* Parameter could get all reset flags.

### 30.4.2 enum rcm\_run\_wait\_filter\_mode\_t

Enumerator

*kRCM\_FilterDisable* All filtering disabled.  
*kRCM\_FilterBusClock* Bus clock filter enabled.  
*kRCM\_FilterLpoClock* LPO clock filter enabled.

## 30.5 Function Documentation

### 30.5.1 static uint32\_t RCM\_GetPreviousResetSources ( RCM\_Type \* *base* ) [inline], [static]

This function gets the current reset source status. Use source masks defined in the `rcm_reset_source_t` to get the desired source status.

This is an example.

```
uint32_t resetStatus;

// To get all reset source statuses.
resetStatus = RCM_GetPreviousResetSources(RCM) & kRCM_SourceAll;

// To test whether the MCU is reset using Watchdog.
resetStatus = RCM_GetPreviousResetSources(RCM) &
    kRCM_SourceWdog;

// To test multiple reset sources.
resetStatus = RCM_GetPreviousResetSources(RCM) & (
    kRCM_SourceWdog | kRCM_SourcePin);
```

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RCM peripheral base address. |
|-------------|------------------------------|

Returns

All reset source status bit map.

## Function Documentation

### 30.5.2 static uint32\_t RCM\_GetStickyResetSources ( RCM\_Type \* *base* ) [inline], [static]

This function gets the current reset source status that has not been cleared by software for a specific source.  
This is an example.

```
uint32_t resetStatus;  
  
// To get all reset source statuses.  
resetStatus = RCM_GetStickyResetSources(RCM) & kRCM_SourceAll;  
  
// To test whether the MCU is reset using Watchdog.  
resetStatus = RCM_GetStickyResetSources(RCM) &  
    kRCM_SourceWdog;  
  
// To test multiple reset sources.  
resetStatus = RCM_GetStickyResetSources(RCM) & (  
    kRCM_SourceWdog | kRCM_SourcePin);
```

#### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RCM peripheral base address. |
|-------------|------------------------------|

#### Returns

All reset source status bit map.

### 30.5.3 static void RCM\_ClearStickyResetSources ( RCM\_Type \* *base*, uint32\_t *sourceMasks* ) [inline], [static]

This function clears the sticky system reset flags indicated by source masks.  
This is an example.

```
// Clears multiple reset sources.  
RCM_ClearStickyResetSources(kRCM_SourceWdog |  
    kRCM_SourcePin);
```

#### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RCM peripheral base address. |
|-------------|------------------------------|

|                    |                             |
|--------------------|-----------------------------|
| <i>sourceMasks</i> | reset source status bit map |
|--------------------|-----------------------------|

#### 30.5.4 void RCM\_ConfigureResetPinFilter ( RCM\_Type \* *base*, const rcm\_reset\_pin\_filter\_config\_t \* *config* )

This function sets the reset pin filter including the filter source, filter width, and so on.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | RCM peripheral base address.            |
| <i>config</i> | Pointer to the configuration structure. |

#### 30.5.5 static bool RCM\_GetEasyPortModePinStatus ( RCM\_Type \* *base* ) [inline], [static]

This function gets the easy port mode status (EZP\_MS\_B) pin assert status.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RCM peripheral base address. |
|-------------|------------------------------|

Returns

status true - asserted, false - reasserted



## Chapter 31

# RNGA: Random Number Generator Accelerator Driver

### 31.1 Overview

The Kinetis SDK provides Peripheral driver for the Random Number Generator Accelerator (RNGA) block of Kinetis devices.

### 31.2 RNGA Initialization

1. To initialize the RNGA module, call the [RNGA\\_Init\(\)](#) function. This function automatically enables the RNGA module and its clock.
2. After calling the [RNGA\\_Init\(\)](#) function, the RNGA is enabled and the counter starts working.
3. To disable the RNGA module, call the [RNGA\\_Deinit\(\)](#) function.

### 31.3 Get random data from RNGA

1. [RNGA\\_GetRandomData\(\)](#) function gets random data from the RNGA module.

### 31.4 RNGA Set/Get Working Mode

The RNGA works either in sleep mode or normal mode

1. [RNGA\\_SetMode\(\)](#) function sets the RNGA mode.
2. [RNGA\\_GetMode\(\)](#) function gets the RNGA working mode.

### 31.5 Seed RNGA

1. [RNGA\\_Seed\(\)](#) function inputs an entropy value that the RNGA can use to seed the pseudo random algorithm.

This example code shows how to initialize and get random data from the RNGA driver:

```
{
    status_t      status;
    uint32_t      data;

    /* Initialize RNGA */
    status = RNGA_Init(RNG);

    /* Read Random data*/
    status = RNGA_GetRandomData(RNG, data, sizeof(data));

    if(status == kStatus_Success)
    {
        /* Print data*/
        PRINTF("Random = 0x%X\r\n", i, data );
        PRINTF("Succeed.\r\n");
    }
    else
    {

```

## Seed RNGA

```
        PRINTF("RNGA failed! (0x%x)\r\n", status);
    }

    /* Deinitialize RNGA */
    RNGA_Deinit(RNG);
}
```

### Note

It is important to note that there is no known cryptographic proof showing this is a secure method for generating random data. In fact, there may be an attack against this random number generator if its output is used directly in a cryptographic application. The attack is based on the linearity of the internal shift registers. Therefore, it is highly recommended that the random data produced by this module be used as an entropy source to provide an input seed to a NIST-approved pseudo-random-number generator based on DES or SHA-1 and defined in NIST FIPS PUB 186-2 Appendix 3 and NIST FIPS PUB SP 800-90. The requirement is needed to maximize the entropy of this input seed. To do this, when data is extracted from RNGA as quickly as the hardware allows, there are one to two bits of added entropy per 32-bit word. Any single bit of that word contains that entropy. Therefore, when used as an entropy source, a random number should be generated for each bit of entropy required and the least significant bit (any bit would be equivalent) of each word retained. The remainder of each random number should then be discarded. Used this way, even with full knowledge of the internal state of RNGA and all prior random numbers, an attacker is not able to predict the values of the extracted bits. Other sources of entropy can be used along with RNGA to generate the seed to the pseudorandom algorithm. The more random sources combined to create the seed, the better. The following is a list of sources that can be easily combined with the output of this module.

- Current time using highest precision possible
- Real-time system inputs that can be characterized as "random"
- Other entropy supplied directly by the user

## Enumerations

- enum `rnga_mode_t` {  
    `kRNGA_ModeNormal` = 0U,  
    `kRNGA_ModeSleep` = 1U }  
    *RNGA working mode.*

## Functions

- void `RNGA_Init` (RNG\_Type \*base)  
    *Initializes the RNGA.*
- void `RNGA_Deinit` (RNG\_Type \*base)  
    *Shuts down the RNGA.*
- status\_t `RNGA_GetRandomData` (RNG\_Type \*base, void \*data, size\_t data\_size)  
    *Gets random data.*
- void `RNGA_Seed` (RNG\_Type \*base, uint32\_t seed)  
    *Feeds the RNGA module.*
- void `RNGA_SetMode` (RNG\_Type \*base, `rnga_mode_t` mode)



- *Sets the RNGA in normal mode or sleep mode.*  
**rnga\_mode\_t RNGA\_GetMode** (RNG\_Type \*base)  
*Gets the RNGA working mode.*

## Driver version

- #define **FSL\_RNGA\_DRIVER\_VERSION** (MAKE\_VERSION(2, 0, 1))  
*RNGA driver version 2.0.1.*

## 31.6 Macro Definition Documentation

### 31.6.1 #define FSL\_RNGA\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

## 31.7 Enumeration Type Documentation

### 31.7.1 enum rnga\_mode\_t

Enumerator

**kRNGA\_ModeNormal** Normal Mode. The ring-oscillator clocks are active; RNGA generates entropy (randomness) from the clocks and stores it in shift registers.

**kRNGA\_ModeSleep** Sleep Mode. The ring-oscillator clocks are inactive; RNGA does not generate entropy.

## 31.8 Function Documentation

### 31.8.1 void RNGA\_Init ( RNG\_Type \* *base* )

This function initializes the RNGA. When called, the RNGA entropy generation starts immediately.

Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | RNGA base address |
|-------------|-------------------|

### 31.8.2 void RNGA\_Deinit ( RNG\_Type \* *base* )

This function shuts down the RNGA.

Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | RNGA base address |
|-------------|-------------------|

## Function Documentation

### 31.8.3 **status\_t** RNGA\_GetRandomData ( **RNG\_Type** \* *base*, **void** \* *data*, **size\_t** *data\_size* )

This function gets random data from the RNGA.

## Parameters

|                  |                                                    |
|------------------|----------------------------------------------------|
| <i>base</i>      | RNGA base address                                  |
| <i>data</i>      | pointer to user buffer to be filled by random data |
| <i>data_size</i> | size of data in bytes                              |

## Returns

RNGA status

### 31.8.4 void RNGA\_Seed ( RNG\_Type \* *base*, uint32\_t *seed* )

This function inputs an entropy value that the RNGA uses to seed its pseudo-random algorithm.

## Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | RNGA base address |
| <i>seed</i> | input seed value  |

### 31.8.5 void RNGA\_SetMode ( RNG\_Type \* *base*, rnga\_mode\_t *mode* )

This function sets the RNGA in sleep mode or normal mode.

## Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | RNGA base address         |
| <i>mode</i> | normal mode or sleep mode |

### 31.8.6 rnga\_mode\_t RNGA\_GetMode ( RNG\_Type \* *base* )

This function gets the RNGA working mode.

## Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | RNGA base address |
|-------------|-------------------|

## Returns

normal mode or sleep mode



## Chapter 32

### RTC: Real Time Clock

#### 32.1 Overview

The KSDK provides a driver for the Real Time Clock (RTC) of Kinetis devices.

#### 32.2 Function groups

The RTC driver supports operating the module as a time counter.

##### 32.2.1 Initialization and deinitialization

The function [RTC\\_Init\(\)](#) initializes the RTC with specified configurations. The function [RTC\\_GetDefaultConfig\(\)](#) gets the default configurations.

The function [RTC\\_Deinit\(\)](#) disables the RTC timer and disables the module clock.

##### 32.2.2 Set & Get Datetime

The function [RTC\\_SetDatetime\(\)](#) sets the timer period in seconds. Users pass in the details in date & time format by using the below data structure.

```
typedef struct _rtc_datetime
{
    uint16_t year;
    uint8_t month;
    uint8_t day;
    uint8_t hour;
    uint8_t minute;
    uint8_t second;
} rtc_datetime_t;
```

The function [RTC\\_GetDatetime\(\)](#) reads the current timer value in seconds, converts it to date & time format and stores it into a datetime structure passed in by the user.

##### 32.2.3 Set & Get Alarm

The function [RTC\\_SetAlarm\(\)](#) sets the alarm time period in seconds. Users pass in the details in date & time format by using the datetime data structure.

The function [RTC\\_GetAlarm\(\)](#) reads the alarm time in seconds, converts it to date & time format and stores it into a datetime structure passed in by the user.

## Typical use case

### 32.2.4 Start & Stop timer

The function [RTC\\_StartTimer\(\)](#) starts the RTC time counter.

The function [RTC\\_StopTimer\(\)](#) stops the RTC time counter.

### 32.2.5 Status

Provides functions to get and clear the RTC status.

### 32.2.6 Interrupt

Provides functions to enable/disable RTC interrupts and get current enabled interrupts.

### 32.2.7 RTC Oscillator

Some SoC's allow control of the RTC oscillator through the RTC module.

The function [RTC\\_SetOscCapLoad\(\)](#) allows the user to modify the capacitor load configuration of the RTC oscillator.

### 32.2.8 Monotonic Counter

Some SoC's have a 64-bit Monotonic counter available in the RTC module.

The function [RTC\\_SetMonotonicCounter\(\)](#) writes a 64-bit to the counter.

The function [RTC\\_GetMonotonicCounter\(\)](#) reads the monotonic counter and returns the 64-bit counter value to the user.

The function [RTC\\_IncrementMonotonicCounter\(\)](#) increments the Monotonic Counter by one.

## 32.3 Typical use case

### 32.3.1 RTC tick example

Example to set the RTC current time and trigger an alarm.

```
int main(void)
{
    uint32_t sec;
    uint32_t currSeconds;
    rtc_datetime_t date;
    rtc_config_t rtcConfig;

    /* Board pin, clock, debug console init */
```

```

BOARD_InitHardware();
/* Init RTC */
RTC_GetDefaultConfig(&rtcConfig);
RTC_Init(RTC, &rtcConfig);
/* Select RTC clock source */
BOARD_SetRtcClockSource();

PRINTF("RTC example: set up time to wake up an alarm\r\n");

/* Set a start date time and start RT */
date.year = 2014U;
date.month = 12U;
date.day = 25U;
date.hour = 19U;
date.minute = 0;
date.second = 0;

/* RTC time counter has to be stopped before setting the date & time in the TSR register */
RTC_StopTimer(RTC);

/* Set RTC time to default */
RTC_SetDatetime(RTC, &date);

/* Enable RTC alarm interrupt */
RTC_EnableInterrupts(RTC, kRTC_AlarmInterruptEnable);

/* Enable at the NVIC */
EnableIRQ(RTC_IRQn);

/* Start the RTC time counter */
RTC_StartTimer(RTC);

/* This loop will set the RTC alarm */
while (1)
{
    busyWait = true;
    /* Get date time */
    RTC_GetDatetime(RTC, &date);

    /* print default time */
    PRINTF("Current datetime: %04hd-%02hd-%02hd %02hd:%02hd:%02hd\r\n", date.
year, date.month, date.day, date.hour,
        date.minute, date.second);

    /* Get alarm time from the user */
    sec = 0;
    PRINTF("Input the number of second to wait for alarm \r\n");
    PRINTF("The second must be positive value\r\n");
    while (sec < 1)
    {
        SCANF("%d", &sec);
    }

    /* Read the RTC seconds register to get current time in seconds */
    currSeconds = RTC->TSR;

    /* Add alarm seconds to current time */
    currSeconds += sec;

    /* Set alarm time in seconds */
    RTC->TAR = currSeconds;

    /* Get alarm time */
    RTC_GetAlarm(RTC, &date);

    /* Print alarm time */
    PRINTF("Alarm will occur at: %04hd-%02hd-%02hd %02hd:%02hd:%02hd\r\n", date.
year, date.month, date.day,

```

## Typical use case

```
        date.hour, date.minute, date.second);

    /* Wait until alarm occurs */
    while (busyWait)
    {
    }

    PRINTF("\r\n Alarm occurs !!!! ");
}
}
```

## Data Structures

- struct `rtc_datetime_t`  
*Structure is used to hold the date and time. [More...](#)*
- struct `rtc_config_t`  
*RTC config structure. [More...](#)*

## Enumerations

- enum `rtc_interrupt_enable_t` {  
    `kRTC_TimeInvalidInterruptEnable` = RTC\_IER\_TIIE\_MASK,  
    `kRTC_TimeOverflowInterruptEnable` = RTC\_IER\_TOIE\_MASK,  
    `kRTC_AlarmInterruptEnable` = RTC\_IER\_TAIE\_MASK,  
    `kRTC_SecondsInterruptEnable` = RTC\_IER\_TSIE\_MASK }  
*List of RTC interrupts.*
- enum `rtc_status_flags_t` {  
    `kRTC_TimeInvalidFlag` = RTC\_SR\_TIF\_MASK,  
    `kRTC_TimeOverflowFlag` = RTC\_SR\_TOF\_MASK,  
    `kRTC_AlarmFlag` = RTC\_SR\_TAF\_MASK }  
*List of RTC flags.*
- enum `rtc_osc_cap_load_t` {  
    `kRTC_Capacitor_2p` = RTC\_CR\_SC2P\_MASK,  
    `kRTC_Capacitor_4p` = RTC\_CR\_SC4P\_MASK,  
    `kRTC_Capacitor_8p` = RTC\_CR\_SC8P\_MASK,  
    `kRTC_Capacitor_16p` = RTC\_CR\_SC16P\_MASK }  
*List of RTC Oscillator capacitor load settings.*

## Functions

- static void `RTC_SetOscCapLoad` (RTC\_Type \*base, uint32\_t capLoad)  
*This function sets the specified capacitor configuration for the RTC oscillator.*
- static void `RTC_Reset` (RTC\_Type \*base)  
*Performs a software reset on the RTC module.*

## Driver version

- #define `FSL_RTC_DRIVER_VERSION` (`MAKE_VERSION`(2, 0, 0))  
*Version 2.0.0.*



## Initialization and deinitialization

- void [RTC\\_Init](#) (RTC\_Type \*base, const [rtc\\_config\\_t](#) \*config)  
*Un gates the RTC clock and configures the peripheral for basic operation.*
- static void [RTC\\_Deinit](#) (RTC\_Type \*base)  
*Stops the timer and gate the RTC clock.*
- void [RTC\\_GetDefaultConfig](#) ([rtc\\_config\\_t](#) \*config)  
*Fills in the RTC config struct with the default settings.*

## Current Time & Alarm

- status\_t [RTC\\_SetDatetime](#) (RTC\_Type \*base, const [rtc\\_datetime\\_t](#) \*datetime)  
*Sets the RTC date and time according to the given time structure.*
- void [RTC\\_GetDatetime](#) (RTC\_Type \*base, [rtc\\_datetime\\_t](#) \*datetime)  
*Gets the RTC time and stores it in the given time structure.*
- status\_t [RTC\\_SetAlarm](#) (RTC\_Type \*base, const [rtc\\_datetime\\_t](#) \*alarmTime)  
*Sets the RTC alarm time.*
- void [RTC\\_GetAlarm](#) (RTC\_Type \*base, [rtc\\_datetime\\_t](#) \*datetime)  
*Returns the RTC alarm time.*

## Interrupt Interface

- static void [RTC\\_EnableInterrupts](#) (RTC\_Type \*base, uint32\_t mask)  
*Enables the selected RTC interrupts.*
- static void [RTC\\_DisableInterrupts](#) (RTC\_Type \*base, uint32\_t mask)  
*Disables the selected RTC interrupts.*
- static uint32\_t [RTC\\_GetEnabledInterrupts](#) (RTC\_Type \*base)  
*Gets the enabled RTC interrupts.*

## Status Interface

- static uint32\_t [RTC\\_GetStatusFlags](#) (RTC\_Type \*base)  
*Gets the RTC status flags.*
- void [RTC\\_ClearStatusFlags](#) (RTC\_Type \*base, uint32\_t mask)  
*Clears the RTC status flags.*

## Timer Start and Stop

- static void [RTC\\_StartTimer](#) (RTC\_Type \*base)  
*Starts the RTC time counter.*
- static void [RTC\\_StopTimer](#) (RTC\_Type \*base)  
*Stops the RTC time counter.*

## Monotonic counter functions

- void [RTC\\_GetMonotonicCounter](#) (RTC\_Type \*base, uint64\_t \*counter)  
*Reads the values of the Monotonic Counter High and Monotonic Counter Low and returns them as a single value.*
- void [RTC\\_SetMonotonicCounter](#) (RTC\_Type \*base, uint64\_t counter)  
*Writes values Monotonic Counter High and Monotonic Counter Low by decomposing the given single value.*

## Data Structure Documentation

- `status_t RTC_IncrementMonotonicCounter` (`RTC_Type *base`)  
*Increments the Monotonic Counter by one.*

## 32.4 Data Structure Documentation

### 32.4.1 struct rtc\_datetime\_t

#### Data Fields

- `uint16_t year`  
*Range from 1970 to 2099.*
- `uint8_t month`  
*Range from 1 to 12.*
- `uint8_t day`  
*Range from 1 to 31 (depending on month).*
- `uint8_t hour`  
*Range from 0 to 23.*
- `uint8_t minute`  
*Range from 0 to 59.*
- `uint8_t second`  
*Range from 0 to 59.*

#### 32.4.1.0.0.80 Field Documentation

32.4.1.0.0.80.1 `uint16_t rtc_datetime_t::year`

32.4.1.0.0.80.2 `uint8_t rtc_datetime_t::month`

32.4.1.0.0.80.3 `uint8_t rtc_datetime_t::day`

32.4.1.0.0.80.4 `uint8_t rtc_datetime_t::hour`

32.4.1.0.0.80.5 `uint8_t rtc_datetime_t::minute`

32.4.1.0.0.80.6 `uint8_t rtc_datetime_t::second`

### 32.4.2 struct rtc\_config\_t

This structure holds the configuration settings for the RTC peripheral. To initialize this structure to reasonable defaults, call the `RTC_GetDefaultConfig()` function and pass a pointer to your config structure instance.

The config struct can be made const so it resides in flash

#### Data Fields

- `bool wakeupSelect`  
*true: Wakeup pin outputs the 32 KHz clock; false: Wakeup pin used to wakeup the chip*

- bool `updateMode`  
*true: Registers can be written even when locked under certain conditions, false: No writes allowed when registers are locked*
- bool `supervisorAccess`  
*true: Non-supervisor accesses are allowed; false: Non-supervisor accesses are not supported*
- uint32\_t `compensationInterval`  
*Compensation interval that is written to the CIR field in RTC TCR Register.*
- uint32\_t `compensationTime`  
*Compensation time that is written to the TCR field in RTC TCR Register.*

## 32.5 Enumeration Type Documentation

### 32.5.1 enum rtc\_interrupt\_enable\_t

Enumerator

*kRTC\_TimeInvalidInterruptEnable* Time invalid interrupt.  
*kRTC\_TimeOverflowInterruptEnable* Time overflow interrupt.  
*kRTC\_AlarmInterruptEnable* Alarm interrupt.  
*kRTC\_SecondsInterruptEnable* Seconds interrupt.

### 32.5.2 enum rtc\_status\_flags\_t

Enumerator

*kRTC\_TimeInvalidFlag* Time invalid flag.  
*kRTC\_TimeOverflowFlag* Time overflow flag.  
*kRTC\_AlarmFlag* Alarm flag.

### 32.5.3 enum rtc\_osc\_cap\_load\_t

Enumerator

*kRTC\_Capacitor\_2p* 2 pF capacitor load  
*kRTC\_Capacitor\_4p* 4 pF capacitor load  
*kRTC\_Capacitor\_8p* 8 pF capacitor load  
*kRTC\_Capacitor\_16p* 16 pF capacitor load

## 32.6 Function Documentation

### 32.6.1 void RTC\_Init ( RTC\_Type \* *base*, const rtc\_config\_t \* *config* )

This function issues a software reset if the timer invalid flag is set.

## Function Documentation

### Note

This API should be called at the beginning of the application using the RTC driver.

### Parameters

|               |                                                    |
|---------------|----------------------------------------------------|
| <i>base</i>   | RTC peripheral base address                        |
| <i>config</i> | Pointer to the user's RTC configuration structure. |

### 32.6.2 static void RTC\_Deinit ( RTC\_Type \* *base* ) [inline], [static]

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | RTC peripheral base address |
|-------------|-----------------------------|

### 32.6.3 void RTC\_GetDefaultConfig ( rtc\_config\_t \* *config* )

The default values are as follows.

```
* config->wakeupSelect = false;
* config->updateMode = false;
* config->supervisorAccess = false;
* config->compensationInterval = 0;
* config->compensationTime = 0;
*
```

### Parameters

|               |                                                    |
|---------------|----------------------------------------------------|
| <i>config</i> | Pointer to the user's RTC configuration structure. |
|---------------|----------------------------------------------------|

### 32.6.4 status\_t RTC\_SetDatetime ( RTC\_Type \* *base*, const rtc\_datetime\_t \* *datetime* )

The RTC counter must be stopped prior to calling this function because writes to the RTC seconds register fail if the RTC counter is running.

## Parameters

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <i>base</i>     | RTC peripheral base address                                          |
| <i>datetime</i> | Pointer to the structure where the date and time details are stored. |

## Returns

kStatus\_Success: Success in setting the time and starting the RTC  
 kStatus\_InvalidArgument: Error because the datetime format is incorrect

### 32.6.5 void RTC\_GetDatetime ( RTC\_Type \* *base*, rtc\_datetime\_t \* *datetime* )

## Parameters

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <i>base</i>     | RTC peripheral base address                                          |
| <i>datetime</i> | Pointer to the structure where the date and time details are stored. |

### 32.6.6 status\_t RTC\_SetAlarm ( RTC\_Type \* *base*, const rtc\_datetime\_t \* *alarmTime* )

The function checks whether the specified alarm time is greater than the present time. If not, the function does not set the alarm and returns an error.

## Parameters

|                  |                                                          |
|------------------|----------------------------------------------------------|
| <i>base</i>      | RTC peripheral base address                              |
| <i>alarmTime</i> | Pointer to the structure where the alarm time is stored. |

## Returns

kStatus\_Success: success in setting the RTC alarm  
 kStatus\_InvalidArgument: Error because the alarm datetime format is incorrect  
 kStatus\_Fail: Error because the alarm time has already passed

### 32.6.7 void RTC\_GetAlarm ( RTC\_Type \* *base*, rtc\_datetime\_t \* *datetime* )

## Function Documentation

### Parameters

|                 |                                                                            |
|-----------------|----------------------------------------------------------------------------|
| <i>base</i>     | RTC peripheral base address                                                |
| <i>datetime</i> | Pointer to the structure where the alarm date and time details are stored. |

### 32.6.8 static void RTC\_EnableInterrupts ( RTC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

### Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | RTC peripheral base address                                                                                         |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">rtc_interrupt_enable_t</a> |

### 32.6.9 static void RTC\_DisableInterrupts ( RTC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

### Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | RTC peripheral base address                                                                                         |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">rtc_interrupt_enable_t</a> |

### 32.6.10 static uint32\_t RTC\_GetEnabledInterrupts ( RTC\_Type \* *base* ) [inline], [static]

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | RTC peripheral base address |
|-------------|-----------------------------|

### Returns

The enabled interrupts. This is the logical OR of members of the enumeration [rtc\\_interrupt\\_enable\\_t](#)

### 32.6.11 static uint32\_t RTC\_GetStatusFlags ( RTC\_Type \* *base* ) [inline], [static]

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | RTC peripheral base address |
|-------------|-----------------------------|

## Returns

The status flags. This is the logical OR of members of the enumeration [rtc\\_status\\_flags\\_t](#)

### 32.6.12 void RTC\_ClearStatusFlags ( RTC\_Type \* *base*, uint32\_t *mask* )

## Parameters

|             |                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | RTC peripheral base address                                                                                      |
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">rtc_status_flags_t</a> |

### 32.6.13 static void RTC\_StartTimer ( RTC\_Type \* *base* ) [inline], [static]

After calling this function, the timer counter increments once a second provided SR[TOF] or SR[TIF] are not set.

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | RTC peripheral base address |
|-------------|-----------------------------|

### 32.6.14 static void RTC\_StopTimer ( RTC\_Type \* *base* ) [inline], [static]

RTC's seconds register can be written to only when the timer is stopped.

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | RTC peripheral base address |
|-------------|-----------------------------|

### 32.6.15 static void RTC\_SetOscCapLoad ( RTC\_Type \* *base*, uint32\_t *capLoad* ) [inline], [static]

## Function Documentation

### Parameters

|                |                                                                                                                   |
|----------------|-------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | RTC peripheral base address                                                                                       |
| <i>capLoad</i> | Oscillator loads to enable. This is a logical OR of members of the enumeration <a href="#">rtc_osc_cap_load_t</a> |

### 32.6.16 static void RTC\_Reset ( RTC\_Type \* *base* ) [inline], [static]

This resets all RTC registers except for the SWR bit and the RTC\_WAR and RTC\_RAR registers. The SWR bit is cleared by software explicitly clearing it.

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | RTC peripheral base address |
|-------------|-----------------------------|

### 32.6.17 void RTC\_GetMonotonicCounter ( RTC\_Type \* *base*, uint64\_t \* *counter* )

### Parameters

|                |                                                |
|----------------|------------------------------------------------|
| <i>base</i>    | RTC peripheral base address                    |
| <i>counter</i> | Pointer to variable where the value is stored. |

### 32.6.18 void RTC\_SetMonotonicCounter ( RTC\_Type \* *base*, uint64\_t *counter* )

### Parameters

|                |                             |
|----------------|-----------------------------|
| <i>base</i>    | RTC peripheral base address |
| <i>counter</i> | Counter value               |

### 32.6.19 status\_t RTC\_IncrementMonotonicCounter ( RTC\_Type \* *base* )

Increments the Monotonic Counter (registers RTC\_MCLR and RTC\_MCHR accordingly) by setting the monotonic counter enable (MER[MCE]) and then writing to the RTC\_MCLR register. A write to the monotonic counter low that causes it to overflow also increments the monotonic counter high.



## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | RTC peripheral base address |
|-------------|-----------------------------|

## Returns

kStatus\_Success: success kStatus\_Fail: error occurred, either time invalid or monotonic overflow flag was found



## Chapter 33

# SAI: Serial Audio Interface

### 33.1 Overview

The KSDK provides a peripheral driver for the Serial Audio Interface (SAI) module of Kinetis devices.

SAI driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for SAI initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the SAI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. SAI functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `sai_handle_t` as the first parameter. Initialize the handle by calling the [SAI\\_TransferTxCreateHandle\(\)](#) or [SAI\\_TransferRxCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [SAI\\_TransferSendNonBlocking\(\)](#) and [SAI\\_TransferReceiveNonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_SAI_TxIdle` and `kStatus_SAI_RxIdle` status.

### 33.2 Typical use case

#### 33.2.1 SAI Send/receive using an interrupt method

```
sai_handle_t g_saiTxHandle;
sai_config_t user_config;
sai_transfer_t sendXfer;
volatile bool txFinished;
volatile bool rxFinished;
const uint8_t sendData[] = [.....];

void SAI_UserCallback(sai_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_SAI_TxIdle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    //...

    SAI_TxGetDefaultConfig(&user_config);
```

## Typical use case

```
SAI_TxInit(SAI0, &user_config);
SAI_TransferTxCreateHandle(SAI0, &g_saiHandle, SAI_UserCallback, NULL);

//Configure sai format
SAI_TransferTxSetTransferFormat(SAI0, &g_saiHandle, mclkSource, mclk);

// Prepare to send.
sendXfer.data = sendData
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Send out.
SAI_TransferSendNonBlocking(SAI0, &g_saiHandle, &sendXfer);

// Wait send finished.
while (!txFinished)
{
}

// ...
}
```

### 33.2.2 SAI Send/receive using a DMA method

```
sai_handle_t g_saiHandle;
dma_handle_t g_saiTxDmaHandle;
dma_handle_t g_saiRxDmaHandle;
sai_config_t user_config;
sai_transfer_t sendXfer;
volatile bool txFinished;
uint8_t sendData[] = ...;

void SAI_UserCallback(sai_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_SAI_TxIdle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    //...

    SAI_TxGetDefaultConfig(&user_config);
    SAI_TxInit(SAI0, &user_config);

    // Sets up the DMA.
    DMAMUX_Init(DMAMUX0);
    DMAMUX_SetSource(DMAMUX0, SAI_TX_DMA_CHANNEL, SAI_TX_DMA_REQUEST);
    DMAMUX_EnableChannel(DMAMUX0, SAI_TX_DMA_CHANNEL);

    DMA_Init(DMA0);

    /* Creates the DMA handle. */
    DMA_CreateHandle(&g_saiTxDmaHandle, DMA0, SAI_TX_DMA_CHANNEL);

    SAI_TransferTxCreateHandleDMA(SAI0, &g_saiTxDmaHandle, SAI_UserCallback,
        NULL);

    // Prepares to send.
    sendXfer.data = sendData
```

```

sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
SAI_TransferSendDMA(&g_saiHandle, &sendXfer);

// Waits for send to complete.
while (!txFinished)
{
}

// ...
}

```

## Modules

- [SAI DMA Driver](#)
- [SAI eDMA Driver](#)

## Data Structures

- struct [sai\\_config\\_t](#)  
*SAI user configuration structure. [More...](#)*
- struct [sai\\_transfer\\_format\\_t](#)  
*sai transfer format [More...](#)*
- struct [sai\\_transfer\\_t](#)  
*SAI transfer structure. [More...](#)*
- struct [sai\\_handle\\_t](#)  
*SAI handle structure. [More...](#)*

## Macros

- #define [SAI\\_XFER\\_QUEUE\\_SIZE](#) (4)  
*SAI transfer queue size, user can refine it according to use case.*

## Typedefs

- typedef void(\* [sai\\_transfer\\_callback\\_t](#))(I2S\_Type \*base, sai\_handle\_t \*handle, status\_t status, void \*userData)  
*SAI transfer callback prototype.*

## Enumerations

- enum [\\_sai\\_status\\_t](#) {  
[kStatus\\_SAI\\_TxBusy](#) = MAKE\_STATUS(kStatusGroup\_SAI, 0),  
[kStatus\\_SAI\\_RxBusy](#) = MAKE\_STATUS(kStatusGroup\_SAI, 1),  
[kStatus\\_SAI\\_TxError](#) = MAKE\_STATUS(kStatusGroup\_SAI, 2),  
[kStatus\\_SAI\\_RxError](#) = MAKE\_STATUS(kStatusGroup\_SAI, 3),  
[kStatus\\_SAI\\_QueueFull](#) = MAKE\_STATUS(kStatusGroup\_SAI, 4),  
[kStatus\\_SAI\\_TxIdle](#) = MAKE\_STATUS(kStatusGroup\_SAI, 5),  
[kStatus\\_SAI\\_RxIdle](#) = MAKE\_STATUS(kStatusGroup\_SAI, 6) }  
*SAI return status.*

## Typical use case

- enum `sai_protocol_t` {  
    `kSAI_BusLeftJustified` = 0x0U,  
    `kSAI_BusRightJustified`,  
    `kSAI_BusI2S`,  
    `kSAI_BusPCMA`,  
    `kSAI_BusPCMB` }  
    *Define the SAI bus type.*
- enum `sai_master_slave_t` {  
    `kSAI_Master` = 0x0U,  
    `kSAI_Slave` = 0x1U }  
    *Master or slave mode.*
- enum `sai_mono_stereo_t` {  
    `kSAI_Stereo` = 0x0U,  
    `kSAI_MonoLeft`,  
    `kSAI_MonoRight` }  
    *Mono or stereo audio format.*
- enum `sai_sync_mode_t` {  
    `kSAI_ModeAsync` = 0x0U,  
    `kSAI_ModeSync`,  
    `kSAI_ModeSyncWithOtherTx`,  
    `kSAI_ModeSyncWithOtherRx` }  
    *Synchronous or asynchronous mode.*
- enum `sai_mclk_source_t` {  
    `kSAI_MclkSourceSysclk` = 0x0U,  
    `kSAI_MclkSourceSelect1`,  
    `kSAI_MclkSourceSelect2`,  
    `kSAI_MclkSourceSelect3` }  
    *Master clock source.*
- enum `sai_bclk_source_t` {  
    `kSAI_BclkSourceBusclk` = 0x0U,  
    `kSAI_BclkSourceMclkDiv`,  
    `kSAI_BclkSourceOtherSai0`,  
    `kSAI_BclkSourceOtherSai1` }  
    *Bit clock source.*
- enum `_sai_interrupt_enable_t` {  
    `kSAI_WordStartInterruptEnable`,  
    `kSAI_SyncErrorInterruptEnable` = I2S\_TCSR\_SEIE\_MASK,  
    `kSAI_FIFOWarningInterruptEnable` = I2S\_TCSR\_FWIE\_MASK,  
    `kSAI_FIFOErrorInterruptEnable` = I2S\_TCSR\_FEIE\_MASK,  
    `kSAI_FIFORequestInterruptEnable` = I2S\_TCSR\_FRIE\_MASK }  
    *The SAI interrupt enable flag.*
- enum `_sai_dma_enable_t` {  
    `kSAI_FIFOWarningDMAEnable` = I2S\_TCSR\_FWDE\_MASK,  
    `kSAI_FIFORequestDMAEnable` = I2S\_TCSR\_FRDE\_MASK }  
    *The DMA request sources.*
- enum `_sai_flags` {

```

kSAI_WordStartFlag = I2S_TCSR_WSF_MASK,
kSAI_SyncErrorFlag = I2S_TCSR_SEF_MASK,
kSAI_FIFOErrorFlag = I2S_TCSR_FEF_MASK,
kSAI_FIFORequestFlag = I2S_TCSR_FRF_MASK,
kSAI_FIFOWarningFlag = I2S_TCSR_FWF_MASK }

```

*The SAI status flag.*

- enum `sai_reset_type_t` {  
`kSAI_ResetTypeSoftware` = I2S\_TCSR\_SR\_MASK,  
`kSAI_ResetTypeFIFO` = I2S\_TCSR\_FR\_MASK,  
`kSAI_ResetAll` = I2S\_TCSR\_SR\_MASK | I2S\_TCSR\_FR\_MASK }

*The reset type.*

- enum `sai_fifo_packing_t` {  
`kSAI_FifoPackingDisabled` = 0x0U,  
`kSAI_FifoPacking8bit` = 0x2U,  
`kSAI_FifoPacking16bit` = 0x3U }

*The SAI packing mode The mode includes 8 bit and 16 bit packing.*

- enum `sai_sample_rate_t` {  
`kSAI_SampleRate8KHz` = 8000U,  
`kSAI_SampleRate11025Hz` = 11025U,  
`kSAI_SampleRate12KHz` = 12000U,  
`kSAI_SampleRate16KHz` = 16000U,  
`kSAI_SampleRate22050Hz` = 22050U,  
`kSAI_SampleRate24KHz` = 24000U,  
`kSAI_SampleRate32KHz` = 32000U,  
`kSAI_SampleRate44100Hz` = 44100U,  
`kSAI_SampleRate48KHz` = 48000U,  
`kSAI_SampleRate96KHz` = 96000U }

*Audio sample rate.*

- enum `sai_word_width_t` {  
`kSAI_WordWidth8bits` = 8U,  
`kSAI_WordWidth16bits` = 16U,  
`kSAI_WordWidth24bits` = 24U,  
`kSAI_WordWidth32bits` = 32U }

*Audio word width.*

## Driver version

- #define `FSL_SAI_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 1)`)  
*Version 2.1.1.*

## Initialization and deinitialization

- void `SAI_TxInit` (I2S\_Type \*base, const `sai_config_t` \*config)  
*Initializes the SAI Tx peripheral.*
- void `SAI_RxInit` (I2S\_Type \*base, const `sai_config_t` \*config)  
*Initializes the the SAI Rx peripheral.*
- void `SAI_TxGetDefaultConfig` (`sai_config_t` \*config)

## Typical use case

- *Sets the SAI Tx configuration structure to default values.*  
void [SAI\\_RxGetDefaultConfig](#) ([sai\\_config\\_t](#) \*config)
- *Sets the SAI Rx configuration structure to default values.*  
void [SAI\\_Deinit](#) ([I2S\\_Type](#) \*base)
- *De-initializes the SAI peripheral.*  
void [SAI\\_TxReset](#) ([I2S\\_Type](#) \*base)
- *Resets the SAI Tx.*  
void [SAI\\_RxReset](#) ([I2S\\_Type](#) \*base)
- *Resets the SAI Rx.*  
void [SAI\\_TxEnable](#) ([I2S\\_Type](#) \*base, bool enable)
- *Enables/disables the SAI Tx.*  
void [SAI\\_RxEnable](#) ([I2S\\_Type](#) \*base, bool enable)
- *Enables/disables the SAI Rx.*

## Status

- static [uint32\\_t](#) [SAI\\_TxGetStatusFlag](#) ([I2S\\_Type](#) \*base)  
*Gets the SAI Tx status flag state.*
- static void [SAI\\_TxClearStatusFlags](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask)  
*Clears the SAI Tx status flag state.*
- static [uint32\\_t](#) [SAI\\_RxGetStatusFlag](#) ([I2S\\_Type](#) \*base)  
*Gets the SAI Rx status flag state.*
- static void [SAI\\_RxClearStatusFlags](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask)  
*Clears the SAI Rx status flag state.*

## Interrupts

- static void [SAI\\_TxEnableInterrupts](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask)  
*Enables the SAI Tx interrupt requests.*
- static void [SAI\\_RxEnableInterrupts](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask)  
*Enables the SAI Rx interrupt requests.*
- static void [SAI\\_TxDisableInterrupts](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask)  
*Disables the SAI Tx interrupt requests.*
- static void [SAI\\_RxDisableInterrupts](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask)  
*Disables the SAI Rx interrupt requests.*

## DMA Control

- static void [SAI\\_TxEnableDMA](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask, bool enable)  
*Enables/disables the SAI Tx DMA requests.*
- static void [SAI\\_RxEnableDMA](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) mask, bool enable)  
*Enables/disables the SAI Rx DMA requests.*
- static [uint32\\_t](#) [SAI\\_TxGetDataRegisterAddress](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) channel)  
*Gets the SAI Tx data register address.*
- static [uint32\\_t](#) [SAI\\_RxGetDataRegisterAddress](#) ([I2S\\_Type](#) \*base, [uint32\\_t](#) channel)  
*Gets the SAI Rx data register address.*

## Bus Operations

- void [SAI\\_TxSetFormat](#) ([I2S\\_Type](#) \*base, [sai\\_transfer\\_format\\_t](#) \*format, [uint32\\_t](#) mclkSourceClockHz, [uint32\\_t](#) bclkSourceClockHz)



- *Configures the SAI Tx audio format.*  
void [SAI\\_RxSetFormat](#) (I2S\_Type \*base, [sai\\_transfer\\_format\\_t](#) \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)
- *Configures the SAI Rx audio format.*  
void [SAI\\_WriteBlocking](#) (I2S\_Type \*base, uint32\_t channel, uint32\_t bitWidth, uint8\_t \*buffer, uint32\_t size)
- *Sends data using a blocking method.*  
static void [SAI\\_WriteData](#) (I2S\_Type \*base, uint32\_t channel, uint32\_t data)
- *Writes data into SAI FIFO.*  
void [SAI\\_ReadBlocking](#) (I2S\_Type \*base, uint32\_t channel, uint32\_t bitWidth, uint8\_t \*buffer, uint32\_t size)
- *Receives data using a blocking method.*  
static uint32\_t [SAI\\_ReadData](#) (I2S\_Type \*base, uint32\_t channel)
- *Reads data from the SAI FIFO.*

## Transactional

- void [SAI\\_TransferTxCreateHandle](#) (I2S\_Type \*base, sai\_handle\_t \*handle, [sai\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the SAI Tx handle.*
- void [SAI\\_TransferRxCreateHandle](#) (I2S\_Type \*base, sai\_handle\_t \*handle, [sai\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the SAI Rx handle.*
- status\_t [SAI\\_TransferTxSetFormat](#) (I2S\_Type \*base, sai\_handle\_t \*handle, [sai\\_transfer\\_format\\_t](#) \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Tx audio format.*
- status\_t [SAI\\_TransferRxSetFormat](#) (I2S\_Type \*base, sai\_handle\_t \*handle, [sai\\_transfer\\_format\\_t](#) \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Rx audio format.*
- status\_t [SAI\\_TransferSendNonBlocking](#) (I2S\_Type \*base, sai\_handle\_t \*handle, [sai\\_transfer\\_t](#) \*xfer)  
*Performs an interrupt non-blocking send transfer on SAI.*
- status\_t [SAI\\_TransferReceiveNonBlocking](#) (I2S\_Type \*base, sai\_handle\_t \*handle, [sai\\_transfer\\_t](#) \*xfer)  
*Performs an interrupt non-blocking receive transfer on SAI.*
- status\_t [SAI\\_TransferGetSendCount](#) (I2S\_Type \*base, sai\_handle\_t \*handle, size\_t \*count)  
*Gets a set byte count.*
- status\_t [SAI\\_TransferGetReceiveCount](#) (I2S\_Type \*base, sai\_handle\_t \*handle, size\_t \*count)  
*Gets a received byte count.*
- void [SAI\\_TransferAbortSend](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Aborts the current send.*
- void [SAI\\_TransferAbortReceive](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Aborts the the current IRQ receive.*
- void [SAI\\_TransferTxHandleIRQ](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Tx interrupt handler.*
- void [SAI\\_TransferRxHandleIRQ](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Tx interrupt handler.*

### 33.3 Data Structure Documentation

#### 33.3.1 struct sai\_config\_t

##### Data Fields

- [sai\\_protocol\\_t protocol](#)  
*Audio bus protocol in SAI.*
- [sai\\_sync\\_mode\\_t syncMode](#)  
*SAI sync mode, control Tx/Rx clock sync.*
- bool [mclkOutputEnable](#)  
*Master clock output enable, true means master clock divider enabled.*
- [sai\\_mclk\\_source\\_t mclkSource](#)  
*Master Clock source.*
- [sai\\_bclk\\_source\\_t bclkSource](#)  
*Bit Clock source.*
- [sai\\_master\\_slave\\_t masterSlave](#)  
*Master or slave.*

#### 33.3.2 struct sai\_transfer\_format\_t

##### Data Fields

- uint32\_t [sampleRate\\_Hz](#)  
*Sample rate of audio data.*
- uint32\_t [bitWidth](#)  
*Data length of audio data, usually 8/16/24/32 bits.*
- [sai\\_mono\\_stereo\\_t stereo](#)  
*Mono or stereo.*
- uint32\_t [masterClockHz](#)  
*Master clock frequency in Hz.*
- uint8\_t [watermark](#)  
*Watermark value.*
- uint8\_t [channel](#)  
*Data channel used in transfer.*
- [sai\\_protocol\\_t protocol](#)  
*Which audio protocol used.*

##### 33.3.2.0.0.81 Field Documentation

###### 33.3.2.0.0.81.1 uint8\_t sai\_transfer\_format\_t::channel

#### 33.3.3 struct sai\_transfer\_t

##### Data Fields

- uint8\_t \* [data](#)  
*Data start address to transfer.*

- `size_t dataSize`  
*Transfer size.*

### 33.3.3.0.0.82 Field Documentation

#### 33.3.3.0.0.82.1 `uint8_t* sai_transfer_t::data`

#### 33.3.3.0.0.82.2 `size_t sai_transfer_t::dataSize`

### 33.3.4 `struct _sai_handle`

#### Data Fields

- `uint32_t state`  
*Transfer status.*
- `sai_transfer_callback_t callback`  
*Callback function called at transfer event.*
- `void * userData`  
*Callback parameter passed to callback function.*
- `uint8_t bitWidth`  
*Bit width for transfer, 8/16/24/32 bits.*
- `uint8_t channel`  
*Transfer channel.*
- `sai_transfer_t saiQueue [SAI_XFER_QUEUE_SIZE]`  
*Transfer queue storing queued transfer.*
- `size_t transferSize [SAI_XFER_QUEUE_SIZE]`  
*Data bytes need to transfer.*
- `volatile uint8_t queueUser`  
*Index for user to queue transfer.*
- `volatile uint8_t queueDriver`  
*Index for driver to get the transfer data and size.*
- `uint8_t watermark`  
*Watermark value.*

### 33.4 Macro Definition Documentation

#### 33.4.1 `#define SAI_XFER_QUEUE_SIZE (4)`

### 33.5 Enumeration Type Documentation

#### 33.5.1 `enum _sai_status_t`

##### Enumerator

- `kStatus_SAI_TxBusy` SAI Tx is busy.
- `kStatus_SAI_RxBusy` SAI Rx is busy.
- `kStatus_SAI_TxError` SAI Tx FIFO error.
- `kStatus_SAI_RxError` SAI Rx FIFO error.
- `kStatus_SAI_QueueFull` SAI transfer queue is full.

## Enumeration Type Documentation

*kStatus\_SAI\_TxIdle* SAI Tx is idle.

*kStatus\_SAI\_RxIdle* SAI Rx is idle.

### 33.5.2 enum sai\_protocol\_t

Enumerator

*kSAI\_BusLeftJustified* Uses left justified format.

*kSAI\_BusRightJustified* Uses right justified format.

*kSAI\_BusI2S* Uses I2S format.

*kSAI\_BusPCMA* Uses I2S PCM A format.

*kSAI\_BusPCMB* Uses I2S PCM B format.

### 33.5.3 enum sai\_master\_slave\_t

Enumerator

*kSAI\_Master* Master mode.

*kSAI\_Slave* Slave mode.

### 33.5.4 enum sai\_mono\_stereo\_t

Enumerator

*kSAI\_Stereo* Stereo sound.

*kSAI\_MonoLeft* Only left channel have sound.

*kSAI\_MonoRight* Only Right channel have sound.

### 33.5.5 enum sai\_sync\_mode\_t

Enumerator

*kSAI\_ModeAsync* Asynchronous mode.

*kSAI\_ModeSync* Synchronous mode (with receiver or transmit)

*kSAI\_ModeSyncWithOtherTx* Synchronous with another SAI transmit.

*kSAI\_ModeSyncWithOtherRx* Synchronous with another SAI receiver.

### 33.5.6 enum sai\_mclk\_source\_t

Enumerator

*kSAI\_MclkSourceSysclk* Master clock from the system clock.  
*kSAI\_MclkSourceSelect1* Master clock from source 1.  
*kSAI\_MclkSourceSelect2* Master clock from source 2.  
*kSAI\_MclkSourceSelect3* Master clock from source 3.

### 33.5.7 enum sai\_bclk\_source\_t

Enumerator

*kSAI\_BclkSourceBusclk* Bit clock using bus clock.  
*kSAI\_BclkSourceMclkDiv* Bit clock using master clock divider.  
*kSAI\_BclkSourceOtherSai0* Bit clock from other SAI device.  
*kSAI\_BclkSourceOtherSai1* Bit clock from other SAI device.

### 33.5.8 enum \_sai\_interrupt\_enable\_t

Enumerator

*kSAI\_WordStartInterruptEnable* Word start flag, means the first word in a frame detected.  
*kSAI\_SyncErrorInterruptEnable* Sync error flag, means the sync error is detected.  
*kSAI\_FIFOWarningInterruptEnable* FIFO warning flag, means the FIFO is empty.  
*kSAI\_FIFOErrorInterruptEnable* FIFO error flag.  
*kSAI\_FIFORequestInterruptEnable* FIFO request, means reached watermark.

### 33.5.9 enum \_sai\_dma\_enable\_t

Enumerator

*kSAI\_FIFOWarningDMAEnable* FIFO warning caused by the DMA request.  
*kSAI\_FIFORequestDMAEnable* FIFO request caused by the DMA request.

### 33.5.10 enum \_sai\_flags

Enumerator

*kSAI\_WordStartFlag* Word start flag, means the first word in a frame detected.  
*kSAI\_SyncErrorFlag* Sync error flag, means the sync error is detected.

## Enumeration Type Documentation

*kSAI\_FIFOErrorFlag* FIFO error flag.  
*kSAI\_FIFORequestFlag* FIFO request flag.  
*kSAI\_FIFOWarningFlag* FIFO warning flag.

### 33.5.11 enum sai\_reset\_type\_t

Enumerator

*kSAI\_ResetTypeSoftware* Software reset, reset the logic state.  
*kSAI\_ResetTypeFIFO* FIFO reset, reset the FIFO read and write pointer.  
*kSAI\_ResetAll* All reset.

### 33.5.12 enum sai\_fifo\_packing\_t

Enumerator

*kSAI\_FifoPackingDisabled* Packing disabled.  
*kSAI\_FifoPacking8bit* 8 bit packing enabled  
*kSAI\_FifoPacking16bit* 16bit packing enabled

### 33.5.13 enum sai\_sample\_rate\_t

Enumerator

*kSAI\_SampleRate8KHz* Sample rate 8000 Hz.  
*kSAI\_SampleRate11025Hz* Sample rate 11025 Hz.  
*kSAI\_SampleRate12KHz* Sample rate 12000 Hz.  
*kSAI\_SampleRate16KHz* Sample rate 16000 Hz.  
*kSAI\_SampleRate22050Hz* Sample rate 22050 Hz.  
*kSAI\_SampleRate24KHz* Sample rate 24000 Hz.  
*kSAI\_SampleRate32KHz* Sample rate 32000 Hz.  
*kSAI\_SampleRate44100Hz* Sample rate 44100 Hz.  
*kSAI\_SampleRate48KHz* Sample rate 48000 Hz.  
*kSAI\_SampleRate96KHz* Sample rate 96000 Hz.

### 33.5.14 enum sai\_word\_width\_t

Enumerator

*kSAI\_WordWidth8bits* Audio data width 8 bits.

*kSAI\_WordWidth16bits* Audio data width 16 bits.  
*kSAI\_WordWidth24bits* Audio data width 24 bits.  
*kSAI\_WordWidth32bits* Audio data width 32 bits.

## 33.6 Function Documentation

### 33.6.1 void SAI\_TxInit ( I2S\_Type \* *base*, const sai\_config\_t \* *config* )

Ungates the SAI clock, resets the module, and configures SAI Tx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI\\_TxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAIM module can cause a hard fault because the clock is not enabled.

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | SAI base pointer             |
| <i>config</i> | SAI configuration structure. |

### 33.6.2 void SAI\_RxInit ( I2S\_Type \* *base*, const sai\_config\_t \* *config* )

Ungates the SAI clock, resets the module, and configures the SAI Rx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI\\_RxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAI module can cause a hard fault because the clock is not enabled.

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | SAI base pointer             |
| <i>config</i> | SAI configuration structure. |

### 33.6.3 void SAI\_TxGetDefaultConfig ( sai\_config\_t \* *config* )

This API initializes the configuration structure for use in SAI\_TxConfig(). The initialized structure can remain unchanged in SAI\_TxConfig(), or it can be modified before calling SAI\_TxConfig(). This is an example.

```
sai_config_t config;
SAI_TxGetDefaultConfig(&config);
```

## Function Documentation

### Parameters

|               |                                           |
|---------------|-------------------------------------------|
| <i>config</i> | pointer to master configuration structure |
|---------------|-------------------------------------------|

### 33.6.4 void SAI\_RxGetDefaultConfig ( sai\_config\_t \* *config* )

This API initializes the configuration structure for use in SAI\_RxConfig(). The initialized structure can remain unchanged in SAI\_RxConfig() or it can be modified before calling SAI\_RxConfig(). This is an example.

```
sai_config_t config;  
SAI_RxGetDefaultConfig(&config);
```

### Parameters

|               |                                           |
|---------------|-------------------------------------------|
| <i>config</i> | pointer to master configuration structure |
|---------------|-------------------------------------------|

### 33.6.5 void SAI\_Deinit ( I2S\_Type \* *base* )

This API gates the SAI clock. The SAI module can't operate unless SAI\_TxInit or SAI\_RxInit is called to enable the clock.

### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | SAI base pointer |
|-------------|------------------|

### 33.6.6 void SAI\_TxReset ( I2S\_Type \* *base* )

This function enables the software reset and FIFO reset of SAI Tx. After reset, clear the reset bit.

### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | SAI base pointer |
|-------------|------------------|

### 33.6.7 void SAI\_RxReset ( I2S\_Type \* *base* )

This function enables the software reset and FIFO reset of SAI Rx. After reset, clear the reset bit.



Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | SAI base pointer |
|-------------|------------------|

### 33.6.8 void SAI\_TxEnable ( I2S\_Type \* *base*, bool *enable* )

Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>base</i>   | SAI base pointer                               |
| <i>enable</i> | True means enable SAI Tx, false means disable. |

### 33.6.9 void SAI\_RxEnable ( I2S\_Type \* *base*, bool *enable* )

Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>base</i>   | SAI base pointer                               |
| <i>enable</i> | True means enable SAI Rx, false means disable. |

### 33.6.10 static uint32\_t SAI\_TxGetStatusFlag ( I2S\_Type \* *base* ) [inline], [static]

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | SAI base pointer |
|-------------|------------------|

Returns

SAI Tx status flag value. Use the Status Mask to get the status value needed.

### 33.6.11 static void SAI\_TxClearStatusFlags ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

## Function Documentation

### Parameters

|             |                                                                                                                                                                                                        |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | SAI base pointer                                                                                                                                                                                       |
| <i>mask</i> | State mask. It can be a combination of the following source if defined: <ul style="list-style-type: none"><li>• kSAI_WordStartFlag</li><li>• kSAI_SyncErrorFlag</li><li>• kSAI_FIFOErrorFlag</li></ul> |

**33.6.12** `static uint32_t SAI_RxGetStatusFlag ( I2S_Type * base ) [inline], [static]`

### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | SAI base pointer |
|-------------|------------------|

### Returns

SAI Rx status flag value. Use the Status Mask to get the status value needed.

**33.6.13** `static void SAI_RxClearStatusFlags ( I2S_Type * base, uint32_t mask ) [inline], [static]`

### Parameters

|             |                                                                                                                                                                                                         |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | SAI base pointer                                                                                                                                                                                        |
| <i>mask</i> | State mask. It can be a combination of the following sources if defined. <ul style="list-style-type: none"><li>• kSAI_WordStartFlag</li><li>• kSAI_SyncErrorFlag</li><li>• kSAI_FIFOErrorFlag</li></ul> |

**33.6.14** `static void SAI_TxEnableInterrupts ( I2S_Type * base, uint32_t mask ) [inline], [static]`

## Parameters

|             |                                                                                                                                                                                                                                                                                                                                                   |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | SAI base pointer                                                                                                                                                                                                                                                                                                                                  |
| <i>mask</i> | interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> <li>• kSAI_WordStartInterruptEnable</li> <li>• kSAI_SyncErrorInterruptEnable</li> <li>• kSAI_FIFOWarningInterruptEnable</li> <li>• kSAI_FIFOResultInterruptEnable</li> <li>• kSAI_FIFOErrorInterruptEnable</li> </ul> |

### 33.6.15 static void SAI\_RxEnableInterrupts ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

## Parameters

|             |                                                                                                                                                                                                                                                                                                                                                   |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | SAI base pointer                                                                                                                                                                                                                                                                                                                                  |
| <i>mask</i> | interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> <li>• kSAI_WordStartInterruptEnable</li> <li>• kSAI_SyncErrorInterruptEnable</li> <li>• kSAI_FIFOWarningInterruptEnable</li> <li>• kSAI_FIFOResultInterruptEnable</li> <li>• kSAI_FIFOErrorInterruptEnable</li> </ul> |

## Function Documentation

### 33.6.16 static void SAI\_TxDisableInterrupts ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

#### Parameters

|             |                                                                                                                                                                                                                                                                                                                                              |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | SAI base pointer                                                                                                                                                                                                                                                                                                                             |
| <i>mask</i> | interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"><li>• kSAI_WordStartInterruptEnable</li><li>• kSAI_SyncErrorInterruptEnable</li><li>• kSAI_FIFOWarningInterruptEnable</li><li>• kSAI_FIFORequestInterruptEnable</li><li>• kSAI_FIFOErrorInterruptEnable</li></ul> |

### 33.6.17 static void SAI\_RxDisableInterrupts ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

#### Parameters

|             |                                                                                                                                                                                                                                                                                                                                              |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | SAI base pointer                                                                                                                                                                                                                                                                                                                             |
| <i>mask</i> | interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"><li>• kSAI_WordStartInterruptEnable</li><li>• kSAI_SyncErrorInterruptEnable</li><li>• kSAI_FIFOWarningInterruptEnable</li><li>• kSAI_FIFORequestInterruptEnable</li><li>• kSAI_FIFOErrorInterruptEnable</li></ul> |

### 33.6.18 static void SAI\_TxEnableDMA ( I2S\_Type \* *base*, uint32\_t *mask*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                                                                                                                                                    |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer                                                                                                                                                                                   |
| <i>mask</i>   | DMA source The parameter can be combination of the following sources if defined. <ul style="list-style-type: none"> <li>• kSAI_FIFOWarningDMAEnable</li> <li>• kSAI_FIFOResultDMAEnable</li> </ul> |
| <i>enable</i> | True means enable DMA, false means disable DMA.                                                                                                                                                    |

### 33.6.19 static void SAI\_RxEnableDMA ( I2S\_Type \* *base*, uint32\_t *mask*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                                                                                                                                                      |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer                                                                                                                                                                                     |
| <i>mask</i>   | DMA source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> <li>• kSAI_FIFOWarningDMAEnable</li> <li>• kSAI_FIFOResultDMAEnable</li> </ul> |
| <i>enable</i> | True means enable DMA, false means disable DMA.                                                                                                                                                      |

### 33.6.20 static uint32\_t SAI\_TxGetDataRegisterAddress ( I2S\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

|                |                          |
|----------------|--------------------------|
| <i>base</i>    | SAI base pointer.        |
| <i>channel</i> | Which data channel used. |

Returns

data register address.

---

## Function Documentation

**33.6.21**   **static uint32\_t SAI\_RxGetDataRegisterAddress ( I2S\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This API is used to provide a transfer address for the SAI DMA transfer configuration.

## Parameters

|                |                          |
|----------------|--------------------------|
| <i>base</i>    | SAI base pointer.        |
| <i>channel</i> | Which data channel used. |

## Returns

data register address.

**33.6.22 void SAI\_TxSetFormat ( I2S\_Type \* *base*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

## Parameters

|                           |                                                                                                                             |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                           |
| <i>format</i>             | Pointer to the SAI audio data format structure.                                                                             |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                    |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz. |

**33.6.23 void SAI\_RxSetFormat ( I2S\_Type \* *base*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

## Parameters

|                           |                                                                                                                             |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                           |
| <i>format</i>             | Pointer to the SAI audio data format structure.                                                                             |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                    |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz. |

## Function Documentation

### 33.6.24 void SAI\_WriteBlocking ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *bitWidth*, uint8\_t \* *buffer*, uint32\_t *size* )

#### Note

This function blocks by polling until data is ready to be sent.

#### Parameters

|                 |                                                          |
|-----------------|----------------------------------------------------------|
| <i>base</i>     | SAI base pointer.                                        |
| <i>channel</i>  | Data channel used.                                       |
| <i>bitWidth</i> | How many bits in an audio word; usually 8/16/24/32 bits. |
| <i>buffer</i>   | Pointer to the data to be written.                       |
| <i>size</i>     | Bytes to be written.                                     |

### 33.6.25 static void SAI\_WriteData ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *data* ) [inline], [static]

#### Parameters

|                |                           |
|----------------|---------------------------|
| <i>base</i>    | SAI base pointer.         |
| <i>channel</i> | Data channel used.        |
| <i>data</i>    | Data needs to be written. |

### 33.6.26 void SAI\_ReadBlocking ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *bitWidth*, uint8\_t \* *buffer*, uint32\_t *size* )

#### Note

This function blocks by polling until data is ready to be sent.

#### Parameters

|                 |                                                          |
|-----------------|----------------------------------------------------------|
| <i>base</i>     | SAI base pointer.                                        |
| <i>channel</i>  | Data channel used.                                       |
| <i>bitWidth</i> | How many bits in an audio word; usually 8/16/24/32 bits. |
| <i>buffer</i>   | Pointer to the data to be read.                          |
| <i>size</i>     | Bytes to be read.                                        |



**33.6.27** `static uint32_t SAI_ReadData ( l2s_Type * base, uint32_t channel )`  
`[inline], [static]`

## Function Documentation

### Parameters

|                |                    |
|----------------|--------------------|
| <i>base</i>    | SAI base pointer.  |
| <i>channel</i> | Data channel used. |

### Returns

Data in SAI FIFO.

### 33.6.28 void SAI\_TransferTxCreateHandle ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the Tx handle for the SAI Tx transactional APIs. Call this function once to get the handle initialized.

### Parameters

|                 |                                                |
|-----------------|------------------------------------------------|
| <i>base</i>     | SAI base pointer                               |
| <i>handle</i>   | SAI handle pointer.                            |
| <i>callback</i> | Pointer to the user callback function.         |
| <i>userData</i> | User parameter passed to the callback function |

### 33.6.29 void SAI\_TransferRxCreateHandle ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the Rx handle for the SAI Rx transactional APIs. Call this function once to get the handle initialized.

### Parameters

|                 |                                                 |
|-----------------|-------------------------------------------------|
| <i>base</i>     | SAI base pointer.                               |
| <i>handle</i>   | SAI handle pointer.                             |
| <i>callback</i> | Pointer to the user callback function.          |
| <i>userData</i> | User parameter passed to the callback function. |

### 33.6.30 **status\_t SAI\_TransferTxSetFormat ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

|                           |                                                                                                                                     |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                                   |
| <i>handle</i>             | SAI handle pointer.                                                                                                                 |
| <i>format</i>             | Pointer to the SAI audio data format structure.                                                                                     |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                            |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the masterClockHz in format. |

Returns

Status of this function. Return value is the status\_t.

### 33.6.31 **status\_t SAI\_TransferRxSetFormat ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

|                           |                                                                                                                                     |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                                   |
| <i>handle</i>             | SAI handle pointer.                                                                                                                 |
| <i>format</i>             | Pointer to the SAI audio data format structure.                                                                                     |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                            |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the masterClockHz in format. |

## Function Documentation

### Returns

Status of this function. Return value is one of `status_t`.

### 33.6.32 `status_t SAI_TransferSendNonBlocking ( I2S_Type * base, sai_handle_t * handle, sai_transfer_t * xfer )`

#### Note

This API returns immediately after the transfer initiates. Call the `SAI_TxGetTransferStatusIRQ` to poll the transfer status and check whether the transfer is finished. If the return status is not `kStatus_SAI_Busy`, the transfer is finished.

#### Parameters

|               |                                                                                     |
|---------------|-------------------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer.                                                                   |
| <i>handle</i> | Pointer to the <code>sai_handle_t</code> structure which stores the transfer state. |
| <i>xfer</i>   | Pointer to the <code>sai_transfer_t</code> structure.                               |

#### Return values

|                                |                                        |
|--------------------------------|----------------------------------------|
| <i>kStatus_Success</i>         | Successfully started the data receive. |
| <i>kStatus_SAI_TxBusy</i>      | Previous receive still not finished.   |
| <i>kStatus_InvalidArgument</i> | The input parameter is invalid.        |

### 33.6.33 `status_t SAI_TransferReceiveNonBlocking ( I2S_Type * base, sai_handle_t * handle, sai_transfer_t * xfer )`

#### Note

This API returns immediately after the transfer initiates. Call the `SAI_RxGetTransferStatusIRQ` to poll the transfer status and check whether the transfer is finished. If the return status is not `kStatus_SAI_Busy`, the transfer is finished.

#### Parameters

---

|               |                                                                                     |
|---------------|-------------------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer                                                                    |
| <i>handle</i> | Pointer to the <code>sai_handle_t</code> structure which stores the transfer state. |
| <i>xfer</i>   | Pointer to the <a href="#">sai_transfer_t</a> structure.                            |

Return values

|                                |                                        |
|--------------------------------|----------------------------------------|
| <i>kStatus_Success</i>         | Successfully started the data receive. |
| <i>kStatus_SAI_RxBusy</i>      | Previous receive still not finished.   |
| <i>kStatus_InvalidArgument</i> | The input parameter is invalid.        |

### 33.6.34 **status\_t SAI\_TransferGetSendCount ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, size\_t \* *count* )**

Parameters

|               |                                                                                     |
|---------------|-------------------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer.                                                                   |
| <i>handle</i> | Pointer to the <code>sai_handle_t</code> structure which stores the transfer state. |
| <i>count</i>  | Bytes count sent.                                                                   |

Return values

|                                     |                                                                |
|-------------------------------------|----------------------------------------------------------------|
| <i>kStatus_Success</i>              | Succeed get the transfer count.                                |
| <i>kStatus_NoTransferInProgress</i> | There is not a non-blocking transaction currently in progress. |

### 33.6.35 **status\_t SAI\_TransferGetReceiveCount ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, size\_t \* *count* )**

Parameters

|               |                                                                                     |
|---------------|-------------------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer.                                                                   |
| <i>handle</i> | Pointer to the <code>sai_handle_t</code> structure which stores the transfer state. |
| <i>count</i>  | Bytes count received.                                                               |

## Function Documentation

### Return values

|                                     |                                                                |
|-------------------------------------|----------------------------------------------------------------|
| <i>kStatus_Success</i>              | Succeed get the transfer count.                                |
| <i>kStatus_NoTransferInProgress</i> | There is not a non-blocking transaction currently in progress. |

### 33.6.36 void SAI\_TransferAbortSend ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

#### Note

This API can be called any time when an interrupt non-blocking transfer initiates to abort the transfer early.

#### Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer.                                                      |
| <i>handle</i> | Pointer to the sai_handle_t structure which stores the transfer state. |

### 33.6.37 void SAI\_TransferAbortReceive ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

#### Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

#### Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | SAI base pointer                                                       |
| <i>handle</i> | Pointer to the sai_handle_t structure which stores the transfer state. |

### 33.6.38 void SAI\_TransferTxHandleIRQ ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

#### Parameters

|               |                                        |
|---------------|----------------------------------------|
| <i>base</i>   | SAI base pointer.                      |
| <i>handle</i> | Pointer to the sai_handle_t structure. |

### 33.6.39 void SAI\_TransferRxHandleIRQ ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

## Parameters

|               |                                        |
|---------------|----------------------------------------|
| <i>base</i>   | SAI base pointer.                      |
| <i>handle</i> | Pointer to the sai_handle_t structure. |

### 33.7 SAI DMA Driver

#### 33.7.1 Overview

##### Data Structures

- struct [sai\\_dma\\_handle\\_t](#)  
*SAI DMA transfer handle, users should not touch the content of the handle. [More...](#)*

##### Typedefs

- typedef void(\* [sai\\_dma\\_callback\\_t](#))(I2S\_Type \*base, sai\_dma\_handle\_t \*handle, status\_t status, void \*userData)  
*Define SAI DMA callback.*

##### DMA Transactional

- void [SAI\\_TransferTxCreateHandleDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, [sai\\_dma\\_callback\\_t](#) callback, void \*userData, dma\_handle\_t \*dmaHandle)  
*Initializes the SAI master DMA handle.*
- void [SAI\\_TransferRxCreateHandleDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, [sai\\_dma\\_callback\\_t](#) callback, void \*userData, dma\_handle\_t \*dmaHandle)  
*Initializes the SAI slave DMA handle.*
- void [SAI\\_TransferTxSetFormatDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, [sai\\_transfer\\_format\\_t](#) \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Tx audio format.*
- void [SAI\\_TransferRxSetFormatDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, [sai\\_transfer\\_format\\_t](#) \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Rx audio format.*
- status\_t [SAI\\_TransferSendDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, [sai\\_transfer\\_t](#) \*xfer)  
*Performs a non-blocking SAI transfer using DMA.*
- status\_t [SAI\\_TransferReceiveDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, [sai\\_transfer\\_t](#) \*xfer)  
*Performs a non-blocking SAI transfer using DMA.*
- void [SAI\\_TransferAbortSendDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle)  
*Aborts a SAI transfer using DMA.*
- void [SAI\\_TransferAbortReceiveDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle)  
*Aborts a SAI transfer using DMA.*
- status\_t [SAI\\_TransferGetSendCountDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, size\_t \*count)  
*Gets byte count sent by SAI.*
- status\_t [SAI\\_TransferGetReceiveCountDMA](#) (I2S\_Type \*base, sai\_dma\_handle\_t \*handle, size\_t \*count)  
*Gets byte count received by SAI.*



## 33.7.2 Data Structure Documentation

### 33.7.2.1 struct \_sai\_dma\_handle

#### Data Fields

- dma\_handle\_t \* [dmaHandle](#)  
*DMA handler for SAI send.*
- uint8\_t [bytesPerFrame](#)  
*Bytes in a frame.*
- uint8\_t [channel](#)  
*Which Data channel SAI use.*
- uint32\_t [state](#)  
*SAI DMA transfer internal state.*
- [sai\\_dma\\_callback\\_t](#) [callback](#)  
*Callback for users while transfer finish or error occurred.*
- void \* [userData](#)  
*User callback parameter.*
- [sai\\_transfer\\_t](#) [saiQueue](#) [SAI\_XFER\_QUEUE\_SIZE]  
*Transfer queue storing queued transfer.*
- size\_t [transferSize](#) [SAI\_XFER\_QUEUE\_SIZE]  
*Data bytes need to transfer.*
- volatile uint8\_t [queueUser](#)  
*Index for user to queue transfer.*
- volatile uint8\_t [queueDriver](#)  
*Index for driver to get the transfer data and size.*

#### 33.7.2.1.0.83 Field Documentation

33.7.2.1.0.83.1 [sai\\_transfer\\_t](#) [sai\\_dma\\_handle\\_t::saiQueue](#)[SAI\_XFER\_QUEUE\_SIZE]

33.7.2.1.0.83.2 [volatile uint8\\_t](#) [sai\\_dma\\_handle\\_t::queueUser](#)

## 33.7.3 Function Documentation

33.7.3.1 **void** [SAI\\_TransferTxCreateHandleDMA](#) ( [I2S\\_Type](#) \* *base*, [sai\\_dma\\_handle\\_t](#) \* *handle*, [sai\\_dma\\_callback\\_t](#) *callback*, void \* *userData*, [dma\\_handle\\_t](#) \* *dmaHandle* )

This function initializes the SAI master DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

## SAI DMA Driver

### Parameters

|                  |                                                                     |
|------------------|---------------------------------------------------------------------|
| <i>base</i>      | SAI base pointer.                                                   |
| <i>handle</i>    | SAI DMA handle pointer.                                             |
| <i>base</i>      | SAI peripheral base address.                                        |
| <i>callback</i>  | Pointer to user callback function.                                  |
| <i>userData</i>  | User parameter passed to the callback function.                     |
| <i>dmaHandle</i> | DMA handle pointer, this handle shall be static allocated by users. |

**33.7.3.2 void SAI\_TransferRxCreateHandleDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle*, sai\_dma\_callback\_t *callback*, void \* *userData*, dma\_handle\_t \* *dmaHandle* )**

This function initializes the SAI slave DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

### Parameters

|                  |                                                                     |
|------------------|---------------------------------------------------------------------|
| <i>base</i>      | SAI base pointer.                                                   |
| <i>handle</i>    | SAI DMA handle pointer.                                             |
| <i>base</i>      | SAI peripheral base address.                                        |
| <i>callback</i>  | Pointer to user callback function.                                  |
| <i>userData</i>  | User parameter passed to the callback function.                     |
| <i>dmaHandle</i> | DMA handle pointer, this handle shall be static allocated by users. |

**33.7.3.3 void SAI\_TransferTxSetFormatDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to the format.

## Parameters

|                           |                                                                                                                                  |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                                |
| <i>handle</i>             | SAI DMA handle pointer.                                                                                                          |
| <i>format</i>             | Pointer to SAI audio data format structure.                                                                                      |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                         |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If bit clock source is master. clock, this value should equals to masterClockHz in format. |

## Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | Audio format set successfully.  |
| <i>kStatus_InvalidArgument</i> | The input arguments is invalid. |

**33.7.3.4 void SAI\_TransferRxSetFormatDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets eDMA parameter according to format.

## Parameters

|                           |                                                                                                                                  |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                                |
| <i>handle</i>             | SAI DMA handle pointer.                                                                                                          |
| <i>format</i>             | Pointer to SAI audio data format structure.                                                                                      |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                         |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If bit clock source is master. clock, this value should equals to masterClockHz in format. |

## Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | Audio format set successfully.  |
| <i>kStatus_InvalidArgument</i> | The input arguments is invalid. |

**33.7.3.5 status\_t SAI\_TransferSendDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )**

## SAI DMA Driver

### Note

This interface returns immediately after the transfer initiates. Call the SAI\_GetTransferStatus to poll the transfer status to check whether the SAI transfer finished.

### Parameters

|               |                                    |
|---------------|------------------------------------|
| <i>base</i>   | SAI base pointer.                  |
| <i>handle</i> | SAI DMA handle pointer.            |
| <i>xfer</i>   | Pointer to DMA transfer structure. |

### Return values

|                                |                                      |
|--------------------------------|--------------------------------------|
| <i>kStatus_Success</i>         | Successfully start the data receive. |
| <i>kStatus_SAI_TxBusy</i>      | Previous receive still not finished. |
| <i>kStatus_InvalidArgument</i> | The input parameter is invalid.      |

### 33.7.3.6 status\_t SAI\_TransferReceiveDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )

### Note

This interface returns immediately after transfer initiates. Call SAI\_GetTransferStatus to poll the transfer status to check whether the SAI transfer is finished.

### Parameters

|               |                                    |
|---------------|------------------------------------|
| <i>base</i>   | SAI base pointer                   |
| <i>handle</i> | SAI DMA handle pointer.            |
| <i>xfer</i>   | Pointer to DMA transfer structure. |

### Return values

|                                |                                      |
|--------------------------------|--------------------------------------|
| <i>kStatus_Success</i>         | Successfully start the data receive. |
| <i>kStatus_SAI_RxBusy</i>      | Previous receive still not finished. |
| <i>kStatus_InvalidArgument</i> | The input parameter is invalid.      |

### 33.7.3.7 void SAI\_TransferAbortSendDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle* )

## Parameters

|               |                         |
|---------------|-------------------------|
| <i>base</i>   | SAI base pointer.       |
| <i>handle</i> | SAI DMA handle pointer. |

### 33.7.3.8 void SAI\_TransferAbortReceiveDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle* )

## Parameters

|               |                         |
|---------------|-------------------------|
| <i>base</i>   | SAI base pointer.       |
| <i>handle</i> | SAI DMA handle pointer. |

### 33.7.3.9 status\_t SAI\_TransferGetSendCountDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle*, size\_t \* *count* )

## Parameters

|               |                          |
|---------------|--------------------------|
| <i>base</i>   | SAI base pointer.        |
| <i>handle</i> | SAI DMA handle pointer.  |
| <i>count</i>  | Bytes count sent by SAI. |

## Return values

|                                     |                                                                |
|-------------------------------------|----------------------------------------------------------------|
| <i>kStatus_Success</i>              | Succeed get the transfer count.                                |
| <i>kStatus_NoTransferInProgress</i> | There is not a non-blocking transaction currently in progress. |

### 33.7.3.10 status\_t SAI\_TransferGetReceiveCountDMA ( I2S\_Type \* *base*, sai\_dma\_handle\_t \* *handle*, size\_t \* *count* )

## Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | SAI base pointer.            |
| <i>handle</i> | SAI DMA handle pointer.      |
| <i>count</i>  | Bytes count received by SAI. |

## SAI DMA Driver

Return values

|                                      |                                                                |
|--------------------------------------|----------------------------------------------------------------|
| <i>kStatus_Success</i>               | Succeed get the transfer count.                                |
| <i>kStatus_NoTransferIn-Progress</i> | There is not a non-blocking transaction currently in progress. |

## 33.8 SAI eDMA Driver

### 33.8.1 Overview

#### Data Structures

- struct [sai\\_edma\\_handle\\_t](#)  
SAI DMA transfer handle, users should not touch the content of the handle. [More...](#)

#### Typedefs

- typedef void(\* [sai\\_edma\\_callback\\_t](#))(I2S\_Type \*base, sai\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
SAI eDMA transfer callback function for finish and error.

#### eDMA Transactional

- void [SAI\\_TransferTxCreateHandleEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, [sai\\_edma\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*dmaHandle)  
*Initializes the SAI eDMA handle.*
- void [SAI\\_TransferRxCreateHandleEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, [sai\\_edma\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*dmaHandle)  
*Initializes the SAI Rx eDMA handle.*
- void [SAI\\_TransferTxSetFormatEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, [sai\\_transfer\\_format\\_t](#) \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Tx audio format.*
- void [SAI\\_TransferRxSetFormatEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, [sai\\_transfer\\_format\\_t](#) \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Rx audio format.*
- status\_t [SAI\\_TransferSendEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, [sai\\_transfer\\_t](#) \*xfer)  
*Performs a non-blocking SAI transfer using DMA.*
- status\_t [SAI\\_TransferReceiveEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, [sai\\_transfer\\_t](#) \*xfer)  
*Performs a non-blocking SAI receive using eDMA.*
- void [SAI\\_TransferAbortSendEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle)  
*Aborts a SAI transfer using eDMA.*
- void [SAI\\_TransferAbortReceiveEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle)  
*Aborts a SAI receive using eDMA.*
- status\_t [SAI\\_TransferGetSendCountEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets byte count sent by SAI.*
- status\_t [SAI\\_TransferGetReceiveCountEDMA](#) (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets byte count received by SAI.*

### 33.8.2 Data Structure Documentation

#### 33.8.2.1 struct \_sai\_edma\_handle

##### Data Fields

- [edma\\_handle\\_t](#) \* [dmaHandle](#)  
*DMA handler for SAI send.*
- [uint8\\_t](#) [nbytes](#)  
*eDMA minor byte transfer count initially configured.*
- [uint8\\_t](#) [bytesPerFrame](#)  
*Bytes in a frame.*
- [uint8\\_t](#) [channel](#)  
*Which data channel.*
- [uint8\\_t](#) [count](#)  
*The transfer data count in a DMA request.*
- [uint32\\_t](#) [state](#)  
*Internal state for SAI eDMA transfer.*
- [sai\\_edma\\_callback\\_t](#) [callback](#)  
*Callback for users while transfer finish or error occurs.*
- [void](#) \* [userData](#)  
*User callback parameter.*
- [edma\\_tcd\\_t](#) [tcd](#) [[SAI\\_XFER\\_QUEUE\\_SIZE](#)+1U]  
*TCD pool for eDMA transfer.*
- [sai\\_transfer\\_t](#) [saiQueue](#) [[SAI\\_XFER\\_QUEUE\\_SIZE](#)]  
*Transfer queue storing queued transfer.*
- [size\\_t](#) [transferSize](#) [[SAI\\_XFER\\_QUEUE\\_SIZE](#)]  
*Data bytes need to transfer.*
- [volatile uint8\\_t](#) [queueUser](#)  
*Index for user to queue transfer.*
- [volatile uint8\\_t](#) [queueDriver](#)  
*Index for driver to get the transfer data and size.*



### 33.8.2.1.0.84 Field Documentation

33.8.2.1.0.84.1 `uint8_t sai_edma_handle_t::nbytes`

33.8.2.1.0.84.2 `edma_tcd_t sai_edma_handle_t::tcd[SAI_XFER_QUEUE_SIZE+1U]`

33.8.2.1.0.84.3 `sai_transfer_t sai_edma_handle_t::saiQueue[SAI_XFER_QUEUE_SIZE]`

33.8.2.1.0.84.4 `volatile uint8_t sai_edma_handle_t::queueUser`

### 33.8.3 Function Documentation

33.8.3.1 `void SAI_TransferTxCreateHandleEDMA ( I2S_Type * base, sai_edma_handle_t * handle, sai_edma_callback_t callback, void * userData, edma_handle_t * dmaHandle )`

This function initializes the SAI master DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

## SAI eDMA Driver

### Parameters

|                  |                                                                      |
|------------------|----------------------------------------------------------------------|
| <i>base</i>      | SAI base pointer.                                                    |
| <i>handle</i>    | SAI eDMA handle pointer.                                             |
| <i>base</i>      | SAI peripheral base address.                                         |
| <i>callback</i>  | Pointer to user callback function.                                   |
| <i>userData</i>  | User parameter passed to the callback function.                      |
| <i>dmaHandle</i> | eDMA handle pointer, this handle shall be static allocated by users. |

**33.8.3.2 void SAI\_TransferRxCreateHandleEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_edma\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *dmaHandle* )**

This function initializes the SAI slave DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

### Parameters

|                  |                                                                      |
|------------------|----------------------------------------------------------------------|
| <i>base</i>      | SAI base pointer.                                                    |
| <i>handle</i>    | SAI eDMA handle pointer.                                             |
| <i>base</i>      | SAI peripheral base address.                                         |
| <i>callback</i>  | Pointer to user callback function.                                   |
| <i>userData</i>  | User parameter passed to the callback function.                      |
| <i>dmaHandle</i> | eDMA handle pointer, this handle shall be static allocated by users. |

**33.8.3.3 void SAI\_TransferTxSetFormatEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to formatting requirements.

## Parameters

|                           |                                                                                                                                 |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                               |
| <i>handle</i>             | SAI eDMA handle pointer.                                                                                                        |
| <i>format</i>             | Pointer to SAI audio data format structure.                                                                                     |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                        |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If bit clock source is master clock, this value should equals to masterClockHz in format. |

## Return values

|                                |                                |
|--------------------------------|--------------------------------|
| <i>kStatus_Success</i>         | Audio format set successfully. |
| <i>kStatus_InvalidArgument</i> | The input argument is invalid. |

**33.8.3.4 void SAI\_TransferRxSetFormatEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to formatting requirements.

## Parameters

|                           |                                                                                                                                      |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | SAI base pointer.                                                                                                                    |
| <i>handle</i>             | SAI eDMA handle pointer.                                                                                                             |
| <i>format</i>             | Pointer to SAI audio data format structure.                                                                                          |
| <i>mclkSource-ClockHz</i> | SAI master clock source frequency in Hz.                                                                                             |
| <i>bclkSource-ClockHz</i> | SAI bit clock source frequency in Hz. If a bit clock source is the master clock, this value should equal to masterClockHz in format. |

## Return values

|                                |                                |
|--------------------------------|--------------------------------|
| <i>kStatus_Success</i>         | Audio format set successfully. |
| <i>kStatus_InvalidArgument</i> | The input argument is invalid. |

**33.8.3.5 status\_t SAI\_TransferSendEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )**

## SAI eDMA Driver

### Note

This interface returns immediately after the transfer initiates. Call SAI\_GetTransferStatus to poll the transfer status and check whether the SAI transfer is finished.

### Parameters

|               |                                        |
|---------------|----------------------------------------|
| <i>base</i>   | SAI base pointer.                      |
| <i>handle</i> | SAI eDMA handle pointer.               |
| <i>xfer</i>   | Pointer to the DMA transfer structure. |

### Return values

|                                |                                     |
|--------------------------------|-------------------------------------|
| <i>kStatus_Success</i>         | Start a SAI eDMA send successfully. |
| <i>kStatus_InvalidArgument</i> | The input argument is invalid.      |
| <i>kStatus_TxBusy</i>          | SAI is busy sending data.           |

### 33.8.3.6 status\_t SAI\_TransferReceiveEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )

### Note

This interface returns immediately after the transfer initiates. Call the SAI\_GetReceiveRemaining-Bytes to poll the transfer status and check whether the SAI transfer is finished.

### Parameters

|               |                                    |
|---------------|------------------------------------|
| <i>base</i>   | SAI base pointer                   |
| <i>handle</i> | SAI eDMA handle pointer.           |
| <i>xfer</i>   | Pointer to DMA transfer structure. |

### Return values

|                                |                                        |
|--------------------------------|----------------------------------------|
| <i>kStatus_Success</i>         | Start a SAI eDMA receive successfully. |
| <i>kStatus_InvalidArgument</i> | The input argument is invalid.         |
| <i>kStatus_RxBusy</i>          | SAI is busy receiving data.            |

### 33.8.3.7 void SAI\_TransferAbortSendEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle* )

## Parameters

|               |                          |
|---------------|--------------------------|
| <i>base</i>   | SAI base pointer.        |
| <i>handle</i> | SAI eDMA handle pointer. |

### 33.8.3.8 void SAI\_TransferAbortReceiveEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle* )

## Parameters

|               |                          |
|---------------|--------------------------|
| <i>base</i>   | SAI base pointer         |
| <i>handle</i> | SAI eDMA handle pointer. |

### 33.8.3.9 status\_t SAI\_TransferGetSendCountEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, size\_t \* *count* )

## Parameters

|               |                          |
|---------------|--------------------------|
| <i>base</i>   | SAI base pointer.        |
| <i>handle</i> | SAI eDMA handle pointer. |
| <i>count</i>  | Bytes count sent by SAI. |

## Return values

|                                     |                                                   |
|-------------------------------------|---------------------------------------------------|
| <i>kStatus_Success</i>              | Succeed get the transfer count.                   |
| <i>kStatus_NoTransferInProgress</i> | There is no non-blocking transaction in progress. |

### 33.8.3.10 status\_t SAI\_TransferGetReceiveCountEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, size\_t \* *count* )

## Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | SAI base pointer             |
| <i>handle</i> | SAI eDMA handle pointer.     |
| <i>count</i>  | Bytes count received by SAI. |

## SAI eDMA Driver

### Return values

|                                     |                                                   |
|-------------------------------------|---------------------------------------------------|
| <i>kStatus_Success</i>              | Succeed get the transfer count.                   |
| <i>kStatus_NoTransferInProgress</i> | There is no non-blocking transaction in progress. |

## Chapter 34

# SDHC: Secured Digital Host Controller Driver

### 34.1 Overview

The KSDK provides a peripheral driver for the Secured Digital Host Controller (SDHC) module of Kinetis devices.

### 34.2 Typical use case

#### 34.2.1 SDHC Operation

```
/* Initializes the SDHC. */
sdhcConfig->cardDetectDat3 = false;
sdhcConfig->endianMode = kSDHC_EndianModeLittle;
sdhcConfig->dmaMode = kSDHC_DmaModeAdma2;
sdhcConfig->readWatermarkLevel = 0x80U;
sdhcConfig->writeWatermarkLevel = 0x80U;
SDHC_Init(BOARD_SDHC_BASEADDR, sdhcConfig);

/* Fills state in the card driver. */
card->sdhcBase = BOARD_SDHC_BASEADDR;
card->sdhcSourceClock = CLOCK_GetFreq(BOARD_SDHC_CLKSRC);
card->sdhcTransfer = sdhc_transfer_function;

/* Initializes the card. */
if (SD_Init(card))
{
    PRINTF("\r\nSD card init failed.\r\n");
}

PRINTF("\r\nRead/Write/Erase the card continuously until it encounters error.....\r\n");
while (true)
{
    if (kStatus_Success != SD_WriteBlocks(card, g_dataWrite, DATA_BLOCK_START, DATA_BLOCK_COUNT))
    {
        PRINTF("Write multiple data blocks failed.\r\n");
    }
    if (kStatus_Success != SD_ReadBlocks(card, g_dataRead, DATA_BLOCK_START, DATA_BLOCK_COUNT))
    {
        PRINTF("Read multiple data blocks failed.\r\n");
    }
    if (kStatus_Success != SD_EraseBlocks(card, DATA_BLOCK_START, DATA_BLOCK_COUNT))
    {
        PRINTF("Erase multiple data blocks failed.\r\n");
    }
}

SD_Deinit(card);
```

### Data Structures

- struct [sdhc\\_adma2\\_descriptor\\_t](#)  
*Defines the ADMA2 descriptor structure. [More...](#)*
- struct [sdhc\\_capability\\_t](#)

## Typical use case

- *SDHC capability information. [More...](#)*  
struct [sdhc\\_transfer\\_config\\_t](#)
- *Card transfer configuration. [More...](#)*  
struct [sdhc\\_boot\\_config\\_t](#)
- *Data structure to configure the MMC boot feature. [More...](#)*  
struct [sdhc\\_config\\_t](#)
- *Data structure to initialize the SDHC. [More...](#)*  
struct [sdhc\\_data\\_t](#)
- *Card data descriptor. [More...](#)*  
struct [sdhc\\_command\\_t](#)
- *Card command descriptor. [More...](#)*  
struct [sdhc\\_transfer\\_t](#)
- *Transfer state. [More...](#)*  
struct [sdhc\\_transfer\\_callback\\_t](#)
- *SDHC callback functions. [More...](#)*  
struct [sdhc\\_handle\\_t](#)
- *SDHC handle. [More...](#)*  
struct [sdhc\\_host\\_t](#)
- *SDHC host descriptor. [More...](#)*

## Macros

- #define [SDHC\\_MAX\\_BLOCK\\_COUNT](#) (SDHC\_BLKATTR\_BLKCNT\_MASK >> SDHC\_BLKATTR\_BLKCNT\_SHIFT)  
*Maximum block count can be set one time.*
- #define [SDHC\\_ADMA1\\_ADDRESS\\_ALIGN](#) (4096U)  
*The alignment size for ADDRESS filed in ADMA1's descriptor.*
- #define [SDHC\\_ADMA1\\_LENGTH\\_ALIGN](#) (4096U)  
*The alignment size for LENGTH field in ADMA1's descriptor.*
- #define [SDHC\\_ADMA2\\_ADDRESS\\_ALIGN](#) (4U)  
*The alignment size for ADDRESS field in ADMA2's descriptor.*
- #define [SDHC\\_ADMA2\\_LENGTH\\_ALIGN](#) (4U)  
*The alignment size for LENGTH filed in ADMA2's descriptor.*
- #define [SDHC\\_ADMA1\\_DESCRIPTOR\\_ADDRESS\\_SHIFT](#) (12U)  
*The bit shift for ADDRESS filed in ADMA1's descriptor.*
- #define [SDHC\\_ADMA1\\_DESCRIPTOR\\_ADDRESS\\_MASK](#) (0xFFFFFU)  
*The bit mask for ADDRESS field in ADMA1's descriptor.*
- #define [SDHC\\_ADMA1\\_DESCRIPTOR\\_LENGTH\\_SHIFT](#) (12U)  
*The bit shift for LENGTH filed in ADMA1's descriptor.*
- #define [SDHC\\_ADMA1\\_DESCRIPTOR\\_LENGTH\\_MASK](#) (0xFFFFU)  
*The mask for LENGTH field in ADMA1's descriptor.*
- #define [SDHC\\_ADMA1\\_DESCRIPTOR\\_MAX\\_LENGTH\\_PER\\_ENTRY](#) (SDHC\_ADMA1\_DESCRIPTOR\_LENGTH\_MASK + 1U)  
*The maximum value of LENGTH filed in ADMA1's descriptor.*
- #define [SDHC\\_ADMA2\\_DESCRIPTOR\\_LENGTH\\_SHIFT](#) (16U)  
*The bit shift for LENGTH field in ADMA2's descriptor.*
- #define [SDHC\\_ADMA2\\_DESCRIPTOR\\_LENGTH\\_MASK](#) (0xFFFFU)  
*The bit mask for LENGTH field in ADMA2's descriptor.*
- #define [SDHC\\_ADMA2\\_DESCRIPTOR\\_MAX\\_LENGTH\\_PER\\_ENTRY](#) (SDHC\_ADMA2\_DESCRIPTOR\_LENGTH\_MASK)  
*The maximum value of LENGTH field in ADMA2's descriptor.*



## Typedefs

- typedef uint32\_t [sdhc\\_adma1\\_descriptor\\_t](#)  
*Defines the adma1 descriptor structure.*
- typedef status\_t(\* [sdhc\\_transfer\\_function\\_t](#))(SDHC\_Type \*base, [sdhc\\_transfer\\_t](#) \*content)  
*SDHC transfer function.*

## Enumerations

- enum [\\_sdhc\\_status](#) {  
[kStatus\\_SDHC\\_BusyTransferring](#) = MAKE\_STATUS(kStatusGroup\_SDHC, 0U),  
[kStatus\\_SDHC\\_PrepareAdmaDescriptorFailed](#) = MAKE\_STATUS(kStatusGroup\_SDHC, 1U),  
[kStatus\\_SDHC\\_SendCommandFailed](#) = MAKE\_STATUS(kStatusGroup\_SDHC, 2U),  
[kStatus\\_SDHC\\_TransferDataFailed](#) = MAKE\_STATUS(kStatusGroup\_SDHC, 3U) }  
*SDHC status.*
- enum [\\_sdhc\\_capability\\_flag](#) {  
[kSDHC\\_SupportAdmaFlag](#) = SDHC\_HTCAPBLT\_ADMAS\_MASK,  
[kSDHC\\_SupportHighSpeedFlag](#) = SDHC\_HTCAPBLT\_HSS\_MASK,  
[kSDHC\\_SupportDmaFlag](#) = SDHC\_HTCAPBLT\_DMAS\_MASK,  
[kSDHC\\_SupportSuspendResumeFlag](#) = SDHC\_HTCAPBLT\_SRS\_MASK,  
[kSDHC\\_SupportV330Flag](#) = SDHC\_HTCAPBLT\_VS33\_MASK,  
[kSDHC\\_Support4BitFlag](#) = (SDHC\_HTCAPBLT\_MBL\_SHIFT << 0U),  
[kSDHC\\_Support8BitFlag](#) = (SDHC\_HTCAPBLT\_MBL\_SHIFT << 1U) }  
*Host controller capabilities flag mask.*
- enum [\\_sdhc\\_wakeup\\_event](#) {  
[kSDHC\\_WakeupEventOnCardInt](#) = SDHC\_PROCTL\_WECINT\_MASK,  
[kSDHC\\_WakeupEventOnCardInsert](#) = SDHC\_PROCTL\_WECINS\_MASK,  
[kSDHC\\_WakeupEventOnCardRemove](#) = SDHC\_PROCTL\_WECRM\_MASK,  
[kSDHC\\_WakeupEventsAll](#) }  
*Wakeup event mask.*
- enum [\\_sdhc\\_reset](#) {  
[kSDHC\\_ResetAll](#) = SDHC\_SYSCTL\_RSTA\_MASK,  
[kSDHC\\_ResetCommand](#) = SDHC\_SYSCTL\_RSTC\_MASK,  
[kSDHC\\_ResetData](#) = SDHC\_SYSCTL\_RSTD\_MASK,  
[kSDHC\\_ResetsAll](#) = (kSDHC\_ResetAll | kSDHC\_ResetCommand | kSDHC\_ResetData) }  
*Reset type mask.*
- enum [\\_sdhc\\_transfer\\_flag](#) {

## Typical use case

```
kSDHC_EnableDmaFlag = SDHC_XFERTYP_DMAEN_MASK,  
kSDHC_CommandTypeSuspendFlag = (SDHC_XFERTYP_CMDTYP(1U)),  
kSDHC_CommandTypeResumeFlag = (SDHC_XFERTYP_CMDTYP(2U)),  
kSDHC_CommandTypeAbortFlag = (SDHC_XFERTYP_CMDTYP(3U)),  
kSDHC_EnableBlockCountFlag = SDHC_XFERTYP_BCEN_MASK,  
kSDHC_EnableAutoCommand12Flag = SDHC_XFERTYP_AC12EN_MASK,  
kSDHC_DataReadFlag = SDHC_XFERTYP_DTDSEL_MASK,  
kSDHC_MultipleBlockFlag = SDHC_XFERTYP_MSBSEL_MASK,  
kSDHC_ResponseLength136Flag = SDHC_XFERTYP_RSPTYP(1U),  
kSDHC_ResponseLength48Flag = SDHC_XFERTYP_RSPTYP(2U),  
kSDHC_ResponseLength48BusyFlag = SDHC_XFERTYP_RSPTYP(3U),  
kSDHC_EnableCrcCheckFlag = SDHC_XFERTYP_CCCEN_MASK,  
kSDHC_EnableIndexCheckFlag = SDHC_XFERTYP_CICEN_MASK,  
kSDHC_DataPresentFlag = SDHC_XFERTYP_DPSEL_MASK }
```

*Transfer flag mask.*

- enum `_sdhc_present_status_flag` {  
    kSDHC\_CommandInhibitFlag = SDHC\_PRSSTAT\_CIHB\_MASK,  
    kSDHC\_DataInhibitFlag = SDHC\_PRSSTAT\_CDIHB\_MASK,  
    kSDHC\_DataLineActiveFlag = SDHC\_PRSSTAT\_DLA\_MASK,  
    kSDHC\_SdClockStableFlag = SDHC\_PRSSTAT\_SDSTB\_MASK,  
    kSDHC\_WriteTransferActiveFlag = SDHC\_PRSSTAT\_WTA\_MASK,  
    kSDHC\_ReadTransferActiveFlag = SDHC\_PRSSTAT\_RTA\_MASK,  
    kSDHC\_BufferWriteEnableFlag = SDHC\_PRSSTAT\_BWEN\_MASK,  
    kSDHC\_BufferReadEnableFlag = SDHC\_PRSSTAT\_BREN\_MASK,  
    kSDHC\_CardInsertedFlag = SDHC\_PRSSTAT\_CINS\_MASK,  
    kSDHC\_CommandLineLevelFlag = SDHC\_PRSSTAT\_CLSL\_MASK,  
    kSDHC\_Data0LineLevelFlag = (1U << 24U),  
    kSDHC\_Data1LineLevelFlag = (1U << 25U),  
    kSDHC\_Data2LineLevelFlag = (1U << 26U),  
    kSDHC\_Data3LineLevelFlag = (1U << 27U),  
    kSDHC\_Data4LineLevelFlag = (1U << 28U),  
    kSDHC\_Data5LineLevelFlag = (1U << 29U),  
    kSDHC\_Data6LineLevelFlag = (1U << 30U),  
    kSDHC\_Data7LineLevelFlag = (1U << 31U) }

*Present status flag mask.*

- enum `_sdhc_interrupt_status_flag` {

```

kSDHC_CommandCompleteFlag = SDHC_IRQSTAT_CC_MASK,
kSDHC_DataCompleteFlag = SDHC_IRQSTAT_TC_MASK,
kSDHC_BlockGapEventFlag = SDHC_IRQSTAT_BGE_MASK,
kSDHC_DmaCompleteFlag = SDHC_IRQSTAT_DINT_MASK,
kSDHC_BufferWriteReadyFlag = SDHC_IRQSTAT_BWR_MASK,
kSDHC_BufferReadReadyFlag = SDHC_IRQSTAT_BRR_MASK,
kSDHC_CardInsertionFlag = SDHC_IRQSTAT_CINS_MASK,
kSDHC_CardRemovalFlag = SDHC_IRQSTAT_CRM_MASK,
kSDHC_CardInterruptFlag = SDHC_IRQSTAT_CINT_MASK,
kSDHC_CommandTimeoutFlag = SDHC_IRQSTAT_CTOE_MASK,
kSDHC_CommandCrcErrorFlag = SDHC_IRQSTAT_CCE_MASK,
kSDHC_CommandEndBitErrorFlag = SDHC_IRQSTAT_CEBE_MASK,
kSDHC_CommandIndexErrorFlag = SDHC_IRQSTAT_CIE_MASK,
kSDHC_DataTimeoutFlag = SDHC_IRQSTAT_DTOE_MASK,
kSDHC_DataCrcErrorFlag = SDHC_IRQSTAT_DCE_MASK,
kSDHC_DataEndBitErrorFlag = SDHC_IRQSTAT_DEBE_MASK,
kSDHC_AutoCommand12ErrorFlag = SDHC_IRQSTAT_AC12E_MASK,
kSDHC_DmaErrorFlag = SDHC_IRQSTAT_DMAE_MASK,
kSDHC_CommandErrorFlag,
kSDHC_DataErrorFlag,
kSDHC_ErrorFlag = (kSDHC_CommandErrorFlag | kSDHC_DataErrorFlag | kSDHC_DmaError-
Flag),
kSDHC_DataFlag,
kSDHC_CommandFlag = (kSDHC_CommandErrorFlag | kSDHC_CommandCompleteFlag),
kSDHC_CardDetectFlag = (kSDHC_CardInsertionFlag | kSDHC_CardRemovalFlag),
kSDHC_AllInterruptFlags }

```

*Interrupt status flag mask.*

- enum `_sdhc_auto_command12_error_status_flag` {

```

kSDHC_AutoCommand12NotExecutedFlag = SDHC_AC12ERR_AC12NE_MASK,
kSDHC_AutoCommand12TimeoutFlag = SDHC_AC12ERR_AC12TOE_MASK,
kSDHC_AutoCommand12EndBitErrorFlag = SDHC_AC12ERR_AC12EBE_MASK,
kSDHC_AutoCommand12CrcErrorFlag = SDHC_AC12ERR_AC12CE_MASK,
kSDHC_AutoCommand12IndexErrorFlag = SDHC_AC12ERR_AC12IE_MASK,
kSDHC_AutoCommand12NotIssuedFlag = SDHC_AC12ERR_CNIBAC12E_MASK }

```

*Auto CMD12 error status flag mask.*

- enum `_sdhc_adma_error_status_flag` {

```

kSDHC_AdmaLenghMismatchFlag = SDHC_ADMAES_ADMALME_MASK,
kSDHC_AdmaDescriptorErrorFlag = SDHC_ADMAES_ADMADCE_MASK }

```

*ADMA error status flag mask.*

- enum `sdhc_adma_error_state_t` {

```

kSDHC_AdmaErrorStateStopDma = 0x00U,
kSDHC_AdmaErrorStateFetchDescriptor = 0x01U,
kSDHC_AdmaErrorStateChangeAddress = 0x02U,
kSDHC_AdmaErrorStateTransferData = 0x03U }

```

*ADMA error state.*

- enum `_sdhc_force_event` {

## Typical use case

```
kSDHC_ForceEventAutoCommand12NotExecuted = SDHC_FEVT_AC12NE_MASK,  
kSDHC_ForceEventAutoCommand12Timeout = SDHC_FEVT_AC12TOE_MASK,  
kSDHC_ForceEventAutoCommand12CrcError = SDHC_FEVT_AC12CE_MASK,  
kSDHC_ForceEventEndBitError = SDHC_FEVT_AC12EBE_MASK,  
kSDHC_ForceEventAutoCommand12IndexError = SDHC_FEVT_AC12IE_MASK,  
kSDHC_ForceEventAutoCommand12NotIssued = SDHC_FEVT_CNIBAC12E_MASK,  
kSDHC_ForceEventCommandTimeout = SDHC_FEVT_CTOE_MASK,  
kSDHC_ForceEventCommandCrcError = SDHC_FEVT_CCE_MASK,  
kSDHC_ForceEventCommandEndBitError = SDHC_FEVT_CEBE_MASK,  
kSDHC_ForceEventCommandIndexError = SDHC_FEVT_CIE_MASK,  
kSDHC_ForceEventDataTimeout = SDHC_FEVT_DTOE_MASK,  
kSDHC_ForceEventDataCrcError = SDHC_FEVT_DCE_MASK,  
kSDHC_ForceEventDataEndBitError = SDHC_FEVT_DEBE_MASK,  
kSDHC_ForceEventAutoCommand12Error = SDHC_FEVT_AC12E_MASK,  
kSDHC_ForceEventCardInt = SDHC_FEVT_CINT_MASK,  
kSDHC_ForceEventDmaError = SDHC_FEVT_DMAE_MASK,  
kSDHC_ForceEventsAll }
```

*Force event mask.*

- enum `sdhc_data_bus_width_t` {  
    `kSDHC_DataBusWidth1Bit` = 0U,  
    `kSDHC_DataBusWidth4Bit` = 1U,  
    `kSDHC_DataBusWidth8Bit` = 2U }

*Data transfer width.*

- enum `sdhc_endian_mode_t` {  
    `kSDHC_EndianModeBig` = 0U,  
    `kSDHC_EndianModeHalfWordBig` = 1U,  
    `kSDHC_EndianModeLittle` = 2U }

*Endian mode.*

- enum `sdhc_dma_mode_t` {  
    `kSDHC_DmaModeNo` = 0U,  
    `kSDHC_DmaModeAdma1` = 1U,  
    `kSDHC_DmaModeAdma2` = 2U }

*DMA mode.*

- enum `_sdhc_sdio_control_flag` {  
    `kSDHC_StopAtBlockGapFlag` = 0x01,  
    `kSDHC_ReadWaitControlFlag` = 0x02,  
    `kSDHC_InterruptAtBlockGapFlag` = 0x04,  
    `kSDHC_ExactBlockNumberReadFlag` = 0x08 }

*SDIO control flag mask.*

- enum `sdhc_boot_mode_t` {  
    `kSDHC_BootModeNormal` = 0U,  
    `kSDHC_BootModeAlternative` = 1U }

*MMC card boot mode.*

- enum `sdhc_command_type_t` {

```
kSDHC_CommandTypeNormal = 0U,
kSDHC_CommandTypeSuspend = 1U,
kSDHC_CommandTypeResume = 2U,
kSDHC_CommandTypeAbort = 3U }
```

*The command type.*

- enum `sdhc_response_type_t` {  
`kSDHC_ResponseTypeNone` = 0U,  
`kSDHC_ResponseTypeR1` = 1U,  
`kSDHC_ResponseTypeR1b` = 2U,  
`kSDHC_ResponseTypeR2` = 3U,  
`kSDHC_ResponseTypeR3` = 4U,  
`kSDHC_ResponseTypeR4` = 5U,  
`kSDHC_ResponseTypeR5` = 6U,  
`kSDHC_ResponseTypeR5b` = 7U,  
`kSDHC_ResponseTypeR6` = 8U,  
`kSDHC_ResponseTypeR7` = 9U }

*The command response type.*

- enum `_sdhc_adma1_descriptor_flag` {  
`kSDHC_Adma1DescriptorValidFlag` = (1U << 0U),  
`kSDHC_Adma1DescriptorEndFlag` = (1U << 1U),  
`kSDHC_Adma1DescriptorInterruptFlag` = (1U << 2U),  
`kSDHC_Adma1DescriptorActivity1Flag` = (1U << 4U),  
`kSDHC_Adma1DescriptorActivity2Flag` = (1U << 5U),  
`kSDHC_Adma1DescriptorTypeNop` = (kSDHC\_Adma1DescriptorValidFlag),  
`kSDHC_Adma1DescriptorTypeTransfer`,  
`kSDHC_Adma1DescriptorTypeLink`,  
`kSDHC_Adma1DescriptorTypeSetLength` }

*The mask for the control/status field in ADMA1 descriptor.*

- enum `_sdhc_adma2_descriptor_flag` {  
`kSDHC_Adma2DescriptorValidFlag` = (1U << 0U),  
`kSDHC_Adma2DescriptorEndFlag` = (1U << 1U),  
`kSDHC_Adma2DescriptorInterruptFlag` = (1U << 2U),  
`kSDHC_Adma2DescriptorActivity1Flag` = (1U << 4U),  
`kSDHC_Adma2DescriptorActivity2Flag` = (1U << 5U),  
`kSDHC_Adma2DescriptorTypeNop` = (kSDHC\_Adma2DescriptorValidFlag),  
`kSDHC_Adma2DescriptorTypeReserved`,  
`kSDHC_Adma2DescriptorTypeTransfer`,  
`kSDHC_Adma2DescriptorTypeLink` }

*ADMA1 descriptor control and status mask.*

## Driver version

- #define `FSL_SDHC_DRIVER_VERSION` (MAKE\_VERSION(2U, 1U, 1U))

*Driver version 2.1.1.*

## Typical use case

### Initialization and deinitialization

- void [SDHC\\_Init](#) (SDHC\_Type \*base, const [sdhc\\_config\\_t](#) \*config)  
*SDHC module initialization function.*
- void [SDHC\\_Deinit](#) (SDHC\_Type \*base)  
*Deinitializes the SDHC.*
- bool [SDHC\\_Reset](#) (SDHC\_Type \*base, uint32\_t mask, uint32\_t timeout)  
*Resets the SDHC.*

### DMA Control

- status\_t [SDHC\\_SetAdmaTableConfig](#) (SDHC\_Type \*base, [sdhc\\_dma\\_mode\\_t](#) dmaMode, uint32\_t \*table, uint32\_t tableWords, const uint32\_t \*data, uint32\_t dataBytes)  
*Sets the ADMA descriptor table configuration.*

### Interrupts

- static void [SDHC\\_EnableInterruptStatus](#) (SDHC\_Type \*base, uint32\_t mask)  
*Enables the interrupt status.*
- static void [SDHC\\_DisableInterruptStatus](#) (SDHC\_Type \*base, uint32\_t mask)  
*Disables the interrupt status.*
- static void [SDHC\\_EnableInterruptSignal](#) (SDHC\_Type \*base, uint32\_t mask)  
*Enables the interrupt signal corresponding to the interrupt status flag.*
- static void [SDHC\\_DisableInterruptSignal](#) (SDHC\_Type \*base, uint32\_t mask)  
*Disables the interrupt signal corresponding to the interrupt status flag.*

### Status

- static uint32\_t [SDHC\\_GetInterruptStatusFlags](#) (SDHC\_Type \*base)  
*Gets the current interrupt status.*
- static void [SDHC\\_ClearInterruptStatusFlags](#) (SDHC\_Type \*base, uint32\_t mask)  
*Clears a specified interrupt status.*
- static uint32\_t [SDHC\\_GetAutoCommand12ErrorStatusFlags](#) (SDHC\_Type \*base)  
*Gets the status of auto command 12 error.*
- static uint32\_t [SDHC\\_GetAdmaErrorStatusFlags](#) (SDHC\_Type \*base)  
*Gets the status of the ADMA error.*
- static uint32\_t [SDHC\\_GetPresentStatusFlags](#) (SDHC\_Type \*base)  
*Gets a present status.*

### Bus Operations

- void [SDHC\\_GetCapability](#) (SDHC\_Type \*base, [sdhc\\_capability\\_t](#) \*capability)  
*Gets the capability information.*
- static void [SDHC\\_EnableSdClock](#) (SDHC\_Type \*base, bool enable)  
*Enables or disables the SD bus clock.*
- uint32\_t [SDHC\\_SetSdClock](#) (SDHC\_Type \*base, uint32\_t srcClock\_Hz, uint32\_t busClock\_Hz)  
*Sets the SD bus clock frequency.*
- bool [SDHC\\_SetCardActive](#) (SDHC\_Type \*base, uint32\_t timeout)  
*Sends 80 clocks to the card to set it to the active state.*
- static void [SDHC\\_SetDataBusWidth](#) (SDHC\_Type \*base, [sdhc\\_data\\_bus\\_width\\_t](#) width)  
*Sets the data transfer width.*

- void [SDHC\\_SetTransferConfig](#) (SDHC\_Type \*base, const [sdhc\\_transfer\\_config\\_t](#) \*config)  
*Sets the card transfer-related configuration.*
- static uint32\_t [SDHC\\_GetCommandResponse](#) (SDHC\_Type \*base, uint32\_t index)  
*Gets the command response.*
- static void [SDHC\\_WriteData](#) (SDHC\_Type \*base, uint32\_t data)  
*Fills the the data port.*
- static uint32\_t [SDHC\\_ReadData](#) (SDHC\_Type \*base)  
*Retrieves the data from the data port.*
- static void [SDHC\\_EnableWakeupEvent](#) (SDHC\_Type \*base, uint32\_t mask, bool enable)  
*Enables or disables a wakeup event in low-power mode.*
- static void [SDHC\\_EnableCardDetectTest](#) (SDHC\_Type \*base, bool enable)  
*Enables or disables the card detection level for testing.*
- static void [SDHC\\_SetCardDetectTestLevel](#) (SDHC\_Type \*base, bool high)  
*Sets the card detection test level.*
- void [SDHC\\_EnableSdioControl](#) (SDHC\_Type \*base, uint32\_t mask, bool enable)  
*Enables or disables the SDIO card control.*
- static void [SDHC\\_SetContinueRequest](#) (SDHC\_Type \*base)  
*Restarts a transaction which has stopped at the block GAP for the SDIO card.*
- void [SDHC\\_SetMmcBootConfig](#) (SDHC\_Type \*base, const [sdhc\\_boot\\_config\\_t](#) \*config)  
*Configures the MMC boot feature.*
- static void [SDHC\\_SetForceEvent](#) (SDHC\_Type \*base, uint32\_t mask)  
*Forces generating events according to the given mask.*

## Transactional

- status\_t [SDHC\\_TransferBlocking](#) (SDHC\_Type \*base, uint32\_t \*admaTable, uint32\_t admaTableWords, [sdhc\\_transfer\\_t](#) \*transfer)  
*Transfers the command/data using a blocking method.*
- void [SDHC\\_TransferCreateHandle](#) (SDHC\_Type \*base, sdhc\_handle\_t \*handle, const [sdhc\\_transfer\\_callback\\_t](#) \*callback, void \*userData)  
*Creates the SDHC handle.*
- status\_t [SDHC\\_TransferNonBlocking](#) (SDHC\_Type \*base, sdhc\_handle\_t \*handle, uint32\_t \*admaTable, uint32\_t admaTableWords, [sdhc\\_transfer\\_t](#) \*transfer)  
*Transfers the command/data using an interrupt and an asynchronous method.*
- void [SDHC\\_TransferHandleIRQ](#) (SDHC\_Type \*base, sdhc\_handle\_t \*handle)  
*IRQ handler for the SDHC.*

## 34.3 Data Structure Documentation

### 34.3.1 struct sdhc\_adma2\_descriptor\_t

#### Data Fields

- uint32\_t [attribute](#)  
*The control and status field.*
- const uint32\_t \* [address](#)  
*The address field.*



### 34.3.2 struct sdhc\_capability\_t

Defines a structure to save the capability information of SDHC.

#### Data Fields

- uint32\_t [specVersion](#)  
*Specification version.*
- uint32\_t [vendorVersion](#)  
*Vendor version.*
- uint32\_t [maxBlockLength](#)  
*Maximum block length united as byte.*
- uint32\_t [maxBlockCount](#)  
*Maximum block count can be set one time.*
- uint32\_t [flags](#)  
*Capability flags to indicate the support information(\_sdhc\_capability\_flag)*

### 34.3.3 struct sdhc\_transfer\_config\_t

Define structure to configure the transfer-related command index/argument/flags and data block size/data block numbers. This structure needs to be filled each time a command is sent to the card.

#### Data Fields

- size\_t [dataBlockSize](#)  
*Data block size.*
- uint32\_t [dataBlockCount](#)  
*Data block count.*
- uint32\_t [commandArgument](#)  
*Command argument.*
- uint32\_t [commandIndex](#)  
*Command index.*
- uint32\_t [flags](#)  
*Transfer flags(\_sdhc\_transfer\_flag)*

### 34.3.4 struct sdhc\_boot\_config\_t

#### Data Fields

- uint32\_t [ackTimeoutCount](#)  
*Timeout value for the boot ACK.*
- [sdhc\\_boot\\_mode\\_t](#) [bootMode](#)  
*Boot mode selection.*
- uint32\_t [blockCount](#)



- *Stop at block gap value of automatic mode.*
- bool [enableBootAck](#)  
*Enable or disable boot ACK.*
- bool [enableBoot](#)  
*Enable or disable fast boot.*
- bool [enableAutoStopAtBlockGap](#)  
*Enable or disable auto stop at block gap function in boot period.*

#### 34.3.4.0.0.85 Field Documentation

##### 34.3.4.0.0.85.1 uint32\_t sdhc\_boot\_config\_t::ackTimeoutCount

The available range is 0 ~ 15.

##### 34.3.4.0.0.85.2 sdhc\_boot\_mode\_t sdhc\_boot\_config\_t::bootMode

##### 34.3.4.0.0.85.3 uint32\_t sdhc\_boot\_config\_t::blockCount

Available range is 0 ~ 65535.

### 34.3.5 struct sdhc\_config\_t

#### Data Fields

- bool [cardDetectDat3](#)  
*Enable DAT3 as card detection pin.*
- [sdhc\\_endian\\_mode\\_t](#) [endianMode](#)  
*Endian mode.*
- [sdhc\\_dma\\_mode\\_t](#) [dmaMode](#)  
*DMA mode.*
- uint32\_t [readWatermarkLevel](#)  
*Watermark level for DMA read operation.*
- uint32\_t [writeWatermarkLevel](#)  
*Watermark level for DMA write operation.*

#### 34.3.5.0.0.86 Field Documentation

##### 34.3.5.0.0.86.1 uint32\_t sdhc\_config\_t::readWatermarkLevel

Available range is 1 ~ 128.

##### 34.3.5.0.0.86.2 uint32\_t sdhc\_config\_t::writeWatermarkLevel

Available range is 1 ~ 128.

### 34.3.6 struct sdhc\_data\_t

Defines a structure to contain data-related attribute. 'enableIgnoreError' is used for the case that upper card driver want to ignore the error event to read/write all the data not to stop read/write immediately when error event happen for example bus testing procedure for MMC card.

#### Data Fields

- bool [enableAutoCommand12](#)  
*Enable auto CMD12.*
- bool [enableIgnoreError](#)  
*Enable to ignore error event to read/write all the data.*
- size\_t [blockSize](#)  
*Block size.*
- uint32\_t [blockCount](#)  
*Block count.*
- uint32\_t \* [rxData](#)  
*Buffer to save data read.*
- const uint32\_t \* [txData](#)  
*Data buffer to write.*

### 34.3.7 struct sdhc\_command\_t

Define card command-related attribute.

#### Data Fields

- uint32\_t [index](#)  
*Command index.*
- uint32\_t [argument](#)  
*Command argument.*
- [sdhc\\_command\\_type\\_t](#) type  
*Command type.*
- [sdhc\\_response\\_type\\_t](#) responseType  
*Command response type.*
- uint32\_t [response](#) [4U]  
*Response for this command.*

### 34.3.8 struct sdhc\_transfer\_t

#### Data Fields

- [sdhc\\_data\\_t](#) \* data  
*Data to transfer.*

- `sdhc_command_t * command`  
*Command to send.*

### 34.3.9 struct sdhc\_transfer\_callback\_t

#### Data Fields

- `void(* CardInserted )(void)`  
*Card inserted occurs when DAT3/CD pin is for card detect.*
- `void(* CardRemoved )(void)`  
*Card removed occurs.*
- `void(* SdioInterrupt )(void)`  
*SDIO card interrupt occurs.*
- `void(* SdioBlockGap )(void)`  
*SDIO card stopped at block gap occurs.*
- `void(* TransferComplete )(SDHC_Type *base, sdhc_handle_t *handle, status_t status, void *user-Data)`  
*Transfer complete callback.*

### 34.3.10 struct \_sdhc\_handle

SDHC handle typedef.

Defines the structure to save the SDHC state information and callback function. The detailed interrupt status when sending a command or transferring data can be obtained from the interruptFlags field by using the mask defined in `sdhc_interrupt_flag_t`.

Note

All the fields except interruptFlags and transferredWords must be allocated by the user.

#### Data Fields

- `sdhc_data_t *volatile data`  
*Data to transfer.*
- `sdhc_command_t *volatile command`  
*Command to send.*
- `volatile uint32_t interruptFlags`  
*Interrupt flags of last transaction.*
- `volatile uint32_t transferredWords`  
*Words transferred by DATAPORT way.*
- `sdhc_transfer_callback_t callback`  
*Callback function.*
- `void * userData`  
*Parameter for transfer complete callback.*

## Enumeration Type Documentation

### 34.3.11 struct sdhc\_host\_t

#### Data Fields

- SDHC\_Type \* [base](#)  
*SDHC peripheral base address.*
- uint32\_t [sourceClock\\_Hz](#)  
*SDHC source clock frequency united in Hz.*
- [sdhc\\_config\\_t](#) [config](#)  
*SDHC configuration.*
- [sdhc\\_capability\\_t](#) [capability](#)  
*SDHC capability information.*
- [sdhc\\_transfer\\_function\\_t](#) [transfer](#)  
*SDHC transfer function.*

## 34.4 Macro Definition Documentation

### 34.4.1 #define FSL\_SDHC\_DRIVER\_VERSION (MAKE\_VERSION(2U, 1U, 1U))

## 34.5 Typedef Documentation

### 34.5.1 typedef uint32\_t sdhc\_adma1\_descriptor\_t

### 34.5.2 typedef status\_t(\* sdhc\_transfer\_function\_t)(SDHC\_Type \*base, sdhc\_transfer\_t \*content)

## 34.6 Enumeration Type Documentation

### 34.6.1 enum \_sdhc\_status

#### Enumerator

*kStatus\_SDHC\_BusyTransferring* Transfer is on-going.  
*kStatus\_SDHC\_PrepareAdmaDescriptorFailed* Set DMA descriptor failed.  
*kStatus\_SDHC\_SendCommandFailed* Send command failed.  
*kStatus\_SDHC\_TransferDataFailed* Transfer data failed.

### 34.6.2 enum \_sdhc\_capability\_flag

#### Enumerator

*kSDHC\_SupportAdmaFlag* Support ADMA.  
*kSDHC\_SupportHighSpeedFlag* Support high-speed.  
*kSDHC\_SupportDmaFlag* Support DMA.  
*kSDHC\_SupportSuspendResumeFlag* Support suspend/resume.

***kSDHC\_SupportV330Flag*** Support voltage 3.3V.

***kSDHC\_Support4BitFlag*** Support 4 bit mode.

***kSDHC\_Support8BitFlag*** Support 8 bit mode.

### 34.6.3 enum \_sdhc\_wakeup\_event

Enumerator

***kSDHC\_WakeupEventOnCardInt*** Wakeup on card interrupt.

***kSDHC\_WakeupEventOnCardInsert*** Wakeup on card insertion.

***kSDHC\_WakeupEventOnCardRemove*** Wakeup on card removal.

***kSDHC\_WakeupEventsAll*** All wakeup events.

### 34.6.4 enum \_sdhc\_reset

Enumerator

***kSDHC\_ResetAll*** Reset all except card detection.

***kSDHC\_ResetCommand*** Reset command line.

***kSDHC\_ResetData*** Reset data line.

***kSDHC\_ResetsAll*** All reset types.

### 34.6.5 enum \_sdhc\_transfer\_flag

Enumerator

***kSDHC\_EnableDmaFlag*** Enable DMA.

***kSDHC\_CommandTypeSuspendFlag*** Suspend command.

***kSDHC\_CommandTypeResumeFlag*** Resume command.

***kSDHC\_CommandTypeAbortFlag*** Abort command.

***kSDHC\_EnableBlockCountFlag*** Enable block count.

***kSDHC\_EnableAutoCommand12Flag*** Enable auto CMD12.

***kSDHC\_DataReadFlag*** Enable data read.

***kSDHC\_MultipleBlockFlag*** Multiple block data read/write.

***kSDHC\_ResponseLength136Flag*** 136 bit response length

***kSDHC\_ResponseLength48Flag*** 48 bit response length

***kSDHC\_ResponseLength48BusyFlag*** 48 bit response length with busy status

***kSDHC\_EnableCrcCheckFlag*** Enable CRC check.

***kSDHC\_EnableIndexCheckFlag*** Enable index check.

***kSDHC\_DataPresentFlag*** Data present flag.

### 34.6.6 enum \_sdhc\_present\_status\_flag

Enumerator

*kSDHC\_CommandInhibitFlag* Command inhibit.  
*kSDHC\_DataInhibitFlag* Data inhibit.  
*kSDHC\_DataLineActiveFlag* Data line active.  
*kSDHC\_SdClockStableFlag* SD bus clock stable.  
*kSDHC\_WriteTransferActiveFlag* Write transfer active.  
*kSDHC\_ReadTransferActiveFlag* Read transfer active.  
*kSDHC\_BufferWriteEnableFlag* Buffer write enable.  
*kSDHC\_BufferReadEnableFlag* Buffer read enable.  
*kSDHC\_CardInsertedFlag* Card inserted.  
*kSDHC\_CommandLineLevelFlag* Command line signal level.  
*kSDHC\_Data0LineLevelFlag* Data0 line signal level.  
*kSDHC\_Data1LineLevelFlag* Data1 line signal level.  
*kSDHC\_Data2LineLevelFlag* Data2 line signal level.  
*kSDHC\_Data3LineLevelFlag* Data3 line signal level.  
*kSDHC\_Data4LineLevelFlag* Data4 line signal level.  
*kSDHC\_Data5LineLevelFlag* Data5 line signal level.  
*kSDHC\_Data6LineLevelFlag* Data6 line signal level.  
*kSDHC\_Data7LineLevelFlag* Data7 line signal level.

### 34.6.7 enum \_sdhc\_interrupt\_status\_flag

Enumerator

*kSDHC\_CommandCompleteFlag* Command complete.  
*kSDHC\_DataCompleteFlag* Data complete.  
*kSDHC\_BlockGapEventFlag* Block gap event.  
*kSDHC\_DmaCompleteFlag* DMA interrupt.  
*kSDHC\_BufferWriteReadyFlag* Buffer write ready.  
*kSDHC\_BufferReadReadyFlag* Buffer read ready.  
*kSDHC\_CardInsertionFlag* Card inserted.  
*kSDHC\_CardRemovalFlag* Card removed.  
*kSDHC\_CardInterruptFlag* Card interrupt.  
*kSDHC\_CommandTimeoutFlag* Command timeout error.  
*kSDHC\_CommandCrcErrorFlag* Command CRC error.  
*kSDHC\_CommandEndBitErrorFlag* Command end bit error.  
*kSDHC\_CommandIndexErrorFlag* Command index error.  
*kSDHC\_DataTimeoutFlag* Data timeout error.  
*kSDHC\_DataCrcErrorFlag* Data CRC error.  
*kSDHC\_DataEndBitErrorFlag* Data end bit error.  
*kSDHC\_AutoCommand12ErrorFlag* Auto CMD12 error.

***kSDHC\_DmaErrorFlag*** DMA error.  
***kSDHC\_CommandErrorFlag*** Command error.  
***kSDHC\_DataErrorFlag*** Data error.  
***kSDHC\_ErrorFlag*** All error.  
***kSDHC\_DataFlag*** Data interrupts.  
***kSDHC\_CommandFlag*** Command interrupts.  
***kSDHC\_CardDetectFlag*** Card detection interrupts.  
***kSDHC\_AllInterruptFlags*** All flags mask.

### 34.6.8 enum \_sdhc\_auto\_command12\_error\_status\_flag

Enumerator

***kSDHC\_AutoCommand12NotExecutedFlag*** Not executed error.  
***kSDHC\_AutoCommand12TimeoutFlag*** Timeout error.  
***kSDHC\_AutoCommand12EndBitErrorFlag*** End bit error.  
***kSDHC\_AutoCommand12CrcErrorFlag*** CRC error.  
***kSDHC\_AutoCommand12IndexErrorFlag*** Index error.  
***kSDHC\_AutoCommand12NotIssuedFlag*** Not issued error.

### 34.6.9 enum \_sdhc\_adma\_error\_status\_flag

Enumerator

***kSDHC\_AdmaLenghMismatchFlag*** Length mismatch error.  
***kSDHC\_AdmaDescriptorErrorFlag*** Descriptor error.

### 34.6.10 enum sdhc\_adma\_error\_state\_t

This state is the detail state when ADMA error has occurred.

Enumerator

***kSDHC\_AdmaErrorStateStopDma*** Stop DMA.  
***kSDHC\_AdmaErrorStateFetchDescriptor*** Fetch descriptor.  
***kSDHC\_AdmaErrorStateChangeAddress*** Change address.  
***kSDHC\_AdmaErrorStateTransferData*** Transfer data.

### 34.6.11 enum \_sdhc\_force\_event

Enumerator

*kSDHC\_ForceEventAutoCommand12NotExecuted* Auto CMD12 not executed error.  
*kSDHC\_ForceEventAutoCommand12Timeout* Auto CMD12 timeout error.  
*kSDHC\_ForceEventAutoCommand12CrcError* Auto CMD12 CRC error.  
*kSDHC\_ForceEventEndBitError* Auto CMD12 end bit error.  
*kSDHC\_ForceEventAutoCommand12IndexError* Auto CMD12 index error.  
*kSDHC\_ForceEventAutoCommand12NotIssued* Auto CMD12 not issued error.  
*kSDHC\_ForceEventCommandTimeout* Command timeout error.  
*kSDHC\_ForceEventCommandCrcError* Command CRC error.  
*kSDHC\_ForceEventCommandEndBitError* Command end bit error.  
*kSDHC\_ForceEventCommandIndexError* Command index error.  
*kSDHC\_ForceEventDataTimeout* Data timeout error.  
*kSDHC\_ForceEventDataCrcError* Data CRC error.  
*kSDHC\_ForceEventDataEndBitError* Data end bit error.  
*kSDHC\_ForceEventAutoCommand12Error* Auto CMD12 error.  
*kSDHC\_ForceEventCardInt* Card interrupt.  
*kSDHC\_ForceEventDmaError* Dma error.  
*kSDHC\_ForceEventsAll* All force event flags mask.

### 34.6.12 enum sdhc\_data\_bus\_width\_t

Enumerator

*kSDHC\_DataBusWidth1Bit* 1-bit mode  
*kSDHC\_DataBusWidth4Bit* 4-bit mode  
*kSDHC\_DataBusWidth8Bit* 8-bit mode

### 34.6.13 enum sdhc\_endian\_mode\_t

Enumerator

*kSDHC\_EndianModeBig* Big endian mode.  
*kSDHC\_EndianModeHalfWordBig* Half word big endian mode.  
*kSDHC\_EndianModeLittle* Little endian mode.

### 34.6.14 enum sdhc\_dma\_mode\_t

Enumerator

*kSDHC\_DmaModeNo* No DMA.



*kSDHC\_DmaModeAdma1* ADMA1 is selected.

*kSDHC\_DmaModeAdma2* ADMA2 is selected.

### 34.6.15 enum \_sdhc\_sdio\_control\_flag

Enumerator

*kSDHC\_StopAtBlockGapFlag* Stop at block gap.

*kSDHC\_ReadWaitControlFlag* Read wait control.

*kSDHC\_InterruptAtBlockGapFlag* Interrupt at block gap.

*kSDHC\_ExactBlockNumberReadFlag* Exact block number read.

### 34.6.16 enum sdhc\_boot\_mode\_t

Enumerator

*kSDHC\_BootModeNormal* Normal boot.

*kSDHC\_BootModeAlternative* Alternative boot.

### 34.6.17 enum sdhc\_command\_type\_t

Enumerator

*kSDHC\_CommandTypeNormal* Normal command.

*kSDHC\_CommandTypeSuspend* Suspend command.

*kSDHC\_CommandTypeResume* Resume command.

*kSDHC\_CommandTypeAbort* Abort command.

### 34.6.18 enum sdhc\_response\_type\_t

Define the command response type from card to host controller.

Enumerator

*kSDHC\_ResponseTypeNone* Response type: none.

*kSDHC\_ResponseTypeR1* Response type: R1.

*kSDHC\_ResponseTypeR1b* Response type: R1b.

*kSDHC\_ResponseTypeR2* Response type: R2.

*kSDHC\_ResponseTypeR3* Response type: R3.

*kSDHC\_ResponseTypeR4* Response type: R4.

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*kSDHC\_ResponseTypeR5* Response type: R5.  
*kSDHC\_ResponseTypeR5b* Response type: R5b.  
*kSDHC\_ResponseTypeR6* Response type: R6.  
*kSDHC\_ResponseTypeR7* Response type: R7.

### 34.6.19 enum \_sdhc\_adma1\_descriptor\_flag

Enumerator

*kSDHC\_Adma1DescriptorValidFlag* Valid flag.  
*kSDHC\_Adma1DescriptorEndFlag* End flag.  
*kSDHC\_Adma1DescriptorInterruptFlag* Interrupt flag.  
*kSDHC\_Adma1DescriptorActivity1Flag* Activity 1 flag.  
*kSDHC\_Adma1DescriptorActivity2Flag* Activity 2 flag.  
*kSDHC\_Adma1DescriptorTypeNop* No operation.  
*kSDHC\_Adma1DescriptorTypeTransfer* Transfer data.  
*kSDHC\_Adma1DescriptorTypeLink* Link descriptor.  
*kSDHC\_Adma1DescriptorTypeSetLength* Set data length.

### 34.6.20 enum \_sdhc\_adma2\_descriptor\_flag

Enumerator

*kSDHC\_Adma2DescriptorValidFlag* Valid flag.  
*kSDHC\_Adma2DescriptorEndFlag* End flag.  
*kSDHC\_Adma2DescriptorInterruptFlag* Interrupt flag.  
*kSDHC\_Adma2DescriptorActivity1Flag* Activity 1 mask.  
*kSDHC\_Adma2DescriptorActivity2Flag* Activity 2 mask.  
*kSDHC\_Adma2DescriptorTypeNop* No operation.  
*kSDHC\_Adma2DescriptorTypeReserved* Reserved.  
*kSDHC\_Adma2DescriptorTypeTransfer* Transfer type.  
*kSDHC\_Adma2DescriptorTypeLink* Link type.

## 34.7 Function Documentation

### 34.7.1 void SDHC\_Init ( SDHC\_Type \* *base*, const sdhc\_config\_t \* *config* )

Configures the SDHC according to the user configuration.

Example:

```
sdhc_config_t config;  
config.cardDetectDat3 = false;  
config.endianMode = kSDHC_EndianModeLittle;
```

```

config.dmaMode = kSDHC_DmaModeAdma2;
config.readWatermarkLevel = 128U;
config.writeWatermarkLevel = 128U;
SDHC_Init(SDHC, &config);

```

## Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | SDHC peripheral base address.   |
| <i>config</i> | SDHC configuration information. |

## Return values

|                        |                       |
|------------------------|-----------------------|
| <i>kStatus_Success</i> | Operate successfully. |
|------------------------|-----------------------|

### 34.7.2 void SDHC\_Deinit ( SDHC\_Type \* *base* )

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
|-------------|-------------------------------|

### 34.7.3 bool SDHC\_Reset ( SDHC\_Type \* *base*, uint32\_t *mask*, uint32\_t *timeout* )

## Parameters

|                |                                   |
|----------------|-----------------------------------|
| <i>base</i>    | SDHC peripheral base address.     |
| <i>mask</i>    | The reset type mask(_sdhc_reset). |
| <i>timeout</i> | Timeout for reset.                |

## Return values

|              |                     |
|--------------|---------------------|
| <i>true</i>  | Reset successfully. |
| <i>false</i> | Reset failed.       |

### 34.7.4 status\_t SDHC\_SetAdmaTableConfig ( SDHC\_Type \* *base*, sdhc\_dma\_mode\_t *dmaMode*, uint32\_t \* *table*, uint32\_t *tableWords*, const uint32\_t \* *data*, uint32\_t *dataBytes* )

## Function Documentation

### Parameters

|                   |                                           |
|-------------------|-------------------------------------------|
| <i>base</i>       | SDHC peripheral base address.             |
| <i>dmaMode</i>    | DMA mode.                                 |
| <i>table</i>      | ADMA table address.                       |
| <i>tableWords</i> | ADMA table buffer length united as Words. |
| <i>data</i>       | Data buffer address.                      |
| <i>dataBytes</i>  | Data length united as bytes.              |

### Return values

|                           |                                                             |
|---------------------------|-------------------------------------------------------------|
| <i>kStatus_OutOfRange</i> | ADMA descriptor table length isn't enough to describe data. |
| <i>kStatus_Success</i>    | Operate successfully.                                       |

### 34.7.5 static void SDHC\_EnableInterruptStatus ( SDHC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

#### Parameters

|             |                                                           |
|-------------|-----------------------------------------------------------|
| <i>base</i> | SDHC peripheral base address.                             |
| <i>mask</i> | Interrupt status flags mask(_sdhc_interrupt_status_flag). |

### 34.7.6 static void SDHC\_DisableInterruptStatus ( SDHC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

#### Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>base</i> | SDHC peripheral base address.                                 |
| <i>mask</i> | The interrupt status flags mask(_sdhc_interrupt_status_flag). |

### 34.7.7 static void SDHC\_EnableInterruptSignal ( SDHC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

## Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>base</i> | SDHC peripheral base address.                                 |
| <i>mask</i> | The interrupt status flags mask(_sdhc_interrupt_status_flag). |

**34.7.8 static void SDHC\_DisableInterruptSignal ( SDHC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

## Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>base</i> | SDHC peripheral base address.                                 |
| <i>mask</i> | The interrupt status flags mask(_sdhc_interrupt_status_flag). |

**34.7.9 static uint32\_t SDHC\_GetInterruptStatusFlags ( SDHC\_Type \* *base* ) [inline], [static]**

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
|-------------|-------------------------------|

## Returns

Current interrupt status flags mask(\_sdhc\_interrupt\_status\_flag).

**34.7.10 static void SDHC\_ClearInterruptStatusFlags ( SDHC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

## Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>base</i> | SDHC peripheral base address.                                 |
| <i>mask</i> | The interrupt status flags mask(_sdhc_interrupt_status_flag). |

**34.7.11 static uint32\_t SDHC\_GetAutoCommand12ErrorStatusFlags ( SDHC\_Type \* *base* ) [inline], [static]**

## Function Documentation

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
|-------------|-------------------------------|

### Returns

Auto command 12 error status flags mask(\_sdhc\_auto\_command12\_error\_status\_flag).

**34.7.12 static uint32\_t SDHC\_GetAdmaErrorStatusFlags ( SDHC\_Type \* *base* )  
[inline], [static]**

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
|-------------|-------------------------------|

### Returns

ADMA error status flags mask(\_sdhc\_adma\_error\_status\_flag).

**34.7.13 static uint32\_t SDHC\_GetPresentStatusFlags ( SDHC\_Type \* *base* )  
[inline], [static]**

This function gets the present SDHC's status except for an interrupt status and an error status.

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
|-------------|-------------------------------|

### Returns

Present SDHC's status flags mask(\_sdhc\_present\_status\_flag).

**34.7.14 void SDHC\_GetCapability ( SDHC\_Type \* *base*, sdhc\_capability\_t \*  
*capability* )**

## Parameters

|                   |                                           |
|-------------------|-------------------------------------------|
| <i>base</i>       | SDHC peripheral base address.             |
| <i>capability</i> | Structure to save capability information. |

### 34.7.15 static void SDHC\_EnableSdClock ( SDHC\_Type \* *base*, bool *enable* ) [inline], [static]

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | SDHC peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

### 34.7.16 uint32\_t SDHC\_SetSdClock ( SDHC\_Type \* *base*, uint32\_t *srcClock\_Hz*, uint32\_t *busClock\_Hz* )

## Parameters

|                    |                                           |
|--------------------|-------------------------------------------|
| <i>base</i>        | SDHC peripheral base address.             |
| <i>srcClock_Hz</i> | SDHC source clock frequency united in Hz. |
| <i>busClock_Hz</i> | SD bus clock frequency united in Hz.      |

## Returns

The nearest frequency of *busClock\_Hz* configured to SD bus.

### 34.7.17 bool SDHC\_SetCardActive ( SDHC\_Type \* *base*, uint32\_t *timeout* )

This function must be called each time the card is inserted to ensure that the card can receive the command correctly.

## Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | SDHC peripheral base address. |
| <i>timeout</i> | Timeout to initialize card.   |

## Function Documentation

Return values

|              |                               |
|--------------|-------------------------------|
| <i>true</i>  | Set card active successfully. |
| <i>false</i> | Set card active failed.       |

### 34.7.18 static void SDHC\_SetDataBusWidth ( SDHC\_Type \* *base*, sdhc\_data\_bus\_width\_t *width* ) [inline], [static]

Parameters

|              |                               |
|--------------|-------------------------------|
| <i>base</i>  | SDHC peripheral base address. |
| <i>width</i> | Data transfer width.          |

### 34.7.19 void SDHC\_SetTransferConfig ( SDHC\_Type \* *base*, const sdhc\_transfer\_config\_t \* *config* )

This function fills the card transfer-related command argument/transfer flag/data size. The command and data are sent by SDHC after calling this function.

Example:

```
sdhc_transfer_config_t transferConfig;  
transferConfig.dataBlockSize = 512U;  
transferConfig.dataBlockCount = 2U;  
transferConfig.commandArgument = 0x01AAU;  
transferConfig.commandIndex = 8U;  
transferConfig.flags |= (kSDHC_EnableDmaFlag |  
    kSDHC_EnableAutoCommand12Flag |  
    kSDHC_MultipleBlockFlag);  
SDHC_SetTransferConfig(SDHC, &transferConfig);
```

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | SDHC peripheral base address.    |
| <i>config</i> | Command configuration structure. |

### 34.7.20 static uint32\_t SDHC\_GetCommandResponse ( SDHC\_Type \* *base*, uint32\_t *index* ) [inline], [static]



## Parameters

|              |                                                    |
|--------------|----------------------------------------------------|
| <i>base</i>  | SDHC peripheral base address.                      |
| <i>index</i> | The index of response register, range from 0 to 3. |

## Returns

Response register transfer.

### 34.7.21 static void SDHC\_WriteData ( SDHC\_Type \* *base*, uint32\_t *data* ) [inline], [static]

This function is used to implement the data transfer by Data Port instead of DMA.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
| <i>data</i> | The data about to be sent.    |

### 34.7.22 static uint32\_t SDHC\_ReadData ( SDHC\_Type \* *base* ) [inline], [static]

This function is used to implement the data transfer by Data Port instead of DMA.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
|-------------|-------------------------------|

## Returns

The data has been read.

### 34.7.23 static void SDHC\_EnableWakeupEvent ( SDHC\_Type \* *base*, uint32\_t *mask*, bool *enable* ) [inline], [static]

## Function Documentation

### Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | SDHC peripheral base address.           |
| <i>mask</i>   | Wakeup events mask(_sdhc_wakeup_event). |
| <i>enable</i> | True to enable, false to disable.       |

**34.7.24 static void SDHC\_EnableCardDetectTest ( SDHC\_Type \* *base*, bool *enable* ) [inline], [static]**

### Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | SDHC peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

**34.7.25 static void SDHC\_SetCardDetectTestLevel ( SDHC\_Type \* *base*, bool *high* ) [inline], [static]**

This function sets the card detection test level to indicate whether the card is inserted into the SDHC when DAT[3]/ CD pin is selected as a card detection pin. This function can also assert the pin logic when DAT[3]/CD pin is selected as the card detection pin.

### Parameters

|             |                                            |
|-------------|--------------------------------------------|
| <i>base</i> | SDHC peripheral base address.              |
| <i>high</i> | True to set the card detect level to high. |

**34.7.26 void SDHC\_EnableSdioControl ( SDHC\_Type \* *base*, uint32\_t *mask*, bool *enable* )**

### Parameters

|               |                                                        |
|---------------|--------------------------------------------------------|
| <i>base</i>   | SDHC peripheral base address.                          |
| <i>mask</i>   | SDIO card control flags mask(_sdhc_sdio_control_flag). |
| <i>enable</i> | True to enable, false to disable.                      |

**34.7.27** `static void SDHC_SetContinueRequest ( SDHC_Type * base ) [inline],  
[static]`

## Function Documentation

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | SDHC peripheral base address. |
|-------------|-------------------------------|

### 34.7.28 void SDHC\_SetMmcBootConfig ( SDHC\_Type \* *base*, const sdhc\_boot\_config\_t \* *config* )

#### Example:

```
sdhc_boot_config_t config;
config.ackTimeoutCount = 4;
config.bootMode = kSDHC_BootModeNormal;
config.blockCount = 5;
config.enableBootAck = true;
config.enableBoot = true;
config.enableAutoStopAtBlockGap = true;
SDHC_SetMmcBootConfig(SDHC, &config);
```

### Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | SDHC peripheral base address.           |
| <i>config</i> | The MMC boot configuration information. |

### 34.7.29 static void SDHC\_SetForceEvent ( SDHC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

### Parameters

|             |                                           |
|-------------|-------------------------------------------|
| <i>base</i> | SDHC peripheral base address.             |
| <i>mask</i> | The force events mask(_sdhc_force_event). |

### 34.7.30 status\_t SDHC\_TransferBlocking ( SDHC\_Type \* *base*, uint32\_t \* *admaTable*, uint32\_t *admaTableWords*, sdhc\_transfer\_t \* *transfer* )

This function waits until the command response/data is received or the SDHC encounters an error by polling the status flag. The application must not call this API in multiple threads at the same time. Because of that this API doesn't support the re-entry mechanism.

#### Note

There is no need to call the API 'SDHC\_TransferCreateHandle' when calling this API.

## Parameters

|                       |                                                                               |
|-----------------------|-------------------------------------------------------------------------------|
| <i>base</i>           | SDHC peripheral base address.                                                 |
| <i>admaTable</i>      | ADMA table address, can't be null if transfer way is ADMA1/ADMA2.             |
| <i>admaTableWords</i> | ADMA table length united as words, can't be 0 if transfer way is ADMA1/ADMA2. |
| <i>transfer</i>       | Transfer content.                                                             |

## Return values

|                                                  |                                 |
|--------------------------------------------------|---------------------------------|
| <i>kStatus_InvalidArgument</i>                   | Argument is invalid.            |
| <i>kStatus_SDHC_Prepare-AdmaDescriptorFailed</i> | Prepare ADMA descriptor failed. |
| <i>kStatus_SDHC_Send-CommandFailed</i>           | Send command failed.            |
| <i>kStatus_SDHC_Transfer-DataFailed</i>          | Transfer data failed.           |
| <i>kStatus_Success</i>                           | Operate successfully.           |

**34.7.31 void SDHC\_TransferCreateHandle ( SDHC\_Type \* *base*, sdhc\_handle\_t \* *handle*, const sdhc\_transfer\_callback\_t \* *callback*, void \* *userData* )**

## Parameters

|                 |                                                      |
|-----------------|------------------------------------------------------|
| <i>base</i>     | SDHC peripheral base address.                        |
| <i>handle</i>   | SDHC handle pointer.                                 |
| <i>callback</i> | Structure pointer to contain all callback functions. |
| <i>userData</i> | Callback function parameter.                         |

**34.7.32 status\_t SDHC\_TransferNonBlocking ( SDHC\_Type \* *base*, sdhc\_handle\_t \* *handle*, uint32\_t \* *admaTable*, uint32\_t *admaTableWords*, sdhc\_transfer\_t \* *transfer* )**

This function sends a command and data and returns immediately. It doesn't wait the transfer complete or encounter an error. The application must not call this API in multiple threads at the same time. Because of that this API doesn't support the re-entry mechanism.

## Function Documentation

### Note

Call the API 'SDHC\_TransferCreateHandle' when calling this API.

### Parameters

|                             |                                                                               |
|-----------------------------|-------------------------------------------------------------------------------|
| <i>base</i>                 | SDHC peripheral base address.                                                 |
| <i>handle</i>               | SDHC handle.                                                                  |
| <i>admaTable</i>            | ADMA table address, can't be null if transfer way is ADMA1/ADMA2.             |
| <i>admaTable-<br/>Words</i> | ADMA table length united as words, can't be 0 if transfer way is ADMA1/ADMA2. |
| <i>transfer</i>             | Transfer content.                                                             |

### Return values

|                                                       |                                 |
|-------------------------------------------------------|---------------------------------|
| <i>kStatus_InvalidArgument</i>                        | Argument is invalid.            |
| <i>kStatus_SDHC_Busy-<br/>Transferring</i>            | Busy transferring.              |
| <i>kStatus_SDHC_Prepare-<br/>AdmaDescriptorFailed</i> | Prepare ADMA descriptor failed. |
| <i>kStatus_Success</i>                                | Operate successfully.           |

### 34.7.33 void SDHC\_TransferHandleIRQ ( SDHC\_Type \* *base*, sdhc\_handle\_t \* *handle* )

This function deals with the IRQs on the given host controller.

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | SDHC peripheral base address. |
| <i>handle</i> | SDHC handle.                  |

## Chapter 35

# SDRAMC: Synchronous DRAM Controller Driver

### 35.1 Overview

The KSDK provides a peripheral driver for the Synchronous DRAM Controller block of Kinetis devices.

The SDRAM controller commands include the initialization MRS command, precharge command, enter/exit self-refresh command, and enable/disable auto-refresh command. Use the [SDRAMC\\_SendCommand\(\)](#) to send these commands to SDRAM to initialize it. The [SDRAMC\\_EnableWriteProtect\(\)](#) is provided to enable/disable the write protection. The [SDRAMC\\_EnableOperateValid\(\)](#) is provided to enable/disable the operation valid.

### 35.2 Typical use case

This example shows how to use the SDRAM Controller driver to initialize the external 16 bit port-size 8-column SDRAM chip. Initialize the SDRAM controller and run the initialization sequence. The external SDRAM is initialized and the SDRAM read and write is available.

First, initialize the SDRAM Controller.

```
sdrmc_config_t config;
uint32_t clockSrc;

// SDRAM refresh timing configuration.
clockSrc = CLOCK_GetFreq(kCLOCK_BusClk);
sdrmc_refresh_config_t refConfig =
{
    kSDRAMC_RefreshThreeClocks,
    15625,    // SDRAM: 4096 rows/ 64ms.
    clockSrc,
};
// SDRAM controller configuration.
sdrmc_blockctl_config_t ctlConfig =
{
    kSDRAMC_Block0,
    kSDRAMC_PortSize16Bit,
    kSDRAMC_Commandbit19,
    kSDRAMC_LatencyOne,
    SDRAM_START_ADDRESS,
    0x7c0000,
};

config.refreshConfig = &refConfig;
config.blockConfig = &ctlConfig;
config.numBlockConfig = 1;

// SDRAM controller initialization.
SDRAMC_Init(base, &config);
```

Then, run the initialization sequence.

```
// Issues a PALL command.
```

## Typical use case

```
SDRAMC_SendCommand(base, whichBlock, kSDRAMC_PrechargeCommand);

// Accesses an SDRAM location.
*(uint8_t *) (SDRAM_START_ADDRESS) = SDRAM_COMMAND_ACCESSVALUE;

// Enables the refresh.
SDRAMC_SendCommand(base, whichBlock,
    kSDRAMC_AutoRefreshEnableCommand);

// Waits for 8 refresh cycles less than one microsecond.
delay;

// Issues the MSR command.
SDRAMC_SendCommand(base, whichBlock, kSDRAMC_ImrsCommand);

// Puts the correct value on the SDRAM address bus for the SDRAM mode register.
addr = ....;

// Set MRS register.
mrsAddr = (uint8_t *) (SDRAM_START_ADDRESS + addr);
*mrsAddr = SDRAM_COMMAND_ACCESSVALUE;
```

## Data Structures

- struct [sdramc\\_blockctl\\_config\\_t](#)  
*SDRAM controller block control configuration structure. [More...](#)*
- struct [sdramc\\_refresh\\_config\\_t](#)  
*SDRAM controller refresh timing configuration structure. [More...](#)*
- struct [sdramc\\_config\\_t](#)  
*SDRAM controller configuration structure. [More...](#)*

## Enumerations

- enum [sdramc\\_refresh\\_time\\_t](#) {  
    [kSDRAMC\\_RefreshThreeClocks](#) = 0x0U,  
    [kSDRAMC\\_RefreshSixClocks](#),  
    [kSDRAMC\\_RefreshNineClocks](#) }  
*SDRAM controller auto-refresh timing.*
- enum [sdramc\\_latency\\_t](#) {  
    [kSDRAMC\\_LatencyZero](#) = 0x0U,  
    [kSDRAMC\\_LatencyOne](#),  
    [kSDRAMC\\_LatencyTwo](#),  
    [kSDRAMC\\_LatencyThree](#) }  
*Setting latency for SDRAM controller timing specifications.*
- enum [sdramc\\_command\\_bit\\_location\\_t](#) {  
    [kSDRAMC\\_Commandbit17](#) = 0x0U,  
    [kSDRAMC\\_Commandbit18](#),  
    [kSDRAMC\\_Commandbit19](#),  
    [kSDRAMC\\_Commandbit20](#),  
    [kSDRAMC\\_Commandbit21](#),  
    [kSDRAMC\\_Commandbit22](#),  
    [kSDRAMC\\_Commandbit23](#),  
    [kSDRAMC\\_Commandbit24](#) }  
*SDRAM controller command bit location.*



- enum `sdramc_command_t` {  
`kSDRAMC_ImrsCommand` = 0x0U,  
`kSDRAMC_PrechargeCommand`,  
`kSDRAMC_SelfrefreshEnterCommand`,  
`kSDRAMC_SelfrefreshExitCommand`,  
`kSDRAMC_AutoRefreshEnableCommand`,  
`kSDRAMC_AutoRefreshDisableCommand` }  
*SDRAM controller command.*
- enum `sdramc_port_size_t` {  
`kSDRAMC_PortSize32Bit` = 0x0U,  
`kSDRAMC_PortSize8Bit`,  
`kSDRAMC_PortSize16Bit` }  
*SDRAM port size.*
- enum `sdramc_block_selection_t` {  
`kSDRAMC_Block0` = 0x0U,  
`kSDRAMC_Block1` }  
*SDRAM controller block selection.*

## Driver version

- #define `FSL_SDRAMC_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 0)`)  
*SDRAMC driver version 2.1.0.*

## SDRAM Controller Initialization and De-initialization

- void `SDRAMC_Init` (`SDRAM_Type *base`, `sdramc_config_t *configure`)  
*Initializes the SDRAM controller.*
- void `SDRAMC_Deinit` (`SDRAM_Type *base`)  
*Deinitializes the SDRAM controller module and gates the clock.*

## SDRAM Controller Basic Operation

- void `SDRAMC_SendCommand` (`SDRAM_Type *base`, `sdramc_block_selection_t` block, `sdramc_command_t` command)  
*Sends the SDRAM command.*
- static void `SDRAMC_EnableWriteProtect` (`SDRAM_Type *base`, `sdramc_block_selection_t` block, bool enable)  
*Enables/disables the write protection.*
- static void `SDRAMC_EnableOperateValid` (`SDRAM_Type *base`, `sdramc_block_selection_t` block, bool enable)  
*Enables/disables the valid operation.*

### 35.3 Data Structure Documentation

#### 35.3.1 struct sdramc\_blockctl\_config\_t

##### Data Fields

- [sdramc\\_block\\_selection\\_t block](#)  
*The block number.*
- [sdramc\\_port\\_size\\_t portSize](#)  
*The port size of the associated SDRAM block.*
- [sdramc\\_command\\_bit\\_location\\_t location](#)  
*The command bit location.*
- [sdramc\\_latency\\_t latency](#)  
*The latency for some timing specifications.*
- [uint32\\_t address](#)  
*The base address of the SDRAM block.*
- [uint32\\_t addressMask](#)  
*The base address mask of the SDRAM block.*

##### 35.3.1.0.0.87 Field Documentation

35.3.1.0.0.87.1 [sdramc\\_block\\_selection\\_t sdramc\\_blockctl\\_config\\_t::block](#)

35.3.1.0.0.87.2 [sdramc\\_port\\_size\\_t sdramc\\_blockctl\\_config\\_t::portSize](#)

35.3.1.0.0.87.3 [sdramc\\_command\\_bit\\_location\\_t sdramc\\_blockctl\\_config\\_t::location](#)

35.3.1.0.0.87.4 [sdramc\\_latency\\_t sdramc\\_blockctl\\_config\\_t::latency](#)

35.3.1.0.0.87.5 [uint32\\_t sdramc\\_blockctl\\_config\\_t::address](#)

35.3.1.0.0.87.6 [uint32\\_t sdramc\\_blockctl\\_config\\_t::addressMask](#)

#### 35.3.2 struct sdramc\_refresh\_config\_t

##### Data Fields

- [sdramc\\_refresh\\_time\\_t refreshTime](#)  
*Trc: The number of bus clocks inserted between a REF and next ACTIVE command.*
- [uint32\\_t sdramRefreshRow](#)  
*The SDRAM refresh time each row: ns/row.*
- [uint32\\_t busClock\\_Hz](#)  
*The bus clock for SDRAMC.*

**35.3.2.0.0.88 Field Documentation****35.3.2.0.0.88.1** `sdrmc_refresh_time_t sdrmc_refresh_config_t::refreshTime`**35.3.2.0.0.88.2** `uint32_t sdrmc_refresh_config_t::sdramRefreshRow`**35.3.2.0.0.88.3** `uint32_t sdrmc_refresh_config_t::busClock_Hz`**35.3.3 struct sdrmc\_config\_t**

Defines a configure structure and uses the SDRAMC\_Configure() function to make necessary initializations.

**Data Fields**

- `sdrmc_refresh_config_t * refreshConfig`  
*Refresh timing configure structure pointer.*
- `sdrmc_blockctl_config_t * blockConfig`  
*Block configure structure pointer.*
- `uint8_t numBlockConfig`  
*SDRAM block numbers for configuration.*

**35.3.3.0.0.89 Field Documentation****35.3.3.0.0.89.1** `sdrmc_refresh_config_t* sdrmc_config_t::refreshConfig`**35.3.3.0.0.89.2** `sdrmc_blockctl_config_t* sdrmc_config_t::blockConfig`

If both SDRAM blocks are used, use the two continuous blockConfig.

**35.3.3.0.0.89.3** `uint8_t sdrmc_config_t::numBlockConfig`**35.4 Macro Definition Documentation****35.4.1** `#define FSL_SDRAMC_DRIVER_VERSION (MAKE_VERSION(2, 1, 0))`**35.5 Enumeration Type Documentation****35.5.1 enum sdrmc\_refresh\_time\_t**

Enumerator

*kSDRAMC\_RefreshThreeClocks* The refresh timing with three bus clocks.

*kSDRAMC\_RefreshSixClocks* The refresh timing with six bus clocks.

*kSDRAMC\_RefreshNineClocks* The refresh timing with nine bus clocks.

## Enumeration Type Documentation

### 35.5.2 enum sdramc\_latency\_t

The latency setting affects the following SDRAM timing specifications:

- trcd: SRAS assertion to SCAS assertion
- tcasl: SCAS assertion to data out
- tras: ACTV command to Precharge command
- trp: Precharge command to ACTV command
- trwl, trdl: Last data input to Precharge command
- tep: Last data out to Precharge command

The details of the latency setting and timing specifications are shown in the following table list.

latency trcd: tcasl tras trp trwl, trdl tep

0 1 bus clock 1 bus clock 2 bus clocks 1 bus clock 1 bus clock 1 bus clock

1 2 bus clock 2 bus clock 4 bus clocks 2 bus clock 1 bus clock 1 bus clock

2 3 bus clock 3 bus clock 6 bus clocks 3 bus clock 1 bus clock 1 bus clock

3 3 bus clock 3 bus clock 6 bus clocks 3 bus clock 1 bus clock 1 bus clock

Enumerator

***kSDRAMC\_LatencyZero*** Latency 0.

***kSDRAMC\_LatencyOne*** Latency 1.

***kSDRAMC\_LatencyTwo*** Latency 2.

***kSDRAMC\_LatencyThree*** Latency 3.

### 35.5.3 enum sdramc\_command\_bit\_location\_t

Enumerator

***kSDRAMC\_Commandbit17*** Command bit location is bit 17.

***kSDRAMC\_Commandbit18*** Command bit location is bit 18.

***kSDRAMC\_Commandbit19*** Command bit location is bit 19.

***kSDRAMC\_Commandbit20*** Command bit location is bit 20.

***kSDRAMC\_Commandbit21*** Command bit location is bit 21.

***kSDRAMC\_Commandbit22*** Command bit location is bit 22.

***kSDRAMC\_Commandbit23*** Command bit location is bit 23.

***kSDRAMC\_Commandbit24*** Command bit location is bit 24.

### 35.5.4 enum sdramc\_command\_t

Enumerator

***kSDRAMC\_ImrsCommand*** Initiate MRS command.

***kSDRAMC\_PrechargeCommand*** Initiate precharge command.

***kSDRAMC\_SelfrefreshEnterCommand*** Enter self-refresh command.

***kSDRAMC\_SelfrefreshExitCommand*** Exit self-refresh command.

***kSDRAMC\_AutoRefreshEnableCommand*** Enable Auto refresh command.

***kSDRAMC\_AutoRefreshDisableCommand*** Disable Auto refresh command.

### 35.5.5 enum sdramc\_port\_size\_t

Enumerator

***kSDRAMC\_PortSize32Bit*** 32-Bit port size.

***kSDRAMC\_PortSize8Bit*** 8-Bit port size.

***kSDRAMC\_PortSize16Bit*** 16-Bit port size.

### 35.5.6 enum sdramc\_block\_selection\_t

Enumerator

***kSDRAMC\_Block0*** Select SDRAM block 0.

***kSDRAMC\_Block1*** Select SDRAM block 1.

## 35.6 Function Documentation

### 35.6.1 void SDRAMC\_Init ( SDRAM\_Type \* *base*, sdramc\_config\_t \* *configure* )

This function ungates the SDRAM controller clock and initializes the SDRAM controller. This function must be called before calling any other SDRAM controller driver functions. Example

```
sdramc_refresh_config_t refreshConfig;
sdramc_blockctl_config_t blockConfig;
sdramc_config_t config;

refreshConfig.refreshTime = kSDRAM_RefreshThreeClocks;
refreshConfig.sdramRefreshRow = 15625;
refreshConfig.busClock = 60000000;

blockConfig.block = kSDRAMC_Block0;
blockConfig.portSize = kSDRAMC_PortSize16Bit;
blockConfig.location = kSDRAMC_Commandbit19;
blockConfig.latency = kSDRAMC_RefreshThreeClocks;
blockConfig.address = SDRAM_START_ADDRESS;
blockConfig.addressMask = 0x7c0000;

config.refreshConfig = &refreshConfig;
config.blockConfig = &blockConfig;
config.totalBlocks = 1;

SDRAMC_Init(SDRAM, &config);
```

## Function Documentation

### Parameters

|                  |                                            |
|------------------|--------------------------------------------|
| <i>base</i>      | SDRAM controller peripheral base address.  |
| <i>configure</i> | The SDRAM configuration structure pointer. |

### 35.6.2 void SDRAMC\_Deinit ( SDRAM\_Type \* *base* )

This function gates the SDRAM controller clock. As a result, the SDRAM controller module doesn't work after calling this function.

### Parameters

|             |                                           |
|-------------|-------------------------------------------|
| <i>base</i> | SDRAM controller peripheral base address. |
|-------------|-------------------------------------------|

### 35.6.3 void SDRAMC\_SendCommand ( SDRAM\_Type \* *base*, sdramc\_block\_selection\_t *block*, sdramc\_command\_t *command* )

This function sends commands to SDRAM. The commands are precharge command, initialization MR-S command, auto-refresh enable/disable command, and self-refresh enter/exit commands. Note that the self-refresh enter/exit commands are all blocks setting and "block" is ignored. Ensure to set the correct "block" when send other commands.

### Parameters

|                |                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | SDRAM controller peripheral base address.                                                                                                                                                                                                                                                                                                                                                                                 |
| <i>block</i>   | The block selection.                                                                                                                                                                                                                                                                                                                                                                                                      |
| <i>command</i> | The SDRAM command, see "sdramc_command_t".<br>kSDRAMC_ImrsCommand - Initialize MRS command<br>kSDRAMC_PrechargeCommand - Initialize precharge command<br>kSDRAMC_SelfrefreshEnterCommand - Enter self-refresh command<br>kSDRAMC_SelfrefreshExitCommand - Exit self-refresh command<br>kSDRAMC_AutoRefreshEnableCommand - Enable auto refresh command<br>kSDRAMC_AutoRefreshDisableCommand - Disable auto refresh command |

### 35.6.4 static void SDRAMC\_EnableWriteProtect ( SDRAM\_Type \* *base*, sdramc\_block\_selection\_t *block*, bool *enable* ) [inline], [static]

## Parameters

|               |                                                               |
|---------------|---------------------------------------------------------------|
| <i>base</i>   | SDRAM peripheral base address.                                |
| <i>block</i>  | The block which is selected.                                  |
| <i>enable</i> | True enable write protection, false disable write protection. |

**35.6.5 static void SDRAMC\_EnableOperateValid ( SDRAM\_Type \* *base*,  
sdramc\_block\_selection\_t *block*, bool *enable* ) [inline], [static]**

## Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | SDRAM peripheral base address.                                      |
| <i>block</i>  | The block which is selected.                                        |
| <i>enable</i> | True enable the valid operation; false disable the valid operation. |





## Chapter 36

# SIM: System Integration Module Driver

### 36.1 Overview

The KSDK provides a peripheral driver for the System Integration Module (SIM) of Kinetis devices.

### Data Structures

- struct [sim\\_uid\\_t](#)  
*Unique ID. [More...](#)*

### Enumerations

- enum [\\_sim\\_usb\\_volt\\_reg\\_enable\\_mode](#) {  
[kSIM\\_UsbVoltRegEnable](#) = SIM\_SOPT1\_USBREGEN\_MASK,  
[kSIM\\_UsbVoltRegEnableInLowPower](#) = SIM\_SOPT1\_USBVSTBY\_MASK,  
[kSIM\\_UsbVoltRegEnableInStop](#) = SIM\_SOPT1\_USBSSTBY\_MASK,  
[kSIM\\_UsbVoltRegEnableInAllModes](#) }  
*USB voltage regulator enable setting.*
- enum [\\_sim\\_flash\\_mode](#) {  
[kSIM\\_FlashDisableInWait](#) = SIM\_FCFG1\_FLASHDOZE\_MASK,  
[kSIM\\_FlashDisable](#) = SIM\_FCFG1\_FLASHDIS\_MASK }  
*Flash enable mode.*

### Functions

- void [SIM\\_SetUsbVoltRegulatorEnableMode](#) (uint32\_t mask)  
*Sets the USB voltage regulator setting.*
- void [SIM\\_GetUniqueId](#) ([sim\\_uid\\_t](#) \*uid)  
*Gets the unique identification register value.*
- static void [SIM\\_SetFlashMode](#) (uint8\_t mode)  
*Sets the flash enable mode.*

### Driver version

- #define [FSL\\_SIM\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 0, 0))  
*Driver version 2.0.0.*

### 36.2 Data Structure Documentation

#### 36.2.1 struct [sim\\_uid\\_t](#)

### Data Fields

- uint32\_t [MH](#)

## Function Documentation

- *UIDMH.*  
uint32\_t [ML](#)
- *UIDML.*  
uint32\_t [L](#)
- *UIDL.*

### 36.2.1.0.0.90 Field Documentation

36.2.1.0.0.90.1 uint32\_t sim\_uid\_t::MH

36.2.1.0.0.90.2 uint32\_t sim\_uid\_t::ML

36.2.1.0.0.90.3 uint32\_t sim\_uid\_t::L

## 36.3 Enumeration Type Documentation

### 36.3.1 enum \_sim\_usb\_volt\_reg\_enable\_mode

Enumerator

*kSIM\_UsbVoltRegEnable* Enable voltage regulator.

*kSIM\_UsbVoltRegEnableInLowPower* Enable voltage regulator in VLPR/VLPW modes.

*kSIM\_UsbVoltRegEnableInStop* Enable voltage regulator in STOP/VLPS/LLS/VLLS modes.

*kSIM\_UsbVoltRegEnableInAllModes* Enable voltage regulator in all power modes.

### 36.3.2 enum \_sim\_flash\_mode

Enumerator

*kSIM\_FlashDisableInWait* Disable flash in wait mode.

*kSIM\_FlashDisable* Disable flash in normal mode.

## 36.4 Function Documentation

### 36.4.1 void SIM\_SetUsbVoltRegulatorEnableMode ( uint32\_t *mask* )

This function configures whether the USB voltage regulator is enabled in normal RUN mode, STOP-/VLPS/LLS/VLLS modes, and VLPR/VLPW modes. The configurations are passed in as mask value of [\\_sim\\_usb\\_volt\\_reg\\_enable\\_mode](#). For example, to enable USB voltage regulator in RUN/VLPR/VLPW modes and disable in STOP/VLPS/LLS/VLLS mode, use:

```
SIM_SetUsbVoltRegulatorEnableMode(kSIM_UsbVoltRegEnable | kSIM_UsbVoltRegEnableInLowPower);
```

Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>mask</i> | USB voltage regulator enable setting. |
|-------------|---------------------------------------|

### 36.4.2 void SIM\_GetUniqueld ( sim\_uid\_t \* *uid* )

Parameters

|            |                                                 |
|------------|-------------------------------------------------|
| <i>uid</i> | Pointer to the structure to save the UID value. |
|------------|-------------------------------------------------|

### 36.4.3 static void SIM\_SetFlashMode ( uint8\_t *mode* ) [inline], [static]

Parameters

|             |                                                                        |
|-------------|------------------------------------------------------------------------|
| <i>mode</i> | The mode to set; see <a href="#">_sim_flash_mode</a> for mode details. |
|-------------|------------------------------------------------------------------------|



## Chapter 37

# SMC: System Mode Controller Driver

### 37.1 Overview

The KSDK provides a peripheral driver for the System Mode Controller (SMC) module of Kinetis devices. The SMC module sequences the system in and out of all low-power stop and run modes.

API functions are provided to configure the system for working in a dedicated power mode. For different power modes, `SMC_SetPowerModexxx()` function accepts different parameters. System power mode state transitions are not available between power modes. For details about available transitions, see the power mode transitions section in the SoC reference manual.

### 37.2 Typical use case

#### 37.2.1 Enter wait or stop modes

SMC driver provides APIs to set MCU to different wait modes and stop modes. Pre and post functions are used for setting the modes. The pre functions and post functions are used as follows.

1. Disable/enable the interrupt through PRIMASK. This is an example use case. The application sets the wakeup interrupt and calls SMC function [SMC\\_SetPowerModeStop](#) to set the MCU to STOP mode, but the wakeup interrupt happens so quickly that the ISR completes before the function [SMC\\_SetPowerModeStop](#). As a result, the MCU enters the STOP mode and never is woken up by the interrupt. In this use case, the application first disables the interrupt through PRIMASK, sets the wakeup interrupt, and enters the STOP mode. After wakeup, enable the interrupt through PRIMASK. The MCU can still be woken up by disabling the interrupt through PRIMASK. The pre and post functions handle the PRIMASK.
2. Disable/enable the flash speculation. When entering stop modes, the flash speculation might be interrupted. As a result, pre functions disable the flash speculation and post functions enable it.

```
SMC_PreEnterStopModes();  
  
/* Enable the wakeup interrupt here. */  
  
SMC_SetPowerModeStop(SMC, kSMC_PartialStop);  
  
SMC_PostExitStopModes();
```

### Data Structures

- struct [smc\\_power\\_mode\\_lls\\_config\\_t](#)  
*SMC Low-Leakage Stop power mode configuration. [More...](#)*
- struct [smc\\_power\\_mode\\_vlls\\_config\\_t](#)  
*SMC Very Low-Leakage Stop power mode configuration. [More...](#)*

## Typical use case

### Enumerations

- enum `smc_power_mode_protection_t` {  
    `kSMC_AllowPowerModeVlls` = `SMC_PMPROT_AVLLS_MASK`,  
    `kSMC_AllowPowerModeLls` = `SMC_PMPROT_ALLS_MASK`,  
    `kSMC_AllowPowerModeVlp` = `SMC_PMPROT_AVLP_MASK`,  
    `kSMC_AllowPowerModeHsrunk` = `SMC_PMPROT_AHSRUN_MASK`,  
    `kSMC_AllowPowerModeAll` }  
    *Power Modes Protection.*
- enum `smc_power_state_t` {  
    `kSMC_PowerStateRun` = `0x01U << 0U`,  
    `kSMC_PowerStateStop` = `0x01U << 1U`,  
    `kSMC_PowerStateVlpr` = `0x01U << 2U`,  
    `kSMC_PowerStateVlpw` = `0x01U << 3U`,  
    `kSMC_PowerStateVlps` = `0x01U << 4U`,  
    `kSMC_PowerStateLls` = `0x01U << 5U`,  
    `kSMC_PowerStateVlls` = `0x01U << 6U`,  
    `kSMC_PowerStateHsrunk` = `0x01U << 7U` }  
    *Power Modes in PMSTAT.*
- enum `smc_run_mode_t` {  
    `kSMC_RunNormal` = `0U`,  
    `kSMC_RunVlpr` = `2U`,  
    `kSMC_Hsrunk` = `3U` }  
    *Run mode definition.*
- enum `smc_stop_mode_t` {  
    `kSMC_StopNormal` = `0U`,  
    `kSMC_StopVlps` = `2U`,  
    `kSMC_StopLls` = `3U`,  
    `kSMC_StopVlls` = `4U` }  
    *Stop mode definition.*
- enum `smc_stop_submode_t` {  
    `kSMC_StopSub0` = `0U`,  
    `kSMC_StopSub1` = `1U`,  
    `kSMC_StopSub2` = `2U`,  
    `kSMC_StopSub3` = `3U` }  
    *VLLS/LLS stop sub mode definition.*
- enum `smc_partial_stop_option_t` {  
    `kSMC_PartialStop` = `0U`,  
    `kSMC_PartialStop1` = `1U`,  
    `kSMC_PartialStop2` = `2U` }  
    *Partial STOP option.*
- enum `_smc_status` { `kStatus_SMC_StopAbort` = `MAKE_STATUS(kStatusGroup_POWER, 0)` }  
    *SMC configuration status.*

### Driver version

- #define `FSL_SMC_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 3)`)  
    *SMC driver version 2.0.3.*

## System mode controller APIs

- static void [SMC\\_SetPowerModeProtection](#) (SMC\_Type \*base, uint8\_t allowedModes)  
*Configures all power mode protection settings.*
- static [smc\\_power\\_state\\_t](#) [SMC\\_GetPowerModeState](#) (SMC\_Type \*base)  
*Gets the current power mode status.*
- void [SMC\\_PreEnterStopModes](#) (void)  
*Prepares to enter stop modes.*
- void [SMC\\_PostExitStopModes](#) (void)  
*Recovers after wake up from stop modes.*
- static void [SMC\\_PreEnterWaitModes](#) (void)  
*Prepares to enter wait modes.*
- static void [SMC\\_PostExitWaitModes](#) (void)  
*Recovers after wake up from stop modes.*
- status\_t [SMC\\_SetPowerModeRun](#) (SMC\_Type \*base)  
*Configures the system to RUN power mode.*
- status\_t [SMC\\_SetPowerModeHsrun](#) (SMC\_Type \*base)  
*Configures the system to HSRUN power mode.*
- status\_t [SMC\\_SetPowerModeWait](#) (SMC\_Type \*base)  
*Configures the system to WAIT power mode.*
- status\_t [SMC\\_SetPowerModeStop](#) (SMC\_Type \*base, [smc\\_partial\\_stop\\_option\\_t](#) option)  
*Configures the system to Stop power mode.*
- status\_t [SMC\\_SetPowerModeVlpr](#) (SMC\_Type \*base)  
*Configures the system to VLPR power mode.*
- status\_t [SMC\\_SetPowerModeVlpw](#) (SMC\_Type \*base)  
*Configures the system to VLPW power mode.*
- status\_t [SMC\\_SetPowerModeVlps](#) (SMC\_Type \*base)  
*Configures the system to VLPS power mode.*
- status\_t [SMC\\_SetPowerModeLls](#) (SMC\_Type \*base, const [smc\\_power\\_mode\\_lls\\_config\\_t](#) \*config)  
*Configures the system to LLS power mode.*
- status\_t [SMC\\_SetPowerModeVlls](#) (SMC\_Type \*base, const [smc\\_power\\_mode\\_vlls\\_config\\_t](#) \*config)  
*Configures the system to VLLS power mode.*

## 37.3 Data Structure Documentation

### 37.3.1 struct smc\_power\_mode\_lls\_config\_t

#### Data Fields

- [smc\\_stop\\_submode\\_t](#) subMode  
*Low-leakage Stop sub-mode.*

### 37.3.2 struct smc\_power\_mode\_vlls\_config\_t

#### Data Fields

- [smc\\_stop\\_submode\\_t](#) subMode

## Enumeration Type Documentation

- *Very Low-leakage Stop sub-mode.*  
bool [enablePorDetectInVlls0](#)  
*Enable Power on reset detect in VLLS mode.*
- bool [enableRam2InVlls2](#)  
*Enable RAM2 power in VLLS2.*

## 37.4 Macro Definition Documentation

### 37.4.1 #define FSL\_SMC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 3))

## 37.5 Enumeration Type Documentation

### 37.5.1 enum smc\_power\_mode\_protection\_t

Enumerator

*kSMC\_AllowPowerModeVlls* Allow Very-low-leakage Stop Mode.  
*kSMC\_AllowPowerModeLls* Allow Low-leakage Stop Mode.  
*kSMC\_AllowPowerModeVlpr* Allow Very-Low-power Mode.  
*kSMC\_AllowPowerModeHsrunk* Allow High-speed Run mode.  
*kSMC\_AllowPowerModeAll* Allow all power mode.

### 37.5.2 enum smc\_power\_state\_t

Enumerator

*kSMC\_PowerStateRun* 0000\_0001 - Current power mode is RUN  
*kSMC\_PowerStateStop* 0000\_0010 - Current power mode is STOP  
*kSMC\_PowerStateVlpr* 0000\_0100 - Current power mode is VLPR  
*kSMC\_PowerStateVlpw* 0000\_1000 - Current power mode is VLPW  
*kSMC\_PowerStateVlps* 0001\_0000 - Current power mode is VLPS  
*kSMC\_PowerStateLls* 0010\_0000 - Current power mode is LLS  
*kSMC\_PowerStateVlls* 0100\_0000 - Current power mode is VLLS  
*kSMC\_PowerStateHsrunk* 1000\_0000 - Current power mode is HSRUN

### 37.5.3 enum smc\_run\_mode\_t

Enumerator

*kSMC\_RunNormal* Normal RUN mode.  
*kSMC\_RunVlpr* Very-low-power RUN mode.  
*kSMC\_Hsrunk* High-speed Run mode (HSRUN).



### 37.5.4 enum smc\_stop\_mode\_t

Enumerator

*kSMC\_StopNormal* Normal STOP mode.  
*kSMC\_StopVlps* Very-low-power STOP mode.  
*kSMC\_StopLls* Low-leakage Stop mode.  
*kSMC\_StopVlls* Very-low-leakage Stop mode.

### 37.5.5 enum smc\_stop\_submode\_t

Enumerator

*kSMC\_StopSub0* Stop submode 0, for VLLS0/LLS0.  
*kSMC\_StopSub1* Stop submode 1, for VLLS1/LLS1.  
*kSMC\_StopSub2* Stop submode 2, for VLLS2/LLS2.  
*kSMC\_StopSub3* Stop submode 3, for VLLS3/LLS3.

### 37.5.6 enum smc\_partial\_stop\_option\_t

Enumerator

*kSMC\_PartialStop* STOP - Normal Stop mode.  
*kSMC\_PartialStop1* Partial Stop with both system and bus clocks disabled.  
*kSMC\_PartialStop2* Partial Stop with system clock disabled and bus clock enabled.

### 37.5.7 enum \_smc\_status

Enumerator

*kStatus\_SMC\_StopAbort* Entering Stop mode is abort.

## 37.6 Function Documentation

### 37.6.1 static void SMC\_SetPowerModeProtection ( SMC\_Type \* *base*, uint8\_t *allowedModes* ) [inline], [static]

This function configures the power mode protection settings for supported power modes in the specified chip family. The available power modes are defined in the `smc_power_mode_protection_t`. This should be done at an early system level initialization stage. See the reference manual for details. This register can only write once after the power reset.

---

## Function Documentation

The allowed modes are passed as bit map. For example, to allow LLS and VLLS, use `SMC_SetPowerModeProtection(kSMC_AllowPowerModeVlls | kSMC_AllowPowerModeVlps)`. To allow all modes, use `SMC_SetPowerModeProtection(kSMC_AllowPowerModeAll)`.

## Parameters

|                     |                                    |
|---------------------|------------------------------------|
| <i>base</i>         | SMC peripheral base address.       |
| <i>allowedModes</i> | Bitmap of the allowed power modes. |

### 37.6.2 static smc\_power\_state\_t SMC\_GetPowerModeState ( SMC\_Type \* *base* ) [inline], [static]

This function returns the current power mode status. After the application switches the power mode, it should always check the status to check whether it runs into the specified mode or not. The application should check this mode before switching to a different mode. The system requires that only certain modes can switch to other specific modes. See the reference manual for details and the `smc_power_state_t` for information about the power status.

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

## Returns

Current power mode status.

### 37.6.3 void SMC\_PreEnterStopModes ( void )

This function should be called before entering STOP/VLPS/LLS/VLLS modes.

### 37.6.4 void SMC\_PostExitStopModes ( void )

This function should be called after wake up from STOP/VLPS/LLS/VLLS modes. It is used with [SMC\\_PreEnterStopModes](#).

### 37.6.5 static void SMC\_PreEnterWaitModes ( void ) [inline], [static]

This function should be called before entering WAIT/VLPW modes.

### 37.6.6 static void SMC\_PostExitWaitModes ( void ) [inline], [static]

This function should be called after wake up from WAIT/VLPW modes. It is used with [SMC\\_PreEnterWaitModes](#).

### 37.6.7 status\_t SMC\_SetPowerModeRun ( SMC\_Type \* *base* )

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

## Returns

SMC configuration error code.

### 37.6.8 **status\_t SMC\_SetPowerModeHsrun ( SMC\_Type \* *base* )**

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

## Returns

SMC configuration error code.

### 37.6.9 **status\_t SMC\_SetPowerModeWait ( SMC\_Type \* *base* )**

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

## Returns

SMC configuration error code.

### 37.6.10 **status\_t SMC\_SetPowerModeStop ( SMC\_Type \* *base*, smc\_partial\_stop\_option\_t *option* )**

## Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | SMC peripheral base address. |
| <i>option</i> | Partial Stop mode option.    |

## Returns

SMC configuration error code.

**37.6.11**   `status_t SMC_SetPowerModeVlpr ( SMC_Type * base )`

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

## Returns

SMC configuration error code.

### 37.6.12 **status\_t SMC\_SetPowerModeVlpw ( SMC\_Type \* *base* )**

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

## Returns

SMC configuration error code.

### 37.6.13 **status\_t SMC\_SetPowerModeVlps ( SMC\_Type \* *base* )**

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

## Returns

SMC configuration error code.

### 37.6.14 **status\_t SMC\_SetPowerModeLls ( SMC\_Type \* *base*, const smc\_power\_mode\_lls\_config\_t \* *config* )**

## Parameters

|               |                                            |
|---------------|--------------------------------------------|
| <i>base</i>   | SMC peripheral base address.               |
| <i>config</i> | The LLS power mode configuration structure |

## Returns

SMC configuration error code.

**37.6.15** `status_t SMC_SetPowerModeVlls ( SMC_Type * base, const  
smc_power_mode_vlls_config_t * config )`



## Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>base</i>   | SMC peripheral base address.                 |
| <i>config</i> | The VLLS power mode configuration structure. |

## Returns

SMC configuration error code.



## Chapter 38

### TPM: Timer PWM Module

#### 38.1 Overview

The KSDK provides a driver for the Timer PWM Module (TPM) of Kinetis devices.

The KSDK TPM driver supports the generation of PWM signals, input capture, and output compare modes. On some SoCs, the driver supports the generation of combined PWM signals, dual-edge capture, and quadrature decoder modes. The driver also supports configuring each of the TPM fault inputs. The fault input is available only on some SoCs.

The function [TPM\\_Init\(\)](#) initializes the TPM with a specified configurations. The function [TPM\\_GetDefaultConfig\(\)](#) gets the default configurations. On some SoCs, the initialization function issues a software reset to reset the TPM internal logic. The initialization function configures the TPM's behavior when it receives a trigger input and its operation in doze and debug modes.

The function [TPM\\_Deinit\(\)](#) disables the TPM counter and turns off the module clock.

The function [TPM\\_SetupPwm\(\)](#) sets up TPM channels for the PWM output. The function can set up the PWM signal properties for multiple channels. Each channel has its own [tpm\\_chnl\\_pwm\\_signal\\_param\\_t](#) structure that is used to specify the output signals duty cycle and level-mode. However, the same PWM period and PWM mode is applied to all channels requesting a PWM output. The signal duty cycle is provided as a percentage of the PWM period. Its value should be between 0 and 100 where 0=inactive signal (0% duty cycle) and 100=always active signal (100% duty cycle). When generating a combined PWM signal, the channel number passed refers to a channel pair number, for example 0 refers to channel 0 and 1, 1 refers to channels 2 and 3.

The function [TPM\\_UpdatePwmDutycycle\(\)](#) updates the PWM signal duty cycle of a particular TPM channel.

The function [TPM\\_UpdateChnlEdgeLevelSelect\(\)](#) updates the level select bits of a particular TPM channel. This can be used to disable the PWM output when making changes to the PWM signal.

The function [TPM\\_SetupInputCapture\(\)](#) sets up a TPM channel for input capture. The user can specify the capture edge.

The function [TPM\\_SetupDualEdgeCapture\(\)](#) can be used to measure the pulse width of a signal. This is available only for certain SoCs. A channel pair is used during the capture with the input signal coming through a channel that can be configured. The user can specify the capture edge for each channel and any filter value to be used when processing the input signal.

The function [TPM\\_SetupOutputCompare\(\)](#) sets up a TPM channel for output comparison. The user can specify the channel output on a successful comparison and a comparison value.

The function [TPM\\_SetupQuadDecode\(\)](#) sets up TPM channels 0 and 1 for quad decode, which is available only for certain SoCs. The user can specify the quad decode mode, polarity, and filter properties for each input signal.

## Typical use case

The function `TPM_SetupFault()` sets up the properties for each fault, which is available only for certain SoCs. The user can specify the fault polarity and whether to use a filter on a fault input. The overall fault filter value and fault control mode are set up during initialization.

Provides functions to get and clear the TPM status.

Provides functions to enable/disable TPM interrupts and get current enabled interrupts.

## 38.2 Typical use case

### 38.2.1 PWM output

Output the PWM signal on 2 TPM channels with different duty cycles. Periodically update the PWM signal duty cycle.

```
int main(void)
{
    bool brightnessUp = true; /* Indicates whether the LED is brighter or dimmer. */
    tpm_config_t tpmInfo;
    uint8_t updatedDutycycle = 0U;
    tpm_chnl_pwm_signal_param_t tpmParam[2];

    /* Configures the TPM parameters with frequency 24 kHz. */
    tpmParam[0].chnlNumber = (tpm_chnl_t)BOARD_FIRST_TPM_CHANNEL;
    tpmParam[0].level = kTPM_LowTrue;
    tpmParam[0].dutyCyclePercent = 0U;

    tpmParam[1].chnlNumber = (tpm_chnl_t)BOARD_SECOND_TPM_CHANNEL;
    tpmParam[1].level = kTPM_LowTrue;
    tpmParam[1].dutyCyclePercent = 0U;

    /* Board pin, clock, and debug console initialization. */
    BOARD_InitHardware();

    TPM_GetDefaultConfig(&tpmInfo);
    /* Initializes the TPM module. */
    TPM_Init(BOARD_TPM_BASEADDR, &tpmInfo);

    TPM_SetupPwm(BOARD_TPM_BASEADDR, tpmParam, 2U,
                 kTPM_EdgeAlignedPwm, 24000U, TPM_SOURCE_CLOCK);
    TPM_StartTimer(BOARD_TPM_BASEADDR, kTPM_SystemClock);
    while (1)
    {
        /* Delays to see the change of LED brightness. */
        delay();

        if (brightnessUp)
        {
            /* Increases a duty cycle until it reaches a limited value. */
            if (++updatedDutycycle == 100U)
            {
                brightnessUp = false;
            }
        }
        else
        {
            /* Decreases a duty cycle until it reaches a limited value. */
            if (--updatedDutycycle == 0U)
            {
                brightnessUp = true;
            }
        }
    }
}
```

```

    /* Starts PWM mode with an updated duty cycle. */
    TPM_UpdatePwmDutycycle(BOARD_TPM_BASEADDR, (
tpm_chnl_t)BOARD_FIRST_TPM_CHANNEL, kTPM_EdgeAlignedPwm,
                        updatedDutycycle);
    TPM_UpdatePwmDutycycle(BOARD_TPM_BASEADDR, (
tpm_chnl_t)BOARD_SECOND_TPM_CHANNEL, kTPM_EdgeAlignedPwm,
                        updatedDutycycle);
}

```

## Data Structures

- struct [tpm\\_chnl\\_pwm\\_signal\\_param\\_t](#)  
Options to configure a TPM channel's PWM signal. [More...](#)
- struct [tpm\\_dual\\_edge\\_capture\\_param\\_t](#)  
TPM dual edge capture parameters. [More...](#)
- struct [tpm\\_phase\\_params\\_t](#)  
TPM quadrature decode phase parameters. [More...](#)
- struct [tpm\\_config\\_t](#)  
TPM config structure. [More...](#)

## Enumerations

- enum [tpm\\_chnl\\_t](#) {  
kTPM\_Chnl\_0 = 0U,  
kTPM\_Chnl\_1,  
kTPM\_Chnl\_2,  
kTPM\_Chnl\_3,  
kTPM\_Chnl\_4,  
kTPM\_Chnl\_5,  
kTPM\_Chnl\_6,  
kTPM\_Chnl\_7 }  
List of TPM channels.
- enum [tpm\\_pwm\\_mode\\_t](#) {  
kTPM\_EdgeAlignedPwm = 0U,  
kTPM\_CenterAlignedPwm,  
kTPM\_CombinedPwm }  
TPM PWM operation modes.
- enum [tpm\\_pwm\\_level\\_select\\_t](#) {  
kTPM\_NoPwmSignal = 0U,  
kTPM\_LowTrue,  
kTPM\_HighTrue }  
TPM PWM output pulse mode: high-true, low-true or no output.
- enum [tpm\\_trigger\\_select\\_t](#)  
Trigger options available.
- enum [tpm\\_trigger\\_source\\_t](#) {  
kTPM\_TriggerSource\_External = 0U,  
kTPM\_TriggerSource\_Internal }  
Trigger source options available.
- enum [tpm\\_output\\_compare\\_mode\\_t](#) {

## Typical use case

```
kTPM_NoOutputSignal = (1U << TPM_CnSC_MSA_SHIFT),
kTPM_ToggleOnMatch = ((1U << TPM_CnSC_MSA_SHIFT) | (1U << TPM_CnSC_ELSA_SHIFT)),
kTPM_ClearOnMatch = ((1U << TPM_CnSC_MSA_SHIFT) | (2U << TPM_CnSC_ELSA_SHIFT)),
kTPM_SetOnMatch = ((1U << TPM_CnSC_MSA_SHIFT) | (3U << TPM_CnSC_ELSA_SHIFT)),
kTPM_HighPulseOutput = ((3U << TPM_CnSC_MSA_SHIFT) | (1U << TPM_CnSC_ELSA_SHIFT)),
kTPM_LowPulseOutput = ((3U << TPM_CnSC_MSA_SHIFT) | (2U << TPM_CnSC_ELSA_SHIFT)) }
```

*TPM output compare modes.*

- enum `tpm_input_capture_edge_t` {  
    kTPM\_RisingEdge = (1U << TPM\_CnSC\_ELSA\_SHIFT),  
    kTPM\_FallingEdge = (2U << TPM\_CnSC\_ELSA\_SHIFT),  
    kTPM\_RiseAndFallEdge = (3U << TPM\_CnSC\_ELSA\_SHIFT) }

*TPM input capture edge.*

- enum `tpm_quad_decode_mode_t` {  
    kTPM\_QuadPhaseEncode = 0U,  
    kTPM\_QuadCountAndDir }

*TPM quadrature decode modes.*

- enum `tpm_phase_polarity_t` {  
    kTPM\_QuadPhaseNormal = 0U,  
    kTPM\_QuadPhaseInvert }

*TPM quadrature phase polarities.*

- enum `tpm_clock_source_t` {  
    kTPM\_SystemClock = 1U,  
    kTPM\_ExternalClock }

*TPM clock source selection.*

- enum `tpm_clock_prescale_t` {  
    kTPM\_Prescale\_Divide\_1 = 0U,  
    kTPM\_Prescale\_Divide\_2,  
    kTPM\_Prescale\_Divide\_4,  
    kTPM\_Prescale\_Divide\_8,  
    kTPM\_Prescale\_Divide\_16,  
    kTPM\_Prescale\_Divide\_32,  
    kTPM\_Prescale\_Divide\_64,  
    kTPM\_Prescale\_Divide\_128 }

*TPM prescale value selection for the clock source.*

- enum `tpm_interrupt_enable_t` {

```

kTPM_Chnl0InterruptEnable = (1U << 0),
kTPM_Chnl1InterruptEnable = (1U << 1),
kTPM_Chnl2InterruptEnable = (1U << 2),
kTPM_Chnl3InterruptEnable = (1U << 3),
kTPM_Chnl4InterruptEnable = (1U << 4),
kTPM_Chnl5InterruptEnable = (1U << 5),
kTPM_Chnl6InterruptEnable = (1U << 6),
kTPM_Chnl7InterruptEnable = (1U << 7),
kTPM_TimeOverflowInterruptEnable = (1U << 8) }

```

*List of TPM interrupts.*

- enum `tpm_status_flags_t` {
 

```

kTPM_Chnl0Flag = (1U << 0),
kTPM_Chnl1Flag = (1U << 1),
kTPM_Chnl2Flag = (1U << 2),
kTPM_Chnl3Flag = (1U << 3),
kTPM_Chnl4Flag = (1U << 4),
kTPM_Chnl5Flag = (1U << 5),
kTPM_Chnl6Flag = (1U << 6),
kTPM_Chnl7Flag = (1U << 7),
kTPM_TimeOverflowFlag = (1U << 8) }

```

*List of TPM flags.*

## Driver version

- #define `FSL_TPM_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 2)`)  
Version 2.0.2.

## Initialization and deinitialization

- void `TPM_Init` (`TPM_Type *base`, const `tpm_config_t *config`)  
*Ungates the TPM clock and configures the peripheral for basic operation.*
- void `TPM_Deinit` (`TPM_Type *base`)  
*Stops the counter and gates the TPM clock.*
- void `TPM_GetDefaultConfig` (`tpm_config_t *config`)  
*Fill in the TPM config struct with the default settings.*

## Channel mode operations

- status\_t `TPM_SetupPwm` (`TPM_Type *base`, const `tpm_chnl_pwm_signal_param_t *chnlParams`, `uint8_t numOfChnls`, `tpm_pwm_mode_t mode`, `uint32_t pwmFreq_Hz`, `uint32_t srcClock_Hz`)  
*Configures the PWM signal parameters.*
- void `TPM_UpdatePwmDutycycle` (`TPM_Type *base`, `tpm_chnl_t chnlNumber`, `tpm_pwm_mode_t currentPwmMode`, `uint8_t dutyCyclePercent`)  
*Update the duty cycle of an active PWM signal.*
- void `TPM_UpdateChnlEdgeLevelSelect` (`TPM_Type *base`, `tpm_chnl_t chnlNumber`, `uint8_t level`)  
*Update the edge level selection for a channel.*
- void `TPM_SetupInputCapture` (`TPM_Type *base`, `tpm_chnl_t chnlNumber`, `tpm_input_capture_edge_t captureMode`)

## Data Structure Documentation

- *Enables capturing an input signal on the channel using the function parameters.*  
void [TPM\\_SetupOutputCompare](#) (TPM\_Type \*base, [tpm\\_chnl\\_t](#) chnlNumber, [tpm\\_output\\_compare\\_mode\\_t](#) compareMode, uint32\_t compareValue)
- *Configures the TPM to generate timed pulses.*  
void [TPM\\_SetupDualEdgeCapture](#) (TPM\_Type \*base, [tpm\\_chnl\\_t](#) chnlPairNumber, const [tpm\\_dual\\_edge\\_capture\\_param\\_t](#) \*edgeParam, uint32\_t filterValue)
- *Configures the dual edge capture mode of the TPM.*  
void [TPM\\_SetupQuadDecode](#) (TPM\_Type \*base, const [tpm\\_phase\\_params\\_t](#) \*phaseAParams, const [tpm\\_phase\\_params\\_t](#) \*phaseBParams, [tpm\\_quad\\_decode\\_mode\\_t](#) quadMode)
- *Configures the parameters and activates the quadrature decode mode.*

## Interrupt Interface

- void [TPM\\_EnableInterrupts](#) (TPM\_Type \*base, uint32\_t mask)  
*Enables the selected TPM interrupts.*
- void [TPM\\_DisableInterrupts](#) (TPM\_Type \*base, uint32\_t mask)  
*Disables the selected TPM interrupts.*
- uint32\_t [TPM\\_GetEnabledInterrupts](#) (TPM\_Type \*base)  
*Gets the enabled TPM interrupts.*

## Status Interface

- static uint32\_t [TPM\\_GetStatusFlags](#) (TPM\_Type \*base)  
*Gets the TPM status flags.*
- static void [TPM\\_ClearStatusFlags](#) (TPM\_Type \*base, uint32\_t mask)  
*Clears the TPM status flags.*

## Timer Start and Stop

- static void [TPM\\_StartTimer](#) (TPM\_Type \*base, [tpm\\_clock\\_source\\_t](#) clockSource)  
*Starts the TPM counter.*
- static void [TPM\\_StopTimer](#) (TPM\_Type \*base)  
*Stops the TPM counter.*

## 38.3 Data Structure Documentation

### 38.3.1 struct tpm\_chnl\_pwm\_signal\_param\_t

#### Data Fields

- [tpm\\_chnl\\_t](#) chnlNumber  
*TPM channel to configure.*
- [tpm\\_pwm\\_level\\_select\\_t](#) level  
*PWM output active level select.*
- uint8\_t [dutyCyclePercent](#)  
*PWM pulse width, value should be between 0 to 100 0=inactive signal(0% duty cycle)...*
- uint8\_t [firstEdgeDelayPercent](#)  
*Used only in combined PWM mode to generate asymmetrical PWM.*



**38.3.1.0.0.91 Field Documentation****38.3.1.0.0.91.1 tpm\_chnl\_t tpm\_chnl\_pwm\_signal\_param\_t::chnlNumber**

In combined mode (available in some SoC's, this represents the channel pair number

**38.3.1.0.0.91.2 uint8\_t tpm\_chnl\_pwm\_signal\_param\_t::dutyCyclePercent**

100=always active signal (100% duty cycle)

**38.3.1.0.0.91.3 uint8\_t tpm\_chnl\_pwm\_signal\_param\_t::firstEdgeDelayPercent**

Specifies the delay to the first edge in a PWM period. If unsure, leave as 0; Should be specified as percentage of the PWM period

**38.3.2 struct tpm\_dual\_edge\_capture\_param\_t**

Note

This mode is available only on some SoC's.

**Data Fields**

- bool [enableSwap](#)  
*true: Use channel n+1 input, channel n input is ignored; false: Use channel n input, channel n+1 input is ignored*
- [tpm\\_input\\_capture\\_edge\\_t currChanEdgeMode](#)  
*Input capture edge select for channel n.*
- [tpm\\_input\\_capture\\_edge\\_t nextChanEdgeMode](#)  
*Input capture edge select for channel n+1.*

**38.3.3 struct tpm\_phase\_params\_t****Data Fields**

- uint32\_t [phaseFilterVal](#)  
*Filter value, filter is disabled when the value is zero.*
- [tpm\\_phase\\_polarity\\_t phasePolarity](#)  
*Phase polarity.*

**38.3.4 struct tpm\_config\_t**

This structure holds the configuration settings for the TPM peripheral. To initialize this structure to reasonable defaults, call the [TPM\\_GetDefaultConfig\(\)](#) function and pass a pointer to your config structure

## Enumeration Type Documentation

instance.

The config struct can be made const so it resides in flash

### Data Fields

- [tpm\\_clock\\_prescale\\_t prescale](#)  
*Select TPM clock prescale value.*
- bool [useGlobalTimeBase](#)  
*true: Use of an external global time base is enabled; false: disabled*
- [tpm\\_trigger\\_select\\_t triggerSelect](#)  
*Input trigger to use for controlling the counter operation.*
- [tpm\\_trigger\\_source\\_t triggerSource](#)  
*Decides if we use external or internal trigger.*
- bool [enableDoze](#)  
*true: TPM counter is paused in doze mode; false: TPM counter continues in doze mode*
- bool [enableDebugMode](#)  
*true: TPM counter continues in debug mode; false: TPM counter is paused in debug mode*
- bool [enableReloadOnTrigger](#)  
*true: TPM counter is reloaded on trigger; false: TPM counter not reloaded*
- bool [enableStopOnOverflow](#)  
*true: TPM counter stops after overflow; false: TPM counter continues running after overflow*
- bool [enableStartOnTrigger](#)  
*true: TPM counter only starts when a trigger is detected; false: TPM counter starts immediately*
- bool [enablePauseOnTrigger](#)  
*true: TPM counter will pause while trigger remains asserted; false: TPM counter continues running*

#### 38.3.4.0.0.92 Field Documentation

##### 38.3.4.0.0.92.1 tpm\_trigger\_source\_t tpm\_config\_t::triggerSource

## 38.4 Enumeration Type Documentation

### 38.4.1 enum tpm\_chnl\_t

Note

Actual number of available channels is SoC dependent

Enumerator

- kTPM\_Chnl\_0** TPM channel number 0.
- kTPM\_Chnl\_1** TPM channel number 1.
- kTPM\_Chnl\_2** TPM channel number 2.
- kTPM\_Chnl\_3** TPM channel number 3.
- kTPM\_Chnl\_4** TPM channel number 4.
- kTPM\_Chnl\_5** TPM channel number 5.
- kTPM\_Chnl\_6** TPM channel number 6.
- kTPM\_Chnl\_7** TPM channel number 7.

### 38.4.2 enum tpm\_pwm\_mode\_t

Enumerator

*kTPM\_EdgeAlignedPwm* Edge aligned PWM.  
*kTPM\_CenterAlignedPwm* Center aligned PWM.  
*kTPM\_CombinedPwm* Combined PWM.

### 38.4.3 enum tpm\_pwm\_level\_select\_t

Enumerator

*kTPM\_NoPwmSignal* No PWM output on pin.  
*kTPM\_LowTrue* Low true pulses.  
*kTPM\_HighTrue* High true pulses.

### 38.4.4 enum tpm\_trigger\_select\_t

This is used for both internal & external trigger sources (external option available in certain SoC's)

Note

The actual trigger options available is SoC-specific.

### 38.4.5 enum tpm\_trigger\_source\_t

Note

This selection is available only on some SoC's. For SoC's without this selection, the only trigger source available is internal trigger.

Enumerator

*kTPM\_TriggerSource\_External* Use external trigger input.  
*kTPM\_TriggerSource\_Internal* Use internal trigger.

### 38.4.6 enum tpm\_output\_compare\_mode\_t

Enumerator

*kTPM\_NoOutputSignal* No channel output when counter reaches CnV.

## Enumeration Type Documentation

*kTPM\_ToggleOnMatch* Toggle output.  
*kTPM\_ClearOnMatch* Clear output.  
*kTPM\_SetOnMatch* Set output.  
*kTPM\_HighPulseOutput* Pulse output high.  
*kTPM\_LowPulseOutput* Pulse output low.

### 38.4.7 enum tpm\_input\_capture\_edge\_t

Enumerator

*kTPM\_RisingEdge* Capture on rising edge only.  
*kTPM\_FallingEdge* Capture on falling edge only.  
*kTPM\_RiseAndFallEdge* Capture on rising or falling edge.

### 38.4.8 enum tpm\_quad\_decode\_mode\_t

Note

This mode is available only on some SoC's.

Enumerator

*kTPM\_QuadPhaseEncode* Phase A and Phase B encoding mode.  
*kTPM\_QuadCountAndDir* Count and direction encoding mode.

### 38.4.9 enum tpm\_phase\_polarity\_t

Enumerator

*kTPM\_QuadPhaseNormal* Phase input signal is not inverted.  
*kTPM\_QuadPhaseInvert* Phase input signal is inverted.

### 38.4.10 enum tpm\_clock\_source\_t

Enumerator

*kTPM\_SystemClock* System clock.  
*kTPM\_ExternalClock* External clock.

### 38.4.11 enum tpm\_clock\_prescale\_t

Enumerator

*kTPM\_Prescale\_Divide\_1* Divide by 1.  
*kTPM\_Prescale\_Divide\_2* Divide by 2.  
*kTPM\_Prescale\_Divide\_4* Divide by 4.  
*kTPM\_Prescale\_Divide\_8* Divide by 8.  
*kTPM\_Prescale\_Divide\_16* Divide by 16.  
*kTPM\_Prescale\_Divide\_32* Divide by 32.  
*kTPM\_Prescale\_Divide\_64* Divide by 64.  
*kTPM\_Prescale\_Divide\_128* Divide by 128.

### 38.4.12 enum tpm\_interrupt\_enable\_t

Enumerator

*kTPM\_Chnl0InterruptEnable* Channel 0 interrupt.  
*kTPM\_Chnl1InterruptEnable* Channel 1 interrupt.  
*kTPM\_Chnl2InterruptEnable* Channel 2 interrupt.  
*kTPM\_Chnl3InterruptEnable* Channel 3 interrupt.  
*kTPM\_Chnl4InterruptEnable* Channel 4 interrupt.  
*kTPM\_Chnl5InterruptEnable* Channel 5 interrupt.  
*kTPM\_Chnl6InterruptEnable* Channel 6 interrupt.  
*kTPM\_Chnl7InterruptEnable* Channel 7 interrupt.  
*kTPM\_TimeOverflowInterruptEnable* Time overflow interrupt.

### 38.4.13 enum tpm\_status\_flags\_t

Enumerator

*kTPM\_Chnl0Flag* Channel 0 flag.  
*kTPM\_Chnl1Flag* Channel 1 flag.  
*kTPM\_Chnl2Flag* Channel 2 flag.  
*kTPM\_Chnl3Flag* Channel 3 flag.  
*kTPM\_Chnl4Flag* Channel 4 flag.  
*kTPM\_Chnl5Flag* Channel 5 flag.  
*kTPM\_Chnl6Flag* Channel 6 flag.  
*kTPM\_Chnl7Flag* Channel 7 flag.  
*kTPM\_TimeOverflowFlag* Time overflow flag.

## 38.5 Function Documentation

### 38.5.1 void TPM\_Init ( TPM\_Type \* *base*, const tpm\_config\_t \* *config* )

## Function Documentation

### Note

This API should be called at the beginning of the application using the TPM driver.

### Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | TPM peripheral base address             |
| <i>config</i> | Pointer to user's TPM config structure. |

### 38.5.2 void TPM\_Deinit ( TPM\_Type \* *base* )

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | TPM peripheral base address |
|-------------|-----------------------------|

### 38.5.3 void TPM\_GetDefaultConfig ( tpm\_config\_t \* *config* )

The default values are:

```
* config->prescale = kTPM_Prescale_Divide_1;
* config->useGlobalTimeBase = false;
* config->dozeEnable = false;
* config->dbgMode = false;
* config->enableReloadOnTrigger = false;
* config->enableStopOnOverflow = false;
* config->enableStartOnTrigger = false;
*#if FSL_FEATURE_TPM_HAS_PAUSE_COUNTER_ON_TRIGGER
* config->enablePauseOnTrigger = false;
*#endif
* config->triggerSelect = kTPM_Trigger_Select_0;
*#if FSL_FEATURE_TPM_HAS_EXTERNAL_TRIGGER_SELECTION
* config->triggerSource = kTPM_TriggerSource_External;
*#endif
*
```

### Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to user's TPM config structure. |
|---------------|-----------------------------------------|

### 38.5.4 status\_t TPM\_SetupPwm ( TPM\_Type \* *base*, const tpm\_chnl\_pwm\_signal\_param\_t \* *chnlParams*, uint8\_t *numOfChnls*, tpm\_pwm\_mode\_t *mode*, uint32\_t *pwmFreq\_Hz*, uint32\_t *srcClock\_Hz* )

User calls this function to configure the PWM signals period, mode, dutycycle and edge. Use this function to configure all the TPM channels that will be used to output a PWM signal

## Parameters

|                    |                                                                                     |
|--------------------|-------------------------------------------------------------------------------------|
| <i>base</i>        | TPM peripheral base address                                                         |
| <i>chnlParams</i>  | Array of PWM channel parameters to configure the channel(s)                         |
| <i>numOfChnls</i>  | Number of channels to configure, this should be the size of the array passed in     |
| <i>mode</i>        | PWM operation mode, options available in enumeration <a href="#">tpm_pwm_mode_t</a> |
| <i>pwmFreq_Hz</i>  | PWM signal frequency in Hz                                                          |
| <i>srcClock_Hz</i> | TPM counter clock in Hz                                                             |

## Returns

kStatus\_Success if the PWM setup was successful, kStatus\_Error on failure

### 38.5.5 void TPM\_UpdatePwmDutycycle ( TPM\_Type \* *base*, tpm\_chnl\_t *chnlNumber*, tpm\_pwm\_mode\_t *currentPwmMode*, uint8\_t *dutyCyclePercent* )

## Parameters

|                          |                                                                                                                               |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>              | TPM peripheral base address                                                                                                   |
| <i>chnlNumber</i>        | The channel number. In combined mode, this represents the channel pair number                                                 |
| <i>currentPwm-Mode</i>   | The current PWM mode set during PWM setup                                                                                     |
| <i>dutyCycle-Percent</i> | New PWM pulse width, value should be between 0 to 100 0=inactive signal(0% duty cycle)... 100=active signal (100% duty cycle) |

### 38.5.6 void TPM\_UpdateChnlEdgeLevelSelect ( TPM\_Type \* *base*, tpm\_chnl\_t *chnlNumber*, uint8\_t *level* )

## Parameters

|                   |                                                                                                                                                       |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | TPM peripheral base address                                                                                                                           |
| <i>chnlNumber</i> | The channel number                                                                                                                                    |
| <i>level</i>      | The level to be set to the ELSnB:ELSnA field; valid values are 00, 01, 10, 11. See the appropriate SoC reference manual for details about this field. |

### 38.5.7 void TPM\_SetupInputCapture ( TPM\_Type \* *base*, tpm\_chnl\_t *chnlNumber*, tpm\_input\_capture\_edge\_t *captureMode* )

When the edge specified in the captureMode argument occurs on the channel, the TPM counter is captured into the CnV register. The user has to read the CnV register separately to get this value.



## Parameters

|                    |                                 |
|--------------------|---------------------------------|
| <i>base</i>        | TPM peripheral base address     |
| <i>chnlNumber</i>  | The channel number              |
| <i>captureMode</i> | Specifies which edge to capture |

### 38.5.8 void TPM\_SetupOutputCompare ( TPM\_Type \* *base*, tpm\_chnl\_t *chnlNumber*, tpm\_output\_compare\_mode\_t *compareMode*, uint32\_t *compareValue* )

When the TPM counter matches the value of compareVal argument (this is written into CnV reg), the channel output is changed based on what is specified in the compareMode argument.

## Parameters

|                     |                                                                        |
|---------------------|------------------------------------------------------------------------|
| <i>base</i>         | TPM peripheral base address                                            |
| <i>chnlNumber</i>   | The channel number                                                     |
| <i>compareMode</i>  | Action to take on the channel output when the compare condition is met |
| <i>compareValue</i> | Value to be programmed in the CnV register.                            |

### 38.5.9 void TPM\_SetupDualEdgeCapture ( TPM\_Type \* *base*, tpm\_chnl\_t *chnlPairNumber*, const tpm\_dual\_edge\_capture\_param\_t \* *edgeParam*, uint32\_t *filterValue* )

This function allows to measure a pulse width of the signal on the input of channel of a channel pair. The filter function is disabled if the filterVal argument passed is zero.

## Parameters

|                        |                                                     |
|------------------------|-----------------------------------------------------|
| <i>base</i>            | TPM peripheral base address                         |
| <i>chnlPair-Number</i> | The TPM channel pair number; options are 0, 1, 2, 3 |
| <i>edgeParam</i>       | Sets up the dual edge capture function              |
| <i>filterValue</i>     | Filter value, specify 0 to disable filter.          |

**38.5.10** void TPM\_SetupQuadDecode ( TPM\_Type \* *base*, const tpm\_phase\_params\_t \* *phaseAParams*, const tpm\_phase\_params\_t \* *phaseBParams*, tpm\_quad\_decode\_mode\_t *quadMode* )

## Parameters

|                     |                                                       |
|---------------------|-------------------------------------------------------|
| <i>base</i>         | TPM peripheral base address                           |
| <i>phaseAParams</i> | Phase A configuration parameters                      |
| <i>phaseBParams</i> | Phase B configuration parameters                      |
| <i>quadMode</i>     | Selects encoding mode used in quadrature decoder mode |

**38.5.11 void TPM\_EnableInterrupts ( TPM\_Type \* *base*, uint32\_t *mask* )**

## Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | TPM peripheral base address                                                                                         |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">tpm_interrupt_enable_t</a> |

**38.5.12 void TPM\_DisableInterrupts ( TPM\_Type \* *base*, uint32\_t *mask* )**

## Parameters

|             |                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | TPM peripheral base address                                                                                          |
| <i>mask</i> | The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">tpm_interrupt_enable_t</a> |

**38.5.13 uint32\_t TPM\_GetEnabledInterrupts ( TPM\_Type \* *base* )**

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | TPM peripheral base address |
|-------------|-----------------------------|

## Returns

The enabled interrupts. This is the logical OR of members of the enumeration [tpm\\_interrupt\\_enable\\_t](#)

**38.5.14 static uint32\_t TPM\_GetStatusFlags ( TPM\_Type \* *base* ) [inline], [static]**

## Function Documentation

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | TPM peripheral base address |
|-------------|-----------------------------|

### Returns

The status flags. This is the logical OR of members of the enumeration [tpm\\_status\\_flags\\_t](#)

**38.5.15** `static void TPM_ClearStatusFlags ( TPM_Type * base, uint32_t mask )  
[inline], [static]`

### Parameters

|             |                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | TPM peripheral base address                                                                                      |
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">tpm_status_flags_t</a> |

**38.5.16** `static void TPM_StartTimer ( TPM_Type * base, tpm_clock_source_t  
clockSource ) [inline], [static]`

### Parameters

|                    |                                                                           |
|--------------------|---------------------------------------------------------------------------|
| <i>base</i>        | TPM peripheral base address                                               |
| <i>clockSource</i> | TPM clock source; once clock source is set the counter will start running |

**38.5.17** `static void TPM_StopTimer ( TPM_Type * base ) [inline], [static]`

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | TPM peripheral base address |
|-------------|-----------------------------|



## Chapter 39

# UART: Universal Asynchronous Receiver/Transmitter Driver

## 39.1 Overview

### Modules

- [UART DMA Driver](#)
- [UART Driver](#)
- [UART FreeRTOS Driver](#)
- [UART eDMA Driver](#)
- [UART  \$\mu\$ COS/II Driver](#)
- [UART  \$\mu\$ COS/III Driver](#)

### 39.2 UART Driver

#### 39.2.1 Overview

The KSDK provides a peripheral driver for the Universal Asynchronous Receiver/Transmitter (UART) module of Kinetis devices.

The UART driver includes functional APIs and transactional APIs.

Functional APIs are used for UART initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the UART peripheral and how to organize functional APIs to meet the application requirements. All functional APIs use the peripheral base address as the first parameter. UART functional operation groups provide the functional API set.

Transactional APIs can be used to enable the peripheral quickly and in the application if the code size and performance of transactional APIs can satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the `uart_handle_t` as the second parameter. Initialize the handle by calling the [UART\\_TransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer, which means that the functions [UART\\_TransferSendNonBlocking\(\)](#) and [UART\\_TransferReceiveNonBlocking\(\)](#) set up an interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_UART_TxIdle` and `kStatus_UART_RxIdle`.

Transactional receive APIs support the ring buffer. Prepare the memory for the ring buffer and pass in the start address and size while calling the [UART\\_TransferCreateHandle\(\)](#). If passing `NULL`, the ring buffer feature is disabled. When the ring buffer is enabled, the received data is saved to the ring buffer in the background. The [UART\\_TransferReceiveNonBlocking\(\)](#) function first gets data from the ring buffer. If the ring buffer does not have enough data, the function first returns the data in the ring buffer and then saves the received data to user memory. When all data is received, the upper layer is informed through a callback with the `kStatus_UART_RxIdle`.

If the receive ring buffer is full, the upper layer is informed through a callback with the `kStatus_UART_RxRingBufferOverflow`. In the callback function, the upper layer reads data out from the ring buffer. If not, existing data is overwritten by the new data.

The ring buffer size is specified when creating the handle. Note that one byte is reserved for the ring buffer maintenance. When creating handle using the following code.

```
UART_TransferCreateHandle(UART0, &handle, UART_UserCallback, NULL);
```

In this example, the buffer size is 32, but only 31 bytes are used for saving data.

#### 39.2.2 Typical use case

##### 39.2.2.1 UART Send/receive using a polling method

```
uint8_t ch;
```

```

UART_GetDefaultConfig(&user_config);
user_config.baudRate_Bps = 115200U;
user_config.enableTx = true;
user_config.enableRx = true;

UART_Init(UART1, &user_config, 120000000U);

while(1)
{
    UART_ReadBlocking(UART1, &ch, 1);
    UART_WriteBlocking(UART1, &ch, 1);
}

```

### 39.2.2.2 UART Send/receive using an interrupt method

```

uart_handle_t g_uartHandle;
uart_config_t user_config;
uart_transfer_t sendXfer;
uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t sendData[] = {'H', 'e', 'l', 'l', 'o'};
uint8_t receiveData[32];

void UART_UserCallback(uart_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_UART_TxIdle == status)
    {
        txFinished = true;
    }

    if (kStatus_UART_RxIdle == status)
    {
        rxFinished = true;
    }
}

void main(void)
{
    //...

    UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableTx = true;
    user_config.enableRx = true;

    UART_Init(UART1, &user_config, 120000000U);
    UART_TransferCreateHandle(UART1, &g_uartHandle, UART_UserCallback, NULL);

    // Prepare to send.
    sendXfer.data = sendData;
    sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
    txFinished = false;

    // Send out.
    UART_TransferSendNonBlocking(&g_uartHandle, &g_uartHandle, &sendXfer);

    // Wait send finished.
    while (!txFinished)
    {
    }

    // Prepare to receive.

```

## UART Driver

```
receiveXfer.data = receiveData;
receiveXfer.dataSize = sizeof(receiveData)/sizeof(receiveData[0]);
rxFinished = false;

// Receive.
UART_TransferReceiveNonBlocking(&g_uartHandle, &g_uartHandle, &
    receiveXfer);

// Wait receive finished.
while (!rxFinished)
{
}

// ...
}
```

### 39.2.2.3 UART Receive using the ringbuffer feature

```
#define RING_BUFFER_SIZE 64
#define RX_DATA_SIZE 32

uart_handle_t g_uartHandle;
uart_config_t user_config;
uart_transfer_t sendXfer;
uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t receiveData[RX_DATA_SIZE];
uint8_t ringBuffer[RING_BUFFER_SIZE];

void UART_UserCallback(uart_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_UART_RxIdle == status)
    {
        rxFinished = true;
    }
}

void main(void)
{
    size_t bytesRead;
    //...

    UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableTx = true;
    user_config.enableRx = true;

    UART_Init(UART1, &user_config, 120000000U);
    UART_TransferCreateHandle(UART1, &g_uartHandle, UART_UserCallback, NULL);

    // Now the RX is working in background, receive in to ring buffer.

    // Prepare to receive.
    receiveXfer.data = receiveData;
    receiveXfer.dataSize = RX_DATA_SIZE;
    rxFinished = false;

    // Receive.
    UART_TransferReceiveNonBlocking(UART1, &g_uartHandle, &receiveXfer);

    if (bytesRead = RX_DATA_SIZE) /* Have read enough data. */
    {
```



```

    ;
}
else
{
    if (bytesRead) /* Received some data, process first. */
    {
        ;
    }

    // Wait receive finished.
    while (!rxFinished)
    {
    }
}

// ...
}

```

### 39.2.2.4 UART Send/Receive using the DMA method

```

uart_handle_t g_uartHandle;
dma_handle_t g_uartTxDmaHandle;
dma_handle_t g_uartRxDmaHandle;
uart_config_t user_config;
uart_transfer_t sendXfer;
uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t sendData[] = {'H', 'e', 'l', 'l', 'o'};
uint8_t receiveData[32];

void UART_UserCallback(uart_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_UART_TxIdle == status)
    {
        txFinished = true;
    }

    if (kStatus_UART_RxIdle == status)
    {
        rxFinished = true;
    }
}

void main(void)
{
    //...

    UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableTx = true;
    user_config.enableRx = true;

    UART_Init(UART1, &user_config, 120000000U);

    // Set up the DMA
    DMAMUX_Init(DMAMUX0);
    DMAMUX_SetSource(DMAMUX0, UART_TX_DMA_CHANNEL, UART_TX_DMA_REQUEST);
    DMAMUX_EnableChannel(DMAMUX0, UART_TX_DMA_CHANNEL);
    DMAMUX_SetSource(DMAMUX0, UART_RX_DMA_CHANNEL, UART_RX_DMA_REQUEST);
    DMAMUX_EnableChannel(DMAMUX0, UART_RX_DMA_CHANNEL);

    DMA_Init(DMA0);

```

## UART Driver

```
/* Create DMA handle. */
DMA_CreateHandle(&g_uartTxDmaHandle, DMA0, UART_TX_DMA_CHANNEL);
DMA_CreateHandle(&g_uartRxDmaHandle, DMA0, UART_RX_DMA_CHANNEL);

UART_TransferCreateHandleDMA(UART1, &g_uartHandle, UART_UserCallback, NULL,
    &g_uartTxDmaHandle, &g_uartRxDmaHandle);

// Prepare to send.
sendXfer.data = sendData
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Send out.
UART_TransferSendDMA(UART1, &g_uartHandle, &sendXfer);

// Wait send finished.
while (!txFinished)
{
}

// Prepare to receive.
receiveXfer.data = receiveData;
receiveXfer.dataSize = sizeof(receiveData)/sizeof(receiveData[0]);
rxFinished = false;

// Receive.
UART_TransferReceiveDMA(UART1, &g_uartHandle, &receiveXfer);

// Wait receive finished.
while (!rxFinished)
{
}

// ...
}
```

## Data Structures

- struct `uart_config_t`  
*UART configuration structure. [More...](#)*
- struct `uart_transfer_t`  
*UART transfer structure. [More...](#)*
- struct `uart_handle_t`  
*UART handle structure. [More...](#)*

## Typedefs

- typedef void(\* `uart_transfer_callback_t`)(UART\_Type \*base, uart\_handle\_t \*handle, status\_t status, void \*userData)  
*UART transfer callback function.*

## Enumerations

- enum `_uart_status` {
  - `kStatus_UART_TxBusy` = MAKE\_STATUS(kStatusGroup\_UART, 0),
  - `kStatus_UART_RxBusy` = MAKE\_STATUS(kStatusGroup\_UART, 1),
  - `kStatus_UART_TxIdle` = MAKE\_STATUS(kStatusGroup\_UART, 2),
  - `kStatus_UART_RxIdle` = MAKE\_STATUS(kStatusGroup\_UART, 3),
  - `kStatus_UART_TxWatermarkTooLarge` = MAKE\_STATUS(kStatusGroup\_UART, 4),
  - `kStatus_UART_RxWatermarkTooLarge` = MAKE\_STATUS(kStatusGroup\_UART, 5),
  - `kStatus_UART_FlagCannotClearManually`,
  - `kStatus_UART_Error` = MAKE\_STATUS(kStatusGroup\_UART, 7),
  - `kStatus_UART_RxRingBufferOverrun` = MAKE\_STATUS(kStatusGroup\_UART, 8),
  - `kStatus_UART_RxHardwareOverrun` = MAKE\_STATUS(kStatusGroup\_UART, 9),
  - `kStatus_UART_NoiseError` = MAKE\_STATUS(kStatusGroup\_UART, 10),
  - `kStatus_UART_FramingError` = MAKE\_STATUS(kStatusGroup\_UART, 11),
  - `kStatus_UART_ParityError` = MAKE\_STATUS(kStatusGroup\_UART, 12),
  - `kStatus_UART_BaudrateNotSupport` }

*Error codes for the UART driver.*
- enum `uart_parity_mode_t` {
  - `kUART_ParityDisabled` = 0x0U,
  - `kUART_ParityEven` = 0x2U,
  - `kUART_ParityOdd` = 0x3U }

*UART parity mode.*
- enum `uart_stop_bit_count_t` {
  - `kUART_OneStopBit` = 0U,
  - `kUART_TwoStopBit` = 1U }

*UART stop bit count.*
- enum `_uart_interrupt_enable` {
  - `kUART_LinBreakInterruptEnable` = (UART\_BDH\_LBKDIE\_MASK),
  - `kUART_RxActiveEdgeInterruptEnable` = (UART\_BDH\_RXEDGIE\_MASK),
  - `kUART_TxDataRegEmptyInterruptEnable` = (UART\_C2\_TIE\_MASK << 8),
  - `kUART_TransmissionCompleteInterruptEnable` = (UART\_C2\_TCIE\_MASK << 8),
  - `kUART_RxDataRegFullInterruptEnable` = (UART\_C2\_RIE\_MASK << 8),
  - `kUART_IdleLineInterruptEnable` = (UART\_C2\_ILIE\_MASK << 8),
  - `kUART_RxOverrunInterruptEnable` = (UART\_C3\_ORIE\_MASK << 16),
  - `kUART_NoiseErrorInterruptEnable` = (UART\_C3\_NEIE\_MASK << 16),
  - `kUART_FramingErrorInterruptEnable` = (UART\_C3\_FEIE\_MASK << 16),
  - `kUART_ParityErrorInterruptEnable` = (UART\_C3\_PEIE\_MASK << 16),
  - `kUART_RxFifoOverflowInterruptEnable` = (UART\_CFIFO\_RXOFE\_MASK << 24),
  - `kUART_TxFifoOverflowInterruptEnable` = (UART\_CFIFO\_TXOFE\_MASK << 24),
  - `kUART_RxFifoUnderflowInterruptEnable` = (UART\_CFIFO\_RXUFE\_MASK << 24) }

*UART interrupt configuration structure, default settings all disabled.*
- enum `_uart_flags` {

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```
kUART_TxDataRegEmptyFlag = (UART_S1_TDRE_MASK),
kUART_TransmissionCompleteFlag = (UART_S1_TC_MASK),
kUART_RxDataRegFullFlag = (UART_S1_RDRF_MASK),
kUART_IdleLineFlag = (UART_S1_IDLE_MASK),
kUART_RxOverrunFlag = (UART_S1_OR_MASK),
kUART_NoiseErrorFlag = (UART_S1_NF_MASK),
kUART_FramingErrorFlag = (UART_S1_FE_MASK),
kUART_ParityErrorFlag = (UART_S1_PF_MASK),
kUART_LinBreakFlag,
kUART_RxActiveEdgeFlag,
kUART_RxActiveFlag,
kUART_NoiseErrorInRxDataRegFlag = (UART_ED_NOISY_MASK << 16),
kUART_ParityErrorInRxDataRegFlag = (UART_ED_PARITYE_MASK << 16),
kUART_TxFifoEmptyFlag = (UART_SFIFO_TXEMPT_MASK << 24),
kUART_RxFifoEmptyFlag = (UART_SFIFO_RXEMPT_MASK << 24),
kUART_TxFifoOverflowFlag = (UART_SFIFO_TXOF_MASK << 24),
kUART_RxFifoOverflowFlag = (UART_SFIFO_RXOF_MASK << 24),
kUART_RxFifoUnderflowFlag = (UART_SFIFO_RXUF_MASK << 24) }
UART status flags.
```

## Driver version

- #define **FSL\_UART\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 1, 4))  
*UART driver version 2.1.4.*

## Initialization and deinitialization

- status\_t **UART\_Init** (UART\_Type \*base, const **uart\_config\_t** \*config, uint32\_t srcClock\_Hz)  
*Initializes a UART instance with a user configuration structure and peripheral clock.*
- void **UART\_Deinit** (UART\_Type \*base)  
*Deinitializes a UART instance.*
- void **UART\_GetDefaultConfig** (**uart\_config\_t** \*config)  
*Gets the default configuration structure.*
- status\_t **UART\_SetBaudRate** (UART\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Sets the UART instance baud rate.*

## Status

- uint32\_t **UART\_GetStatusFlags** (UART\_Type \*base)  
*Gets UART status flags.*
- status\_t **UART\_ClearStatusFlags** (UART\_Type \*base, uint32\_t mask)  
*Clears status flags with the provided mask.*

## Interrupts

- void [UART\\_EnableInterrupts](#) (UART\_Type \*base, uint32\_t mask)  
*Enables UART interrupts according to the provided mask.*
- void [UART\\_DisableInterrupts](#) (UART\_Type \*base, uint32\_t mask)  
*Disables the UART interrupts according to the provided mask.*
- uint32\_t [UART\\_GetEnabledInterrupts](#) (UART\_Type \*base)  
*Gets the enabled UART interrupts.*

## DMA Control

- static uint32\_t [UART\\_GetDataRegisterAddress](#) (UART\_Type \*base)  
*Gets the UART data register address.*
- static void [UART\\_EnableTxDMA](#) (UART\_Type \*base, bool enable)  
*Enables or disables the UART transmitter DMA request.*
- static void [UART\\_EnableRxDMA](#) (UART\_Type \*base, bool enable)  
*Enables or disables the UART receiver DMA.*

## Bus Operations

- static void [UART\\_EnableTx](#) (UART\_Type \*base, bool enable)  
*Enables or disables the UART transmitter.*
- static void [UART\\_EnableRx](#) (UART\_Type \*base, bool enable)  
*Enables or disables the UART receiver.*
- static void [UART\\_WriteByte](#) (UART\_Type \*base, uint8\_t data)  
*Writes to the TX register.*
- static uint8\_t [UART\\_ReadByte](#) (UART\_Type \*base)  
*Reads the RX register directly.*
- void [UART\\_WriteBlocking](#) (UART\_Type \*base, const uint8\_t \*data, size\_t length)  
*Writes to the TX register using a blocking method.*
- status\_t [UART\\_ReadBlocking](#) (UART\_Type \*base, uint8\_t \*data, size\_t length)  
*Read RX data register using a blocking method.*

## Transactional

- void [UART\\_TransferCreateHandle](#) (UART\_Type \*base, uart\_handle\_t \*handle, [uart\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the UART handle.*
- void [UART\\_TransferStartRingBuffer](#) (UART\_Type \*base, uart\_handle\_t \*handle, uint8\_t \*ringBuffer, size\_t ringBufferSize)  
*Sets up the RX ring buffer.*
- void [UART\\_TransferStopRingBuffer](#) (UART\_Type \*base, uart\_handle\_t \*handle)  
*Aborts the background transfer and uninstalls the ring buffer.*
- status\_t [UART\\_TransferSendNonBlocking](#) (UART\_Type \*base, uart\_handle\_t \*handle, [uart\\_transfer\\_t](#) \*xfer)  
*Transmits a buffer of data using the interrupt method.*

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- void [UART\\_TransferAbortSend](#) (UART\_Type \*base, uart\_handle\_t \*handle)  
*Aborts the interrupt-driven data transmit.*
- status\_t [UART\\_TransferGetSendCount](#) (UART\_Type \*base, uart\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes written to the UART TX register.*
- status\_t [UART\\_TransferReceiveNonBlocking](#) (UART\_Type \*base, uart\_handle\_t \*handle, [uart\\_transfer\\_t](#) \*xfer, size\_t \*receivedBytes)  
*Receives a buffer of data using an interrupt method.*
- void [UART\\_TransferAbortReceive](#) (UART\_Type \*base, uart\_handle\_t \*handle)  
*Aborts the interrupt-driven data receiving.*
- status\_t [UART\\_TransferGetReceiveCount](#) (UART\_Type \*base, uart\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes that have been received.*
- void [UART\\_TransferHandleIRQ](#) (UART\_Type \*base, uart\_handle\_t \*handle)  
*UART IRQ handle function.*
- void [UART\\_TransferHandleErrorIRQ](#) (UART\_Type \*base, uart\_handle\_t \*handle)  
*UART Error IRQ handle function.*

### 39.2.3 Data Structure Documentation

#### 39.2.3.1 struct uart\_config\_t

##### Data Fields

- uint32\_t [baudRate\\_Bps](#)  
*UART baud rate.*
- [uart\\_parity\\_mode\\_t](#) [parityMode](#)  
*Parity mode, disabled (default), even, odd.*
- [uart\\_stop\\_bit\\_count\\_t](#) [stopBitCount](#)  
*Number of stop bits, 1 stop bit (default) or 2 stop bits.*
- uint8\_t [txFifoWatermark](#)  
*TX FIFO watermark.*
- uint8\_t [rxFifoWatermark](#)  
*RX FIFO watermark.*
- bool [enableTx](#)  
*Enable TX.*
- bool [enableRx](#)  
*Enable RX.*

#### 39.2.3.2 struct uart\_transfer\_t

##### Data Fields

- uint8\_t \* [data](#)  
*The buffer of data to be transfer.*
- size\_t [dataSize](#)  
*The byte count to be transfer.*

### 39.2.3.2.0.93 Field Documentation

39.2.3.2.0.93.1 `uint8_t* uart_transfer_t::data`

39.2.3.2.0.93.2 `size_t uart_transfer_t::dataSize`

### 39.2.3.3 `struct _uart_handle`

#### Data Fields

- `uint8_t *volatile txData`  
*Address of remaining data to send.*
- `volatile size_t txDataSize`  
*Size of the remaining data to send.*
- `size_t txDataSizeAll`  
*Size of the data to send out.*
- `uint8_t *volatile rxData`  
*Address of remaining data to receive.*
- `volatile size_t rxDataSize`  
*Size of the remaining data to receive.*
- `size_t rxDataSizeAll`  
*Size of the data to receive.*
- `uint8_t * rxRingBuffer`  
*Start address of the receiver ring buffer.*
- `size_t rxRingBufferSize`  
*Size of the ring buffer.*
- `volatile uint16_t rxRingBufferHead`  
*Index for the driver to store received data into ring buffer.*
- `volatile uint16_t rxRingBufferTail`  
*Index for the user to get data from the ring buffer.*
- `uart_transfer_callback_t callback`  
*Callback function.*
- `void * userData`  
*UART callback function parameter.*
- `volatile uint8_t txState`  
*TX transfer state.*
- `volatile uint8_t rxState`  
*RX transfer state.*

## UART Driver

### 39.2.3.3.0.94 Field Documentation

- 39.2.3.3.0.94.1 `uint8_t* volatile uart_handle_t::txData`
- 39.2.3.3.0.94.2 `volatile size_t uart_handle_t::txDataSize`
- 39.2.3.3.0.94.3 `size_t uart_handle_t::txDataSizeAll`
- 39.2.3.3.0.94.4 `uint8_t* volatile uart_handle_t::rxData`
- 39.2.3.3.0.94.5 `volatile size_t uart_handle_t::rxDataSize`
- 39.2.3.3.0.94.6 `size_t uart_handle_t::rxDataSizeAll`
- 39.2.3.3.0.94.7 `uint8_t* uart_handle_t::rxRingBuffer`
- 39.2.3.3.0.94.8 `size_t uart_handle_t::rxRingBufferSize`
- 39.2.3.3.0.94.9 `volatile uint16_t uart_handle_t::rxRingBufferHead`
- 39.2.3.3.0.94.10 `volatile uint16_t uart_handle_t::rxRingBufferTail`
- 39.2.3.3.0.94.11 `uart_transfer_callback_t uart_handle_t::callback`
- 39.2.3.3.0.94.12 `void* uart_handle_t::userData`
- 39.2.3.3.0.94.13 `volatile uint8_t uart_handle_t::txState`

### 39.2.4 Macro Definition Documentation

- 39.2.4.1 `#define FSL_UART_DRIVER_VERSION (MAKE_VERSION(2, 1, 4))`

### 39.2.5 Typedef Documentation

- 39.2.5.1 `typedef void(* uart_transfer_callback_t)(UART_Type *base, uart_handle_t *handle, status_t status, void *userData)`

### 39.2.6 Enumeration Type Documentation

#### 39.2.6.1 `enum _uart_status`

Enumerator

- kStatus\_UART\_TxBusy* Transmitter is busy.
- kStatus\_UART\_RxBusy* Receiver is busy.
- kStatus\_UART\_TxIdle* UART transmitter is idle.
- kStatus\_UART\_RxIdle* UART receiver is idle.
- kStatus\_UART\_TxWatermarkTooLarge* TX FIFO watermark too large.



*kStatus\_UART\_RxWatermarkTooLarge* RX FIFO watermark too large.  
*kStatus\_UART\_FlagCannotClearManually* UART flag can't be manually cleared.  
*kStatus\_UART\_Error* Error happens on UART.  
*kStatus\_UART\_RxRingBufferOverflow* UART RX software ring buffer overrun.  
*kStatus\_UART\_RxHardwareOverflow* UART RX receiver overrun.  
*kStatus\_UART\_NoiseError* UART noise error.  
*kStatus\_UART\_FramingError* UART framing error.  
*kStatus\_UART\_ParityError* UART parity error.  
*kStatus\_UART\_BaudrateNotSupport* Baudrate is not support in current clock source.

### 39.2.6.2 enum uart\_parity\_mode\_t

Enumerator

*kUART\_ParityDisabled* Parity disabled.  
*kUART\_ParityEven* Parity enabled, type even, bit setting: PE|PT = 10.  
*kUART\_ParityOdd* Parity enabled, type odd, bit setting: PE|PT = 11.

### 39.2.6.3 enum uart\_stop\_bit\_count\_t

Enumerator

*kUART\_OneStopBit* One stop bit.  
*kUART\_TwoStopBit* Two stop bits.

### 39.2.6.4 enum \_uart\_interrupt\_enable

This structure contains the settings for all of the UART interrupt configurations.

Enumerator

*kUART\_LinBreakInterruptEnable* LIN break detect interrupt.  
*kUART\_RxActiveEdgeInterruptEnable* RX active edge interrupt.  
*kUART\_TxDataRegEmptyInterruptEnable* Transmit data register empty interrupt.  
*kUART\_TransmissionCompleteInterruptEnable* Transmission complete interrupt.  
*kUART\_RxDataRegFullInterruptEnable* Receiver data register full interrupt.  
*kUART\_IdleLineInterruptEnable* Idle line interrupt.  
*kUART\_RxOverflowInterruptEnable* Receiver overrun interrupt.  
*kUART\_NoiseErrorInterruptEnable* Noise error flag interrupt.  
*kUART\_FramingErrorInterruptEnable* Framing error flag interrupt.  
*kUART\_ParityErrorInterruptEnable* Parity error flag interrupt.  
*kUART\_RxFifoOverflowInterruptEnable* RX FIFO overflow interrupt.  
*kUART\_TxFifoOverflowInterruptEnable* TX FIFO overflow interrupt.  
*kUART\_RxFifoUnderflowInterruptEnable* RX FIFO underflow interrupt.

## UART Driver

### 39.2.6.5 enum \_uart\_flags

This provides constants for the UART status flags for use in the UART functions.

Enumerator

***kUART\_TxDataRegEmptyFlag*** TX data register empty flag.  
***kUART\_TransmissionCompleteFlag*** Transmission complete flag.  
***kUART\_RxDataRegFullFlag*** RX data register full flag.  
***kUART\_IdleLineFlag*** Idle line detect flag.  
***kUART\_RxOverrunFlag*** RX overrun flag.  
***kUART\_NoiseErrorFlag*** RX takes 3 samples of each received bit. If any of these samples differ, noise flag sets  
***kUART\_FramingErrorFlag*** Frame error flag, sets if logic 0 was detected where stop bit expected.  
***kUART\_ParityErrorFlag*** If parity enabled, sets upon parity error detection.  
***kUART\_LinBreakFlag*** LIN break detect interrupt flag, sets when LIN break char detected and LIN circuit enabled.  
***kUART\_RxActiveEdgeFlag*** RX pin active edge interrupt flag, sets when active edge detected.  
***kUART\_RxActiveFlag*** Receiver Active Flag (RAF), sets at beginning of valid start bit.  
***kUART\_NoiseErrorInRxDataRegFlag*** Noisy bit, sets if noise detected.  
***kUART\_ParityErrorInRxDataRegFlag*** Parity bit, sets if parity error detected.  
***kUART\_TxFifoEmptyFlag*** TXEMPTY bit, sets if TX buffer is empty.  
***kUART\_RxFifoEmptyFlag*** RXEMPTY bit, sets if RX buffer is empty.  
***kUART\_TxFifoOverflowFlag*** TXOF bit, sets if TX buffer overflow occurred.  
***kUART\_RxFifoOverflowFlag*** RXOF bit, sets if receive buffer overflow.  
***kUART\_RxFifoUnderflowFlag*** RXUF bit, sets if receive buffer underflow.

### 39.2.7 Function Documentation

#### 39.2.7.1 status\_t UART\_Init ( UART\_Type \* *base*, const uart\_config\_t \* *config*, uint32\_t *srcClock\_Hz* )

This function configures the UART module with the user-defined settings. The user can configure the configuration structure and also get the default configuration by using the [UART\\_GetDefaultConfig\(\)](#) function. The example below shows how to use this API to configure UART.

```
* uart_config_t uartConfig;  
* uartConfig.baudRate_Bps = 115200U;  
* uartConfig.parityMode = kUART_ParityDisabled;  
* uartConfig.stopBitCount = kUART_OneStopBit;  
* uartConfig.txFifoWatermark = 0;  
* uartConfig.rxFifoWatermark = 1;  
* UART_Init(UART1, &uartConfig, 20000000U);  
*
```

## Parameters

|                    |                                                      |
|--------------------|------------------------------------------------------|
| <i>base</i>        | UART peripheral base address.                        |
| <i>config</i>      | Pointer to the user-defined configuration structure. |
| <i>srcClock_Hz</i> | UART clock source frequency in HZ.                   |

## Return values

|                                         |                                                  |
|-----------------------------------------|--------------------------------------------------|
| <i>kStatus_UART_Baudrate-NotSupport</i> | Baudrate is not support in current clock source. |
| <i>kStatus_Success</i>                  | Status UART initialize succeed                   |

**39.2.7.2 void UART\_Deinit ( UART\_Type \* *base* )**

This function waits for TX complete, disables TX and RX, and disables the UART clock.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

**39.2.7.3 void UART\_GetDefaultConfig ( uart\_config\_t \* *config* )**

This function initializes the UART configuration structure to a default value. The default values are as follows. `uartConfig->baudRate_Bps = 115200U`; `uartConfig->bitCountPerChar = kUART_8BitsPerChar`; `uartConfig->parityMode = kUART_ParityDisabled`; `uartConfig->stopBitCount = kUART_OneStopBit`; `uartConfig->txFifoWatermark = 0`; `uartConfig->rxFifoWatermark = 1`; `uartConfig->enableTx = false`; `uartConfig->enableRx = false`;

## Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>config</i> | Pointer to configuration structure. |
|---------------|-------------------------------------|

**39.2.7.4 status\_t UART\_SetBaudRate ( UART\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClock\_Hz* )**

This function configures the UART module baud rate. This function is used to update the UART module baud rate after the UART module is initialized by the `UART_Init`.

```
* UART_SetBaudRate(UART1, 115200U, 200000000U);
*
```

## UART Driver

### Parameters

|                     |                                    |
|---------------------|------------------------------------|
| <i>base</i>         | UART peripheral base address.      |
| <i>baudRate_Bps</i> | UART baudrate to be set.           |
| <i>srcClock_Hz</i>  | UART clock source frequency in Hz. |

### Return values

|                                         |                                                      |
|-----------------------------------------|------------------------------------------------------|
| <i>kStatus_UART_Baudrate-NotSupport</i> | Baudrate is not support in the current clock source. |
| <i>kStatus_Success</i>                  | Set baudrate succeeded.                              |

### 39.2.7.5 uint32\_t UART\_GetStatusFlags ( UART\_Type \* *base* )

This function gets all UART status flags. The flags are returned as the logical OR value of the enumerators [\\_uart\\_flags](#). To check a specific status, compare the return value with enumerators in [\\_uart\\_flags](#). For example, to check whether the TX is empty, do the following.

```
*      if (kUART_TxDataRegEmptyFlag & UART_GetStatusFlags(UART1))
*      {
*          ...
*      }
*
```

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

### Returns

UART status flags which are ORed by the enumerators in the [\\_uart\\_flags](#).

### 39.2.7.6 status\_t UART\_ClearStatusFlags ( UART\_Type \* *base*, uint32\_t *mask* )

This function clears UART status flags with a provided mask. An automatically cleared flag can't be cleared by this function. These flags can only be cleared or set by hardware. kUART\_TxDataRegEmptyFlag, kUART\_TransmissionCompleteFlag, kUART\_RxDataRegFullFlag, kUART\_RxActiveFlag, kUART\_NoiseErrorInRxDataRegFlag, kUART\_ParityErrorInRxDataRegFlag, kUART\_TxFifoEmptyFlag, kUART\_RxFifoEmptyFlag Note that this API should be called when the Tx/Rx is idle. Otherwise it has no effect.

## Parameters

|             |                                                                                         |
|-------------|-----------------------------------------------------------------------------------------|
| <i>base</i> | UART peripheral base address.                                                           |
| <i>mask</i> | The status flags to be cleared; it is logical OR value of <a href="#">_uart_flags</a> . |

## Return values

|                                                   |                                                                                         |
|---------------------------------------------------|-----------------------------------------------------------------------------------------|
| <i>kStatus_UART_Flag-<br/>CannotClearManually</i> | The flag can't be cleared by this function but it is cleared automatically by hardware. |
| <i>kStatus_Success</i>                            | Status in the mask is cleared.                                                          |

### 39.2.7.7 void UART\_EnableInterrupts ( UART\_Type \* *base*, uint32\_t *mask* )

This function enables the UART interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [\\_uart\\_interrupt\\_enable](#). For example, to enable TX empty interrupt and RX full interrupt, do the following.

```
*  UART_EnableInterrupts(UART1,
    kUART_TxDataRegEmptyInterruptEnable |
    kUART_RxDataRegFullInterruptEnable);
*
```

## Parameters

|             |                                                                                  |
|-------------|----------------------------------------------------------------------------------|
| <i>base</i> | UART peripheral base address.                                                    |
| <i>mask</i> | The interrupts to enable. Logical OR of <a href="#">_uart_interrupt_enable</a> . |

### 39.2.7.8 void UART\_DisableInterrupts ( UART\_Type \* *base*, uint32\_t *mask* )

This function disables the UART interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [\\_uart\\_interrupt\\_enable](#). For example, to disable TX empty interrupt and RX full interrupt do the following.

```
*  UART_DisableInterrupts(UART1,
    kUART_TxDataRegEmptyInterruptEnable |
    kUART_RxDataRegFullInterruptEnable);
*
```

## UART Driver

### Parameters

|             |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| <i>base</i> | UART peripheral base address.                                                     |
| <i>mask</i> | The interrupts to disable. Logical OR of <a href="#">_uart_interrupt_enable</a> . |

### 39.2.7.9 uint32\_t UART\_GetEnabledInterrupts ( UART\_Type \* *base* )

This function gets the enabled UART interrupts. The enabled interrupts are returned as the logical OR value of the enumerators [\\_uart\\_interrupt\\_enable](#). To check a specific interrupts enable status, compare the return value with enumerators in [\\_uart\\_interrupt\\_enable](#). For example, to check whether TX empty interrupt is enabled, do the following.

```
*      uint32_t enabledInterrupts = UART_GetEnabledInterrupts(UART1);
*
*      if (kUART_TxDataRegEmptyInterruptEnable & enabledInterrupts)
*      {
*          ...
*      }
*
```

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

### Returns

UART interrupt flags which are logical OR of the enumerators in [\\_uart\\_interrupt\\_enable](#).

### 39.2.7.10 static uint32\_t UART\_GetDataRegisterAddress ( UART\_Type \* *base* ) [inline], [static]

This function returns the UART data register address, which is mainly used by DMA/eDMA.

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

### Returns

UART data register addresses which are used both by the transmitter and the receiver.

### 39.2.7.11 static void UART\_EnableTxDMA ( UART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the transmit data register empty flag, S1[TDRE], to generate the DMA requests.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

### 39.2.7.12 static void UART\_EnableRxDMA ( UART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the receiver data register full flag, S1[RDRF], to generate DMA requests.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

### 39.2.7.13 static void UART\_EnableTx ( UART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the UART transmitter.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

### 39.2.7.14 static void UART\_EnableRx ( UART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the UART receiver.

## Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

### 39.2.7.15 static void UART\_WriteByte ( UART\_Type \* *base*, uint8\_t *data* ) [inline], [static]

This function writes data to the TX register directly. The upper layer must ensure that the TX register is empty or TX FIFO has empty room before calling this function.

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### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
| <i>data</i> | The byte to write.            |

### 39.2.7.16 static uint8\_t UART\_ReadByte ( UART\_Type \* *base* ) [inline], [static]

This function reads data from the TX register directly. The upper layer must ensure that the RX register is full or that the TX FIFO has data before calling this function.

### Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

### Returns

The byte read from UART data register.

### 39.2.7.17 void UART\_WriteBlocking ( UART\_Type \* *base*, const uint8\_t \* *data*, size\_t *length* )

This function polls the TX register, waits for the TX register to be empty or for the TX FIFO to have room and writes data to the TX buffer.

### Note

This function does not check whether all data is sent out to the bus. Before disabling the TX, check kUART\_TransmissionCompleteFlag to ensure that the TX is finished.

### Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | UART peripheral base address.       |
| <i>data</i>   | Start address of the data to write. |
| <i>length</i> | Size of the data to write.          |

### 39.2.7.18 status\_t UART\_ReadBlocking ( UART\_Type \* *base*, uint8\_t \* *data*, size\_t *length* )

This function polls the RX register, waits for the RX register to be full or for RX FIFO to have data, and reads data from the TX register.



## Parameters

|               |                                                         |
|---------------|---------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                           |
| <i>data</i>   | Start address of the buffer to store the received data. |
| <i>length</i> | Size of the buffer.                                     |

## Return values

|                                        |                                                 |
|----------------------------------------|-------------------------------------------------|
| <i>kStatus_UART_Rx-HardwareOverrun</i> | Receiver overrun occurred while receiving data. |
| <i>kStatus_UART_Noise-Error</i>        | A noise error occurred while receiving data.    |
| <i>kStatus_UART_Framing-Error</i>      | A framing error occurred while receiving data.  |
| <i>kStatus_UART_Parity-Error</i>       | A parity error occurred while receiving data.   |
| <i>kStatus_Success</i>                 | Successfully received all data.                 |

### 39.2.7.19 void UART\_TransferCreateHandle ( UART\_Type \* *base*, uart\_handle\_t \* *handle*, uart\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the UART handle which can be used for other UART transactional APIs. Usually, for a specified UART instance, call this API once to get the initialized handle.

## Parameters

|                 |                                         |
|-----------------|-----------------------------------------|
| <i>base</i>     | UART peripheral base address.           |
| <i>handle</i>   | UART handle pointer.                    |
| <i>callback</i> | The callback function.                  |
| <i>userData</i> | The parameter of the callback function. |

### 39.2.7.20 void UART\_TransferStartRingBuffer ( UART\_Type \* *base*, uart\_handle\_t \* *handle*, uint8\_t \* *ringBuffer*, size\_t *ringBufferSize* )

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received are stored into the ring buffer even when the user doesn't call the [UART\\_TransferReceiveNonBlocking\(\)](#) API. If data is already received in the ring buffer, the user can get the received data from the ring buffer directly.

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### Note

When using the RX ring buffer, one byte is reserved for internal use. In other words, if `ringBufferSize` is 32, only 31 bytes are used for saving data.

### Parameters

|                       |                                                                                                  |
|-----------------------|--------------------------------------------------------------------------------------------------|
| <i>base</i>           | UART peripheral base address.                                                                    |
| <i>handle</i>         | UART handle pointer.                                                                             |
| <i>ringBuffer</i>     | Start address of the ring buffer for background receiving. Pass NULL to disable the ring buffer. |
| <i>ringBufferSize</i> | Size of the ring buffer.                                                                         |

#### 39.2.7.21 `void UART_TransferStopRingBuffer ( UART_Type * base, uart_handle_t * handle )`

This function aborts the background transfer and uninstalls the ring buffer.

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

#### 39.2.7.22 `status_t UART_TransferSendNonBlocking ( UART_Type * base, uart_handle_t * handle, uart_transfer_t * xfer )`

This function sends data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data to be written to the TX register. When all data is written to the TX register in the ISR, the UART driver calls the callback function and passes the [kStatus\\_UART\\_TxIdle](#) as status parameter.

### Note

The `kStatus_UART_TxIdle` is passed to the upper layer when all data is written to the TX register. However, it does not ensure that all data is sent out. Before disabling the TX, check the `kUART_TransmissionCompleteFlag` to ensure that the TX is finished.

## Parameters

|               |                                                                |
|---------------|----------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                  |
| <i>handle</i> | UART handle pointer.                                           |
| <i>xfer</i>   | UART transfer structure. See <a href="#">uart_transfer_t</a> . |

## Return values

|                                |                                                                                    |
|--------------------------------|------------------------------------------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully start the data transmission.                                          |
| <i>kStatus_UART_TxBusy</i>     | Previous transmission still not finished; data not all written to TX register yet. |
| <i>kStatus_InvalidArgument</i> | Invalid argument.                                                                  |

**39.2.7.23 void UART\_TransferAbortSend ( UART\_Type \* *base*, uart\_handle\_t \* *handle* )**

This function aborts the interrupt-driven data sending. The user can get the remainBytes to find out how many bytes are not sent out.

## Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

**39.2.7.24 status\_t UART\_TransferGetSendCount ( UART\_Type \* *base*, uart\_handle\_t \* *handle*, uint32\_t \* *count* )**

This function gets the number of bytes written to the UART TX register by using the interrupt method.

## Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Send bytes count.             |

## Return values

|                                     |                                                       |
|-------------------------------------|-------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No send in progress.                                  |
| <i>kStatus_InvalidArgument</i>      | The parameter is invalid.                             |
| <i>kStatus_Success</i>              | Get successfully through the parameter <i>count</i> ; |

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### 39.2.7.25 **status\_t UART\_TransferReceiveNonBlocking ( UART\_Type \* *base*, uart\_handle\_t \* *handle*, uart\_transfer\_t \* *xfer*, size\_t \* *receivedBytes* )**

This function receives data using an interrupt method. This is a non-blocking function, which returns without waiting for all data to be received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter *receivedBytes* shows how many bytes are copied from the ring buffer. After copying, if the data in the ring buffer is not enough to read, the receive request is saved by the UART driver. When the new data arrives, the receive request is serviced first. When all data is received, the UART driver notifies the upper layer through a callback function and passes the status parameter [kStatus\\_UART\\_RxIdle](#). For example, the upper layer needs 10 bytes but there are only 5 bytes in the ring buffer. The 5 bytes are copied to the *xfer->data* and this function returns with the parameter *receivedBytes* set to 5. For the left 5 bytes, newly arrived data is saved from the *xfer->data[5]*. When 5 bytes are received, the UART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to the *xfer->data*. When all data is received, the upper layer is notified.

#### Parameters

|                      |                                                                |
|----------------------|----------------------------------------------------------------|
| <i>base</i>          | UART peripheral base address.                                  |
| <i>handle</i>        | UART handle pointer.                                           |
| <i>xfer</i>          | UART transfer structure, see <a href="#">uart_transfer_t</a> . |
| <i>receivedBytes</i> | Bytes received from the ring buffer directly.                  |

#### Return values

|                                |                                                      |
|--------------------------------|------------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully queue the transfer into transmit queue. |
| <i>kStatus_UART_RxBusy</i>     | Previous receive request is not finished.            |
| <i>kStatus_InvalidArgument</i> | Invalid argument.                                    |

### 39.2.7.26 **void UART\_TransferAbortReceive ( UART\_Type \* *base*, uart\_handle\_t \* *handle* )**

This function aborts the interrupt-driven data receiving. The user can get the *remainBytes* to know how many bytes are not received yet.

#### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

**39.2.7.27** `status_t UART_TransferGetReceiveCount ( UART_Type * base, uart_handle_t * handle, uint32_t * count )`

This function gets the number of bytes that have been received.

## UART Driver

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Receive bytes count.          |

### Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No receive in progress.                                     |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

### 39.2.7.28 void UART\_TransferHandleIRQ ( UART\_Type \* *base*, uart\_handle\_t \* *handle* )

This function handles the UART transmit and receive IRQ request.

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

### 39.2.7.29 void UART\_TransferHandleErrorIRQ ( UART\_Type \* *base*, uart\_handle\_t \* *handle* )

This function handles the UART error IRQ request.

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

## 39.3 UART DMA Driver

### 39.3.1 Overview

#### Data Structures

- struct [uart\\_dma\\_handle\\_t](#)  
UART DMA handle. [More...](#)

#### Typedefs

- typedef void(\* [uart\\_dma\\_transfer\\_callback\\_t](#))(UART\_Type \*base, uart\_dma\_handle\_t \*handle, status\_t status, void \*userData)  
UART transfer callback function.

#### eDMA transactional

- void [UART\\_TransferCreateHandleDMA](#) (UART\_Type \*base, uart\_dma\_handle\_t \*handle, [uart\\_dma\\_transfer\\_callback\\_t](#) callback, void \*userData, dma\_handle\_t \*txDmaHandle, dma\_handle\_t \*rxDmaHandle)  
*Initializes the UART handle which is used in transactional functions and sets the callback.*
- status\_t [UART\\_TransferSendDMA](#) (UART\_Type \*base, uart\_dma\_handle\_t \*handle, [uart\\_transfer\\_t](#) \*xfer)  
*Sends data using DMA.*
- status\_t [UART\\_TransferReceiveDMA](#) (UART\_Type \*base, uart\_dma\_handle\_t \*handle, [uart\\_transfer\\_t](#) \*xfer)  
*Receives data using DMA.*
- void [UART\\_TransferAbortSendDMA](#) (UART\_Type \*base, uart\_dma\_handle\_t \*handle)  
*Aborts the send data using DMA.*
- void [UART\\_TransferAbortReceiveDMA](#) (UART\_Type \*base, uart\_dma\_handle\_t \*handle)  
*Aborts the received data using DMA.*
- status\_t [UART\\_TransferGetSendCountDMA](#) (UART\_Type \*base, uart\_dma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes written to UART TX register.*
- status\_t [UART\\_TransferGetReceiveCountDMA](#) (UART\_Type \*base, uart\_dma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes that have been received.*

### 39.3.2 Data Structure Documentation

#### 39.3.2.1 struct \_uart\_dma\_handle

##### Data Fields

- UART\_Type \* [base](#)

## UART DMA Driver

- UART peripheral base address.*
- [uart\\_dma\\_transfer\\_callback\\_t](#) *callback*  
*Callback function.*
- void \* [userData](#)  
*UART callback function parameter.*
- size\_t [rxDataSizeAll](#)  
*Size of the data to receive.*
- size\_t [txDataSizeAll](#)  
*Size of the data to send out.*
- dma\_handle\_t \* [txDmaHandle](#)  
*The DMA TX channel used.*
- dma\_handle\_t \* [rxDmaHandle](#)  
*The DMA RX channel used.*
- volatile uint8\_t [txState](#)  
*TX transfer state.*
- volatile uint8\_t [rxState](#)  
*RX transfer state.*

### 39.3.2.1.0.95 Field Documentation

39.3.2.1.0.95.1 **UART\_Type\* uart\_dma\_handle\_t::base**

39.3.2.1.0.95.2 **uart\_dma\_transfer\_callback\_t uart\_dma\_handle\_t::callback**

39.3.2.1.0.95.3 **void\* uart\_dma\_handle\_t::userData**

39.3.2.1.0.95.4 **size\_t uart\_dma\_handle\_t::rxDataSizeAll**

39.3.2.1.0.95.5 **size\_t uart\_dma\_handle\_t::txDataSizeAll**

39.3.2.1.0.95.6 **dma\_handle\_t\* uart\_dma\_handle\_t::txDmaHandle**

39.3.2.1.0.95.7 **dma\_handle\_t\* uart\_dma\_handle\_t::rxDmaHandle**

39.3.2.1.0.95.8 **volatile uint8\_t uart\_dma\_handle\_t::txState**

### 39.3.3 Typedef Documentation

39.3.3.1 **typedef void(\* uart\_dma\_transfer\_callback\_t)(UART\_Type \*base,  
uart\_dma\_handle\_t \*handle, status\_t status, void \*userData)**

### 39.3.4 Function Documentation

39.3.4.1 **void UART\_TransferCreateHandleDMA ( UART\_Type \* base, uart\_dma\_handle\_t  
\* handle, uart\_dma\_transfer\_callback\_t callback, void \* userData,  
dma\_handle\_t \* txDmaHandle, dma\_handle\_t \* rxDmaHandle )**



## Parameters

|                    |                                                          |
|--------------------|----------------------------------------------------------|
| <i>base</i>        | UART peripheral base address.                            |
| <i>handle</i>      | Pointer to the <code>uart_dma_handle_t</code> structure. |
| <i>callback</i>    | UART callback, NULL means no callback.                   |
| <i>userData</i>    | User callback function data.                             |
| <i>rxDmaHandle</i> | User requested DMA handle for the RX DMA transfer.       |
| <i>txDmaHandle</i> | User requested DMA handle for the TX DMA transfer.       |

### 39.3.4.2 **status\_t UART\_TransferSendDMA ( UART\_Type \* *base*, uart\_dma\_handle\_t \* *handle*, uart\_transfer\_t \* *xfer* )**

This function sends data using DMA. This is non-blocking function, which returns right away. When all data is sent, the send callback function is called.

## Parameters

|               |                                                                    |
|---------------|--------------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                      |
| <i>handle</i> | UART handle pointer.                                               |
| <i>xfer</i>   | UART DMA transfer structure. See <a href="#">uart_transfer_t</a> . |

## Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | if succeeded; otherwise failed. |
| <i>kStatus_UART_TxBusy</i>     | Previous transfer ongoing.      |
| <i>kStatus_InvalidArgument</i> | Invalid argument.               |

### 39.3.4.3 **status\_t UART\_TransferReceiveDMA ( UART\_Type \* *base*, uart\_dma\_handle\_t \* *handle*, uart\_transfer\_t \* *xfer* )**

This function receives data using DMA. This is non-blocking function, which returns right away. When all data is received, the receive callback function is called.

## Parameters

---

## UART DMA Driver

|               |                                                                    |
|---------------|--------------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                      |
| <i>handle</i> | Pointer to the <code>uart_dma_handle_t</code> structure.           |
| <i>xfer</i>   | UART DMA transfer structure. See <a href="#">uart_transfer_t</a> . |

Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | if succeeded; otherwise failed. |
| <i>kStatus_UART_RxBusy</i>     | Previous transfer on going.     |
| <i>kStatus_InvalidArgument</i> | Invalid argument.               |

### 39.3.4.4 void UART\_TransferAbortSendDMA ( UART\_Type \* *base*, `uart_dma_handle_t` \* *handle* )

This function aborts the sent data using DMA.

Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                        |
| <i>handle</i> | Pointer to <code>uart_dma_handle_t</code> structure. |

### 39.3.4.5 void UART\_TransferAbortReceiveDMA ( UART\_Type \* *base*, `uart_dma_handle_t` \* *handle* )

This function abort receive data which using DMA.

Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                        |
| <i>handle</i> | Pointer to <code>uart_dma_handle_t</code> structure. |

### 39.3.4.6 `status_t` UART\_TransferGetSendCountDMA ( UART\_Type \* *base*, `uart_dma_handle_t` \* *handle*, `uint32_t` \* *count* )

This function gets the number of bytes written to UART TX register by DMA.

## Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Send bytes count.             |

## Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No send in progress.                                        |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

### 39.3.4.7 **status\_t** UART\_TransferGetReceiveCountDMA ( **UART\_Type** \* *base*, **uart\_dma\_handle\_t** \* *handle*, **uint32\_t** \* *count* )

This function gets the number of bytes that have been received.

## Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Receive bytes count.          |

## Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No receive in progress.                                     |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

### 39.4 UART eDMA Driver

#### 39.4.1 Overview

##### Data Structures

- struct [uart\\_edma\\_handle\\_t](#)  
*UART eDMA handle. [More...](#)*

##### Typedefs

- typedef void(\* [uart\\_edma\\_transfer\\_callback\\_t](#))(UART\_Type \*base, uart\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*UART transfer callback function.*

##### eDMA transactional

- void [UART\\_TransferCreateHandleEDMA](#) (UART\_Type \*base, uart\_edma\_handle\_t \*handle, [uart\\_edma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*txEdmaHandle, [edma\\_handle\\_t](#) \*rxEdmaHandle)  
*Initializes the UART handle which is used in transactional functions.*
- status\_t [UART\\_SendEDMA](#) (UART\_Type \*base, uart\_edma\_handle\_t \*handle, [uart\\_transfer\\_t](#) \*xfer)  
*Sends data using eDMA.*
- status\_t [UART\\_ReceiveEDMA](#) (UART\_Type \*base, uart\_edma\_handle\_t \*handle, [uart\\_transfer\\_t](#) \*xfer)  
*Receives data using eDMA.*
- void [UART\\_TransferAbortSendEDMA](#) (UART\_Type \*base, uart\_edma\_handle\_t \*handle)  
*Aborts the sent data using eDMA.*
- void [UART\\_TransferAbortReceiveEDMA](#) (UART\_Type \*base, uart\_edma\_handle\_t \*handle)  
*Aborts the receive data using eDMA.*
- status\_t [UART\\_TransferGetSendCountEDMA](#) (UART\_Type \*base, uart\_edma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes that have been written to UART TX register.*
- status\_t [UART\\_TransferGetReceiveCountEDMA](#) (UART\_Type \*base, uart\_edma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of received bytes.*

#### 39.4.2 Data Structure Documentation

##### 39.4.2.1 struct \_uart\_edma\_handle

##### Data Fields

- [uart\\_edma\\_transfer\\_callback\\_t](#) callback

- *Callback function.*  
void \* [userData](#)
- *UART callback function parameter.*  
size\_t [rxDataSizeAll](#)
- *Size of the data to receive.*  
size\_t [txDataSizeAll](#)
- *Size of the data to send out.*  
[edma\\_handle\\_t](#) \* [txEdmaHandle](#)
- *The eDMA TX channel used.*  
[edma\\_handle\\_t](#) \* [rxEdmaHandle](#)
- *The eDMA RX channel used.*  
uint8\_t [nbytes](#)
- *eDMA minor byte transfer count initially configured.*  
volatile uint8\_t [txState](#)
- *TX transfer state.*  
volatile uint8\_t [rxState](#)
- *RX transfer state.*

#### 39.4.2.1.0.96 Field Documentation

39.4.2.1.0.96.1 [uart\\_edma\\_transfer\\_callback\\_t](#) [uart\\_edma\\_handle\\_t::callback](#)

39.4.2.1.0.96.2 void\* [uart\\_edma\\_handle\\_t::userData](#)

39.4.2.1.0.96.3 size\_t [uart\\_edma\\_handle\\_t::rxDataSizeAll](#)

39.4.2.1.0.96.4 size\_t [uart\\_edma\\_handle\\_t::txDataSizeAll](#)

39.4.2.1.0.96.5 [edma\\_handle\\_t](#)\* [uart\\_edma\\_handle\\_t::txEdmaHandle](#)

39.4.2.1.0.96.6 [edma\\_handle\\_t](#)\* [uart\\_edma\\_handle\\_t::rxEdmaHandle](#)

39.4.2.1.0.96.7 uint8\_t [uart\\_edma\\_handle\\_t::nbytes](#)

39.4.2.1.0.96.8 volatile uint8\_t [uart\\_edma\\_handle\\_t::txState](#)

#### 39.4.3 Typedef Documentation

39.4.3.1 typedef void(\* [uart\\_edma\\_transfer\\_callback\\_t](#))(UART\_Type \*base,  
[uart\\_edma\\_handle\\_t](#) \*handle, status\_t status, void \*userData)

#### 39.4.4 Function Documentation

39.4.4.1 void UART\_TransferCreateHandleEDMA ( UART\_Type \* base,  
[uart\\_edma\\_handle\\_t](#) \* handle, [uart\\_edma\\_transfer\\_callback\\_t](#) callback, void \*  
userData, [edma\\_handle\\_t](#) \* txEdmaHandle, [edma\\_handle\\_t](#) \* rxEdmaHandle )

## UART eDMA Driver

### Parameters

|                     |                                                           |
|---------------------|-----------------------------------------------------------|
| <i>base</i>         | UART peripheral base address.                             |
| <i>handle</i>       | Pointer to the <code>uart_edma_handle_t</code> structure. |
| <i>callback</i>     | UART callback, NULL means no callback.                    |
| <i>userData</i>     | User callback function data.                              |
| <i>rxEdmaHandle</i> | User-requested DMA handle for RX DMA transfer.            |
| <i>txEdmaHandle</i> | User-requested DMA handle for TX DMA transfer.            |

### 39.4.4.2 **status\_t UART\_SendEDMA ( UART\_Type \* *base*, uart\_edma\_handle\_t \* *handle*, uart\_transfer\_t \* *xfer* )**

This function sends data using eDMA. This is a non-blocking function, which returns right away. When all data is sent, the send callback function is called.

### Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                       |
| <i>handle</i> | UART handle pointer.                                                |
| <i>xfer</i>   | UART eDMA transfer structure. See <a href="#">uart_transfer_t</a> . |

### Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | if succeeded; otherwise failed. |
| <i>kStatus_UART_TxBusy</i>     | Previous transfer ongoing.      |
| <i>kStatus_InvalidArgument</i> | Invalid argument.               |

### 39.4.4.3 **status\_t UART\_ReceiveEDMA ( UART\_Type \* *base*, uart\_edma\_handle\_t \* *handle*, uart\_transfer\_t \* *xfer* )**

This function receives data using eDMA. This is a non-blocking function, which returns right away. When all data is received, the receive callback function is called.

### Parameters

---

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                       |
| <i>handle</i> | Pointer to the <code>uart_edma_handle_t</code> structure.           |
| <i>xfer</i>   | UART eDMA transfer structure. See <a href="#">uart_transfer_t</a> . |

Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | if succeeded; otherwise failed. |
| <i>kStatus_UART_RxBusy</i>     | Previous transfer ongoing.      |
| <i>kStatus_InvalidArgument</i> | Invalid argument.               |

#### 39.4.4.4 void UART\_TransferAbortSendEDMA ( UART\_Type \* *base*, `uart_edma_handle_t` \* *handle* )

This function aborts sent data using eDMA.

Parameters

|               |                                                           |
|---------------|-----------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                             |
| <i>handle</i> | Pointer to the <code>uart_edma_handle_t</code> structure. |

#### 39.4.4.5 void UART\_TransferAbortReceiveEDMA ( UART\_Type \* *base*, `uart_edma_handle_t` \* *handle* )

This function aborts receive data using eDMA.

Parameters

|               |                                                           |
|---------------|-----------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                             |
| <i>handle</i> | Pointer to the <code>uart_edma_handle_t</code> structure. |

#### 39.4.4.6 status\_t UART\_TransferGetSendCountEDMA ( UART\_Type \* *base*, `uart_edma_handle_t` \* *handle*, `uint32_t` \* *count* )

This function gets the number of bytes that have been written to UART TX register by DMA.

## UART eDMA Driver

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Send bytes count.             |

### Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No send in progress.                                        |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |

#### 39.4.4.7 **status\_t** UART\_TransferGetReceiveCountEDMA ( UART\_Type \* *base*, uart\_edma\_handle\_t \* *handle*, uint32\_t \* *count* )

This function gets the number of received bytes.

### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Receive bytes count.          |

### Return values

|                                     |                                                             |
|-------------------------------------|-------------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No receive in progress.                                     |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                       |
| <i>kStatus_Success</i>              | Get successfully through the parameter <code>count</code> ; |



## 39.5 UART FreeRTOS Driver

### 39.5.1 Overview

#### Data Structures

- struct [uart\\_rtos\\_config\\_t](#)  
*UART configuration structure. [More...](#)*

#### UART RTOS Operation

- int [UART\\_RTOS\\_Init](#) (uart\_rtos\_handle\_t \*handle, uart\_handle\_t \*t\_handle, const [uart\\_rtos\\_config\\_t](#) \*cfg)  
*Initializes a UART instance for operation in RTOS.*
- int [UART\\_RTOS\\_Deinit](#) (uart\_rtos\_handle\_t \*handle)  
*Deinitializes a UART instance for operation.*

#### UART transactional Operation

- int [UART\\_RTOS\\_Send](#) (uart\_rtos\_handle\_t \*handle, const uint8\_t \*buffer, uint32\_t length)  
*Sends data in the background.*
- int [UART\\_RTOS\\_Receive](#) (uart\_rtos\_handle\_t \*handle, uint8\_t \*buffer, uint32\_t length, size\_t \*received)  
*Receives data.*

### 39.5.2 Data Structure Documentation

#### 39.5.2.1 struct [uart\\_rtos\\_config\\_t](#)

UART RTOS configuration structure.

#### Data Fields

- UART\_Type \* [base](#)  
*UART base address.*
- uint32\_t [srcclk](#)  
*UART source clock in Hz.*
- uint32\_t [baudrate](#)  
*Desired communication speed.*
- [uart\\_parity\\_mode\\_t](#) [parity](#)  
*Parity setting.*
- [uart\\_stop\\_bit\\_count\\_t](#) [stopbits](#)  
*Number of stop bits to use.*
- uint8\_t \* [buffer](#)  
*Buffer for background reception.*

## UART FreeRTOS Driver

- `uint32_t buffer_size`  
*Size of buffer for background reception.*

### 39.5.3 Function Documentation

#### 39.5.3.1 `int UART_RTOS_Init ( uart_rtos_handle_t * handle, uart_handle_t * t_handle, const uart_rtos_config_t * cfg )`

Parameters

|                 |                                                                                     |
|-----------------|-------------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS UART handle, the pointer to an allocated space for RTOS context.           |
| <i>t_handle</i> | The pointer to the allocated space to store the transactional layer internal state. |
| <i>cfg</i>      | The pointer to the parameters required to configure the UART after initialization.  |

Returns

0 succeed; otherwise fail.

#### 39.5.3.2 `int UART_RTOS_Deinit ( uart_rtos_handle_t * handle )`

This function deinitializes the UART module, sets all register values to reset value, and frees the resources.

Parameters

|               |                       |
|---------------|-----------------------|
| <i>handle</i> | The RTOS UART handle. |
|---------------|-----------------------|

#### 39.5.3.3 `int UART_RTOS_Send ( uart_rtos_handle_t * handle, const uint8_t * buffer, uint32_t length )`

This function sends data. It is a synchronous API. If the hardware buffer is full, the task is in the blocked state.

Parameters

|               |                       |
|---------------|-----------------------|
| <i>handle</i> | The RTOS UART handle. |
|---------------|-----------------------|

|               |                                    |
|---------------|------------------------------------|
| <i>buffer</i> | The pointer to the buffer to send. |
| <i>length</i> | The number of bytes to send.       |

#### 39.5.3.4 int UART\_RTOS\_Receive ( uart\_rtos\_handle\_t \* *handle*, uint8\_t \* *buffer*, uint32\_t *length*, size\_t \* *received* )

This function receives data from UART. It is a synchronous API. If data is immediately available, it is returned immediately and the number of bytes received.

Parameters

|                 |                                                                                  |
|-----------------|----------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS UART handle.                                                            |
| <i>buffer</i>   | The pointer to the buffer to write received data.                                |
| <i>length</i>   | The number of bytes to receive.                                                  |
| <i>received</i> | The pointer to a variable of size_t where the number of received data is filled. |

### 39.6 UART $\mu$ COS/II Driver

#### 39.6.1 Overview

##### Data Structures

- struct [uart\\_rtos\\_config\\_t](#)  
*UART configuration structure. [More...](#)*

##### UART RTOS Operation

- int [UART\\_RTOS\\_Init](#) (uart\_rtos\_handle\_t \*handle, uart\_handle\_t \*t\_handle, const [uart\\_rtos\\_config\\_t](#) \*cfg)  
*Initializes a UART instance for operation in RTOS.*
- int [UART\\_RTOS\\_Deinit](#) (uart\_rtos\_handle\_t \*handle)  
*Deinitializes a UART instance for operation.*

##### UART transactional Operation

- int [UART\\_RTOS\\_Send](#) (uart\_rtos\_handle\_t \*handle, const uint8\_t \*buffer, uint32\_t length)  
*Sends data in the background.*
- int [UART\\_RTOS\\_Receive](#) (uart\_rtos\_handle\_t \*handle, uint8\_t \*buffer, uint32\_t length, size\_t \*received)  
*Receives data.*

#### 39.6.2 Data Structure Documentation

##### 39.6.2.1 struct [uart\\_rtos\\_config\\_t](#)

UART RTOS configuration structure.

##### Data Fields

- UART\_Type \* [base](#)  
*UART base address.*
- uint32\_t [srcclk](#)  
*UART source clock in Hz.*
- uint32\_t [baudrate](#)  
*Desired communication speed.*
- [uart\\_parity\\_mode\\_t](#) [parity](#)  
*Parity setting.*
- [uart\\_stop\\_bit\\_count\\_t](#) [stopbits](#)  
*Number of stop bits to use.*
- uint8\_t \* [buffer](#)  
*Buffer for background reception.*

- `uint32_t buffer_size`  
Size of buffer for background reception.

### 39.6.3 Function Documentation

#### 39.6.3.1 `int UART_RTOS_Init ( uart_rtos_handle_t * handle, uart_handle_t * t_handle, const uart_rtos_config_t * cfg )`

Parameters

|                      |                                                                                           |
|----------------------|-------------------------------------------------------------------------------------------|
| <i>handle</i>        | The RTOS UART handle; the pointer to an allocated space for RTOS context.                 |
| <i>uart_t_handle</i> | The pointer to the allocated space where to store the transactional layer internal state. |
| <i>cfg</i>           | The pointer to the parameters required to configure the UART after initialization.        |

Returns

0 Succeed; otherwise fail.

#### 39.6.3.2 `int UART_RTOS_Deinit ( uart_rtos_handle_t * handle )`

This function deinitializes the UART module, sets all register values to reset value, and frees the resources.

Parameters

|               |                       |
|---------------|-----------------------|
| <i>handle</i> | The RTOS UART handle. |
|---------------|-----------------------|

#### 39.6.3.3 `int UART_RTOS_Send ( uart_rtos_handle_t * handle, const uint8_t * buffer, uint32_t length )`

This function sends data. It is a synchronous API. If the hardware buffer is full, the task is in the blocked state.

Parameters

|               |                       |
|---------------|-----------------------|
| <i>handle</i> | The RTOS UART handle. |
|---------------|-----------------------|

## UART $\mu$ COS/II Driver

|               |                                    |
|---------------|------------------------------------|
| <i>buffer</i> | The pointer to the buffer to send. |
| <i>length</i> | The number of bytes to send.       |

### 39.6.3.4 int UART\_RTOS\_Receive ( uart\_rtos\_handle\_t \* *handle*, uint8\_t \* *buffer*, uint32\_t *length*, size\_t \* *received* )

This function receives data from UART. It is a synchronous API. If any data is immediately available it is returned immediately and the number of bytes received.

#### Parameters

|                 |                                                                                  |
|-----------------|----------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS UART handle.                                                            |
| <i>buffer</i>   | The pointer to the buffer where to write received data.                          |
| <i>length</i>   | The number of bytes to receive.                                                  |
| <i>received</i> | The pointer to a variable of size_t where the number of received data is filled. |

## 39.7 UART $\mu$ COS/III Driver

### 39.7.1 Overview

#### Data Structures

- struct `uart_rtos_config_t`  
UART configuration structure. [More...](#)

#### UART RTOS Operation

- int `UART_RTOS_Init` (`uart_rtos_handle_t *handle`, `uart_handle_t *t_handle`, const `uart_rtos_config_t *cfg`)  
*Initializes a UART instance for operation in RTOS.*
- int `UART_RTOS_Deinit` (`uart_rtos_handle_t *handle`)  
*Deinitializes a UART instance for operation.*

#### UART transactional Operation

- int `UART_RTOS_Send` (`uart_rtos_handle_t *handle`, const `uint8_t *buffer`, `uint32_t length`)  
*Sends data in the background.*
- int `UART_RTOS_Receive` (`uart_rtos_handle_t *handle`, `uint8_t *buffer`, `uint32_t length`, `size_t *received`)  
*Receives data.*

### 39.7.2 Data Structure Documentation

#### 39.7.2.1 struct `uart_rtos_config_t`

UART RTOS configuration structure.

#### Data Fields

- UART\_Type \* `base`  
*UART base address.*
- `uint32_t srcclk`  
*UART source clock in Hz.*
- `uint32_t baudrate`  
*Desired communication speed.*
- `uart_parity_mode_t parity`  
*Parity setting.*
- `uart_stop_bit_count_t stopbits`  
*Number of stop bits to use.*
- `uint8_t * buffer`  
*Buffer for background reception.*

## UART $\mu$ COS/III Driver

- `uint32_t buffer_size`  
*Size of buffer for background reception.*

### 39.7.3 Function Documentation

#### 39.7.3.1 `int UART_RTOS_Init ( uart_rtos_handle_t * handle, uart_handle_t * t_handle, const uart_rtos_config_t * cfg )`

Parameters

|                      |                                                                                    |
|----------------------|------------------------------------------------------------------------------------|
| <i>handle</i>        | The RTOS UART handle; the pointer to allocated space for RTOS context.             |
| <i>uart_t_handle</i> | The pointer to an allocated space to store transactional layer internal state.     |
| <i>cfg</i>           | The pointer to the parameters required to configure the UART after initialization. |

Returns

0 Succeed; otherwise fail.

#### 39.7.3.2 `int UART_RTOS_Deinit ( uart_rtos_handle_t * handle )`

This function deinitializes the UART module, sets all register values to reset value, and releases the resources.

Parameters

|               |                       |
|---------------|-----------------------|
| <i>handle</i> | The RTOS UART handle. |
|---------------|-----------------------|

#### 39.7.3.3 `int UART_RTOS_Send ( uart_rtos_handle_t * handle, const uint8_t * buffer, uint32_t length )`

This function sends data. It is a synchronous API. If the hardware buffer is full, the task is in the blocked state.

Parameters

|               |                       |
|---------------|-----------------------|
| <i>handle</i> | The RTOS UART handle. |
|---------------|-----------------------|



|               |                                    |
|---------------|------------------------------------|
| <i>buffer</i> | The pointer to the buffer to send. |
| <i>length</i> | The number of bytes to send.       |

#### 39.7.3.4 int UART\_RTOS\_Receive ( uart\_rtos\_handle\_t \* *handle*, uint8\_t \* *buffer*, uint32\_t *length*, size\_t \* *received* )

This function receives data from UART. It is a synchronous API. If any data is immediately available, it is returned immediately and the number of bytes received.

Parameters

|                 |                                                                                  |
|-----------------|----------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS UART handle.                                                            |
| <i>buffer</i>   | The pointer to the buffer to write received data.                                |
| <i>length</i>   | The number of bytes to receive.                                                  |
| <i>received</i> | The pointer to variable of a size_t where the number of received data is filled. |



## Chapter 40

# VREF: Voltage Reference Driver

### 40.1 Overview

The KSDK provides a peripheral driver for the Crossbar Voltage Reference (VREF) block of Kinetis devices.

The Voltage Reference(VREF) supplies an accurate 1.2 V voltage output that can be trimmed in 0.5 mV steps. VREF can be used in applications to provide a reference voltage to external devices and to internal analog peripherals, such as the ADC, DAC, or CMP. The voltage reference has operating modes that provide different levels of supply rejection and power consumption.

To configure the VREF driver, configure `vref_config_t` structure in one of two ways.

1. Use the `VREF_GetDefaultConfig()` function.
2. Set the parameter in the `vref_config_t` structure.

To initialize the VREF driver, call the `VREF_Init()` function and pass a pointer to the `vref_config_t` structure.

To de-initialize the VREF driver, call the `VREF_Deinit()` function.

### 40.2 Typical use case and example

This example shows how to generate a reference voltage by using the VREF module.

```
vref_config_t vrefUserConfig;
VREF_GetDefaultConfig(&vrefUserConfig); /* Gets a default configuration. */
VREF_Init(VREF, &vrefUserConfig);      /* Initializes and configures the VREF module */

/* Do something */

VREF_Deinit(VREF); /* De-initializes the VREF module */
```

### Data Structures

- struct `vref_config_t`  
*The description structure for the VREF module. [More...](#)*

### Enumerations

- enum `vref_buffer_mode_t` {  
    `kVREF_ModeBandgapOnly` = 0U,  
    `kVREF_ModeHighPowerBuffer` = 1U,  
    `kVREF_ModeLowPowerBuffer` = 2U }  
    *VREF modes.*

## Function Documentation

### Driver version

- #define **FSL\_VREF\_DRIVER\_VERSION** (MAKE\_VERSION(2, 1, 0))  
*Version 2.1.0.*

### VREF functional operation

- void **VREF\_Init** (VREF\_Type \*base, const **vref\_config\_t** \*config)  
*Enables the clock gate and configures the VREF module according to the configuration structure.*
- void **VREF\_Deinit** (VREF\_Type \*base)  
*Stops and disables the clock for the VREF module.*
- void **VREF\_GetDefaultConfig** (**vref\_config\_t** \*config)  
*Initializes the VREF configuration structure.*
- void **VREF\_SetTrimVal** (VREF\_Type \*base, uint8\_t trimValue)  
*Sets a TRIM value for the reference voltage.*
- static uint8\_t **VREF\_GetTrimVal** (VREF\_Type \*base)  
*Reads the value of the TRIM meaning output voltage.*

## 40.3 Data Structure Documentation

### 40.3.1 struct vref\_config\_t

#### Data Fields

- **vref\_buffer\_mode\_t** bufferMode  
*Buffer mode selection.*

## 40.4 Macro Definition Documentation

### 40.4.1 #define FSL\_VREF\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 0))

## 40.5 Enumeration Type Documentation

### 40.5.1 enum vref\_buffer\_mode\_t

Enumerator

**kVREF\_ModeBandgapOnly** Bandgap on only, for stabilization and startup.  
**kVREF\_ModeHighPowerBuffer** High-power buffer mode enabled.  
**kVREF\_ModeLowPowerBuffer** Low-power buffer mode enabled.

## 40.6 Function Documentation

### 40.6.1 void VREF\_Init ( VREF\_Type \* **base**, const **vref\_config\_t** \* **config** )

This function must be called before calling all other VREF driver functions, read/write registers, and configurations with user-defined settings. The example below shows how to set up **vref\_config\_t** parameters and how to call the VREF\_Init function by passing in these parameters. This is an example.

```

*  vref_config_t vrefConfig;
*  vrefConfig.bufferMode = kVREF_ModeHighPowerBuffer;
*  vrefConfig.enableExternalVoltRef = false;
*  vrefConfig.enableLowRef = false;
*  VREF_Init(VREF, &vrefConfig);
*

```

## Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | VREF peripheral address.                |
| <i>config</i> | Pointer to the configuration structure. |

#### 40.6.2 void VREF\_Deinit ( VREF\_Type \* *base* )

This function should be called to shut down the module. This is an example.

```

*  vref_config_t vrefUserConfig;
*  VREF_Init(VREF);
*  VREF_GetDefaultConfig(&vrefUserConfig);
*  ...
*  VREF_Deinit(VREF);
*

```

## Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | VREF peripheral address. |
|-------------|--------------------------|

#### 40.6.3 void VREF\_GetDefaultConfig ( vref\_config\_t \* *config* )

This function initializes the VREF configuration structure to default values. This is an example.

```

*  vrefConfig->bufferMode = kVREF_ModeHighPowerBuffer;
*  vrefConfig->enableExternalVoltRef = false;
*  vrefConfig->enableLowRef = false;
*

```

## Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>config</i> | Pointer to the initialization structure. |
|---------------|------------------------------------------|

### 40.6.4 void VREF\_SetTrimVal ( VREF\_Type \* *base*, uint8\_t *trimValue* )

This function sets a TRIM value for the reference voltage. Note that the TRIM value maximum is 0x3F.

Parameters

|                  |                                                                                        |
|------------------|----------------------------------------------------------------------------------------|
| <i>base</i>      | VREF peripheral address.                                                               |
| <i>trimValue</i> | Value of the trim register to set the output reference voltage (maximum 0x3F (6-bit)). |

### 40.6.5 static uint8\_t VREF\_GetTrimVal ( VREF\_Type \* *base* ) [inline], [static]

This function gets the TRIM value from the TRM register.

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | VREF peripheral address. |
|-------------|--------------------------|

Returns

Six-bit value of trim setting.

# Chapter 41

## WDOG: Watchdog Timer Driver

### 41.1 Overview

The KSDK provides a peripheral driver for the Watchdog module (WDOG) of Kinetis devices.

### 41.2 Typical use case

```
wdog_config_t config;
WDOG_GetDefaultConfig(&config);
config.timeoutValue = 0x7ffU;
config.enableWindowMode = true;
config.windowValue = 0x1ffU;
WDOG_Init(wdog_base, &config);
```

### Data Structures

- struct `wdog_work_mode_t`  
*Defines WDOG work mode. [More...](#)*
- struct `wdog_config_t`  
*Describes WDOG configuration structure. [More...](#)*
- struct `wdog_test_config_t`  
*Describes WDOG test mode configuration structure. [More...](#)*

### Enumerations

- enum `wdog_clock_source_t` {  
    `kWDOG_LpoClockSource` = 0U,  
    `kWDOG_AlternateClockSource` = 1U }  
*Describes WDOG clock source.*
- enum `wdog_clock_prescaler_t` {  
    `kWDOG_ClockPrescalerDivide1` = 0x0U,  
    `kWDOG_ClockPrescalerDivide2` = 0x1U,  
    `kWDOG_ClockPrescalerDivide3` = 0x2U,  
    `kWDOG_ClockPrescalerDivide4` = 0x3U,  
    `kWDOG_ClockPrescalerDivide5` = 0x4U,  
    `kWDOG_ClockPrescalerDivide6` = 0x5U,  
    `kWDOG_ClockPrescalerDivide7` = 0x6U,  
    `kWDOG_ClockPrescalerDivide8` = 0x7U }  
*Describes the selection of the clock prescaler.*
- enum `wdog_test_mode_t` {  
    `kWDOG_QuickTest` = 0U,  
    `kWDOG_ByteTest` = 1U }  
*Describes WDOG test mode.*

## Typical use case

- enum `wdog_tested_byte_t` {  
    `kWDOG_TestByte0` = 0U,  
    `kWDOG_TestByte1` = 1U,  
    `kWDOG_TestByte2` = 2U,  
    `kWDOG_TestByte3` = 3U }  
    *Describes WDOG tested byte selection in byte test mode.*
- enum `_wdog_interrupt_enable_t` { `kWDOG_InterruptEnable` = `WDOG_STCTRLH_IRQRSTEN_MASK` }  
    *WDOG interrupt configuration structure, default settings all disabled.*
- enum `_wdog_status_flags_t` {  
    `kWDOG_RunningFlag` = `WDOG_STCTRLH_WDOGEN_MASK`,  
    `kWDOG_TimeoutFlag` = `WDOG_STCTRLL_INTFLG_MASK` }  
    *WDOG status flags.*

## Driver version

- #define `FSL_WDOG_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 0)`)  
    *Defines WDOG driver version 2.0.0.*

## Unlock sequence

- #define `WDOG_FIRST_WORD_OF_UNLOCK` (`0xC520U`)  
    *First word of unlock sequence.*
- #define `WDOG_SECOND_WORD_OF_UNLOCK` (`0xD928U`)  
    *Second word of unlock sequence.*

## Refresh sequence

- #define `WDOG_FIRST_WORD_OF_REFRESH` (`0xA602U`)  
    *First word of refresh sequence.*
- #define `WDOG_SECOND_WORD_OF_REFRESH` (`0xB480U`)  
    *Second word of refresh sequence.*

## WDOG Initialization and De-initialization

- void `WDOG_GetDefaultConfig` (`wdog_config_t *config`)  
    *Initializes the WDOG configuration structure.*
- void `WDOG_Init` (`WDOG_Type *base`, const `wdog_config_t *config`)  
    *Initializes the WDOG.*
- void `WDOG_Deinit` (`WDOG_Type *base`)  
    *Shuts down the WDOG.*
- void `WDOG_SetTestModeConfig` (`WDOG_Type *base`, `wdog_test_config_t *config`)  
    *Configures the WDOG functional test.*

## WDOG Functional Operation

- static void `WDOG_Enable` (`WDOG_Type *base`)  
    *Enables the WDOG module.*
- static void `WDOG_Disable` (`WDOG_Type *base`)



- *Disables the WDOG module.*
- static void [WDOG\\_EnableInterrupts](#) (WDOG\_Type \*base, uint32\_t mask)  
*Enables the WDOG interrupt.*
- static void [WDOG\\_DisableInterrupts](#) (WDOG\_Type \*base, uint32\_t mask)  
*Disables the WDOG interrupt.*
- uint32\_t [WDOG\\_GetStatusFlags](#) (WDOG\_Type \*base)  
*Gets the WDOG all status flags.*
- void [WDOG\\_ClearStatusFlags](#) (WDOG\_Type \*base, uint32\_t mask)  
*Clears the WDOG flag.*
- static void [WDOG\\_SetTimeoutValue](#) (WDOG\_Type \*base, uint32\_t timeoutCount)  
*Sets the WDOG timeout value.*
- static void [WDOG\\_SetWindowValue](#) (WDOG\_Type \*base, uint32\_t windowValue)  
*Sets the WDOG window value.*
- static void [WDOG\\_Unlock](#) (WDOG\_Type \*base)  
*Unlocks the WDOG register written.*
- void [WDOG\\_Refresh](#) (WDOG\_Type \*base)  
*Refreshes the WDOG timer.*
- static uint16\_t [WDOG\\_GetResetCount](#) (WDOG\_Type \*base)  
*Gets the WDOG reset count.*
- static void [WDOG\\_ClearResetCount](#) (WDOG\_Type \*base)  
*Clears the WDOG reset count.*

## 41.3 Data Structure Documentation

### 41.3.1 struct wdog\_work\_mode\_t

#### Data Fields

- bool [enableWait](#)  
*Enables or disables WDOG in wait mode.*
- bool [enableStop](#)  
*Enables or disables WDOG in stop mode.*
- bool [enableDebug](#)  
*Enables or disables WDOG in debug mode.*

### 41.3.2 struct wdog\_config\_t

#### Data Fields

- bool [enableWdog](#)  
*Enables or disables WDOG.*
- [wdog\\_clock\\_source\\_t](#) clockSource  
*Clock source select.*
- [wdog\\_clock\\_prescaler\\_t](#) prescaler  
*Clock prescaler value.*
- [wdog\\_work\\_mode\\_t](#) workMode  
*Configures WDOG work mode in debug stop and wait mode.*
- bool [enableUpdate](#)

## Enumeration Type Documentation

- *Update write-once register enable.*  
bool [enableInterrupt](#)
- *Enables or disables WDOG interrupt.*  
bool [enableWindowMode](#)
- *Enables or disables WDOG window mode.*  
uint32\_t [windowValue](#)
- *Window value.*  
uint32\_t [timeoutValue](#)
- *Timeout value.*

### 41.3.3 struct wdog\_test\_config\_t

#### Data Fields

- [wdog\\_test\\_mode\\_t testMode](#)  
*Selects test mode.*
- [wdog\\_tested\\_byte\\_t testedByte](#)  
*Selects tested byte in byte test mode.*
- uint32\_t [timeoutValue](#)  
*Timeout value.*

## 41.4 Macro Definition Documentation

### 41.4.1 #define FSL\_WDOG\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 0))

## 41.5 Enumeration Type Documentation

### 41.5.1 enum wdog\_clock\_source\_t

#### Enumerator

- kWDOG\_LpoClockSource*** WDOG clock sourced from LPO.  
***kWDOG\_AlternateClockSource*** WDOG clock sourced from alternate clock source.

### 41.5.2 enum wdog\_clock\_prescaler\_t

#### Enumerator

- kWDOG\_ClockPrescalerDivide1*** Divided by 1.  
***kWDOG\_ClockPrescalerDivide2*** Divided by 2.  
***kWDOG\_ClockPrescalerDivide3*** Divided by 3.  
***kWDOG\_ClockPrescalerDivide4*** Divided by 4.  
***kWDOG\_ClockPrescalerDivide5*** Divided by 5.  
***kWDOG\_ClockPrescalerDivide6*** Divided by 6.  
***kWDOG\_ClockPrescalerDivide7*** Divided by 7.

*kWDOG\_ClockPrescalerDivide8* Divided by 8.

### 41.5.3 enum wdog\_test\_mode\_t

Enumerator

*kWDOG\_QuickTest* Selects quick test.

*kWDOG\_ByteTest* Selects byte test.

### 41.5.4 enum wdog\_tested\_byte\_t

Enumerator

*kWDOG\_TestByte0* Byte 0 selected in byte test mode.

*kWDOG\_TestByte1* Byte 1 selected in byte test mode.

*kWDOG\_TestByte2* Byte 2 selected in byte test mode.

*kWDOG\_TestByte3* Byte 3 selected in byte test mode.

### 41.5.5 enum \_wdog\_interrupt\_enable\_t

This structure contains the settings for all of the WDOG interrupt configurations.

Enumerator

*kWDOG\_InterruptEnable* WDOG timeout generates an interrupt before reset.

### 41.5.6 enum \_wdog\_status\_flags\_t

This structure contains the WDOG status flags for use in the WDOG functions.

Enumerator

*kWDOG\_RunningFlag* Running flag, set when WDOG is enabled.

*kWDOG\_TimeoutFlag* Interrupt flag, set when an exception occurs.

## 41.6 Function Documentation

### 41.6.1 void WDOG\_GetDefaultConfig ( wdog\_config\_t \* config )

This function initializes the WDOG configuration structure to default values. The default values are as follows.

## Function Documentation

```
* wdogConfig->enableWdog = true;
* wdogConfig->clockSource = kWDOG_LpoClockSource;
* wdogConfig->prescaler = kWDOG_ClockPrescalerDivide1;
* wdogConfig->workMode.enableWait = true;
* wdogConfig->workMode.enableStop = false;
* wdogConfig->workMode.enableDebug = false;
* wdogConfig->enableUpdate = true;
* wdogConfig->enableInterrupt = false;
* wdogConfig->enableWindowMode = false;
* wdogConfig->windowValue = 0;
* wdogConfig->timeoutValue = 0xFFFFU;
*
```

### Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>config</i> | Pointer to the WDOG configuration structure. |
|---------------|----------------------------------------------|

### See Also

[wdog\\_config\\_t](#)

### 41.6.2 void WDOG\_Init ( WDOG\_Type \* *base*, const wdog\_config\_t \* *config* )

This function initializes the WDOG. When called, the WDOG runs according to the configuration. To reconfigure WDOG without forcing a reset first, enableUpdate must be set to true in the configuration.

This is an example.

```
* wdog_config_t config;
* WDOG_GetDefaultConfig(&config);
* config.timeoutValue = 0x7ffU;
* config.enableUpdate = true;
* WDOG_Init(wdog_base, &config);
*
```

### Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | WDOG peripheral base address |
| <i>config</i> | The configuration of WDOG    |

### 41.6.3 void WDOG\_Deinit ( WDOG\_Type \* *base* )

This function shuts down the WDOG. Ensure that the WDOG\_STCTRLH.ALLOWUPDATE is 1 which indicates that the register update is enabled.

#### 41.6.4 void WDOG\_SetTestModeConfig ( WDOG\_Type \* *base*, wdog\_test\_config\_t \* *config* )

This function is used to configure the WDOG functional test. When called, the WDOG goes into test mode and runs according to the configuration. Ensure that the WDOG\_STCTRLH.ALLOWUPDATE is 1 which means that the register update is enabled.

This is an example.

```
* wdog_test_config_t test_config;
* test_config.testMode = kWDog_QuickTest;
* test_config.timeoutValue = 0xfffffu;
* WDOG_SetTestModeConfig(wdog_base, &test_config);
*
```

Parameters

|               |                                           |
|---------------|-------------------------------------------|
| <i>base</i>   | WDog peripheral base address              |
| <i>config</i> | The functional test configuration of WDOG |

#### 41.6.5 static void WDOG\_Enable ( WDOG\_Type \* *base* ) [inline], [static]

This function write value into WDOG\_STCTRLH register to enable the WDOG, it is a write-once register, make sure that the WCT window is still open and this register has not been written in this WCT while this function is called.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | WDog peripheral base address |
|-------------|------------------------------|

#### 41.6.6 static void WDOG\_Disable ( WDOG\_Type \* *base* ) [inline], [static]

This function writes a value into the WDOG\_STCTRLH register to disable the WDOG. It is a write-once register. Ensure that the WCT window is still open and that register has not been written to in this WCT while the function is called.

Parameters

---

## Function Documentation

|             |                              |
|-------------|------------------------------|
| <i>base</i> | WDOG peripheral base address |
|-------------|------------------------------|

### 41.6.7 static void WDOG\_EnableInterrupts ( WDOG\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function writes a value into the WDOG\_STCTRLH register to enable the WDOG interrupt. It is a write-once register. Ensure that the WCT window is still open and the register has not been written to in this WCT while the function is called.

Parameters

|             |                                                                                                                                                                       |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | WDOG peripheral base address                                                                                                                                          |
| <i>mask</i> | The interrupts to enable The parameter can be combination of the following source if defined. <ul style="list-style-type: none"><li>• kWDOG_InterruptEnable</li></ul> |

### 41.6.8 static void WDOG\_DisableInterrupts ( WDOG\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function writes a value into the WDOG\_STCTRLH register to disable the WDOG interrupt. It is a write-once register. Ensure that the WCT window is still open and the register has not been written to in this WCT while the function is called.

Parameters

|             |                                                                                                                                                                        |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | WDOG peripheral base address                                                                                                                                           |
| <i>mask</i> | The interrupts to disable The parameter can be combination of the following source if defined. <ul style="list-style-type: none"><li>• kWDOG_InterruptEnable</li></ul> |

### 41.6.9 uint32\_t WDOG\_GetStatusFlags ( WDOG\_Type \* *base* )

This function gets all status flags.

This is an example for getting the Running Flag.

```
*  uint32_t status;
*  status = WDOG_GetStatusFlags (wdog_base) &
*          kWDOG_RunningFlag;
*
```

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | WDOG peripheral base address |
|-------------|------------------------------|

Returns

State of the status flag: asserted (true) or not-asserted (false).

See Also

[\\_wdog\\_status\\_flags\\_t](#)

- true: a related status flag has been set.
- false: a related status flag is not set.

### 41.6.10 void WDOG\_ClearStatusFlags ( WDOG\_Type \* *base*, uint32\_t *mask* )

This function clears the WDOG status flag.

This is an example for clearing the timeout (interrupt) flag.

```
*  WDOG_ClearStatusFlags (wdog_base, kWDOG_TimeoutFlag);
*
```

Parameters

## Function Documentation

|             |                                                                                                              |
|-------------|--------------------------------------------------------------------------------------------------------------|
| <i>base</i> | WDOG peripheral base address                                                                                 |
| <i>mask</i> | The status flags to clear. The parameter could be any combination of the following values. kWDOG_TimeoutFlag |

### 41.6.11 static void WDOG\_SetTimeoutValue ( WDOG\_Type \* *base*, uint32\_t *timeoutCount* ) [inline], [static]

This function sets the timeout value. It should be ensured that the time-out value for the WDOG is always greater than 2xWCT time + 20 bus clock cycles. This function writes a value into WDOG\_TOVALH and WDOG\_TOVALL registers which are write-once. Ensure the WCT window is still open and the two registers have not been written to in this WCT while the function is called.

Parameters

|                     |                                               |
|---------------------|-----------------------------------------------|
| <i>base</i>         | WDOG peripheral base address                  |
| <i>timeoutCount</i> | WDOG timeout value; count of WDOG clock tick. |

### 41.6.12 static void WDOG\_SetWindowValue ( WDOG\_Type \* *base*, uint32\_t *windowValue* ) [inline], [static]

This function sets the WDOG window value. This function writes a value into WDOG\_WINH and WDOG\_WINL registers which are write-once. Ensure the WCT window is still open and the two registers have not been written to in this WCT while the function is called.

Parameters

|                    |                              |
|--------------------|------------------------------|
| <i>base</i>        | WDOG peripheral base address |
| <i>windowValue</i> | WDOG window value.           |

### 41.6.13 static void WDOG\_Unlock ( WDOG\_Type \* *base* ) [inline], [static]

This function unlocks the WDOG register written. Before starting the unlock sequence and following configuration, disable the global interrupts. Otherwise, an interrupt may invalidate the unlocking sequence and the WCT may expire. After the configuration finishes, re-enable the global interrupts.



## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | WDOG peripheral base address |
|-------------|------------------------------|

**41.6.14 void WDOG\_Refresh ( WDOG\_Type \* *base* )**

This function feeds the WDOG. This function should be called before the WDOG timer is in timeout. Otherwise, a reset is asserted.

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | WDOG peripheral base address |
|-------------|------------------------------|

**41.6.15 static uint16\_t WDOG\_GetResetCount ( WDOG\_Type \* *base* ) [inline], [static]**

This function gets the WDOG reset count value.

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | WDOG peripheral base address |
|-------------|------------------------------|

## Returns

WDOG reset count value.

**41.6.16 static void WDOG\_ClearResetCount ( WDOG\_Type \* *base* ) [inline], [static]**

This function clears the WDOG reset count value.

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | WDOG peripheral base address |
|-------------|------------------------------|



## Chapter 42

### Clock Driver

#### 42.1 Overview

The KSDK provides APIs for Kinetis devices clock operation.

#### 42.2 Get frequency

A centralized function `CLOCK_GetFreq` gets different clock type frequencies by passing a clock name. For example, pass a `kCLOCK_CoreSysClk` to get the core clock and pass a `kCLOCK_BusClk` to get the bus clock. Additionally, there are separate functions to get the frequency. For example, use `CLOCK_GetCoreSysClkFreq` to get the core clock frequency and `CLOCK_GetBusClkFreq` to get the bus clock frequency. Using these functions reduces the image size.

#### 42.3 External clock frequency

The external clocks `EXTAL0/EXTAL1/EXTAL32` are decided by the board level design. The Clock driver uses variables `g_xtal0Freq/g_xtal1Freq/g_xtal32Freq` to save clock frequencies. Likewise, the APIs `CLOCK_SetXtal0Freq`, `CLOCK_SetXtal1Freq`, and `CLOCK_SetXtal32Freq` are used to set these variables.

The upper layer must set these values correctly. For example, after `OSC0(SYSOSC)` is initialized using `CLOCK_InitOsc0` or `CLOCK_InitSysOsc`, the upper layer should call the `CLOCK_SetXtal0Freq`. Otherwise, the clock frequency get functions may not receive valid values. This is useful for multicore platforms where only one core calls `CLOCK_InitOsc0` to initialize `OSC0` and other cores call `CLOCK_SetXtal0Freq`.

### Modules

- [Multipurpose Clock Generator \(MCG\)](#)

### Files

- file [fsl\\_clock.h](#)

### Data Structures

- struct [sim\\_clock\\_config\\_t](#)  
*SIM configuration structure for clock setting. [More...](#)*
- struct [oscer\\_config\\_t](#)  
*OSC configuration for OSCERCLK. [More...](#)*
- struct [osc\\_config\\_t](#)  
*OSC Initialization Configuration Structure. [More...](#)*
- struct [mcg\\_pll\\_config\\_t](#)

## External clock frequency

- *MCG PLL configuration. [More...](#)*
- struct [mcg\\_config\\_t](#)  
*MCG mode change configuration structure. [More...](#)*

## Macros

- #define [FSL\\_SDK\\_DISABLE\\_DRIVER\\_CLOCK\\_CONTROL](#) 0  
*Configure whether driver controls clock.*
- #define [MCG\\_INTERNAL\\_IRC\\_48M](#) 48000000U  
*IRC48M clock frequency in Hz.*
- #define [DMAMUX\\_CLOCKS](#)  
*Clock ip name array for DMAMUX.*
- #define [RTC\\_CLOCKS](#)  
*Clock ip name array for RTC.*
- #define [ENET\\_CLOCKS](#)  
*Clock ip name array for ENET.*
- #define [PORT\\_CLOCKS](#)  
*Clock ip name array for PORT.*
- #define [SAI\\_CLOCKS](#)  
*Clock ip name array for SAI.*
- #define [FLEXBUS\\_CLOCKS](#)  
*Clock ip name array for FLEXBUS.*
- #define [TSI\\_CLOCKS](#)  
*Clock ip name array for TSI.*
- #define [LPUART\\_CLOCKS](#)  
*Clock ip name array for LPUART.*
- #define [EWM\\_CLOCKS](#)  
*Clock ip name array for EWM.*
- #define [PIT\\_CLOCKS](#)  
*Clock ip name array for PIT.*
- #define [DSPI\\_CLOCKS](#)  
*Clock ip name array for DSPI.*
- #define [LPTMR\\_CLOCKS](#)  
*Clock ip name array for LPTMR.*
- #define [SDHC\\_CLOCKS](#)  
*Clock ip name array for SDHC.*
- #define [FTM\\_CLOCKS](#)  
*Clock ip name array for FTM.*
- #define [EDMA\\_CLOCKS](#)  
*Clock ip name array for EDMA.*
- #define [FLEXCAN\\_CLOCKS](#)  
*Clock ip name array for FLEXCAN.*
- #define [DAC\\_CLOCKS](#)  
*Clock ip name array for DAC.*
- #define [ADC16\\_CLOCKS](#)  
*Clock ip name array for ADC16.*
- #define [SDRAM\\_CLOCKS](#)  
*Clock ip name array for SDRAM.*
- #define [MPU\\_CLOCKS](#)  
*Clock ip name array for MPU.*
- #define [VREF\\_CLOCKS](#)

- *Clock ip name array for VREF.*  
• #define **CMT\_CLOCKS**
- *Clock ip name array for CMT.*  
• #define **UART\_CLOCKS**
- *Clock ip name array for UART.*  
• #define **TPM\_CLOCKS**
- *Clock ip name array for TPM.*  
• #define **RNGA\_CLOCKS**
- *Clock ip name array for RNGA.*  
• #define **CRC\_CLOCKS**
- *Clock ip name array for CRC.*  
• #define **I2C\_CLOCKS**
- *Clock ip name array for I2C.*  
• #define **PDB\_CLOCKS**
- *Clock ip name array for PDB.*  
• #define **FTF\_CLOCKS**
- *Clock ip name array for FTF.*  
• #define **CMP\_CLOCKS**
- *Clock ip name array for CMP.*  
• #define **LPO\_CLK\_FREQ** 1000U
- *LPO clock frequency.*  
• #define **SYS\_CLK** kCLOCK\_CoreSysClk
- *Peripherals clock source definition.*

## Enumerations

- enum **clock\_name\_t** {  
     **kCLOCK\_CoreSysClk**,  
     **kCLOCK\_PlatClk**,  
     **kCLOCK\_BusClk**,  
     **kCLOCK\_FlexBusClk**,  
     **kCLOCK\_FlashClk**,  
     **kCLOCK\_FastPeriphClk**,  
     **kCLOCK\_PllFllSelClk**,  
     **kCLOCK\_Er32kClk**,  
     **kCLOCK\_Osc0ErClk**,  
     **kCLOCK\_Osc1ErClk**,  
     **kCLOCK\_Osc0ErClkUndiv**,  
     **kCLOCK\_McgFixedFreqClk**,  
     **kCLOCK\_McgInternalRefClk**,  
     **kCLOCK\_McgFllClk**,  
     **kCLOCK\_McgPll0Clk**,  
     **kCLOCK\_McgPll1Clk**,  
     **kCLOCK\_McgExtPllClk**,  
     **kCLOCK\_McgPeriphClk**,  
     **kCLOCK\_McgIrc48MClk**,  
     **kCLOCK\_LpoClk** }  
     *Clock name used to get clock frequency.*

## External clock frequency

- enum `clock_usb_src_t` {  
    `kCLOCK_UsbSrcPll0` = `SIM_SOPT2_USBSRC(1U) | SIM_SOPT2_PLLFLLSEL(1U)`,  
    `kCLOCK_UsbSrcUsbPfd` = `SIM_SOPT2_USBSRC(1U) | SIM_SOPT2_PLLFLLSEL(2U)`,  
    `kCLOCK_UsbSrcIrc48M` = `SIM_SOPT2_USBSRC(1U) | SIM_SOPT2_PLLFLLSEL(3U)`,  
    `kCLOCK_UsbSrcExt` = `SIM_SOPT2_USBSRC(0U)`,  
    `kCLOCK_UsbSrcUnused` = `0xFFFFFFFFU` }  
    *USB clock source definition.*
- enum `clock_usb_phy_src_t` { `kCLOCK_UsbPhySrcExt` = `0U` }  
    *Source of the USB HS PHY.*
- enum `clock_usb_pfd_src_t` {  
    `kCLOCK_UsbPfdSrcExt` = `0U`,  
    `kCLOCK_UsbPfdSrcFracDivBy4` = `1U`,  
    `kCLOCK_UsbPfdSrcFracDivBy2` = `2U`,  
    `kCLOCK_UsbPfdSrcFrac` = `3U` }  
    *Source of the USB HS PFD clock (USB1PFDCLK)*
- enum `clock_ip_name_t`  
    *Clock gate name used for `CLOCK_EnableClock/CLOCK_DisableClock`.*
- enum `osc_mode_t` {  
    `kOSC_ModeExt` = `0U`,  
    `kOSC_ModeOscLowPower` = `MCG_C2_EREFS0_MASK`,  
    `kOSC_ModeOscHighGain` }  
    *OSC work mode.*
- enum `_osc_cap_load` {  
    `kOSC_Cap2P` = `OSC_CR_SC2P_MASK`,  
    `kOSC_Cap4P` = `OSC_CR_SC4P_MASK`,  
    `kOSC_Cap8P` = `OSC_CR_SC8P_MASK`,  
    `kOSC_Cap16P` = `OSC_CR_SC16P_MASK` }  
    *Oscillator capacitor load setting.*
- enum `_oscer_enable_mode` {  
    `kOSC_ErClkEnable` = `OSC_CR_ERCLKEN_MASK`,  
    `kOSC_ErClkEnableInStop` = `OSC_CR_EREFS0_MASK` }  
    *OSCERCLK enable mode.*
- enum `mcg_fll_src_t` {  
    `kMCG_FllSrcExternal`,  
    `kMCG_FllSrcInternal` }  
    *MCG FLL reference clock source select.*
- enum `mcg_irc_mode_t` {  
    `kMCG_IrcSlow`,  
    `kMCG_IrcFast` }  
    *MCG internal reference clock select.*
- enum `mcg_dmx32_t` {  
    `kMCG_Dmx32Default`,  
    `kMCG_Dmx32Fine` }  
    *MCG DCO Maximum Frequency with 32.768 kHz Reference.*
- enum `mcg_drs_t` {

- kMCG\_DrsLow,
  - kMCG\_DrsMid,
  - kMCG\_DrsMidHigh,
  - kMCG\_DrsHigh }
- MCG DCO range select.*
  - enum `mcg_pll_ref_src_t` {  
    - kMCG\_PllRefOsc0,
    - kMCG\_PllRefOsc1 }
  - MCG PLL reference clock select.*
  - enum `mcg_clkout_src_t` {  
    - kMCG\_ClkOutSrcOut,
    - kMCG\_ClkOutSrcInternal,
    - kMCG\_ClkOutSrcExternal }
  - MCGOUT clock source.*
  - enum `mcg_atm_select_t` {  
    - kMCG\_AtmSel32k,
    - kMCG\_AtmSel4m }
  - MCG Automatic Trim Machine Select.*
  - enum `mcg_oscsel_t` {  
    - kMCG\_OscselOsc,
    - kMCG\_OscselRtc,
    - kMCG\_OscselIrc }
  - MCG OSC Clock Select.*
  - enum `mcg_pll_clk_select_t` { kMCG\_PllClkSelPll0 }
  - MCG PLLCS select.*
  - enum `mcg_monitor_mode_t` {  
    - kMCG\_MonitorNone,
    - kMCG\_MonitorInt,
    - kMCG\_MonitorReset }
  - MCG clock monitor mode.*
  - enum `_mcg_status` {  
    - kStatus\_MCG\_ModeUnreachable = MAKE\_STATUS(kStatusGroup\_MCG, 0),
    - kStatus\_MCG\_ModeInvalid = MAKE\_STATUS(kStatusGroup\_MCG, 1),
    - kStatus\_MCG\_AtmBusClockInvalid = MAKE\_STATUS(kStatusGroup\_MCG, 2),
    - kStatus\_MCG\_AtmDesiredFreqInvalid = MAKE\_STATUS(kStatusGroup\_MCG, 3),
    - kStatus\_MCG\_AtmIrcUsed = MAKE\_STATUS(kStatusGroup\_MCG, 4),
    - kStatus\_MCG\_AtmHardwareFail = MAKE\_STATUS(kStatusGroup\_MCG, 5),
    - kStatus\_MCG\_SourceUsed = MAKE\_STATUS(kStatusGroup\_MCG, 6) }
  - MCG status.*
  - enum `_mcg_status_flags_t` {  
    - kMCG\_Osc0LostFlag = (1U << 0U),
    - kMCG\_Osc0InitFlag = (1U << 1U),
    - kMCG\_RtcOscLostFlag = (1U << 4U),
    - kMCG\_Pll0LostFlag = (1U << 5U),
    - kMCG\_Pll0LockFlag = (1U << 6U),
    - kMCG\_ExtPllLostFlag = (1U << 9U) }
  - MCG status flags.*

## External clock frequency

- enum `_mcg_ircclk_enable_mode` {  
    `kMCG_IrcclkEnable` = `MCG_C1_IRCLKEN_MASK`,  
    `kMCG_IrcclkEnableInStop` = `MCG_C1_IREFSTEN_MASK` }  
    *MCG internal reference clock (MCGIRCLK) enable mode definition.*
- enum `_mcg_pll_enable_mode` {  
    `kMCG_PllEnableIndependent` = `MCG_C5_PLLCLKEN0_MASK`,  
    `kMCG_PllEnableInStop` = `MCG_C5_PLLSTEN0_MASK` }  
    *MCG PLL clock enable mode definition.*
- enum `mcg_mode_t` {  
    `kMCG_ModeFEI` = 0U,  
    `kMCG_ModeFBI`,  
    `kMCG_ModeBLPI`,  
    `kMCG_ModeFEE`,  
    `kMCG_ModeFBE`,  
    `kMCG_ModeBLPE`,  
    `kMCG_ModePBE`,  
    `kMCG_ModePEE`,  
    `kMCG_ModeError` }  
    *MCG mode definitions.*

## Functions

- static void `CLOCK_EnableClock` (`clock_ip_name_t` name)  
    *Enable the clock for specific IP.*
- static void `CLOCK_DisableClock` (`clock_ip_name_t` name)  
    *Disable the clock for specific IP.*
- static void `CLOCK_SetEr32kClock` (uint32\_t src)  
    *Set ERCLK32K source.*
- static void `CLOCK_SetSdhc0Clock` (uint32\_t src)  
    *Set SDHC0 clock source.*
- static void `CLOCK_SetEnetTime0Clock` (uint32\_t src)  
    *Set enet timestamp clock source.*
- static void `CLOCK_SetRmii0Clock` (uint32\_t src)  
    *Set RMII clock source.*
- static void `CLOCK_SetLpuartClock` (uint32\_t src)  
    *Set LPUART clock source.*
- static void `CLOCK_SetTpmClock` (uint32\_t src)  
    *Set TPM clock source.*
- static void `CLOCK_SetTraceClock` (uint32\_t src, uint32\_t divValue, uint32\_t fracValue)  
    *Set debug trace clock source.*
- static void `CLOCK_SetPllFllSelClock` (uint32\_t src, uint32\_t divValue, uint32\_t fracValue)  
    *Set PLLFLLSEL clock source.*
- static void `CLOCK_SetClkOutClock` (uint32\_t src)  
    *Set CLKOUT source.*
- static void `CLOCK_SetRtcClkOutClock` (uint32\_t src)  
    *Set RTC\_CLKOUT source.*
- bool `CLOCK_EnableUsbhs0Clock` (`clock_usb_src_t` src, uint32\_t freq)  
    *Enable USB HS clock.*
- void `CLOCK_DisableUsbhs0Clock` (void)



- *Disable USB HS clock.*
- bool [CLOCK\\_EnableUsbhs0PhyPllClock](#) ([clock\\_usb\\_phy\\_src\\_t](#) src, uint32\_t freq)
- *Enable USB HS PHY PLL clock.*
- void [CLOCK\\_DisableUsbhs0PhyPllClock](#) (void)
- *Disable USB HS PHY PLL clock.*
- void [CLOCK\\_EnableUsbhs0PfdClock](#) (uint8\_t frac, [clock\\_usb\\_pfd\\_src\\_t](#) src)
- *Enable USB HS PFD clock.*
- void [CLOCK\\_DisableUsbhs0PfdClock](#) (void)
- *Disable USB HS PFD clock.*
- bool [CLOCK\\_EnableUsbfs0Clock](#) ([clock\\_usb\\_src\\_t](#) src, uint32\_t freq)
- *Enable USB FS clock.*
- static void [CLOCK\\_DisableUsbfs0Clock](#) (void)
- *Disable USB FS clock.*
- static void [CLOCK\\_SetOutDiv](#) (uint32\_t outdiv1, uint32\_t outdiv2, uint32\_t outdiv3, uint32\_t outdiv4)
- *System clock divider.*
- uint32\_t [CLOCK\\_GetFreq](#) ([clock\\_name\\_t](#) clockName)
- *Gets the clock frequency for a specific clock name.*
- uint32\_t [CLOCK\\_GetCoreSysClkFreq](#) (void)
- *Get the core clock or system clock frequency.*
- uint32\_t [CLOCK\\_GetPlatClkFreq](#) (void)
- *Get the platform clock frequency.*
- uint32\_t [CLOCK\\_GetBusClkFreq](#) (void)
- *Get the bus clock frequency.*
- uint32\_t [CLOCK\\_GetFlexBusClkFreq](#) (void)
- *Get the flexbus clock frequency.*
- uint32\_t [CLOCK\\_GetFlashClkFreq](#) (void)
- *Get the flash clock frequency.*
- uint32\_t [CLOCK\\_GetPllFllSelClkFreq](#) (void)
- *Get the output clock frequency selected by SIM[PLL\_FLLSEL].*
- uint32\_t [CLOCK\\_GetEr32kClkFreq](#) (void)
- *Get the external reference 32K clock frequency (ERCLK32K).*
- uint32\_t [CLOCK\\_GetOsc0ErClkFreq](#) (void)
- *Get the OSC0 external reference clock frequency (OSC0ERCLK).*
- uint32\_t [CLOCK\\_GetOsc0ErClkUndivFreq](#) (void)
- *Get the OSC0 external reference undivided clock frequency (OSC0ERCLK\_UNDIV).*
- void [CLOCK\\_SetSimConfig](#) ([sim\\_clock\\_config\\_t](#) const \*config)
- *Set the clock configure in SIM module.*
- static void [CLOCK\\_SetSimSafeDivs](#) (void)
- *Set the system clock dividers in SIM to safe value.*

## Variables

- uint32\_t [g\\_xtal0Freq](#)
- *External XTAL0 (OSC0) clock frequency.*
- uint32\_t [g\\_xtal32Freq](#)
- *External XTAL32/EXTAL32/RTC\_CLKIN clock frequency.*

## Driver version

- #define [FSL\\_CLOCK\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 2, 1))

## External clock frequency

*CLOCK driver version 2.2.1.*

### MCG frequency functions.

- uint32\_t [CLOCK\\_GetOutClkFreq](#) (void)  
*Gets the MCG output clock (MCGOUTCLK) frequency.*
- uint32\_t [CLOCK\\_GetFllFreq](#) (void)  
*Gets the MCG FLL clock (MCGFLLCLK) frequency.*
- uint32\_t [CLOCK\\_GetInternalRefClkFreq](#) (void)  
*Gets the MCG internal reference clock (MCGIRCLK) frequency.*
- uint32\_t [CLOCK\\_GetFixedFreqClkFreq](#) (void)  
*Gets the MCG fixed frequency clock (MCGFFCLK) frequency.*
- uint32\_t [CLOCK\\_GetPll0Freq](#) (void)  
*Gets the MCG PLL0 clock (MCGPLL0CLK) frequency.*
- uint32\_t [CLOCK\\_GetExtPllFreq](#) (void)  
*Gets the MCG external PLL frequency.*
- void [CLOCK\\_SetExtPllFreq](#) (uint32\_t freq)  
*Sets the MCG external PLL frequency.*

### MCG clock configuration.

- static void [CLOCK\\_SetLowPowerEnable](#) (bool enable)  
*Enables or disables the MCG low power.*
- status\_t [CLOCK\\_SetInternalRefClkConfig](#) (uint8\_t enableMode, [mcg\\_irc\\_mode\\_t](#) ircs, uint8\_t fcrdiv)  
*Configures the Internal Reference clock (MCGIRCLK).*
- status\_t [CLOCK\\_SetExternalRefClkConfig](#) ([mcg\\_oscsel\\_t](#) oscsel)  
*Selects the MCG external reference clock.*
- static void [CLOCK\\_SetFllExtRefDiv](#) (uint8\_t frdiv)  
*Set the FLL external reference clock divider value.*
- void [CLOCK\\_EnablePll0](#) ([mcg\\_pll\\_config\\_t](#) const \*config)  
*Enables the PLL0 in FLL mode.*
- static void [CLOCK\\_DisablePll0](#) (void)  
*Disables the PLL0 in FLL mode.*
- uint32\_t [CLOCK\\_CalcPllDiv](#) (uint32\_t refFreq, uint32\_t desireFreq, uint8\_t \*prdiv, uint8\_t \*vdiv)  
*Calculates the PLL divider setting for a desired output frequency.*
- void [CLOCK\\_SetPllClkSel](#) ([mcg\\_pll\\_clk\\_select\\_t](#) pllcs)  
*Set the PLL selection.*

### MCG clock lock monitor functions.

- void [CLOCK\\_SetOsc0MonitorMode](#) ([mcg\\_monitor\\_mode\\_t](#) mode)  
*Sets the OSC0 clock monitor mode.*
- void [CLOCK\\_SetRtcOscMonitorMode](#) ([mcg\\_monitor\\_mode\\_t](#) mode)  
*Sets the RTC OSC clock monitor mode.*
- void [CLOCK\\_SetPll0MonitorMode](#) ([mcg\\_monitor\\_mode\\_t](#) mode)  
*Sets the PLL0 clock monitor mode.*
- void [CLOCK\\_SetExtPllMonitorMode](#) ([mcg\\_monitor\\_mode\\_t](#) mode)  
*Sets the external PLL clock monitor mode.*
- uint32\_t [CLOCK\\_GetStatusFlags](#) (void)  
*Gets the MCG status flags.*

- void [CLOCK\\_ClearStatusFlags](#) (uint32\_t mask)  
*Clears the MCG status flags.*

## OSC configuration

- static void [OSC\\_SetExtRefClkConfig](#) (OSC\_Type \*base, [oscer\\_config\\_t](#) const \*config)  
*Configures the OSC external reference clock (OSCERCLK).*
- static void [OSC\\_SetCapLoad](#) (OSC\_Type \*base, uint8\_t capLoad)  
*Sets the capacitor load configuration for the oscillator.*
- void [CLOCK\\_InitOsc0](#) ([osc\\_config\\_t](#) const \*config)  
*Initializes the OSC0.*
- void [CLOCK\\_DeinitOsc0](#) (void)  
*Deinitializes the OSC0.*

## External clock frequency

- static void [CLOCK\\_SetXtal0Freq](#) (uint32\_t freq)  
*Sets the XTAL0 frequency based on board settings.*
- static void [CLOCK\\_SetXtal32Freq](#) (uint32\_t freq)  
*Sets the XTAL32/RTC\_CLKIN frequency based on board settings.*

## MCG auto-trim machine.

- status\_t [CLOCK\\_TrimInternalRefClk](#) (uint32\_t extFreq, uint32\_t desireFreq, uint32\_t \*actualFreq, [mcg\\_atm\\_select\\_t](#) atms)  
*Auto trims the internal reference clock.*

## MCG mode functions.

- [mcg\\_mode\\_t](#) [CLOCK\\_GetMode](#) (void)  
*Gets the current MCG mode.*
- status\_t [CLOCK\\_SetFeiMode](#) ([mcg\\_dmx32\\_t](#) dmx32, [mcg\\_drs\\_t](#) drs, void(\*flStableDelay)(void))  
*Sets the MCG to FEI mode.*
- status\_t [CLOCK\\_SetFeeMode](#) (uint8\_t frdiv, [mcg\\_dmx32\\_t](#) dmx32, [mcg\\_drs\\_t](#) drs, void(\*flStableDelay)(void))  
*Sets the MCG to FEE mode.*
- status\_t [CLOCK\\_SetFbiMode](#) ([mcg\\_dmx32\\_t](#) dmx32, [mcg\\_drs\\_t](#) drs, void(\*flStableDelay)(void))  
*Sets the MCG to FBI mode.*
- status\_t [CLOCK\\_SetFbeMode](#) (uint8\_t frdiv, [mcg\\_dmx32\\_t](#) dmx32, [mcg\\_drs\\_t](#) drs, void(\*flStableDelay)(void))  
*Sets the MCG to FBE mode.*
- status\_t [CLOCK\\_SetBlpiMode](#) (void)  
*Sets the MCG to BLPI mode.*
- status\_t [CLOCK\\_SetBlpeMode](#) (void)  
*Sets the MCG to BLPE mode.*
- status\_t [CLOCK\\_SetPbeMode](#) ([mcg\\_pll\\_clk\\_select\\_t](#) pllcs, [mcg\\_pll\\_config\\_t](#) const \*config)  
*Sets the MCG to PBE mode.*
- status\_t [CLOCK\\_SetPeeMode](#) (void)  
*Sets the MCG to PEE mode.*
- status\_t [CLOCK\\_ExternalModeToFbeModeQuick](#) (void)

## Data Structure Documentation

- Switches the MCG to FBE mode from the external mode.  
• status\_t [CLOCK\\_InternalModeToFbiModeQuick](#) (void)
- Switches the MCG to FBI mode from internal modes.  
• status\_t [CLOCK\\_BootToFeiMode](#) ([mcg\\_dmx32\\_t](#) dmx32, [mcg\\_drs\\_t](#) drs, void(\*fllStableDelay)(void))
- Sets the MCG to FEI mode during system boot up.  
• status\_t [CLOCK\\_BootToFeeMode](#) ([mcg\\_oscsel\\_t](#) oscsel, uint8\_t frdiv, [mcg\\_dmx32\\_t](#) dmx32, [mcg\\_drs\\_t](#) drs, void(\*fllStableDelay)(void))
- Sets the MCG to FEE mode during system bootup.  
• status\_t [CLOCK\\_BootToBlpiMode](#) (uint8\_t fcrdiv, [mcg\\_irc\\_mode\\_t](#) ircs, uint8\_t ircEnableMode)
- Sets the MCG to BLPI mode during system boot up.  
• status\_t [CLOCK\\_BootToBlpeMode](#) ([mcg\\_oscsel\\_t](#) oscsel)
- Sets the MCG to BLPE mode during sytem boot up.  
• status\_t [CLOCK\\_BootToPeeMode](#) ([mcg\\_oscsel\\_t](#) oscsel, [mcg\\_pll\\_clk\\_select\\_t](#) pllcs, [mcg\\_pll\\_config\\_t](#) const \*config)
- Sets the MCG to PEE mode during system boot up.  
• status\_t [CLOCK\\_SetMcgConfig](#) ([mcg\\_config\\_t](#) const \*config)
- Sets the MCG to a target mode.

## 42.4 Data Structure Documentation

### 42.4.1 struct sim\_clock\_config\_t

#### Data Fields

- uint8\_t [pllFllSel](#)  
*PLL/FLL/IRC48M selection.*
- uint8\_t [pllFllDiv](#)  
*PLL/FLLSEL clock divider divisor.*
- uint8\_t [pllFllFrac](#)  
*PLL/FLLSEL clock divider fraction.*
- uint8\_t [er32kSrc](#)  
*ERCLK32K source selection.*
- uint32\_t [clkdiv1](#)  
*SIM\_CLKDIV1.*

**42.4.1.0.0.97 Field Documentation****42.4.1.0.0.97.1** `uint8_t sim_clock_config_t::pllFllSel`**42.4.1.0.0.97.2** `uint8_t sim_clock_config_t::pllFllDiv`**42.4.1.0.0.97.3** `uint8_t sim_clock_config_t::pllFllFrac`**42.4.1.0.0.97.4** `uint8_t sim_clock_config_t::er32kSrc`**42.4.1.0.0.97.5** `uint32_t sim_clock_config_t::clkdiv1`**42.4.2 struct oscr\_config\_t****Data Fields**

- `uint8_t enableMode`  
*OSCECLK enable mode.*
- `uint8_t erclkDiv`  
*Divider for OSCECLK.*

**42.4.2.0.0.98 Field Documentation****42.4.2.0.0.98.1** `uint8_t oscr_config_t::enableMode`OR'ed value of `_oscer_enable_mode`.**42.4.2.0.0.98.2** `uint8_t oscr_config_t::erclkDiv`**42.4.3 struct osc\_config\_t**

Defines the configuration data structure to initialize the OSC. When porting to a new board, set the following members according to the board setting:

1. `freq`: The external frequency.
2. `workMode`: The OSC module mode.

**Data Fields**

- `uint32_t freq`  
*External clock frequency.*
- `uint8_t capLoad`  
*Capacitor load setting.*
- `osc_mode_t workMode`  
*OSC work mode setting.*
- `oscer_config_t oscerConfig`  
*Configuration for OSCECLK.*

## Data Structure Documentation

### 42.4.3.0.0.99 Field Documentation

42.4.3.0.0.99.1 `uint32_t osc_config_t::freq`

42.4.3.0.0.99.2 `uint8_t osc_config_t::capLoad`

42.4.3.0.0.99.3 `osc_mode_t osc_config_t::workMode`

42.4.3.0.0.99.4 `oscer_config_t osc_config_t::oscerConfig`

### 42.4.4 `struct mcg_pll_config_t`

#### Data Fields

- `uint8_t enableMode`  
*Enable mode.*
- `uint8_t prdiv`  
*Reference divider PRDIV.*
- `uint8_t vdiv`  
*VCO divider VDIV.*

### 42.4.4.0.0.100 Field Documentation

42.4.4.0.0.100.1 `uint8_t mcg_pll_config_t::enableMode`

OR'ed value of `_mcg_pll_enable_mode`.

42.4.4.0.0.100.2 `uint8_t mcg_pll_config_t::prdiv`

42.4.4.0.0.100.3 `uint8_t mcg_pll_config_t::vdiv`

### 42.4.5 `struct mcg_config_t`

When porting to a new board, set the following members according to the board setting:

1. `frdiv`: If the FLL uses the external reference clock, set this value to ensure that the external reference clock divided by `frdiv` is in the 31.25 kHz to 39.0625 kHz range.
2. The PLL reference clock divider `PRDIV`: PLL reference clock frequency after `PRDIV` should be in the `FSL_FEATURE_MCG_PLL_REF_MIN` to `FSL_FEATURE_MCG_PLL_REF_MAX` range.

#### Data Fields

- `mcg_mode_t mcgMode`  
*MCG mode.*
- `uint8_t irclkEnableMode`  
*MCGIRCLK enable mode.*
- `mcg_irc_mode_t ircs`  
*Source, `MCG_C2[IRCS]`.*

- `uint8_t fcrdiv`  
*Divider, MCG\_SC[FCRDIV].*
- `uint8_t frdiv`  
*Divider MCG\_C1[FRDIV].*
- `mcg_drs_t drs`  
*DCO range MCG\_C4[DRST\_DRS].*
- `mcg_dmx32_t dmx32`  
*MCG\_C4[DMX32].*
- `mcg_oscsel_t oscsel`  
*OSC select MCG\_C7[OSCSSEL].*
- `mcg_pll_config_t pll0Config`  
*MCGPLL0CLK configuration.*
- `mcg_pll_clk_select_t pllcs`  
*PLL select as output, PLLCS.*

#### 42.4.5.0.0.101 Field Documentation

- 42.4.5.0.0.101.1 `mcg_mode_t mcg_config_t::mcgMode`
- 42.4.5.0.0.101.2 `uint8_t mcg_config_t::ircclkEnableMode`
- 42.4.5.0.0.101.3 `mcg_irc_mode_t mcg_config_t::ircs`
- 42.4.5.0.0.101.4 `uint8_t mcg_config_t::fcrdiv`
- 42.4.5.0.0.101.5 `uint8_t mcg_config_t::frdiv`
- 42.4.5.0.0.101.6 `mcg_drs_t mcg_config_t::drs`
- 42.4.5.0.0.101.7 `mcg_dmx32_t mcg_config_t::dmx32`
- 42.4.5.0.0.101.8 `mcg_oscsel_t mcg_config_t::oscsel`
- 42.4.5.0.0.101.9 `mcg_pll_config_t mcg_config_t::pll0Config`
- 42.4.5.0.0.101.10 `mcg_pll_clk_select_t mcg_config_t::pllcs`

## 42.5 Macro Definition Documentation

### 42.5.1 `#define FSL_SDK_DISABLE_DRIVER_CLOCK_CONTROL 0`

When set to 0, peripheral drivers will enable clock in initialize function and disable clock in de-initialize function. When set to 1, peripheral driver will not control the clock, application could control the clock out of the driver.

#### Note

All drivers share this feature switcher. If it is set to 1, application should handle clock enable and disable for all drivers.

### 42.5.2 #define FSL\_CLOCK\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 1))

### 42.5.3 #define MCG\_INTERNAL\_IRC\_48M 48000000U

### 42.5.4 #define DMAMUX\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Dmamux0 \
}
```

### 42.5.5 #define RTC\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Rtc0 \
}
```

### 42.5.6 #define ENET\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Enet0 \
}
```

### 42.5.7 #define PORT\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_PortA, kCLOCK_PortB, kCLOCK_PortC, kCLOCK_PortD, kCLOCK_PortE \
}
```

### 42.5.8 #define SAI\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Sai0 \
}
```



### 42.5.9 #define FLEXBUS\_CLOCKS

Value:

```
{  
    \kCLOCK_Flexbus0 \  
}
```

### 42.5.10 #define TSI\_CLOCKS

Value:

```
{  
    \kCLOCK_Tsi0 \  
}
```

### 42.5.11 #define LPUART\_CLOCKS

Value:

```
{  
    \kCLOCK_Lpuart0 \  
}
```

### 42.5.12 #define EWM\_CLOCKS

Value:

```
{  
    \kCLOCK_Ewm0 \  
}
```

### 42.5.13 #define PIT\_CLOCKS

Value:

```
{  
    \kCLOCK_Pit0 \  
}
```

### 42.5.14 #define DSPI\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Spi0, kCLOCK_Spi1, kCLOCK_Spi2 \
}
```

### 42.5.15 #define LPTMR\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Lptmr0 \
}
```

### 42.5.16 #define SDHC\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Sdhc0 \
}
```

### 42.5.17 #define FTM\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Ftm0, kCLOCK_Ftm1, kCLOCK_Ftm2, kCLOCK_Ftm3 \
}
```

### 42.5.18 #define EDMA\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Dma0 \
}
```

### 42.5.19 #define FLEXCAN\_CLOCKS

Value:

```
{
    kCLOCK_Flexcan0, kCLOCK_Flexcan1 \
}
```

### 42.5.20 #define DAC\_CLOCKS

Value:

```
{
    kCLOCK_Dac0, kCLOCK_Dac1 \
}
```

### 42.5.21 #define ADC16\_CLOCKS

Value:

```
{
    kCLOCK_Adc0, kCLOCK_Adc1 \
}
```

### 42.5.22 #define SDRAM\_CLOCKS

Value:

```
{
    kCLOCK_Sdramc0 \
}
```

### 42.5.23 #define MPU\_CLOCKS

Value:

```
{
    kCLOCK_Mpu0 \
}
```

### 42.5.24 #define VREF\_CLOCKS

Value:

```
{
    kCLOCK_Vref0 \
}
```

### 42.5.25 #define CMT\_CLOCKS

Value:

```
{
    kCLOCK_Cmt0 \
}
```

### 42.5.26 #define UART\_CLOCKS

Value:

```
{
    kCLOCK_Uart0, kCLOCK_Uart1, kCLOCK_Uart2, kCLOCK_Uart3, kCLOCK_Uart4 \
}
```

### 42.5.27 #define TPM\_CLOCKS

Value:

```
{
    kCLOCK_IpInvalid, kCLOCK_Tpm1, kCLOCK_Tpm2 \
}
```

### 42.5.28 #define RNGA\_CLOCKS

Value:

```
{
    kCLOCK_Rnga0 \
}
```

#### 42.5.29 #define CRC\_CLOCKS

Value:

```
{  
    \kCLOCK_Crc0 \  
}
```

#### 42.5.30 #define I2C\_CLOCKS

Value:

```
{  
    \kCLOCK_I2c0, kCLOCK_I2c1, kCLOCK_I2c2, kCLOCK_I2c3 \  
}
```

#### 42.5.31 #define PDB\_CLOCKS

Value:

```
{  
    \kCLOCK_Pdb0 \  
}
```

#### 42.5.32 #define FTF\_CLOCKS

Value:

```
{  
    \kCLOCK_Ftf0 \  
}
```

#### 42.5.33 #define CMP\_CLOCKS

Value:

```
{  
    \kCLOCK_Cmp0, kCLOCK_Cmp1, kCLOCK_Cmp2, kCLOCK_Cmp3 \  
}
```

## Enumeration Type Documentation

### 42.5.34 #define SYS\_CLK kCLOCK\_CoreSysClk

## 42.6 Enumeration Type Documentation

### 42.6.1 enum clock\_name\_t

Enumerator

*kCLOCK\_CoreSysClk* Core/system clock.  
*kCLOCK\_PlatClk* Platform clock.  
*kCLOCK\_BusClk* Bus clock.  
*kCLOCK\_FlexBusClk* FlexBus clock.  
*kCLOCK\_FlashClk* Flash clock.  
*kCLOCK\_FastPeriphClk* Fast peripheral clock.  
*kCLOCK\_PllFllSelClk* The clock after SIM[PLL\_FLLSEL].  
*kCLOCK\_Er32kClk* External reference 32K clock (ERCLK32K)  
*kCLOCK\_Osc0ErClk* OSC0 external reference clock (OSC0ERCLK)  
*kCLOCK\_Osc1ErClk* OSC1 external reference clock (OSC1ERCLK)  
*kCLOCK\_Osc0ErClkUndiv* OSC0 external reference undivided clock(OSC0ERCLK\_UNDIV).  
*kCLOCK\_McgFixedFreqClk* MCG fixed frequency clock (MCGFFCLK)  
*kCLOCK\_McgInternalRefClk* MCG internal reference clock (MCGIRCLK)  
*kCLOCK\_McgFllClk* MCGFLLCLK.  
*kCLOCK\_McgPll0Clk* MCGPLL0CLK.  
*kCLOCK\_McgPll1Clk* MCGPLL1CLK.  
*kCLOCK\_McgExtPllClk* EXT\_PLLCLK.  
*kCLOCK\_McgPeriphClk* MCG peripheral clock (MCGPCLK)  
*kCLOCK\_McgIrc48MClk* MCG IRC48M clock.  
*kCLOCK\_LpoClk* LPO clock.

### 42.6.2 enum clock\_usb\_src\_t

Enumerator

*kCLOCK\_UsbSrcPll0* Use PLL0.  
*kCLOCK\_UsbSrcUsbPfd* Use USBPFDCLK.  
*kCLOCK\_UsbSrcIrc48M* Use IRC48M.  
*kCLOCK\_UsbSrcExt* Use USB\_CLKIN.  
*kCLOCK\_UsbSrcUnused* Used when the function does not care the clock source.

### 42.6.3 enum clock\_usb\_phy\_src\_t

Enumerator

*kCLOCK\_UsbPhySrcExt* Use external crystal.

#### 42.6.4 enum clock\_usb\_pfd\_src\_t

Enumerator

*kCLOCK\_UsbPfdSrcExt* Use external crystal.  
*kCLOCK\_UsbPfdSrcFracDivBy4* Use PFD\_FRAC output divided by 4.  
*kCLOCK\_UsbPfdSrcFracDivBy2* Use PFD\_FRAC output divided by 2.  
*kCLOCK\_UsbPfdSrcFrac* Use PFD\_FRAC output.

#### 42.6.5 enum clock\_ip\_name\_t

#### 42.6.6 enum osc\_mode\_t

Enumerator

*kOSC\_ModeExt* Use an external clock.  
*kOSC\_ModeOscLowPower* Oscillator low power.  
*kOSC\_ModeOscHighGain* Oscillator high gain.

#### 42.6.7 enum \_osc\_cap\_load

Enumerator

*kOSC\_Cap2P* 2 pF capacitor load  
*kOSC\_Cap4P* 4 pF capacitor load  
*kOSC\_Cap8P* 8 pF capacitor load  
*kOSC\_Cap16P* 16 pF capacitor load

#### 42.6.8 enum \_oscer\_enable\_mode

Enumerator

*kOSC\_ErClkEnable* Enable.  
*kOSC\_ErClkEnableInStop* Enable in stop mode.

#### 42.6.9 enum mcg\_fll\_src\_t

Enumerator

*kMCG\_FllSrcExternal* External reference clock is selected.  
*kMCG\_FllSrcInternal* The slow internal reference clock is selected.

## Enumeration Type Documentation

### 42.6.10 enum mcg\_irc\_mode\_t

Enumerator

*kMCG\_IrcSlow* Slow internal reference clock selected.

*kMCG\_IrcFast* Fast internal reference clock selected.

### 42.6.11 enum mcg\_dm32\_t

Enumerator

*kMCG\_Dm32Default* DCO has a default range of 25%.

*kMCG\_Dm32Fine* DCO is fine-tuned for maximum frequency with 32.768 kHz reference.

### 42.6.12 enum mcg\_drs\_t

Enumerator

*kMCG\_DrsLow* Low frequency range.

*kMCG\_DrsMid* Mid frequency range.

*kMCG\_DrsMidHigh* Mid-High frequency range.

*kMCG\_DrsHigh* High frequency range.

### 42.6.13 enum mcg\_pll\_ref\_src\_t

Enumerator

*kMCG\_PllRefOsc0* Selects OSC0 as PLL reference clock.

*kMCG\_PllRefOsc1* Selects OSC1 as PLL reference clock.

### 42.6.14 enum mcg\_clkout\_src\_t

Enumerator

*kMCG\_ClkOutSrcOut* Output of the FLL is selected (reset default)

*kMCG\_ClkOutSrcInternal* Internal reference clock is selected.

*kMCG\_ClkOutSrcExternal* External reference clock is selected.



### 42.6.15 enum mcg\_atm\_select\_t

Enumerator

*kMCG\_AtmSel32k* 32 kHz Internal Reference Clock selected

*kMCG\_AtmSel4m* 4 MHz Internal Reference Clock selected

### 42.6.16 enum mcg\_oscsel\_t

Enumerator

*kMCG\_OscselOsc* Selects System Oscillator (OSCCLK)

*kMCG\_OscselRtc* Selects 32 kHz RTC Oscillator.

*kMCG\_OscselIrc* Selects 48 MHz IRC Oscillator.

### 42.6.17 enum mcg\_pll\_clk\_select\_t

Enumerator

*kMCG\_PllClkSelPll0* PLL0 output clock is selected.

### 42.6.18 enum mcg\_monitor\_mode\_t

Enumerator

*kMCG\_MonitorNone* Clock monitor is disabled.

*kMCG\_MonitorInt* Trigger interrupt when clock lost.

*kMCG\_MonitorReset* System reset when clock lost.

### 42.6.19 enum \_mcg\_status

Enumerator

*kStatus\_MCG\_ModeUnreachable* Can't switch to target mode.

*kStatus\_MCG\_ModeInvalid* Current mode invalid for the specific function.

*kStatus\_MCG\_AtmBusClockInvalid* Invalid bus clock for ATM.

*kStatus\_MCG\_AtmDesiredFreqInvalid* Invalid desired frequency for ATM.

*kStatus\_MCG\_AtmIrcUsed* IRC is used when using ATM.

*kStatus\_MCG\_AtmHardwareFail* Hardware fail occurs during ATM.

*kStatus\_MCG\_SourceUsed* Can't change the clock source because it is in use.

### 42.6.20 enum \_mcg\_status\_flags\_t

Enumerator

*kMCG\_Osc0LostFlag* OSC0 lost.  
*kMCG\_Osc0InitFlag* OSC0 crystal initialized.  
*kMCG\_RtcOscLostFlag* RTC OSC lost.  
*kMCG\_Pll0LostFlag* PLL0 lost.  
*kMCG\_Pll0LockFlag* PLL0 locked.  
*kMCG\_ExtPllLostFlag* External PLL lost.

### 42.6.21 enum \_mcg\_ircclk\_enable\_mode

Enumerator

*kMCG\_IrcclkEnable* MCGIRCLK enable.  
*kMCG\_IrcclkEnableInStop* MCGIRCLK enable in stop mode.

### 42.6.22 enum \_mcg\_pll\_enable\_mode

Enumerator

*kMCG\_PllEnableIndependent* MCGPLLCLK enable independent of the MCG clock mode. Generally, the PLL is disabled in FLL modes (FEI/FBI/FEE/FBE). Setting the PLL clock enable independent, enables the PLL in the FLL modes.  
*kMCG\_PllEnableInStop* MCGPLLCLK enable in STOP mode.

### 42.6.23 enum mcg\_mode\_t

Enumerator

*kMCG\_ModeFEI* FEI - FLL Engaged Internal.  
*kMCG\_ModeFBI* FBI - FLL Bypassed Internal.  
*kMCG\_ModeBLPI* BLPI - Bypassed Low Power Internal.  
*kMCG\_ModeFEE* FEE - FLL Engaged External.  
*kMCG\_ModeFBE* FBE - FLL Bypassed External.  
*kMCG\_ModeBLPE* BLPE - Bypassed Low Power External.  
*kMCG\_ModePBE* PBE - PLL Bypassed External.  
*kMCG\_ModePEE* PEE - PLL Engaged External.  
*kMCG\_ModeError* Unknown mode.

## 42.7 Function Documentation

42.7.1 `static void CLOCK_EnableClock ( clock_ip_name_t name ) [inline],  
[static]`

## Function Documentation

### Parameters

|             |                                                              |
|-------------|--------------------------------------------------------------|
| <i>name</i> | Which clock to enable, see <a href="#">clock_ip_name_t</a> . |
|-------------|--------------------------------------------------------------|

**42.7.2 static void CLOCK\_DisableClock ( clock\_ip\_name\_t *name* ) [inline], [static]**

### Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>name</i> | Which clock to disable, see <a href="#">clock_ip_name_t</a> . |
|-------------|---------------------------------------------------------------|

**42.7.3 static void CLOCK\_SetEr32kClock ( uint32\_t *src* ) [inline], [static]**

### Parameters

|            |                                         |
|------------|-----------------------------------------|
| <i>src</i> | The value to set ERCLK32K clock source. |
|------------|-----------------------------------------|

**42.7.4 static void CLOCK\_SetSdhc0Clock ( uint32\_t *src* ) [inline], [static]**

### Parameters

|            |                                      |
|------------|--------------------------------------|
| <i>src</i> | The value to set SDHC0 clock source. |
|------------|--------------------------------------|

**42.7.5 static void CLOCK\_SetEnetTime0Clock ( uint32\_t *src* ) [inline], [static]**

### Parameters

|            |                                               |
|------------|-----------------------------------------------|
| <i>src</i> | The value to set enet timestamp clock source. |
|------------|-----------------------------------------------|

**42.7.6 static void CLOCK\_SetRmii0Clock ( uint32\_t *src* ) [inline], [static]**

## Parameters

|            |                                     |
|------------|-------------------------------------|
| <i>src</i> | The value to set RMII clock source. |
|------------|-------------------------------------|

**42.7.7 static void CLOCK\_SetLpuartClock ( uint32\_t *src* ) [inline], [static]**

## Parameters

|            |                                       |
|------------|---------------------------------------|
| <i>src</i> | The value to set LPUART clock source. |
|------------|---------------------------------------|

**42.7.8 static void CLOCK\_SetTpmClock ( uint32\_t *src* ) [inline], [static]**

## Parameters

|            |                                    |
|------------|------------------------------------|
| <i>src</i> | The value to set TPM clock source. |
|------------|------------------------------------|

**42.7.9 static void CLOCK\_SetTraceClock ( uint32\_t *src*, uint32\_t *divValue*, uint32\_t *fracValue* ) [inline], [static]**

## Parameters

|            |                                            |
|------------|--------------------------------------------|
| <i>src</i> | The value to set debug trace clock source. |
|------------|--------------------------------------------|

**42.7.10 static void CLOCK\_SetPllFllSelClock ( uint32\_t *src*, uint32\_t *divValue*, uint32\_t *fracValue* ) [inline], [static]**

## Parameters

|            |                                          |
|------------|------------------------------------------|
| <i>src</i> | The value to set PLLFLLSEL clock source. |
|------------|------------------------------------------|

**42.7.11 static void CLOCK\_SetClkOutClock ( uint32\_t *src* ) [inline], [static]**

## Function Documentation

### Parameters

|            |                                 |
|------------|---------------------------------|
| <i>src</i> | The value to set CLKOUT source. |
|------------|---------------------------------|

### 42.7.12 static void CLOCK\_SetRtcClkOutClock ( uint32\_t *src* ) [inline], [static]

### Parameters

|            |                                     |
|------------|-------------------------------------|
| <i>src</i> | The value to set RTC_CLKOUT source. |
|------------|-------------------------------------|

### 42.7.13 bool CLOCK\_EnableUsbhs0Clock ( clock\_usb\_src\_t *src*, uint32\_t *freq* )

This function only enables the access to USB HS peripheral, upper layer should first call the [CLOCK\\_EnableUsbhs0PhyPllClock](#) to enable the PHY clock to use USB HS.

### Parameters

|             |                                                                                                |
|-------------|------------------------------------------------------------------------------------------------|
| <i>src</i>  | USB HS does not care about the clock source, here must be <a href="#">kCLOCK_UsbSrc_Used</a> . |
| <i>freq</i> | USB HS does not care about the clock source, so this parameter is ignored.                     |

### Return values

|              |                                                         |
|--------------|---------------------------------------------------------|
| <i>true</i>  | The clock is set successfully.                          |
| <i>false</i> | The clock source is invalid to get proper USB HS clock. |

### 42.7.14 void CLOCK\_DisableUsbhs0Clock ( void )

Disable USB HS clock, this function should not be called after [CLOCK\\_DisableUsbhs0PhyPllClock](#).

### 42.7.15 bool CLOCK\_EnableUsbhs0PhyPllClock ( clock\_usb\_phy\_src\_t *src*, uint32\_t *freq* )

This function enables the internal 480MHz USB PHY PLL clock.

## Parameters

|             |                                         |
|-------------|-----------------------------------------|
| <i>src</i>  | USB HS PHY PLL clock source.            |
| <i>freq</i> | The frequency specified by <i>src</i> . |

## Return values

|              |                                                         |
|--------------|---------------------------------------------------------|
| <i>true</i>  | The clock is set successfully.                          |
| <i>false</i> | The clock source is invalid to get proper USB HS clock. |

**42.7.16 void CLOCK\_DisableUsbhs0PhyPllClock ( void )**

This function disables USB HS PHY PLL clock.

**42.7.17 void CLOCK\_EnableUsbhs0PfdClock ( uint8\_t *frac*, clock\_usb\_pfd\_src\_t *src* )**

This function enables USB HS PFD clock. It should be called after function [CLOCK\\_EnableUsbhs0PhyPllClock](#). The PFD output clock is selected by the parameter *src*. When the *src* is [kCLOCK\\_UsbPfdSrcExt](#), then the PFD output is from external crystal directly, in this case, the *frac* is not used. In other cases, the PFD\_FRAC output clock frequency is 480MHz\*18/frac, the PFD output frequency is based on the PFD\_FRAC output.

## Parameters

|             |                                                                 |
|-------------|-----------------------------------------------------------------|
| <i>frac</i> | The value set to PFD_FRAC, it must be in the range of 18 to 35. |
| <i>src</i>  | Source of the USB HS PFD clock (USB1PFDCLK).                    |

**42.7.18 void CLOCK\_DisableUsbhs0PfdClock ( void )**

This function disables USB HS PFD clock. It should be called before function [CLOCK\\_DisableUsbhs0PhyPllClock](#).

**42.7.19 bool CLOCK\_EnableUsbfs0Clock ( clock\_usb\_src\_t *src*, uint32\_t *freq* )**

## Function Documentation

### Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>src</i>  | USB FS clock source.            |
| <i>freq</i> | The frequency specified by src. |

### Return values

|              |                                                         |
|--------------|---------------------------------------------------------|
| <i>true</i>  | The clock is set successfully.                          |
| <i>false</i> | The clock source is invalid to get proper USB FS clock. |

#### 42.7.20 static void CLOCK\_DisableUsbfs0Clock ( void ) [inline], [static]

Disable USB FS clock.

#### 42.7.21 static void CLOCK\_SetOutDiv ( uint32\_t outdiv1, uint32\_t outdiv2, uint32\_t outdiv3, uint32\_t outdiv4 ) [inline], [static]

Set the SIM\_CLKDIV1[OUTDIV1], SIM\_CLKDIV1[OUTDIV2], SIM\_CLKDIV1[OUTDIV3], SIM\_CLKDIV1[OUTDIV4].

### Parameters

|                |                               |
|----------------|-------------------------------|
| <i>outdiv1</i> | Clock 1 output divider value. |
| <i>outdiv2</i> | Clock 2 output divider value. |
| <i>outdiv3</i> | Clock 3 output divider value. |
| <i>outdiv4</i> | Clock 4 output divider value. |

#### 42.7.22 uint32\_t CLOCK\_GetFreq ( clock\_name\_t clockName )

This function checks the current clock configurations and then calculates the clock frequency for a specific clock name defined in clock\_name\_t. The MCG must be properly configured before using this function.

### Parameters



|                  |                                     |
|------------------|-------------------------------------|
| <i>clockName</i> | Clock names defined in clock_name_t |
|------------------|-------------------------------------|

Returns

Clock frequency value in Hertz

#### 42.7.23 uint32\_t CLOCK\_GetCoreSysClkFreq ( void )

Returns

Clock frequency in Hz.

#### 42.7.24 uint32\_t CLOCK\_GetPlatClkFreq ( void )

Returns

Clock frequency in Hz.

#### 42.7.25 uint32\_t CLOCK\_GetBusClkFreq ( void )

Returns

Clock frequency in Hz.

#### 42.7.26 uint32\_t CLOCK\_GetFlexBusClkFreq ( void )

Returns

Clock frequency in Hz.

#### 42.7.27 uint32\_t CLOCK\_GetFlashClkFreq ( void )

Returns

Clock frequency in Hz.

## Function Documentation

### 42.7.28 `uint32_t CLOCK_GetPIIFllSelClkFreq ( void )`

Returns

Clock frequency in Hz.

### 42.7.29 `uint32_t CLOCK_GetEr32kClkFreq ( void )`

Returns

Clock frequency in Hz.

### 42.7.30 `uint32_t CLOCK_GetOsc0ErClkFreq ( void )`

Returns

Clock frequency in Hz.

### 42.7.31 `uint32_t CLOCK_GetOsc0ErClkUndivFreq ( void )`

Returns

Clock frequency in Hz.

### 42.7.32 `void CLOCK_SetSimConfig ( sim_clock_config_t const * config )`

This function sets system layer clock settings in SIM module.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>config</i> | Pointer to the configure structure. |
|---------------|-------------------------------------|

### 42.7.33 `static void CLOCK_SetSimSafeDivs ( void ) [inline], [static]`

The system level clocks (core clock, bus clock, flexbus clock and flash clock) must be in allowed ranges. During MCG clock mode switch, the MCG output clock changes then the system level clocks may be out of range. This function could be used before MCG mode change, to make sure system level clocks are in allowed range.

## Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>config</i> | Pointer to the configure structure. |
|---------------|-------------------------------------|

**42.7.34 uint32\_t CLOCK\_GetOutClkFreq ( void )**

This function gets the MCG output clock frequency in Hz based on the current MCG register value.

## Returns

The frequency of MCGOUTCLK.

**42.7.35 uint32\_t CLOCK\_GetFllFreq ( void )**

This function gets the MCG FLL clock frequency in Hz based on the current MCG register value. The FLL is enabled in FEI/FBI/FEE/FBE mode and disabled in low power state in other modes.

## Returns

The frequency of MCGFLLCLK.

**42.7.36 uint32\_t CLOCK\_GetInternalRefClkFreq ( void )**

This function gets the MCG internal reference clock frequency in Hz based on the current MCG register value.

## Returns

The frequency of MCGIRCLK.

**42.7.37 uint32\_t CLOCK\_GetFixedFreqClkFreq ( void )**

This function gets the MCG fixed frequency clock frequency in Hz based on the current MCG register value.

## Returns

The frequency of MCGFFCLK.

## Function Documentation

### 42.7.38 uint32\_t CLOCK\_GetPll0Freq ( void )

This function gets the MCG PLL0 clock frequency in Hz based on the current MCG register value.

Returns

The frequency of MCGPLL0CLK.

### 42.7.39 uint32\_t CLOCK\_GetExtPllFreq ( void )

This function gets the MCG external PLL frequency in Hz.

Returns

The frequency of the MCG external PLL.

### 42.7.40 void CLOCK\_SetExtPllFreq ( uint32\_t freq )

This function sets the MCG external PLL frequency in Hz. The MCG external PLL frequency is passed to the MCG driver using this function. Call this function after the external PLL frequency is changed. Otherwise, the APIs, which are used to get the frequency, may return an incorrect value.

Parameters

|            |                                |
|------------|--------------------------------|
| <i>The</i> | frequency of MCG external PLL. |
|------------|--------------------------------|

### 42.7.41 static void CLOCK\_SetLowPowerEnable ( bool enable ) [inline], [static]

Enabling the MCG low power disables the PLL and FLL in bypass modes. In other words, in FBE and PBE modes, enabling low power sets the MCG to BLPE mode. In FBI and PBI modes, enabling low power sets the MCG to BLPI mode. When disabling the MCG low power, the PLL or FLL are enabled based on MCG settings.

Parameters

|               |                                                               |
|---------------|---------------------------------------------------------------|
| <i>enable</i> | True to enable MCG low power, false to disable MCG low power. |
|---------------|---------------------------------------------------------------|

#### 42.7.42 **status\_t** CLOCK\_SetInternalRefClkConfig ( uint8\_t *enableMode*, mcg\_irc\_mode\_t *ircs*, uint8\_t *fcrdiv* )

This function sets the MCGIRCLK base on parameters. It also selects the IRC source. If the fast IRC is used, this function sets the fast IRC divider. This function also sets whether the MCGIRCLK is enabled in stop mode. Calling this function in FBI/PBI/BLPI modes may change the system clock. As a result, using the function in these modes it is not allowed.

Parameters

|                   |                                                                                |
|-------------------|--------------------------------------------------------------------------------|
| <i>enableMode</i> | MCGIRCLK enable mode, OR'ed value of <a href="#">_mcg_ircclk_enable_mode</a> . |
| <i>ircs</i>       | MCGIRCLK clock source, choose fast or slow.                                    |
| <i>fcrdiv</i>     | Fast IRC divider setting (FCRDIV).                                             |

Return values

|                                |                                                                                                                                      |
|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <i>kStatus_MCG_Source-Used</i> | Because the internal reference clock is used as a clock source, the configuration should not be changed. Otherwise, a glitch occurs. |
| <i>kStatus_Success</i>         | MCGIRCLK configuration finished successfully.                                                                                        |

#### 42.7.43 **status\_t** CLOCK\_SetExternalRefClkConfig ( mcg\_oscsel\_t *oscsel* )

Selects the MCG external reference clock source, changes the MCG\_C7[OSCSSEL], and waits for the clock source to be stable. Because the external reference clock should not be changed in FEE/FBE/BLP-E/PBE/PEE modes, do not call this function in these modes.

Parameters

|               |                                                       |
|---------------|-------------------------------------------------------|
| <i>oscsel</i> | MCG external reference clock source, MCG_C7[OSCSSEL]. |
|---------------|-------------------------------------------------------|

Return values

|                                |                                                                                                                                      |
|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <i>kStatus_MCG_Source-Used</i> | Because the external reference clock is used as a clock source, the configuration should not be changed. Otherwise, a glitch occurs. |
|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|

## Function Documentation

|                        |                                            |
|------------------------|--------------------------------------------|
| <i>kStatus_Success</i> | External reference clock set successfully. |
|------------------------|--------------------------------------------|

### 42.7.44 static void CLOCK\_SetFllExtRefDiv ( uint8\_t *frdiv* ) [inline], [static]

Sets the FLL external reference clock divider value, the register MCG\_C1[FRDIV].

Parameters

|              |                                                                |
|--------------|----------------------------------------------------------------|
| <i>frdiv</i> | The FLL external reference clock divider value, MCG_C1[FRDIV]. |
|--------------|----------------------------------------------------------------|

### 42.7.45 void CLOCK\_EnablePll0 ( mcg\_pll\_config\_t const \* *config* )

This function sets us the PLL0 in FLL mode and reconfigures the PLL0. Ensure that the PLL reference clock is enabled before calling this function and that the PLL0 is not used as a clock source. The function CLOCK\_CalcPllDiv gets the correct PLL divider values.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

### 42.7.46 static void CLOCK\_DisablePll0 ( void ) [inline], [static]

This function disables the PLL0 in FLL mode. It should be used together with the [CLOCK\\_EnablePll0](#).

### 42.7.47 uint32\_t CLOCK\_CalcPllDiv ( uint32\_t *refFreq*, uint32\_t *desireFreq*, uint8\_t \* *prdiv*, uint8\_t \* *vdiv* )

This function calculates the correct reference clock divider (PRDIV) and VCO divider (VDIV) to generate a desired PLL output frequency. It returns the closest frequency match with the corresponding PRDIV/-VDIV returned from parameters. If a desired frequency is not valid, this function returns 0.

Parameters

|                   |                                                |
|-------------------|------------------------------------------------|
| <i>refFreq</i>    | PLL reference clock frequency.                 |
| <i>desireFreq</i> | Desired PLL output frequency.                  |
| <i>prdiv</i>      | PRDIV value to generate desired PLL frequency. |
| <i>vdiv</i>       | VDIV value to generate desired PLL frequency.  |

Returns

Closest frequency match that the PLL was able generate.

#### 42.7.48 void CLOCK\_SetPllClkSel ( mcg\_pll\_clk\_select\_t *pllcs* )

This function sets the PLL selection between PLL0/PLL1/EXTPLL, and waits for change finished.

Parameters

|              |                    |
|--------------|--------------------|
| <i>pllcs</i> | The PLL to select. |
|--------------|--------------------|

#### 42.7.49 void CLOCK\_SetOsc0MonitorMode ( mcg\_monitor\_mode\_t *mode* )

This function sets the OSC0 clock monitor mode. See [mcg\\_monitor\\_mode\\_t](#) for details.

Parameters

|             |                      |
|-------------|----------------------|
| <i>mode</i> | Monitor mode to set. |
|-------------|----------------------|

#### 42.7.50 void CLOCK\_SetRtcOscMonitorMode ( mcg\_monitor\_mode\_t *mode* )

This function sets the RTC OSC clock monitor mode. See [mcg\\_monitor\\_mode\\_t](#) for details.

Parameters

|             |                      |
|-------------|----------------------|
| <i>mode</i> | Monitor mode to set. |
|-------------|----------------------|

#### 42.7.51 void CLOCK\_SetPll0MonitorMode ( mcg\_monitor\_mode\_t *mode* )

This function sets the PLL0 clock monitor mode. See [mcg\\_monitor\\_mode\\_t](#) for details.

## Function Documentation

### Parameters

|             |                      |
|-------------|----------------------|
| <i>mode</i> | Monitor mode to set. |
|-------------|----------------------|

### 42.7.52 void CLOCK\_SetExtPllMonitorMode ( mcg\_monitor\_mode\_t *mode* )

This function sets the external PLL clock monitor mode. See [mcg\\_monitor\\_mode\\_t](#) for details.

### Parameters

|             |                      |
|-------------|----------------------|
| <i>mode</i> | Monitor mode to set. |
|-------------|----------------------|

### 42.7.53 uint32\_t CLOCK\_GetStatusFlags ( void )

This function gets the MCG clock status flags. All status flags are returned as a logical OR of the enumeration [\\_mcg\\_status\\_flags\\_t](#). To check a specific flag, compare the return value with the flag.

Example:

```
// To check the clock lost lock status of OSC0 and PLL0.
uint32_t mcgFlags;

mcgFlags = CLOCK_GetStatusFlags();

if (mcgFlags & kMCG_Osc0LostFlag)
{
    // OSC0 clock lock lost. Do something.
}
if (mcgFlags & kMCG_Pll0LostFlag)
{
    // PLL0 clock lock lost. Do something.
}
```

### Returns

Logical OR value of the [\\_mcg\\_status\\_flags\\_t](#).

### 42.7.54 void CLOCK\_ClearStatusFlags ( uint32\_t *mask* )

This function clears the MCG clock lock lost status. The parameter is a logical OR value of the flags to clear. See [\\_mcg\\_status\\_flags\\_t](#).

Example:

```
// To clear the clock lost lock status flags of OSC0 and PLL0.
CLOCK_ClearStatusFlags(kMCG_Osc0LostFlag | kMCG_Pll0LostFlag);
```



## Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">_mcg_status_flags_t</a> . |
|-------------|---------------------------------------------------------------------------------------------------------------------|

#### 42.7.55 static void OSC\_SetExtRefClkConfig ( OSC\_Type \* *base*, oscr\_config\_t const \* *config* ) [inline], [static]

This function configures the OSC external reference clock (OSCERCLK). This is an example to enable the OSCERCLK in normal and stop modes and also set the output divider to 1:

```
oscer_config_t config =
{
    .enableMode = kOSC_ErClkEnable |
                kOSC_ErClkEnableInStop,
    .erclkDiv   = 1U,
};

OSC_SetExtRefClkConfig(OSC, &config);
```

## Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | OSC peripheral address.                 |
| <i>config</i> | Pointer to the configuration structure. |

#### 42.7.56 static void OSC\_SetCapLoad ( OSC\_Type \* *base*, uint8\_t *capLoad* ) [inline], [static]

This function sets the specified capacitors configuration for the oscillator. This should be done in the early system level initialization function call based on the system configuration.

## Parameters

|                |                                                                                |
|----------------|--------------------------------------------------------------------------------|
| <i>base</i>    | OSC peripheral address.                                                        |
| <i>capLoad</i> | OR'ed value for the capacitor load option, see <a href="#">_osc_cap_load</a> . |

## Example:

```
// To enable only 2 pF and 8 pF capacitor load, please use like this.
OSC_SetCapLoad(OSC, kOSC_Cap2P | kOSC_Cap8P);
```

#### 42.7.57 void CLOCK\_InitOsc0 ( osc\_config\_t const \* *config* )

This function initializes the OSC0 according to the board configuration.

## Function Documentation

### Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>config</i> | Pointer to the OSC0 configuration structure. |
|---------------|----------------------------------------------|

### 42.7.58 void CLOCK\_DeinitOsc0 ( void )

This function deinitializes the OSC0.

### 42.7.59 static void CLOCK\_SetXtal0Freq ( uint32\_t freq ) [inline], [static]

### Parameters

|             |                                               |
|-------------|-----------------------------------------------|
| <i>freq</i> | The XTAL0/EXTAL0 input clock frequency in Hz. |
|-------------|-----------------------------------------------|

### 42.7.60 static void CLOCK\_SetXtal32Freq ( uint32\_t freq ) [inline], [static]

### Parameters

|             |                                                           |
|-------------|-----------------------------------------------------------|
| <i>freq</i> | The XTAL32/EXTAL32/RTC_CLKIN input clock frequency in Hz. |
|-------------|-----------------------------------------------------------|

### 42.7.61 status\_t CLOCK\_TrimInternalRefClk ( uint32\_t extFreq, uint32\_t desireFreq, uint32\_t \* actualFreq, mcg\_atm\_select\_t atms )

This function trims the internal reference clock by using the external clock. If successful, it returns the kStatus\_Success and the frequency after trimming is received in the parameter *actualFreq*. If an error occurs, the error code is returned.

### Parameters

|                   |                                                        |
|-------------------|--------------------------------------------------------|
| <i>extFreq</i>    | External clock frequency, which should be a bus clock. |
| <i>desireFreq</i> | Frequency to trim to.                                  |
| <i>actualFreq</i> | Actual frequency after trimming.                       |

|             |                                             |
|-------------|---------------------------------------------|
| <i>atms</i> | Trim fast or slow internal reference clock. |
|-------------|---------------------------------------------|

Return values

|                                           |                                                                |
|-------------------------------------------|----------------------------------------------------------------|
| <i>kStatus_Success</i>                    | ATM success.                                                   |
| <i>kStatus_MCG_AtmBus-ClockInvalid</i>    | The bus clock is not in allowed range for the ATM.             |
| <i>kStatus_MCG_Atm-DesiredFreqInvalid</i> | MCGIRCLK could not be trimmed to the desired frequency.        |
| <i>kStatus_MCG_AtmIrc-Used</i>            | Could not trim because MCGIRCLK is used as a bus clock source. |
| <i>kStatus_MCG_Atm-HardwareFail</i>       | Hardware fails while trimming.                                 |

#### 42.7.62 **mcg\_mode\_t** CLOCK\_GetMode ( void )

This function checks the MCG registers and determines the current MCG mode.

Returns

Current MCG mode or error code; See [mcg\\_mode\\_t](#).

#### 42.7.63 **status\_t** CLOCK\_SetFeiMode ( mcg\_dm32\_t *dmx32*, mcg\_drs\_t *drs*, void(\*)*(void) fllStableDelay* )

This function sets the MCG to FEI mode. If setting to FEI mode fails from the current mode, this function returns an error.

Parameters

|                       |                                                                                       |
|-----------------------|---------------------------------------------------------------------------------------|
| <i>dmx32</i>          | DMX32 in FEI mode.                                                                    |
| <i>drs</i>            | The DCO range selection.                                                              |
| <i>fllStableDelay</i> | Delay function to ensure that the FLL is stable. Passing NULL does not cause a delay. |

Return values

## Function Documentation

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

### Note

If `dmx32` is set to `kMCG_Dmx32Fine`, the slow IRC must not be trimmed to a frequency above 32768 Hz.

#### 42.7.64 **status\_t** CLOCK\_SetFeeMode ( **uint8\_t** *frdiv*, **mcg\_dmx32\_t** *dmx32*, **mcg\_drs\_t** *drs*, **void(\*)**(**void**) *flStableDelay* )

This function sets the MCG to FEE mode. If setting to FEE mode fails from the current mode, this function returns an error.

### Parameters

|                      |                                                                                 |
|----------------------|---------------------------------------------------------------------------------|
| <i>frdiv</i>         | FLL reference clock divider setting, FRDIV.                                     |
| <i>dmx32</i>         | DMX32 in FEE mode.                                                              |
| <i>drs</i>           | The DCO range selection.                                                        |
| <i>flStableDelay</i> | Delay function to make sure FLL is stable. Passing NULL does not cause a delay. |

### Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

#### 42.7.65 **status\_t** CLOCK\_SetFbiMode ( **mcg\_dmx32\_t** *dmx32*, **mcg\_drs\_t** *drs*, **void(\*)**(**void**) *flStableDelay* )

This function sets the MCG to FBI mode. If setting to FBI mode fails from the current mode, this function returns an error.

### Parameters

|                       |                                                                                                                                                 |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>dmx32</i>          | DMX32 in FBI mode.                                                                                                                              |
| <i>drs</i>            | The DCO range selection.                                                                                                                        |
| <i>fllStableDelay</i> | Delay function to make sure FLL is stable. If the FLL is not used in FBI mode, this parameter can be NULL. Passing NULL does not cause a delay. |

## Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

## Note

If *dmx32* is set to *kMCG\_Dmx32Fine*, the slow IRC must not be trimmed to frequency above 32768 Hz.

#### 42.7.66 **status\_t** CLOCK\_SetFbeMode ( **uint8\_t** *frdiv*, **mcg\_dmx32\_t** *dmx32*, **mcg\_drs\_t** *drs*, **void(\*)**(**void**) *fllStableDelay* )

This function sets the MCG to FBE mode. If setting to FBE mode fails from the current mode, this function returns an error.

## Parameters

|                       |                                                                                                                                                 |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>frdiv</i>          | FLL reference clock divider setting, FRDIV.                                                                                                     |
| <i>dmx32</i>          | DMX32 in FBE mode.                                                                                                                              |
| <i>drs</i>            | The DCO range selection.                                                                                                                        |
| <i>fllStableDelay</i> | Delay function to make sure FLL is stable. If the FLL is not used in FBE mode, this parameter can be NULL. Passing NULL does not cause a delay. |

## Return values

|                                     |                                      |
|-------------------------------------|--------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode. |
|-------------------------------------|--------------------------------------|

## Function Documentation

|                        |                                           |
|------------------------|-------------------------------------------|
| <i>kStatus_Success</i> | Switched to the target mode successfully. |
|------------------------|-------------------------------------------|

### 42.7.67 **status\_t** CLOCK\_SetBlpiMode ( void )

This function sets the MCG to BLPI mode. If setting to BLPI mode fails from the current mode, this function returns an error.

Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

### 42.7.68 **status\_t** CLOCK\_SetBlpeMode ( void )

This function sets the MCG to BLPE mode. If setting to BLPE mode fails from the current mode, this function returns an error.

Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

### 42.7.69 **status\_t** CLOCK\_SetPbeMode ( mcg\_pll\_clk\_select\_t *pllcs*, mcg\_pll\_config\_t const \* *config* )

This function sets the MCG to PBE mode. If setting to PBE mode fails from the current mode, this function returns an error.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>pllcs</i>  | The PLL selection, PLLCS.         |
| <i>config</i> | Pointer to the PLL configuration. |

## Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

## Note

1. The parameter `pllcs` selects the PLL. For platforms with only one PLL, the parameter `pllcs` is kept for interface compatibility.
2. The parameter `config` is the PLL configuration structure. On some platforms, it is possible to choose the external PLL directly, which renders the configuration structure not necessary. In this case, pass in NULL. For example: `CLOCK_SetPbeMode(kMCG_OscselOsc, kMCG_PllClkSelExtPll, NULL);`

**42.7.70 status\_t CLOCK\_SetPeeMode ( void )**

This function sets the MCG to PEE mode.

## Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

## Note

This function only changes the CLKS to use the PLL/FLL output. If the PRDIV/VDIV are different than in the PBE mode, set them up in PBE mode and wait. When the clock is stable, switch to PEE mode.

**42.7.71 status\_t CLOCK\_ExternalModeToFbeModeQuick ( void )**

This function switches the MCG from external modes (PEE/PBE/BLPE/FEE) to the FBE mode quickly. The external clock is used as the system clock source and PLL is disabled. However, the FLL settings are not configured. This is a lite function with a small code size, which is useful during the mode switch. For example, to switch from PEE mode to FEI mode:

```
* CLOCK_ExternalModeToFbeModeQuick();
* CLOCK_SetFeiMode(...);
*
```

## Function Documentation

### Return values

|                                 |                                                                         |
|---------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_Success</i>          | Switched successfully.                                                  |
| <i>kStatus_MCG_Mode-Invalid</i> | If the current mode is not an external mode, do not call this function. |

### 42.7.72 **status\_t** CLOCK\_InternalModeToFbiModeQuick ( void )

This function switches the MCG from internal modes (PEI/PBI/BLPI/FEI) to the FBI mode quickly. The MCGIRCLK is used as the system clock source and PLL is disabled. However, FLL settings are not configured. This is a lite function with a small code size, which is useful during the mode switch. For example, to switch from PEI mode to FEE mode:

```
* CLOCK_InternalModeToFbiModeQuick();  
* CLOCK_SetFeeMode(...);  
*
```

### Return values

|                                 |                                                                         |
|---------------------------------|-------------------------------------------------------------------------|
| <i>kStatus_Success</i>          | Switched successfully.                                                  |
| <i>kStatus_MCG_Mode-Invalid</i> | If the current mode is not an internal mode, do not call this function. |

### 42.7.73 **status\_t** CLOCK\_BootToFeiMode ( mcg\_dmx32\_t *dmx32*, mcg\_drs\_t *drs*, void(\*)*(void) flStableDelay* )

This function sets the MCG to FEI mode from the reset mode. It can also be used to set up MCG during system boot up.

### Parameters

|                      |                                                  |
|----------------------|--------------------------------------------------|
| <i>dmx32</i>         | DMX32 in FEI mode.                               |
| <i>drs</i>           | The DCO range selection.                         |
| <i>flStableDelay</i> | Delay function to ensure that the FLL is stable. |

### Return values



|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

## Note

If `dmx32` is set to `kMCG_Dmx32Fine`, the slow IRC must not be trimmed to frequency above 32768 Hz.

#### 42.7.74 **status\_t CLOCK\_BootToFeeMode ( mcg\_oscsel\_t *oscsel*, uint8\_t *frdiv*, mcg\_dmx32\_t *dmx32*, mcg\_drs\_t *drs*, void(\*)(void) *fllStableDelay* )**

This function sets MCG to FEE mode from the reset mode. It can also be used to set up the MCG during system boot up.

## Parameters

|                       |                                                  |
|-----------------------|--------------------------------------------------|
| <i>oscsel</i>         | OSC clock select, OSCSEL.                        |
| <i>frdiv</i>          | FLL reference clock divider setting, FRDIV.      |
| <i>dmx32</i>          | DMX32 in FEE mode.                               |
| <i>drs</i>            | The DCO range selection.                         |
| <i>fllStableDelay</i> | Delay function to ensure that the FLL is stable. |

## Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

#### 42.7.75 **status\_t CLOCK\_BootToBlpiMode ( uint8\_t *fcrdiv*, mcg\_irc\_mode\_t *ircs*, uint8\_t *ircEnableMode* )**

This function sets the MCG to BLPI mode from the reset mode. It can also be used to set up the MCG during sytem boot up.

## Function Documentation

### Parameters

|                      |                                                                                    |
|----------------------|------------------------------------------------------------------------------------|
| <i>fcrdiv</i>        | Fast IRC divider, FCRDIV.                                                          |
| <i>ircs</i>          | The internal reference clock to select, IRCS.                                      |
| <i>ircEnableMode</i> | The MCGIRCLK enable mode, OR'ed value of <a href="#">_mcg_ircclk_enable_mode</a> . |

### Return values

|                                |                                           |
|--------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Source-Used</i> | Could not change MCGIRCLK setting.        |
| <i>kStatus_Success</i>         | Switched to the target mode successfully. |

### 42.7.76 **status\_t** CLOCK\_BootToBlpeMode ( **mcg\_oscsel\_t** *oscsel* )

This function sets the MCG to BLPE mode from the reset mode. It can also be used to set up the MCG during sytem boot up.

### Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>oscsel</i> | OSC clock select, MCG_C7[OSCSEL]. |
|---------------|-----------------------------------|

### Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

### 42.7.77 **status\_t** CLOCK\_BootToPeeMode ( **mcg\_oscsel\_t** *oscsel*, **mcg\_pll\_clk\_select\_t** *pllcs*, **mcg\_pll\_config\_t** *const* \* *config* )

This function sets the MCG to PEE mode from reset mode. It can also be used to set up the MCG during system boot up.

### Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>oscsel</i> | OSC clock select, MCG_C7[OSCSEL]. |
|---------------|-----------------------------------|

|               |                                   |
|---------------|-----------------------------------|
| <i>pllcs</i>  | The PLL selection, PLLCS.         |
| <i>config</i> | Pointer to the PLL configuration. |

Return values

|                                     |                                           |
|-------------------------------------|-------------------------------------------|
| <i>kStatus_MCG_Mode-Unreachable</i> | Could not switch to the target mode.      |
| <i>kStatus_Success</i>              | Switched to the target mode successfully. |

#### 42.7.78 **status\_t** CLOCK\_SetMcgConfig ( **mcg\_config\_t** const \* *config* )

This function sets MCG to a target mode defined by the configuration structure. If switching to the target mode fails, this function chooses the correct path.

Parameters

|               |                                                         |
|---------------|---------------------------------------------------------|
| <i>config</i> | Pointer to the target MCG mode configuration structure. |
|---------------|---------------------------------------------------------|

Returns

Return `kStatus_Success` if switched successfully; Otherwise, it returns an error code [\\_mcg\\_status](#).

Note

If the external clock is used in the target mode, ensure that it is enabled. For example, if the OSC0 is used, set up OSC0 correctly before calling this function.

## 42.8 Variable Documentation

### 42.8.1 **uint32\_t** g\_xtal0Freq

The XTAL0/EXTAL0 (OSC0) clock frequency in Hz. When the clock is set up, use the function `CLOCK_SetXtal0Freq` to set the value in the clock driver. For example, if XTAL0 is 8 MHz:

```
* CLOCK_InitOsc0(...); // Set up the OSC0
* CLOCK_SetXtal0Freq(8000000); // Set the XTAL0 value to the clock driver.
*
```

This is important for the multicore platforms where only one core needs to set up the OSC0 using the `CLOCK_InitOsc0`. All other cores need to call the `CLOCK_SetXtal0Freq` to get a valid clock frequency.

### 42.8.2 uint32\_t g\_xtal32Freq

The XTAL32/EXTAL32/RTC\_CLKIN clock frequency in Hz. When the clock is set up, use the function `CLOCK_SetXtal32Freq` to set the value in the clock driver.

This is important for the multicore platforms where only one core needs to set up the clock. All other cores need to call the `CLOCK_SetXtal32Freq` to get a valid clock frequency.

## 42.9 Multipurpose Clock Generator (MCG)

The KSDK provides a peripheral driver for the MCG module of Kinetis devices.

### 42.9.1 Function description

MCG driver provides these functions:

- Functions to get the MCG clock frequency.
- Functions to configure the MCG clock, such as PLLCLK and MCGIRCLK.
- Functions for the MCG clock lock lost monitor.
- Functions for the OSC configuration.
- Functions for the MCG auto-trim machine.
- Functions for the MCG mode.

#### 42.9.1.1 MCG frequency functions

MCG module provides clocks, such as MCGOUTCLK, MCGIRCLK, MCGFFCLK, MCGFLLCLK and MCGPLLCLK. The MCG driver provides functions to get the frequency of these clocks, such as [CLOCK\\_GetOutClkFreq\(\)](#), [CLOCK\\_GetInternalRefClkFreq\(\)](#), [CLOCK\\_GetFixedFreqClkFreq\(\)](#), [CLOCK\\_GetFllFreq\(\)](#), [CLOCK\\_GetPlloFreq\(\)](#), [CLOCK\\_GetPll1Freq\(\)](#), and [CLOCK\\_GetExtPl1Freq\(\)](#). These functions get the clock frequency based on the current MCG registers.

#### 42.9.1.2 MCG clock configuration

The MCG driver provides functions to configure the internal reference clock (MCGIRCLK), the external reference clock, and MCGPLLCLK.

The function [CLOCK\\_SetInternalRefClkConfig\(\)](#) configures the MCGIRCLK, including the source and the divider. Do not change MCGIRCLK when the MCG mode is BLPI/FBI/PBI because the MCGIRCLK is used as a system clock in these modes and changing settings makes the system clock unstable.

The function [CLOCK\\_SetExternalRefClkConfig\(\)](#) configures the external reference clock source (MCG\_C7[OSCSEL]). Do not call this function when the MCG mode is BLPE/FBE/PBE/FEE/PEE because the external reference clock is used as a clock source in these modes. Changing the external reference clock source requires at least a 50 micro seconds wait. The function [CLOCK\\_SetExternalRefClkConfig\(\)](#) implements a for loop delay internally. The for loop delay assumes that the system clock is 96 MHz, which ensures at least 50 micro seconds delay. However, when the system clock is slow, the delay time may significantly increase. This for loop count can be optimized for better performance for specific cases.

The MCGPLLCLK is disabled in FBE/FEE/FBI/FEI modes by default. Applications can enable the MCGPLLCLK in these modes using the functions [CLOCK\\_EnablePllo\(\)](#) and [CLOCK\\_EnablePll1\(\)](#). To enable the MCGPLLCLK, the PLL reference clock divider (PRDIV) and the PLL VCO divider (VDIV) must be set to a proper value. The function [CLOCK\\_CalcPlldiv\(\)](#) helps to get the PRDIV/VDIV.

## Multipurpose Clock Generator (MCG)

### 42.9.1.3 MCG clock lock monitor functions

The MCG module monitors the OSC and the PLL clock lock status. The MCG driver provides the functions to set the clock monitor mode, check the clock lost status, and clear the clock lost status.

### 42.9.1.4 OSC configuration

The MCG is needed together with the OSC module to enable the OSC clock. The function [CLOCK\\_InitOsc0\(\)](#) [CLOCK\\_InitOsc1](#) uses the MCG and OSC to initialize the OSC. The OSC should be configured based on the board design.

### 42.9.1.5 MCG auto-trim machine

The MCG provides an auto-trim machine to trim the MCG internal reference clock based on the external reference clock (BUS clock). During clock trimming, the MCG must not work in FEI/FBI/BLPI/PBI/PEI modes. The function [CLOCK\\_TrimInternalRefClk\(\)](#) is used for the auto clock trimming.

### 42.9.1.6 MCG mode functions

The function [CLOCK\\_GetMcgMode](#) returns the current MCG mode. The MCG can only switch between the neighbouring modes. If the target mode is not current mode's neighbouring mode, the application must choose the proper switch path. For example, to switch to PEE mode from FEI mode, use FEI -> FBE -> PBE -> PEE.

For the MCG modes, the MCG driver provides three kinds of functions:

The first type of functions involve functions [CLOCK\\_SetXxxMode](#), such as [CLOCK\\_SetFeiMode\(\)](#). These functions only set the MCG mode from neighbouring modes. If switching to the target mode directly from current mode is not possible, the functions return an error.

The second type of functions are the functions [CLOCK\\_BootToXxxMode](#), such as [CLOCK\\_BootToFeiMode\(\)](#). These functions set the MCG to specific modes from reset mode. Because the source mode and target mode are specific, these functions choose the best switch path. The functions are also useful to set up the system clock during boot up.

The third type of functions is the [CLOCK\\_SetMcgConfig\(\)](#). This function chooses the right path to switch to the target mode. It is easy to use, but introduces a large code size.

Whenever the FLL settings change, there should be a 1 millisecond delay to ensure that the FLL is stable. The function [CLOCK\\_SetMcgConfig\(\)](#) implements a for loop delay internally to ensure that the FLL is stable. The for loop delay assumes that the system clock is 96 MHz, which ensures at least 1 millisecond delay. However, when the system clock is slow, the delay time may increase significantly. The for loop count can be optimized for better performance according to a specific use case.

## 42.9.2 Typical use case

The function `CLOCK_SetMcgConfig` is used to switch between any modes. However, this heavy-light function introduces a large code size. This section shows how to use the mode function to implement a quick and light-weight switch between typical specific modes. Note that the step to enable the external clock is not included in the following steps. Enable the corresponding clock before using it as a clock source.

### 42.9.2.1 Switch between BLPI and FEI

| Use case    | Steps                      | Functions                                                               |
|-------------|----------------------------|-------------------------------------------------------------------------|
| BLPI -> FEI | BLPI -> FBI                | <code>CLOCK_InternalModeToFbiModeQuick(...)</code>                      |
|             | FBI -> FEI                 | <code>CLOCK_SetFeiMode(...)</code>                                      |
|             | Configure MCGIRCLK if need | <code>CLOCK_SetInternalRefClkConfig(...)</code>                         |
| FEI -> BLPI | Configure MCGIRCLK if need | <code>CLOCK_SetInternalRefClkConfig(...)</code>                         |
|             | FEI -> FBI                 | <code>CLOCK_SetFbiMode(...)</code> with <code>flStableDelay=NULL</code> |
|             | FBI -> BLPI                | <code>CLOCK_SetLowPowerEnable(true)</code>                              |

### 42.9.2.2 Switch between BLPI and FEE

| Use case    | Steps                                | Functions                                                               |
|-------------|--------------------------------------|-------------------------------------------------------------------------|
| BLPI -> FEE | BLPI -> FBI                          | <code>CLOCK_InternalModeToFbiModeQuick(...)</code>                      |
|             | Change external clock source if need | <code>CLOCK_SetExternalRefClkConfig(...)</code>                         |
|             | FBI -> FEE                           | <code>CLOCK_SetFeeMode(...)</code>                                      |
| FEE -> BLPI | Configure MCGIRCLK if need           | <code>CLOCK_SetInternalRefClkConfig(...)</code>                         |
|             | FEE -> FBI                           | <code>CLOCK_SetFbiMode(...)</code> with <code>flStableDelay=NULL</code> |
|             | FBI -> BLPI                          | <code>CLOCK_SetLowPowerEnable(true)</code>                              |

## Multipurpose Clock Generator (MCG)

### 42.9.2.3 Switch between BLPI and PEE

| Use case    | Steps                                | Functions                                     |
|-------------|--------------------------------------|-----------------------------------------------|
| BLPI -> PEE | BLPI -> FBI                          | CLOCK_InternalModeToFbi-ModeQuick(...)        |
|             | Change external clock source if need | CLOCK_SetExternalRefClk-Config(...)           |
|             | FBI -> FBE                           | CLOCK_SetFbeMode(...) // fl-StableDelay=NULL  |
|             | FBE -> PBE                           | CLOCK_SetPbeMode(...)                         |
|             | PBE -> PEE                           | CLOCK_SetPeeMode(...)                         |
| PEE -> BLPI | PEE -> FBE                           | CLOCK_ExternalModeToFbe-ModeQuick(...)        |
|             | Configure MCGIRCLK if need           | CLOCK_SetInternalRefClk-Config(...)           |
|             | FBE -> FBI                           | CLOCK_SetFbiMode(...) with flStableDelay=NULL |
|             | FBI -> BLPI                          | CLOCK_SetLowPower-Enable(true)                |

### 42.9.2.4 Switch between BLPE and PEE

This table applies when using the same external clock source (MCG\_C7[OSCSEL]) in BLPE mode and PEE mode.

| Use case    | Steps       | Functions                              |
|-------------|-------------|----------------------------------------|
| BLPE -> PEE | BLPE -> PBE | CLOCK_SetPbeMode(...)                  |
|             | PBE -> PEE  | CLOCK_SetPeeMode(...)                  |
| PEE -> BLPE | PEE -> FBE  | CLOCK_ExternalModeToFbe-ModeQuick(...) |
|             | FBE -> BLPE | CLOCK_SetLowPower-Enable(true)         |

If using different external clock sources (MCG\_C7[OSCSEL]) in BLPE mode and PEE mode, call the [CLOCK\\_SetExternalRefClkConfig\(\)](#) in FBI or FEI mode to change the external reference clock.

| Use case | Steps       | Functions                              |
|----------|-------------|----------------------------------------|
|          | BLPE -> FBE | CLOCK_ExternalModeToFbe-ModeQuick(...) |



## Multipurpose Clock Generator (MCG)

|             |               |                                               |
|-------------|---------------|-----------------------------------------------|
|             | FBE -> FBI    | CLOCK_SetFbiMode(...) with flStableDelay=NULL |
|             | Change source | CLOCK_SetExternalRefClkConfig(...)            |
|             | FBI -> FBE    | CLOCK_SetFbeMode(...) with flStableDelay=NULL |
|             | FBE -> PBE    | CLOCK_SetPbeMode(...)                         |
|             | PBE -> PEE    | CLOCK_SetPeeMode(...)                         |
| PEE -> BLPE | PEE -> FBE    | CLOCK_ExternalModeToFbeModeQuick(...)         |
|             | FBE -> FBI    | CLOCK_SetFbiMode(...) with flStableDelay=NULL |
|             | Change source | CLOCK_SetExternalRefClkConfig(...)            |
|             | PBI -> FBE    | CLOCK_SetFbeMode(...) with flStableDelay=NULL |
|             | FBE -> BLPE   | CLOCK_SetLowPowerEnable(true)                 |

### 42.9.2.5 Switch between BLPE and FEE

This table applies when using the same external clock source (MCG\_C7[OSCSEL]) in BLPE mode and FEE mode.

| Use case    | Steps       | Functions                             |
|-------------|-------------|---------------------------------------|
| BLPE -> FEE | BLPE -> FBE | CLOCK_ExternalModeToFbeModeQuick(...) |
|             | FBE -> FEE  | CLOCK_SetFeeMode(...)                 |
| FEE -> BLPE | PEE -> FBE  | CLOCK_SetPbeMode(...)                 |
|             | FBE -> BLPE | CLOCK_SetLowPowerEnable(true)         |

If using different external clock sources (MCG\_C7[OSCSEL]) in BLPE mode and FEE mode, call the [CLOCK\\_SetExternalRefClkConfig\(\)](#) in FBI or FEI mode to change the external reference clock.

| Use case    | Steps       | Functions                             |
|-------------|-------------|---------------------------------------|
| BLPE -> FEE | BLPE -> FBE | CLOCK_ExternalModeToFbeModeQuick(...) |

## Multipurpose Clock Generator (MCG)

|             |               |                                               |
|-------------|---------------|-----------------------------------------------|
|             | FBE -> FBI    | CLOCK_SetFbiMode(...) with flStableDelay=NULL |
|             | Change source | CLOCK_SetExternalRefClk-Config(...)           |
|             | FBI -> FEE    | CLOCK_SetFeeMode(...)                         |
| FEE -> BLPE | FEE -> FBI    | CLOCK_SetFbiMode(...) with flStableDelay=NULL |
|             | Change source | CLOCK_SetExternalRefClk-Config(...)           |
|             | PBI -> FBE    | CLOCK_SetFbeMode(...) with flStableDelay=NULL |
|             | FBE -> BLPE   | CLOCK_SetLowPower-Enable(true)                |

### 42.9.2.6 Switch between BLPI and PEI

| Use case    | Steps                      | Functions                              |
|-------------|----------------------------|----------------------------------------|
| BLPI -> PEI | BLPI -> PBI                | CLOCK_SetPbiMode(...)                  |
|             | PBI -> PEI                 | CLOCK_SetPeiMode(...)                  |
|             | Configure MCGIRCLK if need | CLOCK_SetInternalRefClk-Config(...)    |
| PEI -> BLPI | Configure MCGIRCLK if need | CLOCK_SetInternalRefClk-Config         |
|             | PEI -> FBI                 | CLOCK_InternalModeToFbi-ModeQuick(...) |
|             | FBI -> BLPI                | CLOCK_SetLowPower-Enable(true)         |

## Chapter 43 Debug Console

### 43.1 Overview

This part describes the programming interface of the debug console driver. The debug console enables debug log messages to be output via the specified peripheral with frequency of the peripheral source clock and base address at the specified baud rate. Additionally, it provides input and output functions to scan and print formatted data.

### 43.2 Function groups

#### 43.2.1 Initialization

To initialize the debug console, call the `DbgConsole_Init()` function with these parameters. This function automatically enables the module and the clock.

```
/*
 * @brief Initializes the the peripheral used to debug messages.
 *
 * @param baseAddr      Indicates which address of the peripheral is used to send debug messages.
 * @param baudRate      The desired baud rate in bits per second.
 * @param device         Low level device type for the debug console, can be one of:
 *                      @arg DEBUG_CONSOLE_DEVICE_TYPE_UART,
 *                      @arg DEBUG_CONSOLE_DEVICE_TYPE_LPUART,
 *                      @arg DEBUG_CONSOLE_DEVICE_TYPE_LPSCI,
 *                      @arg DEBUG_CONSOLE_DEVICE_TYPE_USBCDC.
 * @param clkSrcFreq    Frequency of peripheral source clock.
 *
 * @return              Whether initialization was successful or not.
 */
status_t DbgConsole_Init(uint32_t baseAddr, uint32_t baudRate, uint8_t device, uint32_t clkSrcFreq)
```

Selects the supported debug console hardware device type, such as

```
DEBUG_CONSOLE_DEVICE_TYPE_NONE
DEBUG_CONSOLE_DEVICE_TYPE_LPSCI
DEBUG_CONSOLE_DEVICE_TYPE_UART
DEBUG_CONSOLE_DEVICE_TYPE_LPUART
DEBUG_CONSOLE_DEVICE_TYPE_USBCDC
```

After the initialization is successful, stdout and stdin are connected to the selected peripheral. The debug console state is stored in the `debug_console_state_t` structure, such as shown here.

```
typedef struct DebugConsoleState
{
    uint8_t          type;
    void*            base;
    debug_console_ops_t ops;
} debug_console_state_t;
```

## Function groups

This example shows how to call the DbgConsole\_Init() given the user configuration structure.

```
uint32_t uartClkSrcFreq = CLOCK_GetFreq (BOARD_DEBUG_UART_CLKSRC);  
  
DbgConsole_Init (BOARD_DEBUG_UART_BASEADDR, BOARD_DEBUG_UART_BAUDRATE, DEBUG_CONSOLE_DEVICE_TYPE_UART,  
                uartClkSrcFreq);
```

### 43.2.2 Advanced Feature

The debug console provides input and output functions to scan and print formatted data.

- Support a format specifier for PRINTF following this prototype "%[flags][width][.precision][length]specifier", which is explained below

| flags   | Description                                                                                                                                                                                                                                                                                                                                                                             |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| -       | Left-justified within the given field width. Right-justified is the default.                                                                                                                                                                                                                                                                                                            |
| +       | Forces to precede the result with a plus or minus sign (+ or -) even for positive numbers. By default, only negative numbers are preceded with a - sign.                                                                                                                                                                                                                                |
| (space) | If no sign is written, a blank space is inserted before the value.                                                                                                                                                                                                                                                                                                                      |
| #       | Used with o, x, or X specifiers the value is preceded with 0, 0x, or 0X respectively for values other than zero. Used with e, E and f, it forces the written output to contain a decimal point even if no digits would follow. By default, if no digits follow, no decimal point is written. Used with g or G the result is the same as with e or E but trailing zeros are not removed. |
| 0       | Left-pads the number with zeroes (0) instead of spaces, where padding is specified (see width sub-specifier).                                                                                                                                                                                                                                                                           |

| Width    | Description                                                                                                                                                                                            |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| (number) | A minimum number of characters to be printed. If the value to be printed is shorter than this number, the result is padded with blank spaces. The value is not truncated even if the result is larger. |
| *        | The width is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.                                                          |

| <b>.precision</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| .number           | For integer specifiers (d, i, o, u, x, X) precision specifies the minimum number of digits to be written. If the value to be written is shorter than this number, the result is padded with leading zeros. The value is not truncated even if the result is longer. A precision of 0 means that no character is written for the value 0. For e, E, and f specifiers this is the number of digits to be printed after the decimal point. For g and G specifiers This is the maximum number of significant digits to be printed. For s this is the maximum number of characters to be printed. By default, all characters are printed until the ending null character is encountered. For c type it has no effect. When no precision is specified, the default is 1. If the period is specified without an explicit value for precision, 0 is assumed. |
| .*                | The precision is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

| <b>length</b>  | <b>Description</b> |
|----------------|--------------------|
| Do not support |                    |

| <b>specifier</b> | <b>Description</b>                           |
|------------------|----------------------------------------------|
| d or i           | Signed decimal integer                       |
| f                | Decimal floating point                       |
| F                | Decimal floating point capital letters       |
| x                | Unsigned hexadecimal integer                 |
| X                | Unsigned hexadecimal integer capital letters |
| o                | Signed octal                                 |
| b                | Binary value                                 |
| p                | Pointer address                              |
| u                | Unsigned decimal integer                     |
| c                | Character                                    |
| s                | String of characters                         |
| n                | Nothing printed                              |

## Function groups

- Support a format specifier for SCANF following this prototype " %[\*][width][length]specifier", which is explained below

| * | Description |
|---|-------------|
|---|-------------|

An optional starting asterisk indicates that the data is to be read from the stream but ignored. In other words, it is not stored in the corresponding argument.

| width                                                                                        | Description |
|----------------------------------------------------------------------------------------------|-------------|
| This specifies the maximum number of characters to be read in the current reading operation. |             |

| length      | Description                                                                                                                                                                                             |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| hh          | The argument is interpreted as a signed character or unsigned character (only applies to integer specifiers: i, d, o, u, x, and X).                                                                     |
| h           | The argument is interpreted as a short integer or unsigned short integer (only applies to integer specifiers: i, d, o, u, x, and X).                                                                    |
| l           | The argument is interpreted as a long integer or unsigned long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.           |
| ll          | The argument is interpreted as a long long integer or unsigned long long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s. |
| L           | The argument is interpreted as a long double (only applies to floating point specifiers: e, E, f, g, and G).                                                                                            |
| j or z or t | Not supported                                                                                                                                                                                           |

| specifier | Qualifying Input                                                                                                                                                                                                                                 | Type of argument |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| c         | Single character: Reads the next character. If a width different from 1 is specified, the function reads width characters and stores them in the successive locations of the array passed as argument. No null character is appended at the end. | char *           |

| specifier              | Qualifying Input                                                                                                                                                                                                            | Type of argument |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| i                      | Integer: : Number optionally preceded with a + or - sign                                                                                                                                                                    | int *            |
| d                      | Decimal integer: Number optionally preceded with a + or - sign                                                                                                                                                              | int *            |
| a, A, e, E, f, F, g, G | Floating point: Decimal number containing a decimal point, optionally preceded by a + or - sign and optionally followed by the e or E character and a decimal number. Two examples of valid entries are -732.103 and 7.12e4 | float *          |
| o                      | Octal Integer:                                                                                                                                                                                                              | int *            |
| s                      | String of characters. This reads subsequent characters until a white space is found (white space characters are considered to be blank, newline, and tab).                                                                  | char *           |
| u                      | Unsigned decimal integer.                                                                                                                                                                                                   | unsigned int *   |

The debug console has its own printf/scanf/putchar/getchar functions which are defined in the header file.

```
int DbgConsole_Printf(const char *fmt_s, ...);
int DbgConsole_Putchar(int ch);
int DbgConsole_Scanf(const char *fmt_ptr, ...);
int DbgConsole_Getchar(void);
```

This utility supports selecting toolchain's printf/scanf or the KSDK printf/scanf.

```
#if SDK_DEBUGCONSOLE    /* Select printf, scanf, putchar, getchar of SDK version. */
#define PRINTF           DbgConsole_Printf
#define SCANF            DbgConsole_Scanf
#define PUTCHAR          DbgConsole_Putchar
#define GETCHAR          DbgConsole_Getchar
#else                   /* Select printf, scanf, putchar, getchar of toolchain. */
#define PRINTF           printf
#define SCANF            scanf
#define PUTCHAR          putchar
#define GETCHAR          getchar
#endif /* SDK_DEBUGCONSOLE */
```

## 43.3 Typical use case

### Some examples use the PUTCHAR & GETCHAR function

```
ch = GETCHAR();
PUTCHAR(ch);
```

## Typical use case

### Some examples use the PRINTF function

Statement prints the string format.

```
PRINTF("%s %s\r\n", "Hello", "world!");
```

Statement prints the hexadecimal format/

```
PRINTF("0x%02X hexadecimal number equivalent 255", 255);
```

Statement prints the decimal floating point and unsigned decimal.

```
PRINTF("Execution timer: %s\n\rTime: %u ticks %2.5f milliseconds\n\rDONE\n\r", "1 day", 86400, 86.4);
```

### Some examples use the SCANF function

```
PRINTF("Enter a decimal number: ");
SCANF("%d", &i);
PRINTF("\r\nYou have entered %d.\r\n", i, i);
PRINTF("Enter a hexadecimal number: ");
SCANF("%x", &i);
PRINTF("\r\nYou have entered 0x%X (%d).\r\n", i, i);
```

### Print out failure messages using KSDK \_\_assert\_func:

```
void __assert_func(const char *file, int line, const char *func, const char *failedExpr)
{
    PRINTF("ASSERT ERROR \" %s \": file \"%s\" Line \"%d\" function name \"%s\" \n", failedExpr, file ,
        line, func);
    for (;;)
    {}
}
```

### Note:

To use 'printf' and 'scanf' for GNUC Base, add file 'fsl\_sbrk.c' in path: ..\{package}\devices\{subset}\utilities\fsl-  
\_sbrk.c to your project.

## Modules

- [Semihosting](#)



## 43.4 Semihosting

Semihosting is a mechanism for ARM targets to communicate input/output requests from application code to a host computer running a debugger. This mechanism can be used, for example, to enable functions in the C library, such as `printf()` and `scanf()`, to use the screen and keyboard of the host rather than having a screen and keyboard on the target system.

### 43.4.1 Guide Semihosting for IAR

**NOTE:** After the setting both "printf" and "scanf" are available for debugging.

#### Step 1: Setting up the environment

1. To set debugger options, choose Project>Options. In the Debugger category, click the Setup tab.
2. Select Run to main and click OK. This ensures that the debug session starts by running the main function.
3. The project is now ready to be built.

#### Step 2: Building the project

1. Compile and link the project by choosing Project>Make or F7.
2. Alternatively, click the Make button on the tool bar. The Make command compiles and links those files that have been modified.

#### Step 3: Starting semihosting

1. Choose "Semihosting\_IAR" project -> "Options" -> "Debugger" -> "J-Link/J-Trace".
2. Choose tab "J-Link/J-Trace" -> "Connection" tab -> "SWD".
3. Start the project by choosing Project>Download and Debug.
4. Choose View>Terminal I/O to display the output from the I/O operations.

### 43.4.2 Guide Semihosting for Keil $\mu$ Vision

**NOTE:** Keil supports Semihosting only for Cortex-M3/Cortex-M4 cores.

#### Step 1: Prepare code

Remove function `fputc` and `fgetc` is used to support KEIL in "fsl\_debug\_console.c" and add the following code to project.

```
#pragma import(__use_no_semihosting_swi)

volatile int ITM_RxBuffer = ITM_RXBUFFER_EMPTY;    /* used for Debug Input */
```

## Semihosting

```
struct __FILE
{
    int handle;
};
FILE __stdout;
FILE __stdin;

int fputc(int ch, FILE *f)
{
    return (ITM_SendChar(ch));
}

int fgetc(FILE *f)
{
    /* blocking */
    while (ITM_CheckChar() != 1)
        ;
    return (ITM_ReceiveChar());
}

int ferror(FILE *f)
{
    /* Your implementation of ferror */
    return EOF;
}

void _ttywrch(int ch)
{
    ITM_SendChar(ch);
}

void _sys_exit(int return_code)
{
label:
    goto label; /* endless loop */
}
```

### Step 2: Setting up the environment

1. In menu bar, choose Project>Options for target or using Alt+F7 or click.
2. Select "Target" tab and not select "Use MicroLIB".
3. Select "Debug" tab, select "J-Link/J-Trace Cortex" and click "Setting button".
4. Select "Debug" tab and choose Port:SW, then select "Trace" tab, choose "Enable" and click OK.

### Step 3: Building the project

1. Compile and link the project by choosing Project>Build Target or using F7.

### Step 4: Building the project

1. Choose "Debug" on menu bar or Ctrl F5.
2. In menu bar, choose "Serial Window" and click to "Debug (printf) Viewer".
3. Run line by line to see result in Console Window.

### 43.4.3 Guide Semihosting for KDS

**NOTE:** After the setting use "printf" for debugging.

#### Step 1: Setting up the environment

1. In menu bar, choose Project>Properties>C/C++ Build>Settings>Tool Settings.
2. Select "Libraries" on "Cross ARM C Linker" and delete "nosys".
3. Select "Miscellaneous" on "Cross ARM C Linker", add "-specs=rdimon.specs" to "Other link flages" and tick "Use newlib-nano", and click OK.

#### Step 2: Building the project

1. In menu bar, choose Project>Build Project.

#### Step 3: Starting semihosting

1. In Debug configurations, choose "Startup" tab, tick "Enable semihosting and Telnet". Press "Apply" and "Debug".
2. After clicking Debug, the Window is displayed same as below. Run line by line to see the result in the Console Window.

### 43.4.4 Guide Semihosting for ATL

**NOTE:** J-Link has to be used to enable semihosting.

#### Step 1: Prepare code

Add the following code to the project.

```
int _write(int file, char *ptr, int len)
{
    /* Implement your write code here. This is used by puts and printf. */
    int i=0;
    for(i=0 ; i<len ; i++)
        ITM_SendChar((*ptr++));
    return len;
}
```

#### Step 2: Setting up the environment

1. In menu bar, choose Debug Configurations. In tab "Embedded C/C++ Application" choose "- Semihosting\_ATL\_xxx debug J-Link".
2. In tab "Debugger" set up as follows.
  - JTAG mode must be selected

## Semihosting

- SWV tracing must be enabled
  - Enter the Core Clock frequency, which is hardware board-specific.
  - Enter the desired SWO Clock frequency. The latter depends on the JTAG Probe and must be a multiple of the Core Clock value.
3. Click "Apply" and "Debug".

### Step 3: Starting semihosting

1. In the Views menu, expand the submenu SWV and open the docking view "SWV Console". 2. Open the SWV settings panel by clicking the "Configure Serial Wire Viewer" button in the SWV Console view toolbar. 3. Configure the data ports to be traced by enabling the ITM channel 0 check-box in the ITM stimulus ports group: Choose "EXETRC: Trace Exceptions" and In tab "ITM Stimulus Ports" choose "Enable Port" 0. Then click "OK".
2. It is recommended not to enable other SWV trace functionalities at the same time because this may over use the SWO pin causing packet loss due to a limited bandwidth (certain other SWV tracing capabilities can send a lot of data at very high-speed). Save the SWV configuration by clicking the OK button. The configuration is saved with other debug configurations and remains effective until changed.
3. Press the red Start/Stop Trace button to send the SWV configuration to the target board to enable SWV trace recoding. The board does not send any SWV packages until it is properly configured. The SWV Configuration must be present, if the configuration registers on the target board are reset. Also, tracing does not start until the target starts to execute.
4. Start the target execution again by pressing the green Resume Debug button.
5. The SWV console now shows the printf() output.

## 43.4.5 Guide Semihosting for ARMGCC

### Step 1: Setting up the environment

1. Turn on "J-LINK GDB Server" -> Select suitable "Target device" -> "OK".
2. Turn on "PuTTY". Set up as follows.
  - "Host Name (or IP address)" : localhost
  - "Port" :2333
  - "Connection type" : Telet.
  - Click "Open".
3. Increase "Heap/Stack" for GCC to 0x2000:

#### Add to "CMakeLists.txt"

```
SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE}  
--defsym=__stack_size__=0x2000")
```

```
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --  
defsym=__stack_size__=0x2000")
```

```
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --
```

```

defsym=__heap_size__=0x2000")
SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE}
--defsym=__heap_size__=0x2000")

```

## Step 2: Building the project

1. Change "CMakeLists.txt":

**Change** "SET(CMAKE\_EXE\_LINKER\_FLAGS\_RELEASE "\${CMAKE\_EXE\_LINKER\_FLAGS\_RELEASE} -specs=nano.specs")"

**to** "SET(CMAKE\_EXE\_LINKER\_FLAGS\_RELEASE "\${CMAKE\_EXE\_LINKER\_FLAGS\_RELEASE} -specs=rdimon.specs")"

**Replace paragraph**

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -fno-common")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -ffunction-sections")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -fdata-sections")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -ffreestanding")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -fno-builtin")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -mthumb")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -mapcs")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -Xlinker")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} --gc-sections")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -Xlinker")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -static")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -Xlinker")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -z")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} -Xlinker")

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG} muldefs")

**To**

SET(CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG "\${CMAKE\_EXE\_LINKER\_FLAGS\_DEBUG

## Semihosting

```
G} --specs=rdimon.specs ")
```

### Remove

```
target_link_libraries(semihosting_ARMGCC.elf debug nosys)
```

2. Run "build\_debug.bat" to build project

### Step 3: Starting semihosting

- (a) Download the image and set as follows.

```
cd D:\mcu-sdk-2.0-origin\boards\twrk64f120m\driver_examples\semihosting\armgcc\debug
d:
C:\PROGRA~2\GNUTOO~1\4BD65~1.920\bin\arm-none-eabi-gdb.exe
target remote localhost:2331
monitor reset
monitor semihosting enable
monitor semihosting thumbSWI 0xAB
monitor semihosting IOClient 1
monitor flash device = MK64FN1M0xxx12
load semihosting_ARMGCC.elf
monitor reg pc = (0x00000004)
monitor reg sp = (0x00000000)
continue
```

- (b) After the setting, press "enter". The PuTTY window now shows the printf() output.

## Chapter 44

# Notification Framework

### 44.1 Overview

This section describes the programming interface of the Notifier driver.

### 44.2 Notifier Overview

The Notifier provides a configuration dynamic change service. Based on this service, applications can switch between pre-defined configurations. The Notifier enables drivers and applications to register callback functions to this framework. Each time that the configuration is changed, drivers and applications receive a notification and change their settings. To simplify, the Notifier only supports the static callback registration. This means that, for applications, all callback functions are collected into a static table and passed to the Notifier.

These are the steps for the configuration transition.

1. Before configuration transition, the Notifier sends a "BEFORE" message to the callback table. When this message is received, IP drivers should check whether any current processes can be stopped and stop them. If the processes cannot be stopped, the callback function returns an error.  
The Notifier supports two types of transition policies, a graceful policy and a forceful policy. When the graceful policy is used, if some callbacks return an error while sending a "BEFORE" message, the configuration transition stops and the Notifier sends a "RECOVER" message to all drivers that have stopped. Then, these drivers can recover the previous status and continue to work. When the forceful policy is used, drivers are stopped forcefully.
2. After the "BEFORE" message is processed successfully, the system switches to the new configuration.
3. After the configuration changes, the Notifier sends an "AFTER" message to the callback table to notify drivers that the configuration transition is finished.

This example shows how to use the Notifier in the Power Manager application.

```
#include "fsl_notifier.h"

/* Definition of the Power Manager callback */
status_t callback0(notifier_notification_block_t *notify, void *data)
{
    status_t ret = kStatus_Success;

    ...
    ...
    ...

    return ret;
}

/* Definition of the Power Manager user function */
status_t APP_PowerModeSwitch(notifier_user_config_t *targetConfig, void *userData)
{

```

## Notifier Overview

```
...
...
...
}
...
...
...
...
...
/* Main function */
int main(void)
{
    /* Define a notifier handle */
    notifier_handle_t powerModeHandle;

    /* Callback configuration */
    user_callback_data_t callbackData0;

    notifier_callback_config_t callbackCfg0 = {callback0,
        kNOTIFIER_CallbackBeforeAfter,
        (void *)&callbackData0};

    notifier_callback_config_t callbacks[] = {callbackCfg0};

    /* Power mode configurations */
    power_user_config_t vlprConfig;
    power_user_config_t stopConfig;

    notifier_user_config_t *powerConfigs[] = {&vlprConfig, &stopConfig};

    /* Definition of a transition to and out the power modes */
    vlprConfig.mode = kAPP_PowerModeVlpr;
    vlprConfig.enableLowPowerWakeUpOnInterrupt = false;

    stopConfig = vlprConfig;
    stopConfig.mode = kAPP_PowerModeStop;

    /* Create Notifier handle */
    NOTIFIER_CreateHandle(&powerModeHandle, powerConfigs, 2U, callbacks, 1U,
        APP_PowerModeSwitch, NULL);
    ...
    ...
    /* Power mode switch */
    NOTIFIER_switchConfig(&powerModeHandle, targetConfigIndex,
        kNOTIFIER_PolicyAgreement);
}
```

## Data Structures

- struct `notifier_notification_block_t`  
*notification block passed to the registered callback function. [More...](#)*
- struct `notifier_callback_config_t`  
*Callback configuration structure. [More...](#)*
- struct `notifier_handle_t`  
*Notifier handle structure. [More...](#)*

## Typedefs

- typedef void `notifier_user_config_t`  
*Notifier user configuration type.*
- typedef status\_t(\* `notifier_user_function_t`)(`notifier_user_config_t` \*targetConfig, void \*userData)  
*Notifier user function prototype Use this function to execute specific operations in configuration switch.*



- typedef status\_t(\* [notifier\\_callback\\_t](#))([notifier\\_notification\\_block\\_t](#) \*notify, void \*data)  
*Callback prototype.*

## Enumerations

- enum [\\_notifier\\_status](#) {  
    [kStatus\\_NOTIFIER\\_ErrorNotificationBefore](#),  
    [kStatus\\_NOTIFIER\\_ErrorNotificationAfter](#) }  
*Notifier error codes.*
- enum [notifier\\_policy\\_t](#) {  
    [kNOTIFIER\\_PolicyAgreement](#),  
    [kNOTIFIER\\_PolicyForcible](#) }  
*Notifier policies.*
- enum [notifier\\_notification\\_type\\_t](#) {  
    [kNOTIFIER\\_NotifyRecover](#) = 0x00U,  
    [kNOTIFIER\\_NotifyBefore](#) = 0x01U,  
    [kNOTIFIER\\_NotifyAfter](#) = 0x02U }  
*Notification type.*
- enum [notifier\\_callback\\_type\\_t](#) {  
    [kNOTIFIER\\_CallbackBefore](#) = 0x01U,  
    [kNOTIFIER\\_CallbackAfter](#) = 0x02U,  
    [kNOTIFIER\\_CallbackBeforeAfter](#) = 0x03U }  
*The callback type, which indicates kinds of notification the callback handles.*

## Functions

- status\_t [NOTIFIER\\_CreateHandle](#) ([notifier\\_handle\\_t](#) \*notifierHandle, [notifier\\_user\\_config\\_t](#) \*\*configs, uint8\_t configsNumber, [notifier\\_callback\\_config\\_t](#) \*callbacks, uint8\_t callbacksNumber, [notifier\\_user\\_function\\_t](#) userFunction, void \*userData)  
*Creates a Notifier handle.*
- status\_t [NOTIFIER\\_SwitchConfig](#) ([notifier\\_handle\\_t](#) \*notifierHandle, uint8\_t configIndex, [notifier-\\_policy\\_t](#) policy)  
*Switches the configuration according to a pre-defined structure.*
- uint8\_t [NOTIFIER\\_GetErrorCallbackIndex](#) ([notifier\\_handle\\_t](#) \*notifierHandle)  
*This function returns the last failed notification callback.*

## 44.3 Data Structure Documentation

### 44.3.1 struct [notifier\\_notification\\_block\\_t](#)

#### Data Fields

- [notifier\\_user\\_config\\_t](#) \* [targetConfig](#)  
*Pointer to target configuration.*
- [notifier\\_policy\\_t](#) [policy](#)  
*Configure transition policy.*
- [notifier\\_notification\\_type\\_t](#) [notifyType](#)  
*Configure notification type.*

## Data Structure Documentation

### 44.3.1.0.0.102 Field Documentation

44.3.1.0.0.102.1 `notifier_user_config_t* notifier_notification_block_t::targetConfig`

44.3.1.0.0.102.2 `notifier_policy_t notifier_notification_block_t::policy`

44.3.1.0.0.102.3 `notifier_notification_type_t notifier_notification_block_t::notifyType`

### 44.3.2 struct `notifier_callback_config_t`

This structure holds the configuration of callbacks. Callbacks of this type are expected to be statically allocated. This structure contains the following application-defined data. `callback` - pointer to the callback function `callbackType` - specifies when the callback is called `callbackData` - pointer to the data passed to the callback.

#### Data Fields

- `notifier_callback_t callback`  
*Pointer to the callback function.*
- `notifier_callback_type_t callbackType`  
*Callback type.*
- `void * callbackData`  
*Pointer to the data passed to the callback.*

### 44.3.2.0.0.103 Field Documentation

44.3.2.0.0.103.1 `notifier_callback_t notifier_callback_config_t::callback`

44.3.2.0.0.103.2 `notifier_callback_type_t notifier_callback_config_t::callbackType`

44.3.2.0.0.103.3 `void* notifier_callback_config_t::callbackData`

### 44.3.3 struct `notifier_handle_t`

Notifier handle structure. Contains data necessary for the Notifier proper function. Stores references to registered configurations, callbacks, information about their numbers, user function, user data, and other internal data. `NOTIFIER_CreateHandle()` must be called to initialize this handle.

#### Data Fields

- `notifier_user_config_t ** configsTable`  
*Pointer to configure table.*
- `uint8_t configsNumber`  
*Number of configurations.*
- `notifier_callback_config_t * callbacksTable`  
*Pointer to callback table.*

- `uint8_t callbacksNumber`  
*Maximum number of callback configurations.*
- `uint8_t errorCallbackIndex`  
*Index of callback returns error.*
- `uint8_t currentConfigIndex`  
*Index of current configuration.*
- `notifier_user_function_t userFunction`  
*User function.*
- `void * userData`  
*User data passed to user function.*

#### 44.3.3.0.0.104 Field Documentation

44.3.3.0.0.104.1 `notifier_user_config_t** notifier_handle_t::configsTable`

44.3.3.0.0.104.2 `uint8_t notifier_handle_t::configsNumber`

44.3.3.0.0.104.3 `notifier_callback_config_t* notifier_handle_t::callbacksTable`

44.3.3.0.0.104.4 `uint8_t notifier_handle_t::callbacksNumber`

44.3.3.0.0.104.5 `uint8_t notifier_handle_t::errorCallbackIndex`

44.3.3.0.0.104.6 `uint8_t notifier_handle_t::currentConfigIndex`

44.3.3.0.0.104.7 `notifier_user_function_t notifier_handle_t::userFunction`

44.3.3.0.0.104.8 `void* notifier_handle_t::userData`

### 44.4 Typedef Documentation

#### 44.4.1 `typedef void notifier_user_config_t`

Reference of the user defined configuration is stored in an array; the notifier switches between these configurations based on this array.

#### 44.4.2 `typedef status_t(* notifier_user_function_t)(notifier_user_config_t *targetConfig, void *userData)`

Before and after this function execution, different notification is sent to registered callbacks. If this function returns any error code, `NOTIFIER_SwitchConfig()` exits.

Parameters

---

## Enumeration Type Documentation

|                     |                                                        |
|---------------------|--------------------------------------------------------|
| <i>targetConfig</i> | target Configuration.                                  |
| <i>userData</i>     | Refers to other specific data passed to user function. |

### Returns

An error code or `kStatus_Success`.

#### 44.4.3 `typedef status_t(* notifier_callback_t)(notifier_notification_block_t *notify, void *data)`

Declaration of a callback. It is common for registered callbacks. Reference to function of this type is part of the `notifier_callback_config_t` callback configuration structure. Depending on callback type, function of this prototype is called (see `NOTIFIER_SwitchConfig()`) before configuration switch, after it or in both use cases to notify about the switch progress (see `notifier_callback_type_t`). When called, the type of the notification is passed as a parameter along with the reference to the target configuration structure (see `notifier_notification_block_t`) and any data passed during the callback registration. When notified before the configuration switch, depending on the configuration switch policy (see `notifier_policy_t`), the callback may deny the execution of the user function by returning an error code different than `kStatus_Success` (see `NOTIFIER_SwitchConfig()`).

### Parameters

|               |                                                                                                                                                            |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>notify</i> | Notification block.                                                                                                                                        |
| <i>data</i>   | Callback data. Refers to the data passed during callback registration. Intended to pass any driver or application data such as internal state information. |

### Returns

An error code or `kStatus_Success`.

## 44.5 Enumeration Type Documentation

### 44.5.1 `enum _notifier_status`

Used as return value of Notifier functions.

### Enumerator

***kStatus\_NOTIFIER\_ErrorNotificationBefore*** An error occurs during send "BEFORE" notification.

***kStatus\_NOTIFIER\_ErrorNotificationAfter*** An error occurs during send "AFTER" notification.

### 44.5.2 enum notifier\_policy\_t

Defines whether the user function execution is forced or not. For `kNOTIFIER_PolicyForcible`, the user function is executed regardless of the callback results, while `kNOTIFIER_PolicyAgreement` policy is used to exit `NOTIFIER_SwitchConfig()` when any of the callbacks returns error code. See also `NOTIFIER_SwitchConfig()` description.

Enumerator

***kNOTIFIER\_PolicyAgreement*** `NOTIFIER_SwitchConfig()` method is exited when any of the callbacks returns error code.

***kNOTIFIER\_PolicyForcible*** The user function is executed regardless of the results.

### 44.5.3 enum notifier\_notification\_type\_t

Used to notify registered callbacks

Enumerator

***kNOTIFIER\_NotifyRecover*** Notify IP to recover to previous work state.

***kNOTIFIER\_NotifyBefore*** Notify IP that configuration setting is going to change.

***kNOTIFIER\_NotifyAfter*** Notify IP that configuration setting has been changed.

### 44.5.4 enum notifier\_callback\_type\_t

Used in the callback configuration structure (`notifier_callback_config_t`) to specify when the registered callback is called during configuration switch initiated by the `NOTIFIER_SwitchConfig()`. Callback can be invoked in following situations.

- Before the configuration switch (Callback return value can affect `NOTIFIER_SwitchConfig()` execution. See the `NOTIFIER_SwitchConfig()` and `notifier_policy_t` documentation).
- After an unsuccessful attempt to switch configuration
- After a successful configuration switch

Enumerator

***kNOTIFIER\_CallbackBefore*** Callback handles BEFORE notification.

***kNOTIFIER\_CallbackAfter*** Callback handles AFTER notification.

***kNOTIFIER\_CallbackBeforeAfter*** Callback handles BEFORE and AFTER notification.

## 44.6 Function Documentation

**44.6.1** `status_t NOTIFIER_CreateHandle ( notifier_handle_t * notifierHandle,  
notifier_user_config_t ** configs, uint8_t configsNumber, notifier_callback-  
_config_t * callbacks, uint8_t callbacksNumber, notifier_user_function_t  
userFunction, void * userData )`

## Parameters

|                         |                                                                                                                                         |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <i>notifierHandle</i>   | A pointer to the notifier handle.                                                                                                       |
| <i>configs</i>          | A pointer to an array with references to all configurations which is handled by the Notifier.                                           |
| <i>configsNumber</i>    | Number of configurations. Size of the configuration array.                                                                              |
| <i>callbacks</i>        | A pointer to an array of callback configurations. If there are no callbacks to register during Notifier initialization, use NULL value. |
| <i>callbacks-Number</i> | Number of registered callbacks. Size of the callbacks array.                                                                            |
| <i>userFunction</i>     | User function.                                                                                                                          |
| <i>userData</i>         | User data passed to user function.                                                                                                      |

## Returns

An error Code or kStatus\_Success.

#### 44.6.2 **status\_t NOTIFIER\_SwitchConfig ( notifier\_handle\_t \* *notifierHandle*, uint8\_t *configIndex*, notifier\_policy\_t *policy* )**

This function sets the system to the target configuration. Before transition, the Notifier sends notifications to all callbacks registered to the callback table. Callbacks are invoked in the following order: All registered callbacks are notified ordered by index in the callbacks array. The same order is used for before and after switch notifications. The notifications before the configuration switch can be used to obtain confirmation about the change from registered callbacks. If any registered callback denies the configuration change, further execution of this function depends on the notifier policy: the configuration change is either forced (kNOTIFIER\_PolicyForcible) or exited (kNOTIFIER\_PolicyAgreement). When configuration change is forced, the result of the before switch notifications are ignored. If an agreement is required, if any callback returns an error code, further notifications before switch notifications are cancelled and all already notified callbacks are re-invoked. The index of the callback which returned error code during pre-switch notifications is stored (any error codes during callbacks re-invocation are ignored) and NOTIFIER\_GetErrorCallback() can be used to get it. Regardless of the policies, if any callback returns an error code, an error code indicating in which phase the error occurred is returned when [NOTIFIER\\_SwitchConfig\(\)](#) exits.

## Parameters

## Function Documentation

|                       |                                                                            |
|-----------------------|----------------------------------------------------------------------------|
| <i>notifierHandle</i> | pointer to notifier handle                                                 |
| <i>configIndex</i>    | Index of the target configuration.                                         |
| <i>policy</i>         | Transaction policy, kNOTIFIER_PolicyAgreement or kNOTIFIER_PolicyForcible. |

### Returns

An error code or kStatus\_Success.

### 44.6.3 uint8\_t NOTIFIER\_GetErrorCallbackIndex ( notifier\_handle\_t \* *notifierHandle* )

This function returns an index of the last callback that failed during the configuration switch while the last [NOTIFIER\\_SwitchConfig\(\)](#) was called. If the last [NOTIFIER\\_SwitchConfig\(\)](#) call ended successfully value equal to callbacks number is returned. The returned value represents an index in the array of static call-backs.

### Parameters

|                       |                                |
|-----------------------|--------------------------------|
| <i>notifierHandle</i> | Pointer to the notifier handle |
|-----------------------|--------------------------------|

### Returns

Callback Index of the last failed callback or value equal to callbacks count.



## Chapter 45 Shell

### 45.1 Overview

This part describes the programming interface of the Shell middleware. Shell controls MCUs by commands via the specified communication peripheral based on the debug console driver.

### 45.2 Function groups

#### 45.2.1 Initialization

To initialize the Shell middleware, call the [SHELL\\_Init\(\)](#) function with these parameters. This function automatically enables the middleware.

```
void SHELL_Init(p_shell_context_t context, send_data_cb_t send_cb,  
               recv_data_cb_t recv_cb, char *prompt);
```

Then, after the initialization was successful, call a command to control MCUs.

This example shows how to call the [SHELL\\_Init\(\)](#) given the user configuration structure.

```
SHELL_Init(&user_context, SHELL_SendDataCallback, SHELL_ReceiveDataCallback, "SHELL>> ");
```

#### 45.2.2 Advanced Feature

- Support to get a character from standard input devices.

```
static uint8_t GetChar(p_shell_context_t context);
```

| Commands   | Description                                      |
|------------|--------------------------------------------------|
| Help       | Lists all commands which are supported by Shell. |
| Exit       | Exits the Shell program.                         |
| strCompare | Compares the two input strings.                  |

| Input character | Description                                         |
|-----------------|-----------------------------------------------------|
| A               | Gets the latest command in the history.             |
| B               | Gets the first command in the history.              |
| C               | Replaces one character at the right of the pointer. |

## Function groups

|   | Input character | Description                                        |
|---|-----------------|----------------------------------------------------|
| D |                 | Replaces one character at the left of the pointer. |
|   |                 | Run AutoComplete function                          |
|   |                 | Run cmdProcess function                            |
|   |                 | Clears a command.                                  |

### 45.2.3 Shell Operation

```
SHELL_Init(&user_context, SHELL_SendDataCallback, SHELL_ReceiveDataCallback, "SHELL>> ");  
SHELL_Main(&user_context);
```

## Data Structures

- struct [p\\_shell\\_context\\_t](#)  
*Data structure for Shell environment. [More...](#)*
- struct [shell\\_command\\_context\\_t](#)  
*User command data structure. [More...](#)*
- struct [shell\\_command\\_context\\_list\\_t](#)  
*Structure list command. [More...](#)*

## Macros

- #define [SHELL\\_USE\\_HISTORY](#) (0U)  
*Macro to set on/off history feature.*
- #define [SHELL\\_SEARCH\\_IN\\_HIST](#) (1U)  
*Macro to set on/off history feature.*
- #define [SHELL\\_USE\\_FILE\\_STREAM](#) (0U)  
*Macro to select method stream.*
- #define [SHELL\\_AUTO\\_COMPLETE](#) (1U)  
*Macro to set on/off auto-complete feature.*
- #define [SHELL\\_BUFFER\\_SIZE](#) (64U)  
*Macro to set console buffer size.*
- #define [SHELL\\_MAX\\_ARGS](#) (8U)  
*Macro to set maximum arguments in command.*
- #define [SHELL\\_HIST\\_MAX](#) (3U)  
*Macro to set maximum count of history commands.*
- #define [SHELL\\_MAX\\_CMD](#) (6U)  
*Macro to set maximum count of commands.*

## Typedefs

- typedef void(\* [send\\_data\\_cb\\_t](#))(uint8\_t \*buf, uint32\_t len)  
*Shell user send data callback prototype.*
- typedef void(\* [recv\\_data\\_cb\\_t](#))(uint8\_t \*buf, uint32\_t len)  
*Shell user receiver data callback prototype.*
- typedef int(\* [printf\\_data\\_t](#))(const char \*format,...)

*Shell user printf data prototype.*

- typedef int32\_t(\* [cmd\\_function\\_t](#))(p\_shell\_context\_t context, int32\_t argc, char \*\*argv)  
*User command function prototype.*

## Enumerations

- enum [fun\\_key\\_status\\_t](#) {  
    [kSHELL\\_Normal](#) = 0U,  
    [kSHELL\\_Special](#) = 1U,  
    [kSHELL\\_Function](#) = 2U }  
*A type for the handle special key.*

## Shell functional operation

- void [SHELL\\_Init](#) (p\_shell\_context\_t context, [send\\_data\\_cb\\_t](#) send\_cb, [recv\\_data\\_cb\\_t](#) recv\_cb, [printf\\_data\\_t](#) shell\_printf, char \*prompt)  
*Enables the clock gate and configures the Shell module according to the configuration structure.*
- int32\_t [SHELL\\_RegisterCommand](#) (const [shell\\_command\\_context\\_t](#) \*command\_context)  
*Shell register command.*
- int32\_t [SHELL\\_Main](#) (p\_shell\_context\_t context)  
*Main loop for Shell.*

## 45.3 Data Structure Documentation

### 45.3.1 struct shell\_context\_struct

#### Data Fields

- char \* [prompt](#)  
*Prompt string.*
- enum [\\_fun\\_key\\_status](#) [stat](#)  
*Special key status.*
- char [line](#) [[SHELL\\_BUFFER\\_SIZE](#)]  
*Consult buffer.*
- uint8\_t [cmd\\_num](#)  
*Number of user commands.*
- uint8\_t [l\\_pos](#)  
*Total line position.*
- uint8\_t [c\\_pos](#)  
*Current line position.*
- [send\\_data\\_cb\\_t](#) [send\\_data\\_func](#)  
*Send data interface operation.*
- [recv\\_data\\_cb\\_t](#) [recv\\_data\\_func](#)  
*Receive data interface operation.*
- uint16\_t [hist\\_current](#)  
*Current history command in hist buff.*
- uint16\_t [hist\\_count](#)  
*Total history command in hist buff.*
- char [hist\\_buf](#) [[SHELL\\_HIST\\_MAX](#)][[SHELL\\_BUFFER\\_SIZE](#)]

## Data Structure Documentation

- History buffer.*
- bool [exit](#)  
*Exit Flag.*

### 45.3.2 struct shell\_command\_context\_t

#### Data Fields

- const char \* [pcCommand](#)  
*The command that is executed.*
- char \* [pcHelpString](#)  
*String that describes how to use the command.*
- const [cmd\\_function\\_t](#) [pFuncCallBack](#)  
*A pointer to the callback function that returns the output generated by the command.*
- uint8\_t [cExpectedNumberOfParameters](#)  
*Commands expect a fixed number of parameters, which may be zero.*

#### 45.3.2.0.0.105 Field Documentation

##### 45.3.2.0.0.105.1 const char\* shell\_command\_context\_t::pcCommand

For example "help". It must be all lower case.

##### 45.3.2.0.0.105.2 char\* shell\_command\_context\_t::pcHelpString

It should start with the command itself, and end with "\r\n". For example "help: Returns a list of all the commands\r\n".

##### 45.3.2.0.0.105.3 const cmd\_function\_t shell\_command\_context\_t::pFuncCallBack

##### 45.3.2.0.0.105.4 uint8\_t shell\_command\_context\_t::cExpectedNumberOfParameters

### 45.3.3 struct shell\_command\_context\_list\_t

#### Data Fields

- const [shell\\_command\\_context\\_t](#) \* [CommandList](#) [[SHELL\\_MAX\\_CMD](#)]  
*The command table list.*
- uint8\_t [numberOfCommandInList](#)  
*The total command in list.*

## 45.4 Macro Definition Documentation

45.4.1 `#define SHELL_USE_HISTORY (0U)`

45.4.2 `#define SHELL_SEARCH_IN_HIST (1U)`

45.4.3 `#define SHELL_USE_FILE_STREAM (0U)`

45.4.4 `#define SHELL_AUTO_COMPLETE (1U)`

45.4.5 `#define SHELL_BUFFER_SIZE (64U)`

45.4.6 `#define SHELL_MAX_ARGS (8U)`

45.4.7 `#define SHELL_HIST_MAX (3U)`

45.4.8 `#define SHELL_MAX_CMD (6U)`

## 45.5 Typedef Documentation

45.5.1 `typedef void(* send_data_cb_t)(uint8_t *buf, uint32_t len)`

45.5.2 `typedef void(* recv_data_cb_t)(uint8_t *buf, uint32_t len)`

45.5.3 `typedef int(* printf_data_t)(const char *format,...)`

45.5.4 `typedef int32_t(* cmd_function_t)(p_shell_context_t context, int32_t argc, char **argv)`

## 45.6 Enumeration Type Documentation

45.6.1 `enum fun_key_status_t`

Enumerator

*kSHELL\_Normal* Normal key.

*kSHELL\_Special* Special key.

*kSHELL\_Function* Function key.

### 45.7 Function Documentation

#### 45.7.1 void SHELL\_Init ( p\_shell\_context\_t *context*, send\_data\_cb\_t *send\_cb*, recv\_data\_cb\_t *recv\_cb*, printf\_data\_t *shell\_printf*, char \* *prompt* )

This function must be called before calling all other Shell functions. Call operation the Shell commands with user-defined settings. The example below shows how to set up the middleware Shell and how to call the SHELL\_Init function by passing in these parameters. This is an example.

```
*  shell_context_struct user_context;
*  SHELL_Init(&user_context, SendDataFunc, ReceiveDataFunc, "SHELL>> ");
*
```

##### Parameters

|                |                                                          |
|----------------|----------------------------------------------------------|
| <i>context</i> | The pointer to the Shell environment and runtime states. |
| <i>send_cb</i> | The pointer to call back send data function.             |
| <i>recv_cb</i> | The pointer to call back receive data function.          |
| <i>prompt</i>  | The string prompt of Shell                               |

#### 45.7.2 int32\_t SHELL\_RegisterCommand ( const shell\_command\_context\_t \* *command\_context* )

##### Parameters

|                           |                                            |
|---------------------------|--------------------------------------------|
| <i>command_ - context</i> | The pointer to the command data structure. |
|---------------------------|--------------------------------------------|

##### Returns

-1 if error or 0 if success

#### 45.7.3 int32\_t SHELL\_Main ( p\_shell\_context\_t *context* )

Main loop for Shell; After this function is called, Shell begins to initialize the basic variables and starts to work.

## Parameters

|                |                                                          |
|----------------|----------------------------------------------------------|
| <i>context</i> | The pointer to the Shell environment and runtime states. |
|----------------|----------------------------------------------------------|

## Returns

This function does not return until Shell command exit was called.





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