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# MCUXpresso SDK API Reference Manual

NXP Semiconductors



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# Chapter 1

## Introduction

The MCUXpresso Software Development Kit (MCUXpresso SDK) is a collection of software enablement for NXP Microcontrollers that includes peripheral drivers, multicore support and integrated RTOS support for FreeRTOS<sup>TM</sup>. In addition to the base enablement, the MCUXpresso SDK is augmented with demo applications, driver example projects, and API documentation to help users quickly leverage the support provided by MCUXpresso SDK. The [MCUXpresso SDK Web Builder](#) is available to provide access to all MCUXpresso SDK packages. See the *MCUXpresso Software Development Kit (SDK) Release Notes* (document MCUXSDKRNN) in the Supported Devices section at [MCUXpresso-SDK: Software Development Kit for MCUXpresso](#) for details.

The MCUXpresso SDK is built with the following runtime software components:

- Arm<sup>®</sup> and DSP standard libraries, and CMSIS-compliant device header files which provide direct access to the peripheral registers.
- Peripheral drivers that provide stateless, high-performance, ease-of-use APIs. Communication drivers provide higher-level transactional APIs for a higher-performance option.
- RTOS wrapper driver built on top of MCUXpresso SDK peripheral drivers and leverage native RTOS services to better comply to the RTOS cases.
- Real time operation systems (RTOS) for FreeRTOS OS.
- Stacks and middleware in source or object formats including:
- CMSIS-DSP, a suite of common signal processing functions.
- The MCUXpresso SDK comes complete with software examples demonstrating the usage of the peripheral drivers, RTOS wrapper drivers, middleware, and RTOSes.

The peripheral drivers and RTOS driver wrappers can be used across multiple devices within the product family without modification. The configuration items for each driver are encapsulated into C language data structures. Device-specific configuration information is provided as part of the MCUXpresso SDK and need not be modified by the user. If necessary, the user is able to modify the peripheral driver and RTOS wrapper driver configuration during runtime. The driver examples demonstrate how to configure the drivers by passing the proper configuration data to the APIs. The folder structure is organized to reduce the total number of includes required to compile a project.

The rest of this document describes the API references in detail for the peripheral drivers and RTOS wrapper drivers. For the latest version of this and other MCUXpresso SDK documents, see the [mcuxpresso.nxp.com/apidoc/](#).

<b>Deliverable</b>	<b>Location</b>
Demo Applications	<install_dir>/boards/<board_name>/demo_apps
Driver Examples	<install_dir>/boards/<board_name>/driver_examples
Documentation	<install_dir>/docs
Middleware	<install_dir>/middleware
Drivers	<install_dir>/<device_name>/drivers/
CMSIS Standard Arm Cortex-M Headers, math and DSP Libraries	<install_dir>/CMSIS
Device Startup and Linker	<install_dir>/<device_name>/<toolchain>/
MCUXpresso SDK Utilities	<install_dir>/devices/<device_name>/utilities
RTOS Kernel Code	<install_dir>/rtos

### **MCUXpresso SDK Folder Structure**

# Chapter 2

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# Chapter 3

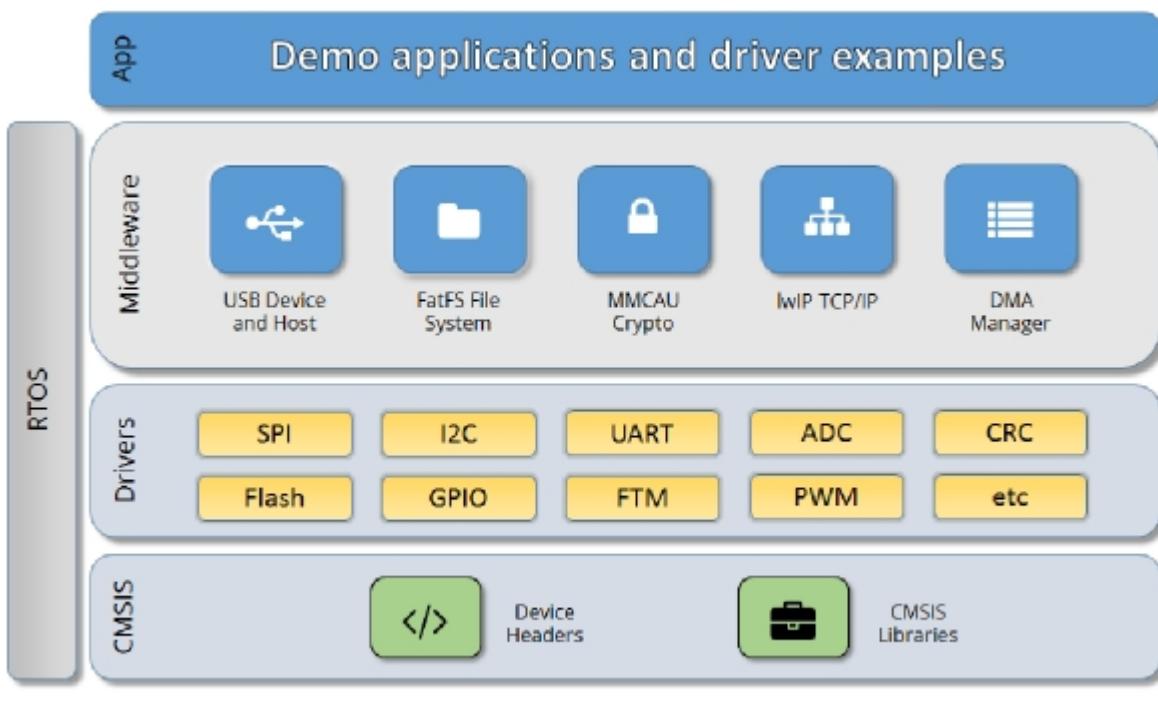
## Architectural Overview

This chapter provides the architectural overview for the MCUXpresso Software Development Kit (MCUXpresso SDK). It describes each layer within the architecture and its associated components.

### Overview

The MCUXpresso SDK architecture consists of five key components listed below.

1. The Arm Cortex Microcontroller Software Interface Standard (CMSIS) CORE compliance device-specific header files, SOC Header, and CMSIS math/DSP libraries.
2. Peripheral Drivers
3. Real-time Operating Systems (RTOS)
4. Stacks and Middleware that integrate with the MCUXpresso SDK
5. Demo Applications based on the MCUXpresso SDK



### MCU header files

Each supported MCU device in the MCUXpresso SDK has an overall System-on Chip (SoC) memory-

mapped header file. This header file contains the memory map and register base address for each peripheral and the IRQ vector table with associated vector numbers. The overall SoC header file provides access to the peripheral registers through pointers and predefined bit masks. In addition to the overall SoC memory-mapped header file, the MCUXpresso SDK includes a feature header file for each device. The feature header file allows NXP to deliver a single software driver for a given peripheral. The feature file ensures that the driver is properly compiled for the target SOC.

## CMSIS Support

Along with the SoC header files and peripheral extension header files, the MCUXpresso SDK also includes common CMSIS header files for the Arm Cortex-M core and the math and DSP libraries from the latest CMSIS release. The CMSIS DSP library source code is also included for reference.

## MCUXpresso SDK Peripheral Drivers

The MCUXpresso SDK peripheral drivers mainly consist of low-level functional APIs for the MCU product family on-chip peripherals and also of high-level transactional APIs for some bus drivers/DM-A driver/eDMA driver to quickly enable the peripherals and perform transfers.

All MCUXpresso SDK peripheral drivers only depend on the CMSIS headers, device feature files, fsl\_common.h, and fsl\_clock.h files so that users can easily pull selected drivers and their dependencies into projects. With the exception of the clock/power-relevant peripherals, each peripheral has its own driver. Peripheral drivers handle the peripheral clock gating/ungating inside the drivers during initialization and deinitialization respectively.

Low-level functional APIs provide common peripheral functionality, abstracting the hardware peripheral register accesses into a set of stateless basic functional operations. These APIs primarily focus on the control, configuration, and function of basic peripheral operations. The APIs hide the register access details and various MCU peripheral instantiation differences so that the application can be abstracted from the low-level hardware details. The API prototypes are intentionally similar to help ensure easy portability across supported MCUXpresso SDK devices.

Transactional APIs provide a quick method for customers to utilize higher-level functionality of the peripherals. The transactional APIs utilize interrupts and perform asynchronous operations without user intervention. Transactional APIs operate on high-level logic that requires data storage for internal operation context handling. However, the Peripheral Drivers do not allocate this memory space. Rather, the user passes in the memory to the driver for internal driver operation. Transactional APIs ensure the NVIC is enabled properly inside the drivers. The transactional APIs do not meet all customer needs, but provide a baseline for development of custom user APIs.

Note that the transactional drivers never disable an NVIC after use. This is due to the shared nature of interrupt vectors on devices. It is up to the user to ensure that NVIC interrupts are properly disabled after usage is complete.

## Interrupt handling for transactional APIs

A double weak mechanism is introduced for drivers with transactional API. The double weak indicates two levels of weak vector entries. See the examples below:

```
PUBWEAK SPI0_IRQHandler  
PUBWEAK SPI0_DriverIRQHandler  
SPI0_IRQHandler
```

```
LDR      R0, =SPI0_DriverIRQHandler  
BX      R0
```

The first level of the weak implementation are the functions defined in the vector table. In the devices/<DEVICE\_NAME>/<TOOLCHAIN>/startup\_<DEVICE\_NAME>.s/.S file, the implementation of the first layer weak function calls the second layer of weak function. The implementation of the second layer weak function (ex. SPI0\_DriverIRQHandler) jumps to itself (B). The MCUXpresso SDK drivers with transactional APIs provide the reimplementation of the second layer function inside of the peripheral driver. If the MCUXpresso SDK drivers with transactional APIs are linked into the image, the SPI0\_DriverIRQHandler is replaced with the function implemented in the MCUXpresso SDK SPI driver.

The reason for implementing the double weak functions is to provide a better user experience when using the transactional APIs. For drivers with a transactional function, call the transactional APIs and the drivers complete the interrupt-driven flow. Users are not required to redefine the vector entries out of the box. At the same time, if users are not satisfied by the second layer weak function implemented in the MCUXpresso SDK drivers, users can redefine the first layer weak function and implement their own interrupt handler functions to suit their implementation.

The limitation of the double weak mechanism is that it cannot be used for peripherals that share the same vector entry. For this use case, redefine the first layer weak function to enable the desired peripheral interrupt functionality. For example, if the MCU's UART0 and UART1 share the same vector entry, redefine the UART0\_UART1\_IRQHandler according to the use case requirements.

## Feature Header Files

The peripheral drivers are designed to be reusable regardless of the peripheral functional differences from one MCU device to another. An overall Peripheral Feature Header File is provided for the MCUXpresso SDK-supported MCU device to define the features or configuration differences for each sub-family device.

## Application

See the *Getting Started with MCUXpresso SDK* document (MCUXSDKGSUG).

# Chapter 4

## Clock Driver

### 4.1 Overview

The MCUXpresso SDK provides APIs for MCUXpresso SDK devices' clock operation.

The clock driver supports:

- Clock generator (PLL, FLL, and so on) configuration
- Clock mux and divider configuration
- Getting clock frequency

### Files

- file `fsl_clock.h`

### Data Structures

- struct `clock_arm_pll_config_t`  
*PLL configuration for ARM.* [More...](#)
- struct `clock_usb_pll_config_t`  
*PLL configuration for USB.* [More...](#)
- struct `clock_sys_pll_config_t`  
*PLL configuration for System.* [More...](#)
- struct `clock_audio_pll_config_t`  
*PLL configuration for AUDIO and VIDEO.* [More...](#)
- struct `clock_video_pll_config_t`  
*PLL configuration for AUDIO and VIDEO.* [More...](#)
- struct `clock_enet_pll_config_t`  
*PLL configuration for ENET.* [More...](#)

### Macros

- `#define FSL_SDK_DISABLE_DRIVER_CLOCK_CONTROL 0`  
*Configure whether driver controls clock.*
- `#define CCSR_OFFSET 0x0C`  
*CCM registers offset.*
- `#define PLL_ARM_OFFSET 0x00`  
*CCM Analog registers offset.*
- `#define CCM_ANALOG_TUPLE(reg, shift) (((reg)&0xFFFFU) << 16U) | (shift)`  
*CCM ANALOG tuple macros to map corresponding registers and bit fields.*
- `#define CLKPN_FREQ 0U`  
*clockIPN frequency.*
- `#define ADC_CLOCKS`  
*Clock ip name array for ADC.*
- `#define AOI_CLOCKS`

- `#define BEE_CLOCKS`  
*Clock ip name array for BEE.*
- `#define CMP_CLOCKS`  
*Clock ip name array for CMP.*
- `#define DCDC_CLOCKS`  
*Clock ip name array for DCDC.*
- `#define DCP_CLOCKS`  
*Clock ip name array for DCP.*
- `#define DMAMUX_CLOCKS`  
*Clock ip name array for DMAMUX\_CLOCKS.*
- `#define EDMA_CLOCKS`  
*Clock ip name array for DMA.*
- `#define ENC_CLOCKS`  
*Clock ip name array for ENC.*
- `#define ENET_CLOCKS`  
*Clock ip name array for ENET.*
- `#define EWM_CLOCKS`  
*Clock ip name array for EWM.*
- `#define FLEXCAN_CLOCKS`  
*Clock ip name array for FLEXCAN.*
- `#define FLEXCAN_PERIPH_CLOCKS`  
*Clock ip name array for FLEXCAN Peripheral clock.*
- `#define FLEXIO_CLOCKS`  
*Clock ip name array for FLEXIO.*
- `#define FLEXRAM_CLOCKS`  
*Clock ip name array for FLEXRAM.*
- `#define FLEXSPI_CLOCKS`  
*Clock ip name array for FLEXSPI.*
- `#define FLEXSPI_EXSC_CLOCKS`  
*Clock ip name array for FLEXSPI EXSC.*
- `#define GPIO_CLOCKS`  
*Clock ip name array for GPIO.*
- `#define GPT_CLOCKS`  
*Clock ip name array for GPT.*
- `#define LCDIF_CLOCKS`  
*Clock ip name array for LCDIF.*
- `#define LCDIF_PERIPH_CLOCKS`  
*Clock ip name array for LCDIF PIXEL.*
- `#define LPI2C_CLOCKS`  
*Clock ip name array for LPI2C.*
- `#define LPSPI_CLOCKS`  
*Clock ip name array for LPSPI.*
- `#define LPUART_CLOCKS`  
*Clock ip name array for LPUART.*
- `#define MQS_CLOCKS`  
*Clock ip name array for MQS.*
- `#define OCRAM_EXSC_CLOCKS`  
*Clock ip name array for OCRAM EXSC.*
- `#define PIT_CLOCKS`  
*Clock ip name array for PIT.*

- #define **PWM\_CLOCKS**  
*Clock ip name array for PWM.*
- #define **PXP\_CLOCKS**  
*Clock ip name array for PXP.*
- #define **RTWDOG\_CLOCKS**  
*Clock ip name array for RTWDOG.*
- #define **SAI\_CLOCKS**  
*Clock ip name array for SAI.*
- #define **SEMC\_CLOCKS**  
*Clock ip name array for SEMC.*
- #define **SEMC\_EXSC\_CLOCKS**  
*Clock ip name array for SEMC EXSC.*
- #define **TMR\_CLOCKS**  
*Clock ip name array for QTIMER.*
- #define **TRNG\_CLOCKS**  
*Clock ip name array for TRNG.*
- #define **TSC\_CLOCKS**  
*Clock ip name array for TSC.*
- #define **WDOG\_CLOCKS**  
*Clock ip name array for WDOG.*
- #define **USDHC\_CLOCKS**  
*Clock ip name array for USDHC.*
- #define **SPDIF\_CLOCKS**  
*Clock ip name array for SPDIF.*
- #define **XBARA\_CLOCKS**  
*Clock ip name array for XBARA.*
- #define **XBARB\_CLOCKS**  
*Clock ip name array for XBARB.*
- #define **kCLOCK\_CoreSysClk kCLOCK\_CpuClk**  
*For compatible with other platforms without CCM.*
- #define **CLOCK\_GetCoreSysClkFreq CLOCK\_GetCpuClkFreq**  
*For compatible with other platforms without CCM.*

## Enumerations

- enum `clock_name_t` {  
    `kCLOCK_CpuClk` = 0x0U,  
    `kCLOCK_AhbClk` = 0x1U,  
    `kCLOCK_SemcClk` = 0x2U,  
    `kCLOCK_IpgClk` = 0x3U,  
    `kCLOCK_PerClk` = 0x4U,  
    `kCLOCK_OscClk` = 0x5U,  
    `kCLOCK_RtcClk` = 0x6U,  
    `kCLOCK_ArmPllClk` = 0x7U,  
    `kCLOCK_Usb1PllClk` = 0x8U,  
    `kCLOCK_Usb1PllPfd0Clk` = 0x9U,  
    `kCLOCK_Usb1PllPfd1Clk` = 0xAU,  
    `kCLOCK_Usb1PllPfd2Clk` = 0xBU,  
    `kCLOCK_Usb1PllPfd3Clk` = 0xCU,  
    `kCLOCK_Usb1SwClk` = 0x18U,  
    `kCLOCK_Usb1Sw120MClk` = 0x19U,  
    `kCLOCK_Usb1Sw60MClk` = 0x1AU,  
    `kCLOCK_Usb1Sw80MClk` = 0x1BU,  
    `kCLOCK_Usb2PllClk` = 0xDU,  
    `kCLOCK_SysPllClk` = 0xEU,  
    `kCLOCK_SysPllPfd0Clk` = 0xFU,  
    `kCLOCK_SysPllPfd1Clk` = 0x10U,  
    `kCLOCK_SysPllPfd2Clk` = 0x11U,  
    `kCLOCK_SysPllPfd3Clk` = 0x12U,  
    `kCLOCK_EnetPll0Clk` = 0x13U,  
    `kCLOCK_EnetPll1Clk` = 0x14U,  
    `kCLOCK_AudioPllClk` = 0x15U,  
    `kCLOCK_VideoPllClk` = 0x16U,  
    `kCLOCK_NoneName` = `CLOCK_SOURCE_NONE` }

*Clock name used to get clock frequency.*

- enum `clock_ip_name_t` { ,

```

kCLOCK_Aips_tz1 = (0U << 8U) | CCM_CCCR0(CG0_SHIFT),
kCLOCK_Aips_tz2 = (0U << 8U) | CCM_CCCR0(CG1_SHIFT),
kCLOCK_Mqs = (0U << 8U) | CCM_CCCR0(CG2_SHIFT),
kCLOCK_FlexSpiExsc = (0U << 8U) | CCM_CCCR0(CG3_SHIFT),
kCLOCK_Sim_M_Main = (0U << 8U) | CCM_CCCR0(CG4_SHIFT),
kCLOCK_Dcp = (0U << 8U) | CCM_CCCR0(CG5_SHIFT),
kCLOCK_Lpuart3 = (0U << 8U) | CCM_CCCR0(CG6_SHIFT),
kCLOCK_Can1 = (0U << 8U) | CCM_CCCR0(CG7_SHIFT),
kCLOCK_Can1S = (0U << 8U) | CCM_CCCR0(CG8_SHIFT),
kCLOCK_Can2 = (0U << 8U) | CCM_CCCR0(CG9_SHIFT),
kCLOCK_Can2S = (0U << 8U) | CCM_CCCR0(CG10_SHIFT),
kCLOCK_Trace = (0U << 8U) | CCM_CCCR0(CG11_SHIFT),
kCLOCK_Gpt2 = (0U << 8U) | CCM_CCCR0(CG12_SHIFT),
kCLOCK_Gpt2S = (0U << 8U) | CCM_CCCR0(CG13_SHIFT),
kCLOCK_Lpuart2 = (0U << 8U) | CCM_CCCR0(CG14_SHIFT),
kCLOCK_Gpio2 = (0U << 8U) | CCM_CCCR0(CG15_SHIFT),
kCLOCK_Lpssi1 = (1U << 8U) | CCM_CCCR1(CG0_SHIFT),
kCLOCK_Lpssi2 = (1U << 8U) | CCM_CCCR1(CG1_SHIFT),
kCLOCK_Lpssi3 = (1U << 8U) | CCM_CCCR1(CG3_SHIFT),
kCLOCK_Adc2 = (1U << 8U) | CCM_CCCR1(CG4_SHIFT),
kCLOCK_Enet = (1U << 8U) | CCM_CCCR1(CG5_SHIFT),
kCLOCK_Pit = (1U << 8U) | CCM_CCCR1(CG6_SHIFT),
kCLOCK_Aoi2 = (1U << 8U) | CCM_CCCR1(CG7_SHIFT),
kCLOCK_Adcl = (1U << 8U) | CCM_CCCR1(CG8_SHIFT),
kCLOCK_SemcExsc = (1U << 8U) | CCM_CCCR1(CG9_SHIFT),
kCLOCK_Gpt1 = (1U << 8U) | CCM_CCCR1(CG10_SHIFT),
kCLOCK_Gpt1S = (1U << 8U) | CCM_CCCR1(CG11_SHIFT),
kCLOCK_Lpuart4 = (1U << 8U) | CCM_CCCR1(CG12_SHIFT),
kCLOCK_Gpio1 = (1U << 8U) | CCM_CCCR1(CG13_SHIFT),
kCLOCK_Csu = (1U << 8U) | CCM_CCCR1(CG14_SHIFT),
kCLOCK_Gpio5 = (1U << 8U) | CCM_CCCR1(CG15_SHIFT),
kCLOCK_OramExsc = (2U << 8U) | CCM_CCCR2(CG0_SHIFT),
kCLOCK_IomuxcSnvs = (2U << 8U) | CCM_CCCR2(CG2_SHIFT),
kCLOCK_Lpi2c1 = (2U << 8U) | CCM_CCCR2(CG3_SHIFT),
kCLOCK_Lpi2c2 = (2U << 8U) | CCM_CCCR2(CG4_SHIFT),
kCLOCK_Lpi2c3 = (2U << 8U) | CCM_CCCR2(CG5_SHIFT),
kCLOCK_Ocotp = (2U << 8U) | CCM_CCCR2(CG6_SHIFT),
kCLOCK_Xbar3 = (2U << 8U) | CCM_CCCR2(CG7_SHIFT),
kCLOCK_Ipmux1 = (2U << 8U) | CCM_CCCR2(CG8_SHIFT),
kCLOCK_Ipmux2 = (2U << 8U) | CCM_CCCR2(CG9_SHIFT),
kCLOCK_Ipmux3 = (2U << 8U) | CCM_CCCR2(CG10_SHIFT),
kCLOCK_Xbar1 = (2U << 8U) | CCM_CCCR2(CG11_SHIFT),
kCLOCK_Xbar2 = (2U << 8U) | CCM_CCCR2(CG12_SHIFT),
kCLOCK_Gpio3 = (2U << 8U) | CCM_CCCR2(CG13_SHIFT),
kCLOCK_Lcd = (2U << 8U) | CCM_CCCR2(CG14_SHIFT),
kCLOCK_Pxp = (2U << 8U) | CCM_CCCR2(CG15_SHIFT),
kCLOCK_Flo2 = (3U << 8U) | CCM_CCCR2(CG0_SHIFT),
kCLOCK_Lpuart5 = (3U << 8U) | CCM_CCCR3(CG1_SHIFT),
kCLOCK_Semc = (3U << 8U) | CCM_CCCR3(CG2_SHIFT),

```

- `kCLOCK_Flexio3 = (7U << 8U) | CCM_CCGR7(CG6_SHIFT) }`
  - CCM CCGR gate control for each module independently.*
- enum `clock_osc_t` {
   
`kCLOCK_RcOsc = 0U,`
  
`kCLOCK_XtalOsc = 1U }`
  - OSC 24M source select.*
- enum `clock_gate_value_t` {
   
`kCLOCK_ClockNotNeeded = 0U,`
  
`kCLOCK_ClockNeededRun = 1U,`
  
`kCLOCK_ClockNeededRunWait = 3U }`
  - Clock gate value.*
- enum `clock_mode_t` {
   
`kCLOCK_ModeRun = 0U,`
  
`kCLOCK_ModeWait = 1U,`
  
`kCLOCK_ModeStop = 2U }`
  - System clock mode.*
- enum `clock_mux_t` {
   
`kCLOCK_Pl3SwMux,`
  
`kCLOCK_PeriphMux,`
  
`kCLOCK_SemcAltMux,`
  
`kCLOCK_SemcMux,`
  
`kCLOCK_PrePeriphMux,`
  
`kCLOCK_TraceMux,`
  
`kCLOCK_PeriphClk2Mux,`
  
`kCLOCK_Flexspi2Mux,`
  
`kCLOCK_LpSpiMux,`
  
`kCLOCK_FlexspiMux,`
  
`kCLOCK_Usdhc2Mux,`
  
`kCLOCK_Usdhc1Mux,`
  
`kCLOCK_Sai3Mux,`
  
`kCLOCK_Sai2Mux,`
  
`kCLOCK_Sai1Mux,`
  
`kCLOCK_PerclkMux,`
  
`kCLOCK_Flexio2Mux,`
  
`kCLOCK_CanMux,`
  
`kCLOCK_UartMux,`
  
`kCLOCK_SpdifMux,`
  
`kCLOCK_Flexio1Mux,`
  
`kCLOCK_Lpi2cMux,`
  
`kCLOCK_LcdifPreMux }`
  - MUX control names for clock mux setting.*
- enum `clock_div_value_t` {

```
kCLOCK_ArmDivBy1 = 0,  
kCLOCK_ArmDivBy2 = 1,  
kCLOCK_ArmDivBy3 = 2,  
kCLOCK_ArmDivBy4 = 3,  
kCLOCK_ArmDivBy5 = 4,  
kCLOCK_ArmDivBy6 = 5,  
kCLOCK_ArmDivBy7 = 6,  
kCLOCK_ArmDivBy8 = 7,  
kCLOCK_PeriphClk2DivBy1 = 0,  
kCLOCK_PeriphClk2DivBy2 = 1,  
kCLOCK_PeriphClk2DivBy3 = 2,  
kCLOCK_PeriphClk2DivBy4 = 3,  
kCLOCK_PeriphClk2DivBy5 = 4,  
kCLOCK_PeriphClk2DivBy6 = 5,  
kCLOCK_PeriphClk2DivBy7 = 6,  
kCLOCK_PeriphClk2DivBy8 = 7,  
kCLOCK_SemcDivBy1 = 0,  
kCLOCK_SemcDivBy2 = 1,  
kCLOCK_SemcDivBy3 = 2,  
kCLOCK_SemcDivBy4 = 3,  
kCLOCK_SemcDivBy5 = 4,  
kCLOCK_SemcDivBy6 = 5,  
kCLOCK_SemcDivBy7 = 6,  
kCLOCK_SemcDivBy8 = 7,  
kCLOCK_AhbDivBy1 = 0,  
kCLOCK_AhbDivBy2 = 1,  
kCLOCK_AhbDivBy3 = 2,  
kCLOCK_AhbDivBy4 = 3,  
kCLOCK_AhbDivBy5 = 4,  
kCLOCK_AhbDivBy6 = 5,  
kCLOCK_AhbDivBy7 = 6,  
kCLOCK_AhbDivBy8 = 7,  
kCLOCK_IpgDivBy1 = 0,  
kCLOCK_IpgDivBy2 = 1,  
kCLOCK_IpgDivBy3 = 2,  
kCLOCK_IpgDivBy4 = 3,  
kCLOCK_Flexspi2DivBy1 = 0,  
kCLOCK_Flexspi2DivBy2 = 1,  
kCLOCK_Flexspi2DivBy3 = 2,  
kCLOCK_Flexspi2DivBy4 = 3,  
kCLOCK_Flexspi2DivBy5 = 4,  
kCLOCK_Flexspi2DivBy6 = 5,  
kCLOCK_Flexspi2DivBy7 = 6,  
kCLOCK_Flexspi2DivBy8 = 7,  
kCLOCK_LpspiDivBy1 = 0,  
kCLOCK_LpspiDivBy2 = 1,
```

- ```
kCLOCK_MiscDivBy64 = 63 }
```

*Clock divider value.*
- enum `clock_div_t` {
 

```
kCLOCK_ArmDiv,
```

```
kCLOCK_PeriphClk2Div,
```

```
kCLOCK_SemcDiv,
```

```
kCLOCK_AhbDiv,
```

```
kCLOCK_IpgDiv,
```

```
kCLOCK_Flexspi2Div,
```

```
kCLOCK_LpspiDiv,
```

```
kCLOCK_LcdifDiv,
```

```
kCLOCK_FlexspiDiv,
```

```
kCLOCK_PerclkDiv,
```

```
kCLOCK_CanDiv,
```

```
kCLOCK_TraceDiv,
```

```
kCLOCK_Usdhc2Div,
```

```
kCLOCK_Usdhc1Div,
```

```
kCLOCK_UartDiv,
```

```
kCLOCK_Flexio2Div,
```

```
kCLOCK_Sai3PreDiv,
```

```
kCLOCK_Sai3Div,
```

```
kCLOCK_Flexio2PreDiv,
```

```
kCLOCK_Sai1PreDiv,
```

```
kCLOCK_Sai1Div,
```

```
kCLOCK_Sai2PreDiv,
```

```
kCLOCK_Sai2Div,
```

```
kCLOCK_Spdif0PreDiv,
```

```
kCLOCK_Spdif0Div,
```

```
kCLOCK_Flexio1PreDiv,
```

```
kCLOCK_Flexio1Div,
```

```
kCLOCK_Lpi2cDiv,
```

```
kCLOCK_LcdifPreDiv,
```

```
kCLOCK_NonePreDiv = CLOCK_ROOT_NONE_PRE_DIV }
```

*DIV control names for clock div setting.*
- enum `clock_usb_src_t` {
 

```
kCLOCK_Usb480M = 0,
```

```
kCLOCK_UsbSrcUnused = (int)0xFFFFFFFFU }
```

*USB clock source definition.*
- enum `clock_usb_phy_src_t` { 

```
kCLOCK_Usbphy480M = 0 }
```

*Source of the USB HS PHY.*
- enum `_clock_pll_clk_src` {
 

```
kCLOCK_PliClkSrc24M = 0U,
```

```
kCLOCK_PliSrcClkPN = 1U }
```

*PLL clock source, bypass cloco source also.*
- enum `clock_pll_t` {
 

```
kCLOCK_PlArm = CCM_ANALOG_TUPLE(PLL_ARM_OFFSET, CCM_ANALOG_PLL_AR-
```

```

M_ENABLE_SHIFT),
kCLOCK_PllSys = CCM_ANALOG_TUPLE(PLL_SYS_OFFSET, CCM_ANALOG_PLL_SYS-
_ENABLE_SHIFT),
kCLOCK_PllUsb1 = CCM_ANALOG_TUPLE(PLL_USB1_OFFSET, CCM_ANALOG_PLL_U-
SB1_ENABLE_SHIFT),
kCLOCK_PllAudio = CCM_ANALOG_TUPLE(PLL_AUDIO_OFFSET, CCM_ANALOG_PLL-
_AUDIO_ENABLE_SHIFT),
kCLOCK_PllVideo = CCM_ANALOG_TUPLE(PLL_VIDEO_OFFSET, CCM_ANALOG_PLL-
VIDEO_ENABLE_SHIFT),
kCLOCK_PllEnet = CCM_ANALOG_TUPLE(PLL_ENET_OFFSET, CCM_ANALOG_PLL_E-
NET_ENABLE_SHIFT),
kCLOCK_PllEnet25M = CCM_ANALOG_TUPLE(PLL_ENET_OFFSET, CCM_ANALOG_PL-
L_ENET_ENET_25M_REF_EN_SHIFT) }

```

*PLL name.*

- enum `clock_pfd_t` {
   
kCLOCK\_Pfd0 = 0U,
   
kCLOCK\_Pfd1 = 1U,
   
kCLOCK\_Pfd2 = 2U,
   
kCLOCK\_Pfd3 = 3U }

*PLL PFD name.*

- enum `clock_output1_selection_t` {
   
kCLOCK\_OutputPllUsb1 = 0U,
   
kCLOCK\_OutputPllSys = 1U,
   
kCLOCK\_OutputPllVideo = 3U,
   
kCLOCK\_OutputSemcClk = 5U,
   
kCLOCK\_OutputLcdifPixClk = 0xAU,
   
kCLOCK\_OutputAhbClk = 0xBU,
   
kCLOCK\_OutputIpgClk = 0xCU,
   
kCLOCK\_OutputPerClk = 0xDU,
   
kCLOCK\_OutputCkilSyncClk = 0xEU,
   
kCLOCK\_OutputPll4MainClk = 0xFU,
   
kCLOCK\_DisableClockOutput1 = 0x10U }

*The enumerater of clock output1's clock source, such as USB1 PLL, SYS PLL and so on.*

- enum `clock_output2_selection_t` {
   
kCLOCK\_OutputUsdhc1Clk = 3U,
   
kCLOCK\_OutputLpi2cClk = 6U,
   
kCLOCK\_OutputOscClk = 0xEU,
   
kCLOCK\_OutputUsdhc2Clk = 0x11U,
   
kCLOCK\_OutputSai1Clk = 0x12U,
   
kCLOCK\_OutputSai2Clk = 0x13U,
   
kCLOCK\_OutputSai3Clk = 0x14U,
   
kCLOCK\_OutputCanClk = 0x17U,
   
kCLOCK\_OutputFlexspiClk = 0x1BU,
   
kCLOCK\_OutputUartClk = 0x1CU,
   
kCLOCK\_OutputSpdif0Clk = 0x1DU,

```
kCLOCK_DisableClockOutput2 = 0x1FU }
```

*The enumerator of clock output2's clock source, such as USDHC1 clock root, LPI2C clock root and so on.*

- enum `clock_output_divider_t` {
   
kCLOCK\_DivideBy1 = 0U,
   
kCLOCK\_DivideBy2,
   
kCLOCK\_DivideBy3,
   
kCLOCK\_DivideBy4,
   
kCLOCK\_DivideBy5,
   
kCLOCK\_DivideBy6,
   
kCLOCK\_DivideBy7,
   
kCLOCK\_DivideBy8 }

*The enumerator of clock output's divider.*

- enum `clock_root_t` {
   
kCLOCK\_Usdhc1ClkRoot = 0U,
   
kCLOCK\_Usdhc2ClkRoot,
   
kCLOCK\_FlexspiClkRoot,
   
kCLOCK\_Flexspi2ClkRoot,
   
kCLOCK\_LpSpiClkRoot,
   
kCLOCK\_TraceClkRoot,
   
kCLOCK\_Sai1ClkRoot,
   
kCLOCK\_Sai2ClkRoot,
   
kCLOCK\_Sai3ClkRoot,
   
kCLOCK\_Lpi2cClkRoot,
   
kCLOCK\_CanClkRoot,
   
kCLOCK\_UartClkRoot,
   
kCLOCK\_LcdifClkRoot,
   
kCLOCK\_SpdifClkRoot,
   
kCLOCK\_Flexio1ClkRoot,
   
kCLOCK\_Flexio2ClkRoot }

*The enumerator of clock root.*

## Functions

- static void `CLOCK_SetMux (clock_mux_t mux, uint32_t value)`
  
*Set CCM MUX node to certain value.*
- static uint32\_t `CLOCK_GetMux (clock_mux_t mux)`
  
*Get CCM MUX value.*
- static void `CLOCK_SetDiv (clock_div_t divider, uint32_t value)`
  
*Set clock divider value.*
- static uint32\_t `CLOCK_GetDiv (clock_div_t divider)`
  
*Get CCM DIV node value.*
- static void `CLOCK_ControlGate (clock_ip_name_t name, clock_gate_value_t value)`
  
*Control the clock gate for specific IP.*
- static void `CLOCK_EnableClock (clock_ip_name_t name)`
  
*Enable the clock for specific IP.*
- static void `CLOCK_DisableClock (clock_ip_name_t name)`
  
*Disable the clock for specific IP.*
- static void `CLOCK_SetMode (clock_mode_t mode)`

- Setting the low power mode that system will enter on next assertion of `dsm_request` signal.
- static `uint32_t CLOCK_GetOscFreq (void)`  
Gets the OSC clock frequency.
- `uint32_t CLOCK_GetAhbFreq (void)`  
Gets the AHB clock frequency.
- `uint32_t CLOCK_GetSemcFreq (void)`  
Gets the SEMC clock frequency.
- `uint32_t CLOCK_GetIpqFreq (void)`  
Gets the IPQ clock frequency.
- `uint32_t CLOCK_GetPerClkFreq (void)`  
Gets the PER clock frequency.
- `uint32_t CLOCK_GetFreq (clock_name_t name)`  
Gets the clock frequency for a specific clock name.
- static `uint32_t CLOCK_GetCpuClkFreq (void)`  
Get the CCM CPU/core/system frequency.
- `uint32_t CLOCK_GetClockRootFreq (clock_root_t clockRoot)`  
Gets the frequency of selected clock root.
- `bool CLOCK_EnableUsbhs0Clock (clock_usb_src_t src, uint32_t freq)`  
Enable USB HS clock.

## Variables

- volatile `uint32_t g_xtalFreq`  
External XTAL (24M OSC/SYSOSC) clock frequency.
- volatile `uint32_t g_rtcXtalFreq`  
External RTC XTAL (32K OSC) clock frequency.

## Driver version

- `#define FSL_CLOCK_DRIVER_VERSION (MAKE_VERSION(2, 0, 0))`  
*CLOCK driver version 2.0.0.*
- `#define SDK_DEVICE_MAXIMUM_CPU_CLOCK_FREQUENCY (600000000UL)`
- `#define CCM_ANALOG_PLL_BYPASS_SHIFT (16U)`
- `#define CCM_ANALOG_PLL_BYPASS_CLK_SRC_MASK (0xC000U)`
- `#define CCM_ANALOG_PLL_BYPASS_CLK_SRC_SHIFT (14U)`

## OSC operations

- void `CLOCK_InitExternalClk (bool bypassXtalOsc)`  
Initialize the external 24MHz clock.
- void `CLOCK_DeinitExternalClk (void)`  
Deinitialize the external 24MHz clock.
- void `CLOCK_SwitchOsc (clock_osc_t osc)`  
Switch the OSC.
- static `uint32_t CLOCK_GetRtcFreq (void)`  
Gets the RTC clock frequency.
- static `void CLOCK_SetXtalFreq (uint32_t freq)`  
Set the XTAL (24M OSC) frequency based on board setting.
- static `void CLOCK_SetRtcXtalFreq (uint32_t freq)`  
Set the RTC XTAL (32K OSC) frequency based on board setting.
- void `CLOCK_InitRcOsc24M (void)`

- `void CLOCK_DeinitRcOsc24M (void)`  
*Power down the RCOSC 24M clock.*

## 4.2 Data Structure Documentation

### 4.2.1 struct clock\_arm\_pll\_config\_t

#### Data Fields

- `uint32_t loopDivider`  
*PLL loop divider.*
- `uint8_t src`  
*Pll clock source, reference \_clock\_pll\_clk\_src.*

#### Field Documentation

(1) `uint32_t clock_arm_pll_config_t::loopDivider`

Valid range for divider value: 54-108.  $Fout=Fin*loopDivider/2$ .

### 4.2.2 struct clock\_usb\_pll\_config\_t

#### Data Fields

- `uint8_t loopDivider`  
*PLL loop divider.*
- `uint8_t src`  
*Pll clock source, reference \_clock\_pll\_clk\_src.*

#### Field Documentation

(1) `uint8_t clock_usb_pll_config_t::loopDivider`

0 -  $Fout=Fref*20$ ; 1 -  $Fout=Fref*22$

### 4.2.3 struct clock\_sys\_pll\_config\_t

#### Data Fields

- `uint8_t loopDivider`  
*PLL loop divider.*
- `uint32_t numerator`  
*30 bit numerator of fractional loop divider.*
- `uint32_t denominator`  
*30 bit denominator of fractional loop divider*

- **uint8\_t src**  
*Pll clock source, reference \_clock\_pll\_clk\_src.*
- **uint16\_t ss\_stop**  
*Stop value to get frequency change.*
- **uint8\_t ss\_enable**  
*Enable spread spectrum modulation.*
- **uint16\_t ss\_step**  
*Step value to get frequency change step.*

**Field Documentation****(1) uint8\_t clock\_sys\_pll\_config\_t::loopDivider**

Intended to be 1 (528M). 0 - Fout=Fref\*20; 1 - Fout=Fref\*22

**(2) uint32\_t clock\_sys\_pll\_config\_t::numerator****(3) uint16\_t clock\_sys\_pll\_config\_t::ss\_stop****(4) uint16\_t clock\_sys\_pll\_config\_t::ss\_step****4.2.4 struct clock\_audio\_pll\_config\_t****Data Fields**

- **uint8\_t loopDivider**  
*PLL loop divider.*
- **uint8\_t postDivider**  
*Divider after the PLL, should only be 1, 2, 4, 8, 16.*
- **uint32\_t numerator**  
*30 bit numerator of fractional loop divider.*
- **uint32\_t denominator**  
*30 bit denominator of fractional loop divider*
- **uint8\_t src**  
*Pll clock source, reference \_clock\_pll\_clk\_src.*

**Field Documentation****(1) uint8\_t clock\_audio\_pll\_config\_t::loopDivider**

Valid range for DIV\_SELECT divider value: 27~54.

- (2) `uint8_t clock_audio_pll_config_t::postDivider`
- (3) `uint32_t clock_audio_pll_config_t::numerator`

#### 4.2.5 struct `clock_video_pll_config_t`

##### Data Fields

- `uint8_t loopDivider`  
*PLL loop divider.*
- `uint8_t postDivider`  
*Divider after the PLL, should only be 1, 2, 4, 8, 16.*
- `uint32_t numerator`  
*30 bit numerator of fractional loop divider.*
- `uint32_t denominator`  
*30 bit denominator of fractional loop divider*
- `uint8_t src`  
*Pll clock source, reference \_clock\_pll\_clk\_src.*

##### Field Documentation

- (1) `uint8_t clock_video_pll_config_t::loopDivider`

Valid range for DIV\_SELECT divider value: 27~54.

- (2) `uint8_t clock_video_pll_config_t::postDivider`
- (3) `uint32_t clock_video_pll_config_t::numerator`

#### 4.2.6 struct `clock_enet_pll_config_t`

##### Data Fields

- `bool enableClkOutput`  
*Power on and enable PLL clock output for ENET0 (ref\_enetpll0).*
- `bool enableClkOutput25M`  
*Power on and enable PLL clock output for ENET1 (ref\_enetpll1).*
- `uint8_t loopDivider`  
*Controls the frequency of the ENET0 reference clock.*
- `uint8_t src`  
*Pll clock source, reference \_clock\_pll\_clk\_src.*

**Field Documentation**

- (1) `bool clock_enet_pll_config_t::enableClkOutput`
- (2) `bool clock_enet_pll_config_t::enableClkOutput25M`
- (3) `uint8_t clock_enet_pll_config_t::loopDivider`

b00 25MHz b01 50MHz b10 100MHz (not 50% duty cycle) b11 125MHz

## 4.3 Macro Definition Documentation

### 4.3.1 #define FSL\_SDK\_DISABLE\_DRIVER\_CLOCK\_CONTROL 0

When set to 0, peripheral drivers will enable clock in initialize function and disable clock in de-initialize function. When set to 1, peripheral driver will not control the clock, application could control the clock out of the driver.

Note

All drivers share this feature switcher. If it is set to 1, application should handle clock enable and disable for all drivers.

### 4.3.2 #define FSL\_CLOCK\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 0))

### 4.3.3 #define ADC\_CLOCKS

**Value:**

```
{
    kCLOCK_IpInvalid, kCLOCK_Adc1, kCLOCK_Adc2 \
}
```

### 4.3.4 #define AOI\_CLOCKS

**Value:**

```
{
    kCLOCK_IpInvalid, kCLOCK_Aoi1, kCLOCK_Aoi2 \
}
```

#### 4.3.5 #define BEE\_CLOCKS

**Value:**

```
{  
    kCLOCK_Bee \  
}
```

#### 4.3.6 #define CMP\_CLOCKS

**Value:**

```
{  
    kCLOCK_IpInvalid, kCLOCK_Acmp1, kCLOCK_Acmp2,  
    kCLOCK_Acmp3, kCLOCK_Acmp4 \  
}
```

#### 4.3.7 #define DCDC\_CLOCKS

**Value:**

```
{  
    kCLOCK_Dcdc \  
}
```

#### 4.3.8 #define DCP\_CLOCKS

**Value:**

```
{  
    kCLOCK_Dcp \  
}
```

#### 4.3.9 #define DMAMUX\_CLOCKS

**Value:**

```
{  
    kCLOCK_Dma \  
}
```

#### 4.3.10 #define EDMA\_CLOCKS

**Value:**

```
{  
    kCLOCK_Dma \\\n}
```

#### 4.3.11 #define ENC\_CLOCKS

**Value:**

```
{  
    kCLOCK_IpInvalid, kCLOCK_Enc1, kCLOCK_Enc2,  
    kCLOCK_Enc3, kCLOCK_Enc4 \\  
}
```

#### 4.3.12 #define ENET\_CLOCKS

**Value:**

```
{  
    kCLOCK_Enet \\  
}
```

#### 4.3.13 #define EWM\_CLOCKS

**Value:**

```
{  
    kCLOCK_Ewm0 \\  
}
```

#### 4.3.14 #define FLEXCAN\_CLOCKS

**Value:**

```
{  
    kCLOCK_IpInvalid, kCLOCK_Can1, kCLOCK_Can2,  
    kCLOCK_Can3 \\  
}
```

### 4.3.15 #define FLEXCAN\_PERIPH\_CLOCKS

**Value:**

```
{           \
    kCLOCK_IpInvalid, kCLOCK_Can1S, kCLOCK_Can2S,
    kCLOCK_Can3S \
}
```

### 4.3.16 #define FLEXIO\_CLOCKS

**Value:**

```
{           \
    kCLOCK_IpInvalid, kCLOCK_Flexio1, kCLOCK_Flexio2,
    kCLOCK_Flexio3 \
}
```

### 4.3.17 #define FLEXRAM\_CLOCKS

**Value:**

```
{           \
    kCLOCK_FlexRam \
}
```

### 4.3.18 #define FLEXSPI\_CLOCKS

**Value:**

```
{           \
    kCLOCK_FlexSpi, kCLOCK_IpInvalid, kCLOCK_FlexSpi2 \
}
```

### 4.3.19 #define FLEXSPI\_EXSC\_CLOCKS

**Value:**

```
{           \
    kCLOCK_FlexSpiExsc \
}
```

### 4.3.20 #define GPIO\_CLOCKS

**Value:**

```
{
    kCLOCK_Invalid, kCLOCK_Gpio1, kCLOCK_Gpio2,
    kCLOCK_Gpio3, kCLOCK_Gpio4, kCLOCK_Gpio5 \
}
```

### 4.3.21 #define GPT\_CLOCKS

**Value:**

```
{
    kCLOCK_Invalid, kCLOCK_Gpt1, kCLOCK_Gpt2 \
}
```

### 4.3.22 #define LCDIF\_CLOCKS

**Value:**

```
{
    kCLOCK_Lcd \
}
```

### 4.3.23 #define LCDIF\_PERIPH\_CLOCKS

**Value:**

```
{
    kCLOCK_LcdPixel \
}
```

### 4.3.24 #define LPI2C\_CLOCKS

**Value:**

```
{
    kCLOCK_Invalid, kCLOCK_Lpi2c1, kCLOCK_Lpi2c2,
    kCLOCK_Lpi2c3, kCLOCK_Lpi2c4 \
}
```

#### 4.3.25 #define LPSPI\_CLOCKS

**Value:**

```
{          \
    kCLOCK_IpInvalid, kCLOCK_Lpspi1, kCLOCK_Lpspi2,
    kCLOCK_Lpspi3 \
}
```

#### 4.3.26 #define LPUART\_CLOCKS

**Value:**

```
{          \
    kCLOCK_IpInvalid, kCLOCK_Lpuart1, kCLOCK_Lpuart2,
    kCLOCK_Lpuart3, kCLOCK_Lpuart4, kCLOCK_Lpuart5,
    \          kCLOCK_Lpuart6, kCLOCK_Lpuart7,
    kCLOCK_Lpuart8 \
}
```

#### 4.3.27 #define MQS\_CLOCKS

**Value:**

```
{          \
    kCLOCK_Mqs \
}
```

#### 4.3.28 #define OCRAM\_EXSC\_CLOCKS

**Value:**

```
{          \
    kCLOCK_OcramExsc \
}
```

#### 4.3.29 #define PIT\_CLOCKS

**Value:**

```
{          \
    kCLOCK_Pit \
}
```

### 4.3.30 #define PWM\_CLOCKS

**Value:**

```
{
    {kCLOCK_IpInvalid, kCLOCK_IpInvalid, kCLOCK_IpInvalid, kCLOCK_IpInvalid}, \
        \
    {kCLOCK_Pwm1, kCLOCK_Pwm1, kCLOCK_Pwm1, kCLOCK_Pwm1}, \
        \
    {kCLOCK_Pwm2, kCLOCK_Pwm2, kCLOCK_Pwm2, kCLOCK_Pwm2}, \
        \
    {kCLOCK_Pwm3, kCLOCK_Pwm3, kCLOCK_Pwm3, kCLOCK_Pwm3}, \
        \
    {
        \
        kCLOCK_Pwm4, kCLOCK_Pwm4, \
        kCLOCK_Pwm4, kCLOCK_Pwm4 \
    }
}
```

### 4.3.31 #define PXP\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Pxp \
}
```

### 4.3.32 #define RTWDOG\_CLOCKS

**Value:**

```
{
    \
    kCLOCK_Wdog3 \
}
```

### 4.3.33 #define SAI\_CLOCKS

**Value:**

```
{
    kCLOCK_IpInvalid, kCLOCK_Sai1, kCLOCK_Sai2, \
    kCLOCK_Sai3 \
}
```

#### 4.3.34 #define SEMC\_CLOCKS

**Value:**

```
{  
    kCLOCK_Semc \  
}
```

#### 4.3.35 #define SEMC\_EXSC\_CLOCKS

**Value:**

```
{  
    kCLOCK_SemcExsc \  
}
```

#### 4.3.36 #define TMR\_CLOCKS

**Value:**

```
{  
    kCLOCK_Invalid, kCLOCK_Timer1, kCLOCK_Timer2,  
    kCLOCK_Timer3, kCLOCK_Timer4 \  
}
```

#### 4.3.37 #define TRNG\_CLOCKS

**Value:**

```
{  
    kCLOCK_Trng \  
}
```

#### 4.3.38 #define TSC\_CLOCKS

**Value:**

```
{  
    kCLOCK_Tsc \  
}
```

### 4.3.39 #define WDOG\_CLOCKS

**Value:**

```
{\n    kCLOCK_IpInvalid, kCLOCK_Wdog1, kCLOCK_Wdog2 \n}
```

### 4.3.40 #define USDHC\_CLOCKS

**Value:**

```
{\n    kCLOCK_IpInvalid, kCLOCK_Usdhc1, kCLOCK_Usdhc2 \n}
```

### 4.3.41 #define SPDIF\_CLOCKS

**Value:**

```
{\n    kCLOCK_Spdif \n}
```

### 4.3.42 #define XBARA\_CLOCKS

**Value:**

```
{\n    kCLOCK_IpInvalid, kCLOCK_Xbar1 \n}
```

### 4.3.43 #define XBARB\_CLOCKS

**Value:**

```
{\n    kCLOCK_IpInvalid, kCLOCK_IpInvalid, kCLOCK_Xbar2,\n    kCLOCK_Xbar3 \n}
```

**4.3.44 #define kCLOCK\_CoreSysClk kCLOCK\_CpuClk**

**4.3.45 #define CLOCK\_GetCoreSysClkFreq CLOCK\_GetCpuClkFreq**

## 4.4 Enumeration Type Documentation

### 4.4.1 enum clock\_name\_t

Enumerator

*kCLOCK\_CpuClk* CPU clock.

*kCLOCK\_AhbClk* AHB clock.

*kCLOCK\_SemcClk* SEMC clock.

*kCLOCK\_IpgClk* IPG clock.

*kCLOCK\_PerClk* PER clock.

*kCLOCK\_OscClk* OSC clock selected by PMU\_LOWPWR\_CTRL[OSC\_SEL].

*kCLOCK\_RtcClk* RTC clock. (RTCKLK)

*kCLOCK\_ArmPllClk* ARMPLLCLK.

*kCLOCK\_Usb1PllClk* USB1PLLCLK.

*kCLOCK\_Usb1PllPfd0Clk* USB1PLLPFD0CLK.

*kCLOCK\_Usb1PllPfd1Clk* USB1PLLPFD1CLK.

*kCLOCK\_Usb1PllPfd2Clk* USB1PLLPFD2CLK.

*kCLOCK\_Usb1PllPfd3Clk* USB1PLLPFD3CLK.

*kCLOCK\_Usb1SwClk* USB1PLLSWCLK.

*kCLOCK\_Usb1Sw120MClk* USB1PLLSw120MCLK.

*kCLOCK\_Usb1Sw60MClk* USB1PLLSw60MCLK.

*kCLOCK\_Usb1Sw80MClk* USB1PLLSw80MCLK.

*kCLOCK\_Usb2PllClk* USB2PLLCLK.

*kCLOCK\_SysPllClk* SYSPLLCLK.

*kCLOCK\_SysPllPfd0Clk* SYSPLLPFD0CLK.

*kCLOCK\_SysPllPfd1Clk* SYSPLLPFD1CLK.

*kCLOCK\_SysPllPfd2Clk* SYSPLLPFD2CLK.

*kCLOCK\_SysPllPfd3Clk* SYSPLLPFD3CLK.

*kCLOCK\_EnetPll0Clk* Enet PLLCLK ref\_enetpll0.

*kCLOCK\_EnetPll1Clk* Enet PLLCLK ref\_enetpll1.

*kCLOCK\_AudioPllClk* Audio PLLCLK.

*kCLOCK\_VideoPllClk* Video PLLCLK.

*kCLOCK\_NoneName* None Clock Name.

### 4.4.2 enum clock\_ip\_name\_t

Enumerator

*kCLOCK\_Aips\_tz1* CCGR0, CG0.

*kCLOCK\_Aips\_tz2* CCGR0, CG1.  
*kCLOCK\_Mqs* CCGR0, CG2.  
*kCLOCK\_FlexSpiExsc* CCGR0, CG3.  
*kCLOCK\_Sim\_M\_Main* CCGR0, CG4.  
*kCLOCK\_Dcp* CCGR0, CG5.  
*kCLOCK\_Lpuart3* CCGR0, CG6.  
*kCLOCK\_Can1* CCGR0, CG7.  
*kCLOCK\_Can1S* CCGR0, CG8.  
*kCLOCK\_Can2* CCGR0, CG9.  
*kCLOCK\_Can2S* CCGR0, CG10.  
*kCLOCK\_Trace* CCGR0, CG11.  
*kCLOCK\_Gpt2* CCGR0, CG12.  
*kCLOCK\_Gpt2S* CCGR0, CG13.  
*kCLOCK\_Lpuart2* CCGR0, CG14.  
*kCLOCK\_Gpio2* CCGR0, CG15.  
*kCLOCK\_Lpspi1* CCGR1, CG0.  
*kCLOCK\_Lpspi2* CCGR1, CG1.  
*kCLOCK\_Lpspi3* CCGR1, CG3.  
*kCLOCK\_Adc2* CCGR1, CG4.  
*kCLOCK\_Enet* CCGR1, CG5.  
*kCLOCK\_Pit* CCGR1, CG6.  
*kCLOCK\_Aoi2* CCGR1, CG7.  
*kCLOCK\_Adc1* CCGR1, CG8.  
*kCLOCK\_SemcExsc* CCGR1, CG9.  
*kCLOCK\_Gpt1* CCGR1, CG10.  
*kCLOCK\_Gpt1S* CCGR1, CG11.  
*kCLOCK\_Lpuart4* CCGR1, CG12.  
*kCLOCK\_Gpio1* CCGR1, CG13.  
*kCLOCK\_Csu* CCGR1, CG14.  
*kCLOCK\_Gpio5* CCGR1, CG15.  
*kCLOCK\_OcramExsc* CCGR2, CG0.  
*kCLOCK\_IomuxcSnvs* CCGR2, CG2.  
*kCLOCK\_Lpi2c1* CCGR2, CG3.  
*kCLOCK\_Lpi2c2* CCGR2, CG4.  
*kCLOCK\_Lpi2c3* CCGR2, CG5.  
*kCLOCK\_Ocotp* CCGR2, CG6.  
*kCLOCK\_Xbar3* CCGR2, CG7.  
*kCLOCK\_Ipmux1* CCGR2, CG8.  
*kCLOCK\_Ipmux2* CCGR2, CG9.  
*kCLOCK\_Ipmux3* CCGR2, CG10.  
*kCLOCK\_Xbar1* CCGR2, CG11.  
*kCLOCK\_Xbar2* CCGR2, CG12.  
*kCLOCK\_Gpio3* CCGR2, CG13.  
*kCLOCK\_Lcd* CCGR2, CG14.  
*kCLOCK\_Pxp* CCGR2, CG15.

*kCLOCK\_Flexio2* CCGR3, CG0.  
*kCLOCK\_Lpuart5* CCGR3, CG1.  
*kCLOCK\_Semc* CCGR3, CG2.  
*kCLOCK\_Lpuart6* CCGR3, CG3.  
*kCLOCK\_Aoi1* CCGR3, CG4.  
*kCLOCK\_LcdPixel* CCGR3, CG5.  
*kCLOCK\_Gpio4* CCGR3, CG6.  
*kCLOCK\_Ewm0* CCGR3, CG7.  
*kCLOCK\_Wdog1* CCGR3, CG8.  
*kCLOCK\_FlexRam* CCGR3, CG9.  
*kCLOCK\_Acmp1* CCGR3, CG10.  
*kCLOCK\_Acmp2* CCGR3, CG11.  
*kCLOCK\_Acmp3* CCGR3, CG12.  
*kCLOCK\_Acmp4* CCGR3, CG13.  
*kCLOCK\_Ocram* CCGR3, CG14.  
*kCLOCK\_IomuxcSnvsGpr* CCGR3, CG15.  
*kCLOCK\_Sim\_m7\_clk\_r* CCGR4, CG0.  
*kCLOCK\_Iomuxc* CCGR4, CG1.  
*kCLOCK\_IomuxcGpr* CCGR4, CG2.  
*kCLOCK\_Bee* CCGR4, CG3.  
*kCLOCK\_SimM7* CCGR4, CG4.  
*kCLOCK\_Tsc* CCGR4, CG5.  
*kCLOCK\_SimM* CCGR4, CG6.  
*kCLOCK\_SimEms* CCGR4, CG7.  
*kCLOCK\_Pwm1* CCGR4, CG8.  
*kCLOCK\_Pwm2* CCGR4, CG9.  
*kCLOCK\_Pwm3* CCGR4, CG10.  
*kCLOCK\_Pwm4* CCGR4, CG11.  
*kCLOCK\_Enc1* CCGR4, CG12.  
*kCLOCK\_Enc2* CCGR4, CG13.  
*kCLOCK\_Enc3* CCGR4, CG14.  
*kCLOCK\_Enc4* CCGR4, CG15.  
*kCLOCK\_Rom* CCGR5, CG0.  
*kCLOCK\_Flexio1* CCGR5, CG1.  
*kCLOCK\_Wdog3* CCGR5, CG2.  
*kCLOCK\_Dma* CCGR5, CG3.  
*kCLOCK\_Wdog2* CCGR5, CG5.  
*kCLOCK\_Aips\_tz4* CCGR5, CG6.  
*kCLOCK\_Spdif* CCGR5, CG7.  
*kCLOCK\_SimMain* CCGR5, CG8.  
*kCLOCK\_Sai1* CCGR5, CG9.  
*kCLOCK\_Sai2* CCGR5, CG10.  
*kCLOCK\_Sai3* CCGR5, CG11.  
*kCLOCK\_Lpuart1* CCGR5, CG12.  
*kCLOCK\_Lpuart7* CCGR5, CG13.

*kCLOCK\_SnvsHp* CCGR5, CG14.  
*kCLOCK\_SnvsLp* CCGR5, CG15.  
*kCLOCK\_UsbOh3* CCGR6, CG0.  
*kCLOCK\_Usdhc1* CCGR6, CG1.  
*kCLOCK\_Usdhc2* CCGR6, CG2.  
*kCLOCK\_Dcdc* CCGR6, CG3.  
*kCLOCK\_Ipmux4* CCGR6, CG4.  
*kCLOCK\_FlexSpi* CCGR6, CG5.  
*kCLOCK\_Trng* CCGR6, CG6.  
*kCLOCK\_Lpuart8* CCGR6, CG7.  
*kCLOCK\_Timer4* CCGR6, CG8.  
*kCLOCK\_Aips\_tz3* CCGR6, CG9.  
*kCLOCK\_SimPer* CCGR6, CG10.  
*kCLOCK\_Anadig* CCGR6, CG11.  
*kCLOCK\_Lpi2c4* CCGR6, CG12.  
*kCLOCK\_Timer1* CCGR6, CG13.  
*kCLOCK\_Timer2* CCGR6, CG14.  
*kCLOCK\_Timer3* CCGR6, CG15.  
*kCLOCK\_FlexSpi2* CCGR7, CG1.  
*kCLOCK\_Axbs\_l* CCGR7, CG2.  
*kCLOCK\_Can3* CCGR7, CG3.  
*kCLOCK\_Can3S* CCGR7, CG4.  
*kCLOCK\_Aips\_lite* CCGR7, CG5.  
*kCLOCK\_Flexio3* CCGR7, CG6.

#### 4.4.3 enum clock\_osc\_t

Enumerator

*kCLOCK\_RcOsc* On chip OSC.  
*kCLOCK\_XtalOsc* 24M Xtal OSC

#### 4.4.4 enum clock\_gate\_value\_t

Enumerator

*kCLOCK\_ClockNotNeeded* Clock is off during all modes.  
*kCLOCK\_ClockNeededRun* Clock is on in run mode, but off in WAIT and STOP modes.  
*kCLOCK\_ClockNeededRunWait* Clock is on during all modes, except STOP mode.

#### 4.4.5 enum clock\_mode\_t

Enumerator

- kCLOCK\_ModeRun*** Remain in run mode.
- kCLOCK\_ModeWait*** Transfer to wait mode.
- kCLOCK\_ModeStop*** Transfer to stop mode.

#### 4.4.6 enum clock\_mux\_t

These constants define the mux control names for clock mux setting.

- 0:7: REG offset to CCM\_BASE in bytes.
- 8:15: Root clock setting bit field shift.
- 16:31: Root clock setting bit field width.

Enumerator

- kCLOCK\_Pl3SwMux*** pll3\_sw\_clk mux name
- kCLOCK\_PeriphMux*** periph mux name
- kCLOCK\_SemcAltMux*** semc mux name
- kCLOCK\_SemcMux*** semc mux name
- kCLOCK\_PrePeriphMux*** pre-periph mux name
- kCLOCK\_TraceMux*** trace mux name
- kCLOCK\_PeriphClk2Mux*** periph clock2 mux name
- kCLOCK\_Flexspi2Mux*** flexspi2 mux name
- kCLOCK\_LpSpiMux*** lpspi mux name
- kCLOCK\_FlexspiMux*** flexspi mux name
- kCLOCK\_Usdhc2Mux*** usdhc2 mux name
- kCLOCK\_Usdhc1Mux*** usdhc1 mux name
- kCLOCK\_Sai3Mux*** sai3 mux name
- kCLOCK\_Sai2Mux*** sai2 mux name
- kCLOCK\_Sai1Mux*** sai1 mux name
- kCLOCK\_PerclkMux*** perclk mux name
- kCLOCK\_Flexio2Mux*** flexio2 mux name
- kCLOCK\_CanMux*** can mux name
- kCLOCK\_UartMux*** uart mux name
- kCLOCK\_SpdifMux*** spdif mux name
- kCLOCK\_Flexio1Mux*** flexio1 mux name
- kCLOCK\_Lpi2cMux*** lpi2c mux name
- kCLOCK\_LcdifPreMux*** lcdif pre mux name

#### 4.4.7 enum clock\_div\_value\_t

Enumerator

*kCLOCK\_ArmDivBy1* ARM clock divider set to divided by 1.  
*kCLOCK\_ArmDivBy2* ARM clock divider set to divided by 2.  
*kCLOCK\_ArmDivBy3* ARM clock divider set to divided by 3.  
*kCLOCK\_ArmDivBy4* ARM clock divider set to divided by 4.  
*kCLOCK\_ArmDivBy5* ARM clock divider set to divided by 5.  
*kCLOCK\_ArmDivBy6* ARM clock divider set to divided by 6.  
*kCLOCK\_ArmDivBy7* ARM clock divider set to divided by 7.  
*kCLOCK\_ArmDivBy8* ARM clock divider set to divided by 8.  
*kCLOCK\_PерiphClk2DivBy1* PeriphClk2 divider set to divided by 1.  
*kCLOCK\_PерiphClk2DivBy2* PeriphClk2 divider set to divided by 2.  
*kCLOCK\_PерiphClk2DivBy3* PeriphClk2 divider set to divided by 3.  
*kCLOCK\_PерiphClk2DivBy4* PeriphClk2 divider set to divided by 4.  
*kCLOCK\_PерiphClk2DivBy5* PeriphClk2 divider set to divided by 5.  
*kCLOCK\_PерiphClk2DivBy6* PeriphClk2 divider set to divided by 6.  
*kCLOCK\_PерiphClk2DivBy7* PeriphClk2 divider set to divided by 7.  
*kCLOCK\_PерiphClk2DivBy8* PeriphClk2 divider set to divided by 8.  
*kCLOCK\_SemcDivBy1* SEMC clock divider set to divided by 1.  
*kCLOCK\_SemcDivBy2* SEMC clock divider set to divided by 2.  
*kCLOCK\_SemcDivBy3* SEMC clock divider set to divided by 3.  
*kCLOCK\_SemcDivBy4* SEMC clock divider set to divided by 4.  
*kCLOCK\_SemcDivBy5* SEMC clock divider set to divided by 5.  
*kCLOCK\_SemcDivBy6* SEMC clock divider set to divided by 6.  
*kCLOCK\_SemcDivBy7* SEMC clock divider set to divided by 7.  
*kCLOCK\_SemcDivBy8* SEMC clock divider set to divided by 8.  
*kCLOCK\_AhbDivBy1* AHB clock divider set to divided by 1.  
*kCLOCK\_AhbDivBy2* AHB clock divider set to divided by 2.  
*kCLOCK\_AhbDivBy3* AHB clock divider set to divided by 3.  
*kCLOCK\_AhbDivBy4* AHB clock divider set to divided by 4.  
*kCLOCK\_AhbDivBy5* AHB clock divider set to divided by 5.  
*kCLOCK\_AhbDivBy6* AHB clock divider set to divided by 6.  
*kCLOCK\_AhbDivBy7* AHB clock divider set to divided by 7.  
*kCLOCK\_AhbDivBy8* AHB clock divider set to divided by 8.  
*kCLOCK\_IpgDivBy1* IPG clock divider set to divided by 1.  
*kCLOCK\_IpgDivBy2* IPG clock divider set to divided by 2.  
*kCLOCK\_IpgDivBy3* IPG clock divider set to divided by 3.  
*kCLOCK\_IpgDivBy4* IPG clock divider set to divided by 4.  
*kCLOCK\_Flexspi2DivBy1* Flexspi2 divider set to divided by 1.  
*kCLOCK\_Flexspi2DivBy2* Flexspi2 divider set to divided by 2.  
*kCLOCK\_Flexspi2DivBy3* Flexspi2 divider set to divided by 3.  
*kCLOCK\_Flexspi2DivBy4* Flexspi2 divider set to divided by 4.  
*kCLOCK\_Flexspi2DivBy5* Flexspi2 divider set to divided by 5.

***kCLOCK\_Flexspi2DivBy6*** Flexspi2 divider set to divided by 6.  
***kCLOCK\_Flexspi2DivBy7*** Flexspi2 divider set to divided by 7.  
***kCLOCK\_Flexspi2DivBy8*** Flexspi2 divider set to divided by 8.  
***kCLOCK\_LpspiDivBy1*** Lpspi divider set to divided by 1.  
***kCLOCK\_LpspiDivBy2*** Lpspi divider set to divided by 2.  
***kCLOCK\_LpspiDivBy3*** Lpspi divider set to divided by 3.  
***kCLOCK\_LpspiDivBy4*** Lpspi divider set to divided by 4.  
***kCLOCK\_LpspiDivBy5*** Lpspi divider set to divided by 5.  
***kCLOCK\_LpspiDivBy6*** Lpspi divider set to divided by 6.  
***kCLOCK\_LpspiDivBy7*** Lpspi divider set to divided by 7.  
***kCLOCK\_LpspiDivBy8*** Lpspi divider set to divided by 8.  
***kCLOCK\_LcdifDivBy1*** Lcdif divider set to divided by 1.  
***kCLOCK\_LcdifDivBy2*** Lcdif divider set to divided by 2.  
***kCLOCK\_LcdifDivBy3*** Lcdif divider set to divided by 3.  
***kCLOCK\_LcdifDivBy4*** Lcdif divider set to divided by 4.  
***kCLOCK\_LcdifDivBy5*** Lcdif divider set to divided by 5.  
***kCLOCK\_LcdifDivBy6*** Lcdif divider set to divided by 6.  
***kCLOCK\_LcdifDivBy7*** Lcdif divider set to divided by 7.  
***kCLOCK\_LcdifDivBy8*** Lcdif divider set to divided by 8.  
***kCLOCK\_FlexspiDivBy1*** Flexspi divider set to divided by 1.  
***kCLOCK\_FlexspiDivBy2*** Flexspi divider set to divided by 2.  
***kCLOCK\_FlexspiDivBy3*** Flexspi divider set to divided by 3.  
***kCLOCK\_FlexspiDivBy4*** Flexspi divider set to divided by 4.  
***kCLOCK\_FlexspiDivBy5*** Flexspi divider set to divided by 5.  
***kCLOCK\_FlexspiDivBy6*** Flexspi divider set to divided by 6.  
***kCLOCK\_FlexspiDivBy7*** Flexspi divider set to divided by 7.  
***kCLOCK\_FlexspiDivBy8*** Flexspi divider set to divided by 8.  
***kCLOCK\_TraceDivBy1*** Trace divider set to divided by 1.  
***kCLOCK\_TraceDivBy2*** Trace divider set to divided by 2.  
***kCLOCK\_TraceDivBy3*** Trace divider set to divided by 3.  
***kCLOCK\_TraceDivBy4*** Trace divider set to divided by 4.  
***kCLOCK\_Usdhc2DivBy1*** Usdhc2 divider set to divided by 1.  
***kCLOCK\_Usdhc2DivBy2*** Usdhc2 divider set to divided by 2.  
***kCLOCK\_Usdhc2DivBy3*** Usdhc2 divider set to divided by 3.  
***kCLOCK\_Usdhc2DivBy4*** Usdhc2 divider set to divided by 4.  
***kCLOCK\_Usdhc2DivBy5*** Usdhc2 divider set to divided by 5.  
***kCLOCK\_Usdhc2DivBy6*** Usdhc2 divider set to divided by 6.  
***kCLOCK\_Usdhc2DivBy7*** Usdhc2 divider set to divided by 7.  
***kCLOCK\_Usdhc2DivBy8*** Usdhc2 divider set to divided by 8.  
***kCLOCK\_Usdhc1DivBy1*** Usdhc1 divider set to divided by 1.  
***kCLOCK\_Usdhc1DivBy2*** Usdhc1 divider set to divided by 2.  
***kCLOCK\_Usdhc1DivBy3*** Usdhc1 divider set to divided by 3.  
***kCLOCK\_Usdhc1DivBy4*** Usdhc1 divider set to divided by 4.  
***kCLOCK\_Usdhc1DivBy5*** Usdhc1 divider set to divided by 5.  
***kCLOCK\_Usdhc1DivBy6*** Usdhc1 divider set to divided by 6.

|                                |                                         |
|--------------------------------|-----------------------------------------|
| <i>kCLOCK_Usdhc1DivBy7</i>     | Usdhc1 divider set to divided by 7.     |
| <i>kCLOCK_Usdhc1DivBy8</i>     | Usdhc1 divider set to divided by 8.     |
| <i>kCLOCK_Flexio2DivBy1</i>    | Flexio2 divider set to divided by 1.    |
| <i>kCLOCK_Flexio2DivBy2</i>    | Flexio2 divider set to divided by 2.    |
| <i>kCLOCK_Flexio2DivBy3</i>    | Flexio2 divider set to divided by 3.    |
| <i>kCLOCK_Flexio2DivBy4</i>    | Flexio2 divider set to divided by 4.    |
| <i>kCLOCK_Flexio2DivBy5</i>    | Flexio2 divider set to divided by 5.    |
| <i>kCLOCK_Flexio2DivBy6</i>    | Flexio2 divider set to divided by 6.    |
| <i>kCLOCK_Flexio2DivBy7</i>    | Flexio2 divider set to divided by 7.    |
| <i>kCLOCK_Flexio2DivBy8</i>    | Flexio2 divider set to divided by 8.    |
| <i>kCLOCK_Sai3PreDivBy1</i>    | Sai3Pre divider set to divided by 1.    |
| <i>kCLOCK_Sai3PreDivBy2</i>    | Sai3Pre divider set to divided by 2.    |
| <i>kCLOCK_Sai3PreDivBy3</i>    | Sai3Pre divider set to divided by 3.    |
| <i>kCLOCK_Sai3PreDivBy4</i>    | Sai3Pre divider set to divided by 4.    |
| <i>kCLOCK_Sai3PreDivBy5</i>    | Sai3Pre divider set to divided by 5.    |
| <i>kCLOCK_Sai3PreDivBy6</i>    | Sai3Pre divider set to divided by 6.    |
| <i>kCLOCK_Sai3PreDivBy7</i>    | Sai3Pre divider set to divided by 7.    |
| <i>kCLOCK_Sai3PreDivBy8</i>    | Sai3Pre divider set to divided by 8.    |
| <i>kCLOCK_Flexio2PreDivBy1</i> | Flexio2Pre divider set to divided by 1. |
| <i>kCLOCK_Flexio2PreDivBy2</i> | Flexio2Pre divider set to divided by 2. |
| <i>kCLOCK_Flexio2PreDivBy3</i> | Flexio2Pre divider set to divided by 3. |
| <i>kCLOCK_Flexio2PreDivBy4</i> | Flexio2Pre divider set to divided by 4. |
| <i>kCLOCK_Flexio2PreDivBy5</i> | Flexio2Pre divider set to divided by 5. |
| <i>kCLOCK_Flexio2PreDivBy6</i> | Flexio2Pre divider set to divided by 6. |
| <i>kCLOCK_Flexio2PreDivBy7</i> | Flexio2Pre divider set to divided by 7. |
| <i>kCLOCK_Flexio2PreDivBy8</i> | Flexio2Pre divider set to divided by 8. |
| <i>kCLOCK_Sai1PreDivBy1</i>    | Sai1Pre divider set to divided by 1.    |
| <i>kCLOCK_Sai1PreDivBy2</i>    | Sai1Pre divider set to divided by 2.    |
| <i>kCLOCK_Sai1PreDivBy3</i>    | Sai1Pre divider set to divided by 3.    |
| <i>kCLOCK_Sai1PreDivBy4</i>    | Sai1Pre divider set to divided by 4.    |
| <i>kCLOCK_Sai1PreDivBy5</i>    | Sai1Pre divider set to divided by 5.    |
| <i>kCLOCK_Sai1PreDivBy6</i>    | Sai1Pre divider set to divided by 6.    |
| <i>kCLOCK_Sai1PreDivBy7</i>    | Sai1Pre divider set to divided by 7.    |
| <i>kCLOCK_Sai1PreDivBy8</i>    | Sai1Pre divider set to divided by 8.    |
| <i>kCLOCK_Sai2PreDivBy1</i>    | Sai2Pre divider set to divided by 1.    |
| <i>kCLOCK_Sai2PreDivBy2</i>    | Sai2Pre divider set to divided by 2.    |
| <i>kCLOCK_Sai2PreDivBy3</i>    | Sai2Pre divider set to divided by 3.    |
| <i>kCLOCK_Sai2PreDivBy4</i>    | Sai2Pre divider set to divided by 4.    |
| <i>kCLOCK_Sai2PreDivBy5</i>    | Sai2Pre divider set to divided by 5.    |
| <i>kCLOCK_Sai2PreDivBy6</i>    | Sai2Pre divider set to divided by 6.    |
| <i>kCLOCK_Sai2PreDivBy7</i>    | Sai2Pre divider set to divided by 7.    |
| <i>kCLOCK_Sai2PreDivBy8</i>    | Sai2Pre divider set to divided by 8.    |
| <i>kCLOCK_Spdif0PreDivBy1</i>  | Spdif0Pre divider set to divided by 1.  |
| <i>kCLOCK_Spdif0PreDivBy2</i>  | Spdif0Pre divider set to divided by 2.  |
| <i>kCLOCK_Spdif0PreDivBy3</i>  | Spdif0Pre divider set to divided by 3.  |

- kCLOCK\_Spdif0PreDivBy4*** Spdif0Pre divider set to divided by 4.
- kCLOCK\_Spdif0PreDivBy5*** Spdif0Pre divider set to divided by 5.
- kCLOCK\_Spdif0PreDivBy6*** Spdif0Pre divider set to divided by 6.
- kCLOCK\_Spdif0PreDivBy7*** Spdif0Pre divider set to divided by 7.
- kCLOCK\_Spdif0PreDivBy8*** Spdif0Pre divider set to divided by 8.
- kCLOCK\_Spdif0DivBy1*** Spdif0 divider set to divided by 1.
- kCLOCK\_Spdif0DivBy2*** Spdif0 divider set to divided by 2.
- kCLOCK\_Spdif0DivBy3*** Spdif0 divider set to divided by 3.
- kCLOCK\_Spdif0DivBy4*** Spdif0 divider set to divided by 4.
- kCLOCK\_Spdif0DivBy5*** Spdif0 divider set to divided by 5.
- kCLOCK\_Spdif0DivBy6*** Spdif0 divider set to divided by 6.
- kCLOCK\_Spdif0DivBy7*** Spdif0 divider set to divided by 7.
- kCLOCK\_Spdif0DivBy8*** Spdif0 divider set to divided by 8.
- kCLOCK\_Flexio1PreDivBy1*** Flexio1Pre divider set to divided by 1.
- kCLOCK\_Flexio1PreDivBy2*** Flexio1Pre divider set to divided by 2.
- kCLOCK\_Flexio1PreDivBy3*** Flexio1Pre divider set to divided by 3.
- kCLOCK\_Flexio1PreDivBy4*** Flexio1Pre divider set to divided by 4.
- kCLOCK\_Flexio1DivBy1*** Flexio1 divider set to divided by 1.
- kCLOCK\_Flexio1DivBy2*** Flexio1 divider set to divided by 2.
- kCLOCK\_Flexio1DivBy3*** Flexio1 divider set to divided by 3.
- kCLOCK\_Flexio1DivBy4*** Flexio1 divider set to divided by 4.
- kCLOCK\_Flexio1DivBy5*** Flexio1 divider set to divided by 5.
- kCLOCK\_Flexio1DivBy6*** Flexio1 divider set to divided by 6.
- kCLOCK\_Flexio1DivBy7*** Flexio1 divider set to divided by 7.
- kCLOCK\_Flexio1DivBy8*** Flexio1 divider set to divided by 8.
- kCLOCK\_LcdifPreDivBy1*** LcdifPre divider set to divided by 1.
- kCLOCK\_LcdifPreDivBy2*** LcdifPre divider set to divided by 2.
- kCLOCK\_LcdifPreDivBy3*** LcdifPre divider set to divided by 3.
- kCLOCK\_LcdifPreDivBy4*** LcdifPre divider set to divided by 4.
- kCLOCK\_LcdifPreDivBy5*** LcdifPre divider set to divided by 5.
- kCLOCK\_LcdifPreDivBy6*** LcdifPre divider set to divided by 6.
- kCLOCK\_LcdifPreDivBy7*** LcdifPre divider set to divided by 7.
- kCLOCK\_LcdifPreDivBy8*** LcdifPre divider set to divided by 8.
- kCLOCK\_MiscDivBy1*** Misc divider like LPI2C set to divided by 1 .
- kCLOCK\_MiscDivBy2*** Misc divider like LPI2C set to divided by 2 .
- kCLOCK\_MiscDivBy3*** Misc divider like LPI2C set to divided by 3 .
- kCLOCK\_MiscDivBy4*** Misc divider like LPI2C set to divided by 4 .
- kCLOCK\_MiscDivBy5*** Misc divider like LPI2C set to divided by 5 .
- kCLOCK\_MiscDivBy6*** Misc divider like LPI2C set to divided by 6 .
- kCLOCK\_MiscDivBy7*** Misc divider like LPI2C set to divided by 7 .
- kCLOCK\_MiscDivBy8*** Misc divider like LPI2C set to divided by 8 .
- kCLOCK\_MiscDivBy9*** Misc divider like LPI2C set to divided by 9 .
- kCLOCK\_MiscDivBy10*** Misc divider like LPI2C set to divided by 10.
- kCLOCK\_MiscDivBy11*** Misc divider like LPI2C set to divided by 11.
- kCLOCK\_MiscDivBy12*** Misc divider like LPI2C set to divided by 12.

|                                 |                                               |
|---------------------------------|-----------------------------------------------|
| <code>kCLOCK_MiscDivBy13</code> | Misc divider like LPI2C set to divided by 13. |
| <code>kCLOCK_MiscDivBy14</code> | Misc divider like LPI2C set to divided by 14. |
| <code>kCLOCK_MiscDivBy15</code> | Misc divider like LPI2C set to divided by 15. |
| <code>kCLOCK_MiscDivBy16</code> | Misc divider like LPI2C set to divided by 16. |
| <code>kCLOCK_MiscDivBy17</code> | Misc divider like LPI2C set to divided by 17. |
| <code>kCLOCK_MiscDivBy18</code> | Misc divider like LPI2C set to divided by 18. |
| <code>kCLOCK_MiscDivBy19</code> | Misc divider like LPI2C set to divided by 19. |
| <code>kCLOCK_MiscDivBy20</code> | Misc divider like LPI2C set to divided by 20. |
| <code>kCLOCK_MiscDivBy21</code> | Misc divider like LPI2C set to divided by 21. |
| <code>kCLOCK_MiscDivBy22</code> | Misc divider like LPI2C set to divided by 22. |
| <code>kCLOCK_MiscDivBy23</code> | Misc divider like LPI2C set to divided by 23. |
| <code>kCLOCK_MiscDivBy24</code> | Misc divider like LPI2C set to divided by 24. |
| <code>kCLOCK_MiscDivBy25</code> | Misc divider like LPI2C set to divided by 25. |
| <code>kCLOCK_MiscDivBy26</code> | Misc divider like LPI2C set to divided by 26. |
| <code>kCLOCK_MiscDivBy27</code> | Misc divider like LPI2C set to divided by 27. |
| <code>kCLOCK_MiscDivBy28</code> | Misc divider like LPI2C set to divided by 28. |
| <code>kCLOCK_MiscDivBy29</code> | Misc divider like LPI2C set to divided by 29. |
| <code>kCLOCK_MiscDivBy30</code> | Misc divider like LPI2C set to divided by 30. |
| <code>kCLOCK_MiscDivBy31</code> | Misc divider like LPI2C set to divided by 31. |
| <code>kCLOCK_MiscDivBy32</code> | Misc divider like LPI2C set to divided by 32. |
| <code>kCLOCK_MiscDivBy33</code> | Misc divider like LPI2C set to divided by 33. |
| <code>kCLOCK_MiscDivBy34</code> | Misc divider like LPI2C set to divided by 34. |
| <code>kCLOCK_MiscDivBy35</code> | Misc divider like LPI2C set to divided by 35. |
| <code>kCLOCK_MiscDivBy36</code> | Misc divider like LPI2C set to divided by 36. |
| <code>kCLOCK_MiscDivBy37</code> | Misc divider like LPI2C set to divided by 37. |
| <code>kCLOCK_MiscDivBy38</code> | Misc divider like LPI2C set to divided by 38. |
| <code>kCLOCK_MiscDivBy39</code> | Misc divider like LPI2C set to divided by 39. |
| <code>kCLOCK_MiscDivBy40</code> | Misc divider like LPI2C set to divided by 40. |
| <code>kCLOCK_MiscDivBy41</code> | Misc divider like LPI2C set to divided by 41. |
| <code>kCLOCK_MiscDivBy42</code> | Misc divider like LPI2C set to divided by 42. |
| <code>kCLOCK_MiscDivBy43</code> | Misc divider like LPI2C set to divided by 43. |
| <code>kCLOCK_MiscDivBy44</code> | Misc divider like LPI2C set to divided by 44. |
| <code>kCLOCK_MiscDivBy45</code> | Misc divider like LPI2C set to divided by 45. |
| <code>kCLOCK_MiscDivBy46</code> | Misc divider like LPI2C set to divided by 46. |
| <code>kCLOCK_MiscDivBy47</code> | Misc divider like LPI2C set to divided by 47. |
| <code>kCLOCK_MiscDivBy48</code> | Misc divider like LPI2C set to divided by 48. |
| <code>kCLOCK_MiscDivBy49</code> | Misc divider like LPI2C set to divided by 49. |
| <code>kCLOCK_MiscDivBy50</code> | Misc divider like LPI2C set to divided by 50. |
| <code>kCLOCK_MiscDivBy51</code> | Misc divider like LPI2C set to divided by 51. |
| <code>kCLOCK_MiscDivBy52</code> | Misc divider like LPI2C set to divided by 52. |
| <code>kCLOCK_MiscDivBy53</code> | Misc divider like LPI2C set to divided by 53. |
| <code>kCLOCK_MiscDivBy54</code> | Misc divider like LPI2C set to divided by 54. |
| <code>kCLOCK_MiscDivBy55</code> | Misc divider like LPI2C set to divided by 55. |
| <code>kCLOCK_MiscDivBy56</code> | Misc divider like LPI2C set to divided by 56. |
| <code>kCLOCK_MiscDivBy57</code> | Misc divider like LPI2C set to divided by 57. |

- kCLOCK\_MiscDivBy58* Misc divider like LPI2C set to divided by 58.  
*kCLOCK\_MiscDivBy59* Misc divider like LPI2C set to divided by 59.  
*kCLOCK\_MiscDivBy60* Misc divider like LPI2C set to divided by 60.  
*kCLOCK\_MiscDivBy61* Misc divider like LPI2C set to divided by 61.  
*kCLOCK\_MiscDivBy62* Misc divider like LPI2C set to divided by 62.  
*kCLOCK\_MiscDivBy63* Misc divider like LPI2C set to divided by 63.  
*kCLOCK\_MiscDivBy64* Misc divider like LPI2C set to divided by 64.

#### 4.4.8 enum clock\_div\_t

These constants define div control names for clock div setting.

- 0:7: REG offset to CCM\_BASE in bytes.
- 8:15: Root clock setting bit field shift.
- 16:31: Root clock setting bit field width.

Enumerator

- kCLOCK\_ArmDiv* core div name  
*kCLOCK\_PeriphClk2Div* periph clock2 div name  
*kCLOCK\_SemcDiv* semc div name  
*kCLOCK\_AhbDiv* ahb div name  
*kCLOCK\_IpgDiv* ipg div name  
*kCLOCK\_Flexspi2Div* flexspi2 div name  
*kCLOCK\_LpspiDiv* lpspi div name  
*kCLOCK\_LcdifDiv* lcdif div name  
*kCLOCK\_FlexspiDiv* flexspi div name  
*kCLOCK\_PerclkDiv* perclk div name  
*kCLOCK\_CanDiv* can div name  
*kCLOCK\_TraceDiv* trace div name  
*kCLOCK\_Usdhc2Div* usdhc2 div name  
*kCLOCK\_Usdhc1Div* usdhc1 div name  
*kCLOCK\_UartDiv* uart div name  
*kCLOCK\_Flexio2Div* flexio2 pre div name  
*kCLOCK\_Sai3PreDiv* sai3 pre div name  
*kCLOCK\_Sai3Div* sai3 div name  
*kCLOCK\_Flexio2PreDiv* sai3 pre div name  
*kCLOCK\_Sai1PreDiv* sai1 pre div name  
*kCLOCK\_Sai1Div* sai1 div name  
*kCLOCK\_Sai2PreDiv* sai2 pre div name  
*kCLOCK\_Sai2Div* sai2 div name  
*kCLOCK\_Spdif0PreDiv* spdif pre div name  
*kCLOCK\_Spdif0Div* spdif div name  
*kCLOCK\_Flexio1PreDiv* flexio1 pre div name

*kCLOCK\_Flexio1Div* flexio1 div name  
*kCLOCK\_Lpi2cDiv* lpi2c div name  
*kCLOCK\_LcdifPreDiv* lcdif pre div name  
*kCLOCK\_NonePreDiv* None Pre div.

#### 4.4.9 enum clock\_usb\_src\_t

Enumerator

*kCLOCK\_Usb480M* Use 480M.  
*kCLOCK\_UsbSrcUnused* Used when the function does not care the clock source.

#### 4.4.10 enum clock\_usb\_phy\_src\_t

Enumerator

*kCLOCK\_Usbphy480M* Use 480M.

#### 4.4.11 enum \_clock\_pll\_clk\_src

Enumerator

*kCLOCK\_PllClkSrc24M* Pll clock source 24M.  
*kCLOCK\_PllSrcClkPN* Pll clock source CLK1\_P and CLK1\_N.

#### 4.4.12 enum clock\_pll\_t

Enumerator

*kCLOCK\_PllArm* PLL ARM.  
*kCLOCK\_PllSys* PLL SYS.  
*kCLOCK\_PllUsb1* PLL USB1.  
*kCLOCK\_PllAudio* PLL Audio.  
*kCLOCK\_PllVideo* PLL Video.  
*kCLOCK\_PllEnet* PLL Enet0.  
*kCLOCK\_PllEnet25M* PLL Enet1.

#### 4.4.13 enum clock\_pfd\_t

Enumerator

- kCLOCK\_Pfd0* PLL PFD0.
- kCLOCK\_Pfd1* PLL PFD1.
- kCLOCK\_Pfd2* PLL PFD2.
- kCLOCK\_Pfd3* PLL PFD3.

#### 4.4.14 enum clock\_output1\_selection\_t

Enumerator

- kCLOCK\_OutputPllUsb1* Selects USB1 PLL clock(Divided by 2) output.
- kCLOCK\_OutputPllSys* Selects SYS PLL clock(Divided by 2) output.
- kCLOCK\_OutputPllVideo* Selects Video PLL clock(Divided by 2) output.
- kCLOCK\_OutputSemcClk* Selects semc clock root output.
- kCLOCK\_OutputLcdifPixClk* Selects Lcdif pix clock root output.
- kCLOCK\_OutputAhbClk* Selects AHB clock root output.
- kCLOCK\_OutputIpgClk* Selects IPG clock root output.
- kCLOCK\_OutputPerClk* Selects PERCLK clock root output.
- kCLOCK\_OutputCkilSyncClk* Selects Ckil clock root output.
- kCLOCK\_OutputPll4MainClk* Selects PLL4 main clock output.
- kCLOCK\_DisableClockOutput1* Disables CLKO1.

#### 4.4.15 enum clock\_output2\_selection\_t

Enumerator

- kCLOCK\_OutputUsdhc1Clk* Selects USDHC1 clock root output.
- kCLOCK\_OutputLpi2cClk* Selects LPI2C clock root output.
- kCLOCK\_OutputOscClk* Selects OSC output.
- kCLOCK\_OutputUsdhc2Clk* Selects USDHC2 clock root output.
- kCLOCK\_OutputSai1Clk* Selects SAI1 clock root output.
- kCLOCK\_OutputSai2Clk* Selects SAI2 clock root output.
- kCLOCK\_OutputSai3Clk* Selects SAI3 clock root output.
- kCLOCK\_OutputCanClk* Selects CAN clock root output.
- kCLOCK\_OutputFlexspiClk* Selects FLEXSPI clock root output.
- kCLOCK\_OutputUartClk* Selects UART clock root output.
- kCLOCK\_OutputSpdif0Clk* Selects SPDIF0 clock root output.
- kCLOCK\_DisableClockOutput2* Disables CLKO2.

#### 4.4.16 enum clock\_output\_divider\_t

Enumerator

- kCLOCK\_DivideBy1* Output clock divided by 1.
- kCLOCK\_DivideBy2* Output clock divided by 2.
- kCLOCK\_DivideBy3* Output clock divided by 3.
- kCLOCK\_DivideBy4* Output clock divided by 4.
- kCLOCK\_DivideBy5* Output clock divided by 5.
- kCLOCK\_DivideBy6* Output clock divided by 6.
- kCLOCK\_DivideBy7* Output clock divided by 7.
- kCLOCK\_DivideBy8* Output clock divided by 8.

#### 4.4.17 enum clock\_root\_t

Enumerator

- kCLOCK\_Usdhc1ClkRoot* USDHC1 clock root.
- kCLOCK\_Usdhc2ClkRoot* USDHC2 clock root.
- kCLOCK\_FlexspiClkRoot* FLEXSPI clock root.
- kCLOCK\_Flexspi2ClkRoot* FLEXSPI2 clock root.
- kCLOCK\_LpspiClkRoot* LPSPI clock root.
- kCLOCK\_TraceClkRoot* Trace clock root.
- kCLOCK\_Sai1ClkRoot* SAI1 clock root.
- kCLOCK\_Sai2ClkRoot* SAI2 clock root.
- kCLOCK\_Sai3ClkRoot* SAI3 clock root.
- kCLOCK\_Lpi2cClkRoot* LPI2C clock root.
- kCLOCK\_CanClkRoot* CAN clock root.
- kCLOCK\_UartClkRoot* UART clock root.
- kCLOCK\_LcdifClkRoot* LCD clock root.
- kCLOCK\_SpdifClkRoot* SPDIF clock root.
- kCLOCK\_Flexio1ClkRoot* FLEXIO1 clock root.
- kCLOCK\_Flexio2ClkRoot* FLEXIO2 clock root.

### 4.5 Function Documentation

#### 4.5.1 static void CLOCK\_SetMux( *clock\_mux\_t mux*, *uint32\_t value* ) [inline], [static]

Parameters

|              |                                                                  |
|--------------|------------------------------------------------------------------|
| <i>mux</i>   | Which mux node to set, see <a href="#">clock_mux_t</a> .         |
| <i>value</i> | Clock mux value to set, different mux has different value range. |

#### 4.5.2 static uint32\_t CLOCK\_GetMux( *clock\_mux\_t mux* ) [inline], [static]

Parameters

|            |                                                          |
|------------|----------------------------------------------------------|
| <i>mux</i> | Which mux node to get, see <a href="#">clock_mux_t</a> . |
|------------|----------------------------------------------------------|

Returns

Clock mux value.

#### 4.5.3 static void CLOCK\_SetDiv( *clock\_div\_t divider*, *uint32\_t value* ) [inline], [static]

Example, set the ARM clock divider to divide by 2:

```
CLOCK_SetDiv(kCLOCK_ArmDiv, kCLOCK_ArmDivBy2);
```

Example, set the LPI2C clock divider to divide by 5.

```
CLOCK_SetDiv(kCLOCK_Lpi2cDiv, kCLOCK_MiscDivBy5);
```

Only [kCLOCK\\_PerClk](#), [kCLOCK\\_Lpi2cDiv](#), [kCLOCK\\_CanDiv](#), [kCLOCK\\_UartDiv](#), [kCLOCK\\_Sai1Div](#), [kCLOCK\\_Sai2Div](#), [kCLOCK\\_Sai3Div](#) can use the divider [kCLOCK\\_MiscDivByxxx](#).

Parameters

|                |                                                                                                                                                                                           |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>divider</i> | Which divider node to set.                                                                                                                                                                |
| <i>value</i>   | Clock div value to set, different divider has different value range. See <a href="#">clock_div_value_t</a> for details. Divided clock frequency = Undivided clock frequency / (value + 1) |

#### 4.5.4 static uint32\_t CLOCK\_GetDiv( *clock\_div\_t divider* ) [inline], [static]

Parameters

|                |                                                          |
|----------------|----------------------------------------------------------|
| <i>divider</i> | Which div node to get, see <a href="#">clock_div_t</a> . |
|----------------|----------------------------------------------------------|

#### 4.5.5 static void CLOCK\_ControlGate( `clock_ip_name_t name`, `clock_gate_value_t value` ) [inline], [static]

Parameters

|              |                                                                   |
|--------------|-------------------------------------------------------------------|
| <i>name</i>  | Which clock to enable, see <a href="#">clock_ip_name_t</a> .      |
| <i>value</i> | Clock gate value to set, see <a href="#">clock_gate_value_t</a> . |

#### 4.5.6 static void CLOCK\_EnableClock( `clock_ip_name_t name` ) [inline], [static]

Parameters

|             |                                                              |
|-------------|--------------------------------------------------------------|
| <i>name</i> | Which clock to enable, see <a href="#">clock_ip_name_t</a> . |
|-------------|--------------------------------------------------------------|

#### 4.5.7 static void CLOCK\_DisableClock( `clock_ip_name_t name` ) [inline], [static]

Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>name</i> | Which clock to disable, see <a href="#">clock_ip_name_t</a> . |
|-------------|---------------------------------------------------------------|

#### 4.5.8 static void CLOCK\_SetMode( `clock_mode_t mode` ) [inline], [static]

Parameters

|             |                                                         |
|-------------|---------------------------------------------------------|
| <i>mode</i> | Which mode to enter, see <a href="#">clock_mode_t</a> . |
|-------------|---------------------------------------------------------|

**4.5.9 static uint32\_t CLOCK\_GetOscFreq( void ) [inline], [static]**

This function will return the external XTAL OSC frequency if it is selected as the source of OSC, otherwise internal 24MHz RC OSC frequency will be returned.

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.10 uint32\_t CLOCK\_GetAhbFreq( void )**

Returns

The AHB clock frequency value in hertz.

**4.5.11 uint32\_t CLOCK\_GetSemcFreq( void )**

Returns

The SEMC clock frequency value in hertz.

**4.5.12 uint32\_t CLOCK\_GetIpqFreq( void )**

Returns

The IPG clock frequency value in hertz.

**4.5.13 uint32\_t CLOCK\_GetPerClkFreq( void )**

Returns

The PER clock frequency value in hertz.

**4.5.14 uint32\_t CLOCK\_GetFreq( clock\_name\_t name )**

This function checks the current clock configurations and then calculates the clock frequency for a specific clock name defined in `clock_name_t`.

Parameters

|             |                                                  |
|-------------|--------------------------------------------------|
| <i>name</i> | Clock names defined in <code>clock_name_t</code> |
|-------------|--------------------------------------------------|

Returns

Clock frequency value in hertz

#### 4.5.15 `static uint32_t CLOCK_GetCpuClkFreq( void ) [inline], [static]`

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.16 `uint32_t CLOCK_GetClockRootFreq( clock_root_t clockRoot )`

Parameters

|                  |                                                                                          |
|------------------|------------------------------------------------------------------------------------------|
| <i>clockRoot</i> | The clock root used to get the frequency, please refer to <a href="#">clock_root_t</a> . |
|------------------|------------------------------------------------------------------------------------------|

Returns

The frequency of selected clock root.

#### 4.5.17 `void CLOCK_InitExternalClk( bool bypassXtalOsc )`

This function supports two modes:

1. Use external crystal oscillator.
2. Bypass the external crystal oscillator, using input source clock directly.

After this function, please call `CLOCK_SetXtal0Freq` to inform clock driver the external clock frequency.

Parameters

|                      |                                                         |
|----------------------|---------------------------------------------------------|
| <i>bypassXtalOsc</i> | Pass in true to bypass the external crystal oscillator. |
|----------------------|---------------------------------------------------------|

Note

This device does not support bypass external crystal oscillator, so the input parameter should always be false.

**4.5.18 void CLOCK\_DeinitExternalClk ( void )**

This function disables the external 24MHz clock.

After this function, please call CLOCK\_SetXtal0Freq to set external clock frequency to 0.

**4.5.19 void CLOCK\_SwitchOsc ( clock\_osc\_t osc )**

This function switches the OSC source for SoC.

Parameters

|            |                          |
|------------|--------------------------|
| <i>osc</i> | OSC source to switch to. |
|------------|--------------------------|

**4.5.20 static uint32\_t CLOCK\_GetRtcFreq ( void ) [inline], [static]**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.21 static void CLOCK\_SetXtalFreq ( uint32\_t freq ) [inline], [static]**

Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>freq</i> | The XTAL input clock frequency in Hz. |
|-------------|---------------------------------------|

**4.5.22 static void CLOCK\_SetRtcXtalFreq ( uint32\_t freq ) [inline], [static]**

Parameters

|             |                                           |
|-------------|-------------------------------------------|
| <i>freq</i> | The RTC XTAL input clock frequency in Hz. |
|-------------|-------------------------------------------|

**4.5.23 bool CLOCK\_EnableUsbhs0Clock ( clock\_usb\_src\_t src, uint32\_t freq )**

This function only enables the access to USB HS prepheral, upper layer should first call the CLOCK\_EnableUsbhs0PhyPllClock to enable the PHY clock to use USB HS.

## Parameters

|             |                                                                                                 |
|-------------|-------------------------------------------------------------------------------------------------|
| <i>src</i>  | USB HS does not care about the clock source, here must be <a href="#">kCLOCK_UsbSrcUnused</a> . |
| <i>freq</i> | USB HS does not care about the clock source, so this parameter is ignored.                      |

## Return values

|              |                                                         |
|--------------|---------------------------------------------------------|
| <i>true</i>  | The clock is set successfully.                          |
| <i>false</i> | The clock source is invalid to get proper USB HS clock. |

## 4.6 Variable Documentation

### 4.6.1 volatile uint32\_t g\_xtalFreq

The XTAL (24M OSC/SYSOSC) clock frequency in Hz, when the clock is setup, use the function CLOCK\_SetXtalFreq to set the value in to clock driver. For example, if XTAL is 24MHz,

```
* CLOCK_InitExternalClk(false);
* CLOCK_SetXtalFreq(240000000);
*
```

### 4.6.2 volatile uint32\_t g\_rtcXtalFreq

The RTC XTAL (32K OSC) clock frequency in Hz, when the clock is setup, use the function CLOCK\_SetRtcXtalFreq to set the value in to clock driver.

# Chapter 5

## ROMAPI Driver

### 5.1 Overview

The ROMAPI driver provides the functionalities to operate the external NOR Flash connected to the FLEXSPI controller.

The ROMAPI driver supports:

- Initialize serial NOR flash via FLEXSPI
- Program data to serial NOR flash via FLEXSPI.
- Erase serial NOR flash region via FLEXSPI.

### Data Structures

- struct `serial_nor_config_option_t`  
*Serial NOR Configuration Option. [More...](#)*
- struct `flexspi_lut_seq_t`  
*FLEXSPI LUT Sequence structure. [More...](#)*
- struct `flexspi_mem_config_t`  
*FLEXSPI Memory Configuration Block. [More...](#)*
- struct `flexspi_nor_config_t`  
*Serial NOR configuration block. [More...](#)*
- struct `flexspi_xfer_t`  
*FLEXSPI Transfer Context. [More...](#)*

### Macros

- #define `FSL_ROM_ROMAPI_VERSION` (`MAKE_VERSION(1U, 0U, 2U)`)  
*ROM API version 1.0.2.*
- #define `FSL_ROM_FLEXSPINOR_DRIVER_VERSION` (`MAKE_VERSION(1U, 5U, 0U)`)  
*ROM FLEXSPI NOR driver version 1.5.0.*
- #define `kROM_StatusGroup_FLEXSPI` 60U  
*ROM FLEXSPI status group number.*
- #define `kROM_StatusGroup_FLEXSPINOR` 200U  
*ROM FLEXSPI NOR status group number.*
- #define `FSL_ROM_FLEXSPI_BITMASK`(bit\_offset) (`1U << (bit_offset)`)  
*Generate bit mask.*
- #define `FLEXSPI_CFG_BLK_TAG` (0x42464346UL)  
*FLEXSPI memory config block related definitions.*
- #define `FLEXSPI_CFG_BLK_VERSION` (0x56010400UL)  
*V1.4.0.*
- #define `NOR_CMD_LUT_SEQ_IDX_READ` 0U  
*NOR LUT sequence index used for default LUT assignment NOTE: The will take effect if the lut sequences are not customized.*
- #define `NOR_CMD_LUT_SEQ_IDX_READSTATUS` 1U

- *Read Status LUT sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_READSTATUS\_XPI 2U
- *Read status DPI/QPI/OPI sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_WRITEENABLE 3U
- *Write Enable sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_WRITEENABLE\_XPI 4U
- *Write Enable DPI/QPI/OPI sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_ERASESECTOR 5U
- *Erase Sector sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_ERASEBLOCK 8U
- *Erase Block sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_PAGEPROGRAM 9U
- *Program sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_CHIPERASE 11U
- *Chip Erase sequence in lookupTable id stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_READ\_SFDP 13U
- *Read SFDP sequence in lookupTable id stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_RESTORE\_NOCMD 14U
- *Restore 0-4-4/0-8-8 mode sequence id in lookupTable stored in config block.*  
• #define NOR\_CMD\_LUT\_SEQ\_IDX\_EXIT\_NOCMD 15U
- *Exit 0-4-4/0-8-8 mode sequence id in lookupTable stored in config blobk.*

## Enumerations

- enum \_flexspi\_nor\_status {
 kStatus\_ROM\_FLEXSPI\_SequenceExecutionTimeout,  
 kStatus\_ROM\_FLEXSPI\_InvalidSequence = MAKE\_STATUS(kROM\_StatusGroup\_FLEXSPI, 1),  
 kStatus\_ROM\_FLEXSPI\_DeviceTimeout = MAKE\_STATUS(kROM\_StatusGroup\_FLEXSPI, 2),  
 kStatus\_FLEXSPINOR\_DTRRead\_DummyProbeFailed,  
 kStatus\_ROM\_FLEXSPINOR\_SFDP\_NotFound,  
 kStatus\_ROM\_FLEXSPINOR\_Flash\_NotFound }
- ROM FLEXSPI NOR flash status.
- enum flexspi\_operation\_t {
 kFLEXSPIOperation\_Command,  
 kFLEXSPIOperation\_Config,  
 kFLEXSPIOperation\_Write,  
 kFLEXSPIOperation\_Read }

## Common ROMAPI features info defines

- #define FSL\_ROM\_HAS\_FLEXSPINOR\_API (1)
- #define FSL\_ROM\_HAS\_RUNBOOTLOADER\_API (1)
- #define FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_GET\_CONFIG (1)
- #define FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_FLASH\_INIT (1)
- #define FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_ERASE (1)
- #define FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_ERASE\_SECTOR (0)
- #define FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_ERASE\_BLOCK (0)
- #define FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_ERASE\_ALL (1)
- #define FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_READ (1)

- #define **FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_UPDATE\_LUT** (1)
- #define **FSL\_ROM\_FLEXSPINOR\_API\_HAS\_FEATURE\_CMD\_XFER** (1)

## Support for init FLEXSPI NOR configuration

- enum
  - Flash Pad Definitions.*
- enum {
  - kFLEXSPIClk\_SDR,**
  - kFLEXSPIClk\_DDR }**

*FLEXSPI clock configuration type.*
- enum **\_flexspi\_read\_sample\_clk**
  - FLEXSPI Read Sample Clock Source definition.*
- enum { **kFLEXSPIDeviceType\_SerialNOR** = 1U }
  - Flash Type Definition.*
- enum {
  - kDeviceConfigCmdType\_Generic,**
  - kDeviceConfigCmdType\_QuadEnable,**
  - kDeviceConfigCmdType\_Spi2Xpi,**
  - kDeviceConfigCmdType\_Xpi2Spi,**
  - kDeviceConfigCmdType\_Spi2NoCmd,**
  - kDeviceConfigCmdType\_Reset }**

*Flash Configuration Command Type.*
- enum **\_flexspi\_serial\_clk\_freq**
  - Definitions for FLEXSPI Serial Clock Frequency.*
- enum {
  - kFLEXSPIMiscOffset\_DiffClkEnable** = 0U,
  - kFLEXSPIMiscOffset\_Ck2Enable** = 1U,
  - kFLEXSPIMiscOffset\_ParallelEnable** = 2U,
  - kFLEXSPIMiscOffset\_WordAddressableEnable** = 3U,
  - kFLEXSPIMiscOffset\_SafeConfigFreqEnable** = 4U,
  - kFLEXSPIMiscOffset\_PadSettingOverrideEnable** = 5U,
  - kFLEXSPIMiscOffset\_DdrModeEnable** = 6U,
  - kFLEXSPIMiscOffset\_UseValidTimeForAllFreq** = 7U }

*Misc feature bit definitions.*
- enum {
  - kSerialFlash\_ISSI\_ManufacturerID** = 0x9DU,
  - kSerialFlash\_Adesto\_ManufacturerID** = 0x1F,
  - kSerialFlash\_Winbond\_ManufacturerID** = 0xEFU,
  - kSerialFlash\_Cypress\_ManufacturerID** = 0x01U }

*Manufacturer ID.*

## Enter Bootloader

- void **ROM\_RunBootloader** (void \*arg)
  - Enter Bootloader.*

## Initialization

- `status_t ROM_FLEXSPI_NorFlash_Init` (`uint32_t` instance, `flexspi_nor_config_t` \*config)  
*Initialize Serial NOR devices via FLEXSPI.*

## Programming

- `status_t ROM_FLEXSPI_NorFlash_ProgramPage` (`uint32_t` instance, `flexspi_nor_config_t` \*config, `uint32_t` dstAddr, `const uint32_t` \*src)  
*Program data to Serial NOR via FLEXSPI.*

## Reading

- `status_t ROM_FLEXSPI_NorFlash_Read` (`uint32_t` instance, `flexspi_nor_config_t` \*config, `uint32_t` \*dst, `uint32_t` start, `uint32_t` lengthInBytes)  
*Read data from Serial NOR via FLEXSPI.*

## Erasing

- `status_t ROM_FLEXSPI_NorFlash_Erase` (`uint32_t` instance, `flexspi_nor_config_t` \*config, `uint32_t` start, `uint32_t` length)  
*Erase Flash Region specified by address and length.*
- `status_t ROM_FLEXSPI_NorFlash_EraseAll` (`uint32_t` instance, `flexspi_nor_config_t` \*config)  
*Erase all the Serial NOR devices connected on FLEXSPI.*

## Command

- `status_t ROM_FLEXSPI_NorFlash_CommandXfer` (`uint32_t` instance, `flexspi_xfer_t` \*xfer)  
*FLEXSPI command.*

## UpdateLut

- `status_t ROM_FLEXSPI_NorFlash_UpdateLut` (`uint32_t` instance, `uint32_t` seqIndex, `const uint32_t` \*lutBase, `uint32_t` seqNumber)  
*Configure FLEXSPI Lookup table.*

## ClearCache

- `void ROM_FLEXSPI_NorFlash_ClearCache` (`uint32_t` instance)  
*Software reset for the FLEXSPI logic.*

## GetConfig

- `status_t ROM_FLEXSPI_NorFlash_GetConfig` (`uint32_t` instance, `flexspi_nor_config_t` \*config, `serial_nor_config_option_t` \*option)  
*Get FLEXSPI NOR Configuration Block based on specified option.*

## 5.2 Data Structure Documentation

### 5.2.1 struct serial\_nor\_config\_option\_t

### 5.2.2 struct flexspi\_lut\_seq\_t

#### Data Fields

- `uint8_t seqNum`  
*Sequence Number, valid number: 1-16.*
- `uint8_t seqId`  
*Sequence Index, valid number: 0-15.*

### 5.2.3 struct flexspi\_mem\_config\_t

#### Data Fields

- `uint32_t tag`  
*[0x000-0x003] Tag, fixed value 0x42464346UL*
- `uint32_t version`  
*[0x004-0x007] Version,[31:24] - 'V', [23:16] - Major, [15:8] - Minor, [7:0] - bugfix*
- `uint32_t reserved0`  
*[0x008-0x00b] Reserved for future use*
- `uint8_t readSampleClkSrc`  
*[0x00c-0x00c] Read Sample Clock Source, valid value: 0/1/3*
- `uint8_t csHoldTime`  
*[0x00d-0x00d] Data hold time, default value: 3*
- `uint8_t csSetupTime`  
*[0x00e-0x00e] Date setup time, default value: 3*
- `uint8_t columnAddressWidth`  
*[0x00f-0x00f] Column Address width, for HyperBus protocol, it is fixed to 3, For Serial NAND, need to refer to datasheet*
- `uint8_t deviceModeCfgEnable`  
*[0x010-0x010] Device Mode Configure enable flag, 1 - Enable, 0 - Disable*
- `uint8_t deviceModeType`  
*[0x011-0x011] Specify the configuration command type:Quad Enable, DPI/QPI/OPI switch, Generic configuration, etc.*
- `uint16_t waitTimeCfgCommands`  
*[0x012-0x013] Wait time for all configuration commands, unit: 100us, Used for DPI/QPI/OPI switch or reset command*
- `flexspi_lut_seq_t deviceModeSeq`  
*[0x014-0x017] Device mode sequence info, [7:0] - LUT sequence id, [15:8] - LUt sequence number, [31:16] Reserved*
- `uint32_t deviceModeArg`  
*[0x018-0x01b] Argument/Parameter for device configuration*
- `uint8_t configCmdEnable`  
*[0x01c-0x01c] Configure command Enable Flag, 1 - Enable, 0 - Disable*
- `uint8_t configModeType`  
*[3]*

- **[0x01d-0x01f] Configure Mode Type, similar as deviceModeType**
- **flexspi\_lut\_seq\_t configCmdSeqs [3]**  
[0x020-0x02b] Sequence info for Device Configuration command, similar as deviceModeSeq
- **uint32\_t reserved1**  
[0x02c-0x02f] Reserved for future use
- **uint32\_t configCmdArgs [3]**  
[0x030-0x03b] Arguments/Parameters for device Configuration commands
- **uint32\_t reserved2**  
[0x03c-0x03f] Reserved for future use
- **uint32\_t controllerMiscOption**  
[0x040-0x043] Controller Misc Options, see Misc feature bit definitions for more details
- **uint8\_t deviceType**  
[0x044-0x044] Device Type: See Flash Type Definition for more details
- **uint8\_t sflashPadType**  
[0x045-0x045] Serial Flash Pad Type: 1 - Single, 2 - Dual, 4 - Quad, 8 - Octal
- **uint8\_t serialClkFreq**  
[0x046-0x046] Serial Flash Frequency, device specific definitions, See System Boot Chapter for more details
- **uint8\_t lutCustomSeqEnable**  
[0x047-0x047] LUT customization Enable, it is required if the program/erase cannot be done using 1 LUT sequence, currently, only applicable to HyperFLASH
- **uint32\_t reserved3 [2]**  
[0x048-0x04f] Reserved for future use
- **uint32\_t sflashA1Size**  
[0x050-0x053] Size of Flash connected to A1
- **uint32\_t sflashA2Size**  
[0x054-0x057] Size of Flash connected to A2
- **uint32\_t sflashB1Size**  
[0x058-0x05b] Size of Flash connected to B1
- **uint32\_t sflashB2Size**  
[0x05c-0x05f] Size of Flash connected to B2
- **uint32\_t csPadSettingOverride**  
[0x060-0x063] CS pad setting override value
- **uint32\_t sclkPadSettingOverride**  
[0x064-0x067] SCK pad setting override value
- **uint32\_t dataPadSettingOverride**  
[0x068-0x06b] data pad setting override value
- **uint32\_t dqsPadSettingOverride**  
[0x06c-0x06f] DQS pad setting override value
- **uint32\_t timeoutInMs**  
[0x070-0x073] Timeout threshold for read status command
- **uint32\_t commandInterval**  
[0x074-0x077] CS deselect interval between two commands
- **flexspi\_dll\_time\_t dataValidTime [2]**  
[0x078-0x07b] CLK edge to data valid time for PORT A and PORT B
- **uint16\_t busyOffset**  
[0x07c-0x07d] Busy offset, valid value: 0-31
- **uint16\_t busyBitPolarity**  
[0x07e-0x07f] Busy flag polarity, 0 - busy flag is 1 when flash device is busy, 1 - busy flag is 0 when flash device is busy
- **uint32\_t lookupTable [64]**

- **flexspi\_lut\_seq\_t lutCustomSeq [12]**  
[0x180-0x1af] Customizable LUT Sequences
- **uint32\_t reserved4 [4]**  
[0x1b0-0x1bf] Reserved for future use

## Field Documentation

(1) **uint8\_t flexspi\_mem\_config\_t::deviceModeType**

### 5.2.4 struct flexspi\_nor\_config\_t

#### Data Fields

- **flexspi\_mem\_config\_t memConfig**  
*Common memory configuration info via FLEXSPI.*
- **uint32\_t pageSize**  
*Page size of Serial NOR.*
- **uint32\_t sectorSize**  
*Sector size of Serial NOR.*
- **uint8\_t ipcmdSerialClkFreq**  
*Clock frequency for IP command.*
- **uint8\_t isUniformBlockSize**  
*Sector/Block size is the same.*
- **uint8\_t isDataOrderSwapped**  
*Data order (D0, D1, D2, D3) is swapped (D1,D0, D3, D2)*
- **uint8\_t reserved0 [1]**  
*Reserved for future use.*
- **uint8\_t serialNorType**  
*Serial NOR Flash type: 0/1/2/3.*
- **uint8\_t needExitNoCmdMode**  
*Need to exit NoCmd mode before other IP command.*
- **uint8\_t halfClkForNonReadCmd**  
*Half the Serial Clock for non-read command: true/false.*
- **uint8\_t needRestoreNoCmdMode**  
*Need to Restore NoCmd mode after IP command execution.*
- **uint32\_t blockSize**  
*Block size.*
- **uint32\_t reserve2 [11]**  
*Reserved for future use.*

### 5.2.5 struct flexspi\_xfer\_t

#### Data Fields

- **flexspi\_operation\_t operation**  
*FLEXSPI operation.*
- **uint32\_t baseAddress**

- `uint32_t seqId`  
*Sequence Id.*
- `uint32_t seqNum`  
*Sequence Number.*
- `bool isParallelModeEnable`  
*Is a parallel transfer.*
- `uint32_t * txBuffer`  
*Tx buffer.*
- `uint32_t txSize`  
*Tx size in bytes.*
- `uint32_t * rxBuffer`  
*Rx buffer.*
- `uint32_t rxSize`  
*Rx size in bytes.*

## 5.3 Macro Definition Documentation

**5.3.1 #define FSL\_ROM\_ROMAPI\_VERSION (MAKE\_VERSION(1U, 0U, 2U))**

**5.3.2 #define FSL\_ROM\_FLEXSPINOR\_DRIVER\_VERSION (MAKE\_VERSION(1U, 5U, 0U))**

**5.3.3 #define kROM\_StatusGroup\_FLEXSPI 60U**

**5.3.4 #define kROM\_StatusGroup\_FLEXSPINOR 200U**

**5.3.5 #define FLEXSPI\_CFG\_BLK\_TAG (0x42464346UL)**

ascii "FCFB" Big Endian

**5.3.6 #define NOR\_CMD\_LUT\_SEQ\_IDX\_READ 0U**

READ LUT sequence id in lookupTable stored in config block

## 5.4 Enumeration Type Documentation

### 5.4.1 anonymous enum

Enumerator

**kFLEXSPIClk\_SDR** Clock configure for SDR mode.

**kFLEXSPIClk\_DDR** Clock configurat for DDR mode.

### 5.4.2 anonymous enum

Enumerator

***kFLEXSPIDeviceType\_SerialNOR*** Flash device is Serial NOR.

### 5.4.3 anonymous enum

Enumerator

***kDeviceConfigCmdType\_Generic*** Generic command, for example: configure dummy cycles, drive strength, etc.

***kDeviceConfigCmdType\_QuadEnable*** Quad Enable command.

***kDeviceConfigCmdType\_Spi2Xpi*** Switch from SPI to DPI/QPI/OPI mode.

***kDeviceConfigCmdType\_Xpi2Spi*** Switch from DPI/QPI/OPI to SPI mode.

***kDeviceConfigCmdType\_Spi2NoCmd*** Switch to 0-4-4/0-8-8 mode.

***kDeviceConfigCmdType\_Reset*** Reset device command.

### 5.4.4 anonymous enum

Enumerator

***kFLEXSPIMiscOffset\_DiffClkEnable*** Bit for Differential clock enable.

***kFLEXSPIMiscOffset\_Ck2Enable*** Bit for CK2 enable.

***kFLEXSPIMiscOffset\_ParallelEnable*** Bit for Parallel mode enable.

***kFLEXSPIMiscOffset\_WordAddressableEnable*** Bit for Word Addressable enable.

***kFLEXSPIMiscOffset\_SafeConfigFreqEnable*** Bit for Safe Configuration Frequency enable.

***kFLEXSPIMiscOffset\_PadSettingOverrideEnable*** Bit for Pad setting override enable.

***kFLEXSPIMiscOffset\_DdrModeEnable*** Bit for DDR clock configuration indication.

***kFLEXSPIMiscOffset\_UseValidTimeForAllFreq*** Bit for DLLCR settings under all modes.

### 5.4.5 anonymous enum

Enumerator

***kSerialFlash\_ISSI\_ManufacturerID*** Manufacturer ID of the ISSI serial flash.

***kSerialFlash\_Adesto\_ManufacturerID*** Manufacturer ID of the Adesto Technologies serial flash.

***kSerialFlash\_Winbond\_ManufacturerID*** Manufacturer ID of the Winbond serial flash.

***kSerialFlash\_Cypress\_ManufacturerID*** Manufacturer ID for Cypress.

## 5.4.6 enum \_flexspi\_nor\_status

Enumerator

*kStatus\_ROM\_FLEXSPI\_SequenceExecutionTimeout* Status for Sequence Execution timeout.

*kStatus\_ROM\_FLEXSPI\_InvalidSequence* Status for Invalid Sequence.

*kStatus\_ROM\_FLEXSPI\_DeviceTimeout* Status for Device timeout.

*kStatus\_FLEXSPINOR\_DTRRead\_DummyProbeFailed* Status for DDR Read dummy probe failure.

*kStatus\_ROM\_FLEXSPINOR\_SFDP\_NotFound* Status for SFDP read failure.

*kStatus\_ROM\_FLEXSPINOR\_Flash\_NotFound* Status for Flash detection failure.

## 5.4.7 enum flexspi\_operation\_t

Enumerator

*kFLEXSPIOperation\_Command* FLEXSPI operation: Only command, both TX and RX buffer are ignored.

*kFLEXSPIOperation\_Config* FLEXSPI operation: Configure device mode, the TX FIFO size is fixed in LUT.

*kFLEXSPIOperation\_Write* FLEXSPI operation: Write, only TX buffer is effective.

*kFLEXSPIOperation\_Read* FLEXSPI operation: Read, only Rx Buffer is effective.

## 5.5 Function Documentation

### 5.5.1 void ROM\_RunBootloader ( void \* *arg* )

Parameters

|            |                                                                                                                         |
|------------|-------------------------------------------------------------------------------------------------------------------------|
| <i>arg</i> | A pointer to the storage for the bootloader param. refer to System Boot Chapter in device reference manual for details. |
|------------|-------------------------------------------------------------------------------------------------------------------------|

### 5.5.2 status\_t ROM\_FLEXSPI\_NorFlash\_Init ( uint32\_t *instance*, flexspi\_nor\_config\_t \* *config* )

This function checks and initializes the FLEXSPI module for the other FLEXSPI APIs.

Parameters

|                 |                                                        |
|-----------------|--------------------------------------------------------|
| <i>instance</i> | storage the instance of FLEXSPI.                       |
| <i>config</i>   | A pointer to the storage for the driver runtime state. |

Return values

|                                                     |                                 |
|-----------------------------------------------------|---------------------------------|
| <i>kStatus_Success</i>                              | Api was executed successfully.  |
| <i>kStatus_InvalidArgument</i>                      | A invalid argument is provided. |
| <i>kStatus_ROM_FLEXSPI_InvalidSequence</i>          | A invalid Sequence is provided. |
| <i>kStatus_ROM_FLEXSPI_SequenceExecutionTimeout</i> | Sequence Execution timeout.     |
| <i>kStatus_ROM_FLEXSPI_DeviceTimeout</i>            | the device timeout              |

### 5.5.3 status\_t ROM\_FLEXSPI\_NorFlash\_ProgramPage ( uint32\_t *instance*, flexspi\_nor\_config\_t \* *config*, uint32\_t *dstAddr*, const uint32\_t \* *src* )

This function programs the NOR flash memory with the dest address for a given flash area as determined by the dst address and the length.

Parameters

|                 |                                                                                                                                                                                                                          |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>instance</i> | storage the instance of FLEXSPI.                                                                                                                                                                                         |
| <i>config</i>   | A pointer to the storage for the driver runtime state.                                                                                                                                                                   |
| <i>dstAddr</i>  | A pointer to the desired flash memory to be programmed. NOTE: It is recommended that use page aligned access; If the dstAddr is not aligned to page, the driver automatically aligns address down with the page address. |
| <i>src</i>      | A pointer to the source buffer of data that is to be programmed into the NOR flash.                                                                                                                                      |

Return values

|                        |                                |
|------------------------|--------------------------------|
| <i>kStatus_Success</i> | Api was executed successfully. |
|------------------------|--------------------------------|

|                                                                 |                                 |
|-----------------------------------------------------------------|---------------------------------|
| <i>kStatus_InvalidArgument</i>                                  | A invalid argument is provided. |
| <i>kStatus_ROM_FLEXSPI-<br/>_InvalidSequence</i>                | A invalid Sequence is provided. |
| <i>kStatus_ROM_FLEXSPI-<br/>_SequenceExecution-<br/>Timeout</i> | Sequence Execution timeout.     |
| <i>kStatus_ROM_FLEXSPI-<br/>_DeviceTimeout</i>                  | the device timeout              |

#### 5.5.4 status\_t ROM\_FLEXSPI\_NorFlash\_Read ( *uint32\_t instance,* *flexspi\_nor\_config\_t \* config, uint32\_t \* dst, uint32\_t start, uint32\_t* *lengthInBytes* )

This function read the NOR flash memory with the start address for a given flash area as determined by the dst address and the length.

Parameters

|                      |                                                                                                                                                                                                                                              |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>instance</i>      | storage the instance of FLEXSPI.                                                                                                                                                                                                             |
| <i>config</i>        | A pointer to the storage for the driver runtime state.                                                                                                                                                                                       |
| <i>dst</i>           | A pointer to the dest buffer of data that is to be read from the NOR flash. NOTE: It is recommended that use page aligned access; If the dstAddr is not aligned to page, the driver automatically aligns address down with the page address. |
| <i>start</i>         | The start address of the desired NOR flash memory to be read.                                                                                                                                                                                |
| <i>lengthInBytes</i> | The length, given in bytes to be read.                                                                                                                                                                                                       |

Return values

|                                                                 |                                 |
|-----------------------------------------------------------------|---------------------------------|
| <i>kStatus_Success</i>                                          | Api was executed succesfuly.    |
| <i>kStatus_InvalidArgument</i>                                  | A invalid argument is provided. |
| <i>kStatus_ROM_FLEXSPI-<br/>_InvalidSequence</i>                | A invalid Sequence is provided. |
| <i>kStatus_ROM_FLEXSPI-<br/>_SequenceExecution-<br/>Timeout</i> | Sequence Execution timeout.     |

|                                                 |                    |
|-------------------------------------------------|--------------------|
| <code>kStatus_ROM_FLEXSPI-_DeviceTimeout</code> | the device timeout |
|-------------------------------------------------|--------------------|

### 5.5.5 status\_t ROM\_FLEXSPI\_NorFlash\_Erase ( `uint32_t instance,` `flexspi_nor_config_t * config, uint32_t start, uint32_t length` )

This function erases the appropriate number of flash sectors based on the desired start address and length.

Parameters

|                       |                                                                                                                                                                                                                                                     |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <code>instance</code> | storage the index of FLEXSPI.                                                                                                                                                                                                                       |
| <code>config</code>   | A pointer to the storage for the driver runtime state.                                                                                                                                                                                              |
| <code>start</code>    | The start address of the desired NOR flash memory to be erased. NOTE: It is recommended that use sector-aligned access nor device; If dstAddr is not aligned with the sector, the driver automatically aligns address down with the sector address. |
| <code>length</code>   | The length, given in bytes to be erased. NOTE: It is recommended that use sector-aligned access nor device; If length is not aligned with the sector, the driver automatically aligns up with the sector.                                           |

Return values

|                                                             |                                 |
|-------------------------------------------------------------|---------------------------------|
| <code>kStatus_Success</code>                                | Api was executed successfully.  |
| <code>kStatus_InvalidArgument</code>                        | A invalid argument is provided. |
| <code>kStatus_ROM_FLEXSPI-_InvalidSequence</code>           | A invalid Sequence is provided. |
| <code>kStatus_ROM_FLEXSPI-_SequenceExecution-Timeout</code> | Sequence Execution timeout.     |
| <code>kStatus_ROM_FLEXSPI-_DeviceTimeout</code>             | the device timeout              |

### 5.5.6 status\_t ROM\_FLEXSPI\_NorFlash\_EraseAll ( `uint32_t instance,` `flexspi_nor_config_t * config` )

Parameters

|                 |                                                        |
|-----------------|--------------------------------------------------------|
| <i>instance</i> | storage the instance of FLEXSPI.                       |
| <i>config</i>   | A pointer to the storage for the driver runtime state. |

Return values

|                                                     |                                 |
|-----------------------------------------------------|---------------------------------|
| <i>kStatus_Success</i>                              | Api was executed successfully.  |
| <i>kStatus_InvalidArgument</i>                      | A invalid argument is provided. |
| <i>kStatus_ROM_FLEXSPI_InvalidSequence</i>          | A invalid Sequence is provided. |
| <i>kStatus_ROM_FLEXSPI_SequenceExecutionTimeout</i> | Sequence Execution timeout.     |
| <i>kStatus_ROM_FLEXSPI_DeviceTimeout</i>            | the device timeout              |

### 5.5.7 status\_t ROM\_FLEXSPI\_NorFlash\_CommandXfer ( uint32\_t *instance*, flexspi\_xfer\_t \* *xfer* )

This function is used to perform the command write sequence to the NOR device.

Parameters

|                 |                                                    |
|-----------------|----------------------------------------------------|
| <i>instance</i> | storage the index of FLEXSPI.                      |
| <i>xfer</i>     | A pointer to the storage FLEXSPI Transfer Context. |

Return values

|                                                     |                                 |
|-----------------------------------------------------|---------------------------------|
| <i>kStatus_Success</i>                              | Api was executed successfully.  |
| <i>kStatus_InvalidArgument</i>                      | A invalid argument is provided. |
| <i>kStatus_ROM_FLEXSPI_InvalidSequence</i>          | A invalid Sequence is provided. |
| <i>kStatus_ROM_FLEXSPI_SequenceExecutionTimeout</i> | Sequence Execution timeout.     |

5.5.8 **status\_t ROM\_FLEXSPI\_NorFlash\_UpdateLut( uint32\_t *instance*, uint32\_t *seqIndex*, const uint32\_t \* *lutBase*, uint32\_t *seqNumber* )**

Parameters

|                  |                                                       |
|------------------|-------------------------------------------------------|
| <i>instance</i>  | storage the index of FLEXSPI.                         |
| <i>seqIndex</i>  | storage the sequence Id.                              |
| <i>lutBase</i>   | A pointer to the look-up-table for command sequences. |
| <i>seqNumber</i> | storage sequence number.                              |

Return values

|                                                     |                                 |
|-----------------------------------------------------|---------------------------------|
| <i>kStatus_Success</i>                              | Api was executed successfully.  |
| <i>kStatus_InvalidArgument</i>                      | A invalid argument is provided. |
| <i>kStatus_ROM_FLEXSPI_InvalidSequence</i>          | A invalid Sequence is provided. |
| <i>kStatus_ROM_FLEXSPI_SequenceExecutionTimeout</i> | Sequence Execution timeout.     |

### 5.5.9 void ROM\_FLEXSPI\_NorFlash\_ClearCache ( uint32\_t *instance* )

This function sets the software reset flags for both AHB and buffer domain and resets both AHB buffer and also IP FIFOs.

Parameters

|                 |                               |
|-----------------|-------------------------------|
| <i>instance</i> | storage the index of FLEXSPI. |
|-----------------|-------------------------------|

### 5.5.10 status\_t ROM\_FLEXSPI\_NorFlash\_GetConfig ( uint32\_t *instance*, flexspi\_nor\_config\_t \* *config*, serial\_nor\_config\_option\_t \* *option* )

Parameters

|                 |                                                        |
|-----------------|--------------------------------------------------------|
| <i>instance</i> | storage the instance of FLEXSPI.                       |
| <i>config</i>   | A pointer to the storage for the driver runtime state. |

|               |                                                                   |
|---------------|-------------------------------------------------------------------|
| <i>option</i> | A pointer to the storage Serial NOR Configuration Option Context. |
|---------------|-------------------------------------------------------------------|

Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | Api was executed successfully.  |
| <i>kStatus_InvalidArgument</i> | A invalid argument is provided. |

# Chapter 6

## IOMUXC: IOMUX Controller

### 6.1 Overview

IOMUXC driver provides APIs for pin configuration. It also supports the miscellaneous functions integrated in IOMUXC.

### Files

- file [fsl\\_iomuxc.h](#)

### Driver version

- #define [FSL\\_IOMUXC\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 0, 0))  
*IOMUXC driver version 2.0.0.*

### Pin function ID

The pin function ID is a tuple of <muxRegister muxMode inputRegister inputDaisy configRegister>

- #define [IOMUXC\\_GPIO\\_EMC\\_00\\_SEMC\\_DATA00](#) 0x401F8014U, 0x0U, 0, 0, 0x401F8204U
- #define [IOMUXC\\_GPIO\\_EMC\\_00\\_FLEXPWM4\\_PWMA00](#) 0x401F8014U, 0x1U, 0x401F8494U, 0x0U, 0x401F8204U
- #define [IOMUXC\\_GPIO\\_EMC\\_00\\_LPSPI2\\_SCK](#) 0x401F8014U, 0x2U, 0x401F8500U, 0x1U, 0x401F8204U
- #define [IOMUXC\\_GPIO\\_EMC\\_00\\_XBAR1\\_XBAR\\_IN02](#) 0x401F8014U, 0x3U, 0x401F860CU, 0x0U, 0x401F8204U
- #define [IOMUXC\\_GPIO\\_EMC\\_00\\_FLEXIO1\\_FLEXIO00](#) 0x401F8014U, 0x4U, 0, 0, 0x401F8204U
- #define [IOMUXC\\_GPIO\\_EMC\\_00\\_GPIO4\\_IO00](#) 0x401F8014U, 0x5U, 0, 0, 0x401F8204U
- #define [IOMUXC\\_GPIO\\_EMC\\_01\\_SEMC\\_DATA01](#) 0x401F8018U, 0x0U, 0, 0, 0x401F8208U
- #define [IOMUXC\\_GPIO\\_EMC\\_01\\_FLEXPWM4\\_PWMB00](#) 0x401F8018U, 0x1U, 0, 0, 0x401F8208U
- #define [IOMUXC\\_GPIO\\_EMC\\_01\\_LPSPI2\\_PCS0](#) 0x401F8018U, 0x2U, 0x401F84FCU, 0x1U, 0x401F8208U
- #define [IOMUXC\\_GPIO\\_EMC\\_01\\_XBAR1\\_IN03](#) 0x401F8018U, 0x3U, 0x401F8610U, 0x0U, 0x401F8208U
- #define [IOMUXC\\_GPIO\\_EMC\\_01\\_FLEXIO1\\_FLEXIO01](#) 0x401F8018U, 0x4U, 0, 0, 0x401F8208U
- #define [IOMUXC\\_GPIO\\_EMC\\_01\\_GPIO4\\_IO01](#) 0x401F8018U, 0x5U, 0, 0, 0x401F8208U
- #define [IOMUXC\\_GPIO\\_EMC\\_02\\_SEMC\\_DATA02](#) 0x401F801CU, 0x0U, 0, 0, 0x401F820CU
- #define [IOMUXC\\_GPIO\\_EMC\\_02\\_FLEXPWM4\\_PWMA01](#) 0x401F801CU, 0x1U, 0x401F8498U, 0x0U, 0x401F820CU
- #define [IOMUXC\\_GPIO\\_EMC\\_02\\_LPSPI2\\_SDO](#) 0x401F801CU, 0x2U, 0x401F8508U, 0x1U, 0x401F820CU

- #define **IOMUXC\_GPIO\_EMC\_02\_XBAR1\_INOUT04** 0x401F801CU, 0x3U, 0x401F8614U, 0x0U, 0x401F820CU
- #define **IOMUXC\_GPIO\_EMC\_02\_FLEXIO1\_FLEXIO02** 0x401F801CU, 0x4U, 0, 0, 0x401F820CU
- #define **IOMUXC\_GPIO\_EMC\_02\_GPIO4\_IO02** 0x401F801CU, 0x5U, 0, 0, 0x401F820CU
- #define **IOMUXC\_GPIO\_EMC\_03\_SEMC\_DATA03** 0x401F8020U, 0x0U, 0, 0, 0x401F8210U
- #define **IOMUXC\_GPIO\_EMC\_03\_FLEXPWM4\_PWMB01** 0x401F8020U, 0x1U, 0, 0, 0x401F8210U
- #define **IOMUXC\_GPIO\_EMC\_03\_LPSPi2\_SDI** 0x401F8020U, 0x2U, 0x401F8504U, 0x1U, 0x401F8210U
- #define **IOMUXC\_GPIO\_EMC\_03\_XBAR1\_INOUT05** 0x401F8020U, 0x3U, 0x401F8618U, 0x0U, 0x401F8210U
- #define **IOMUXC\_GPIO\_EMC\_03\_FLEXIO1\_FLEXIO03** 0x401F8020U, 0x4U, 0, 0, 0x401F8210U
- #define **IOMUXC\_GPIO\_EMC\_03\_GPIO4\_IO03** 0x401F8020U, 0x5U, 0, 0, 0x401F8210U
- #define **IOMUXC\_GPIO\_EMC\_04\_SEMC\_DATA04** 0x401F8024U, 0x0U, 0, 0, 0x401F8214U
- #define **IOMUXC\_GPIO\_EMC\_04\_FLEXPWM4\_PWMA02** 0x401F8024U, 0x1U, 0x401F849CU, 0x0U, 0x401F8214U
- #define **IOMUXC\_GPIO\_EMC\_04\_SAI2\_TX\_DATA** 0x401F8024U, 0x2U, 0, 0, 0x401F8214U
- #define **IOMUXC\_GPIO\_EMC\_04\_XBAR1\_INOUT06** 0x401F8024U, 0x3U, 0x401F861CU, 0x0U, 0x401F8214U
- #define **IOMUXC\_GPIO\_EMC\_04\_FLEXIO1\_FLEXIO04** 0x401F8024U, 0x4U, 0, 0, 0x401F8214U
- #define **IOMUXC\_GPIO\_EMC\_04\_GPIO4\_IO04** 0x401F8024U, 0x5U, 0, 0, 0x401F8214U
- #define **IOMUXC\_GPIO\_EMC\_05\_SEMC\_DATA05** 0x401F8028U, 0x0U, 0, 0, 0x401F8218U
- #define **IOMUXC\_GPIO\_EMC\_05\_FLEXPWM4\_PWMB02** 0x401F8028U, 0x1U, 0, 0, 0x401F8218U
- #define **IOMUXC\_GPIO\_EMC\_05\_SAI2\_TX\_SYNC** 0x401F8028U, 0x2U, 0x401F85C4U, 0x0U, 0x401F8218U
- #define **IOMUXC\_GPIO\_EMC\_05\_XBAR1\_INOUT07** 0x401F8028U, 0x3U, 0x401F8620U, 0x0U, 0x401F8218U
- #define **IOMUXC\_GPIO\_EMC\_05\_FLEXIO1\_FLEXIO05** 0x401F8028U, 0x4U, 0, 0, 0x401F8218U
- #define **IOMUXC\_GPIO\_EMC\_05\_GPIO4\_IO05** 0x401F8028U, 0x5U, 0, 0, 0x401F8218U
- #define **IOMUXC\_GPIO\_EMC\_06\_SEMC\_DATA06** 0x401F802CU, 0x0U, 0, 0, 0x401F821CU
- #define **IOMUXC\_GPIO\_EMC\_06\_FLEXPWM2\_PWMA00** 0x401F802CU, 0x1U, 0x401F8478U, 0x0U, 0x401F821CU
- #define **IOMUXC\_GPIO\_EMC\_06\_SAI2\_TX\_BCLK** 0x401F802CU, 0x2U, 0x401F85C0U, 0x0U, 0x401F821CU
- #define **IOMUXC\_GPIO\_EMC\_06\_XBAR1\_INOUT08** 0x401F802CU, 0x3U, 0x401F8624U, 0x0U, 0x401F821CU
- #define **IOMUXC\_GPIO\_EMC\_06\_FLEXIO1\_FLEXIO06** 0x401F802CU, 0x4U, 0, 0, 0x401F821CU
- #define **IOMUXC\_GPIO\_EMC\_06\_GPIO4\_IO06** 0x401F802CU, 0x5U, 0, 0, 0x401F821CU
- #define **IOMUXC\_GPIO\_EMC\_07\_SEMC\_DATA07** 0x401F8030U, 0x0U, 0, 0, 0x401F8220U
- #define **IOMUXC\_GPIO\_EMC\_07\_FLEXPWM2\_PWMB00** 0x401F8030U, 0x1U, 0x401F8488U, 0x0U, 0x401F8220U
- #define **IOMUXC\_GPIO\_EMC\_07\_SAI2\_MCLK** 0x401F8030U, 0x2U, 0x401F85B0U, 0x0U, 0x401F8220U
- #define **IOMUXC\_GPIO\_EMC\_07\_XBAR1\_INOUT09** 0x401F8030U, 0x3U, 0x401F8628U, 0x0U, 0x401F8220U

- #define **IOMUXC\_GPIO\_EMC\_07\_FLEXIO1\_FLEXIO07** 0x401F8030U, 0x4U, 0, 0, 0x401F8220U
- #define **IOMUXC\_GPIO\_EMC\_07\_GPIO4\_IO07** 0x401F8030U, 0x5U, 0, 0, 0x401F8220U
- #define **IOMUXC\_GPIO\_EMC\_08\_SEMC\_DM00** 0x401F8034U, 0x0U, 0, 0, 0x401F8224U
- #define **IOMUXC\_GPIO\_EMC\_08\_FLEXPWM2\_PWMA01** 0x401F8034U, 0x1U, 0x401F847CU, 0x0U, 0x401F8224U
- #define **IOMUXC\_GPIO\_EMC\_08\_SAI2\_RX\_DATA** 0x401F8034U, 0x2U, 0x401F85B8U, 0x0U, 0x401F8224U
- #define **IOMUXC\_GPIO\_EMC\_08\_XBAR1\_INOUT17** 0x401F8034U, 0x3U, 0x401F862CU, 0x0U, 0x401F8224U
- #define **IOMUXC\_GPIO\_EMC\_08\_FLEXIO1\_FLEXIO08** 0x401F8034U, 0x4U, 0, 0, 0x401F8224U
- #define **IOMUXC\_GPIO\_EMC\_08\_GPIO4\_IO08** 0x401F8034U, 0x5U, 0, 0, 0x401F8224U
- #define **IOMUXC\_GPIO\_EMC\_09\_SEMC\_ADDR00** 0x401F8038U, 0x0U, 0, 0, 0x401F8228U
- #define **IOMUXC\_GPIO\_EMC\_09\_FLEXPWM2\_PWMB01** 0x401F8038U, 0x1U, 0x401F848-CU, 0x0U, 0x401F8228U
- #define **IOMUXC\_GPIO\_EMC\_09\_SAI2\_RX\_SYNC** 0x401F8038U, 0x2U, 0x401F85BCU, 0x0U, 0x401F8228U
- #define **IOMUXC\_GPIO\_EMC\_09\_FLEXCAN2\_TX** 0x401F8038U, 0x3U, 0, 0, 0x401F8228U
- #define **IOMUXC\_GPIO\_EMC\_09\_FLEXIO1\_FLEXIO09** 0x401F8038U, 0x4U, 0, 0, 0x401F8228U
- #define **IOMUXC\_GPIO\_EMC\_09\_GPIO4\_IO09** 0x401F8038U, 0x5U, 0, 0, 0x401F8228U
- #define **IOMUXC\_GPIO\_EMC\_09\_FLEXSPI2\_B\_SS1\_B** 0x401F8038U, 0x8U, 0, 0, 0x401F8228U
- #define **IOMUXC\_GPIO\_EMC\_10\_SEMC\_ADDR01** 0x401F803CU, 0x0U, 0, 0, 0x401F822CU
- #define **IOMUXC\_GPIO\_EMC\_10\_FLEXPWM2\_PWMA02** 0x401F803CU, 0x1U, 0x401F8480U, 0x0U, 0x401F822CU
- #define **IOMUXC\_GPIO\_EMC\_10\_SAI2\_RX\_BCLK** 0x401F803CU, 0x2U, 0x401F85B4U, 0x0U, 0x401F822CU
- #define **IOMUXC\_GPIO\_EMC\_10\_FLEXCAN2\_RX** 0x401F803CU, 0x3U, 0x401F8450U, 0x0U, 0x401F822CU
- #define **IOMUXC\_GPIO\_EMC\_10\_FLEXIO1\_FLEXIO10** 0x401F803CU, 0x4U, 0, 0, 0x401F822CU
- #define **IOMUXC\_GPIO\_EMC\_10\_GPIO4\_IO10** 0x401F803CU, 0x5U, 0, 0, 0x401F822CU
- #define **IOMUXC\_GPIO\_EMC\_10\_FLEXSPI2\_B\_SS0\_B** 0x401F803CU, 0x8U, 0, 0, 0x401F822CU
- #define **IOMUXC\_GPIO\_EMC\_11\_SEMC\_ADDR02** 0x401F8040U, 0x0U, 0, 0, 0x401F8230U
- #define **IOMUXC\_GPIO\_EMC\_11\_FLEXPWM2\_PWMB02** 0x401F8040U, 0x1U, 0x401F8490U, 0x0U, 0x401F8230U
- #define **IOMUXC\_GPIO\_EMC\_11\_LPI2C4\_SDA** 0x401F8040U, 0x2U, 0x401F84E8U, 0x0U, 0x401F8230U
- #define **IOMUXC\_GPIO\_EMC\_11\_USDHC2\_RESET\_B** 0x401F8040U, 0x3U, 0, 0, 0x401F8230U
- #define **IOMUXC\_GPIO\_EMC\_11\_FLEXIO1\_FLEXIO11** 0x401F8040U, 0x4U, 0, 0, 0x401F8230U
- #define **IOMUXC\_GPIO\_EMC\_11\_GPIO4\_IO11** 0x401F8040U, 0x5U, 0, 0, 0x401F8230U
- #define **IOMUXC\_GPIO\_EMC\_11\_FLEXSPI2\_B\_DQS** 0x401F8040U, 0x8U, 0, 0, 0x401F8230U
- #define **IOMUXC\_GPIO\_EMC\_12\_SEMC\_ADDR03** 0x401F8044U, 0x0U, 0, 0, 0x401F8234U
- #define **IOMUXC\_GPIO\_EMC\_12\_XBAR1\_IN24** 0x401F8044U, 0x1U, 0x401F8640U, 0x0U, 0x401F8234U

- #define **IOMUXC\_GPIO\_EMC\_12\_LPI2C4\_SCL** 0x401F8044U, 0x2U, 0x401F84E4U, 0x0U, 0x401F8234U
- #define **IOMUXC\_GPIO\_EMC\_12\_USDHC1\_WP** 0x401F8044U, 0x3U, 0x401F85D8U, 0x0U, 0x401F8234U
- #define **IOMUXC\_GPIO\_EMC\_12\_FLEXPWM1\_PWMA03** 0x401F8044U, 0x4U, 0x401F8454U, 0x1U, 0x401F8234U
- #define **IOMUXC\_GPIO\_EMC\_12\_GPIO4\_IO12** 0x401F8044U, 0x5U, 0, 0, 0x401F8234U
- #define **IOMUXC\_GPIO\_EMC\_12\_FLEXSPI2\_B\_SCLK** 0x401F8044U, 0x8U, 0x401F8754U, 0x0U, 0x401F8234U
- #define **IOMUXC\_GPIO\_EMC\_13\_SEMC\_ADDR04** 0x401F8048U, 0x0U, 0, 0, 0x401F8238U
- #define **IOMUXC\_GPIO\_EMC\_13\_XBAR1\_IN25** 0x401F8048U, 0x1U, 0x401F8650U, 0x1U, 0x401F8238U
- #define **IOMUXC\_GPIO\_EMC\_13\_LPUART3\_TX** 0x401F8048U, 0x2U, 0x401F853CU, 0x1U, 0x401F8238U
- #define **IOMUXC\_GPIO\_EMC\_13\_MQS\_RIGHT** 0x401F8048U, 0x3U, 0, 0, 0x401F8238U
- #define **IOMUXC\_GPIO\_EMC\_13\_FLEXPWM1\_PWMB03** 0x401F8048U, 0x4U, 0x401F8464U, 0x1U, 0x401F8238U
- #define **IOMUXC\_GPIO\_EMC\_13\_GPIO4\_IO13** 0x401F8048U, 0x5U, 0, 0, 0x401F8238U
- #define **IOMUXC\_GPIO\_EMC\_13\_FLEXSPI2\_B\_DATA00** 0x401F8048U, 0x8U, 0x401F8740U, 0x0U, 0x401F8238U
- #define **IOMUXC\_GPIO\_EMC\_14\_SEMC\_ADDR05** 0x401F804CU, 0x0U, 0, 0, 0x401F823CU
- #define **IOMUXC\_GPIO\_EMC\_14\_XBAR1\_INOUT19** 0x401F804CU, 0x1U, 0x401F8654U, 0x0U, 0x401F823CU
- #define **IOMUXC\_GPIO\_EMC\_14\_LPUART3\_RX** 0x401F804CU, 0x2U, 0x401F8538U, 0x1U, 0x401F823CU
- #define **IOMUXC\_GPIO\_EMC\_14\_MQS\_LEFT** 0x401F804CU, 0x3U, 0, 0, 0x401F823CU
- #define **IOMUXC\_GPIO\_EMC\_14\_LPSPI2\_PCS1** 0x401F804CU, 0x4U, 0, 0, 0x401F823CU
- #define **IOMUXC\_GPIO\_EMC\_14\_GPIO4\_IO14** 0x401F804CU, 0x5U, 0, 0, 0x401F823CU
- #define **IOMUXC\_GPIO\_EMC\_14\_FLEXSPI2\_B\_DATA01** 0x401F804CU, 0x8U, 0x401F8744U, 0x0U, 0x401F823CU
- #define **IOMUXC\_GPIO\_EMC\_15\_SEMC\_ADDR06** 0x401F8050U, 0x0U, 0, 0, 0x401F8240U
- #define **IOMUXC\_GPIO\_EMC\_15\_XBAR1\_IN20** 0x401F8050U, 0x1U, 0x401F8634U, 0x0U, 0x401F8240U
- #define **IOMUXC\_GPIO\_EMC\_15\_LPUART3\_CTS\_B** 0x401F8050U, 0x2U, 0x401F8534U, 0x0U, 0x401F8240U
- #define **IOMUXC\_GPIO\_EMC\_15\_SPDIF\_OUT** 0x401F8050U, 0x3U, 0, 0, 0x401F8240U
- #define **IOMUXC\_GPIO\_EMC\_15\_QTIMER3\_TIMER0** 0x401F8050U, 0x4U, 0x401F857CU, 0x0U, 0x401F8240U
- #define **IOMUXC\_GPIO\_EMC\_15\_GPIO4\_IO15** 0x401F8050U, 0x5U, 0, 0, 0x401F8240U
- #define **IOMUXC\_GPIO\_EMC\_15\_FLEXSPI2\_B\_DATA02** 0x401F8050U, 0x8U, 0x401F8748U, 0x0U, 0x401F8240U
- #define **IOMUXC\_GPIO\_EMC\_16\_SEMC\_ADDR07** 0x401F8054U, 0x0U, 0, 0, 0x401F8244U
- #define **IOMUXC\_GPIO\_EMC\_16\_XBAR1\_IN21** 0x401F8054U, 0x1U, 0x401F8658U, 0x0U, 0x401F8244U
- #define **IOMUXC\_GPIO\_EMC\_16\_LPUART3\_RTS\_B** 0x401F8054U, 0x2U, 0, 0, 0x401F8244U
- #define **IOMUXC\_GPIO\_EMC\_16\_SPDIF\_IN** 0x401F8054U, 0x3U, 0x401F85C8U, 0x1U, 0x401F8244U
- #define **IOMUXC\_GPIO\_EMC\_16\_QTIMER3\_TIMER1** 0x401F8054U, 0x4U, 0x401F8580U, 0x1U, 0x401F8244U
- #define **IOMUXC\_GPIO\_EMC\_16\_GPIO4\_IO16** 0x401F8054U, 0x5U, 0, 0, 0x401F8244U

- #define **IOMUXC\_GPIO\_EMC\_16\_FLEXSPI2\_B\_DATA03** 0x401F8054U, 0x8U, 0x401F874-CU, 0x0U, 0x401F8244U
- #define **IOMUXC\_GPIO\_EMC\_17\_SEMC\_ADDR08** 0x401F8058U, 0x0U, 0, 0, 0x401F8248U
- #define **IOMUXC\_GPIO\_EMC\_17\_FLEXPWM4\_PWMA03** 0x401F8058U, 0x1U, 0x401F84-A0U, 0x0U, 0x401F8248U
- #define **IOMUXC\_GPIO\_EMC\_17\_LPUART4\_CTS\_B** 0x401F8058U, 0x2U, 0, 0, 0x401F8248U
- #define **IOMUXC\_GPIO\_EMC\_17\_FLEXCAN1\_TX** 0x401F8058U, 0x3U, 0, 0, 0x401F8248U
- #define **IOMUXC\_GPIO\_EMC\_17\_QTIMER3\_TIMER2** 0x401F8058U, 0x4U, 0x401F8584U, 0x0U, 0x401F8248U
- #define **IOMUXC\_GPIO\_EMC\_17\_GPIO4\_IO17** 0x401F8058U, 0x5U, 0, 0, 0x401F8248U
- #define **IOMUXC\_GPIO\_EMC\_18\_SEMC\_ADDR09** 0x401F805CU, 0x0U, 0, 0, 0x401F824CU
- #define **IOMUXC\_GPIO\_EMC\_18\_FLEXPWM4\_PWMB03** 0x401F805CU, 0x1U, 0, 0, 0x401F824CU
- #define **IOMUXC\_GPIO\_EMC\_18\_LPUART4 RTS\_B** 0x401F805CU, 0x2U, 0, 0, 0x401F824-CU
- #define **IOMUXC\_GPIO\_EMC\_18\_FLEXCAN1\_RX** 0x401F805CU, 0x3U, 0x401F844CU, 0x1U, 0x401F824CU
- #define **IOMUXC\_GPIO\_EMC\_18\_QTIMER3\_TIMER3** 0x401F805CU, 0x4U, 0x401F8588U, 0x0U, 0x401F824CU
- #define **IOMUXC\_GPIO\_EMC\_18\_GPIO4\_IO18** 0x401F805CU, 0x5U, 0, 0, 0x401F824CU
- #define **IOMUXC\_GPIO\_EMC\_18\_SNVS\_VIO\_5\_CTL** 0x401F805CU, 0x6U, 0, 0, 0x401F824CU
- #define **IOMUXC\_GPIO\_EMC\_19\_SEMC\_ADDR11** 0x401F8060U, 0x0U, 0, 0, 0x401F8250U
- #define **IOMUXC\_GPIO\_EMC\_19\_FLEXPWM2\_PWMA03** 0x401F8060U, 0x1U, 0x401F8474U, 0x1U, 0x401F8250U
- #define **IOMUXC\_GPIO\_EMC\_19\_LPUART4\_TX** 0x401F8060U, 0x2U, 0x401F8544U, 0x1U, 0x401F8250U
- #define **IOMUXC\_GPIO\_EMC\_19\_ENET\_RDATA01** 0x401F8060U, 0x3U, 0x401F8438U, 0x0U, 0x401F8250U
- #define **IOMUXC\_GPIO\_EMC\_19\_QTIMER2\_TIMER0** 0x401F8060U, 0x4U, 0x401F856CU, 0x0U, 0x401F8250U
- #define **IOMUXC\_GPIO\_EMC\_19\_GPIO4\_IO19** 0x401F8060U, 0x5U, 0, 0, 0x401F8250U
- #define **IOMUXC\_GPIO\_EMC\_19\_SNVS\_VIO\_5** 0x401F8060U, 0x6U, 0, 0, 0x401F8250U
- #define **IOMUXC\_GPIO\_EMC\_20\_SEMC\_ADDR12** 0x401F8064U, 0x0U, 0, 0, 0x401F8254U
- #define **IOMUXC\_GPIO\_EMC\_20\_FLEXPWM2\_PWMB03** 0x401F8064U, 0x1U, 0x401F8484U, 0x1U, 0x401F8254U
- #define **IOMUXC\_GPIO\_EMC\_20\_LPUART4\_RX** 0x401F8064U, 0x2U, 0x401F8540U, 0x1U, 0x401F8254U
- #define **IOMUXC\_GPIO\_EMC\_20\_ENET\_RDATA00** 0x401F8064U, 0x3U, 0x401F8434U, 0x0U, 0x401F8254U
- #define **IOMUXC\_GPIO\_EMC\_20\_QTIMER2\_TIMER1** 0x401F8064U, 0x4U, 0x401F8570U, 0x0U, 0x401F8254U
- #define **IOMUXC\_GPIO\_EMC\_20\_GPIO4\_IO20** 0x401F8064U, 0x5U, 0, 0, 0x401F8254U
- #define **IOMUXC\_GPIO\_EMC\_21\_SEMC\_BA0** 0x401F8068U, 0x0U, 0, 0, 0x401F8258U
- #define **IOMUXC\_GPIO\_EMC\_21\_FLEXPWM3\_PWMA03** 0x401F8068U, 0x1U, 0, 0, 0x401F8258U
- #define **IOMUXC\_GPIO\_EMC\_21\_LPI2C3\_SDA** 0x401F8068U, 0x2U, 0x401F84E0U, 0x0U, 0x401F8258U
- #define **IOMUXC\_GPIO\_EMC\_21\_ENET\_TDATA01** 0x401F8068U, 0x3U, 0, 0, 0x401F8258-U

- #define **IOMUXC\_GPIO\_EMC\_21\_QTIMER2\_TIMER2** 0x401F8068U, 0x4U, 0x401F8574U, 0x0U, 0x401F8258U
- #define **IOMUXC\_GPIO\_EMC\_21\_GPIO4\_IO21** 0x401F8068U, 0x5U, 0, 0, 0x401F8258U
- #define **IOMUXC\_GPIO\_EMC\_22\_SEMC\_BA1** 0x401F806CU, 0x0U, 0, 0, 0x401F825CU
- #define **IOMUXC\_GPIO\_EMC\_22\_FLEXPWM3\_PWMB03** 0x401F806CU, 0x1U, 0, 0, 0x401F825CU
- #define **IOMUXC\_GPIO\_EMC\_22\_LPI2C3\_SCL** 0x401F806CU, 0x2U, 0x401F84DCU, 0x0U, 0x401F825CU
- #define **IOMUXC\_GPIO\_EMC\_22\_ENET\_TDATA00** 0x401F806CU, 0x3U, 0, 0, 0x401F825CU
- #define **IOMUXC\_GPIO\_EMC\_22\_QTIMER2\_TIMER3** 0x401F806CU, 0x4U, 0x401F8578U, 0x0U, 0x401F825CU
- #define **IOMUXC\_GPIO\_EMC\_22\_GPIO4\_IO22** 0x401F806CU, 0x5U, 0, 0, 0x401F825CU
- #define **IOMUXC\_GPIO\_EMC\_22\_FLEXSPI2\_A\_SS1\_B** 0x401F806CU, 0x8U, 0, 0, 0x401F825CU
- #define **IOMUXC\_GPIO\_EMC\_23\_SEMC\_ADDR10** 0x401F8070U, 0x0U, 0, 0, 0x401F8260U
- #define **IOMUXC\_GPIO\_EMC\_23\_FLEXPWM1\_PWMA00** 0x401F8070U, 0x1U, 0x401F8458U, 0x0U, 0x401F8260U
- #define **IOMUXC\_GPIO\_EMC\_23\_LPUART5\_TX** 0x401F8070U, 0x2U, 0x401F854CU, 0x0U, 0x401F8260U
- #define **IOMUXC\_GPIO\_EMC\_23\_ENET\_RX\_EN** 0x401F8070U, 0x3U, 0x401F843CU, 0x0U, 0x401F8260U
- #define **IOMUXC\_GPIO\_EMC\_23\_GPT1\_CAPTURE2** 0x401F8070U, 0x4U, 0x401F875CU, 0x0U, 0x401F8260U
- #define **IOMUXC\_GPIO\_EMC\_23\_GPIO4\_IO23** 0x401F8070U, 0x5U, 0, 0, 0x401F8260U
- #define **IOMUXC\_GPIO\_EMC\_23\_FLEXSPI2\_A\_DQS** 0x401F8070U, 0x8U, 0x401F872CU, 0x1U, 0x401F8260U
- #define **IOMUXC\_GPIO\_EMC\_24\_SEMC\_CAS** 0x401F8074U, 0x0U, 0, 0, 0x401F8264U
- #define **IOMUXC\_GPIO\_EMC\_24\_FLEXPWM1\_PWMB00** 0x401F8074U, 0x1U, 0x401F8468U, 0x0U, 0x401F8264U
- #define **IOMUXC\_GPIO\_EMC\_24\_LPUART5\_RX** 0x401F8074U, 0x2U, 0x401F8548U, 0x0U, 0x401F8264U
- #define **IOMUXC\_GPIO\_EMC\_24\_ENET\_TX\_EN** 0x401F8074U, 0x3U, 0, 0, 0x401F8264U
- #define **IOMUXC\_GPIO\_EMC\_24\_GPT1\_CAPTURE1** 0x401F8074U, 0x4U, 0x401F8758U, 0x0U, 0x401F8264U
- #define **IOMUXC\_GPIO\_EMC\_24\_GPIO4\_IO24** 0x401F8074U, 0x5U, 0, 0, 0x401F8264U
- #define **IOMUXC\_GPIO\_EMC\_24\_FLEXSPI2\_A\_SS0\_B** 0x401F8074U, 0x8U, 0, 0, 0x401F8264U
- #define **IOMUXC\_GPIO\_EMC\_25\_SEMC\_RAS** 0x401F8078U, 0x0U, 0, 0, 0x401F8268U
- #define **IOMUXC\_GPIO\_EMC\_25\_FLEXPWM1\_PWMA01** 0x401F8078U, 0x1U, 0x401F845CU, 0x0U, 0x401F8268U
- #define **IOMUXC\_GPIO\_EMC\_25\_LPUART6\_TX** 0x401F8078U, 0x2U, 0x401F8554U, 0x0U, 0x401F8268U
- #define **IOMUXC\_GPIO\_EMC\_25\_ENET\_TX\_CLK** 0x401F8078U, 0x3U, 0x401F8448U, 0x0U, 0x401F8268U
- #define **IOMUXC\_GPIO\_EMC\_25\_ENET\_REF\_CLK** 0x401F8078U, 0x4U, 0x401F842CU, 0x0U, 0x401F8268U
- #define **IOMUXC\_GPIO\_EMC\_25\_GPIO4\_IO25** 0x401F8078U, 0x5U, 0, 0, 0x401F8268U
- #define **IOMUXC\_GPIO\_EMC\_25\_FLEXSPI2\_A\_SCLK** 0x401F8078U, 0x8U, 0x401F8750U, 0x1U, 0x401F8268U
- #define **IOMUXC\_GPIO\_EMC\_26\_SEMC\_CLK** 0x401F807CU, 0x0U, 0, 0, 0x401F826CU

- #define **IOMUXC\_GPIO\_EMC\_26\_FLEXPWM1\_PWMB01** 0x401F807CU, 0x1U, 0x401F846CU, 0x0U, 0x401F826CU
- #define **IOMUXC\_GPIO\_EMC\_26\_LPUART6\_RX** 0x401F807CU, 0x2U, 0x401F8550U, 0x0U, 0x401F826CU
- #define **IOMUXC\_GPIO\_EMC\_26\_ENET\_RX\_ER** 0x401F807CU, 0x3U, 0x401F8440U, 0x0U, 0x401F826CU
- #define **IOMUXC\_GPIO\_EMC\_26\_FLEXIO1\_FLEXIO12** 0x401F807CU, 0x4U, 0, 0, 0x401F826CU
- #define **IOMUXC\_GPIO\_EMC\_26\_GPIO4\_IO26** 0x401F807CU, 0x5U, 0, 0, 0x401F826CU
- #define **IOMUXC\_GPIO\_EMC\_26\_FLEXSPI2\_A\_DATA00** 0x401F807CU, 0x8U, 0x401F8730U, 0x1U, 0x401F826CU
- #define **IOMUXC\_GPIO\_EMC\_27\_SEMC\_CKE** 0x401F8080U, 0x0U, 0, 0, 0x401F8270U
- #define **IOMUXC\_GPIO\_EMC\_27\_FLEXPWM1\_PWMA02** 0x401F8080U, 0x1U, 0x401F8460U, 0x0U, 0x401F8270U
- #define **IOMUXC\_GPIO\_EMC\_27\_LPUART5\_RTS\_B** 0x401F8080U, 0x2U, 0, 0, 0x401F8270U
- #define **IOMUXC\_GPIO\_EMC\_27\_LPSP1\_SCK** 0x401F8080U, 0x3U, 0x401F84FOU, 0x0U, 0x401F8270U
- #define **IOMUXC\_GPIO\_EMC\_27\_FLEXIO1\_FLEXIO13** 0x401F8080U, 0x4U, 0, 0, 0x401F8270U
- #define **IOMUXC\_GPIO\_EMC\_27\_GPIO4\_IO27** 0x401F8080U, 0x5U, 0, 0, 0x401F8270U
- #define **IOMUXC\_GPIO\_EMC\_27\_FLEXSPI2\_A\_DATA01** 0x401F8080U, 0x8U, 0x401F8734U, 0x1U, 0x401F8270U
- #define **IOMUXC\_GPIO\_EMC\_28\_SEMC\_WE** 0x401F8084U, 0x0U, 0, 0, 0x401F8274U
- #define **IOMUXC\_GPIO\_EMC\_28\_FLEXPWM1\_PWMB02** 0x401F8084U, 0x1U, 0x401F8470U, 0x0U, 0x401F8274U
- #define **IOMUXC\_GPIO\_EMC\_28\_LPUART5\_CTS\_B** 0x401F8084U, 0x2U, 0, 0, 0x401F8274U
- #define **IOMUXC\_GPIO\_EMC\_28\_LPSP1\_SDO** 0x401F8084U, 0x3U, 0x401F84F8U, 0x0U, 0x401F8274U
- #define **IOMUXC\_GPIO\_EMC\_28\_FLEXIO1\_FLEXIO14** 0x401F8084U, 0x4U, 0, 0, 0x401F8274U
- #define **IOMUXC\_GPIO\_EMC\_28\_GPIO4\_IO28** 0x401F8084U, 0x5U, 0, 0, 0x401F8274U
- #define **IOMUXC\_GPIO\_EMC\_28\_FLEXSPI2\_A\_DATA02** 0x401F8084U, 0x8U, 0x401F8738U, 0x1U, 0x401F8274U
- #define **IOMUXC\_GPIO\_EMC\_29\_SEMC\_CS0** 0x401F8088U, 0x0U, 0, 0, 0x401F8278U
- #define **IOMUXC\_GPIO\_EMC\_29\_FLEXPWM3\_PWMA00** 0x401F8088U, 0x1U, 0, 0, 0x401F8278U
- #define **IOMUXC\_GPIO\_EMC\_29\_LPUART6\_RTS\_B** 0x401F8088U, 0x2U, 0, 0, 0x401F8278U
- #define **IOMUXC\_GPIO\_EMC\_29\_LPSP1\_SDI** 0x401F8088U, 0x3U, 0x401F84F4U, 0x0U, 0x401F8278U
- #define **IOMUXC\_GPIO\_EMC\_29\_FLEXIO1\_FLEXIO15** 0x401F8088U, 0x4U, 0, 0, 0x401F8278U
- #define **IOMUXC\_GPIO\_EMC\_29\_GPIO4\_IO29** 0x401F8088U, 0x5U, 0, 0, 0x401F8278U
- #define **IOMUXC\_GPIO\_EMC\_29\_FLEXSPI2\_A\_DATA03** 0x401F8088U, 0x8U, 0x401F873CU, 0x1U, 0x401F8278U
- #define **IOMUXC\_GPIO\_EMC\_30\_SEMC\_DATA08** 0x401F808CU, 0x0U, 0, 0, 0x401F827CU
- #define **IOMUXC\_GPIO\_EMC\_30\_FLEXPWM3\_PWMB00** 0x401F808CU, 0x1U, 0, 0, 0x401F827CU
- #define **IOMUXC\_GPIO\_EMC\_30\_LPUART6\_CTS\_B** 0x401F808CU, 0x2U, 0, 0, 0x401F827-

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- #define **IOMUXC\_GPIO\_EMC\_30\_LPSPI1\_PCS0** 0x401F808CU, 0x3U, 0x401F84ECU, 0x1-U, 0x401F827CU
- #define **IOMUXC\_GPIO\_EMC\_30\_GPIO4\_IO30** 0x401F808CU, 0x5U, 0, 0, 0x401F827CU
- #define **IOMUXC\_GPIO\_EMC\_31\_SEMC\_DATA09** 0x401F8090U, 0x0U, 0, 0, 0x401F8280U
- #define **IOMUXC\_GPIO\_EMC\_31\_FLEXPWM3\_PWMA01** 0x401F8090U, 0x1U, 0, 0, 0x401-F8280U
- #define **IOMUXC\_GPIO\_EMC\_31\_LPUART7\_TX** 0x401F8090U, 0x2U, 0x401F855CU, 0x1-U, 0x401F8280U
- #define **IOMUXC\_GPIO\_EMC\_31\_LPSPI1\_PCS1** 0x401F8090U, 0x3U, 0, 0, 0x401F8280U
- #define **IOMUXC\_GPIO\_EMC\_31\_GPIO4\_IO31** 0x401F8090U, 0x5U, 0, 0, 0x401F8280U
- #define **IOMUXC\_GPIO\_EMC\_32\_SEMC\_DATA10** 0x401F8094U, 0x0U, 0, 0, 0x401F8284U
- #define **IOMUXC\_GPIO\_EMC\_32\_FLEXPWM3\_PWMB01** 0x401F8094U, 0x1U, 0, 0, 0x401-F8284U
- #define **IOMUXC\_GPIO\_EMC\_32\_LPUART7\_RX** 0x401F8094U, 0x2U, 0x401F8558U, 0x1U, 0x401F8284U
- #define **IOMUXC\_GPIO\_EMC\_32\_CCM\_PMIC\_RDY** 0x401F8094U, 0x3U, 0x401F83FCU, 0x4U, 0x401F8284U
- #define **IOMUXC\_GPIO\_EMC\_32\_GPIO3\_IO18** 0x401F8094U, 0x5U, 0, 0, 0x401F8284U
- #define **IOMUXC\_GPIO\_EMC\_33\_SEMC\_DATA11** 0x401F8098U, 0x0U, 0, 0, 0x401F8288U
- #define **IOMUXC\_GPIO\_EMC\_33\_FLEXPWM3\_PWMA02** 0x401F8098U, 0x1U, 0, 0, 0x401-F8288U
- #define **IOMUXC\_GPIO\_EMC\_33\_USDHC1\_RESET\_B** 0x401F8098U, 0x2U, 0, 0, 0x401-F8288U
- #define **IOMUXC\_GPIO\_EMC\_33\_SAI3\_RX\_DATA** 0x401F8098U, 0x3U, 0x401F8778U, 0x0U, 0x401F8288U
- #define **IOMUXC\_GPIO\_EMC\_33\_GPIO3\_IO19** 0x401F8098U, 0x5U, 0, 0, 0x401F8288U
- #define **IOMUXC\_GPIO\_EMC\_34\_SEMC\_DATA12** 0x401F809CU, 0x0U, 0, 0, 0x401F828CU
- #define **IOMUXC\_GPIO\_EMC\_34\_FLEXPWM3\_PWMB02** 0x401F809CU, 0x1U, 0, 0, 0x401F828CU
- #define **IOMUXC\_GPIO\_EMC\_34\_USDHC1\_VSELECT** 0x401F809CU, 0x2U, 0, 0, 0x401-F828CU
- #define **IOMUXC\_GPIO\_EMC\_34\_SAI3\_RX\_SYNC** 0x401F809CU, 0x3U, 0x401F877CU, 0x0U, 0x401F828CU
- #define **IOMUXC\_GPIO\_EMC\_34\_GPIO3\_IO20** 0x401F809CU, 0x5U, 0, 0, 0x401F828CU
- #define **IOMUXC\_GPIO\_EMC\_35\_SEMC\_DATA13** 0x401F80A0U, 0x0U, 0, 0, 0x401F8290U
- #define **IOMUXC\_GPIO\_EMC\_35\_XBAR1\_INOUT18** 0x401F80A0U, 0x1U, 0x401F8630U, 0x0U, 0x401F8290U
- #define **IOMUXC\_GPIO\_EMC\_35\_GPT1\_COMPARE1** 0x401F80A0U, 0x2U, 0, 0, 0x401-F8290U
- #define **IOMUXC\_GPIO\_EMC\_35\_SAI3\_RX\_BCLK** 0x401F80A0U, 0x3U, 0x401F8774U, 0x0U, 0x401F8290U
- #define **IOMUXC\_GPIO\_EMC\_35\_GPIO3\_IO21** 0x401F80A0U, 0x5U, 0, 0, 0x401F8290U
- #define **IOMUXC\_GPIO\_EMC\_35\_USDHC1\_CD\_B** 0x401F80A0U, 0x6U, 0x401F85D4U, 0x0U, 0x401F8290U
- #define **IOMUXC\_GPIO\_EMC\_36\_SEMC\_DATA14** 0x401F80A4U, 0x0U, 0, 0, 0x401F8294U
- #define **IOMUXC\_GPIO\_EMC\_36\_XBAR1\_IN22** 0x401F80A4U, 0x1U, 0x401F8638U, 0x0U, 0x401F8294U
- #define **IOMUXC\_GPIO\_EMC\_36\_GPT1\_COMPARE2** 0x401F80A4U, 0x2U, 0, 0, 0x401-F8294U
- #define **IOMUXC\_GPIO\_EMC\_36\_SAI3\_TX\_DATA** 0x401F80A4U, 0x3U, 0, 0, 0x401F8294U

- #define **IOMUXC\_GPIO\_EMC\_36\_GPIO3\_IO22** 0x401F80A4U, 0x5U, 0, 0, 0x401F8294U
- #define **IOMUXC\_GPIO\_EMC\_36\_USDHC1\_WP** 0x401F80A4U, 0x6U, 0x401F85D8U, 0x1U, 0x401F8294U
- #define **IOMUXC\_GPIO\_EMC\_36\_FLEXCAN3\_TX** 0x401F80A4U, 0x9U, 0, 0, 0x401F8294U
- #define **IOMUXC\_GPIO\_EMC\_37\_SEMC\_DATA15** 0x401F80A8U, 0x0U, 0, 0, 0x401F8298U
- #define **IOMUXC\_GPIO\_EMC\_37\_XBAR1\_IN23** 0x401F80A8U, 0x1U, 0x401F863CU, 0x0U, 0x401F8298U
- #define **IOMUXC\_GPIO\_EMC\_37\_GPT1\_COMPARE3** 0x401F80A8U, 0x2U, 0, 0, 0x401F8298U
- #define **IOMUXC\_GPIO\_EMC\_37\_SAI3\_MCLK** 0x401F80A8U, 0x3U, 0x401F8770U, 0x0U, 0x401F8298U
- #define **IOMUXC\_GPIO\_EMC\_37\_GPIO3\_IO23** 0x401F80A8U, 0x5U, 0, 0, 0x401F8298U
- #define **IOMUXC\_GPIO\_EMC\_37\_USDHC2\_WP** 0x401F80A8U, 0x6U, 0x401F8608U, 0x0U, 0x401F8298U
- #define **IOMUXC\_GPIO\_EMC\_37\_FLEXCAN3\_RX** 0x401F80A8U, 0x9U, 0x401F878CU, 0x0U, 0x401F8298U
- #define **IOMUXC\_GPIO\_EMC\_38\_SEMC\_DM01** 0x401F80ACU, 0x0U, 0, 0, 0x401F829CU
- #define **IOMUXC\_GPIO\_EMC\_38\_FLEXPWM1\_PWMA03** 0x401F80ACU, 0x1U, 0x401F8454U, 0x2U, 0x401F829CU
- #define **IOMUXC\_GPIO\_EMC\_38\_LPUART8\_TX** 0x401F80ACU, 0x2U, 0x401F8564U, 0x2U, 0x401F829CU
- #define **IOMUXC\_GPIO\_EMC\_38\_SAI3\_TX\_BCLK** 0x401F80ACU, 0x3U, 0x401F8780U, 0x0U, 0x401F829CU
- #define **IOMUXC\_GPIO\_EMC\_38\_GPIO3\_IO24** 0x401F80ACU, 0x5U, 0, 0, 0x401F829CU
- #define **IOMUXC\_GPIO\_EMC\_38\_USDHC2\_VSELECT** 0x401F80ACU, 0x6U, 0, 0, 0x401F829CU
- #define **IOMUXC\_GPIO\_EMC\_39\_SEMC\_DQS** 0x401F80B0U, 0x0U, 0, 0, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_39\_FLEXPWM1\_PWMB03** 0x401F80B0U, 0x1U, 0x401F8464U, 0x2U, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_39\_LPUART8\_RX** 0x401F80B0U, 0x2U, 0x401F8560U, 0x2U, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_39\_SAI3\_TX\_SYNC** 0x401F80B0U, 0x3U, 0x401F8784U, 0x0U, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_39\_WDOG1\_WDOG\_B** 0x401F80B0U, 0x4U, 0, 0, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_39\_GPIO3\_IO25** 0x401F80B0U, 0x5U, 0, 0, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_39\_USDHC2\_CD\_B** 0x401F80B0U, 0x6U, 0x401F85E0U, 0x1U, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_39\_SEMC\_DQS4** 0x401F80B0U, 0x9U, 0x401F8788U, 0x1U, 0x401F82A0U
- #define **IOMUXC\_GPIO\_EMC\_40\_SEMC\_RDY** 0x401F80B4U, 0x0U, 0, 0, 0x401F82A4U
- #define **IOMUXC\_GPIO\_EMC\_40\_GPT2\_CAPTURE2** 0x401F80B4U, 0x1U, 0x401F8768U, 0x0U, 0x401F82A4U
- #define **IOMUXC\_GPIO\_EMC\_40\_LPSPI1\_PCS2** 0x401F80B4U, 0x2U, 0, 0, 0x401F82A4U
- #define **IOMUXC\_GPIO\_EMC\_40\_ENET\_MDC** 0x401F80B4U, 0x4U, 0, 0, 0x401F82A4U
- #define **IOMUXC\_GPIO\_EMC\_40\_GPIO3\_IO26** 0x401F80B4U, 0x5U, 0, 0, 0x401F82A4U
- #define **IOMUXC\_GPIO\_EMC\_40\_USDHC2\_RESET\_B** 0x401F80B4U, 0x6U, 0, 0, 0x401F82A4U
- #define **IOMUXC\_GPIO\_EMC\_40\_SEMC\_CLK5** 0x401F80B4U, 0x9U, 0, 0, 0x401F82A4U
- #define **IOMUXC\_GPIO\_EMC\_41\_SEMC\_CSX00** 0x401F80B8U, 0x0U, 0, 0, 0x401F82A8U
- #define **IOMUXC\_GPIO\_EMC\_41\_GPT2\_CAPTURE1** 0x401F80B8U, 0x1U, 0x401F8764U,

- 0x0U, 0x401F82A8U
- #define **IOMUXC\_GPIO\_EMC\_41\_LPSP11\_PCS3** 0x401F80B8U, 0x2U, 0, 0, 0x401F82A8U
- #define **IOMUXC\_GPIO\_EMC\_41\_ENET\_MDIO** 0x401F80B8U, 0x4U, 0x401F8430U, 0x1U, 0x401F82A8U
- #define **IOMUXC\_GPIO\_EMC\_41\_GPIO3\_IO27** 0x401F80B8U, 0x5U, 0, 0, 0x401F82A8U
- #define **IOMUXC\_GPIO\_EMC\_41\_USDHC1\_VSELECT** 0x401F80B8U, 0x6U, 0, 0, 0x401F82A8U
- #define **IOMUXC\_GPIO\_AD\_B0\_04\_SRC\_BOOT\_MODE00** 0x401F80CCU, 0x0U, 0, 0, 0x401F82BCU
- #define **IOMUXC\_GPIO\_AD\_B0\_04\_MQS\_RIGHT** 0x401F80CCU, 0x1U, 0, 0, 0x401F82BCU
- #define **IOMUXC\_GPIO\_AD\_B0\_04\_ENET\_TX\_DATA03** 0x401F80CCU, 0x2U, 0, 0, 0x401F82BCU
- #define **IOMUXC\_GPIO\_AD\_B0\_04\_SAI2\_TX\_SYNC** 0x401F80CCU, 0x3U, 0x401F85C4U, 0x1U, 0x401F82BCU
- #define **IOMUXC\_GPIO\_AD\_B0\_04\_GPIO1\_IO04** 0x401F80CCU, 0x5U, 0, 0, 0x401F82BCU
- #define **IOMUXC\_GPIO\_AD\_B0\_04\_PIT\_TRIGGER00** 0x401F80CCU, 0x6U, 0, 0, 0x401F82BCU
- #define **IOMUXC\_GPIO\_AD\_B0\_05\_SRC\_BOOT\_MODE01** 0x401F80D0U, 0x0U, 0, 0, 0x401F82C0U
- #define **IOMUXC\_GPIO\_AD\_B0\_05\_MQS\_LEFT** 0x401F80D0U, 0x1U, 0, 0, 0x401F82C0U
- #define **IOMUXC\_GPIO\_AD\_B0\_05\_ENET\_TX\_DATA02** 0x401F80D0U, 0x2U, 0, 0, 0x401F82C0U
- #define **IOMUXC\_GPIO\_AD\_B0\_05\_SAI2\_TX\_BCLK** 0x401F80D0U, 0x3U, 0x401F85C0U, 0x1U, 0x401F82C0U
- #define **IOMUXC\_GPIO\_AD\_B0\_05\_GPIO1\_IO05** 0x401F80D0U, 0x5U, 0, 0, 0x401F82C0U
- #define **IOMUXC\_GPIO\_AD\_B0\_05\_XBAR1\_INOUT17** 0x401F80D0U, 0x6U, 0x401F862CU, 0x2U, 0x401F82C0U
- #define **IOMUXC\_GPIO\_AD\_B0\_06\_JTAG\_TMS** 0x401F80D4U, 0x0U, 0, 0, 0x401F82C4U
- #define **IOMUXC\_GPIO\_AD\_B0\_06\_GPT2\_COMPARE1** 0x401F80D4U, 0x1U, 0, 0, 0x401F82C4U
- #define **IOMUXC\_GPIO\_AD\_B0\_06\_ENET\_RX\_CLK** 0x401F80D4U, 0x2U, 0, 0, 0x401F82C4U
- #define **IOMUXC\_GPIO\_AD\_B0\_06\_SAI2\_RX\_BCLK** 0x401F80D4U, 0x3U, 0x401F85B4U, 0x1U, 0x401F82C4U
- #define **IOMUXC\_GPIO\_AD\_B0\_06\_GPIO1\_IO06** 0x401F80D4U, 0x5U, 0, 0, 0x401F82C4U
- #define **IOMUXC\_GPIO\_AD\_B0\_06\_XBAR1\_INOUT18** 0x401F80D4U, 0x6U, 0x401F8630U, 0x1U, 0x401F82C4U
- #define **IOMUXC\_GPIO\_AD\_B0\_07\_JTAG\_TCK** 0x401F80D8U, 0x0U, 0, 0, 0x401F82C8U
- #define **IOMUXC\_GPIO\_AD\_B0\_07\_GPT2\_COMPARE2** 0x401F80D8U, 0x1U, 0, 0, 0x401F82C8U
- #define **IOMUXC\_GPIO\_AD\_B0\_07\_ENET\_TX\_ER** 0x401F80D8U, 0x2U, 0, 0, 0x401F82C8U
- #define **IOMUXC\_GPIO\_AD\_B0\_07\_SAI2\_RX\_SYNC** 0x401F80D8U, 0x3U, 0x401F85BCU, 0x1U, 0x401F82C8U
- #define **IOMUXC\_GPIO\_AD\_B0\_07\_GPIO1\_IO07** 0x401F80D8U, 0x5U, 0, 0, 0x401F82C8U
- #define **IOMUXC\_GPIO\_AD\_B0\_07\_XBAR1\_INOUT19** 0x401F80D8U, 0x6U, 0x401F8654U, 0x1U, 0x401F82C8U
- #define **IOMUXC\_GPIO\_AD\_B0\_07\_ENET\_1588\_EVENT3\_OUT** 0x401F80D8U, 0x7U, 0, 0, 0x401F82C8U
- #define **IOMUXC\_GPIO\_AD\_B0\_08\_JTAG\_MOD** 0x401F80DCU, 0x0U, 0, 0, 0x401F82CCU
- #define **IOMUXC\_GPIO\_AD\_B0\_08\_GPT2\_COMPARE3** 0x401F80DCU, 0x1U, 0, 0, 0x401F82CCU

- F82CCU
- #define **IOMUXC\_GPIO\_AD\_B0\_08\_ENET\_RX\_DATA03** 0x401F80DCU, 0x2U, 0, 0, 0x401F82CCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_08\_SAI2\_RX\_DATA** 0x401F80DCU, 0x3U, 0x401F85B8U, 0x1U, 0x401F82CCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_08\_GPIO1\_IO08** 0x401F80DCU, 0x5U, 0, 0, 0x401F82CCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_08\_XBAR1\_IN20** 0x401F80DCU, 0x6U, 0x401F8634U, 0x1U, 0x401F82CCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_08\_ENET\_1588\_EVENT3\_IN** 0x401F80DCU, 0x7U, 0, 0, 0x401F82CCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_JTAG\_TDI** 0x401F80E0U, 0x0U, 0, 0, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_FLEXPWM2\_PWMA03** 0x401F80E0U, 0x1U, 0x401F8474U, 0x3U, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_ENET\_RX\_DATA02** 0x401F80E0U, 0x2U, 0, 0, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_SAI2\_TX\_DATA** 0x401F80E0U, 0x3U, 0, 0, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_GPIO1\_IO09** 0x401F80E0U, 0x5U, 0, 0, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_XBAR1\_IN21** 0x401F80E0U, 0x6U, 0x401F8658U, 0x1U, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_GPT2\_CLK** 0x401F80E0U, 0x7U, 0x401F876CU, 0x0U, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_09\_SEMC\_DQS4** 0x401F80E0U, 0x9U, 0x401F8788U, 0x2U, 0x401F82D0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_JTAG\_TDO** 0x401F80E4U, 0x0U, 0, 0, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_FLEXPWM1\_PWMA03** 0x401F80E4U, 0x1U, 0x401F8454U, 0x3U, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_ENET\_CRS** 0x401F80E4U, 0x2U, 0, 0, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_SAI2\_MCLK** 0x401F80E4U, 0x3U, 0x401F85B0U, 0x1U, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_GPIO1\_IO10** 0x401F80E4U, 0x5U, 0, 0, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_XBAR1\_IN22** 0x401F80E4U, 0x6U, 0x401F8638U, 0x1U, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_ENET\_1588\_EVENT0\_OUT** 0x401F80E4U, 0x7U, 0, 0, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_FLEXCAN3\_TX** 0x401F80E4U, 0x8U, 0, 0, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_10\_ARM\_TRACE\_SWO** 0x401F80E4U, 0x9U, 0, 0, 0x401F82D4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_JTAG\_TRSTB** 0x401F80E8U, 0x0U, 0, 0, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_FLEXPWM1\_PWMB03** 0x401F80E8U, 0x1U, 0x401F8464U, 0x3U, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_ENET\_COL** 0x401F80E8U, 0x2U, 0, 0, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_WDOG1\_WDOG\_B** 0x401F80E8U, 0x3U, 0, 0, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_GPIO1\_IO11** 0x401F80E8U, 0x5U, 0, 0, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_XBAR1\_IN23** 0x401F80E8U, 0x6U, 0x401F863CU, 0x1U, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_ENET\_1588\_EVENT0\_IN** 0x401F80E8U, 0x7U, 0x401F8444U, 0x1U, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_11\_FLEXCAN3\_RX** 0x401F80E8U, 0x8U, 0x401F878CU,

- 0x2U, 0x401F82D8U
- #define **IOMUXC\_GPIO\_AD\_B0\_11\_SEMC\_CLK6** 0x401F80E8U, 0x9U, 0, 0, 0x401F82D8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_LPI2C4\_SCL** 0x401F80ECU, 0x0U, 0x401F84E4U, 0x1-U, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_CCM\_PMIC\_READY** 0x401F80ECU, 0x1U, 0x401F83-FCU, 0x1U, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_LPUART1\_TX** 0x401F80ECU, 0x2U, 0, 0, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_WDOG2\_WDOG\_B** 0x401F80ECU, 0x3U, 0, 0, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_FLEXPWM1\_PWMX02** 0x401F80ECU, 0x4U, 0, 0, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_GPIO1\_IO12** 0x401F80ECU, 0x5U, 0, 0, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_ENET\_1588\_EVENT1\_OUT** 0x401F80ECU, 0x6U, 0, 0, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_12\_NMI\_GLUE\_NMI** 0x401F80ECU, 0x7U, 0x401F8568U, 0x0U, 0x401F82DCU
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_LPI2C4\_SDA** 0x401F80F0U, 0x0U, 0x401F84E8U, 0x1-U, 0x401F82E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_GPT1\_CLK** 0x401F80F0U, 0x1U, 0x401F8760U, 0x0U, 0x401F82E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_LPUART1\_RX** 0x401F80F0U, 0x2U, 0, 0, 0x401F82E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_EWM\_OUT\_B** 0x401F80F0U, 0x3U, 0, 0, 0x401F82E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_FLEXPWM1\_PWMX03** 0x401F80F0U, 0x4U, 0, 0, 0x401F82E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_GPIO1\_IO13** 0x401F80F0U, 0x5U, 0, 0, 0x401F82E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_ENET\_1588\_EVENT1\_IN** 0x401F80F0U, 0x6U, 0, 0, 0x401F82E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_13\_REF\_CLK\_24M** 0x401F80F0U, 0x7U, 0, 0, 0x401F82-E0U
  - #define **IOMUXC\_GPIO\_AD\_B0\_14\_XBAR1\_IN24** 0x401F80F4U, 0x1U, 0x401F8640U, 0x1-U, 0x401F82E4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_14\_LPUART1\_CTS\_B** 0x401F80F4U, 0x2U, 0, 0, 0x401F82E4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_14\_ENET\_1588\_EVENT0\_OUT** 0x401F80F4U, 0x3U, 0, 0, 0x401F82E4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_14\_GPIO1\_IO14** 0x401F80F4U, 0x5U, 0, 0, 0x401F82E4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_14\_FLEXCAN2\_TX** 0x401F80F4U, 0x6U, 0, 0, 0x401F82-E4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_14\_FLEXCAN3\_TX** 0x401F80F4U, 0x8U, 0, 0, 0x401F82-E4U
  - #define **IOMUXC\_GPIO\_AD\_B0\_15\_XBAR1\_IN25** 0x401F80F8U, 0x1U, 0x401F8650U, 0x0-U, 0x401F82E8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_15\_LPUART1\_RTS\_B** 0x401F80F8U, 0x2U, 0, 0, 0x401F82E8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_15\_ENET\_1588\_EVENT0\_IN** 0x401F80F8U, 0x3U, 0x401F8444U, 0x0U, 0x401F82E8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_15\_GPIO1\_IO15** 0x401F80F8U, 0x5U, 0, 0, 0x401F82E8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_15\_FLEXCAN2\_RX** 0x401F80F8U, 0x6U, 0x401F8450U, 0x2U, 0x401F82E8U
  - #define **IOMUXC\_GPIO\_AD\_B0\_15\_WDOG1\_WDOG\_RST\_B\_DEB** 0x401F80F8U, 0x7U, 0,

- 0, 0x401F82E8U
- #define **IOMUXC\_GPIO\_AD\_B0\_15\_FLEXCAN3\_RX** 0x401F80F8U, 0x8U, 0x401F878CU, 0x1U, 0x401F82E8U
- #define **IOMUXC\_GPIO\_AD\_B1\_00\_QTIMER3\_TIMER0** 0x401F80FCU, 0x1U, 0x401F857-CU, 0x1U, 0x401F82ECU
- #define **IOMUXC\_GPIO\_AD\_B1\_00\_LPUART2\_CTS\_B** 0x401F80FCU, 0x2U, 0, 0, 0x401F82ECU
- #define **IOMUXC\_GPIO\_AD\_B1\_00\_LPI2C1\_SCL** 0x401F80FCU, 0x3U, 0x401F84CCU, 0x1-U, 0x401F82ECU
- #define **IOMUXC\_GPIO\_AD\_B1\_00\_WDOG1\_B** 0x401F80FCU, 0x4U, 0, 0, 0x401F82ECU
- #define **IOMUXC\_GPIO\_AD\_B1\_00\_GPIO1\_IO16** 0x401F80FCU, 0x5U, 0, 0, 0x401F82ECU
- #define **IOMUXC\_GPIO\_AD\_B1\_00\_USDHC1\_WP** 0x401F80FCU, 0x6U, 0x401F85D8U, 0x2U, 0x401F82ECU
- #define **IOMUXC\_GPIO\_AD\_B1\_00\_FLEXIO3\_FLEXIO00** 0x401F80FCU, 0x9U, 0, 0, 0x401F82ECU
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_USB\_OTG1\_PWR** 0x401F8100U, 0x0U, 0, 0, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_QTIMER3\_TIMER1** 0x401F8100U, 0x1U, 0x401F8580-U, 0x0U, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_LPUART2\_RTS\_B** 0x401F8100U, 0x2U, 0, 0, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_LPI2C1\_SDA** 0x401F8100U, 0x3U, 0x401F84D0U, 0x1-U, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_CCM\_PMIC\_READY** 0x401F8100U, 0x4U, 0x401F83-FCU, 0x2U, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_GPIO1\_IO17** 0x401F8100U, 0x5U, 0, 0, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_USDHC1\_VSELECT** 0x401F8100U, 0x6U, 0, 0, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_01\_FLEXIO3\_FLEXIO01** 0x401F8100U, 0x9U, 0, 0, 0x401F82F0U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_USB\_OTG1\_ID** 0x401F8104U, 0x0U, 0x401F83F4U, 0x1U, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_QTIMER3\_TIMER2** 0x401F8104U, 0x1U, 0x401F8584-U, 0x1U, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_LPUART2\_TX** 0x401F8104U, 0x2U, 0x401F8530U, 0x1-U, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_SPDIF\_OUT** 0x401F8104U, 0x3U, 0, 0, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_ENET\_1588\_EVENT2\_OUT** 0x401F8104U, 0x4U, 0, 0, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_GPIO1\_IO18** 0x401F8104U, 0x5U, 0, 0, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_USDHC1\_CD\_B** 0x401F8104U, 0x6U, 0x401F85D4U, 0x1U, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_GPT2\_CLK** 0x401F8104U, 0x8U, 0x401F876CU, 0x1U, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_02\_FLEXIO3\_FLEXIO02** 0x401F8104U, 0x9U, 0, 0, 0x401F82F4U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_USB\_OTG1\_OC** 0x401F8108U, 0x0U, 0x401F85D0U, 0x1U, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_QTIMER3\_TIMER3** 0x401F8108U, 0x1U, 0x401F8588-U, 0x1U, 0x401F82F8U

- #define **IOMUXC\_GPIO\_AD\_B1\_03\_LPUART2\_RX** 0x401F8108U, 0x2U, 0x401F852CU, 0x1U, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_SPDIF\_IN** 0x401F8108U, 0x3U, 0x401F85C8U, 0x0U, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_ENET\_1588\_EVENT2\_IN** 0x401F8108U, 0x4U, 0, 0, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_GPIO1\_IO19** 0x401F8108U, 0x5U, 0, 0, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_USDHC2\_CD\_B** 0x401F8108U, 0x6U, 0x401F85E0U, 0x0U, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_GPT2\_CAPTURE1** 0x401F8108U, 0x8U, 0x401F8764U, 0x1U, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_03\_FLEXIO3\_FLEXIO03** 0x401F8108U, 0x9U, 0, 0, 0x401F82F8U
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_FLEXSPIB\_DATA03** 0x401F810CU, 0x0U, 0x401F84-C4U, 0x1U, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_ENET\_MDC** 0x401F810CU, 0x1U, 0, 0, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_LPUART3\_CTS\_B** 0x401F810CU, 0x2U, 0x401F8534U, 0x1U, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_SPDIF\_SR\_CLK** 0x401F810CU, 0x3U, 0, 0, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_GPIO1\_IO20** 0x401F810CU, 0x5U, 0, 0, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_USDHC2\_DATA0** 0x401F810CU, 0x6U, 0x401F85E8U, 0x1U, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_GPT2\_CAPTURE2** 0x401F810CU, 0x8U, 0x401F8768-U, 0x1U, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_04\_FLEXIO3\_FLEXIO04** 0x401F810CU, 0x9U, 0, 0, 0x401F82FCU
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_FLEXSPIB\_DATA02** 0x401F8110U, 0x0U, 0x401F84-C0U, 0x1U, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_ENET\_MDIO** 0x401F8110U, 0x1U, 0x401F8430U, 0x0-U, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_LPUART3\_RTS\_B** 0x401F8110U, 0x2U, 0, 0, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_SPDIF\_OUT** 0x401F8110U, 0x3U, 0, 0, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_GPIO1\_IO21** 0x401F8110U, 0x5U, 0, 0, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_USDHC2\_DATA1** 0x401F8110U, 0x6U, 0x401F85ECU, 0x1U, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_GPT2\_COMPARE1** 0x401F8110U, 0x8U, 0, 0, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_05\_FLEXIO3\_FLEXIO05** 0x401F8110U, 0x9U, 0, 0, 0x401F8300U
- #define **IOMUXC\_GPIO\_AD\_B1\_06\_FLEXSPIB\_DATA01** 0x401F8114U, 0x0U, 0x401F84-B-CU, 0x1U, 0x401F8304U
- #define **IOMUXC\_GPIO\_AD\_B1\_06\_LPI2C3\_SDA** 0x401F8114U, 0x1U, 0x401F84E0U, 0x2-U, 0x401F8304U
- #define **IOMUXC\_GPIO\_AD\_B1\_06\_LPUART3\_TX** 0x401F8114U, 0x2U, 0x401F853CU, 0x0U, 0x401F8304U
- #define **IOMUXC\_GPIO\_AD\_B1\_06\_SPDIF\_LOCK** 0x401F8114U, 0x3U, 0, 0, 0x401F8304U
- #define **IOMUXC\_GPIO\_AD\_B1\_06\_GPIO1\_IO22** 0x401F8114U, 0x5U, 0, 0, 0x401F8304U
- #define **IOMUXC\_GPIO\_AD\_B1\_06\_USDHC2\_DATA2** 0x401F8114U, 0x6U, 0x401F85F0U,

- 0x1U, 0x401F8304U
- #define **IOMUXC\_GPIO\_AD\_B1\_06\_GPT2\_COMPARE2** 0x401F8114U, 0x8U, 0, 0, 0x401F8304U
  - #define **IOMUXC\_GPIO\_AD\_B1\_06\_FLEXIO3\_FLEXIO06** 0x401F8114U, 0x9U, 0, 0, 0x401F8304U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_FLEXSPIB\_DATA00** 0x401F8118U, 0x0U, 0x401F84B8U, 0x1U, 0x401F8308U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_LPI2C3\_SCL** 0x401F8118U, 0x1U, 0x401F84DCU, 0x2U, 0x401F8308U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_LPUART3\_RX** 0x401F8118U, 0x2U, 0x401F8538U, 0x0U, 0x401F8308U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_SPDIF\_EXT\_CLK** 0x401F8118U, 0x3U, 0, 0, 0x401F8308U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_GPIO1\_IO23** 0x401F8118U, 0x5U, 0, 0, 0x401F8308U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_USDH\_C2\_DATA3** 0x401F8118U, 0x6U, 0x401F85F4U, 0x1U, 0x401F8308U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_GPT2\_COMPARE3** 0x401F8118U, 0x8U, 0, 0, 0x401F8308U
  - #define **IOMUXC\_GPIO\_AD\_B1\_07\_FLEXIO3\_FLEXIO07** 0x401F8118U, 0x9U, 0, 0, 0x401F8308U
  - #define **IOMUXC\_GPIO\_B0\_00\_LCD\_CLK** 0x401F813CU, 0x0U, 0, 0, 0x401F832CU
  - #define **IOMUXC\_GPIO\_B0\_00\_QTIMER1\_TIMER0** 0x401F813CU, 0x1U, 0, 0, 0x401F832CU
  - #define **IOMUXC\_GPIO\_B0\_00\_MQS\_RIGHT** 0x401F813CU, 0x2U, 0, 0, 0x401F832CU
  - #define **IOMUXC\_GPIO\_B0\_00\_LPSPi3\_PCS0** 0x401F813CU, 0x3U, 0x401F851CU, 0x0U, 0x401F832CU
  - #define **IOMUXC\_GPIO\_B0\_00\_FLEXIO2\_FLEXIO00** 0x401F813CU, 0x4U, 0, 0, 0x401F832CU
  - #define **IOMUXC\_GPIO\_B0\_00\_GPIO2\_IO00** 0x401F813CU, 0x5U, 0, 0, 0x401F832CU
  - #define **IOMUXC\_GPIO\_B0\_00\_SEMC\_CSX01** 0x401F813CU, 0x6U, 0, 0, 0x401F832CU
  - #define **IOMUXC\_GPIO\_B0\_01\_LCD\_ENABLE** 0x401F8140U, 0x0U, 0, 0, 0x401F8330U
  - #define **IOMUXC\_GPIO\_B0\_01\_QTIMER1\_TIMER1** 0x401F8140U, 0x1U, 0, 0, 0x401F8330U
  - #define **IOMUXC\_GPIO\_B0\_01\_MQS\_LEFT** 0x401F8140U, 0x2U, 0, 0, 0x401F8330U
  - #define **IOMUXC\_GPIO\_B0\_01\_LPSPi3\_SDI** 0x401F8140U, 0x3U, 0x401F8524U, 0x0U, 0x401F8330U
  - #define **IOMUXC\_GPIO\_B0\_01\_FLEXIO2\_FLEXIO01** 0x401F8140U, 0x4U, 0, 0, 0x401F8330U
  - #define **IOMUXC\_GPIO\_B0\_01\_GPIO2\_IO01** 0x401F8140U, 0x5U, 0, 0, 0x401F8330U
  - #define **IOMUXC\_GPIO\_B0\_01\_SEMC\_CSX02** 0x401F8140U, 0x6U, 0, 0, 0x401F8330U
  - #define **IOMUXC\_GPIO\_B0\_02\_LCD\_HSYNC** 0x401F8144U, 0x0U, 0, 0, 0x401F8334U
  - #define **IOMUXC\_GPIO\_B0\_02\_QTIMER1\_TIMER2** 0x401F8144U, 0x1U, 0, 0, 0x401F8334U
  - #define **IOMUXC\_GPIO\_B0\_02\_FLEXCAN1\_TX** 0x401F8144U, 0x2U, 0, 0, 0x401F8334U
  - #define **IOMUXC\_GPIO\_B0\_02\_LPSPi3\_SDO** 0x401F8144U, 0x3U, 0x401F8528U, 0x0U, 0x401F8334U
  - #define **IOMUXC\_GPIO\_B0\_02\_FLEXIO2\_FLEXIO02** 0x401F8144U, 0x4U, 0, 0, 0x401F8334U
  - #define **IOMUXC\_GPIO\_B0\_02\_GPIO2\_IO02** 0x401F8144U, 0x5U, 0, 0, 0x401F8334U
  - #define **IOMUXC\_GPIO\_B0\_02\_SEMC\_CSX03** 0x401F8144U, 0x6U, 0, 0, 0x401F8334U
  - #define **IOMUXC\_GPIO\_B0\_03\_LCD\_VSYNC** 0x401F8148U, 0x0U, 0, 0, 0x401F8338U

- #define **IOMUXC\_GPIO\_B0\_03\_QTIMER2\_TIMER0** 0x401F8148U, 0x1U, 0x401F856CU, 0x1U, 0x401F8338U
- #define **IOMUXC\_GPIO\_B0\_03\_FLEXCAN1\_RX** 0x401F8148U, 0x2U, 0x401F844CU, 0x3U, 0x401F8338U
- #define **IOMUXC\_GPIO\_B0\_03\_LPSPI3\_SCK** 0x401F8148U, 0x3U, 0x401F8520U, 0x0U, 0x401F8338U
- #define **IOMUXC\_GPIO\_B0\_03\_FLEXIO2\_FLEXIO03** 0x401F8148U, 0x4U, 0, 0, 0x401F8338U
- #define **IOMUXC\_GPIO\_B0\_03\_GPIO2\_IO03** 0x401F8148U, 0x5U, 0, 0, 0x401F8338U
- #define **IOMUXC\_GPIO\_B0\_03\_WDOG2\_RESET\_B\_DEB** 0x401F8148U, 0x6U, 0, 0, 0x401F8338U
- #define **IOMUXC\_GPIO\_B0\_04\_LCD\_DATA00** 0x401F814CU, 0x0U, 0, 0, 0x401F833CU
- #define **IOMUXC\_GPIO\_B0\_04\_QTIMER2\_TIMER1** 0x401F814CU, 0x1U, 0x401F8570U, 0x1U, 0x401F833CU
- #define **IOMUXC\_GPIO\_B0\_04\_LPI2C2\_SCL** 0x401F814CU, 0x2U, 0x401F84D4U, 0x1U, 0x401F833CU
- #define **IOMUXC\_GPIO\_B0\_04\_ARM\_TRACE0** 0x401F814CU, 0x3U, 0, 0, 0x401F833CU
- #define **IOMUXC\_GPIO\_B0\_04\_FLEXIO2\_FLEXIO04** 0x401F814CU, 0x4U, 0, 0, 0x401F833CU
- #define **IOMUXC\_GPIO\_B0\_04\_GPIO2\_IO04** 0x401F814CU, 0x5U, 0, 0, 0x401F833CU
- #define **IOMUXC\_GPIO\_B0\_04\_SRC\_BOOT\_CFG00** 0x401F814CU, 0x6U, 0, 0, 0x401F833CU
- #define **IOMUXC\_GPIO\_B0\_05\_LCD\_DATA01** 0x401F8150U, 0x0U, 0, 0, 0x401F8340U
- #define **IOMUXC\_GPIO\_B0\_05\_QTIMER2\_TIMER2** 0x401F8150U, 0x1U, 0x401F8574U, 0x1U, 0x401F8340U
- #define **IOMUXC\_GPIO\_B0\_05\_LPI2C2\_SDA** 0x401F8150U, 0x2U, 0x401F84D8U, 0x1U, 0x401F8340U
- #define **IOMUXC\_GPIO\_B0\_05\_ARM\_TRACE1** 0x401F8150U, 0x3U, 0, 0, 0x401F8340U
- #define **IOMUXC\_GPIO\_B0\_05\_FLEXIO2\_FLEXIO05** 0x401F8150U, 0x4U, 0, 0, 0x401F8340U
- #define **IOMUXC\_GPIO\_B0\_05\_GPIO2\_IO05** 0x401F8150U, 0x5U, 0, 0, 0x401F8340U
- #define **IOMUXC\_GPIO\_B0\_05\_SRC\_BOOT\_CFG01** 0x401F8150U, 0x6U, 0, 0, 0x401F8340U
- #define **IOMUXC\_GPIO\_B0\_06\_LCD\_DATA02** 0x401F8154U, 0x0U, 0, 0, 0x401F8344U
- #define **IOMUXC\_GPIO\_B0\_06\_QTIMER3\_TIMER0** 0x401F8154U, 0x1U, 0x401F857CU, 0x2U, 0x401F8344U
- #define **IOMUXC\_GPIO\_B0\_06\_FLEXPWM2\_PWMA00** 0x401F8154U, 0x2U, 0x401F8478U, 0x1U, 0x401F8344U
- #define **IOMUXC\_GPIO\_B0\_06\_ARM\_TRACE2** 0x401F8154U, 0x3U, 0, 0, 0x401F8344U
- #define **IOMUXC\_GPIO\_B0\_06\_FLEXIO2\_FLEXIO06** 0x401F8154U, 0x4U, 0, 0, 0x401F8344U
- #define **IOMUXC\_GPIO\_B0\_06\_GPIO2\_IO06** 0x401F8154U, 0x5U, 0, 0, 0x401F8344U
- #define **IOMUXC\_GPIO\_B0\_06\_SRC\_BOOT\_CFG02** 0x401F8154U, 0x6U, 0, 0, 0x401F8344U
- #define **IOMUXC\_GPIO\_B0\_07\_LCD\_DATA03** 0x401F8158U, 0x0U, 0, 0, 0x401F8348U
- #define **IOMUXC\_GPIO\_B0\_07\_QTIMER3\_TIMER1** 0x401F8158U, 0x1U, 0x401F8580U, 0x2U, 0x401F8348U
- #define **IOMUXC\_GPIO\_B0\_07\_FLEXPWM2\_PWMB00** 0x401F8158U, 0x2U, 0x401F8488U, 0x1U, 0x401F8348U
- #define **IOMUXC\_GPIO\_B0\_07\_ARM\_TRACE3** 0x401F8158U, 0x3U, 0, 0, 0x401F8348U
- #define **IOMUXC\_GPIO\_B0\_07\_FLEXIO2\_FLEXIO07** 0x401F8158U, 0x4U, 0, 0, 0x401F8348U

F8348U

- #define **IOMUXC\_GPIO\_B0\_07\_GPIO2\_IO07** 0x401F8158U, 0x5U, 0, 0, 0x401F8348U
- #define **IOMUXC\_GPIO\_B0\_07\_SRC\_BOOT\_CFG03** 0x401F8158U, 0x6U, 0, 0, 0x401F8348-U
- #define **IOMUXC\_GPIO\_B0\_08\_LCD\_DATA04** 0x401F815CU, 0x0U, 0, 0, 0x401F834CU
- #define **IOMUXC\_GPIO\_B0\_08\_QTIMER3\_TIMER2** 0x401F815CU, 0x1U, 0x401F8584U, 0x2U, 0x401F834CU
- #define **IOMUXC\_GPIO\_B0\_08\_FLEXPWM2\_PWMA01** 0x401F815CU, 0x2U, 0x401F847CU, 0x1U, 0x401F834CU
- #define **IOMUXC\_GPIO\_B0\_08\_LPUART3\_TX** 0x401F815CU, 0x3U, 0x401F853CU, 0x2U, 0x401F834CU
- #define **IOMUXC\_GPIO\_B0\_08\_FLEXIO2\_FLEXIO08** 0x401F815CU, 0x4U, 0, 0, 0x401F834CU
- #define **IOMUXC\_GPIO\_B0\_08\_GPIO2\_IO08** 0x401F815CU, 0x5U, 0, 0, 0x401F834CU
- #define **IOMUXC\_GPIO\_B0\_08\_SRC\_BOOT\_CFG04** 0x401F815CU, 0x6U, 0, 0, 0x401F834-CU
- #define **IOMUXC\_GPIO\_B0\_09\_LCD\_DATA05** 0x401F8160U, 0x0U, 0, 0, 0x401F8350U
- #define **IOMUXC\_GPIO\_B0\_09\_QTIMER4\_TIMER0** 0x401F8160U, 0x1U, 0, 0, 0x401F8350-U
- #define **IOMUXC\_GPIO\_B0\_09\_FLEXPWM2\_PWMB01** 0x401F8160U, 0x2U, 0x401F848CU, 0x1U, 0x401F8350U
- #define **IOMUXC\_GPIO\_B0\_09\_LPUART3\_RX** 0x401F8160U, 0x3U, 0x401F8538U, 0x2U, 0x401F8350U
- #define **IOMUXC\_GPIO\_B0\_09\_FLEXIO2\_FLEXIO09** 0x401F8160U, 0x4U, 0, 0, 0x401F8350U
- #define **IOMUXC\_GPIO\_B0\_09\_GPIO2\_IO09** 0x401F8160U, 0x5U, 0, 0, 0x401F8350U
- #define **IOMUXC\_GPIO\_B0\_09\_SRC\_BOOT\_CFG05** 0x401F8160U, 0x6U, 0, 0, 0x401F8350-U
- #define **IOMUXC\_GPIO\_B0\_10\_LCD\_DATA06** 0x401F8164U, 0x0U, 0, 0, 0x401F8354U
- #define **IOMUXC\_GPIO\_B0\_10\_QTIMER4\_TIMER1** 0x401F8164U, 0x1U, 0, 0, 0x401F8354-U
- #define **IOMUXC\_GPIO\_B0\_10\_FLEXPWM2\_PWMA02** 0x401F8164U, 0x2U, 0x401F8480-U, 0x1U, 0x401F8354U
- #define **IOMUXC\_GPIO\_B0\_10\_SAI1\_TX\_DATA03** 0x401F8164U, 0x3U, 0x401F8598U, 0x1-U, 0x401F8354U
- #define **IOMUXC\_GPIO\_B0\_10\_FLEXIO2\_FLEXIO10** 0x401F8164U, 0x4U, 0, 0, 0x401F8354U
- #define **IOMUXC\_GPIO\_B0\_10\_GPIO2\_IO10** 0x401F8164U, 0x5U, 0, 0, 0x401F8354U
- #define **IOMUXC\_GPIO\_B0\_10\_SRC\_BOOT\_CFG06** 0x401F8164U, 0x6U, 0, 0, 0x401F8354-U
- #define **IOMUXC\_GPIO\_B0\_11\_LCD\_DATA07** 0x401F8168U, 0x0U, 0, 0, 0x401F8358U
- #define **IOMUXC\_GPIO\_B0\_11\_QTIMER4\_TIMER2** 0x401F8168U, 0x1U, 0, 0, 0x401F8358-U
- #define **IOMUXC\_GPIO\_B0\_11\_FLEXPWM2\_PWMB02** 0x401F8168U, 0x2U, 0x401F8490U, 0x1U, 0x401F8358U
- #define **IOMUXC\_GPIO\_B0\_11\_SAI1\_TX\_DATA02** 0x401F8168U, 0x3U, 0x401F859CU, 0x1U, 0x401F8358U
- #define **IOMUXC\_GPIO\_B0\_11\_FLEXIO2\_FLEXIO11** 0x401F8168U, 0x4U, 0, 0, 0x401F8358U
- #define **IOMUXC\_GPIO\_B0\_11\_GPIO2\_IO11** 0x401F8168U, 0x5U, 0, 0, 0x401F8358U
- #define **IOMUXC\_GPIO\_B0\_11\_SRC\_BOOT\_CFG07** 0x401F8168U, 0x6U, 0, 0, 0x401F8358-

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- #define **IOMUXC\_GPIO\_B0\_12\_LCD\_DATA08** 0x401F816CU, 0x0U, 0, 0, 0x401F835CU
  - #define **IOMUXC\_GPIO\_B0\_12\_XBAR1\_INOUT10** 0x401F816CU, 0x1U, 0, 0, 0x401F835CU
  - #define **IOMUXC\_GPIO\_B0\_12\_ARM\_TRACE\_CLK** 0x401F816CU, 0x2U, 0, 0, 0x401F835CU
  - #define **IOMUXC\_GPIO\_B0\_12\_SAI1\_TX\_DATA01** 0x401F816CU, 0x3U, 0x401F85A0U, 0x1U, 0x401F835CU
  - #define **IOMUXC\_GPIO\_B0\_12\_FLEXIO2\_FLEXIO12** 0x401F816CU, 0x4U, 0, 0, 0x401F835CU
  - #define **IOMUXC\_GPIO\_B0\_12\_GPIO2\_IO12** 0x401F816CU, 0x5U, 0, 0, 0x401F835CU
  - #define **IOMUXC\_GPIO\_B0\_12\_SRC\_BOOT\_CFG08** 0x401F816CU, 0x6U, 0, 0, 0x401F835CU
  - #define **IOMUXC\_GPIO\_B0\_13\_LCD\_DATA09** 0x401F8170U, 0x0U, 0, 0, 0x401F8360U
  - #define **IOMUXC\_GPIO\_B0\_13\_XBAR1\_INOUT11** 0x401F8170U, 0x1U, 0, 0, 0x401F8360U
  - #define **IOMUXC\_GPIO\_B0\_13\_ARM\_TRACE\_SWO** 0x401F8170U, 0x2U, 0, 0, 0x401F8360U
  - #define **IOMUXC\_GPIO\_B0\_13\_SAI1\_MCLK** 0x401F8170U, 0x3U, 0x401F858CU, 0x2U, 0x401F8360U
  - #define **IOMUXC\_GPIO\_B0\_13\_FLEXIO2\_FLEXIO13** 0x401F8170U, 0x4U, 0, 0, 0x401F8360U
  - #define **IOMUXC\_GPIO\_B0\_13\_GPIO2\_IO13** 0x401F8170U, 0x5U, 0, 0, 0x401F8360U
  - #define **IOMUXC\_GPIO\_B0\_13\_SRC\_BOOT\_CFG09** 0x401F8170U, 0x6U, 0, 0, 0x401F8360U
  - #define **IOMUXC\_GPIO\_B0\_14\_LCD\_DATA10** 0x401F8174U, 0x0U, 0, 0, 0x401F8364U
  - #define **IOMUXC\_GPIO\_B0\_14\_XBAR1\_INOUT12** 0x401F8174U, 0x1U, 0, 0, 0x401F8364U
  - #define **IOMUXC\_GPIO\_B0\_14\_ARM\_TXEV** 0x401F8174U, 0x2U, 0, 0, 0x401F8364U
  - #define **IOMUXC\_GPIO\_B0\_14\_SAI1\_RX\_SYNC** 0x401F8174U, 0x3U, 0x401F85A4U, 0x2U, 0x401F8364U
  - #define **IOMUXC\_GPIO\_B0\_14\_FLEXIO2\_FLEXIO14** 0x401F8174U, 0x4U, 0, 0, 0x401F8364U
  - #define **IOMUXC\_GPIO\_B0\_14\_GPIO2\_IO14** 0x401F8174U, 0x5U, 0, 0, 0x401F8364U
  - #define **IOMUXC\_GPIO\_B0\_14\_SRC\_BOOT\_CFG10** 0x401F8174U, 0x6U, 0, 0, 0x401F8364U
  - #define **IOMUXC\_GPIO\_B0\_15\_LCD\_DATA11** 0x401F8178U, 0x0U, 0, 0, 0x401F8368U
  - #define **IOMUXC\_GPIO\_B0\_15\_XBAR1\_INOUT13** 0x401F8178U, 0x1U, 0, 0, 0x401F8368U
  - #define **IOMUXC\_GPIO\_B0\_15\_ARM\_RXEV** 0x401F8178U, 0x2U, 0, 0, 0x401F8368U
  - #define **IOMUXC\_GPIO\_B0\_15\_SAI1\_RX\_BCLK** 0x401F8178U, 0x3U, 0x401F8590U, 0x2U, 0x401F8368U
  - #define **IOMUXC\_GPIO\_B0\_15\_FLEXIO2\_FLEXIO15** 0x401F8178U, 0x4U, 0, 0, 0x401F8368U
  - #define **IOMUXC\_GPIO\_B0\_15\_GPIO2\_IO15** 0x401F8178U, 0x5U, 0, 0, 0x401F8368U
  - #define **IOMUXC\_GPIO\_B0\_15\_SRC\_BOOT\_CFG11** 0x401F8178U, 0x6U, 0, 0, 0x401F8368U
  - #define **IOMUXC\_GPIO\_B1\_00\_LCD\_DATA12** 0x401F817CU, 0x0U, 0, 0, 0x401F836CU
  - #define **IOMUXC\_GPIO\_B1\_00\_XBAR1\_INOUT14** 0x401F817CU, 0x1U, 0x401F8644U, 0x1U, 0x401F836CU
  - #define **IOMUXC\_GPIO\_B1\_00\_LPUART4\_TX** 0x401F817CU, 0x2U, 0x401F8544U, 0x2U, 0x401F836CU
  - #define **IOMUXC\_GPIO\_B1\_00\_SAI1\_RX\_DATA00** 0x401F817CU, 0x3U, 0x401F8594U, 0x2U, 0x401F836CU
  - #define **IOMUXC\_GPIO\_B1\_00\_FLEXIO2\_FLEXIO16** 0x401F817CU, 0x4U, 0, 0, 0x401F836CU

F836CU

- #define **IOMUXC\_GPIO\_B1\_00\_GPIO2\_IO16** 0x401F817CU, 0x5U, 0, 0, 0x401F836CU
- #define **IOMUXC\_GPIO\_B1\_00\_FLEXPWM1\_PWMA03** 0x401F817CU, 0x6U, 0x401F8454-U, 0x4U, 0x401F836CU
- #define **IOMUXC\_GPIO\_B1\_00\_FLEXIO3\_FLEXIO16** 0x401F817CU, 0x9U, 0, 0, 0x401-F836CU
- #define **IOMUXC\_GPIO\_B1\_01\_LCD\_DATA13** 0x401F8180U, 0x0U, 0, 0, 0x401F8370U
- #define **IOMUXC\_GPIO\_B1\_01\_XBAR1\_INOUT15** 0x401F8180U, 0x1U, 0x401F8648U, 0x1-U, 0x401F8370U
- #define **IOMUXC\_GPIO\_B1\_01\_LPUART4\_RX** 0x401F8180U, 0x2U, 0x401F8540U, 0x2U, 0x401F8370U
- #define **IOMUXC\_GPIO\_B1\_01\_SAI1\_TX\_DATA00** 0x401F8180U, 0x3U, 0, 0, 0x401F8370U
- #define **IOMUXC\_GPIO\_B1\_01\_FLEXIO2\_FLEXIO17** 0x401F8180U, 0x4U, 0, 0, 0x401-F8370U
- #define **IOMUXC\_GPIO\_B1\_01\_GPIO2\_IO17** 0x401F8180U, 0x5U, 0, 0, 0x401F8370U
- #define **IOMUXC\_GPIO\_B1\_01\_FLEXPWM1\_PWMB03** 0x401F8180U, 0x6U, 0x401F8464U, 0x4U, 0x401F8370U
- #define **IOMUXC\_GPIO\_B1\_01\_FLEXIO3\_FLEXIO17** 0x401F8180U, 0x9U, 0, 0, 0x401-F8370U
- #define **IOMUXC\_GPIO\_B1\_02\_LCD\_DATA14** 0x401F8184U, 0x0U, 0, 0, 0x401F8374U
- #define **IOMUXC\_GPIO\_B1\_02\_XBAR1\_INOUT16** 0x401F8184U, 0x1U, 0x401F864CU, 0x1-U, 0x401F8374U
- #define **IOMUXC\_GPIO\_B1\_02\_LPSPI3\_PCS2** 0x401F8184U, 0x2U, 0, 0, 0x401F8374U
- #define **IOMUXC\_GPIO\_B1\_02\_SAI1\_TX\_BCLK** 0x401F8184U, 0x3U, 0x401F85A8U, 0x2U, 0x401F8374U
- #define **IOMUXC\_GPIO\_B1\_02\_FLEXIO2\_FLEXIO18** 0x401F8184U, 0x4U, 0, 0, 0x401-F8374U
- #define **IOMUXC\_GPIO\_B1\_02\_GPIO2\_IO18** 0x401F8184U, 0x5U, 0, 0, 0x401F8374U
- #define **IOMUXC\_GPIO\_B1\_02\_FLEXPWM2\_PWMA03** 0x401F8184U, 0x6U, 0x401F8474-U, 0x4U, 0x401F8374U
- #define **IOMUXC\_GPIO\_B1\_02\_FLEXIO3\_FLEXIO18** 0x401F8184U, 0x9U, 0, 0, 0x401-F8374U
- #define **IOMUXC\_GPIO\_B1\_03\_LCD\_DATA15** 0x401F8188U, 0x0U, 0, 0, 0x401F8378U
- #define **IOMUXC\_GPIO\_B1\_03\_XBAR1\_INOUT17** 0x401F8188U, 0x1U, 0x401F862CU, 0x3-U, 0x401F8378U
- #define **IOMUXC\_GPIO\_B1\_03\_LPSPI3\_PCS1** 0x401F8188U, 0x2U, 0, 0, 0x401F8378U
- #define **IOMUXC\_GPIO\_B1\_03\_SAI1\_TX\_SYNC** 0x401F8188U, 0x3U, 0x401F85ACU, 0x2U, 0x401F8378U
- #define **IOMUXC\_GPIO\_B1\_03\_FLEXIO2\_FLEXIO19** 0x401F8188U, 0x4U, 0, 0, 0x401-F8378U
- #define **IOMUXC\_GPIO\_B1\_03\_GPIO2\_IO19** 0x401F8188U, 0x5U, 0, 0, 0x401F8378U
- #define **IOMUXC\_GPIO\_B1\_03\_FLEXPWM2\_PWMB03** 0x401F8188U, 0x6U, 0x401F8484U, 0x3U, 0x401F8378U
- #define **IOMUXC\_GPIO\_B1\_03\_FLEXIO3\_FLEXIO19** 0x401F8188U, 0x9U, 0, 0, 0x401-F8378U
- #define **IOMUXC\_GPIO\_B1\_04\_LCD\_DATA16** 0x401F818CU, 0x0U, 0, 0, 0x401F837CU
- #define **IOMUXC\_GPIO\_B1\_04\_LPSPI3\_PCS0** 0x401F818CU, 0x1U, 0x401F851CU, 0x1U, 0x401F837CU
- #define **IOMUXC\_GPIO\_B1\_04\_ENET\_RX\_DATA00** 0x401F818CU, 0x3U, 0x401F8434U, 0x1U, 0x401F837CU
- #define **IOMUXC\_GPIO\_B1\_04\_FLEXIO2\_FLEXIO20** 0x401F818CU, 0x4U, 0, 0, 0x401-

F837CU

- #define **IOMUXC\_GPIO\_B1\_04\_GPIO2\_IO20** 0x401F818CU, 0x5U, 0, 0, 0x401F837CU
- #define **IOMUXC\_GPIO\_B1\_04\_GPT1\_CLK** 0x401F818CU, 0x8U, 0x401F8760U, 0x1U, 0x401F837CU
- #define **IOMUXC\_GPIO\_B1\_04\_FLEXIO3\_FLEXIO20** 0x401F818CU, 0x9U, 0, 0, 0x401F837CU
- #define **IOMUXC\_GPIO\_B1\_05\_LCD\_DATA17** 0x401F8190U, 0x0U, 0, 0, 0x401F8380U
- #define **IOMUXC\_GPIO\_B1\_05\_LPSPI3\_SDI** 0x401F8190U, 0x1U, 0x401F8524U, 0x1U, 0x401F8380U
- #define **IOMUXC\_GPIO\_B1\_05\_ENET\_RX\_DATA01** 0x401F8190U, 0x3U, 0x401F8438U, 0x1U, 0x401F8380U
- #define **IOMUXC\_GPIO\_B1\_05\_FLEXIO2\_FLEXIO21** 0x401F8190U, 0x4U, 0, 0, 0x401F8380U
- #define **IOMUXC\_GPIO\_B1\_05\_GPIO2\_IO21** 0x401F8190U, 0x5U, 0, 0, 0x401F8380U
- #define **IOMUXC\_GPIO\_B1\_05\_GPT1\_CAPTURE1** 0x401F8190U, 0x8U, 0x401F8758U, 0x1U, 0x401F8380U
- #define **IOMUXC\_GPIO\_B1\_05\_FLEXIO3\_FLEXIO21** 0x401F8190U, 0x9U, 0, 0, 0x401F8380U
- #define **IOMUXC\_GPIO\_B1\_06\_LCD\_DATA18** 0x401F8194U, 0x0U, 0, 0, 0x401F8384U
- #define **IOMUXC\_GPIO\_B1\_06\_LPSPI3\_SDO** 0x401F8194U, 0x1U, 0x401F8528U, 0x1U, 0x401F8384U
- #define **IOMUXC\_GPIO\_B1\_06\_ENET\_RX\_EN** 0x401F8194U, 0x3U, 0x401F843CU, 0x1U, 0x401F8384U
- #define **IOMUXC\_GPIO\_B1\_06\_FLEXIO2\_FLEXIO22** 0x401F8194U, 0x4U, 0, 0, 0x401F8384U
- #define **IOMUXC\_GPIO\_B1\_06\_GPIO2\_IO22** 0x401F8194U, 0x5U, 0, 0, 0x401F8384U
- #define **IOMUXC\_GPIO\_B1\_06\_GPT1\_CAPTURE2** 0x401F8194U, 0x8U, 0x401F875CU, 0x1U, 0x401F8384U
- #define **IOMUXC\_GPIO\_B1\_06\_FLEXIO3\_FLEXIO22** 0x401F8194U, 0x9U, 0, 0, 0x401F8384U
- #define **IOMUXC\_GPIO\_B1\_07\_LCD\_DATA19** 0x401F8198U, 0x0U, 0, 0, 0x401F8388U
- #define **IOMUXC\_GPIO\_B1\_07\_LPSPI3\_SCK** 0x401F8198U, 0x1U, 0x401F8520U, 0x1U, 0x401F8388U
- #define **IOMUXC\_GPIO\_B1\_07\_ENET\_TX\_DATA00** 0x401F8198U, 0x3U, 0, 0, 0x401F8388U
- #define **IOMUXC\_GPIO\_B1\_07\_FLEXIO2\_FLEXIO23** 0x401F8198U, 0x4U, 0, 0, 0x401F8388U
- #define **IOMUXC\_GPIO\_B1\_07\_GPIO2\_IO23** 0x401F8198U, 0x5U, 0, 0, 0x401F8388U
- #define **IOMUXC\_GPIO\_B1\_07\_GPT1\_COMPARE1** 0x401F8198U, 0x8U, 0, 0, 0x401F8388U
- #define **IOMUXC\_GPIO\_B1\_07\_FLEXIO3\_FLEXIO23** 0x401F8198U, 0x9U, 0, 0, 0x401F8388U
- #define **IOMUXC\_GPIO\_B1\_08\_LCD\_DATA20** 0x401F819CU, 0x0U, 0, 0, 0x401F838CU
- #define **IOMUXC\_GPIO\_B1\_08\_QTIMER1\_TIMER3** 0x401F819CU, 0x1U, 0, 0, 0x401F838CU
- #define **IOMUXC\_GPIO\_B1\_08\_ENET\_TX\_DATA01** 0x401F819CU, 0x3U, 0, 0, 0x401F838CU
- #define **IOMUXC\_GPIO\_B1\_08\_FLEXIO2\_FLEXIO24** 0x401F819CU, 0x4U, 0, 0, 0x401F838CU
- #define **IOMUXC\_GPIO\_B1\_08\_GPIO2\_IO24** 0x401F819CU, 0x5U, 0, 0, 0x401F838CU
- #define **IOMUXC\_GPIO\_B1\_08\_FLEXCAN2\_TX** 0x401F819CU, 0x6U, 0, 0, 0x401F838CU
- #define **IOMUXC\_GPIO\_B1\_08\_GPT1\_COMPARE2** 0x401F819CU, 0x8U, 0, 0, 0x401F838-

CU

- #define **IOMUXC\_GPIO\_B1\_08\_FLEXIO3\_FLEXIO24** 0x401F819CU, 0x9U, 0, 0, 0x401-F838CU
- #define **IOMUXC\_GPIO\_B1\_09\_LCD\_DATA21** 0x401F81A0U, 0x0U, 0, 0, 0x401F8390U
- #define **IOMUXC\_GPIO\_B1\_09\_QTIMER2\_TIMER3** 0x401F81A0U, 0x1U, 0x401F8578U, 0x1U, 0x401F8390U
- #define **IOMUXC\_GPIO\_B1\_09\_ENET\_TX\_EN** 0x401F81A0U, 0x3U, 0, 0, 0x401F8390U
- #define **IOMUXC\_GPIO\_B1\_09\_FLEXIO2\_FLEXIO25** 0x401F81A0U, 0x4U, 0, 0, 0x401-F8390U
- #define **IOMUXC\_GPIO\_B1\_09\_GPIO2\_IO25** 0x401F81A0U, 0x5U, 0, 0, 0x401F8390U
- #define **IOMUXC\_GPIO\_B1\_09\_FLEXCAN2\_RX** 0x401F81A0U, 0x6U, 0x401F8450U, 0x3U, 0x401F8390U
- #define **IOMUXC\_GPIO\_B1\_09\_GPT1\_COMPARE3** 0x401F81A0U, 0x8U, 0, 0, 0x401F8390-U
- #define **IOMUXC\_GPIO\_B1\_09\_FLEXIO3\_FLEXIO25** 0x401F81A0U, 0x9U, 0, 0, 0x401-F8390U
- #define **IOMUXC\_GPIO\_B1\_10\_LCD\_DATA22** 0x401F81A4U, 0x0U, 0, 0, 0x401F8394U
- #define **IOMUXC\_GPIO\_B1\_10\_QTIMER3\_TIMER3** 0x401F81A4U, 0x1U, 0x401F8588U, 0x2U, 0x401F8394U
- #define **IOMUXC\_GPIO\_B1\_10\_ENET\_TX\_CLK** 0x401F81A4U, 0x3U, 0x401F8448U, 0x1U, 0x401F8394U
- #define **IOMUXC\_GPIO\_B1\_10\_FLEXIO2\_FLEXIO26** 0x401F81A4U, 0x4U, 0, 0, 0x401-F8394U
- #define **IOMUXC\_GPIO\_B1\_10\_GPIO2\_IO26** 0x401F81A4U, 0x5U, 0, 0, 0x401F8394U
- #define **IOMUXC\_GPIO\_B1\_10\_ENET\_REF\_CLK** 0x401F81A4U, 0x6U, 0x401F842CU, 0x1-U, 0x401F8394U
- #define **IOMUXC\_GPIO\_B1\_10\_FLEXIO3\_FLEXIO26** 0x401F81A4U, 0x9U, 0, 0, 0x401-F8394U
- #define **IOMUXC\_GPIO\_B1\_11\_LCD\_DATA23** 0x401F81A8U, 0x0U, 0, 0, 0x401F8398U
- #define **IOMUXC\_GPIO\_B1\_11\_QTIMER4\_TIMER3** 0x401F81A8U, 0x1U, 0, 0, 0x401-F8398U
- #define **IOMUXC\_GPIO\_B1\_11\_ENET\_RX\_ER** 0x401F81A8U, 0x3U, 0x401F8440U, 0x1U, 0x401F8398U
- #define **IOMUXC\_GPIO\_B1\_11\_FLEXIO2\_FLEXIO27** 0x401F81A8U, 0x4U, 0, 0, 0x401-F8398U
- #define **IOMUXC\_GPIO\_B1\_11\_GPIO2\_IO27** 0x401F81A8U, 0x5U, 0, 0, 0x401F8398U
- #define **IOMUXC\_GPIO\_B1\_11\_LPSPI3\_PCS3** 0x401F81A8U, 0x6U, 0, 0, 0x401F8398U
- #define **IOMUXC\_GPIO\_B1\_11\_FLEXIO3\_FLEXIO27** 0x401F81A8U, 0x9U, 0, 0, 0x401-F8398U
- #define **IOMUXC\_GPIO\_B1\_12\_LPUART5\_TX** 0x401F81ACU, 0x1U, 0x401F854CU, 0x1U, 0x401F839CU
- #define **IOMUXC\_GPIO\_B1\_12\_ENET\_1588\_EVENT0\_IN** 0x401F81ACU, 0x3U, 0x401-F8444U, 0x2U, 0x401F839CU
- #define **IOMUXC\_GPIO\_B1\_12\_FLEXIO2\_FLEXIO28** 0x401F81ACU, 0x4U, 0, 0, 0x401-F839CU
- #define **IOMUXC\_GPIO\_B1\_12\_GPIO2\_IO28** 0x401F81ACU, 0x5U, 0, 0, 0x401F839CU
- #define **IOMUXC\_GPIO\_B1\_12\_USDHC1\_CD\_B** 0x401F81ACU, 0x6U, 0x401F85D4U, 0x2U, 0x401F839CU
- #define **IOMUXC\_GPIO\_B1\_12\_FLEXIO3\_FLEXIO28** 0x401F81ACU, 0x9U, 0, 0, 0x401-F839CU
- #define **IOMUXC\_GPIO\_B1\_13\_WDOG1\_B** 0x401F81B0U, 0x0U, 0, 0, 0x401F83A0U

- #define **IOMUXC\_GPIO\_B1\_13\_LPUART5\_RX** 0x401F81B0U, 0x1U, 0x401F8548U, 0x1U, 0x401F83A0U
- #define **IOMUXC\_GPIO\_B1\_13\_ENET\_1588\_EVENT0\_OUT** 0x401F81B0U, 0x3U, 0, 0, 0x401F83A0U
- #define **IOMUXC\_GPIO\_B1\_13\_FLEXIO2\_FLEXIO29** 0x401F81B0U, 0x4U, 0, 0, 0x401F83A0U
- #define **IOMUXC\_GPIO\_B1\_13\_GPIO2\_IO29** 0x401F81B0U, 0x5U, 0, 0, 0x401F83A0U
- #define **IOMUXC\_GPIO\_B1\_13\_USDHC1\_WP** 0x401F81B0U, 0x6U, 0x401F85D8U, 0x3U, 0x401F83A0U
- #define **IOMUXC\_GPIO\_B1\_13\_SEMC\_DQS4** 0x401F81B0U, 0x8U, 0x401F8788U, 0x3U, 0x401F83A0U
- #define **IOMUXC\_GPIO\_B1\_13\_FLEXIO3\_FLEXIO29** 0x401F81B0U, 0x9U, 0, 0, 0x401F83A0U
- #define **IOMUXC\_GPIO\_B1\_14\_ENET\_MDC** 0x401F81B4U, 0x0U, 0, 0, 0x401F83A4U
- #define **IOMUXC\_GPIO\_B1\_14\_FLEXPWM4\_PWMA02** 0x401F81B4U, 0x1U, 0x401F849CU, 0x1U, 0x401F83A4U
- #define **IOMUXC\_GPIO\_B1\_14\_XBAR1\_IN02** 0x401F81B4U, 0x3U, 0x401F860CU, 0x1U, 0x401F83A4U
- #define **IOMUXC\_GPIO\_B1\_14\_FLEXIO2\_FLEXIO30** 0x401F81B4U, 0x4U, 0, 0, 0x401F83A4U
- #define **IOMUXC\_GPIO\_B1\_14\_GPIO2\_IO30** 0x401F81B4U, 0x5U, 0, 0, 0x401F83A4U
- #define **IOMUXC\_GPIO\_B1\_14\_USDHC1\_VSELECT** 0x401F81B4U, 0x6U, 0, 0, 0x401F83A4U
- #define **IOMUXC\_GPIO\_B1\_14\_FLEXIO3\_FLEXIO30** 0x401F81B4U, 0x9U, 0, 0, 0x401F83A4U
- #define **IOMUXC\_GPIO\_B1\_15\_ENET\_MDIO** 0x401F81B8U, 0x0U, 0x401F8430U, 0x2U, 0x401F83A8U
- #define **IOMUXC\_GPIO\_B1\_15\_FLEXPWM4\_PWMA03** 0x401F81B8U, 0x1U, 0x401F84A0U, 0x1U, 0x401F83A8U
- #define **IOMUXC\_GPIO\_B1\_15\_XBAR1\_IN03** 0x401F81B8U, 0x3U, 0x401F8610U, 0x1U, 0x401F83A8U
- #define **IOMUXC\_GPIO\_B1\_15\_FLEXIO2\_FLEXIO31** 0x401F81B8U, 0x4U, 0, 0, 0x401F83A8U
- #define **IOMUXC\_GPIO\_B1\_15\_GPIO2\_IO31** 0x401F81B8U, 0x5U, 0, 0, 0x401F83A8U
- #define **IOMUXC\_GPIO\_B1\_15\_USDHC1\_RESET\_B** 0x401F81B8U, 0x6U, 0, 0, 0x401F83A8U
- #define **IOMUXC\_GPIO\_B1\_15\_FLEXIO3\_FLEXIO31** 0x401F81B8U, 0x9U, 0, 0, 0x401F83A8U
- #define **IOMUXC\_GPIO\_SD\_B0\_00\_USDHC1\_CMD** 0x401F81BCU, 0x0U, 0, 0, 0x401F83ACU
- #define **IOMUXC\_GPIO\_SD\_B0\_00\_FLEXPWM1\_PWMA00** 0x401F81BCU, 0x1U, 0x401F8458U, 0x1U, 0x401F83ACU
- #define **IOMUXC\_GPIO\_SD\_B0\_00\_LPI2C3\_SCL** 0x401F81BCU, 0x2U, 0x401F84DCU, 0x1U, 0x401F83ACU
- #define **IOMUXC\_GPIO\_SD\_B0\_00\_XBAR1\_INOUT04** 0x401F81BCU, 0x3U, 0x401F8614U, 0x1U, 0x401F83ACU
- #define **IOMUXC\_GPIO\_SD\_B0\_00\_LPSPPI1\_SCK** 0x401F81BCU, 0x4U, 0x401F84F0U, 0x1U, 0x401F83ACU
- #define **IOMUXC\_GPIO\_SD\_B0\_00\_GPIO3\_IO12** 0x401F81BCU, 0x5U, 0, 0, 0x401F83ACU
- #define **IOMUXC\_GPIO\_SD\_B0\_00\_FLEXSPIA\_SS1\_B** 0x401F81BCU, 0x6U, 0, 0, 0x401F83ACU

F83ACU

- #define **IOMUXC\_GPIO\_SD\_B0\_00\_SEMC\_DQS4** 0x401F81BCU, 0x9U, 0x401F8788U, 0x0-U, 0x401F83ACU
- #define **IOMUXC\_GPIO\_SD\_B0\_01\_USDHC1\_CLK** 0x401F81C0U, 0x0U, 0, 0, 0x401F83B0U
- #define **IOMUXC\_GPIO\_SD\_B0\_01\_FLEXPWM1\_PWMB00** 0x401F81C0U, 0x1U, 0x401-F8468U, 0x1U, 0x401F83B0U
- #define **IOMUXC\_GPIO\_SD\_B0\_01\_LPI2C3\_SDA** 0x401F81C0U, 0x2U, 0x401F84E0U, 0x1-U, 0x401F83B0U
- #define **IOMUXC\_GPIO\_SD\_B0\_01\_XBAR1\_INOUT05** 0x401F81C0U, 0x3U, 0x401F8618U, 0x1U, 0x401F83B0U
- #define **IOMUXC\_GPIO\_SD\_B0\_01\_LPSP1\_PCS0** 0x401F81C0U, 0x4U, 0x401F84ECU, 0x0-U, 0x401F83B0U
- #define **IOMUXC\_GPIO\_SD\_B0\_01\_GPIO3\_IO13** 0x401F81C0U, 0x5U, 0, 0, 0x401F83B0U
- #define **IOMUXC\_GPIO\_SD\_B0\_01\_FLEXSPIB\_SS1\_B** 0x401F81C0U, 0x6U, 0, 0, 0x401F83-B0U
- #define **IOMUXC\_GPIO\_SD\_B0\_02\_USDHC1\_DATA0** 0x401F81C4U, 0x0U, 0, 0, 0x401F83-B4U
- #define **IOMUXC\_GPIO\_SD\_B0\_02\_FLEXPWM1\_PWMA01** 0x401F81C4U, 0x1U, 0x401-F845CU, 0x1U, 0x401F83B4U
- #define **IOMUXC\_GPIO\_SD\_B0\_02\_LPUART8\_CTS\_B** 0x401F81C4U, 0x2U, 0, 0, 0x401F83-B4U
- #define **IOMUXC\_GPIO\_SD\_B0\_02\_XBAR1\_INOUT06** 0x401F81C4U, 0x3U, 0x401F861CU, 0x1U, 0x401F83B4U
- #define **IOMUXC\_GPIO\_SD\_B0\_02\_LPSP1\_SDO** 0x401F81C4U, 0x4U, 0x401F84F8U, 0x1-U, 0x401F83B4U
- #define **IOMUXC\_GPIO\_SD\_B0\_02\_GPIO3\_IO14** 0x401F81C4U, 0x5U, 0, 0, 0x401F83B4U
- #define **IOMUXC\_GPIO\_SD\_B0\_02\_SEMC\_CLK5** 0x401F81C4U, 0x9U, 0, 0, 0x401F83B4U
- #define **IOMUXC\_GPIO\_SD\_B0\_03\_USDHC1\_DATA1** 0x401F81C8U, 0x0U, 0, 0, 0x401F83-B8U
- #define **IOMUXC\_GPIO\_SD\_B0\_03\_FLEXPWM1\_PWMB01** 0x401F81C8U, 0x1U, 0x401-F846CU, 0x1U, 0x401F83B8U
- #define **IOMUXC\_GPIO\_SD\_B0\_03\_LPUART8\_RTS\_B** 0x401F81C8U, 0x2U, 0, 0, 0x401F83-B8U
- #define **IOMUXC\_GPIO\_SD\_B0\_03\_XBAR1\_INOUT07** 0x401F81C8U, 0x3U, 0x401F8620U, 0x1U, 0x401F83B8U
- #define **IOMUXC\_GPIO\_SD\_B0\_03\_LPSP1\_SDI** 0x401F81C8U, 0x4U, 0x401F84F4U, 0x1U, 0x401F83B8U
- #define **IOMUXC\_GPIO\_SD\_B0\_03\_GPIO3\_IO15** 0x401F81C8U, 0x5U, 0, 0, 0x401F83B8U
- #define **IOMUXC\_GPIO\_SD\_B0\_03\_SEMC\_CLK6** 0x401F81C8U, 0x9U, 0, 0, 0x401F83B8U
- #define **IOMUXC\_GPIO\_SD\_B0\_04\_USDHC1\_DATA2** 0x401F81CCU, 0x0U, 0, 0, 0x401F83-BCU
- #define **IOMUXC\_GPIO\_SD\_B0\_04\_FLEXPWM1\_PWMA02** 0x401F81CCU, 0x1U, 0x401-F8460U, 0x1U, 0x401F83BCU
- #define **IOMUXC\_GPIO\_SD\_B0\_04\_LPUART8\_TX** 0x401F81CCU, 0x2U, 0x401F8564U, 0x0U, 0x401F83BCU
- #define **IOMUXC\_GPIO\_SD\_B0\_04\_XBAR1\_INOUT08** 0x401F81CCU, 0x3U, 0x401F8624U, 0x1U, 0x401F83BCU
- #define **IOMUXC\_GPIO\_SD\_B0\_04\_FLEXSPIB\_SS0\_B** 0x401F81CCU, 0x4U, 0, 0, 0x401-F83BCU
- #define **IOMUXC\_GPIO\_SD\_B0\_04\_GPIO3\_IO16** 0x401F81CCU, 0x5U, 0, 0, 0x401F83BCU
- #define **IOMUXC\_GPIO\_SD\_B0\_04\_CCM\_CLKO1** 0x401F81CCU, 0x6U, 0, 0, 0x401F83BCU

- #define **IOMUXC\_GPIO\_SD\_B0\_05\_USDHC1\_DATA3** 0x401F81D0U, 0x0U, 0, 0, 0x401F83-C0U
- #define **IOMUXC\_GPIO\_SD\_B0\_05\_FLEXPWM1\_PWMB02** 0x401F81D0U, 0x1U, 0x401-F8470U, 0x1U, 0x401F83C0U
- #define **IOMUXC\_GPIO\_SD\_B0\_05\_LPUART8\_RX** 0x401F81D0U, 0x2U, 0x401F8560U, 0x0U, 0x401F83C0U
- #define **IOMUXC\_GPIO\_SD\_B0\_05\_XBAR1\_INOUT09** 0x401F81D0U, 0x3U, 0x401F8628U, 0x1U, 0x401F83C0U
- #define **IOMUXC\_GPIO\_SD\_B0\_05\_FLEXSPIB\_DQS** 0x401F81D0U, 0x4U, 0, 0, 0x401F83-C0U
- #define **IOMUXC\_GPIO\_SD\_B0\_05\_GPIO3\_IO17** 0x401F81D0U, 0x5U, 0, 0, 0x401F83C0U
- #define **IOMUXC\_GPIO\_SD\_B0\_05\_CCM\_CLKO2** 0x401F81D0U, 0x6U, 0, 0, 0x401F83C0U
- #define **IOMUXC\_GPIO\_SD\_B1\_00\_USDHC2\_DATA3** 0x401F81D4U, 0x0U, 0x401F85F4U, 0x0U, 0x401F83C4U
- #define **IOMUXC\_GPIO\_SD\_B1\_00\_FLEXSPIB\_DATA03** 0x401F81D4U, 0x1U, 0x401F84-C4U, 0x0U, 0x401F83C4U
- #define **IOMUXC\_GPIO\_SD\_B1\_00\_FLEXPWM1\_PWMA03** 0x401F81D4U, 0x2U, 0x401-F8454U, 0x0U, 0x401F83C4U
- #define **IOMUXC\_GPIO\_SD\_B1\_00\_SAI1\_TX\_DATA03** 0x401F81D4U, 0x3U, 0x401F8598U, 0x0U, 0x401F83C4U
- #define **IOMUXC\_GPIO\_SD\_B1\_00\_LPUART4\_TX** 0x401F81D4U, 0x4U, 0x401F8544U, 0x0U, 0x401F83C4U
- #define **IOMUXC\_GPIO\_SD\_B1\_00\_GPIO3\_IO00** 0x401F81D4U, 0x5U, 0, 0, 0x401F83C4U
- #define **IOMUXC\_GPIO\_SD\_B1\_00\_SAI3\_RX\_DATA** 0x401F81D4U, 0x8U, 0x401F8778U, 0x1U, 0x401F83C4U
- #define **IOMUXC\_GPIO\_SD\_B1\_01\_USDHC2\_DATA2** 0x401F81D8U, 0x0U, 0x401F85F0U, 0x0U, 0x401F83C8U
- #define **IOMUXC\_GPIO\_SD\_B1\_01\_FLEXSPIB\_DATA02** 0x401F81D8U, 0x1U, 0x401F84-C0U, 0x0U, 0x401F83C8U
- #define **IOMUXC\_GPIO\_SD\_B1\_01\_FLEXPWM1\_PWMB03** 0x401F81D8U, 0x2U, 0x401-F8464U, 0x0U, 0x401F83C8U
- #define **IOMUXC\_GPIO\_SD\_B1\_01\_SAI1\_TX\_DATA02** 0x401F81D8U, 0x3U, 0x401F859C-U, 0x0U, 0x401F83C8U
- #define **IOMUXC\_GPIO\_SD\_B1\_01\_LPUART4\_RX** 0x401F81D8U, 0x4U, 0x401F8540U, 0x0U, 0x401F83C8U
- #define **IOMUXC\_GPIO\_SD\_B1\_01\_GPIO3\_IO01** 0x401F81D8U, 0x5U, 0, 0, 0x401F83C8U
- #define **IOMUXC\_GPIO\_SD\_B1\_01\_SAI3\_TX\_DATA** 0x401F81D8U, 0x8U, 0, 0, 0x401F83-C8U
- #define **IOMUXC\_GPIO\_SD\_B1\_02\_USDHC2\_DATA1** 0x401F81DCU, 0x0U, 0x401F85ECU, 0x0U, 0x401F83CCU
- #define **IOMUXC\_GPIO\_SD\_B1\_02\_FLEXSPIB\_DATA01** 0x401F81DCU, 0x1U, 0x401F84B-CU, 0x0U, 0x401F83CCU
- #define **IOMUXC\_GPIO\_SD\_B1\_02\_FLEXPWM2\_PWMA03** 0x401F81DCU, 0x2U, 0x401-F8474U, 0x0U, 0x401F83CCU
- #define **IOMUXC\_GPIO\_SD\_B1\_02\_SAI1\_TX\_DATA01** 0x401F81DCU, 0x3U, 0x401F85A0-U, 0x0U, 0x401F83CCU
- #define **IOMUXC\_GPIO\_SD\_B1\_02\_FLEXCAN1\_TX** 0x401F81DCU, 0x4U, 0, 0, 0x401F83-CCU
- #define **IOMUXC\_GPIO\_SD\_B1\_02\_GPIO3\_IO02** 0x401F81DCU, 0x5U, 0, 0, 0x401F83CCU
- #define **IOMUXC\_GPIO\_SD\_B1\_02\_CCM\_WAIT** 0x401F81DCU, 0x6U, 0, 0, 0x401F83CCU

- #define **IOMUXC\_GPIO\_SD\_B1\_02\_SAI3\_TX\_SYNC** 0x401F81DCU, 0x8U, 0x401F8784U, 0x1U, 0x401F83CCU
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_USDHC2\_DATA0** 0x401F81E0U, 0x0U, 0x401F85E8U, 0x0U, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_FLEXSPIB\_DATA00** 0x401F81E0U, 0x1U, 0x401F84-B8U, 0x0U, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_FLEXPWM2\_PWMB03** 0x401F81E0U, 0x2U, 0x401-F8484U, 0x0U, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_SAI1\_MCLK** 0x401F81E0U, 0x3U, 0x401F858CU, 0x0-U, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_FLEXCAN1\_RX** 0x401F81E0U, 0x4U, 0x401F844CU, 0x0U, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_GPIO3\_IO03** 0x401F81E0U, 0x5U, 0, 0, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_CCM\_PMIC\_READY** 0x401F81E0U, 0x6U, 0x401F83-FCU, 0x0U, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_03\_SAI3\_TX\_BCLK** 0x401F81E0U, 0x8U, 0x401F8780U, 0x1U, 0x401F83D0U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_USDHC2\_CLK** 0x401F81E4U, 0x0U, 0x401F85DCU, 0x0U, 0x401F83D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_FLEXSPIB\_SCLK** 0x401F81E4U, 0x1U, 0, 0, 0x401F83-D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_LPI2C1\_SCL** 0x401F81E4U, 0x2U, 0x401F84CCU, 0x0-U, 0x401F83D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_SAI1\_RX\_SYNC** 0x401F81E4U, 0x3U, 0x401F85A4U, 0x0U, 0x401F83D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_FLEXSPIA\_SS1\_B** 0x401F81E4U, 0x4U, 0, 0, 0x401F83-D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_GPIO3\_IO04** 0x401F81E4U, 0x5U, 0, 0, 0x401F83D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_CCM\_STOP** 0x401F81E4U, 0x6U, 0, 0, 0x401F83D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_04\_SAI3\_MCLK** 0x401F81E4U, 0x8U, 0x401F8770U, 0x1U, 0x401F83D4U
- #define **IOMUXC\_GPIO\_SD\_B1\_05\_USDHC2\_CMD** 0x401F81E8U, 0x0U, 0x401F85E4U, 0x0U, 0x401F83D8U
- #define **IOMUXC\_GPIO\_SD\_B1\_05\_FLEXSPIA\_DQS** 0x401F81E8U, 0x1U, 0x401F84A4U, 0x0U, 0x401F83D8U
- #define **IOMUXC\_GPIO\_SD\_B1\_05\_LPI2C1\_SDA** 0x401F81E8U, 0x2U, 0x401F84D0U, 0x0-U, 0x401F83D8U
- #define **IOMUXC\_GPIO\_SD\_B1\_05\_SAI1\_RX\_BCLK** 0x401F81E8U, 0x3U, 0x401F8590U, 0x0U, 0x401F83D8U
- #define **IOMUXC\_GPIO\_SD\_B1\_05\_FLEXSPIB\_SS0\_B** 0x401F81E8U, 0x4U, 0, 0, 0x401F83-D8U
- #define **IOMUXC\_GPIO\_SD\_B1\_05\_GPIO3\_IO05** 0x401F81E8U, 0x5U, 0, 0, 0x401F83D8U
- #define **IOMUXC\_GPIO\_SD\_B1\_05\_SAI3\_RX\_SYNC** 0x401F81E8U, 0x8U, 0x401F877CU, 0x1U, 0x401F83D8U
- #define **IOMUXC\_GPIO\_SD\_B1\_06\_USDHC2\_RESET\_B** 0x401F81ECU, 0x0U, 0, 0, 0x401-F83DCU
- #define **IOMUXC\_GPIO\_SD\_B1\_06\_FLEXSPIA\_SS0\_B** 0x401F81ECU, 0x1U, 0, 0, 0x401-F83DCU
- #define **IOMUXC\_GPIO\_SD\_B1\_06\_LPUART7\_CTS\_B** 0x401F81ECU, 0x2U, 0, 0, 0x401-F83DCU

- #define **IOMUXC\_GPIO\_SD\_B1\_06\_SAI1\_RX\_DATA00** 0x401F81ECU, 0x3U, 0x401F8594-U, 0x0U, 0x401F83DCU
- #define **IOMUXC\_GPIO\_SD\_B1\_06\_LPSPi2\_PCS0** 0x401F81ECU, 0x4U, 0x401F84FCU, 0x0U, 0x401F83DCU
- #define **IOMUXC\_GPIO\_SD\_B1\_06\_GPIO3\_IO06** 0x401F81ECU, 0x5U, 0, 0, 0x401F83DCU
- #define **IOMUXC\_GPIO\_SD\_B1\_06\_SAI3\_RX\_BCLK** 0x401F81ECU, 0x8U, 0x401F8774U, 0x1U, 0x401F83DCU
- #define **IOMUXC\_GPIO\_SD\_B1\_07\_SEMC\_CSX01** 0x401F81F0U, 0x0U, 0, 0, 0x401F83E0U
- #define **IOMUXC\_GPIO\_SD\_B1\_07\_FLEXSPIA\_SCLK** 0x401F81F0U, 0x1U, 0x401F84C8U, 0x0U, 0x401F83E0U
- #define **IOMUXC\_GPIO\_SD\_B1\_07\_LPUART7\_RTS\_B** 0x401F81F0U, 0x2U, 0, 0, 0x401F83-E0U
- #define **IOMUXC\_GPIO\_SD\_B1\_07\_SAI1\_TX\_DATA00** 0x401F81F0U, 0x3U, 0, 0, 0x401-F83E0U
- #define **IOMUXC\_GPIO\_SD\_B1\_07\_LPSPi2\_SCK** 0x401F81F0U, 0x4U, 0x401F8500U, 0x0U, 0x401F83E0U
- #define **IOMUXC\_GPIO\_SD\_B1\_07\_GPIO3\_IO07** 0x401F81F0U, 0x5U, 0, 0, 0x401F83E0U
- #define **IOMUXC\_GPIO\_SD\_B1\_08\_USDHC2\_DATA4** 0x401F81F4U, 0x0U, 0x401F85F8U, 0x0U, 0x401F83E4U
- #define **IOMUXC\_GPIO\_SD\_B1\_08\_FLEXSPIA\_DATA00** 0x401F81F4U, 0x1U, 0x401F84-A8U, 0x0U, 0x401F83E4U
- #define **IOMUXC\_GPIO\_SD\_B1\_08\_LPUART7\_TX** 0x401F81F4U, 0x2U, 0x401F855CU, 0x0U, 0x401F83E4U
- #define **IOMUXC\_GPIO\_SD\_B1\_08\_SAI1\_TX\_BCLK** 0x401F81F4U, 0x3U, 0x401F85A8U, 0x0U, 0x401F83E4U
- #define **IOMUXC\_GPIO\_SD\_B1\_08\_LPSPi2\_SD0** 0x401F81F4U, 0x4U, 0x401F8508U, 0x0U, 0x401F83E4U
- #define **IOMUXC\_GPIO\_SD\_B1\_08\_GPIO3\_IO08** 0x401F81F4U, 0x5U, 0, 0, 0x401F83E4U
- #define **IOMUXC\_GPIO\_SD\_B1\_08\_SEMC\_CSX02** 0x401F81F4U, 0x6U, 0, 0, 0x401F83E4U
- #define **IOMUXC\_GPIO\_SD\_B1\_09\_USDHC2\_DATA5** 0x401F81F8U, 0x0U, 0x401F85FCU, 0x0U, 0x401F83E8U
- #define **IOMUXC\_GPIO\_SD\_B1\_09\_FLEXSPIA\_DATA01** 0x401F81F8U, 0x1U, 0x401F84A-CU, 0x0U, 0x401F83E8U
- #define **IOMUXC\_GPIO\_SD\_B1\_09\_LPUART7\_RX** 0x401F81F8U, 0x2U, 0x401F8558U, 0x0-U, 0x401F83E8U
- #define **IOMUXC\_GPIO\_SD\_B1\_09\_SAI1\_TX\_SYNC** 0x401F81F8U, 0x3U, 0x401F85ACU, 0x0U, 0x401F83E8U
- #define **IOMUXC\_GPIO\_SD\_B1\_09\_LPSPi2\_SDI** 0x401F81F8U, 0x4U, 0x401F8504U, 0x0U, 0x401F83E8U
- #define **IOMUXC\_GPIO\_SD\_B1\_09\_GPIO3\_IO09** 0x401F81F8U, 0x5U, 0, 0, 0x401F83E8U
- #define **IOMUXC\_GPIO\_SD\_B1\_10\_USDHC2\_DATA6** 0x401F81FCU, 0x0U, 0x401F8600U, 0x0U, 0x401F83ECU
- #define **IOMUXC\_GPIO\_SD\_B1\_10\_FLEXSPIA\_DATA02** 0x401F81FCU, 0x1U, 0x401F84-B0U, 0x0U, 0x401F83ECU
- #define **IOMUXC\_GPIO\_SD\_B1\_10\_LPUART2\_RX** 0x401F81FCU, 0x2U, 0x401F852CU, 0x0U, 0x401F83ECU
- #define **IOMUXC\_GPIO\_SD\_B1\_10\_LPI2C2\_SDA** 0x401F81FCU, 0x3U, 0x401F84D8U, 0x0-U, 0x401F83ECU
- #define **IOMUXC\_GPIO\_SD\_B1\_10\_LPSPi2\_PCS2** 0x401F81FCU, 0x4U, 0, 0, 0x401F83ECU
- #define **IOMUXC\_GPIO\_SD\_B1\_10\_GPIO3\_IO10** 0x401F81FCU, 0x5U, 0, 0, 0x401F83ECU
- #define **IOMUXC\_GPIO\_SD\_B1\_11\_USDHC2\_DATA7** 0x401F8200U, 0x0U, 0x401F8604U,

- #define **IOMUXC\_GPIO\_SD\_B1\_11\_FLEXSPIA\_DATA03** 0x401F8200U, 0x1U, 0x401F84-B4U, 0x0U, 0x401F83F0U
- #define **IOMUXC\_GPIO\_SD\_B1\_11\_LPUART2\_TX** 0x401F8200U, 0x2U, 0x401F8530U, 0x0-U, 0x401F83F0U
- #define **IOMUXC\_GPIO\_SD\_B1\_11\_LPI2C2\_SCL** 0x401F8200U, 0x3U, 0x401F84D4U, 0x0-U, 0x401F83F0U
- #define **IOMUXC\_GPIO\_SD\_B1\_11\_LPSPi2\_PCS3** 0x401F8200U, 0x4U, 0, 0, 0x401F83F0U
- #define **IOMUXC\_GPIO\_SD\_B1\_11\_GPIO3\_IO11** 0x401F8200U, 0x5U, 0, 0, 0x401F83F0U
- #define **IOMUXC\_SNVS\_WAKEUP\_GPIO5\_IO00** 0x400A8000U, 0x5U, 0, 0, 0x400A8018U
- #define **IOMUXC\_SNVS\_WAKEUP\_NMI** 0x400A8000U, 0x7U, 0x401F8568U, 0x1U, 0x400-A8018U
- #define **IOMUXC\_SNVS\_PMIC\_ON\_REQ\_SNVS\_PMIC\_ON\_REQ** 0x400A8004U, 0x0U, 0, 0, 0x400A801CU
- #define **IOMUXC\_SNVS\_PMIC\_ON\_REQ\_GPIO5\_IO01** 0x400A8004U, 0x5U, 0, 0, 0x400-A801CU
- #define **IOMUXC\_SNVS\_PMIC\_STBY\_REQ\_CCM\_PMIC\_STBY\_REQ** 0x400A8008U, 0x0-U, 0, 0, 0x400A8020U
- #define **IOMUXC\_SNVS\_PMIC\_STBY\_REQ\_GPIO5\_IO02** 0x400A8008U, 0x5U, 0, 0, 0x400-A8020U
- #define **IOMUXC\_SNVS\_TEST\_MODE** 0, 0, 0, 0, 0x400A800CU
- #define **IOMUXC\_SNVS\_POR\_B** 0, 0, 0, 0, 0x400A8010U
- #define **IOMUXC\_SNVS\_ONOFF** 0, 0, 0, 0x400A8014U

## Configuration

- static void **IOMUXC\_SetPinMux** (uint32\_t muxRegister, uint32\_t muxMode, uint32\_t inputRegister, uint32\_t inputDaisy, uint32\_t configRegister, uint32\_t inputOnfield)
 

*Sets the IOMUXC pin mux mode.*
- static void **IOMUXC\_SetPinConfig** (uint32\_t muxRegister, uint32\_t muxMode, uint32\_t inputRegister, uint32\_t inputDaisy, uint32\_t configRegister, uint32\_t configValue)
 

*Sets the IOMUXC pin configuration.*
- static void **IOMUXC\_EnableMode** (IOMUXC\_GPR\_Type \*base, uint32\_t mode, bool enable)
 

*Sets IOMUXC general configuration for some mode.*
- static void **IOMUXC\_SetSaiMClkClockSource** (IOMUXC\_GPR\_Type \*base, iomuxc\_gpr\_saimclk\_t mclk, uint8\_t clkSrc)
 

*Sets IOMUXC general configuration for SAI MCLK selection.*
- static void **IOMUXC\_MQSEEnterSoftwareReset** (IOMUXC\_GPR\_Type \*base, bool enable)
 

*Enters or exit MQS software reset.*
- static void **IOMUXC\_MQSEnable** (IOMUXC\_GPR\_Type \*base, bool enable)
 

*Enables or disables MQS.*
- static void **IOMUXC\_MQSConfig** (IOMUXC\_GPR\_Type \*base, iomuxc\_mqs\_pwm\_oversample\_rate\_t rate, uint8\_t divider)
 

*Configure MQS PWM oversampling rate compared with mclk and divider ratio control for mclk from hmclk.*

## 6.2 Macro Definition Documentation

### 6.2.1 #define FSL\_IOMUXC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 0))

## 6.3 Function Documentation

### 6.3.1 static void IOMUXC\_SetPinMux ( *uint32\_t muxRegister*, *uint32\_t muxMode*, *uint32\_t inputRegister*, *uint32\_t inputDaisy*, *uint32\_t configRegister*, *uint32\_t inputOnfield* ) [inline], [static]

Note

The first five parameters can be filled with the pin function ID macros.

This is an example to set the PTA6 as the lpuart0\_tx:

```
* IOMUXC_SetPinMux(IOMUXC_PTA6_LPUART0_TX, 0);
*
```

This is an example to set the PTA0 as GPIOA0:

```
* IOMUXC_SetPinMux(IOMUXC_PTA0_GPIOA0, 0);
*
```

Parameters

|                       |                            |
|-----------------------|----------------------------|
| <i>muxRegister</i>    | The pin mux register.      |
| <i>muxMode</i>        | The pin mux mode.          |
| <i>inputRegister</i>  | The select input register. |
| <i>inputDaisy</i>     | The input daisy.           |
| <i>configRegister</i> | The config register.       |
| <i>inputOnfield</i>   | Software input on field.   |

### 6.3.2 static void IOMUXC\_SetPinConfig ( *uint32\_t muxRegister*, *uint32\_t muxMode*, *uint32\_t inputRegister*, *uint32\_t inputDaisy*, *uint32\_t configRegister*, *uint32\_t configValue* ) [inline], [static]

Note

The previous five parameters can be filled with the pin function ID macros.

This is an example to set pin configuration for IOMUXC\_PTA3\_LPI2C0\_SCLS:

```
* IOMUXC_SetPinConfig(IOMUXC_PTA3_LPI2C0_SCLS, IOMUXC_SW_PAD_CTL_PAD_PUS_MASK |
    IOMUXC_SW_PAD_CTL_PAD_PUS(2U))
*
```

Parameters

|                       |                            |
|-----------------------|----------------------------|
| <i>muxRegister</i>    | The pin mux register.      |
| <i>muxMode</i>        | The pin mux mode.          |
| <i>inputRegister</i>  | The select input register. |
| <i>inputDaisy</i>     | The input daisy.           |
| <i>configRegister</i> | The config register.       |
| <i>configValue</i>    | The pin config value.      |

### 6.3.3 static void IOMUXC\_EnableMode( IOMUXC\_GPR\_Type \* *base*, uint32\_t *mode*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                       |
|---------------|-----------------------------------------------------------------------|
| <i>base</i>   | The IOMUXC GPR base address.                                          |
| <i>mode</i>   | The mode for setting. the mode is the logical OR of "iomuxc_gpr_mode" |
| <i>enable</i> | True enable false disable.                                            |

### 6.3.4 static void IOMUXC\_SetSaiMClkClockSource( IOMUXC\_GPR\_Type \* *base*, iomuxc\_gpr\_saimclk\_t *mclk*, uint8\_t *clkSrc* ) [inline], [static]

Parameters

|               |                                                                                      |
|---------------|--------------------------------------------------------------------------------------|
| <i>base</i>   | The IOMUXC GPR base address.                                                         |
| <i>mclk</i>   | The SAI MCLK.                                                                        |
| <i>clkSrc</i> | The clock source. Take refer to register setting details for the clock source in RM. |

### 6.3.5 static void IOMUXC\_MQSEnterSoftwareReset( IOMUXC\_GPR\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | The IOMUXC GPR base address.      |
| <i>enable</i> | Enter or exit MQS software reset. |

**6.3.6 static void IOMUXC\_MQSEnable ( IOMUXC\_GPR\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | The IOMUXC GPR base address. |
| <i>enable</i> | Enable or disable the MQS.   |

**6.3.7 static void IOMUXC\_MQSConfig ( IOMUXC\_GPR\_Type \* *base*,  
iomuxc\_mqs\_pwm\_oversample\_rate\_t *rate*, uint8\_t *divider* ) [inline],  
[static]**

Parameters

|                |                                                                                            |
|----------------|--------------------------------------------------------------------------------------------|
| <i>base</i>    | The IOMUXC GPR base address.                                                               |
| <i>rate</i>    | The MQS PWM oversampling rate, refer to "iomuxc_mqs_pwm_oversample_rate_t".                |
| <i>divider</i> | The divider ratio control for mclk from hmclk. mclk freq = 1 / (divider + 1) * hmclk freq. |

# Chapter 7

## ADC: 12-bit Analog to Digital Converter Driver

### 7.1 Overview

The MCUXpresso SDK provides a peripheral driver for the 12-bit Analog to Digital Converter (ADC) module of MCUXpresso SDK devices.

### 7.2 Typical use case

#### 7.2.1 Polling Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/fsl\_adc

#### 7.2.2 Polling Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/fsl\_adc

### Data Structures

- struct `adc_config_t`  
*Converter configuration. [More...](#)*
- struct `adc_offset_config_t`  
*Converter Offset configuration. [More...](#)*
- struct `adc_hardware_compare_config_t`  
*ADC hardware compare configuration. [More...](#)*
- struct `adc_channel_config_t`  
*ADC channel conversion configuration. [More...](#)*

### Macros

- #define `FSL_ADC_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 4)`)  
*ADC driver version.*

### Enumerations

- enum `adc_status_flags_t` {  
    `kADC_ConversionActiveFlag` = `ADC_GS_ADACT_MASK`,  
    `kADC_CalibrationFailedFlag` = `ADC_GS_CALF_MASK`,  
    `kADC_AsynchronousWakeupInterruptFlag` }  
*Converter's status flags.*

- enum `adc_reference_voltage_source_t` { `kADC_ReferenceVoltageSourceAlt0` = 0U }
 

*Reference voltage source.*
- enum `adc_sample_period_mode_t` {
 `kADC_SamplePeriod2or12Clocks` = 0U,  
`kADC_SamplePeriod4or16Clocks` = 1U,  
`kADC_SamplePeriod6or20Clocks` = 2U,  
`kADC_SamplePeriod8or24Clocks` = 3U,  
`kADC_SamplePeriodLong12Clcoks` = `kADC_SamplePeriod2or12Clocks`,  
`kADC_SamplePeriodLong16Clcoks` = `kADC_SamplePeriod4or16Clocks`,  
`kADC_SamplePeriodLong20Clcoks` = `kADC_SamplePeriod6or20Clocks`,  
`kADC_SamplePeriodLong24Clcoks` = `kADC_SamplePeriod8or24Clocks`,  
`kADC_SamplePeriodShort2Clocks` = `kADC_SamplePeriod2or12Clocks`,  
`kADC_SamplePeriodShort4Clocks` = `kADC_SamplePeriod4or16Clocks`,  
`kADC_SamplePeriodShort6Clocks` = `kADC_SamplePeriod6or20Clocks`,  
`kADC_SamplePeriodShort8Clocks` = `kADC_SamplePeriod8or24Clocks` }
 

*Sample time duration.*
- enum `adc_clock_source_t` {
 `kADC_ClockSourceIPG` = 0U,  
`kADC_ClockSourceIPGDiv2` = 1U,  
`kADC_ClockSourceAD` = 3U }
 

*Clock source.*
- enum `adc_clock_driver_t` {
 `kADC_ClockDriver1` = 0U,  
`kADC_ClockDriver2` = 1U,  
`kADC_ClockDriver4` = 2U,  
`kADC_ClockDriver8` = 3U }
 

*Clock divider for the converter.*
- enum `adc_resolution_t` {
 `kADC_Resolution8Bit` = 0U,  
`kADC_Resolution10Bit` = 1U,  
`kADC_Resolution12Bit` = 2U }
 

*Converter's resolution.*
- enum `adc_hardware_compare_mode_t` {
 `kADC_HardwareCompareMode0` = 0U,  
`kADC_HardwareCompareMode1` = 1U,  
`kADC_HardwareCompareMode2` = 2U,  
`kADC_HardwareCompareMode3` = 3U }
 

*Converter hardware compare mode.*
- enum `adc_hardware_average_mode_t` {
 `kADC_HardwareAverageCount4` = 0U,  
`kADC_HardwareAverageCount8` = 1U,  
`kADC_HardwareAverageCount16` = 2U,  
`kADC_HardwareAverageCount32` = 3U,  
`kADC_HardwareAverageDiasable` = 4U }
 

*Converter hardware average mode.*

## Initialization

- void `ADC_Init` (ADC\_Type \*base, const `adc_config_t` \*config)  
*Initialize the ADC module.*
- void `ADC_Deinit` (ADC\_Type \*base)  
*De-initializes the ADC module.*
- void `ADC_GetDefaultConfig` (`adc_config_t` \*config)  
*Gets an available pre-defined settings for the converter's configuration.*
- void `ADC_SetChannelConfig` (ADC\_Type \*base, uint32\_t channelGroup, const `adc_channel_config_t` \*config)  
*Configures the conversion channel.*
- static uint32\_t `ADC_GetChannelConversionValue` (ADC\_Type \*base, uint32\_t channelGroup)  
*Gets the conversion value.*
- static uint32\_t `ADC_GetChannelStatusFlags` (ADC\_Type \*base, uint32\_t channelGroup)  
*Gets the status flags of channel.*
- `status_t ADC_DoAutoCalibration` (ADC\_Type \*base)  
*Automates the hardware calibration.*
- void `ADC_SetOffsetConfig` (ADC\_Type \*base, const `adc_offset_config_t` \*config)  
*Set user defined offset.*
- static void `ADC_EnableDMA` (ADC\_Type \*base, bool enable)  
*Enables generating the DMA trigger when the conversion is complete.*
- static void `ADC_EnableHardwareTrigger` (ADC\_Type \*base, bool enable)  
*Enables the hardware trigger mode.*
- void `ADC_SetHardwareCompareConfig` (ADC\_Type \*base, const `adc_hardware_compare_config_t` \*config)  
*Configures the hardware compare mode.*
- void `ADC_SetHardwareAverageConfig` (ADC\_Type \*base, `adc_hardware_average_mode_t` mode)  
*Configures the hardware average mode.*
- static uint32\_t `ADC_GetStatusFlags` (ADC\_Type \*base)  
*Gets the converter's status flags.*
- void `ADC_ClearStatusFlags` (ADC\_Type \*base, uint32\_t mask)  
*Clears the converter's status flags.*

## 7.3 Data Structure Documentation

### 7.3.1 struct `adc_config_t`

#### Data Fields

- bool `enableOverWrite`  
*Enable the overwriting.*
- bool `enableContinuousConversion`  
*Enable the continuous conversion mode.*
- bool `enableHighSpeed`  
*Enable the high-speed mode.*
- bool `enableLowPower`  
*Enable the low power mode.*
- bool `enableLongSample`  
*Enable the long sample mode.*
- bool `enableAsynchronousClockOutput`

- **adc\_reference\_voltage\_source\_t referenceVoltageSource**  
*Select the reference voltage source.*
- **adc\_sample\_period\_mode\_t samplePeriodMode**  
*Select the sample period in long sample mode or short mode.*
- **adc\_clock\_source\_t clockSource**  
*Select the input clock source to generate the internal clock ADCK.*
- **adc\_clock\_driver\_t clockDriver**  
*Select the divide ratio used by the ADC to generate the internal clock ADCK.*
- **adc\_resolution\_t resolution**  
*Select the ADC resolution mode.*

## Field Documentation

- (1) **bool adc\_config\_t::enableOverWrite**
- (2) **bool adc\_config\_t::enableContinuousConversion**
- (3) **bool adc\_config\_t::enableHighSpeed**
- (4) **bool adc\_config\_t::enableLowPower**
- (5) **bool adc\_config\_t::enableLongSample**
- (6) **bool adc\_config\_t::enableAsynchronousClockOutput**
- (7) **adc\_reference\_voltage\_source\_t adc\_config\_t::referenceVoltageSource**
- (8) **adc\_sample\_period\_mode\_t adc\_config\_t::samplePeriodMode**
- (9) **adc\_clock\_source\_t adc\_config\_t::clockSource**
- (10) **adc\_clock\_driver\_t adc\_config\_t::clockDriver**
- (11) **adc\_resolution\_t adc\_config\_t::resolution**

### 7.3.2 struct adc\_offset\_config\_t

#### Data Fields

- **bool enableSigned**  
*if false,The offset value is added with the raw result.*
- **uint32\_t offsetYValue**  
*User configurable offset value(0-4095).*

## Field Documentation

- (1) **bool adc\_offset\_config\_t::enableSigned**

if true,The offset value is subtracted from the raw converted value.

(2) `uint32_t adc_offset_config_t::offsetValue`

### 7.3.3 struct adc\_hardware\_compare\_config\_t

In kADC\_HardwareCompareMode0, compare true if the result is less than the value1. In kADC\_HardwareCompareMode1, compare true if the result is greater than or equal to value1. In kADC\_HardwareCompareMode2, Value1 <= Value2, compare true if the result is less than value1 Or the result is Greater than value2. Value1 > Value2, compare true if the result is less than value1 And the result is Greater than value2. In kADC\_HardwareCompareMode3, Value1 <= Value2, compare true if the result is greater than or equal to value1 And the result is less than or equal to value2. Value1 > Value2, compare true if the result is greater than or equal to value1 Or the result is less than or equal to value2.

### Data Fields

- `adc_hardware_compare_mode_t hardwareCompareMode`  
*Select the hardware compare mode.*
- `uint16_t value1`  
*Setting value1(0-4095) for hardware compare mode.*
- `uint16_t value2`  
*Setting value2(0-4095) for hardware compare mode.*

### Field Documentation

(1) `adc_hardware_compare_mode_t adc_hardware_compare_config_t::hardwareCompareMode`

See "adc\_hardware\_compare\_mode\_t".

(2) `uint16_t adc_hardware_compare_config_t::value1`

(3) `uint16_t adc_hardware_compare_config_t::value2`

### 7.3.4 struct adc\_channel\_config\_t

### Data Fields

- `uint32_t channelNumber`  
*Setting the conversion channel number.*
- `bool enableInterruptOnConversionCompleted`  
*Generate an interrupt request once the conversion is completed.*

### Field Documentation

(1) `uint32_t adc_channel_config_t::channelNumber`

The available range is 0-31. See channel connection information for each chip in Reference Manual document.

(2) `bool adc_channel_config_t::enableInterruptOnConversionCompleted`

## 7.4 Macro Definition Documentation

### 7.4.1 `#define FSL_ADC_DRIVER_VERSION (MAKE_VERSION(2, 0, 4))`

Version 2.0.4.

## 7.5 Enumeration Type Documentation

### 7.5.1 `enum adc_status_flags_t`

Enumerator

*kADC\_ConversionActiveFlag* Conversion is active,not support w1c.

*kADC\_CalibrationFailedFlag* Calibration is failed,support w1c.

*kADC\_AsynchronousWakeupInterruptFlag* Asynchronous wakeup interrupt occurred, support w1c.

### 7.5.2 `enum adc_reference_voltage_source_t`

Enumerator

*kADC\_ReferenceVoltageSourceAlt0* For external pins pair of VrefH and VrefL.

### 7.5.3 `enum adc_sample_period_mode_t`

Enumerator

*kADC\_SamplePeriod2or12Clocks* Long sample 12 clocks or short sample 2 clocks.

*kADC\_SamplePeriod4or16Clocks* Long sample 16 clocks or short sample 4 clocks.

*kADC\_SamplePeriod6or20Clocks* Long sample 20 clocks or short sample 6 clocks.

*kADC\_SamplePeriod8or24Clocks* Long sample 24 clocks or short sample 8 clocks.

*kADC\_SamplePeriodLong12Clcoks* Long sample 12 clocks.

*kADC\_SamplePeriodLong16Clcoks* Long sample 16 clocks.

*kADC\_SamplePeriodLong20Clcoks* Long sample 20 clocks.

*kADC\_SamplePeriodLong24Clcoks* Long sample 24 clocks.

*kADC\_SamplePeriodShort2Clocks* Short sample 2 clocks.

*kADC\_SamplePeriodShort4Clocks* Short sample 4 clocks.

*kADC\_SamplePeriodShort6Clocks* Short sample 6 clocks.

*kADC\_SamplePeriodShort8Clocks* Short sample 8 clocks.

## 7.5.4 enum adc\_clock\_source\_t

Enumerator

*kADC\_ClockSourceIPG* Select IPG clock to generate ADCK.

*kADC\_ClockSourceIPGDiv2* Select IPG clock divided by 2 to generate ADCK.

*kADC\_ClockSourceAD* Select Asynchronous clock to generate ADCK.

## 7.5.5 enum adc\_clock\_driver\_t

Enumerator

*kADC\_ClockDriver1* For divider 1 from the input clock to the module.

*kADC\_ClockDriver2* For divider 2 from the input clock to the module.

*kADC\_ClockDriver4* For divider 4 from the input clock to the module.

*kADC\_ClockDriver8* For divider 8 from the input clock to the module.

## 7.5.6 enum adc\_resolution\_t

Enumerator

*kADC\_Resolution8Bit* Single End 8-bit resolution.

*kADC\_Resolution10Bit* Single End 10-bit resolution.

*kADC\_Resolution12Bit* Single End 12-bit resolution.

## 7.5.7 enum adc\_hardware\_compare\_mode\_t

Enumerator

*kADC\_HardwareCompareMode0* Compare true if the result is less than the value1.

*kADC\_HardwareCompareMode1* Compare true if the result is greater than or equal to value1.

*kADC\_HardwareCompareMode2* Value1 <= Value2, compare true if the result is less than value1  
Or the result is Greater than value2. Value1 > Value2, compare true if the result is less than  
value1 And the result is greater than value2

*kADC\_HardwareCompareMode3* Value1 <= Value2, compare true if the result is greater than or  
equal to value1 And the result is less than or equal to value2. Value1 > Value2, compare true if  
the result is greater than or equal to value1 Or the result is less than or equal to value2.

## 7.5.8 enum adc.hardware\_average\_mode\_t

Enumerator

- kADC\_HardwareAverageCount4*** For hardware average with 4 samples.
- kADC\_HardwareAverageCount8*** For hardware average with 8 samples.
- kADC\_HardwareAverageCount16*** For hardware average with 16 samples.
- kADC\_HardwareAverageCount32*** For hardware average with 32 samples.
- kADC\_HardwareAverageDiable*** Disable the hardware average function.

## 7.6 Function Documentation

### 7.6.1 void ADC\_Init ( ADC\_Type \* *base*, const adc\_config\_t \* *config* )

Parameters

|               |                                      |
|---------------|--------------------------------------|
| <i>base</i>   | ADC peripheral base address.         |
| <i>config</i> | Pointer to "adc_config_t" structure. |

### 7.6.2 void ADC\_Deinit ( ADC\_Type \* *base* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | ADC peripheral base address. |
|-------------|------------------------------|

### 7.6.3 void ADC\_GetDefaultConfig ( adc\_config\_t \* *config* )

This function initializes the converter configuration structure with available settings. The default values are:

```
* config->enableAsynchronousClockOutput = true;
* config->enableOverWrite = false;
* config->enableContinuousConversion = false;
* config->enableHighSpeed = false;
* config->enableLowPower = false;
* config->enableLongSample = false;
* config->referenceVoltageSource =
  kADC_ReferenceVoltageSourceAlt0;
* config->samplePeriodMode =
  kADC_SamplePeriod2or12Clocks;
* config->clockSource =
  kADC_ClockSourceAD;
* config->clockDriver =
  kADC_ClockDriver1;
* config->resolution =
  kADC_Resolution12Bit;
```

## Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

#### 7.6.4 void ADC\_SetChannelConfig ( **ADC\_Type** \* *base*, **uint32\_t** *channelGroup*, **const adc\_channel\_config\_t** \* *config* )

This operation triggers the conversion when in software trigger mode. When in hardware trigger mode, this API configures the channel while the external trigger source helps to trigger the conversion.

Note that the "Channel Group" has a detailed description. To allow sequential conversions of the ADC to be triggered by internal peripherals, the ADC has more than one group of status and control registers, one for each conversion. The channel group parameter indicates which group of registers are used, for example channel group 0 is for Group A registers and channel group 1 is for Group B registers. The channel groups are used in a "ping-pong" approach to control the ADC operation. At any point, only one of the channel groups is actively controlling ADC conversions. The channel group 0 is used for both software and hardware trigger modes. Channel groups 1 and greater indicate potentially multiple channel group registers for use only in hardware trigger mode. See the chip configuration information in the appropriate MCU reference manual about the number of SC1n registers (channel groups) specific to this device. None of the channel groups 1 or greater are used for software trigger operation. Therefore, writing to these channel groups does not initiate a new conversion. Updating the channel group 0 while a different channel group is actively controlling a conversion is allowed and vice versa. Writing any of the channel group registers while that specific channel group is actively controlling a conversion aborts the current conversion.

## Parameters

|                     |                                                                             |
|---------------------|-----------------------------------------------------------------------------|
| <i>base</i>         | ADC peripheral base address.                                                |
| <i>channelGroup</i> | Channel group index.                                                        |
| <i>config</i>       | Pointer to the "adc_channel_config_t" structure for the conversion channel. |

#### 7.6.5 static uint32\_t ADC\_GetChannelConversionValue ( **ADC\_Type** \* *base*, **uint32\_t** *channelGroup* ) [inline], [static]

## Parameters

|                     |                              |
|---------------------|------------------------------|
| <i>base</i>         | ADC peripheral base address. |
| <i>channelGroup</i> | Channel group index.         |

Returns

Conversion value.

### 7.6.6 static uint32\_t ADC\_GetChannelStatusFlags ( ADC\_Type \* *base*, uint32\_t *channelGroup* ) [inline], [static]

A conversion is completed when the result of the conversion is transferred into the data result registers. (provided the compare function & hardware averaging is disabled), this is indicated by the setting of COCOn. If hardware averaging is enabled, COCOn sets only, if the last of the selected number of conversions is complete. If the compare function is enabled, COCOn sets and conversion result data is transferred only if the compare condition is true. If both hardware averaging and compare functions are enabled, then COCOn sets only if the last of the selected number of conversions is complete and the compare condition is true.

Parameters

|                     |                              |
|---------------------|------------------------------|
| <i>base</i>         | ADC peripheral base address. |
| <i>channelGroup</i> | Channel group index.         |

Returns

Status flags of channel.return 0 means COCO flag is 0,return 1 means COCOflag is 1.

### 7.6.7 status\_t ADC\_DoAutoCalibration ( ADC\_Type \* *base* )

This auto calibration helps to adjust the plus/minus side gain automatically. Execute the calibration before using the converter. Note that the software trigger should be used during calibration.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | ADC peripheral base address. |
|-------------|------------------------------|

Returns

Execution status.

Return values

|                        |                                   |
|------------------------|-----------------------------------|
| <i>kStatus_Success</i> | Calibration is done successfully. |
| <i>kStatus_Fail</i>    | Calibration has failed.           |

### 7.6.8 void ADC\_SetOffsetConfig ( ADC\_Type \* *base*, const adc\_offset\_config\_t \* *config* )

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | ADC peripheral base address.                |
| <i>config</i> | Pointer to "adc_offset_config_t" structure. |

### 7.6.9 static void ADC\_EnableDMA ( ADC\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                               |
|---------------|-------------------------------------------------------------------------------|
| <i>base</i>   | ADC peripheral base address.                                                  |
| <i>enable</i> | Switcher of the DMA feature. "true" means enabled, "false" means not enabled. |

### 7.6.10 static void ADC\_EnableHardwareTrigger ( ADC\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                                                |
|---------------|------------------------------------------------------------------------------------------------|
| <i>base</i>   | ADC peripheral base address.                                                                   |
| <i>enable</i> | Switcher of the trigger mode. "true" means hardware trigger mode, "false" means software mode. |

### 7.6.11 void ADC\_SetHardwareCompareConfig ( ADC\_Type \* *base*, const adc\_hardware\_compare\_config\_t \* *config* )

The hardware compare mode provides a way to process the conversion result automatically by using hardware. Only the result in the compare range is available. To compare the range, see "adc\_hardware\_compare\_mode\_t" or the appropriate reference manual for more information.

Parameters

|               |                                                       |
|---------------|-------------------------------------------------------|
| <i>base</i>   | ADC peripheral base address.                          |
| <i>config</i> | Pointer to "adc_hardware_compare_config_t" structure. |

### 7.6.12 void ADC\_SetHardwareAverageConfig ( ADC\_Type \* *base*, adc.hardware\_average\_mode\_t *mode* )

The hardware average mode provides a way to process the conversion result automatically by using hardware. The multiple conversion results are accumulated and averaged internally making them easier to read.

Parameters

|             |                                                                       |
|-------------|-----------------------------------------------------------------------|
| <i>base</i> | ADC peripheral base address.                                          |
| <i>mode</i> | Setting the hardware average mode. See "adc.hardware_average_mode_t". |

### 7.6.13 static uint32\_t ADC\_GetStatusFlags ( ADC\_Type \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | ADC peripheral base address. |
|-------------|------------------------------|

Returns

Flags' mask if indicated flags are asserted. See "adc\_status\_flags\_t".

### 7.6.14 void ADC\_ClearStatusFlags ( ADC\_Type \* *base*, uint32\_t *mask* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | ADC peripheral base address. |
|-------------|------------------------------|

|             |                                                             |
|-------------|-------------------------------------------------------------|
| <i>mask</i> | Mask value for the cleared flags. See "adc_status_flags_t". |
|-------------|-------------------------------------------------------------|

# Chapter 8

## ADC\_ETC: ADC External Trigger Control

### 8.1 Overview

The MCUXpresso SDK provides a peripheral driver for the ADC\_ETC module of MCUXpresso SDK devices.

### 8.2 Typical use case

#### 8.2.1 Software trigger Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/adc\_etc

#### 8.2.2 Hardware trigger Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/adc\_etc

## Data Structures

- struct `adc_etc_config_t`  
*ADC\_ETC configuration. [More...](#)*
- struct `adc_etc_trigger_chain_config_t`  
*ADC\_ETC trigger chain configuration. [More...](#)*
- struct `adc_etc_trigger_config_t`  
*ADC\_ETC trigger configuration. [More...](#)*

## Macros

- `#define FSL_ADC_ETC_DRIVER_VERSION (MAKE_VERSION(2, 2, 1))`  
*ADC\_ETC driver version.*
- `#define ADC_ETC_DMA_CTRL_TRGn_REQ_MASK 0xFF0000U`  
*The mask of status flags cleared by writing 1.*

## Enumerations

- enum `_adc_etc_status_flag_mask`  
*ADC\_ETC customized status flags mask.*
- enum `adc_etc_external_trigger_source_t`  
*External triggers sources.*
- enum `adc_etc_interrupt_enable_t`  
*Interrupt enable/disable mask.*

- enum [adc\\_etc\\_dma\\_mode\\_selection\\_t](#)  
*DMA mode selection.*

## Initialization

- void [ADC\\_ETC\\_Init](#) (ADC\_ETC\_Type \*base, const adc\_etc\_config\_t \*config)  
*Initialize the ADC\_ETC module.*
- void [ADC\\_ETC\\_Deinit](#) (ADC\_ETC\_Type \*base)  
*De-Initialize the ADC\_ETC module.*
- void [ADC\\_ETC\\_GetDefaultConfig](#) (adc\_etc\_config\_t \*config)  
*Gets an available pre-defined settings for the ADC\_ETC's configuration.*
- void [ADC\\_ETC\\_SetTriggerConfig](#) (ADC\_ETC\_Type \*base, uint32\_t triggerGroup, const adc\_etc\_trigger\_config\_t \*config)  
*Set the external XBAR trigger configuration.*
- void [ADC\\_ETC\\_SetTriggerChainConfig](#) (ADC\_ETC\_Type \*base, uint32\_t triggerGroup, uint32\_t chainGroup, const adc\_etc\_trigger\_chain\_config\_t \*config)  
*Set the external XBAR trigger chain configuration.*
- uint32\_t [ADC\\_ETC\\_GetInterruptStatusFlags](#) (ADC\_ETC\_Type \*base, adc\_etc\_external\_trigger\_source\_t sourceIndex)  
*Gets the interrupt status flags of external XBAR and TSC triggers.*
- void [ADC\\_ETC\\_ClearInterruptStatusFlags](#) (ADC\_ETC\_Type \*base, adc\_etc\_external\_trigger\_source\_t sourceIndex, uint32\_t mask)  
*Clears the ADC\_ETC's interrupt status falgs.*
- static void [ADC\\_ETC\\_EnableDMA](#) (ADC\_ETC\_Type \*base, uint32\_t triggerGroup)  
*Enable the DMA corresponding to each trigger source.*
- static void [ADC\\_ETC\\_DisableDMA](#) (ADC\_ETC\_Type \*base, uint32\_t triggerGroup)  
*Disable the DMA corresponding to each trigger sources.*
- static uint32\_t [ADC\\_ETC\\_GetDMAStatusFlags](#) (ADC\_ETC\_Type \*base)  
*Get the DMA request status falgs.*
- static void [ADC\\_ETC\\_ClearDMAStatusFlags](#) (ADC\_ETC\_Type \*base, uint32\_t mask)  
*Clear the DMA request status falgs.*
- static void [ADC\\_ETC\\_DoSoftwareReset](#) (ADC\_ETC\_Type \*base, bool enable)  
*When enable, all logical will be reset.*
- static void [ADC\\_ETC\\_DoSoftwareTrigger](#) (ADC\_ETC\_Type \*base, uint32\_t triggerGroup)  
*Do software trigger corresponding to each XBAR trigger sources.*
- uint32\_t [ADC\\_ETC\\_GetADCConversionValue](#) (ADC\_ETC\_Type \*base, uint32\_t triggerGroup, uint32\_t chainGroup)  
*Get ADC conversion result from external XBAR sources.*

## 8.3 Data Structure Documentation

### 8.3.1 struct adc\_etc\_config\_t

### 8.3.2 struct adc\_etc\_trigger\_chain\_config\_t

### 8.3.3 struct adc\_etc\_trigger\_config\_t

## 8.4 Macro Definition Documentation

### 8.4.1 #define FSL\_ADC\_ETC\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 1))

Version 2.2.1.

### 8.4.2 #define ADC\_ETC\_DMA\_CTRL\_TRGn\_REQ\_MASK 0xFF0000U

## 8.5 Function Documentation

### 8.5.1 void ADC\_ETC\_Init ( ADC\_ETC\_Type \* *base*, const adc\_etc\_config\_t \* *config* )

Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>base</i>   | ADC_ETC peripheral base address.         |
| <i>config</i> | Pointer to "adc_etc_config_t" structure. |

### 8.5.2 void ADC\_ETC\_Deinit ( ADC\_ETC\_Type \* *base* )

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | ADC_ETC peripheral base address. |
|-------------|----------------------------------|

### 8.5.3 void ADC\_ETC\_GetDefaultConfig ( adc\_etc\_config\_t \* *config* )

This function initializes the ADC\_ETC's configuration structure with available settings. The default values are:

```
* config->enableTSCBypass = true;
* config->enableTSC0Trigger = false;
* config->enableTSC1Trigger = false;
* config->TSC0triggerPriority = 0U;
* config->TSC1triggerPriority = 0U;
* config->clockPreDivider = 0U;
* config->XBARtriggerMask = 0U;
*
```

Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>config</i> | Pointer to "adc_etc_config_t" structure. |
|---------------|------------------------------------------|

#### 8.5.4 void ADC\_ETC\_SetTriggerConfig ( **ADC\_ETC\_Type** \* *base*, **uint32\_t** *triggerGroup*, **const adc\_etc\_trigger\_config\_t** \* *config* )

Parameters

|                     |                                                  |
|---------------------|--------------------------------------------------|
| <i>base</i>         | ADC_ETC peripheral base address.                 |
| <i>triggerGroup</i> | Trigger group index.                             |
| <i>config</i>       | Pointer to "adc_etc_trigger_config_t" structure. |

#### 8.5.5 void ADC\_ETC\_SetTriggerChainConfig ( **ADC\_ETC\_Type** \* *base*, **uint32\_t** *triggerGroup*, **uint32\_t** *chainGroup*, **const adc\_etc\_trigger\_chain\_config\_t** \* *config* )

For example, if triggerGroup is set to 0U and chainGroup is set to 1U, which means Trigger0 source's chain1 would be configurated.

Parameters

|                     |                                                        |
|---------------------|--------------------------------------------------------|
| <i>base</i>         | ADC_ETC peripheral base address.                       |
| <i>triggerGroup</i> | Trigger group index. Available number is 0~7.          |
| <i>chainGroup</i>   | Trigger chain group index. Available number is 0~7.    |
| <i>config</i>       | Pointer to "adc_etc_trigger_chain_config_t" structure. |

#### 8.5.6 **uint32\_t** ADC\_ETC\_GetInterruptStatusFlags ( **ADC\_ETC\_Type** \* *base*, **adc\_etc\_external\_trigger\_source\_t** *sourceIndex* )

Parameters

|                    |                                  |
|--------------------|----------------------------------|
| <i>base</i>        | ADC_ETC peripheral base address. |
| <i>sourceIndex</i> | trigger source index.            |

Returns

Status flags mask of trigger. Refer to "\_adc\_etc\_status\_flag\_mask".

#### 8.5.7 void ADC\_ETC\_ClearInterruptStatusFlags ( ADC\_ETC\_Type \* *base*, adc\_etc\_external\_trigger\_source\_t *sourceIndex*, uint32\_t *mask* )

Parameters

|                    |                                                                     |
|--------------------|---------------------------------------------------------------------|
| <i>base</i>        | ADC_ETC peripheral base address.                                    |
| <i>sourceIndex</i> | trigger source index.                                               |
| <i>mask</i>        | Status flags mask of trigger. Refer to "_adc_etc_status_flag_mask". |

#### 8.5.8 static void ADC\_ETC\_EnableDMA ( ADC\_ETC\_Type \* *base*, uint32\_t *triggerGroup* ) [inline], [static]

Parameters

|                     |                                               |
|---------------------|-----------------------------------------------|
| <i>base</i>         | ADC_ETC peripheral base address.              |
| <i>triggerGroup</i> | Trigger group index. Available number is 0~7. |

#### 8.5.9 static void ADC\_ETC\_DisableDMA ( ADC\_ETC\_Type \* *base*, uint32\_t *triggerGroup* ) [inline], [static]

Parameters

|                     |                                               |
|---------------------|-----------------------------------------------|
| <i>base</i>         | ADC_ETC peripheral base address.              |
| <i>triggerGroup</i> | Trigger group index. Available number is 0~7. |

#### 8.5.10 static uint32\_t ADC\_ETC\_GetDMAStatusFlags ( ADC\_ETC\_Type \* *base* ) [inline], [static]

Only external XBAR sources support DMA request.

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | ADC_ETC peripheral base address. |
|-------------|----------------------------------|

Returns

Mask of external XBAR trigger's DMA request asserted flags. Available range is trigger0:0x01 to trigger7:0x80.

### 8.5.11 static void ADC\_ETC\_ClearDMAStatusFlags ( ADC\_ETC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Only external XBAR sources support DMA request.

Parameters

|             |                                                                                                                |
|-------------|----------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ADC_ETC peripheral base address.                                                                               |
| <i>mask</i> | Mask of external XBAR trigger's DMA request asserted flags. Available range is trigger0:0x01 to trigger7:0x80. |

### 8.5.12 static void ADC\_ETC\_DoSoftwareReset ( ADC\_ETC\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                    |
|---------------|------------------------------------|
| <i>base</i>   | ADC_ETC peripheral base address.   |
| <i>enable</i> | Enable/Disable the software reset. |

### 8.5.13 static void ADC\_ETC\_DoSoftwareTrigger ( ADC\_ETC\_Type \* *base*, uint32\_t *triggerGroup* ) [inline], [static]

Each XBAR trigger sources can be configured as HW or SW trigger mode. In hardware trigger mode, trigger source is from XBAR. In software mode, trigger source is from software trigger. TSC trigger sources can only work in hardware trigger mode.

Parameters

|                     |                                               |
|---------------------|-----------------------------------------------|
| <i>base</i>         | ADC_ETC peripheral base address.              |
| <i>triggerGroup</i> | Trigger group index. Available number is 0~7. |

### 8.5.14 **uint32\_t ADC\_ETC\_GetADCConversionValue ( ADC\_ETC\_Type \* *base*, uint32\_t *triggerGroup*, uint32\_t *chainGroup* )**

For example, if triggerGroup is set to 0U and chainGroup is set to 1U, which means the API would return Trigger0 source's chain1 conversion result.

Parameters

|                     |                                                     |
|---------------------|-----------------------------------------------------|
| <i>base</i>         | ADC_ETC peripheral base address.                    |
| <i>triggerGroup</i> | Trigger group index. Available number is 0~7.       |
| <i>chainGroup</i>   | Trigger chain group index. Available number is 0~7. |

Returns

ADC conversion result value.

# Chapter 9

## AIPSTZ: AHB to IP Bridge

### 9.1 Overview

The MCUXpresso SDK provides a driver for the AHB-to-IP Bridge (AIPSTZ) of MCUXpresso SDK devices.

### Enumerations

- enum `aipstz_master_privilege_level_t`{  
    `kAIPSTZ_MasterBufferedWriteEnable` = (1U << 3),  
    `kAIPSTZ_MasterTrustedForReadEnable` = (1U << 2),  
    `kAIPSTZ_MasterTrustedForWriteEnable` = (1U << 1),  
    `kAIPSTZ_MasterForceUserModeEnable` = 1U }  
    *List of AIPSTZ privilege configuration.*
- enum `aipstz_master_t`  
    *List of AIPSTZ masters.*
- enum `aipstz_peripheral_access_control_t`  
    *List of AIPSTZ peripheral access control configuration.*
- enum `aipstz_peripheral_t`  
    *List of AIPSTZ peripherals.*

### Driver version

- #define `FSL_AIPSTZ_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 1)`)  
*Version 2.0.1.*

### Initialization and deinitialization

- void `AIPSTZ_SetMasterPriviledgeLevel` (`AIPSTZ_Type` \*base, `aipstz_master_t` master, `uint32_t` privilegeConfig)  
    *Configure the privilege level for master.*
- void `AIPSTZ_SetPeripheralAccessControl` (`AIPSTZ_Type` \*base, `aipstz_peripheral_t` peripheral, `uint32_t` accessControl)  
    *Configure the access for peripheral.*

### 9.2 Enumeration Type Documentation

#### 9.2.1 enum `aipstz_master_privilege_level_t`

Enumerator

**`kAIPSTZ_MasterBufferedWriteEnable`** Write accesses from this master are allowed to be buffered.

*kAIPSTZ\_MasterTrustedForReadEnable* This master is trusted for read accesses.

*kAIPSTZ\_MasterTrustedForWriteEnable* This master is trusted for write accesses.

*kAIPSTZ\_MasterForceUserModeEnable* Accesses from this master are forced to user-mode.

## 9.2.2 enum aipstz\_master\_t

Organized by width for the 8-15 bits and shift for lower 8 bits.

## 9.2.3 enum aipstz\_peripheral\_access\_control\_t

## 9.2.4 enum aipstz\_peripheral\_t

Organized by register offset for higher 32 bits, width for the 8-15 bits and shift for lower 8 bits.

## 9.3 Function Documentation

### 9.3.1 void AIPSTZ\_SetMasterPriviledgeLevel ( *AIPSTZ\_Type \* base*, *aipstz\_master\_t master*, *uint32\_t privilegeConfig* )

Parameters

|                        |                                                                              |
|------------------------|------------------------------------------------------------------------------|
| <i>base</i>            | AIPSTZ peripheral base pointer                                               |
| <i>master</i>          | Masters for AIPSTZ.                                                          |
| <i>privilegeConfig</i> | Configuration is ORed from <a href="#">aipstz_master_privilege_level_t</a> . |

### 9.3.2 void AIPSTZ\_SetPeripheralAccessControl ( *AIPSTZ\_Type \* base*, *aipstz\_peripheral\_t peripheral*, *uint32\_t accessControl* )

Parameters

|                   |                                |
|-------------------|--------------------------------|
| <i>base</i>       | AIPSTZ peripheral base pointer |
| <i>peripheral</i> | Peripheral for AIPSTZ.         |

|                      |                                                                                 |
|----------------------|---------------------------------------------------------------------------------|
| <i>accessControl</i> | Configuration is ORed from <a href="#">aipstz_peripheral_access_control_t</a> . |
|----------------------|---------------------------------------------------------------------------------|

# Chapter 10

## AOI: Crossbar AND/OR/INVERT Driver

### 10.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Crossbar AND/OR/INVERT (AOI) block of MCUXpresso SDK devices.

The AOI module supports a configurable number of event outputs, where each event output represents a user-programmed combinational boolean function based on four event inputs. The key features of this module include:

- Four dedicated inputs for each event output
- User-programmable combinational boolean function evaluation for each event output
- Memory-mapped device connected to a slave peripheral (IPS) bus
- Configurable number of event outputs

### 10.2 Function groups

#### 10.2.1 AOI Initialization

To initialize the AOI driver, call the [AOI\\_Init\(\)](#) function and pass a baseaddr pointer.

See the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/aoi.

#### 10.2.2 AOI Get Set Operation

The AOI module provides a universal boolean function generator using a four-term sum of products expression with each product term containing true or complement values of the four selected event inputs (A, B, C, D). The AOI is a highly programmable module for creating combinational boolean outputs for use as hardware triggers. Each selected input term in each product term can be configured to produce a logical 0 or 1 or pass the true or complement of the selected event input. To configure the selected AOI module event, call the API of the [AOI\\_SetEventLogicConfig\(\)](#) function. To get the current event state configure, call the API of [AOI\\_GetEventLogicConfig\(\)](#) function. The AOI module does not support any special modes of operation. See the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/aoi.

### 10.3 Typical use case

The AOI module is designed to be integrated in conjunction with one or more inter-peripheral crossbar switch (XBAR) modules. A crossbar switch is typically used to select the 4\*n AOI inputs from among available peripheral outputs and GPIO signals. The n EVENTn outputs from the AOI module are typically

used as additional inputs to a second crossbar switch, adding to it the ability to connect to its outputs an arbitrary 4-input boolean function of its other inputs.

This is an example to initialize and configure the AOI driver for a possible use case. Because the AOI module function is directly connected with an XBAR (Inter-peripheral crossbar) module, other peripheral drivers (PIT, CMP, and XBAR) are used to show full functionality of AOI module.

For example: Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver-examples/aoi

## Data Structures

- struct `aoi_event_config_t`  
*AOI event configuration structure. [More...](#)*

## Macros

- #define `AOI` AOI0  
*AOI peripheral address.*

## Enumerations

- enum `aoi_input_config_t` {
   
`kAOI_LogicZero` = 0x0U,  
`kAOI_InputSignal` = 0x1U,  
`kAOI_InvInputSignal` = 0x2U,  
`kAOI_LogicOne` = 0x3U }
   
*AOI input configurations.*
- enum `aoi_event_t` {
   
`kAOI_Event0` = 0x0U,  
`kAOI_Event1` = 0x1U,  
`kAOI_Event2` = 0x2U,  
`kAOI_Event3` = 0x3U }
   
*AOI event indexes, where an event is the collection of the four product terms (0, 1, 2, and 3) and the four signal inputs (A, B, C, and D).*

## Driver version

- #define `FSL_AOI_DRIVER_VERSION` (MAKE\_VERSION(2, 0, 1))  
*Version 2.0.1.*

## AOI Initialization

- void `AOI_Init` (AOI\_Type \*base)  
*Initializes an AOI instance for operation.*
- void `AOI_Deinit` (AOI\_Type \*base)  
*Deinitializes an AOI instance for operation.*

## AOI Get Set Operation

- void [AOI\\_GetEventLogicConfig](#) (AOI\_Type \*base, aoi\_event\_t event, aoi\_event\_config\_t \*config)  
*Gets the Boolean evaluation associated.*
- void [AOI\\_SetEventLogicConfig](#) (AOI\_Type \*base, aoi\_event\_t event, const aoi\_event\_config\_t \*eventConfig)  
*Configures an AOI event.*

## 10.4 Data Structure Documentation

### 10.4.1 struct aoi\_event\_config\_t

Defines structure \_aoi\_event\_config and use the [AOI\\_SetEventLogicConfig\(\)](#) function to make whole event configuration.

#### Data Fields

- aoi\_input\_config\_t PT0AC  
*Product term 0 input A.*
- aoi\_input\_config\_t PT0BC  
*Product term 0 input B.*
- aoi\_input\_config\_t PT0CC  
*Product term 0 input C.*
- aoi\_input\_config\_t PT0DC  
*Product term 0 input D.*
- aoi\_input\_config\_t PT1AC  
*Product term 1 input A.*
- aoi\_input\_config\_t PT1BC  
*Product term 1 input B.*
- aoi\_input\_config\_t PT1CC  
*Product term 1 input C.*
- aoi\_input\_config\_t PT1DC  
*Product term 1 input D.*
- aoi\_input\_config\_t PT2AC  
*Product term 2 input A.*
- aoi\_input\_config\_t PT2BC  
*Product term 2 input B.*
- aoi\_input\_config\_t PT2CC  
*Product term 2 input C.*
- aoi\_input\_config\_t PT2DC  
*Product term 2 input D.*
- aoi\_input\_config\_t PT3AC  
*Product term 3 input A.*
- aoi\_input\_config\_t PT3BC  
*Product term 3 input B.*
- aoi\_input\_config\_t PT3CC  
*Product term 3 input C.*
- aoi\_input\_config\_t PT3DC  
*Product term 3 input D.*

## 10.5 Macro Definition Documentation

### 10.5.1 #define FSL\_AOI\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

## 10.6 Enumeration Type Documentation

### 10.6.1 enum aoi\_input\_config\_t

The selection item represents the Boolean evaluations.

Enumerator

*kAOI\_LogicZero* Forces the input to logical zero.

*kAOI\_InputSignal* Passes the input signal.

*kAOI\_InvInputSignal* Inverts the input signal.

*kAOI\_LogicOne* Forces the input to logical one.

### 10.6.2 enum aoi\_event\_t

Enumerator

*kAOI\_Event0* Event 0 index.

*kAOI\_Event1* Event 1 index.

*kAOI\_Event2* Event 2 index.

*kAOI\_Event3* Event 3 index.

## 10.7 Function Documentation

### 10.7.1 void AOI\_Init ( AOI\_Type \* *base* )

This function un-gates the AOI clock.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | AOI peripheral address. |
|-------------|-------------------------|

### 10.7.2 void AOI\_Deinit ( AOI\_Type \* *base* )

This function shutdowns AOI module.

## Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | AOI peripheral address. |
|-------------|-------------------------|

### 10.7.3 void AOI\_GetEventLogicConfig ( AOI\_Type \* *base*, aoi\_event\_t *event*, aoi\_event\_config\_t \* *config* )

This function returns the Boolean evaluation associated.

Example:

```
aoi_event_config_t demoEventLogicStruct;
AOI_GetEventLogicConfig(AOI, kAOI_Event0, &demoEventLogicStruct);
```

## Parameters

|               |                                                           |
|---------------|-----------------------------------------------------------|
| <i>base</i>   | AOI peripheral address.                                   |
| <i>event</i>  | Index of the event which will be set of type aoi_event_t. |
| <i>config</i> | Selected input configuration .                            |

### 10.7.4 void AOI\_SetEventLogicConfig ( AOI\_Type \* *base*, aoi\_event\_t *event*, const aoi\_event\_config\_t \* *eventConfig* )

This function configures an AOI event according to the aoiEventConfig structure. This function configures all inputs (A, B, C, and D) of all product terms (0, 1, 2, and 3) of a desired event.

Example:

```
aoi_event_config_t demoEventLogicStruct;
demoEventLogicStruct.PT0AC = kAOI_InvInputSignal;
demoEventLogicStruct.PT0BC = kAOI_InputSignal;
demoEventLogicStruct.PT0CC = kAOI_LogicOne;
demoEventLogicStruct.PT0DC = kAOI_LogicOne;

demoEventLogicStruct.PT1AC = kAOI_LogicZero;
demoEventLogicStruct.PT1BC = kAOI_LogicOne;
demoEventLogicStruct.PT1CC = kAOI_LogicOne;
demoEventLogicStruct.PT1DC = kAOI_LogicOne;

demoEventLogicStruct.PT2AC = kAOI_LogicZero;
demoEventLogicStruct.PT2BC = kAOI_LogicOne;
demoEventLogicStruct.PT2CC = kAOI_LogicOne;
demoEventLogicStruct.PT2DC = kAOI_LogicOne;

demoEventLogicStruct.PT3AC = kAOI_LogicZero;
demoEventLogicStruct.PT3BC = kAOI_LogicOne;
demoEventLogicStruct.PT3CC = kAOI_LogicOne;
```

```
demoEventLogicStruct.PT3DC = kAOI_LogicOne;  
AOI_SetEventLogicConfig(AOI, kAOI_Event0, demoEventLogicStruct);
```

## Parameters

|                    |                                                                                                                                                               |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>        | AOI peripheral address.                                                                                                                                       |
| <i>event</i>       | Event which will be configured of type aoi_event_t.                                                                                                           |
| <i>eventConfig</i> | Pointer to type aoi_event_config_t structure. The user is responsible for filling out the members of this structure and passing the pointer to this function. |

# Chapter 11

## BEE: Bus Encryption Engine

### 11.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Bus Encryption Engine (BEE) module.

The BEE module is implemented as an on-the-fly decryption engine. The main features of the BEE module are:

- Standard AXI interconnection
- On-the-fly AES-128 decryption, supporting ECB and CTR mode
- Aliased memory space support. Address remapping for up to two individual regions
- Independent AES Key management for those two individual regions
- Bus access pattern optimization with the aid of local store and forward buffer
- Non-secured access filtering based on security label of the access
- Illegal access check and filtering.

The known hardware limitations of the BEE module are as follows:

- Only supports 128 bits data width AXI interconnection
- Only supports 16-byte burst access size. For a single transaction, the minimum supported access size is limited to 4 bytes.
- Granularity of the address bias is 128 KB per step

### 11.2 BEE Driver Initialization and Configuration

The function `BEE_Init()` initializes the BEE to default values. The function `BEE_GetDefaultConfig()` loads default values to the BEE configuration structure. The default values are described below.

See the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/bee. The function `BEE_Deinit()` performs a hardware reset of BEE module and disables clocks. Configuration and keys from software for both regions are cleared.

### 11.3 Enable & Disable BEE

The function `BEE_Enable()` enables decryption using BEE. The function `BEE_Disable()` disables decryption using BEE.

### 11.4 Set BEE region config and key

The function `BEE_SetConfig()` sets BEE settings according to given configuration structure. The structure is described below.

See the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/bee. The function `BEE_SetRegionKey()` loads given AES key to BEE register for the given region. The key must be 32-bit aligned and stored in little-endian format. Note that eFuse BEE\_KEYx\_SEL must be set

accordingly to be able to load and use the key loaded in BEE registers. Otherwise, the key cannot be loaded and BEE uses the key from OTPMK or SW\_GP2.

The function [BEE\\_SetRegionNonce\(\)](#) loads given AES nonce (used only for AES CTR mode) to BEE register for the given region. The nonce must be 32-bit aligned and stored in little-endian format.

## 11.5 Status

Provides functions to get and clear the BEE status.

The function [BEE\\_GetStatusFlags\(\)](#) returns status of BEE peripheral. The function [BEE\\_ClearStatusFlags\(\)](#) clears the BEE status flags.

### 11.5.1 BEE example

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/bee

## Data Structures

- struct [bee\\_region\\_config\\_t](#)  
*BEE region configuration structure. [More...](#)*

## Enumerations

- enum [bee\\_aes\\_mode\\_t](#) {
   
   kBEE\_AesEcbMode = 0U,
   
   kBEE\_AesCtrMode = 1U }
   
*BEE aes mode.*
- enum [bee\\_region\\_t](#) {
   
   kBEE\_Region0 = 0U,
   
   kBEE\_Region1 = 1U }
   
*BEE region.*
- enum [bee\\_ac\\_prot\\_enable](#) {
   
   kBEE\_AccessProtDisabled = 0U,
   
   kBEE\_AccessProtEnabled = 1U }
   
*BEE ac prot enable.*
- enum [bee\\_endian\\_swap\\_enable](#) {
   
   kBEE\_EndianSwapDisabled = 1U,
   
   kBEE\_EndianSwapEnabled = 0U }
   
*BEE endian swap enable.*
- enum [bee\\_security\\_level](#) {
   
   kBEE\_SecurityLevel0 = 0U,
   
   kBEE\_SecurityLevel1 = 1U,
   
   kBEE\_SecurityLevel2 = 2U,
   
   kBEE\_SecurityLevel3 = 3U }
   
*BEE security level.*

- enum `bee_status_flags_t` {
   
    `kBEE_DisableAbortFlag` = 1U,
   
    `kBEE_Reg0ReadSecViolation` = 2U,
   
    `kBEE_ReadIllegalAccess` = 4U,
   
    `kBEE_Reg1ReadSecViolation` = 8U,
   
    `kBEE_Reg0AccessViolation` = 16U,
   
    `kBEE_Reg1AccessViolation` = 32U,
   
    `kBEE_IdleFlag` = `BEE_STATUS_BEE_IDLE_MASK` }
- BEE status flags.*

## Functions

- void `BEE_Init` (`BEE_Type` \*base)
   
*Resets BEE module to factory default values.*
- void `BEE_Deinit` (`BEE_Type` \*base)
   
*Resets BEE module, clears keys for both regions and disables clock to the BEE.*
- static void `BEE_Enable` (`BEE_Type` \*base)
   
*Enables BEE decryption.*
- static void `BEE_Disable` (`BEE_Type` \*base)
   
*Disables BEE decryption.*
- void `BEE_GetDefaultConfig` (`bee_region_config_t` \*config)
   
*Loads default values to the BEE region configuration structure.*
- void `BEE_SetConfig` (`BEE_Type` \*base, const `bee_region_config_t` \*config)
   
*Sets BEE configuration.*
- `status_t BEE_SetRegionKey` (`BEE_Type` \*base, `bee_region_t` region, const `uint8_t` \*key, `size_t` keySize)
   
*Loads the AES key for selected region into BEE key registers.*
- `status_t BEE_SetRegionNonce` (`BEE_Type` \*base, `bee_region_t` region, const `uint8_t` \*nonce, `size_t` nonceSize)
   
*Loads the nonce for selected region into BEE nonce registers.*
- `uint32_t BEE_GetStatusFlags` (`BEE_Type` \*base)
   
*Gets the BEE status flags.*
- void `BEE_ClearStatusFlags` (`BEE_Type` \*base, `uint32_t` mask)
   
*Clears the BEE status flags.*

## Driver version

- #define `FSL_BEE_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 2)`)
   
*BEE driver version.*

## 11.6 Data Structure Documentation

### 11.6.1 struct `bee_region_config_t`

#### Data Fields

- `bee_aes_mode_t region0Mode`
  
*AES mode used for encryption/decryption for region 0.*

- **bee\_aes\_mode\_t region1Mode**  
*AES mode used for encryption/decryption for region 1.*
- **uint32\_t region0AddrOffset**  
*Region 0 address offset.*
- **uint32\_t region1AddrOffset**  
*Region 1 address offset.*
- **bee\_security\_level region0SecLevel**  
*Region 0 security level.*
- **bee\_security\_level region1SecLevel**  
*Region 1 security level.*
- **uint32\_t region1Bot**  
*Region 1 bottom address.*
- **uint32\_t region1Top**  
*Region 1 top address.*
- **bee\_ac\_prot\_enable accessPermission**  
*Access permission control enable/disable.*
- **bee\_endian\_swap\_enable endianSwapEn**  
*Endian swap enable/disable.*

## 11.7 Macro Definition Documentation

### 11.7.1 #define FSL\_BEE\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 2))

Version 2.0.2.

Current version: 2.0.2

Change log:

- 2.0.2
  - Bug Fixes
    - \* Fixed MISRA issue.
- 2.0.1
  - Bug Fixes
    - \* Fixed bug in key user key loading sequence. BEE must be enabled during loading of user key.
    - \* Fixed typos in comments.
  - New Features
    - \* Added configuration setting for endian swap, access permission and region security level.
  - Improvements
    - \* Setting of AES nonce was moved from [BEE\\_SetRegionKey\(\)](#) into separate [BEE\\_SetRegionNonce\(\)](#) function.
      - Changed handling of region settings. Both regions are configured simultaneously by [BEE\\_SetConfig\(\)](#) function. Configuration of FAC start and end address using IOM-UXC\_GPRs was moved to application.
    - \* Default value for region address offset was changed to 0.
- 2.0.0
  - Initial version

## 11.8 Enumeration Type Documentation

### 11.8.1 enum bee\_aes\_mode\_t

Enumerator

*kBEE\_AesEcbMode* AES ECB Mode.

*kBEE\_AesCtrMode* AES CTR Mode.

### 11.8.2 enum bee\_region\_t

Enumerator

*kBEE\_Region0* BEE region 0.

*kBEE\_Region1* BEE region 1.

### 11.8.3 enum bee\_ac\_prot\_enable

Enumerator

*kBEE\_AccessProtDisabled* BEE access permission control disabled.

*kBEE\_AccessProtEnabled* BEE access permission control enabled.

### 11.8.4 enum bee\_endian\_swap\_enable

Enumerator

*kBEE\_EndianSwapDisabled* BEE endian swap disabled.

*kBEE\_EndianSwapEnabled* BEE endian swap enabled.

### 11.8.5 enum bee\_security\_level

Enumerator

*kBEE\_SecurityLevel0* BEE security level 0.

*kBEE\_SecurityLevel1* BEE security level 1.

*kBEE\_SecurityLevel2* BEE security level 2.

*kBEE\_SecurityLevel3* BEE security level 3.

## 11.8.6 enum bee\_status\_flags\_t

Enumerator

- kBEE\_DisableAbortFlag* Disable abort flag.
- kBEE\_Reg0ReadSecViolation* Region-0 read channel security violation.
- kBEE\_ReadIllegalAccess* Read channel illegal access detected.
- kBEE\_Reg1ReadSecViolation* Region-1 read channel security violation.
- kBEE\_Reg0AccessViolation* Protected region-0 access violation.
- kBEE\_Reg1AccessViolation* Protected region-1 access violation.
- kBEE\_IdleFlag* Idle flag.

## 11.9 Function Documentation

### 11.9.1 void BEE\_Init ( BEE\_Type \* *base* )

This function performs hardware reset of BEE module. Attributes and keys from software for both regions are cleared.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | BEE peripheral address. |
|-------------|-------------------------|

### 11.9.2 void BEE\_Deinit ( BEE\_Type \* *base* )

This function performs hardware reset of BEE module and disables clocks. Attributes and keys from software for both regions are cleared.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | BEE peripheral address. |
|-------------|-------------------------|

### 11.9.3 static void BEE\_Enable ( BEE\_Type \* *base* ) [inline], [static]

This function enables decryption using BEE.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | BEE peripheral address. |
|-------------|-------------------------|

**11.9.4 static void BEE\_Disable ( BEE\_Type \* *base* ) [inline], [static]**

This function disables decryption using BEE.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | BEE peripheral address. |
|-------------|-------------------------|

**11.9.5 void BEE\_GetDefaultConfig ( bee\_region\_config\_t \* *config* )**

Loads default values to the BEE region configuration structure. The default values are as follows:

```
* config->region0Mode = kBEE_AesCtrMode;
* config->region1Mode = kBEE_AesCtrMode;
* config->region0AddrOffset = 0U;
* config->region1AddrOffset = 0U;
* config->region0SecLevel = kBEE_SecurityLevel3;
* config->region1SecLevel = kBEE_SecurityLevel3;
* config->region1Bot = 0U;
* config->region1Top = 0U;
* config->accessPermission = kBEE_AccessProtDisabled;
* config->endianSwapEn = kBEE_EndianSwapEnabled;
```

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Configuration structure for BEE peripheral. |
|---------------|---------------------------------------------|

**11.9.6 void BEE\_SetConfig ( BEE\_Type \* *base*, const bee\_region\_config\_t \* *config* )**

This function sets BEE peripheral and BEE region settings according to given configuration structure.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | BEE peripheral address. |
|-------------|-------------------------|

|               |                                  |
|---------------|----------------------------------|
| <i>config</i> | Configuration structure for BEE. |
|---------------|----------------------------------|

### 11.9.7 status\_t BEE\_SetRegionKey ( **BEE\_Type** \* *base*, **bee\_region\_t** *region*, const **uint8\_t** \* *key*, **size\_t** *keySize* )

This function loads given AES key to BEE register for the given region. The key must be 32-bit aligned and stored in little-endian format.

Please note, that eFuse BEE\_KEYx\_SEL must be set accordingly to be able to load and use key loaded in BEE registers. Otherwise, key cannot be loaded and BEE will use key from OTPMK or SW\_GP2.

Parameters

|                |                                               |
|----------------|-----------------------------------------------|
| <i>base</i>    | BEE peripheral address.                       |
| <i>region</i>  | Selection of the BEE region to be configured. |
| <i>key</i>     | AES key (in little-endian format).            |
| <i>keySize</i> | Size of AES key.                              |

### 11.9.8 status\_t BEE\_SetRegionNonce ( **BEE\_Type** \* *base*, **bee\_region\_t** *region*, const **uint8\_t** \* *nonce*, **size\_t** *nonceSize* )

This function loads given nonce(only AES CTR mode) to BEE register for the given region. The nonce must be 32-bit aligned and stored in little-endian format.

Parameters

|                  |                                               |
|------------------|-----------------------------------------------|
| <i>base</i>      | BEE peripheral address.                       |
| <i>region</i>    | Selection of the BEE region to be configured. |
| <i>nonce</i>     | AES nonce (in little-endian format).          |
| <i>nonceSize</i> | Size of AES nonce.                            |

### 11.9.9 uint32\_t BEE\_GetStatusFlags ( **BEE\_Type** \* *base* )

This function returns status of BEE peripheral.

## Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | BEE peripheral address. |
|-------------|-------------------------|

## Returns

The status flags. This is the logical OR of members of the enumeration [bee\\_status\\_flags\\_t](#)

**11.9.10 void BEE\_ClearStatusFlags ( BEE\_Type \* *base*, uint32\_t *mask* )**

## Parameters

|             |                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | BEE peripheral base address.                                                                                     |
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">bee_status_flags_t</a> |

# **Chapter 12**

## **CACHE: ARMV7-M7 CACHE Memory Controller**

### **12.1 Overview**

The MCUXpresso SDK provides a peripheral driver for the CACHE Controller of MCUXpresso SDK devices.

The CACHE driver is created to help the user more easily operate the cache memory. The APIs for basic operations are including the following three levels:

1L. The L1 cache driver API. This level provides the level 1 caches controller drivers. The L1 caches are mainly integrated in the Core memory system, Cortex-M7 L1 caches, etc. For our Cortex-M4 series platforms, the L1 cache is the local memory controller (LMEM) which is not integrated in the Cortex-M4 processor memory system.

2L. The L2 cache driver API. This level provides the level 2 cache controller drivers. The L2 cache could be integrated in the CORE memory system or an external L2 cache memory, PL310, etc.

3L. The combined cache driver API. This level provides many APIs for combined L1 and L2 cache maintain operations. This is provided for MCUXpresso SDK drivers (DMA, ENET, USDHC, etc) which should do the cache maintenance in their transactional APIs.

### **12.2 Function groups**

#### **12.2.1 L1 CACHE Operation**

The L1 CACHE has both code cache and data cache. This function group provides independent two groups API for both code cache and data cache. There are Enable/Disable APIs for code cache and data cache control and cache maintenance operations as Invalidate/Clean/CleanInvalidate by all and by address range.

#### **12.2.2 L2 CACHE Operation**

The L2 CACHE does not divide the cache to data and code. Instead, this function group provides one group cache maintenance operations as Enable/Disable/Invalidate/Clean/CleanInvalidate by all and by address range. Except the maintenance operation APIs, the L2 CACHE has its initialization/configure API. The user can use the default configure parameter by calling L2CACHE\_GetDefaultConfig() or changing the parameters as they wish. Then, call L2CACHE\_Init to do the L2 CACHE initialization. After initialization, the L2 cache can then be enabled.

Note: For the core external l2 Cache, the SoC usually has the control bit to select the SRAM to use as L2 Cache or normal SRAM. Make sure this selection is right when you use the L2 CACHE feature.

## Driver version

- #define **FSL\_CACHE\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 0, 4))  
*cache driver version 2.0.4.*

## Control for cortex-m7 L1 cache

- static void **L1CACHE\_EnableICache** (void)  
*Enables cortex-m7 L1 instruction cache.*
- static void **L1CACHE\_DisableICache** (void)  
*Disables cortex-m7 L1 instruction cache.*
- static void **L1CACHE\_InvalidateICache** (void)  
*Invalidate cortex-m7 L1 instruction cache.*
- void **L1CACHE\_InvalidateICacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidate cortex-m7 L1 instruction cache by range.*
- static void **L1CACHE\_EnableDCache** (void)  
*Enables cortex-m7 L1 data cache.*
- static void **L1CACHE\_DisableDCache** (void)  
*Disables cortex-m7 L1 data cache.*
- static void **L1CACHE\_InvalidateDCache** (void)  
*Invalidates cortex-m7 L1 data cache.*
- static void **L1CACHE\_CleanDCache** (void)  
*Cleans cortex-m7 L1 data cache.*
- static void **L1CACHE\_CleanInvalidateDCache** (void)  
*Cleans and Invalidates cortex-m7 L1 data cache.*
- static void **L1CACHE\_InvalidateDCacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidates cortex-m7 L1 data cache by range.*
- static void **L1CACHE\_CleanDCacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans cortex-m7 L1 data cache by range.*
- static void **L1CACHE\_CleanInvalidateDCacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans and Invalidates cortex-m7 L1 data cache by range.*

## Unified Cache Control for all caches (cortex-m7 L1 cache + I2 pI310)

Mainly used for many drivers for easy cache operation.

- void **ICACHE\_InvalidateByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidates all instruction caches by range.*
- void **DCACHE\_InvalidateByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidates all data caches by range.*
- void **DCACHE\_CleanByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans all data caches by range.*
- void **DCACHE\_CleanInvalidateByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans and Invalidates all data caches by range.*

## 12.3 Macro Definition Documentation

### 12.3.1 #define FSL\_CACHE\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 4))

## 12.4 Function Documentation

12.4.1 **void L1CACHE\_InvalidateCacheByRange ( *uint32\_t address*, *uint32\_t size\_byte* )**

## Parameters

|                  |                                                    |
|------------------|----------------------------------------------------|
| <i>address</i>   | The start address of the memory to be invalidated. |
| <i>size_byte</i> | The memory size.                                   |

## Note

The start address and size\_byte should be 32-byte(FSL\_FEATURE\_L1ICACHE\_LINESIZE\_BYT-E) aligned. The startAddr here will be forced to align to L1 I-cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 12.4.2 static void L1CACHE\_InvalidateDCacheByRange ( **uint32\_t address,** **uint32\_t size\_byte** ) [inline], [static]

## Parameters

|                  |                                                    |
|------------------|----------------------------------------------------|
| <i>address</i>   | The start address of the memory to be invalidated. |
| <i>size_byte</i> | The memory size.                                   |

## Note

The start address and size\_byte should be 32-byte(FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE) aligned. The startAddr here will be forced to align to L1 D-cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 12.4.3 static void L1CACHE\_CleanDCacheByRange ( **uint32\_t address,** **uint32\_t** **size\_byte** ) [inline], [static]

## Parameters

|                  |                                                |
|------------------|------------------------------------------------|
| <i>address</i>   | The start address of the memory to be cleaned. |
| <i>size_byte</i> | The memory size.                               |

## Note

The start address and size\_byte should be 32-byte(FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE) aligned. The startAddr here will be forced to align to L1 D-cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

12.4.4 **static void L1CACHE\_CleanInvalidateDCacheByRange ( uint32\_t *address*,  
                  uint32\_t *size\_byte* ) [inline], [static]**

Parameters

|                  |                                                              |
|------------------|--------------------------------------------------------------|
| <i>address</i>   | The start address of the memory to be clean and invalidated. |
| <i>size_byte</i> | The memory size.                                             |

Note

The start address and size\_byte should be 32-byte(FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE) aligned. The startAddr here will be forced to align to L1 D-cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 12.4.5 void ICACHE\_InvalidateByRange ( uint32\_t *address*, uint32\_t *size\_byte* )

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

Parameters

|                  |                                       |
|------------------|---------------------------------------|
| <i>address</i>   | The physical address.                 |
| <i>size_byte</i> | size of the memory to be invalidated. |

Note

address and size should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 12.4.6 void DCACHE\_InvalidateByRange ( uint32\_t *address*, uint32\_t *size\_byte* )

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

Parameters

|                |                       |
|----------------|-----------------------|
| <i>address</i> | The physical address. |
|----------------|-----------------------|

|                  |                                       |
|------------------|---------------------------------------|
| <i>size_byte</i> | size of the memory to be invalidated. |
|------------------|---------------------------------------|

## Note

address and size should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

**12.4.7 void DCACHE\_CleanByRange ( uint32\_t address, uint32\_t size\_byte )**

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

## Parameters

|                  |                                   |
|------------------|-----------------------------------|
| <i>address</i>   | The physical address.             |
| <i>size_byte</i> | size of the memory to be cleaned. |

## Note

address and size should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

**12.4.8 void DCACHE\_CleanInvalidateByRange ( uint32\_t address, uint32\_t size\_byte )**

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

## Parameters

|                  |                                                   |
|------------------|---------------------------------------------------|
| <i>address</i>   | The physical address.                             |
| <i>size_byte</i> | size of the memory to be cleaned and invalidated. |

## Note

address and size should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

# Chapter 13

## CMP: Analog Comparator Driver

### 13.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Analog Comparator (CMP) module of MCUXpresso SDK devices.

The CMP driver is a basic comparator with advanced features. The APIs for the basic comparator enable the CMP to compare the two voltages of the two input channels and create the output of the comparator result. The APIs for advanced features can be used as the plug-in functions based on the basic comparator. They can process the comparator's output with hardware support.

### 13.2 Typical use case

#### 13.2.1 Polling Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/cmp

#### 13.2.2 Interrupt Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/cmp

## Data Structures

- struct `cmp_config_t`  
*Configures the comparator. [More...](#)*
- struct `cmp_filter_config_t`  
*Configures the filter. [More...](#)*
- struct `cmp_dac_config_t`  
*Configures the internal DAC. [More...](#)*

## Enumerations

- enum `_cmp_interrupt_enable` {  
  `kCMP_OutputRisingInterruptEnable` = `CMP_SCR_IER_MASK`,  
  `kCMP_OutputFallingInterruptEnable` = `CMP_SCR_IEF_MASK` }  
*Interrupt enable/disable mask.*
- enum `_cmp_status_flags` {  
  `kCMP_OutputRisingEventFlag` = `CMP_SCR_CFR_MASK`,  
  `kCMP_OutputFallingEventFlag` = `CMP_SCR_CFF_MASK`,  
  `kCMP_OutputAssertEventFlag` = `CMP_SCR_COUT_MASK` }  
*Status flags' mask.*

- enum `cmp_hysteresis_mode_t` {
   
    `kCMP_HysteresisLevel0` = 0U,  
`kCMP_HysteresisLevel1` = 1U,  
`kCMP_HysteresisLevel2` = 2U,  
`kCMP_HysteresisLevel3` = 3U }
   
*CMP Hysteresis mode.*
- enum `cmp_reference_voltage_source_t` {
   
    `kCMP_VrefSourceVin1` = 0U,  
`kCMP_VrefSourceVin2` = 1U }
   
*CMP Voltage Reference source.*

## Driver version

- #define `FSL_CMP_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 3)`)
   
*CMP driver version 2.0.3.*

## Initialization

- void `CMP_Init` (`CMP_Type` \*base, const `cmp_config_t` \*config)
   
*Initializes the CMP.*
- void `CMP_Deinit` (`CMP_Type` \*base)
   
*De-initializes the CMP module.*
- static void `CMP_Enable` (`CMP_Type` \*base, bool enable)
   
*Enables/disables the CMP module.*
- void `CMP_GetDefaultConfig` (`cmp_config_t` \*config)
   
*Initializes the CMP user configuration structure.*
- void `CMP_SetInputChannels` (`CMP_Type` \*base, `uint8_t` positiveChannel, `uint8_t` negativeChannel)
   
*Sets the input channels for the comparator.*

## Advanced Features

- void `CMP_EnableDMA` (`CMP_Type` \*base, bool enable)
   
*Enables/disables the DMA request for rising/falling events.*
- static void `CMP_EnableWindowMode` (`CMP_Type` \*base, bool enable)
   
*Enables/disables the window mode.*
- void `CMP_SetFilterConfig` (`CMP_Type` \*base, const `cmp_filter_config_t` \*config)
   
*Configures the filter.*
- void `CMP_SetDACConfig` (`CMP_Type` \*base, const `cmp_dac_config_t` \*config)
   
*Configures the internal DAC.*
- void `CMP_EnableInterrupts` (`CMP_Type` \*base, `uint32_t` mask)
   
*Enables the interrupts.*
- void `CMP_DisableInterrupts` (`CMP_Type` \*base, `uint32_t` mask)
   
*Disables the interrupts.*

## Results

- `uint32_t CMP_GetStatusFlags` (`CMP_Type` \*base)
   
*Gets the status flags.*
- void `CMP_ClearStatusFlags` (`CMP_Type` \*base, `uint32_t` mask)
   
*Clears the status flags.*

## 13.3 Data Structure Documentation

### 13.3.1 struct cmp\_config\_t

#### Data Fields

- bool `enableCmp`  
*Enable the CMP module.*
- `cmp_hysteresis_mode_t hysteresisMode`  
*CMP Hysteresis mode.*
- bool `enableHighSpeed`  
*Enable High-speed (HS) comparison mode.*
- bool `enableInvertOutput`  
*Enable the inverted comparator output.*
- bool `useUnfilteredOutput`  
*Set the compare output(COUT) to equal COUTA(true) or COUT(false).*
- bool `enablePinOut`  
*The comparator output is available on the associated pin.*

#### Field Documentation

- (1) `bool cmp_config_t::enableCmp`
- (2) `cmp_hysteresis_mode_t cmp_config_t::hysteresisMode`
- (3) `bool cmp_config_t::enableHighSpeed`
- (4) `bool cmp_config_t::enableInvertOutput`
- (5) `bool cmp_config_t::useUnfilteredOutput`
- (6) `bool cmp_config_t::enablePinOut`

### 13.3.2 struct cmp\_filter\_config\_t

#### Data Fields

- bool `enableSample`  
*Using the external SAMPLE as a sampling clock input or using a divided bus clock.*
- `uint8_t filterCount`  
*Filter Sample Count.*
- `uint8_t filterPeriod`  
*Filter Sample Period.*

**Field Documentation**(1) `bool cmp_filter_config_t::enableSample`(2) `uint8_t cmp_filter_config_t::filterCount`

Available range is 1-7; 0 disables the filter.

(3) `uint8_t cmp_filter_config_t::filterPeriod`

The divider to the bus clock. Available range is 0-255.

**13.3.3 struct cmp\_dac\_config\_t****Data Fields**

- `cmp_reference_voltage_source_t referenceVoltageSource`  
*Supply voltage reference source.*
- `uint8_t DACValue`  
*Value for the DAC Output Voltage.*

**Field Documentation**(1) `cmp_reference_voltage_source_t cmp_dac_config_t::referenceVoltageSource`(2) `uint8_t cmp_dac_config_t::DACValue`

Available range is 0-63.

**13.4 Macro Definition Documentation****13.4.1 #define FSL\_CMP\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 3))****13.5 Enumeration Type Documentation****13.5.1 enum \_cmp\_interrupt\_enable**

Enumerator

`kCMP_OutputRisingInterruptEnable` Comparator interrupt enable rising.`kCMP_OutputFallingInterruptEnable` Comparator interrupt enable falling.**13.5.2 enum \_cmp\_status\_flags**

Enumerator

`kCMP_OutputRisingEventFlag` Rising-edge on the comparison output has occurred.

***kCMP\_OutputFallingEventFlag*** Falling-edge on the comparison output has occurred.

***kCMP\_OutputAssertEventFlag*** Return the current value of the analog comparator output.

### 13.5.3 enum cmp\_hysteresis\_mode\_t

Enumerator

***kCMP\_HysteresisLevel0*** Hysteresis level 0.

***kCMP\_HysteresisLevel1*** Hysteresis level 1.

***kCMP\_HysteresisLevel2*** Hysteresis level 2.

***kCMP\_HysteresisLevel3*** Hysteresis level 3.

### 13.5.4 enum cmp\_reference\_voltage\_source\_t

Enumerator

***kCMP\_VrefSourceVin1*** Vin1 is selected as a resistor ladder network supply reference Vin.

***kCMP\_VrefSourceVin2*** Vin2 is selected as a resistor ladder network supply reference Vin.

## 13.6 Function Documentation

### 13.6.1 void CMP\_Init ( **CMP\_Type** \* *base*, **const cmp\_config\_t** \* *config* )

This function initializes the CMP module. The operations included are as follows.

- Enabling the clock for CMP module.
- Configuring the comparator.
- Enabling the CMP module. Note that for some devices, multiple CMP instances share the same clock gate. In this case, to enable the clock for any instance enables all CMPs. See the appropriate MCU reference manual for the clock assignment of the CMP.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | CMP peripheral base address.            |
| <i>config</i> | Pointer to the configuration structure. |

### 13.6.2 void CMP\_Deinit ( **CMP\_Type** \* *base* )

This function de-initializes the CMP module. The operations included are as follows.

- Disabling the CMP module.
- Disabling the clock for CMP module.

This function disables the clock for the CMP. Note that for some devices, multiple CMP instances share the same clock gate. In this case, before disabling the clock for the CMP, ensure that all the CMP instances are not used.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | CMP peripheral base address. |
|-------------|------------------------------|

### 13.6.3 static void CMP\_Enable ( **CMP\_Type** \* *base*, **bool** *enable* ) [inline], [static]

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | CMP peripheral base address.    |
| <i>enable</i> | Enables or disables the module. |

### 13.6.4 void CMP\_GetDefaultConfig ( **cmp\_config\_t** \* *config* )

This function initializes the user configuration structure to these default values.

```
* config->enableCmp          = true;
* config->hysteresisMode     = kCMP_HysteresisLevel0;
* config->enableHighSpeed    = false;
* config->enableInvertOutput = false;
* config->useUnfilteredOutput= false;
* config->enablePinOut       = false;
* config->enableTriggerMode  = false;
*
```

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

### 13.6.5 void CMP\_SetInputChannels ( **CMP\_Type** \* *base*, **uint8\_t** *positiveChannel*, **uint8\_t** *negativeChannel* )

This function sets the input channels for the comparator. Note that two input channels cannot be set the same way in the application. When the user selects the same input from the analog mux to the positive and negative port, the comparator is disabled automatically.

Parameters

|                         |                                                             |
|-------------------------|-------------------------------------------------------------|
| <i>base</i>             | CMP peripheral base address.                                |
| <i>positive-Channel</i> | Positive side input channel number. Available range is 0-7. |
| <i>negative-Channel</i> | Negative side input channel number. Available range is 0-7. |

### 13.6.6 void CMP\_EnableDMA ( **CMP\_Type** \* *base*, **bool** *enable* )

This function enables/disables the DMA request for rising/falling events. Either event triggers the generation of the DMA request from CMP if the DMA feature is enabled. Both events are ignored for generating the DMA request from the CMP if the DMA is disabled.

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | CMP peripheral base address.     |
| <i>enable</i> | Enables or disables the feature. |

### 13.6.7 static void CMP\_EnableWindowMode ( **CMP\_Type** \* *base*, **bool** *enable* ) [**inline**], [**static**]

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | CMP peripheral base address.     |
| <i>enable</i> | Enables or disables the feature. |

### 13.6.8 void CMP\_SetFilterConfig ( **CMP\_Type** \* *base*, **const cmp\_filter\_config\_t** \* *config* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | CMP peripheral base address. |
|-------------|------------------------------|

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

### 13.6.9 void CMP\_SetDACConfig ( **CMP\_Type** \* *base*, **const cmp\_dac\_config\_t** \* *config* )

Parameters

|               |                                                                      |
|---------------|----------------------------------------------------------------------|
| <i>base</i>   | CMP peripheral base address.                                         |
| <i>config</i> | Pointer to the configuration structure. "NULL" disables the feature. |

### 13.6.10 void CMP\_EnableInterrupts ( **CMP\_Type** \* *base*, **uint32\_t** *mask* )

Parameters

|             |                                                         |
|-------------|---------------------------------------------------------|
| <i>base</i> | CMP peripheral base address.                            |
| <i>mask</i> | Mask value for interrupts. See "_cmp_interrupt_enable". |

### 13.6.11 void CMP\_DisableInterrupts ( **CMP\_Type** \* *base*, **uint32\_t** *mask* )

Parameters

|             |                                                         |
|-------------|---------------------------------------------------------|
| <i>base</i> | CMP peripheral base address.                            |
| <i>mask</i> | Mask value for interrupts. See "_cmp_interrupt_enable". |

### 13.6.12 **uint32\_t** CMP\_GetStatusFlags ( **CMP\_Type** \* *base* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | CMP peripheral base address. |
|-------------|------------------------------|

Returns

Mask value for the asserted flags. See "\_cmp\_status\_flags".

13.6.13 void CMP\_ClearStatusFlags ( **CMP\_Type** \* *base*, **uint32\_t** *mask* )

## Parameters

|             |                                                    |
|-------------|----------------------------------------------------|
| <i>base</i> | CMP peripheral base address.                       |
| <i>mask</i> | Mask value for the flags. See "_cmp_status_flags". |

# Chapter 14

## Common Driver

### 14.1 Overview

The MCUXpresso SDK provides a driver for the common module of MCUXpresso SDK devices.

#### Macros

- `#define FSL_DRIVER_TRANSFER_DOUBLE_WEAK_IRQ 1`  
*Macro to use the default weak IRQ handler in drivers.*
- `#define MAKE_STATUS(group, code) (((group)*100L) + (code)))`  
*Construct a status code value from a group and code number.*
- `#define MAKE_VERSION(major, minor, bugfix) (((major)*65536L) + ((minor)*256L) + (bugfix))`  
*Construct the version number for drivers.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_NONE 0U`  
*No debug console.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_UART 1U`  
*Debug console based on UART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_LPUART 2U`  
*Debug console based on LPUART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_LPSCI 3U`  
*Debug console based on LPSCI.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_USBCDC 4U`  
*Debug console based on USBCDC.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM 5U`  
*Debug console based on FLEXCOMM.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_IUART 6U`  
*Debug console based on i.MX UART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_VUSART 7U`  
*Debug console based on LPC\_VUSART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART 8U`  
*Debug console based on LPC\_USART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_SWO 9U`  
*Debug console based on SWO.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_QSCI 10U`  
*Debug console based on QSCI.*
- `#define ARRAY_SIZE(x) (sizeof(x) / sizeof((x)[0]))`  
*Computes the number of elements in an array.*

#### Typedefs

- `typedef int32_t status_t`  
*Type used for all status and error return values.*

## Enumerations

- enum `_status_groups` {  
    `kStatusGroup_Generic` = 0,  
    `kStatusGroup_FLASH` = 1,  
    `kStatusGroup_LP SPI` = 4,  
    `kStatusGroup_FLEXIO_SPI` = 5,  
    `kStatusGroup_DSPI` = 6,  
    `kStatusGroup_FLEXIO_UART` = 7,  
    `kStatusGroup_FLEXIO_I2C` = 8,  
    `kStatusGroup_LPI2C` = 9,  
    `kStatusGroup_UART` = 10,  
    `kStatusGroup_I2C` = 11,  
    `kStatusGroup_LPSCI` = 12,  
    `kStatusGroup_LPUART` = 13,  
    `kStatusGroup_SPI` = 14,  
    `kStatusGroup_XRDC` = 15,  
    `kStatusGroup_SEMA42` = 16,  
    `kStatusGroup_SDHC` = 17,  
    `kStatusGroup_SDMMC` = 18,  
    `kStatusGroup_SAI` = 19,  
    `kStatusGroup_MCG` = 20,  
    `kStatusGroup_SCG` = 21,  
    `kStatusGroup_SD SPI` = 22,  
    `kStatusGroup_FLEXIO_I2S` = 23,  
    `kStatusGroup_FLEXIO_MCULCD` = 24,  
    `kStatusGroup_FLASHIAP` = 25,  
    `kStatusGroup_FLEXCOMM_I2C` = 26,  
    `kStatusGroup_I2S` = 27,  
    `kStatusGroup_IUART` = 28,  
    `kStatusGroup_CSI` = 29,  
    `kStatusGroup_MIPI_DSI` = 30,  
    `kStatusGroup_SDRAMC` = 35,  
    `kStatusGroup_POWER` = 39,  
    `kStatusGroup_ENET` = 40,  
    `kStatusGroup_PHY` = 41,  
    `kStatusGroup_TRGMUX` = 42,  
    `kStatusGroup_SMARTCARD` = 43,  
    `kStatusGroup_LMEM` = 44,  
    `kStatusGroup_QSPI` = 45,  
    `kStatusGroup_DMA` = 50,  
    `kStatusGroup_EDMA` = 51,  
    `kStatusGroup_DMAMGR` = 52,  
    `kStatusGroup_FLEXCAN` = 53,  
    `kStatusGroup_LTC` = 54,  
    `kStatusGroup_FLEXIO_CAMERA` = 55,  
    `kStatusGroup_LPC_SPI` = 56,  
    `kStatusGroup_EPC_USAR` = 57,  
    `kStatusGroup_DMIC` = 58,  
    `kStatusGroup_SDIF` = 59,  
}

```

kStatusGroup_NETC = 166 }

Status group numbers.
• enum {
    kStatus_Success = MAKE_STATUS(kStatusGroup_Generic, 0),
    kStatus_Fail = MAKE_STATUS(kStatusGroup_Generic, 1),
    kStatus_ReadOnly = MAKE_STATUS(kStatusGroup_Generic, 2),
    kStatus_OutOfRange = MAKE_STATUS(kStatusGroup_Generic, 3),
    kStatus_InvalidArgument = MAKE_STATUS(kStatusGroup_Generic, 4),
    kStatus_Timeout = MAKE_STATUS(kStatusGroup_Generic, 5),
    kStatus_NoTransferInProgress,
    kStatus_Busy = MAKE_STATUS(kStatusGroup_Generic, 7),
    kStatus_NoData }
Generic status return codes.

```

## Functions

- void \* **SDK\_Malloc** (size\_t size, size\_t alignbytes)  
*Allocate memory with given alignment and aligned size.*
- void **SDK\_Free** (void \*ptr)  
*Free memory.*
- void **SDK\_DelayAtLeastUs** (uint32\_t delayTime\_us, uint32\_t coreClock\_Hz)  
*Delay at least for some time.*
- static **status\_t EnableIRQ** (IRQn\_Type interrupt)  
*Enable specific interrupt.*
- static **status\_t DisableIRQ** (IRQn\_Type interrupt)  
*Disable specific interrupt.*
- static **status\_t EnableIRQWithPriority** (IRQn\_Type interrupt, uint8\_t priNum)  
*Enable the IRQ, and also set the interrupt priority.*
- static **status\_t IRQ\_SetPriority** (IRQn\_Type interrupt, uint8\_t priNum)  
*Set the IRQ priority.*
- static **status\_t IRQ\_ClearPendingIRQ** (IRQn\_Type interrupt)  
*Clear the pending IRQ flag.*
- static uint32\_t **DisableGlobalIRQ** (void)  
*Disable the global IRQ.*
- static void **EnableGlobalIRQ** (uint32\_t primask)  
*Enable the global IRQ.*

## Driver version

- #define **FSL\_COMMON\_DRIVER\_VERSION** (MAKE\_VERSION(2, 4, 0))  
*common driver version.*

## Min/max macros

- #define **MIN**(a, b) (((a) < (b)) ? (a) : (b))
- #define **MAX**(a, b) (((a) > (b)) ? (a) : (b))

## UINT16\_MAX/UINT32\_MAX value

- #define **UINT16\_MAX** ((uint16\_t)-1)

- #define **UINT32\_MAX** ((uint32\_t)-1)

## Suppress fallthrough warning macro

- #define **SUPPRESS\_FALL\_THROUGH\_WARNING()**

## Atomic modification

These macros are used for atomic access, such as read-modify-write to the peripheral registers.

- **SDK\_ATOMIC\_LOCAL\_ADD**
- **SDK\_ATOMIC\_LOCAL\_SET**
- **SDK\_ATOMIC\_LOCAL\_CLEAR**
- **SDK\_ATOMIC\_LOCAL\_TOGGLE**
- **SDK\_ATOMIC\_LOCAL\_CLEAR\_AND\_SET**

Take **SDK\_ATOMIC\_LOCAL\_CLEAR\_AND\_SET** as an example: the parameter `addr` means the address of the peripheral register or variable you want to modify atomically, the parameter `clearBits` is the bits to clear, the parameter `setBits` is the bits to set. For example, to set a 32-bit register bit1:bit0 to 0b10, use like this:

```
volatile uint32_t * reg = (volatile uint32_t *)REG_ADDR;
SDK_ATOMIC_LOCAL_CLEAR_AND_SET(reg, 0x03, 0x02);
```

In this example, the register bit1:bit0 are cleared and bit1 is set, as a result, register bit1:bit0 = 0b10.

### Note

For the platforms don't support exclusive load and store, these macros disable the global interrupt to protect the modification.

These macros only guarantee the local processor atomic operations. For the multi-processor devices, use hardware semaphore such as SEMA42 to guarantee exclusive access if necessary.

- #define **SDK\_ATOMIC\_LOCAL\_ADD(addr, val)**
- #define **SDK\_ATOMIC\_LOCAL\_SUB(addr, val)**
- #define **SDK\_ATOMIC\_LOCAL\_SET(addr, bits)**
- #define **SDK\_ATOMIC\_LOCAL\_CLEAR(addr, bits)**
- #define **SDK\_ATOMIC\_LOCAL\_TOGGLE(addr, bits)**
- #define **SDK\_ATOMIC\_LOCAL\_CLEAR\_AND\_SET(addr, clearBits, setBits)**

## Timer utilities

- #define **USEC\_TO\_COUNT(us, clockFreqInHz)** (uint64\_t)((uint64\_t)(us) \* (clockFreqInHz)) / 1000000U
 

*Macro to convert a microsecond period to raw count value.*
- #define **COUNT\_TO\_USEC(count, clockFreqInHz)** (uint64\_t)((uint64\_t)(count)\*1000000U / (clockFreqInHz))
 

*Macro to convert a raw count value to microsecond.*

- #define **MSEC\_TO\_COUNT**(ms, clockFreqInHz) (uint64\_t)((uint64\_t)(ms) \* (clockFreqInHz) / 1000U)
 

*Macro to convert a millisecond period to raw count value.*
- #define **COUNT\_TO\_MSEC**(count, clockFreqInHz) (uint64\_t)((uint64\_t)(count)\*1000U / (clockFreqInHz))
 

*Macro to convert a raw count value to millisecond.*

## Alignment variable definition macros

- #define **SDK\_L1DCACHE\_ALIGN**(var) SDK\_ALIGN(var, FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTEx)
 

*Macro to define a variable with L1 d-cache line size alignment.*
- #define **SDK\_SIZEALIGN**(var, alignbytes) ((unsigned int)((var) + ((alignbytes)-1U)) & (unsigned int)(~(unsigned int)((alignbytes)-1U)))
 

*Macro to define a variable with L2 cache line size alignment.*

## 14.2 Macro Definition Documentation

### 14.2.1 #define FSL\_DRIVER\_TRANSFER\_DOUBLE\_WEAK\_IRQ 1

### 14.2.2 #define MAKE\_STATUS( group, code ) (((group)\*100L) + (code))

### 14.2.3 #define MAKE\_VERSION( major, minor, bugfix ) (((major)\*65536L) + ((minor)\*256L) + (bugfix))

The driver version is a 32-bit number, for both 32-bit platforms(such as Cortex M) and 16-bit platforms(such as DSC).

|    |        |    |               |    |               |   |         |  |  |
|----|--------|----|---------------|----|---------------|---|---------|--|--|
|    | Unused |    | Major Version |    | Minor Version |   | Bug Fix |  |  |
| 31 | 25     | 24 | 17            | 16 | 9             | 8 | 0       |  |  |

- 14.2.4 `#define FSL_COMMON_DRIVER_VERSION (MAKE_VERSION(2, 4, 0))`
- 14.2.5 `#define DEBUG_CONSOLE_DEVICE_TYPE_NONE 0U`
- 14.2.6 `#define DEBUG_CONSOLE_DEVICE_TYPE_UART 1U`
- 14.2.7 `#define DEBUG_CONSOLE_DEVICE_TYPE_LPUART 2U`
- 14.2.8 `#define DEBUG_CONSOLE_DEVICE_TYPE_LPSCI 3U`
- 14.2.9 `#define DEBUG_CONSOLE_DEVICE_TYPE_USBCDC 4U`
- 14.2.10 `#define DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM 5U`
- 14.2.11 `#define DEBUG_CONSOLE_DEVICE_TYPE_IUART 6U`
- 14.2.12 `#define DEBUG_CONSOLE_DEVICE_TYPE_VUSART 7U`
- 14.2.13 `#define DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART 8U`
- 14.2.14 `#define DEBUG_CONSOLE_DEVICE_TYPE_SWO 9U`
- 14.2.15 `#define DEBUG_CONSOLE_DEVICE_TYPE_QSCI 10U`
- 14.2.16 `#define ARRAY_SIZE( x ) (sizeof(x) / sizeof((x)[0]))`
- 14.2.17 `#define SDK_SIZEALIGN( var, alignbytes ) ((unsigned int)((var) + ((alignbytes)-1U)) & (unsigned int)(~(unsigned int)((alignbytes)-1U)))`

Macro to change a value to a given size aligned value

## 14.3 Typedef Documentation

- 14.3.1 `typedef int32_t status_t`

## 14.4 Enumeration Type Documentation

### 14.4.1 enum \_status\_groups

Enumerator

- kStatusGroup\_Generic* Group number for generic status codes.
- kStatusGroup\_FLASH* Group number for FLASH status codes.
- kStatusGroup\_LP SPI* Group number for LP SPI status codes.
- kStatusGroup\_FLEXIO\_SPI* Group number for FLEXIO SPI status codes.
- kStatusGroup\_DSPI* Group number for DSPI status codes.
- kStatusGroup\_FLEXIO\_UART* Group number for FLEXIO UART status codes.
- kStatusGroup\_FLEXIO\_I2C* Group number for FLEXIO I2C status codes.
- kStatusGroup\_LPI2C* Group number for LPI2C status codes.
- kStatusGroup\_UART* Group number for UART status codes.
- kStatusGroup\_I2C* Group number for I2C status codes.
- kStatusGroup\_LPSCI* Group number for LPSCI status codes.
- kStatusGroup\_LPUART* Group number for LPUART status codes.
- kStatusGroup\_SPI* Group number for SPI status code.
- kStatusGroup\_XRDC* Group number for XRDC status code.
- kStatusGroup\_SEMA42* Group number for SEMA42 status code.
- kStatusGroup\_SDHC* Group number for SDHC status code.
- kStatusGroup\_SDMMC* Group number for SDMMC status code.
- kStatusGroup\_SAI* Group number for SAI status code.
- kStatusGroup\_MCG* Group number for MCG status codes.
- kStatusGroup\_SCG* Group number for SCG status codes.
- kStatusGroup\_SD SPI* Group number for SD SPI status codes.
- kStatusGroup\_FLEXIO\_I2S* Group number for FLEXIO I2S status codes.
- kStatusGroup\_FLEXIO\_MCU LCD* Group number for FLEXIO LCD status codes.
- kStatusGroup\_FLASHIAP* Group number for FLASHIAP status codes.
- kStatusGroup\_FLEXCOMM\_I2C* Group number for FLEXCOMM I2C status codes.
- kStatusGroup\_I2S* Group number for I2S status codes.
- kStatusGroup\_IUART* Group number for IUART status codes.
- kStatusGroup\_CSI* Group number for CSI status codes.
- kStatusGroup\_MIPI\_DSI* Group number for MIPI DSI status codes.
- kStatusGroup\_SDRAMC* Group number for SDRAMC status codes.
- kStatusGroup\_POWER* Group number for POWER status codes.
- kStatusGroup\_ENET* Group number for ENET status codes.
- kStatusGroup\_PHY* Group number for PHY status codes.
- kStatusGroup\_TRGMUX* Group number for TRGMUX status codes.
- kStatusGroup\_SMARTCARD* Group number for SMARTCARD status codes.
- kStatusGroup\_LMEM* Group number for LMEM status codes.
- kStatusGroup\_QSPI* Group number for QSPI status codes.
- kStatusGroup\_DMA* Group number for DMA status codes.
- kStatusGroup\_EDMA* Group number for EDMA status codes.
- kStatusGroup\_DMAMGR* Group number for DMAMGR status codes.

*kStatusGroup\_FLEXCAN* Group number for FlexCAN status codes.  
*kStatusGroup\_LTC* Group number for LTC status codes.  
*kStatusGroup\_FLEXIO\_CAMERA* Group number for FLEXIO CAMERA status codes.  
*kStatusGroup\_LPC\_SPI* Group number for LPC\_SPI status codes.  
*kStatusGroup\_LPC\_USART* Group number for LPC\_USART status codes.  
*kStatusGroup\_DMIC* Group number for DMIC status codes.  
*kStatusGroup\_SDIF* Group number for SDIF status codes.  
*kStatusGroup\_SPIFI* Group number for SPIFI status codes.  
*kStatusGroup OTP* Group number for OTP status codes.  
*kStatusGroup\_MCAN* Group number for MCAN status codes.  
*kStatusGroup\_CAAM* Group number for CAAM status codes.  
*kStatusGroup\_ECSPI* Group number for ECSPI status codes.  
*kStatusGroup\_USDHC* Group number for USDHC status codes.  
*kStatusGroup\_LPC\_I2C* Group number for LPC\_I2C status codes.  
*kStatusGroup\_DCP* Group number for DCP status codes.  
*kStatusGroup\_MSCAN* Group number for MSCAN status codes.  
*kStatusGroup\_ESAI* Group number for ESAI status codes.  
*kStatusGroup\_FLEXSPI* Group number for FLEXSPI status codes.  
*kStatusGroup\_MMDC* Group number for MMDC status codes.  
*kStatusGroup\_PDM* Group number for MIC status codes.  
*kStatusGroup\_SDMA* Group number for SDMA status codes.  
*kStatusGroup\_ICS* Group number for ICS status codes.  
*kStatusGroup\_SPDIF* Group number for SPDIF status codes.  
*kStatusGroup\_LPC\_MINISPI* Group number for LPC\_MINISPI status codes.  
*kStatusGroup\_HASHCRYPT* Group number for Hashcrypt status codes.  
*kStatusGroup\_LPC\_SPI\_SSP* Group number for LPC\_SPI\_SSP status codes.  
*kStatusGroup\_I3C* Group number for I3C status codes.  
*kStatusGroup\_LPC\_I2C\_1* Group number for LPC\_I2C\_1 status codes.  
*kStatusGroup\_NOTIFIER* Group number for NOTIFIER status codes.  
*kStatusGroup\_DebugConsole* Group number for debug console status codes.  
*kStatusGroup\_SEMC* Group number for SEMC status codes.  
*kStatusGroup\_ApplicationRangeStart* Starting number for application groups.  
*kStatusGroup\_IAP* Group number for IAP status codes.  
*kStatusGroup\_SFA* Group number for SFA status codes.  
*kStatusGroup\_SPC* Group number for SPC status codes.  
*kStatusGroup\_PUF* Group number for PUF status codes.  
*kStatusGroup\_TOUCH\_PANEL* Group number for touch panel status codes.  
*kStatusGroup\_VBAT* Group number for VBAT status codes.  
*kStatusGroup\_HAL\_GPIO* Group number for HAL GPIO status codes.  
*kStatusGroup\_HAL\_UART* Group number for HAL UART status codes.  
*kStatusGroup\_HAL\_TIMER* Group number for HAL TIMER status codes.  
*kStatusGroup\_HAL\_SPI* Group number for HAL SPI status codes.  
*kStatusGroup\_HAL\_I2C* Group number for HAL I2C status codes.  
*kStatusGroup\_HAL\_FLASH* Group number for HAL FLASH status codes.  
*kStatusGroup\_HAL\_PWM* Group number for HAL PWM status codes.

*kStatusGroup\_HAL\_RNG* Group number for HAL RNG status codes.  
*kStatusGroup\_HAL\_I2S* Group number for HAL I2S status codes.  
*kStatusGroup\_HAL\_ADC\_SENSOR* Group number for HAL ADC SENSOR status codes.  
*kStatusGroup\_TIMERMANAGER* Group number for TiMER MANAGER status codes.  
*kStatusGroup\_SERIALMANAGER* Group number for SERIAL MANAGER status codes.  
*kStatusGroup\_LED* Group number for LED status codes.  
*kStatusGroup\_BUTTON* Group number for BUTTON status codes.  
*kStatusGroup\_EXTERN\_EEPROM* Group number for EXTERN EEPROM status codes.  
*kStatusGroup\_SHELL* Group number for SHELL status codes.  
*kStatusGroup\_MEM\_MANAGER* Group number for MEM MANAGER status codes.  
*kStatusGroup\_LIST* Group number for List status codes.  
*kStatusGroup\_OSA* Group number for OSA status codes.  
*kStatusGroup\_COMMON\_TASK* Group number for Common task status codes.  
*kStatusGroup\_MSG* Group number for messaging status codes.  
*kStatusGroup\_SDK\_OCOTP* Group number for OCOTP status codes.  
*kStatusGroup\_SDK\_FLEXSPINOR* Group number for FLEXSPINOR status codes.  
*kStatusGroup\_CODEC* Group number for codec status codes.  
*kStatusGroup\_ASRC* Group number for codec status ASRC.  
*kStatusGroup\_OTFAD* Group number for codec status codes.  
*kStatusGroup\_SDIOSLV* Group number for SDIOSLV status codes.  
*kStatusGroup\_MECC* Group number for MECC status codes.  
*kStatusGroup\_ENET\_QOS* Group number for ENET\_QOS status codes.  
*kStatusGroup\_LOG* Group number for LOG status codes.  
*kStatusGroup\_I3CBUS* Group number for I3CBUS status codes.  
*kStatusGroup\_QSCI* Group number for QSCI status codes.  
*kStatusGroup\_SNT* Group number for SNT status codes.  
*kStatusGroup\_QUEUEDSPI* Group number for QSPI status codes.  
*kStatusGroup\_POWER\_MANAGER* Group number for POWER\_MANAGER status codes.  
*kStatusGroup\_IPED* Group number for IPED status codes.  
*kStatusGroup\_ELS\_PKC* Group number for ELS PKC status codes.  
*kStatusGroup\_CSS\_PKC* Group number for CSS PKC status codes.  
*kStatusGroup\_HOSTIF* Group number for HOSTIF status codes.  
*kStatusGroup\_CLIF* Group number for CLIF status codes.  
*kStatusGroup\_BMA* Group number for BMA status codes.  
*kStatusGroup\_NETC* Group number for NETC status codes.

#### 14.4.2 anonymous enum

Enumerator

*kStatus\_Success* Generic status for Success.  
*kStatus\_Fail* Generic status for Fail.  
*kStatus\_ReadOnly* Generic status for read only failure.  
*kStatus\_OutOfRange* Generic status for out of range access.

***kStatus\_InvalidArgument*** Generic status for invalid argument check.

***kStatus\_Timeout*** Generic status for timeout.

***kStatus\_NoTransferInProgress*** Generic status for no transfer in progress.

***kStatus\_Busy*** Generic status for module is busy.

***kStatus\_NoData*** Generic status for no data is found for the operation.

## 14.5 Function Documentation

### 14.5.1 void\* SDK\_Malloc ( size\_t *size*, size\_t *alignbytes* )

This is provided to support the dynamically allocated memory used in cache-able region.

Parameters

|                   |                                |
|-------------------|--------------------------------|
| <i>size</i>       | The length required to malloc. |
| <i>alignbytes</i> | The alignment size.            |

Return values

|            |                   |
|------------|-------------------|
| <i>The</i> | allocated memory. |
|------------|-------------------|

### 14.5.2 void SDK\_Free ( void \* *ptr* )

Parameters

|            |                           |
|------------|---------------------------|
| <i>ptr</i> | The memory to be release. |
|------------|---------------------------|

### 14.5.3 void SDK\_DelayAtLeastUs ( uint32\_t *delayTime\_us*, uint32\_t *coreClock\_Hz* )

Please note that, this API uses while loop for delay, different run-time environments make the time not precise, if precise delay count was needed, please implement a new delay function with hardware timer.

Parameters

|                     |                                    |
|---------------------|------------------------------------|
| <i>delayTime_us</i> | Delay time in unit of microsecond. |
|---------------------|------------------------------------|

|                     |                               |
|---------------------|-------------------------------|
| <i>coreClock_Hz</i> | Core clock frequency with Hz. |
|---------------------|-------------------------------|

#### 14.5.4 static status\_t EnableIRQ ( IRQn\_Type *interrupt* ) [inline], [static]

Enable LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only enables the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                 |
|------------------|-----------------|
| <i>interrupt</i> | The IRQ number. |
|------------------|-----------------|

Return values

|                        |                                |
|------------------------|--------------------------------|
| <i>kStatus_Success</i> | Interrupt enabled successfully |
| <i>kStatus_Fail</i>    | Failed to enable the interrupt |

#### 14.5.5 static status\_t DisableIRQ ( IRQn\_Type *interrupt* ) [inline], [static]

Disable LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only disables the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                 |
|------------------|-----------------|
| <i>interrupt</i> | The IRQ number. |
|------------------|-----------------|

Return values

|                        |                                 |
|------------------------|---------------------------------|
| <i>kStatus_Success</i> | Interrupt disabled successfully |
| <i>kStatus_Fail</i>    | Failed to disable the interrupt |

#### 14.5.6 static status\_t EnableIRQWithPriority( IRQn\_Type *interrupt*, uint8\_t *priNum* ) [inline], [static]

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1\_INT\_VECTORS.

Parameters

|                  |                                                       |
|------------------|-------------------------------------------------------|
| <i>interrupt</i> | The IRQ to Enable.                                    |
| <i>priNum</i>    | Priority number set to interrupt controller register. |

Return values

|                        |                                       |
|------------------------|---------------------------------------|
| <i>kStatus_Success</i> | Interrupt priority set successfully   |
| <i>kStatus_Fail</i>    | Failed to set the interrupt priority. |

#### 14.5.7 static status\_t IRQ\_SetPriority( IRQn\_Type *interrupt*, uint8\_t *priNum* ) [inline], [static]

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1\_INT\_VECTORS.

Parameters

|                  |                                                       |
|------------------|-------------------------------------------------------|
| <i>interrupt</i> | The IRQ to set.                                       |
| <i>priNum</i>    | Priority number set to interrupt controller register. |

Return values

|                        |                                       |
|------------------------|---------------------------------------|
| <i>kStatus_Success</i> | Interrupt priority set successfully   |
| <i>kStatus_Fail</i>    | Failed to set the interrupt priority. |

#### 14.5.8 static status\_t IRQ\_ClearPendingIRQ ( IRQn\_Type *interrupt* ) [inline], [static]

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                              |
|------------------|------------------------------|
| <i>interrupt</i> | The flag which IRQ to clear. |
|------------------|------------------------------|

Return values

|                        |                                       |
|------------------------|---------------------------------------|
| <i>kStatus_Success</i> | Interrupt priority set successfully   |
| <i>kStatus_Fail</i>    | Failed to set the interrupt priority. |

#### 14.5.9 static uint32\_t DisableGlobalIRQ ( void ) [inline], [static]

Disable the global interrupt and return the current primask register. User is required to provided the primask register for the [EnableGlobalIRQ\(\)](#).

Returns

Current primask value.

#### 14.5.10 static void EnableGlobalIRQ ( uint32\_t *primask* ) [inline], [static]

Set the primask register with the provided primask value but not just enable the primask. The idea is for the convenience of integration of RTOS. some RTOS get its own management mechanism of primask.

User is required to use the [EnableGlobalIRQ\(\)](#) and [DisableGlobalIRQ\(\)](#) in pair.

### Parameters

|                |                                                                                                                                    |
|----------------|------------------------------------------------------------------------------------------------------------------------------------|
| <i>primask</i> | value of primask register to be restored. The primask value is supposed to be provided by the <a href="#">DisableGlobalIRQ()</a> . |
|----------------|------------------------------------------------------------------------------------------------------------------------------------|

# Chapter 15

## DCDC: DCDC Converter

### 15.1 Overview

The MCUXpresso SDK provides a peripheral driver for the DCDC Converter (DCDC) module of MCUXpresso SDK devices.

The DCDC converter module is a synchronous buck mode DCDC converter. It can produce single outputs for SoC peripherals and external devices with high conversion efficiency. The converter can be operated in continuous or pulsed mode.

As a module to provide the power for hardware system, the DCDC starts working when the system is powered up before the software takes over the SoC. Some important configuration is done by the board settings. Before the software can access the DCDC's registers, the DCDC is already working normally with the default settings.

However, if the application needs to improve the DCDC's performance or change the default settings, the DCDC driver would help. The DCDC's register cannot be accessed by software before its initialization (open the clock gate). The user can configure the hardware according to the application guide from reference manual.

### 15.2 Function groups

#### 15.2.1 Initialization and deinitialization

This function group is to enable/disable the operations to DCDC module through the driver.

#### 15.2.2 Status

Provides functions to get the DCDC status.

#### 15.2.3 Misc control

Provides functions to set the DCDC's miscellaneous control.

#### Set point mode control

Provides functions to initialize/de-initialize DCDC module in set point mode.

## 15.3 Application guideline

### 15.3.1 Continous conduction mode

### 15.3.2 Discontinuous conduction mode

/\*!

## Data Structures

- struct `dcdc_detection_config_t`  
*Configuration for DCDC detection. [More...](#)*
- struct `dcdc_loop_control_config_t`  
*Configuration for the loop control. [More...](#)*
- struct `dcdc_low_power_config_t`  
*Configuration for DCDC low power. [More...](#)*
- struct `dcdc_internal_regulator_config_t`  
*Configuration for DCDC internal regulator. [More...](#)*
- struct `dcdc_min_power_config_t`  
*Configuration for min power setting. [More...](#)*

## Macros

- #define `FSL_DCDC_DRIVER_VERSION` (MAKE\_VERSION(2, 3, 0))  
*DCDC driver version.*

## Enumerations

- enum `_dcdc_status_flags_t` { `kDCDC_LockedOKStatus` = (1U << 0U) }  
*DCDC status flags.*
- enum `dcdc_comparator_current_bias_t` {  
`kDCDC_ComparatorCurrentBias50nA` = 0U,  
`kDCDC_ComparatorCurrentBias100nA` = 1U,  
`kDCDC_ComparatorCurrentBias200nA` = 2U,  
`kDCDC_ComparatorCurrentBias400nA` = 3U }  
*The current bias of low power comparator.*
- enum `dcdc_over_current_threshold_t` {  
`kDCDC_OverCurrentThresholdAlt0` = 0U,  
`kDCDC_OverCurrentThresholdAlt1` = 1U,  
`kDCDC_OverCurrentThresholdAlt2` = 2U,  
`kDCDC_OverCurrentThresholdAlt3` = 3U }  
*The threshold of over current detection.*
- enum `dcdc_peak_current_threshold_t` {  
`kDCDC_PeakCurrentThresholdAlt0` = 0U,  
`kDCDC_PeakCurrentThresholdAlt1` = 1U,  
`kDCDC_PeakCurrentThresholdAlt2` = 2U,  
`kDCDC_PeakCurrentThresholdAlt3` = 3U,  
`kDCDC_PeakCurrentThresholdAlt4` = 4U,

- `kDCDC_PeakCurrentThresholdAlt5 = 5U }`  
*The threshold if peak current detection.*
- enum `dcdc_count_charging_time_period_t` {
   
`kDCDC_CountChargingTimePeriod8Cycle = 0U,`
  
`kDCDC_CountChargingTimePeriod16Cycle = 1U }`
  
*The period of counting the charging times in power save mode.*
- enum `dcdc_count_charging_time_threshold_t` {
   
`kDCDC_CountChargingTimeThreshold32 = 0U,`
  
`kDCDC_CountChargingTimeThreshold64 = 1U,`
  
`kDCDC_CountChargingTimeThreshold16 = 2U,`
  
`kDCDC_CountChargingTimeThreshold8 = 3U }`
  
*The threshold of the counting number of charging times.*
- enum `dcdc_clock_source_t` {
   
`kDCDC_ClockAutoSwitch = 0U,`
  
`kDCDC_ClockInternalOsc = 1U,`
  
`kDCDC_ClockExternalOsc = 2U }`
  
*Oscillator clock option.*

## Initialization and deinitialization

- void `DCDC_Init` (DCDC\_Type \*base)  
*Enable the access to DCDC registers.*
- void `DCDC_Deinit` (DCDC\_Type \*base)  
*Disable the access to DCDC registers.*

## Status

- uint32\_t `DCDC_GetstatusFlags` (DCDC\_Type \*base)  
*Get DCDC status flags.*

## Misc control

- static void `DCDC_EnableOutputRangeComparator` (DCDC\_Type \*base, bool enable)  
*Enable the output range comparator.*
- void `DCDC_SetClockSource` (DCDC\_Type \*base, `dcdc_clock_source_t` clockSource)  
*Configure the DCDC clock source.*
- void `DCDC_GetDefaultDetectionConfig` (`dcdc_detection_config_t` \*config)  
*Get the default setting for detection configuration.*
- void `DCDC_SetDetectionConfig` (DCDC\_Type \*base, const `dcdc_detection_config_t` \*config)  
*Configure the DCDC detection.*
- void `DCDC_GetDefaultLowPowerConfig` (`dcdc_low_power_config_t` \*config)  
*Get the default setting for low power configuration.*
- void `DCDC_SetLowPowerConfig` (DCDC\_Type \*base, const `dcdc_low_power_config_t` \*config)  
*Configure the DCDC low power.*
- void `DCDC_ResetCurrentAlertSignal` (DCDC\_Type \*base, bool enable)  
*Reset current alert signal.*
- static void `DCDC_SetBandgapVoltageTrimValue` (DCDC\_Type \*base, uint32\_t trimValue)  
*Set the bangap trim value to trim bandgap voltage.*
- void `DCDC_GetDefaultLoopControlConfig` (`dcdc_loop_control_config_t` \*config)

- Get the default setting for loop control configuration.
- void **DCDC\_SetLoopControlConfig** (DCDC\_Type \*base, const dcdc\_loop\_control\_config\_t \*config)
 

Configure the DCDC loop control.
- void **DCDC\_SetMinPowerConfig** (DCDC\_Type \*base, const dcdc\_min\_power\_config\_t \*config)
 

Configure for the min power.
- static void **DCDC\_SetLPCComparatorBiasValue** (DCDC\_Type \*base, dcdc\_comparator\_current\_bias\_t biasVaule)
 

Set the current bias of low power comparator.
- static void **DCDC\_LockTargetVoltage** (DCDC\_Type \*base)
 

Lock target voltage.
- void **DCDC\_AdjustTargetVoltage** (DCDC\_Type \*base, uint32\_t VDDRun, uint32\_t VDDStandby)
 

Adjust the target voltage of VDD\_SOC in run mode and low power mode.
- void **DCDC\_AdjustRunTargetVoltage** (DCDC\_Type \*base, uint32\_t VDDRun)
 

Adjust the target voltage of VDD\_SOC in run mode.
- void **DCDC\_AdjustLowPowerTargetVoltage** (DCDC\_Type \*base, uint32\_t VDDStandby)
 

Adjust the target voltage of VDD\_SOC in low power mode.
- void **DCDC\_SetInternalRegulatorConfig** (DCDC\_Type \*base, const dcdc\_internal\_regulator\_config\_t \*config)
 

Configure the DCDC internal regulator.
- static void **DCDC\_EnableImproveTransition** (DCDC\_Type \*base, bool enable)
 

Enable/Disable to improve the transition from heavy load to light load.

## Application guideline

- void **DCDC\_BootIntoDCM** (DCDC\_Type \*base)
 

Boot DCDC into DCM(discontinous conduction mode).
- void **DCDC\_BootIntoCCM** (DCDC\_Type \*base)
 

Boot DCDC into CCM(continous conduction mode).

## 15.4 Data Structure Documentation

### 15.4.1 struct dcdc\_detection\_config\_t

#### Data Fields

- bool **enableXtalokDetection**

Enable xtalok detection circuit.
- bool **powerDownOverVoltageDetection**

Power down over-voltage detection comparator.
- bool **powerDownLowVlotageDetection**

Power down low-voltage detection comparator.
- bool **powerDownOverCurrentDetection**

Power down over-current detection.
- bool **powerDownPeakCurrentDetection**

Power down peak-current detection.
- bool **powerDownZeroCrossDetection**

Power down the zero cross detection function for discontinuous conductor mode.
- **dcdc\_over\_current\_threshold\_t OverCurrentThreshold**

The threshold of over current detection.

- [dcdc\\_peak\\_current\\_threshold\\_t PeakCurrentThreshold](#)  
*The threshold of peak current detection.*

### Field Documentation

- (1) [bool dcdc\\_detection\\_config\\_t::enableXtalokDetection](#)
- (2) [bool dcdc\\_detection\\_config\\_t::powerDownOverVoltageDetection](#)
- (3) [bool dcdc\\_detection\\_config\\_t::powerDownLowVoltageDetection](#)
- (4) [bool dcdc\\_detection\\_config\\_t::powerDownOverCurrentDetection](#)
- (5) [bool dcdc\\_detection\\_config\\_t::powerDownPeakCurrentDetection](#)
- (6) [bool dcdc\\_detection\\_config\\_t::powerDownZeroCrossDetection](#)
- (7) [dcdc\\_over\\_current\\_threshold\\_t dcdc\\_detection\\_config\\_t::OverCurrentThreshold](#)
- (8) [dcdc\\_peak\\_current\\_threshold\\_t dcdc\\_detection\\_config\\_t::PeakCurrentThreshold](#)

### 15.4.2 struct dc当地环控制配置

#### Data Fields

- [bool enableCommonHysteresis](#)  
*Enable hysteresis in switching converter common mode analog comparators.*
- [bool enableCommonThresholdDetection](#)  
*Increase the threshold detection for common mode analog comparator.*
- [bool enableInvertHysteresisSign](#)  
*Invert the sign of the hysteresis in DC-DC analog comparators.*
- [bool enableRCThresholdDetection](#)  
*Increase the threshold detection for RC scale circuit.*
- [uint32\\_t enableRCscaleCircuit](#)  
*Available range is 0~7.*
- [uint32\\_t complementFeedForwardStep](#)  
*Available range is 0~7.*

### Field Documentation

- (1) [bool dc当地环控制配置::enableCommonHysteresis](#)

This feature will improve transient supply ripple and efficiency.

- (2) **bool dcdc\_loop\_control\_config\_t::enableCommonThresholdDetection**
- (3) **bool dcdc\_loop\_control\_config\_t::enableInvertHysteresisSign**
- (4) **bool dcdc\_loop\_control\_config\_t::enableRCThresholdDetection**
- (5) **uint32\_t dcdc\_loop\_control\_config\_t::enableRCScaleCircuit**

Enable analog circuit of DC-DC converter to respond faster under transient load conditions.

- (6) **uint32\_t dcdc\_loop\_control\_config\_t::complementFeedForwardStep**

Two's complement feed forward step in duty cycle in the switching DC-DC converter. Each time this field makes a transition from 0x0, the loop filter of the DC-DC converter is stepped once by a value proportional to the change. This can be used to force a certain control loop behavior, such as improving response under known heavy load transients.

### 15.4.3 struct dc当地\_low\_power\_config\_t

#### Data Fields

- bool **enableOverloadDetection**  
*Enable the overload detection in power save mode, if current is larger than the overloading threshold (typical value is 50 mA), DCDC will switch to the run mode automatically.*
- bool **enableAdjustHystereticValue**  
*Adjust hysteretic value in low power from 12.5mV to 25mV.*
- **dcdc\_count\_charging\_time\_period\_t countChargingTimePeriod**  
*The period of counting the charging times in power save mode.*
- **dcdc\_count\_charging\_time\_threshold\_t countChargingTimeThreshold**  
*the threshold of the counting number of charging times during the period that lp\_overload\_freq\_sel sets in power save mode.*

**Field Documentation**

- (1) `bool dcdc_low_power_config_t::enableOverloadDetection`
- (2) `bool dcdc_low_power_config_t::enableAdjustHystereticValue`
- (3) `dcdc_count_charging_time_period_t dcdc_low_power_config_t::countChargingTimePeriod`
- (4) `dcdc_count_charging_time_threshold_t dcdc_low_power_config_t::countChargingTimeThreshold`

**15.4.4 struct dc当地内部调节器配置\_t****Data Fields**

- `bool enableLoadResistor`  
*control the load resistor of the internal regulator of DCDC, the load resistor is connected as default "true", and need set to "false" to disconnect the load resistor.*
- `uint32_t feedbackPoint`  
*Available range is 0~3.*

**Field Documentation**

- (1) `bool dc当地内部调节器配置_t::enableLoadResistor`
- (2) `uint32_t dc当地内部调节器配置_t::feedbackPoint`

Select the feedback point of the internal regulator.

**15.4.5 struct dc当地最小功率配置\_t****Data Fields**

- `bool enableUseHalfFreqForContinuous`  
*Set DCDC clock to half frequency for the continuous mode.*

**Field Documentation**

- (1) `bool dc当地最小功率配置_t::enableUseHalfFreqForContinuous`

**15.5 Macro Definition Documentation****15.5.1 #define FSL\_DCDC\_DRIVER\_VERSION (MAKE\_VERSION(2, 3, 0))**

Version 2.3.0.

## 15.6 Enumeration Type Documentation

### 15.6.1 enum \_dcdc\_status\_flags\_t

Enumerator

*kDCDC\_LockedOKStatus* Indicate DCDC status. 1'b1: DCDC already settled 1'b0: DCDC is settling.

### 15.6.2 enum dcdc\_comparator\_current\_bias\_t

Enumerator

*kDCDC\_ComparatorCurrentBias50nA* The current bias of low power comparator is 50nA.

*kDCDC\_ComparatorCurrentBias100nA* The current bias of low power comparator is 100nA.

*kDCDC\_ComparatorCurrentBias200nA* The current bias of low power comparator is 200nA.

*kDCDC\_ComparatorCurrentBias400nA* The current bias of low power comparator is 400nA.

### 15.6.3 enum dcdc\_over\_current\_threshold\_t

Enumerator

*kDCDC\_OverCurrentThresholdAlt0* 1A in the run mode, 0.25A in the power save mode.

*kDCDC\_OverCurrentThresholdAlt1* 2A in the run mode, 0.25A in the power save mode.

*kDCDC\_OverCurrentThresholdAlt2* 1A in the run mode, 0.2A in the power save mode.

*kDCDC\_OverCurrentThresholdAlt3* 2A in the run mode, 0.2A in the power save mode.

### 15.6.4 enum dcdc\_peak\_current\_threshold\_t

Enumerator

*kDCDC\_PeakCurrentThresholdAlt0* 150mA peak current threshold.

*kDCDC\_PeakCurrentThresholdAlt1* 250mA peak current threshold.

*kDCDC\_PeakCurrentThresholdAlt2* 350mA peak current threshold.

*kDCDC\_PeakCurrentThresholdAlt3* 450mA peak current threshold.

*kDCDC\_PeakCurrentThresholdAlt4* 550mA peak current threshold.

*kDCDC\_PeakCurrentThresholdAlt5* 650mA peak current threshold.

### 15.6.5 enum dc当地\_charging\_time\_period\_t

Enumerator

*kDCDC\_CountChargingTimePeriod8Cycle* Eight 32k cycle.

*kDCDC\_CountChargingTimePeriod16Cycle* Sixteen 32k cycle.

### 15.6.6 enum dc当地\_charging\_time\_threshold\_t

Enumerator

*kDCDC\_CountChargingTimeThreshold32* 0x0: 32.

*kDCDC\_CountChargingTimeThreshold64* 0x1: 64.

*kDCDC\_CountChargingTimeThreshold16* 0x2: 16.

*kDCDC\_CountChargingTimeThreshold8* 0x3: 8.

### 15.6.7 enum dc当地\_clock\_source\_t

Enumerator

*kDCDC\_ClockAutoSwitch* Automatic clock switch from internal oscillator to external clock.

*kDCDC\_ClockInternalOsc* Use internal oscillator.

*kDCDC\_ClockExternalOsc* Use external 24M crystal oscillator.

## 15.7 Function Documentation

### 15.7.1 void DCDC\_Init ( DCDC\_Type \* *base* )

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | DCDC peripheral base address. |
|-------------|-------------------------------|

### 15.7.2 void DCDC\_Deinit ( DCDC\_Type \* *base* )

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | DCDC peripheral base address. |
|-------------|-------------------------------|

### 15.7.3 **uint32\_t DCDC\_GetstatusFlags ( DCDC\_Type \* *base* )**

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | peripheral base address. |
|-------------|--------------------------|

Returns

Mask of asserted status flags. See to "\_dcdc\_status\_flags\_t".

### 15.7.4 **static void DCDC\_EnableOutputRangeComparator ( DCDC\_Type \* *base*, bool *enable* ) [inline], [static]**

The output range comparator is disabled by default.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | DCDC peripheral base address. |
| <i>enable</i> | Enable the feature or not.    |

### 15.7.5 **void DCDC\_SetClockSource ( DCDC\_Type \* *base*, dcdc\_clock\_source\_t *clockSource* )**

Parameters

|                    |                                                      |
|--------------------|------------------------------------------------------|
| <i>base</i>        | DCDC peripheral base address.                        |
| <i>clockSource</i> | Clock source for DCDC. See to "dcdc_clock_source_t". |

### 15.7.6 **void DCDC\_GetDefaultDetectionConfig ( dcdc\_detection\_config\_t \* *config* )**

The default configuration are set according to responding registers' setting when powered on. They are:

```
* config->enableXtalokDetection = false;
* config->powerDownOverVoltageDetection = true;
* config->powerDownLowVoltageDetection = false;
```

```
* config->powerDownOverCurrentDetection = true;
* config->powerDownPeakCurrentDetection = true;
* config->powerDownZeroCrossDetection = true;
* config->OverCurrentThreshold = kDCDC_OverCurrentThresholdAlt0;
* config->PeakCurrentThreshold = kDCDC_PeakCurrentThresholdAlt0;
*
```

## Parameters

|               |                                                                      |
|---------------|----------------------------------------------------------------------|
| <i>config</i> | Pointer to configuration structure. See to "dcdc_detection_config_t" |
|---------------|----------------------------------------------------------------------|

### 15.7.7 void DCDC\_SetDetectionConfig ( DCDC\_Type \* *base*, const dcdc\_detection\_config\_t \* *config* )

## Parameters

|               |                                                                      |
|---------------|----------------------------------------------------------------------|
| <i>base</i>   | DCDC peripheral base address.                                        |
| <i>config</i> | Pointer to configuration structure. See to "dcdc_detection_config_t" |

### 15.7.8 void DCDC\_GetDefaultLowPowerConfig ( dcdc\_low\_power\_config\_t \* *config* )

The default configuration are set according to responding registers' setting when powered on. They are:

```
* config->enableOverloadDetection = true;
* config->enableAdjustHystereticValue = false;
* config->countChargingTimePeriod = kDCDC_CountChargingTimePeriod8Cycle
    ;
* config->countChargingTimeThreshold = kDCDC_CountChargingTimeThreshold32
    ;
*
```

## Parameters

|               |                                                                      |
|---------------|----------------------------------------------------------------------|
| <i>config</i> | Pointer to configuration structure. See to "dcdc_low_power_config_t" |
|---------------|----------------------------------------------------------------------|

### 15.7.9 void DCDC\_SetLowPowerConfig ( DCDC\_Type \* *base*, const dcdc\_low\_power\_config\_t \* *config* )

Parameters

|               |                                                                       |
|---------------|-----------------------------------------------------------------------|
| <i>base</i>   | DCDC peripheral base address.                                         |
| <i>config</i> | Pointer to configuration structure. See to "dcdc_low_power_config_t". |

### 15.7.10 void DCDC\_ResetCurrentAlertSignal ( DCDC\_Type \* *base*, bool *enable* )

Alert signal is generate by peak current detection.

Parameters

|               |                                                                                    |
|---------------|------------------------------------------------------------------------------------|
| <i>base</i>   | DCDC peripheral base address.                                                      |
| <i>enable</i> | Switcher to reset signal. True means reset signal. False means don't reset signal. |

### 15.7.11 static void DCDC\_SetBandgapVoltageTrimValue ( DCDC\_Type \* *base*, uint32\_t *trimValue* ) [inline], [static]

Parameters

|                  |                                                   |
|------------------|---------------------------------------------------|
| <i>base</i>      | DCDC peripheral base address.                     |
| <i>trimValue</i> | The bangap trim value. Available range is 0U-31U. |

### 15.7.12 void DCDC\_GetDefaultLoopControlConfig ( dcdc\_loop\_control\_config\_t \* *config* )

The default configuration are set according to responding registers' setting when powered on. They are:

```
* config->enableCommonHysteresis = false;
* config->enableCommonThresholdDetection = false;
* config->enableInvertHysteresisSign = false;
* config->enableRCThresholdDetection = false;
* config->enableRCSCircuit = 0U;
* config->complementFeedForwardStep = 0U;
*
```

Parameters

|               |                                                                         |
|---------------|-------------------------------------------------------------------------|
| <i>config</i> | Pointer to configuration structure. See to "dcdc_loop_control_config_t" |
|---------------|-------------------------------------------------------------------------|

**15.7.13 void DCDC\_SetLoopControlConfig ( DCDC\_Type \* *base*, const dcdc\_loop\_control\_config\_t \* *config* )**

Parameters

|               |                                                                          |
|---------------|--------------------------------------------------------------------------|
| <i>base</i>   | DCDC peripheral base address.                                            |
| <i>config</i> | Pointer to configuration structure. See to "dcdc_loop_control_config_t". |

**15.7.14 void DCDC\_SetMinPowerConfig ( DCDC\_Type \* *base*, const dcdc\_min\_power\_config\_t \* *config* )**

Parameters

|               |                                                                       |
|---------------|-----------------------------------------------------------------------|
| <i>base</i>   | DCDC peripheral base address.                                         |
| <i>config</i> | Pointer to configuration structure. See to "dcdc_min_power_config_t". |

**15.7.15 static void DCDC\_SetLPComparatorBiasValue ( DCDC\_Type \* *base*, dcdc\_comparator\_current\_bias\_t *biasVaule* ) [inline], [static]**

Parameters

|                  |                                                                                      |
|------------------|--------------------------------------------------------------------------------------|
| <i>base</i>      | DCDC peripheral base address.                                                        |
| <i>biasVaule</i> | The current bias of low power comparator. Refer to "dcdc_comparator_current_bias_t". |

**15.7.16 static void DCDC\_LockTargetVoltage ( DCDC\_Type \* *base* ) [inline], [static]**

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | DCDC peripheral base address. |
|-------------|-------------------------------|

### 15.7.17 void DCDC\_AdjustTargetVoltage ( DCDC\_Type \* *base*, uint32\_t *VDDRun*, uint32\_t *VDDStandby* )

**Deprecated** Do not use this function. It has been superceded by [DCDC\\_AdjustRunTargetVoltage](#) and [DCDC\\_AdjustLowPowerTargetVoltage](#)

This function is to adjust the target voltage of DCDC output. Change them and finally wait until the output is stabled. Set the target value of run mode the same as low power mode before entering power save mode, because DCDC will switch back to run mode if it detects the current loading is larger than about 50 mA(typical value).

Parameters

|                   |                                                                                                    |
|-------------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>       | DCDC peripheral base address.                                                                      |
| <i>VDDRun</i>     | Target value in run mode. 25 mV each step from 0x00 to 0x1F. 00 is for 0.8V, 0x1F is for 1.575V.   |
| <i>VDDStandby</i> | Target value in low power mode. 25 mV each step from 0x00 to 0x4. 00 is for 0.9V, 0x4 is for 1.0V. |

### 15.7.18 void DCDC\_AdjustRunTargetVoltage ( DCDC\_Type \* *base*, uint32\_t *VDDRun* )

This function is to adjust the target voltage of DCDC output. Change them and finally wait until the output is stabled. Set the target value of run mode the same as low power mode before entering power save mode, because DCDC will switch back to run mode if it detects the current loading is larger than about 50 mA(typical value).

Parameters

|               |                                                                                                  |
|---------------|--------------------------------------------------------------------------------------------------|
| <i>base</i>   | DCDC peripheral base address.                                                                    |
| <i>VDDRun</i> | Target value in run mode. 25 mV each step from 0x00 to 0x1F. 00 is for 0.8V, 0x1F is for 1.575V. |

### 15.7.19 void DCDC\_AdjustLowPowerTargetVoltage ( DCDC\_Type \* *base*, uint32\_t *VDDStandby* )

This function is to adjust the target voltage of DCDC output. Change them and finally wait until the output is stabled. Set the target value of run mode the same as low power mode before entering power save mode, because DCDC will switch back to run mode if it detects the current loading is larger than about 50 mA(typical value).

Parameters

|                   |                                                                                                    |
|-------------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>       | DCDC peripheral base address.                                                                      |
| <i>VDDStandby</i> | Target value in low power mode. 25 mV each step from 0x00 to 0x4. 00 is for 0.9V, 0x4 is for 1.0V. |

### 15.7.20 void DCDC\_SetInternalRegulatorConfig ( DCDC\_Type \* *base*, const dcdc\_internal\_regulator\_config\_t \* *config* )

Parameters

|               |                                                                                |
|---------------|--------------------------------------------------------------------------------|
| <i>base</i>   | DCDC peripheral base address.                                                  |
| <i>config</i> | Pointer to configuration structure. See to "dcdc_internal_regulator_config_t". |

### 15.7.21 static void DCDC\_EnableImproveTransition ( DCDC\_Type \* *base*, bool *enable* ) [inline], [static]

It is valid while zero cross detection is enabled. If ouput exceeds the threshold, DCDC would return CCM from DCM.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | DCDC peripheral base address. |
| <i>enable</i> | Enable the feature or not.    |

### 15.7.22 void DCDC\_BootIntoDCM ( DCDC\_Type \* *base* )

pwd\_zcd=0x0; pwd\_cmp\_offset=0x0; dcdc\_loopctrl\_en\_rcscale= 0x5; DCM\_set\_ctrl=1'b1;

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | DCDC peripheral base address. |
|-------------|-------------------------------|

### 15.7.23 void DCDC\_BootIntoCCM ( DCDC\_Type \* *base* )

pwd\_zcd=0x1; pwd\_cmp\_offset=0x0; dcdc\_loopctrl\_en\_rcscale=0x3;

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | DCDC peripheral base address. |
|-------------|-------------------------------|

# Chapter 16

## DCP: Data Co-Processor

### 16.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Data Co-Processor (DCP) module. For security purposes, the Data Co-Processor (DCP) provides hardware acceleration for the cryptographic algorithms. The features of DCP are: Encryption Algorithms: AES-128 (ECB and CBC modes), Hashing Algorithms: SHA-1 and SHA-256, modified CRC-32, Key selection from the SNVS, DCP internal key storage, or general memory, Internal Memory for storing up to four AES-128 keys-when a key is written to a key slot it can be read only by the DCP AES-128 engine, IP slave interface, and DMA.

The driver comprises two sets of API functions.

In the first set, blocking APIs are provided, for selected subset of operations supported by DCP hardware. The DCP operations are complete (and results are made available for further usage) when a function returns. When called, these functions do not return until a DCP operation is complete. These functions use main CPU for simple polling loops to determine operation complete or error status.

The DCP work packets (descriptors) are placed on the system stack during the blocking API calls. The driver uses critical section (implemented as global interrupt enable/disable) for a short time whenever it needs to pass DCP work packets to DCP channel for processing. Therefore, the driver functions are designed to be re-entrant and as a consequence, one CPU thread can call one blocking API, such as AES Encrypt, while other CPU thread can call another blocking API, such as SHA-256 Update. The blocking functions provide typical interface to upper layer or application software.

In the second set, non-blocking variants of the first set APIs are provided. Internally, the blocking APIs are implemented as a non-blocking operation start, followed by a blocking wait (CPU polling DCP work packet's status word) for an operation completion. The non-blocking functions allow upper layer to inject an application specific operation after the DCP operation start and DCP channel complete events. RTOS event wait and RTOS event set can be an example of such an operation.

### 16.2 DCP Driver Initialization and Configuration

Initialize DCP after Power On Reset or reset cycle Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/dcp

The DCP Driver is initialized by calling the [DCP\\_Init\(\)](#) function. It enables the DCP module clock and configures DCP for operation.

### Key Management

The DCP implements four different key storage mechanisms: OTP-key, OTP-Unique key, Payload key, and SRAM-based keys that can be used by the software to securely store keys on a semi-permanent basis (kDCP\_KeySlot0 ~ kDCP\_KeySlot3). Once the function [DCP\\_AES\\_SetKey\(\)](#) is called, it sets the AES key for encryption/decryption with the [dcp\\_handle\\_t](#) structure. In case the SRAM-based key is selected,

the function copies and holds the key in memory. In case the OTP key is used, please make sure to set DCP related IOMUXC\_GPRs before DCP initialization, since the software reset of DCP must be issued to take these setting in effect. Refer to the DCP OTPKeySelect() function in BEE driver example.

### 16.3 Comments about API usage in RTOS

DCP transactional (encryption or hash) APIs can be called from multiple threads.

### 16.4 Comments about API usage in interrupt handler

Assuming the host processor receiving interrupt has the ownership of the DCP module, it can request Encrypt/Decrypt/Hash/public\_key operations in an interrupt routine. Additionally, as the DCP accesses system memory for its operation with data (such as message, plaintext, ciphertext, or keys) all data should remain valid until the DCP operation completes.

### 16.5 Comments about DCACHE

Input and output buffers passed to DCP API should be in non-cached memory or handled properly (DCACHE Clean and Invalidate) while using DCACHE.

## 16.6 DCP Driver Examples

### 16.6.1 Simple examples

Encrypt plaintext by AES engine Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/DCP

Compute hash (CRC-32) The CRC-32 algorithm implements a 32-bit CRC algorithm similar to the one used by Ethernet and many other protocols. The CRC differs from the Unix cksum() function in these four ways: The CRC initial value is 0xFFFFFFFF instead of 0x00000000, final XOR value is 0x00000000 instead of 0xFFFFFFFF, the logic pads the zeros to a 32-bit boundary for the trailing bytes, and it does not post-pend the file length. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/DCP

Compute hash (SHA-256) Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/DCP

## Modules

- [DCP AES blocking driver](#)
- [DCP AES non-blocking driver](#)
- [DCP HASH driver](#)

## Data Structures

- struct [dcp\\_work\\_packet\\_t](#)  
*DCP's work packet.* [More...](#)
- struct [dcp\\_handle\\_t](#)  
*Specify DCP's key resource and DCP channel.* [More...](#)

- struct `dcp_context_t`  
*DCP's context buffer, used by DCP for context switching between channels.* [More...](#)
- struct `dcp_config_t`  
*DCP's configuration structure.* [More...](#)

## Enumerations

- enum `_dcp_status` { `kStatus_DCP_Again` = MAKE\_STATUS(kStatusGroup\_DCP, 0) }  
*DCP status return codes.*
- enum `_dcp_ch_enable_t` {  
`kDCP_chDisable` = 0U,  
`kDCP_ch0Enable` = 1U,  
`kDCP_ch1Enable` = 2U,  
`kDCP_ch2Enable` = 4U,  
`kDCP_ch3Enable` = 8U,  
`kDCP_chEnableAll` = 15U }  
*DCP channel enable.*
- enum `_dcp_ch_int_enable_t` {  
`kDCP_chIntDisable` = 0U,  
`kDCP_ch0IntEnable` = 1U,  
`kDCP_ch1IntEnable` = 2U,  
`kDCP_ch2IntEnable` = 4U,  
`kDCP_ch3IntEnable` = 8U }  
*DCP interrupt enable.*
- enum `dcp_channel_t` {  
`kDCP_Channel0` = (1u << 16),  
`kDCP_Channel1` = (1u << 17),  
`kDCP_Channel2` = (1u << 18),  
`kDCP_Channel3` = (1u << 19) }  
*DCP channel selection.*
- enum `dcp_key_slot_t` {  
`kDCP_KeySlot0` = 0U,  
`kDCP_KeySlot1` = 1U,  
`kDCP_KeySlot2` = 2U,  
`kDCP_KeySlot3` = 3U,  
`kDCP_OtpKey` = 4U,  
`kDCP_OtpUniqueKey` = 5U,  
`kDCP_PayloadKey` = 6U }  
*DCP key slot selection.*
- enum `dcp_swap_t`  
*DCP key, input & output swap options.*

## Functions

- void `DCP_Init` (DCP\_Type \*base, const `dcp_config_t` \*config)  
*Enables clock to and enables DCP.*
- void `DCP_Deinit` (DCP\_Type \*base)  
*Disable DCP clock.*

- void `DCP_GetDefaultConfig (dcp_config_t *config)`  
*Gets the default configuration structure.*
- `status_t DCP_WaitForChannelComplete (DCP_Type *base, dcp_handle_t *handle)`  
*Poll and wait on DCP channel.*

## Driver version

- #define `FSL_DCP_DRIVER_VERSION (MAKE_VERSION(2, 1, 7))`  
*DCP driver version.*

## 16.7 Data Structure Documentation

### 16.7.1 struct dcp\_work\_packet\_t

### 16.7.2 struct dcp\_handle\_t

#### Data Fields

- `dcp_channel_t channel`  
*Specify DCP channel.*
- `dcp_key_slot_t keySlot`  
*For operations with key (such as AES encryption/decryption), specify DCP key slot.*
- `uint32_t swapConfig`  
*For configuration of key, input, output byte/word swap options.*

#### Field Documentation

(1) `dcp_channel_t dcp_handle_t::channel`

(2) `dcp_key_slot_t dcp_handle_t::keySlot`

### 16.7.3 struct dcp\_context\_t

### 16.7.4 struct dcp\_config\_t

#### Data Fields

- `bool gatherResidualWrites`  
*Enable the ragged writes to the unaligned buffers.*
- `bool enableContextCaching`  
*Enable the caching of contexts between the operations.*
- `bool enableContextSwitching`  
*Enable automatic context switching for the channels.*
- `uint8_t enableChannel`  
*DCP channel enable.*
- `uint8_t enableChannelInterrupt`  
*Per-channel interrupt enable.*

## Field Documentation

- (1) `bool dcp_config_t::gatherResidualWrites`
- (2) `bool dcp_config_t::enableContextCaching`
- (3) `bool dcp_config_t::enableContextSwitching`
- (4) `uint8_t dcp_config_t::enableChannel`
- (5) `uint8_t dcp_config_t::enableChannelInterrupt`

## 16.8 Macro Definition Documentation

### 16.8.1 #define FSL\_DCP\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 7))

Version 2.1.7.

Current version: 2.1.7

Change log:

- Version 2.1.7
  - Bug Fix
    - \* Reduce optimization level for critical functions working with SRF.
- Version 2.1.6
  - Bug Fix
    - \* MISRA C-2012 issue fix.
- Version 2.1.5
  - Improvements
    - \* Add support for DCACHE.
- Version 2.1.4
  - Bug Fix
    - \* Fix CRC-32 computation issue on the code's block boundary size.
- Version 2.1.3
  - Bug Fix
    - \* MISRA C-2012 issue fixed: rule 10.1, 10.3, 10.4, 11.9, 14.4, 16.4 and 17.7.
- Version 2.1.2
  - Fix sign-compare warning in dcp\_reverse\_and\_copy.
- Version 2.1.1
  - Add DCP status clearing when channel operation is complete
- 2.1.0
  - Add byte/word swap feature for key, input and output data
- Version 2.0.0
  - Initial version

## 16.9 Enumeration Type Documentation

### 16.9.1 enum \_dcp\_status

Enumerator

*kStatus\_DCP\_Again* Non-blocking function shall be called again.

### 16.9.2 enum \_dcp\_ch\_enable\_t

Enumerator

*kDCP\_chDisable* DCP channel disable.  
*kDCP\_ch0Enable* DCP channel 0 enable.  
*kDCP\_ch1Enable* DCP channel 1 enable.  
*kDCP\_ch2Enable* DCP channel 2 enable.  
*kDCP\_ch3Enable* DCP channel 3 enable.  
*kDCP\_chEnableAll* DCP channel enable all.

### 16.9.3 enum \_dcp\_ch\_int\_enable\_t

Enumerator

*kDCP\_chIntDisable* DCP interrupts disable.  
*kDCP\_ch0IntEnable* DCP channel 0 interrupt enable.  
*kDCP\_ch1IntEnable* DCP channel 1 interrupt enable.  
*kDCP\_ch2IntEnable* DCP channel 2 interrupt enable.  
*kDCP\_ch3IntEnable* DCP channel 3 interrupt enable.

### 16.9.4 enum dcp\_channel\_t

Enumerator

*kDCP\_Channel0* DCP channel 0.  
*kDCP\_Channel1* DCP channel 1.  
*kDCP\_Channel2* DCP channel 2.  
*kDCP\_Channel3* DCP channel 3.

### 16.9.5 enum dcp\_key\_slot\_t

Enumerator

*kDCP\_KeySlot0* DCP key slot 0.  
*kDCP\_KeySlot1* DCP key slot 1.  
*kDCP\_KeySlot2* DCP key slot 2.  
*kDCP\_KeySlot3* DCP key slot 3.  
*kDCP\_OtpKey* DCP OTP key.  
*kDCP\_OtpUniqueKey* DCP unique OTP key.  
*kDCP\_PayloadKey* DCP payload key.

### 16.9.6 enum dcp\_swap\_t

## 16.10 Function Documentation

### 16.10.1 void DCP\_Init ( **DCP\_Type** \* *base*, **const dcp\_config\_t** \* *config* )

Enable DCP clock and configure DCP.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | DCP base address                    |
| <i>config</i> | Pointer to configuration structure. |

### 16.10.2 void DCP\_Deinit ( **DCP\_Type** \* *base* )

Reset DCP and Disable DCP clock.

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | DCP base address |
|-------------|------------------|

### 16.10.3 void DCP\_GetDefaultConfig ( **dcp\_config\_t** \* *config* )

This function initializes the DCP configuration structure to a default value. The default values are as follows. `dcpConfig->gatherResidualWrites = true;` `dcpConfig->enableContextCaching = true;` `dcpConfig->enableContextSwitching = true;` `dcpConfig->enableChannnel = kDCP_chEnableAll;` `dcpConfig->enableChannelInterrupt = kDCP_chIntDisable;`

Parameters

|     |               |                                     |
|-----|---------------|-------------------------------------|
| out | <i>config</i> | Pointer to configuration structure. |
|-----|---------------|-------------------------------------|

#### 16.10.4 **status\_t DCP\_WaitForChannelComplete ( DCP\_Type \* *base*, dcp\_handle\_t \* *handle* )**

Polls the specified DCP channel until current it completes activity.

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | DCP peripheral base address. |
| <i>handle</i> | Specifies DCP channel.       |

Returns

kStatus\_Success When data processing completes without error.

kStatus\_Fail When error occurs.

## 16.11 DCP AES blocking driver

### 16.11.1 Overview

This section describes the programming interface of the DCP AES blocking driver.

### Macros

- `#define DCP_AES_BLOCK_SIZE 16`  
*AES block size in bytes.*

### Functions

- `status_t DCP_AES_SetKey (DCP_Type *base, dcp_handle_t *handle, const uint8_t *key, size_t keySize)`  
*Set AES key to `dcp_handle_t` struct and optionally to DCP.*
- `status_t DCP_AES_EncryptEcb (DCP_Type *base, dcp_handle_t *handle, const uint8_t *plaintext, uint8_t *ciphertext, size_t size)`  
*Encrypts AES on one or multiple 128-bit block(s).*
- `status_t DCP_AES_DecryptEcb (DCP_Type *base, dcp_handle_t *handle, const uint8_t *ciphertext, uint8_t *plaintext, size_t size)`  
*Decrypts AES on one or multiple 128-bit block(s).*
- `status_t DCP_AES_EncryptCbc (DCP_Type *base, dcp_handle_t *handle, const uint8_t *plaintext, uint8_t *ciphertext, size_t size, const uint8_t iv[16])`  
*Encrypts AES using CBC block mode.*
- `status_t DCP_AES_DecryptCbc (DCP_Type *base, dcp_handle_t *handle, const uint8_t *ciphertext, uint8_t *plaintext, size_t size, const uint8_t iv[16])`  
*Decrypts AES using CBC block mode.*

### 16.11.2 Function Documentation

#### 16.11.2.1 `status_t DCP_AES_SetKey ( DCP_Type * base, dcp_handle_t * handle, const uint8_t * key, size_t keySize )`

Sets the AES key for encryption/decryption with the `dcp_handle_t` structure. The `dcp_handle_t` input argument specifies keySlot. If the keySlot is `kDCP_OtpKey`, the function will check the `OTP_KEY_READY` bit and will return it's ready to use status. For other keySlot selections, the function will copy and hold the key in `dcp_handle_t` struct. If the keySlot is one of the four DCP SRAM-based keys (one of `kDCP_KeySlot0`, `kDCP_KeySlot1`, `kDCP_KeySlot2`, `kDCP_KeySlot3`), this function will also load the supplied key to the specified keySlot in DCP.

Parameters

|                |                                        |
|----------------|----------------------------------------|
| <i>base</i>    | DCP peripheral base address.           |
| <i>handle</i>  | Handle used for the request.           |
| <i>key</i>     | 0-mod-4 aligned pointer to AES key.    |
| <i>keySize</i> | AES key size in bytes. Shall equal 16. |

Returns

status from set key operation

#### **16.11.2.2 status\_t DCP\_AES\_EncryptEcb ( DCP\_Type \* *base*, dcp\_handle\_t \* *handle*, const uint8\_t \* *plaintext*, uint8\_t \* *ciphertext*, size\_t *size* )**

Encrypts AES. The source plaintext and destination ciphertext can overlap in system memory.

Parameters

|            |                   |                                                                       |
|------------|-------------------|-----------------------------------------------------------------------|
|            | <i>base</i>       | DCP peripheral base address                                           |
|            | <i>handle</i>     | Handle used for this request.                                         |
|            | <i>plaintext</i>  | Input plain text to encrypt                                           |
| <i>out</i> | <i>ciphertext</i> | Output cipher text                                                    |
|            | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |

Returns

Status from encrypt operation

#### **16.11.2.3 status\_t DCP\_AES\_DecryptEcb ( DCP\_Type \* *base*, dcp\_handle\_t \* *handle*, const uint8\_t \* *ciphertext*, uint8\_t \* *plaintext*, size\_t *size* )**

Decrypts AES. The source ciphertext and destination plaintext can overlap in system memory.

Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                           |
|     | <i>handle</i>     | Handle used for this request.                                         |
|     | <i>ciphertext</i> | Input plain text to encrypt                                           |
| out | <i>plaintext</i>  | Output cipher text                                                    |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |

Returns

Status from decrypt operation

#### 16.11.2.4 status\_t DCP\_AES\_EncryptCbc ( **DCP\_Type \* base**, **dcp\_handle\_t \* handle**, **const uint8\_t \* plaintext**, **uint8\_t \* ciphertext**, **size\_t size**, **const uint8\_t iv[16]** )

Encrypts AES using CBC block mode. The source plaintext and destination ciphertext can overlap in system memory.

Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                           |
|     | <i>handle</i>     | Handle used for this request.                                         |
|     | <i>plaintext</i>  | Input plain text to encrypt                                           |
| out | <i>ciphertext</i> | Output cipher text                                                    |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |
|     | <i>iv</i>         | Input initial vector to combine with the first input block.           |

Returns

Status from encrypt operation

#### 16.11.2.5 status\_t DCP\_AES\_DecryptCbc ( **DCP\_Type \* base**, **dcp\_handle\_t \* handle**, **const uint8\_t \* ciphertext**, **uint8\_t \* plaintext**, **size\_t size**, **const uint8\_t iv[16]** )

Decrypts AES using CBC block mode. The source ciphertext and destination plaintext can overlap in system memory.

## Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                           |
|     | <i>handle</i>     | Handle used for this request.                                         |
|     | <i>ciphertext</i> | Input cipher text to decrypt                                          |
| out | <i>plaintext</i>  | Output plain text                                                     |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |
|     | <i>iv</i>         | Input initial vector to combine with the first input block.           |

## Returns

Status from decrypt operation

## 16.12 DCP AES non-blocking driver

### 16.12.1 Overview

This section describes the programming interface of the DCP AES non-blocking driver.

## Functions

- `status_t DCP_AES_EncryptEcbNonBlocking (DCP_Type *base, dcp_handle_t *handle, dcp_work_packet_t *dcpPacket, const uint8_t *plaintext, uint8_t *ciphertext, size_t size)`  
*Encrypts AES using the ECB block mode.*
- `status_t DCP_AES_DecryptEcbNonBlocking (DCP_Type *base, dcp_handle_t *handle, dcp_work_packet_t *dcpPacket, const uint8_t *ciphertext, uint8_t *plaintext, size_t size)`  
*Decrypts AES using ECB block mode.*
- `status_t DCP_AES_EncryptCbcNonBlocking (DCP_Type *base, dcp_handle_t *handle, dcp_work_packet_t *dcpPacket, const uint8_t *plaintext, uint8_t *ciphertext, size_t size, const uint8_t *iv)`  
*Encrypts AES using CBC block mode.*
- `status_t DCP_AES_DecryptCbcNonBlocking (DCP_Type *base, dcp_handle_t *handle, dcp_work_packet_t *dcpPacket, const uint8_t *ciphertext, uint8_t *plaintext, size_t size, const uint8_t *iv)`  
*Decrypts AES using CBC block mode.*

### 16.12.2 Function Documentation

#### 16.12.2.1 `status_t DCP_AES_EncryptEcbNonBlocking ( DCP_Type * base, dcp_handle_t * handle, dcp_work_packet_t * dcpPacket, const uint8_t * plaintext, uint8_t * ciphertext, size_t size )`

Puts AES ECB encrypt work packet to DCP channel.

Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                           |
|     | <i>handle</i>     | Handle used for this request.                                         |
| out | <i>dcpPacket</i>  | Memory for the DCP work packet.                                       |
|     | <i>plaintext</i>  | Input plain text to encrypt.                                          |
| out | <i>ciphertext</i> | Output cipher text                                                    |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |

Returns

`kStatus_Success` The work packet has been scheduled at DCP channel.

`kStatus_DCP_Again` The DCP channel is busy processing previous request.

**16.12.2.2 status\_t DCP\_AES\_DecryptEcbNonBlocking ( DCP\_Type \* *base*, dcp\_handle\_t \* *handle*, dcp\_work\_packet\_t \* *dcpPacket*, const uint8\_t \* *ciphertext*, uint8\_t \* *plaintext*, size\_t *size* )**

Puts AES ECB decrypt *dcpPacket* to DCP input job ring.

Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                           |
|     | <i>handle</i>     | Handle used for this request.                                         |
| out | <i>dcpPacket</i>  | Memory for the DCP work packet.                                       |
|     | <i>ciphertext</i> | Input cipher text to decrypt                                          |
| out | <i>plaintext</i>  | Output plain text                                                     |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |

Returns

kStatus\_Success The work packet has been scheduled at DCP channel.

kStatus\_DCP\_Again The DCP channel is busy processing previous request.

#### 16.12.2.3 status\_t DCP\_AES\_EncryptCbcNonBlocking ( DCP\_Type \* *base*, dcp\_handle\_t \* *handle*, dcp\_work\_packet\_t \* *dcpPacket*, const uint8\_t \* *plaintext*, uint8\_t \* *ciphertext*, size\_t *size*, const uint8\_t \* *iv* )

Puts AES CBC encrypt *dcpPacket* to DCP input job ring.

Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                           |
|     | <i>handle</i>     | Handle used for this request. Specifies jobRing.                      |
| out | <i>dcpPacket</i>  | Memory for the DCP work packet.                                       |
|     | <i>plaintext</i>  | Input plain text to encrypt                                           |
| out | <i>ciphertext</i> | Output cipher text                                                    |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |
|     | <i>iv</i>         | Input initial vector to combine with the first input block.           |

Returns

kStatus\_Success The work packet has been scheduled at DCP channel.

kStatus\_DCP\_Again The DCP channel is busy processing previous request.

#### 16.12.2.4 status\_t DCP\_AES\_DecryptCbcNonBlocking ( DCP\_Type \* *base*, dcp\_handle\_t \* *handle*, dcp\_work\_packet\_t \* *dcpPacket*, const uint8\_t \* *ciphertext*, uint8\_t \* *plaintext*, size\_t *size*, const uint8\_t \* *iv* )

Puts AES CBC decrypt *dcpPacket* to DCP input job ring.

## Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                           |
|     | <i>handle</i>     | Handle used for this request. Specifies jobRing.                      |
| out | <i>dcpPacket</i>  | Memory for the DCP work packet.                                       |
|     | <i>ciphertext</i> | Input cipher text to decrypt                                          |
| out | <i>plaintext</i>  | Output plain text                                                     |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |
|     | <i>iv</i>         | Input initial vector to combine with the first input block.           |

## Returns

kStatus\_Success The work packet has been scheduled at DCP channel.

kStatus\_DCP\_Again The DCP channel is busy processing previous request.

## 16.13 DCP HASH driver

### 16.13.1 Overview

This section describes the programming interface of the DCP HASH driver.

### Data Structures

- struct `dcp_hash_ctx_t`  
*Storage type used to save hash context. [More...](#)*

### Macros

- `#define DCP_SHA_BLOCK_SIZE 128U`  
*DCP HASH Context size.*
- `#define DCP_HASH_BLOCK_SIZE DCP_SHA_BLOCK_SIZE`  
*DCP hash block size.*
- `#define DCP_HASH_CTX_SIZE 64`  
*DCP HASH Context size.*

### Enumerations

- enum `dcp_hash_algo_t` {
   
`kDCP_Sha1,`
  
`kDCP_Sha256,`
  
`kDCP_Crc32 }`
  
*Supported cryptographic block cipher functions for HASH creation.*

### Functions

- `status_t DCP_HASH_Init (DCP_Type *base, dcp_handle_t *handle, dcp_hash_ctx_t *ctx, dcp_hash_algo_t algo)`  
*Initialize HASH context.*
- `status_t DCP_HASH_Update (DCP_Type *base, dcp_hash_ctx_t *ctx, const uint8_t *input, size_t inputSize)`  
*Add data to current HASH.*
- `status_t DCP_HASH_Finish (DCP_Type *base, dcp_hash_ctx_t *ctx, uint8_t *output, size_t *outputSize)`  
*Finalize hashing.*
- `status_t DCP_HASH (DCP_Type *base, dcp_handle_t *handle, dcp_hash_algo_t algo, const uint8_t *input, size_t inputSize, uint8_t *output, size_t *outputSize)`  
*Create HASH on given data.*

## 16.13.2 Data Structure Documentation

### 16.13.2.1 struct dcp\_hash\_ctx\_t

## 16.13.3 Macro Definition Documentation

### 16.13.3.1 #define DCP\_SHA\_BLOCK\_SIZE 128U

internal buffer block size

### 16.13.3.2 #define DCP\_HASH\_CTX\_SIZE 64

## 16.13.4 Enumeration Type Documentation

### 16.13.4.1 enum dcp\_hash\_algo\_t

Enumerator

*kDCP\_Sha1* SHA\_1.  
*kDCP\_Sha256* SHA\_256.  
*kDCP\_Crc32* CRC\_32.

## 16.13.5 Function Documentation

### 16.13.5.1 status\_t DCP\_HASH\_Init ( DCP\_Type \* *base*, dcp\_handle\_t \* *handle*, dcp\_hash\_ctx\_t \* *ctx*, dcp\_hash\_algo\_t *algo* )

This function initializes the HASH.

Parameters

|     |               |                                                    |
|-----|---------------|----------------------------------------------------|
|     | <i>base</i>   | DCP peripheral base address                        |
|     | <i>handle</i> | Specifies the DCP channel used for hashing.        |
| out | <i>ctx</i>    | Output hash context                                |
|     | <i>algo</i>   | Underlaying algorithm to use for hash computation. |

Returns

Status of initialization

### 16.13.5.2 status\_t DCP\_HASH\_Update ( ***DCP\_Type \* base***, ***dcp\_hash\_ctx\_t \* ctx***, ***const uint8\_t \* input***, ***size\_t inputSize*** )

Add data to current HASH. This can be called repeatedly with an arbitrary amount of data to be hashed. The function blocks. If it returns kStatus\_Success, the running hash has been updated (DCP has processed the input data), so the memory at the input pointer can be released back to system. The DCP context buffer is updated with the running hash and with all necessary information to support possible context switch.

Parameters

|               |                  |                             |
|---------------|------------------|-----------------------------|
|               | <i>base</i>      | DCP peripheral base address |
| <i>in,out</i> | <i>ctx</i>       | HASH context                |
|               | <i>input</i>     | Input data                  |
|               | <i>inputSize</i> | Size of input data in bytes |

Returns

Status of the hash update operation

### 16.13.5.3 status\_t DCP\_HASH\_Finish ( ***DCP\_Type \* base***, ***dcp\_hash\_ctx\_t \* ctx***, ***uint8\_t \* output***, ***size\_t \* outputSize*** )

Outputs the final hash (computed by [DCP\\_HASH\\_Update\(\)](#)) and erases the context.

Parameters

|               |                   |                                                                                                                                                                            |
|---------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|               | <i>base</i>       | DCP peripheral base address                                                                                                                                                |
| <i>in,out</i> | <i>ctx</i>        | Input hash context                                                                                                                                                         |
| <i>out</i>    | <i>output</i>     | Output hash data                                                                                                                                                           |
| <i>in,out</i> | <i>outputSize</i> | Optional parameter (can be passed as NULL). On function entry, it specifies the size of output[] buffer. On function return, it stores the number of updated output bytes. |

Returns

Status of the hash finish operation

### 16.13.5.4 status\_t DCP\_HASH ( ***DCP\_Type \* base***, ***dcp\_handle\_t \* handle***, ***dcp\_hash\_algo\_t algo***, ***const uint8\_t \* input***, ***size\_t inputSize***, ***uint8\_t \* output***, ***size\_t \* outputSize*** )

Perform the full SHA or CRC32 in one function call. The function is blocking.

## Parameters

|     |                   |                                                               |
|-----|-------------------|---------------------------------------------------------------|
|     | <i>base</i>       | DCP peripheral base address                                   |
|     | <i>handle</i>     | Handle used for the request.                                  |
|     | <i>algo</i>       | Underlying algorithm to use for hash computation.             |
|     | <i>input</i>      | Input data                                                    |
|     | <i>inputSize</i>  | Size of input data in bytes                                   |
| out | <i>output</i>     | Output hash data                                              |
| out | <i>outputSize</i> | Output parameter storing the size of the output hash in bytes |

## Returns

Status of the one call hash operation.

# Chapter 17

## DMAMUX: Direct Memory Access Multiplexer Driver

### 17.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Direct Memory Access Multiplexer (DMAMUX) of MCUXpresso SDK devices.

### 17.2 Typical use case

#### 17.2.1 DMAMUX Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/dmamux

#### Driver version

- `#define FSL_DMAMUX_DRIVER_VERSION (MAKE_VERSION(2, 1, 0))`  
*DMAMUX driver version 2.1.0.*

#### DMAMUX Initialization and de-initialization

- `void DMAMUX_Init (DMAMUX_Type *base)`  
*Initializes the DMAMUX peripheral.*
- `void DMAMUX_Deinit (DMAMUX_Type *base)`  
*Deinitializes the DMAMUX peripheral.*

#### DMAMUX Channel Operation

- `static void DMAMUX_EnableChannel (DMAMUX_Type *base, uint32_t channel)`  
*Enables the DMAMUX channel.*
- `static void DMAMUX_DisableChannel (DMAMUX_Type *base, uint32_t channel)`  
*Disables the DMAMUX channel.*
- `static void DMAMUX_SetSource (DMAMUX_Type *base, uint32_t channel, int32_t source)`  
*Configures the DMAMUX channel source.*
- `static void DMAMUX_EnablePeriodTrigger (DMAMUX_Type *base, uint32_t channel)`  
*Enables the DMAMUX period trigger.*
- `static void DMAMUX_DisablePeriodTrigger (DMAMUX_Type *base, uint32_t channel)`  
*Disables the DMAMUX period trigger.*
- `static void DMAMUX_EnableAlwaysOn (DMAMUX_Type *base, uint32_t channel, bool enable)`  
*Enables the DMA channel to be always ON.*

### 17.3 Macro Definition Documentation

#### 17.3.1 `#define FSL_DMAMUX_DRIVER_VERSION (MAKE_VERSION(2, 1, 0))`

## 17.4 Function Documentation

### 17.4.1 void DMAMUX\_Init ( **DMAMUX\_Type** \* *base* )

This function ungates the DMAMUX clock.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | DMAMUX peripheral base address. |
|-------------|---------------------------------|

#### 17.4.2 void DMAMUX\_Deinit ( DMAMUX\_Type \* *base* )

This function gates the DMAMUX clock.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | DMAMUX peripheral base address. |
|-------------|---------------------------------|

#### 17.4.3 static void DMAMUX\_EnableChannel ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function enables the DMAMUX channel.

Parameters

|                |                                 |
|----------------|---------------------------------|
| <i>base</i>    | DMAMUX peripheral base address. |
| <i>channel</i> | DMAMUX channel number.          |

#### 17.4.4 static void DMAMUX\_DisableChannel ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function disables the DMAMUX channel.

Note

The user must disable the DMAMUX channel before configuring it.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | DMAMUX peripheral base address. |
|-------------|---------------------------------|

|                |                        |
|----------------|------------------------|
| <i>channel</i> | DMAMUX channel number. |
|----------------|------------------------|

#### 17.4.5 static void DMAMUX\_SetSource ( DMAMUX\_Type \* *base*, uint32\_t *channel*, int32\_t *source* ) [inline], [static]

Parameters

|                |                                                                                                                                   |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | DMAMUX peripheral base address.                                                                                                   |
| <i>channel</i> | DMAMUX channel number.                                                                                                            |
| <i>source</i>  | Channel source, which is used to trigger the DMA transfer. User need to use the dma_request_source_t type as the input parameter. |

#### 17.4.6 static void DMAMUX\_EnablePeriodTrigger ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function enables the DMAMUX period trigger feature.

Parameters

|                |                                 |
|----------------|---------------------------------|
| <i>base</i>    | DMAMUX peripheral base address. |
| <i>channel</i> | DMAMUX channel number.          |

#### 17.4.7 static void DMAMUX\_DisablePeriodTrigger ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function disables the DMAMUX period trigger.

Parameters

|                |                                 |
|----------------|---------------------------------|
| <i>base</i>    | DMAMUX peripheral base address. |
| <i>channel</i> | DMAMUX channel number.          |

#### 17.4.8 static void DMAMUX\_EnableAlwaysOn ( DMAMUX\_Type \* *base*, uint32\_t *channel*, bool *enable* ) [inline], [static]

This function enables the DMAMUX channel always ON feature.

## Parameters

|                |                                                                                  |
|----------------|----------------------------------------------------------------------------------|
| <i>base</i>    | DMAMUX peripheral base address.                                                  |
| <i>channel</i> | DMAMUX channel number.                                                           |
| <i>enable</i>  | Switcher of the always ON feature. "true" means enabled, "false" means disabled. |

# Chapter 18

## eDMA: Enhanced Direct Memory Access (eDMA) Controller Driver

### 18.1 Overview

The MCUXpresso SDK provides a peripheral driver for the enhanced Direct Memory Access (eDMA) of MCUXpresso SDK devices.

### 18.2 Typical use case

#### 18.2.1 eDMA Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/edma

## Data Structures

- struct [edma\\_config\\_t](#)  
*eDMA global configuration structure.* [More...](#)
- struct [edma\\_transfer\\_config\\_t](#)  
*eDMA transfer configuration* [More...](#)
- struct [edma\\_channel\\_Preemption\\_config\\_t](#)  
*eDMA channel priority configuration* [More...](#)
- struct [edma\\_minor\\_offset\\_config\\_t](#)  
*eDMA minor offset configuration* [More...](#)
- struct [edma\\_tcd\\_t](#)  
*eDMA TCD.* [More...](#)
- struct [edma\\_handle\\_t](#)  
*eDMA transfer handle structure* [More...](#)

## Macros

- #define [DMA\\_DCHPRI\\_INDEX](#)(channel) (((channel) & ~0x03U) | (3U - ((channel)&0x03U)))  
*Compute the offset unit from DCHPRI3.*

## Typedefs

- typedef void(\* [edma\\_callback](#) )(struct \_edma\_handle \*handle, void \*userData, bool transferDone, uint32\_t tcds)  
*Define callback function for eDMA.*

## Enumerations

- enum `edma_transfer_size_t` {
   
    `kEDMA_TransferSize1Bytes` = 0x0U,
   
    `kEDMA_TransferSize2Bytes` = 0x1U,
   
    `kEDMA_TransferSize4Bytes` = 0x2U,
   
    `kEDMA_TransferSize8Bytes` = 0x3U,
   
    `kEDMA_TransferSize16Bytes` = 0x4U,
   
    `kEDMA_TransferSize32Bytes` = 0x5U }

*eDMA transfer configuration*

- enum `edma_modulo_t` {
   
    `kEDMA_ModuloDisable` = 0x0U,
   
    `kEDMA_Modulo2bytes`,
   
    `kEDMA_Modulo4bytes`,
   
    `kEDMA_Modulo8bytes`,
   
    `kEDMA_Modulo16bytes`,
   
    `kEDMA_Modulo32bytes`,
   
    `kEDMA_Modulo64bytes`,
   
    `kEDMA_Modulo128bytes`,
   
    `kEDMA_Modulo256bytes`,
   
    `kEDMA_Modulo512bytes`,
   
    `kEDMA_Modulo1Kbytes`,
   
    `kEDMA_Modulo2Kbytes`,
   
    `kEDMA_Modulo4Kbytes`,
   
    `kEDMA_Modulo8Kbytes`,
   
    `kEDMA_Modulo16Kbytes`,
   
    `kEDMA_Modulo32Kbytes`,
   
    `kEDMA_Modulo64Kbytes`,
   
    `kEDMA_Modulo128Kbytes`,
   
    `kEDMA_Modulo256Kbytes`,
   
    `kEDMA_Modulo512Kbytes`,
   
    `kEDMA_Modulo1Mbytes`,
   
    `kEDMA_Modulo2Mbytes`,
   
    `kEDMA_Modulo4Mbytes`,
   
    `kEDMA_Modulo8Mbytes`,
   
    `kEDMA_Modulo16Mbytes`,
   
    `kEDMA_Modulo32Mbytes`,
   
    `kEDMA_Modulo64Mbytes`,
   
    `kEDMA_Modulo128Mbytes`,
   
    `kEDMA_Modulo256Mbytes`,
   
    `kEDMA_Modulo512Mbytes`,
   
    `kEDMA_Modulo1Gbytes`,
   
    `kEDMA_Modulo2Gbytes` }

*eDMA modulo configuration*

- enum `edma_bandwidth_t` {

- ```

kEDMA_BandwidthStallNone = 0x0U,
kEDMA_BandwidthStall4Cycle = 0x2U,
kEDMA_BandwidthStall8Cycle = 0x3U }

Bandwidth control.
• enum edma_channel_link_type_t {
    kEDMA_LinkNone = 0x0U,
    kEDMA_MinorLink,
    kEDMA_MajorLink }

Channel link type.
• enum {
    kEDMA_DoneFlag = 0x1U,
    kEDMA_ErrorFlag = 0x2U,
    kEDMA_InterruptFlag = 0x4U }

_edma_channel_status_flags eDMA channel status flags.
• enum {
    kEDMA_DestinationBusErrorFlag = DMA_ES_DBE_MASK,
    kEDMA_SourceBusErrorFlag = DMA_ES_SBE_MASK,
    kEDMA_ScatterGatherErrorFlag = DMA_ES_SGE_MASK,
    kEDMA_NbytesErrorFlag = DMA_ES_NCE_MASK,
    kEDMA_DestinationOffsetErrorFlag = DMA_ES_DOE_MASK,
    kEDMA_DestinationAddressErrorFlag = DMA_ES_DAE_MASK,
    kEDMA_SourceOffsetErrorFlag = DMA_ES_SOE_MASK,
    kEDMA_SourceAddressErrorFlag = DMA_ES_SAE_MASK,
    kEDMA_ErrorChannelFlag = DMA_ES_ERRCHN_MASK,
    kEDMA_ChannelPriorityErrorFlag = DMA_ES_CPE_MASK,
    kEDMA_TransferCanceledFlag = DMA_ES_ECX_MASK,
    kEDMA_ValidFlag = (int)DMA_ES_VLD_MASK }

_edma_error_status_flags eDMA channel error status flags.
• enum edma_interrupt_enable_t {
    kEDMA_ErrorInterruptEnable = 0x1U,
    kEDMA_MajorInterruptEnable = DMA_CSR_INTMAJOR_MASK,
    kEDMA_HalfInterruptEnable = DMA_CSR_INTHALF_MASK }

eDMA interrupt source
• enum edma_transfer_type_t {
    kEDMA_MemoryToMemory = 0x0U,
    kEDMA_PeripheralToMemory,
    kEDMA_MemoryToPeripheral,
    kEDMA_PeripheralToPeripheral }

eDMA transfer type
• enum {
    kStatus_EDMA_QueueFull = MAKE_STATUS(kStatusGroup_EDMA, 0),
    kStatus_EDMA_Busy = MAKE_STATUS(kStatusGroup_EDMA, 1) }

_edma_transfer_status eDMA transfer status

```

## Driver version

- #define `FSL_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 4, 3)`)

*eDMA driver version*

## eDMA initialization and de-initialization

- void [EDMA\\_Init](#) (DMA\_Type \*base, const [edma\\_config\\_t](#) \*config)  
*Initializes the eDMA peripheral.*
- void [EDMA\\_Deinit](#) (DMA\_Type \*base)  
*Deinitializes the eDMA peripheral.*
- void [EDMA\\_InstallTCD](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_tcd\\_t](#) \*tcd)  
*Push content of TCD structure into hardware TCD register.*
- void [EDMA\\_GetDefaultConfig](#) ([edma\\_config\\_t](#) \*config)  
*Gets the eDMA default configuration structure.*
- static void [EDMA\\_EnableContinuousChannelLinkMode](#) (DMA\_Type \*base, bool enable)  
*Enable/Disable continuous channel link mode.*
- static void [EDMA\\_EnableMinorLoopMapping](#) (DMA\_Type \*base, bool enable)  
*Enable/Disable minor loop mapping.*

## eDMA Channel Operation

- void [EDMA\\_ResetChannel](#) (DMA\_Type \*base, uint32\_t channel)  
*Sets all TCD registers to default values.*
- void [EDMA\\_SetTransferConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_transfer\\_config\\_t](#) \*config, [edma\\_tcd\\_t](#) \*nextTcd)  
*Configures the eDMA transfer attribute.*
- void [EDMA\\_SetMinorOffsetConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_minor\\_offset\\_config\\_t](#) \*config)  
*Configures the eDMA minor offset feature.*
- void [EDMA\\_SetChannelPreemptionConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_channel\\_Preemption\\_config\\_t](#) \*config)  
*Configures the eDMA channel preemption feature.*
- void [EDMA\\_SetChannelLink](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_channel\\_link\\_type\\_t](#) linkType, uint32\_t linkedChannel)  
*Sets the channel link for the eDMA transfer.*
- void [EDMA\\_SetBandWidth](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_bandwidth\\_t](#) bandWidth)  
*Sets the bandwidth for the eDMA transfer.*
- void [EDMA\\_SetModulo](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_modulo\\_t](#) srcModulo, [edma\\_modulo\\_t](#) destModulo)  
*Sets the source modulo and the destination modulo for the eDMA transfer.*
- static void [EDMA\\_EnableAsyncRequest](#) (DMA\_Type \*base, uint32\_t channel, bool enable)  
*Enables an async request for the eDMA transfer.*
- static void [EDMA\\_EnableAutoStopRequest](#) (DMA\_Type \*base, uint32\_t channel, bool enable)  
*Enables an auto stop request for the eDMA transfer.*
- void [EDMA\\_EnableChannelInterrupts](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Enables the interrupt source for the eDMA transfer.*
- void [EDMA\\_DisableChannelInterrupts](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Disables the interrupt source for the eDMA transfer.*
- void [EDMA\\_SetMajorOffsetConfig](#) (DMA\_Type \*base, uint32\_t channel, int32\_t sourceOffset, int32\_t destOffset)  
*Configures the eDMA channel TCD major offset feature.*

## eDMA TCD Operation

- void [EDMA\\_TcdReset](#) (edma\_tcd\_t \*tcd)  
*Sets all fields to default values for the TCD structure.*
- void [EDMA\\_TcdSetTransferConfig](#) (edma\_tcd\_t \*tcd, const edma\_transfer\_config\_t \*config, edma\_tcd\_t \*nextTcd)  
*Configures the eDMA TCD transfer attribute.*
- void [EDMA\\_TcdSetMinorOffsetConfig](#) (edma\_tcd\_t \*tcd, const edma\_minor\_offset\_config\_t \*config)  
*Configures the eDMA TCD minor offset feature.*
- void [EDMA\\_TcdSetChannelLink](#) (edma\_tcd\_t \*tcd, edma\_channel\_link\_type\_t linkType, uint32\_t linkedChannel)  
*Sets the channel link for the eDMA TCD.*
- static void [EDMA\\_TcdSetBandWidth](#) (edma\_tcd\_t \*tcd, edma\_bandwidth\_t bandWidth)  
*Sets the bandwidth for the eDMA TCD.*
- void [EDMA\\_TcdSetModulo](#) (edma\_tcd\_t \*tcd, edma\_modulo\_t srcModulo, edma\_modulo\_t destModulo)  
*Sets the source modulo and the destination modulo for the eDMA TCD.*
- static void [EDMA\\_TcdEnableAutoStopRequest](#) (edma\_tcd\_t \*tcd, bool enable)  
*Sets the auto stop request for the eDMA TCD.*
- void [EDMA\\_TcdEnableInterrupts](#) (edma\_tcd\_t \*tcd, uint32\_t mask)  
*Enables the interrupt source for the eDMA TCD.*
- void [EDMA\\_TcdDisableInterrupts](#) (edma\_tcd\_t \*tcd, uint32\_t mask)  
*Disables the interrupt source for the eDMA TCD.*
- void [EDMA\\_TcdSetMajorOffsetConfig](#) (edma\_tcd\_t \*tcd, int32\_t sourceOffset, int32\_t destOffset)  
*Configures the eDMA TCD major offset feature.*

## eDMA Channel Transfer Operation

- static void [EDMA\\_EnableChannelRequest](#) (DMA\_Type \*base, uint32\_t channel)  
*Enables the eDMA hardware channel request.*
- static void [EDMA\\_DisableChannelRequest](#) (DMA\_Type \*base, uint32\_t channel)  
*Disables the eDMA hardware channel request.*
- static void [EDMA\\_TriggerChannelStart](#) (DMA\_Type \*base, uint32\_t channel)  
*Starts the eDMA transfer by using the software trigger.*

## eDMA Channel Status Operation

- uint32\_t [EDMA\\_GetRemainingMajorLoopCount](#) (DMA\_Type \*base, uint32\_t channel)  
*Gets the remaining major loop count from the eDMA current channel TCD.*
- static uint32\_t [EDMA\\_GetErrorStatusFlags](#) (DMA\_Type \*base)  
*Gets the eDMA channel error status flags.*
- uint32\_t [EDMA\\_GetChannelStatusFlags](#) (DMA\_Type \*base, uint32\_t channel)  
*Gets the eDMA channel status flags.*
- void [EDMA\\_ClearChannelStatusFlags](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Clears the eDMA channel status flags.*

## eDMA Transactional Operation

- void [EDMA\\_CreateHandle](#) (edma\_handle\_t \*handle, DMA\_Type \*base, uint32\_t channel)  
*Creates the eDMA handle.*

- void **EDMA\_InstallTCDMemory** (**edma\_handle\_t** \*handle, **edma\_tcd\_t** \*tcdPool, **uint32\_t** tcdSize)  
*Installs the TCDs memory pool into the eDMA handle.*
- void **EDMA\_SetCallback** (**edma\_handle\_t** \*handle, **edma\_callback** callback, void \*userData)  
*Installs a callback function for the eDMA transfer.*
- void **EDMA\_PreparesTransferConfig** (**edma\_transfer\_config\_t** \*config, void \*srcAddr, **uint32\_t** srcWidth, **int16\_t** srcOffset, void \*destAddr, **uint32\_t** destWidth, **int16\_t** destOffset, **uint32\_t** bytesEachRequest, **uint32\_t** transferBytes)  
*Prepares the eDMA transfer structure configurations.*
- void **EDMA\_PreparesTransfer** (**edma\_transfer\_config\_t** \*config, void \*srcAddr, **uint32\_t** srcWidth, void \*destAddr, **uint32\_t** destWidth, **uint32\_t** bytesEachRequest, **uint32\_t** transferBytes, **edma\_transfer\_type\_t** transferType)  
*Prepares the eDMA transfer structure.*
- **status\_t EDMA\_SubmitTransfer** (**edma\_handle\_t** \*handle, const **edma\_transfer\_config\_t** \*config)  
*Submits the eDMA transfer request.*
- void **EDMA\_StartTransfer** (**edma\_handle\_t** \*handle)  
*eDMA starts transfer.*
- void **EDMA\_StopTransfer** (**edma\_handle\_t** \*handle)  
*eDMA stops transfer.*
- void **EDMA\_AbortTransfer** (**edma\_handle\_t** \*handle)  
*eDMA aborts transfer.*
- static **uint32\_t EDMA\_GetUnusedTCDNumber** (**edma\_handle\_t** \*handle)  
*Get unused TCD slot number.*
- static **uint32\_t EDMA\_GetNextTCDAddress** (**edma\_handle\_t** \*handle)  
*Get the next tcd address.*
- void **EDMA\_HandleIRQ** (**edma\_handle\_t** \*handle)  
*eDMA IRQ handler for the current major loop transfer completion.*

## 18.3 Data Structure Documentation

### 18.3.1 struct edma\_config\_t

#### Data Fields

- bool **enableContinuousLinkMode**  
*Enable (true) continuous link mode.*
- bool **enableHaltOnError**  
*Enable (true) transfer halt on error.*
- bool **enableRoundRobinArbitration**  
*Enable (true) round robin channel arbitration method or fixed priority arbitration is used for channel selection.*
- bool **enableDebugMode**  
*Enable(true) eDMA debug mode.*

#### Field Documentation

##### (1) bool **edma\_config\_t::enableContinuousLinkMode**

Upon minor loop completion, the channel activates again if that channel has a minor loop channel link enabled and the link channel is itself.

**(2) bool edma\_config\_t::enableHaltOnError**

Any error causes the HALT bit to set. Subsequently, all service requests are ignored until the HALT bit is cleared.

**(3) bool edma\_config\_t::enableDebugMode**

When in debug mode, the eDMA stalls the start of a new channel. Executing channels are allowed to complete.

**18.3.2 struct edma\_transfer\_config\_t**

This structure configures the source/destination transfer attribute.

**Data Fields**

- uint32\_t **srcAddr**  
*Source data address.*
- uint32\_t **destAddr**  
*Destination data address.*
- **edma\_transfer\_size\_t srcTransferSize**  
*Source data transfer size.*
- **edma\_transfer\_size\_t destTransferSize**  
*Destination data transfer size.*
- int16\_t **srcOffset**  
*Sign-extended offset applied to the current source address to form the next-state value as each source read is completed.*
- int16\_t **destOffset**  
*Sign-extended offset applied to the current destination address to form the next-state value as each destination write is completed.*
- uint32\_t **minorLoopBytes**  
*Bytes to transfer in a minor loop.*
- uint32\_t **majorLoopCounts**  
*Major loop iteration count.*

**Field Documentation**

- (1) `uint32_t edma_transfer_config_t::srcAddr`
- (2) `uint32_t edma_transfer_config_t::destAddr`
- (3) `edma_transfer_size_t edma_transfer_config_t::srcTransferSize`
- (4) `edma_transfer_size_t edma_transfer_config_t::destTransferSize`
- (5) `int16_t edma_transfer_config_t::srcOffset`
- (6) `int16_t edma_transfer_config_t::destOffset`
- (7) `uint32_t edma_transfer_config_t::majorLoopCounts`

**18.3.3 struct edma\_channel\_Preemption\_config\_t****Data Fields**

- `bool enableChannelPreemption`  
*If true: a channel can be suspended by other channel with higher priority.*
- `bool enablePreemptAbility`  
*If true: a channel can suspend other channel with low priority.*
- `uint8_t channelPriority`  
*Channel priority.*

**18.3.4 struct edma\_minor\_offset\_config\_t****Data Fields**

- `bool enableSrcMinorOffset`  
*Enable(true) or Disable(false) source minor loop offset.*
- `bool enableDestMinorOffset`  
*Enable(true) or Disable(false) destination minor loop offset.*
- `uint32_t minorOffset`  
*Offset for a minor loop mapping.*

**Field Documentation**

- (1) **bool edma\_minor\_offset\_config\_t::enableSrcMinorOffset**
- (2) **bool edma\_minor\_offset\_config\_t::enableDestMinorOffset**
- (3) **uint32\_t edma\_minor\_offset\_config\_t::minorOffset**

**18.3.5 struct edma\_tcd\_t**

This structure is same as TCD register which is described in reference manual, and is used to configure the scatter/gather feature as a next hardware TCD.

**Data Fields**

- **\_IO uint32\_t SADDR**  
*SADDR register, used to save source address.*
- **\_IO uint16\_t SOFF**  
*SOFF register, save offset bytes every transfer.*
- **\_IO uint16\_t ATTR**  
*ATTR register, source/destination transfer size and modulo.*
- **\_IO uint32\_t NBYTES**  
*Nbytes register, minor loop length in bytes.*
- **\_IO uint32\_t SLAST**  
*SLAST register.*
- **\_IO uint32\_t DADDR**  
*DADDR register, used for destination address.*
- **\_IO uint16\_t DOFF**  
*DOFF register, used for destination offset.*
- **\_IO uint16\_t CITER**  
*CITER register, current minor loop numbers, for unfinished minor loop.*
- **\_IO uint32\_t DLAST\_SGA**  
*DLASTSGA register, next tcd address used in scatter-gather mode.*
- **\_IO uint16\_t CSR**  
*CSR register, for TCD control status.*
- **\_IO uint16\_t BITER**  
*BITER register, begin minor loop count.*

**Field Documentation**

- (1) `__IO uint16_t edma_tcd_t::CITER`
- (2) `__IO uint16_t edma_tcd_t::BITER`

**18.3.6 struct edma\_handle\_t****Data Fields**

- `edma_callback callback`  
*Callback function for major count exhausted.*
- `void * userData`  
*Callback function parameter.*
- `DMA_Type * base`  
*eDMA peripheral base address.*
- `edma_tcd_t * tcdPool`  
*Pointer to memory stored TCDs.*
- `uint8_t channel`  
*eDMA channel number.*
- `volatile int8_t header`  
*The first TCD index.*
- `volatile int8_t tail`  
*The last TCD index.*
- `volatile int8_t tcdUsed`  
*The number of used TCD slots.*
- `volatile int8_t tcdSize`  
*The total number of TCD slots in the queue.*
- `uint8_t flags`  
*The status of the current channel.*

**Field Documentation**

- (1) `edma_callback edma_handle_t::callback`
- (2) `void* edma_handle_t::userData`
- (3) `DMA_Type* edma_handle_t::base`
- (4) `edma_tcd_t* edma_handle_t::tcdPool`
- (5) `uint8_t edma_handle_t::channel`
- (6) `volatile int8_t edma_handle_t::header`

Should point to the next TCD to be loaded into the eDMA engine.

- (7) `volatile int8_t edma_handle_t::tail`

Should point to the next TCD to be stored into the memory pool.

(8) **volatile int8\_t edma\_handle\_t::tcdUsed**

Should reflect the number of TCDs can be used/loaded in the memory.

(9) **volatile int8\_t edma\_handle\_t::tcdSize**(10) **uint8\_t edma\_handle\_t::flags****18.4 Macro Definition Documentation****18.4.1 #define FSL\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 4, 3))**

Version 2.4.3.

**18.5 Typedef Documentation****18.5.1 typedef void(\* edma\_callback)(struct \_edma\_handle \*handle, void \*userData, bool transferDone, uint32\_t tclds)**

This callback function is called in the EDMA interrupt handle. In normal mode, run into callback function means the transfer users need is done. In scatter gather mode, run into callback function means a transfer control block (tcd) is finished. Not all transfer finished, users can get the finished tcd numbers using interface EDMA\_GetUnusedTCDNumber.

Parameters

<i>handle</i>	EDMA handle pointer, users shall not touch the values inside.
<i>userData</i>	The callback user parameter pointer. Users can use this parameter to involve things users need to change in EDMA callback function.
<i>transferDone</i>	If the current loaded transfer done. In normal mode it means if all transfer done. In scatter gather mode, this parameter shows is the current transfer block in EDM-A register is done. As the load of core is different, it will be different if the new tcd loaded into EDMA registers while this callback called. If true, it always means new tcd still not loaded into registers, while false means new tcd already loaded into registers.

<i>tcds</i>	How many tcds are done from the last callback. This parameter only used in scatter gather mode. It tells user how many tcds are finished between the last callback and this.
-------------	--

## 18.6 Enumeration Type Documentation

### 18.6.1 enum edma\_transfer\_size\_t

Enumerator

- kEDMA\_TransferSize1Bytes* Source/Destination data transfer size is 1 byte every time.
- kEDMA\_TransferSize2Bytes* Source/Destination data transfer size is 2 bytes every time.
- kEDMA\_TransferSize4Bytes* Source/Destination data transfer size is 4 bytes every time.
- kEDMA\_TransferSize8Bytes* Source/Destination data transfer size is 8 bytes every time.
- kEDMA\_TransferSize16Bytes* Source/Destination data transfer size is 16 bytes every time.
- kEDMA\_TransferSize32Bytes* Source/Destination data transfer size is 32 bytes every time.

### 18.6.2 enum edma\_modulo\_t

Enumerator

- kEDMA\_ModuloDisable* Disable modulo.
- kEDMA\_Modulo2bytes* Circular buffer size is 2 bytes.
- kEDMA\_Modulo4bytes* Circular buffer size is 4 bytes.
- kEDMA\_Modulo8bytes* Circular buffer size is 8 bytes.
- kEDMA\_Modulo16bytes* Circular buffer size is 16 bytes.
- kEDMA\_Modulo32bytes* Circular buffer size is 32 bytes.
- kEDMA\_Modulo64bytes* Circular buffer size is 64 bytes.
- kEDMA\_Modulo128bytes* Circular buffer size is 128 bytes.
- kEDMA\_Modulo256bytes* Circular buffer size is 256 bytes.
- kEDMA\_Modulo512bytes* Circular buffer size is 512 bytes.
- kEDMA\_Modulo1Kbytes* Circular buffer size is 1 K bytes.
- kEDMA\_Modulo2Kbytes* Circular buffer size is 2 K bytes.
- kEDMA\_Modulo4Kbytes* Circular buffer size is 4 K bytes.
- kEDMA\_Modulo8Kbytes* Circular buffer size is 8 K bytes.
- kEDMA\_Modulo16Kbytes* Circular buffer size is 16 K bytes.
- kEDMA\_Modulo32Kbytes* Circular buffer size is 32 K bytes.
- kEDMA\_Modulo64Kbytes* Circular buffer size is 64 K bytes.
- kEDMA\_Modulo128Kbytes* Circular buffer size is 128 K bytes.
- kEDMA\_Modulo256Kbytes* Circular buffer size is 256 K bytes.
- kEDMA\_Modulo512Kbytes* Circular buffer size is 512 K bytes.
- kEDMA\_Modulo1Mbytes* Circular buffer size is 1 M bytes.
- kEDMA\_Modulo2Mbytes* Circular buffer size is 2 M bytes.
- kEDMA\_Modulo4Mbytes* Circular buffer size is 4 M bytes.

*kEDMA\_Modulo8Mbytes* Circular buffer size is 8 M bytes.  
*kEDMA\_Modulo16Mbytes* Circular buffer size is 16 M bytes.  
*kEDMA\_Modulo32Mbytes* Circular buffer size is 32 M bytes.  
*kEDMA\_Modulo64Mbytes* Circular buffer size is 64 M bytes.  
*kEDMA\_Modulo128Mbytes* Circular buffer size is 128 M bytes.  
*kEDMA\_Modulo256Mbytes* Circular buffer size is 256 M bytes.  
*kEDMA\_Modulo512Mbytes* Circular buffer size is 512 M bytes.  
*kEDMA\_Modulo1Gbytes* Circular buffer size is 1 G bytes.  
*kEDMA\_Modulo2Gbytes* Circular buffer size is 2 G bytes.

### 18.6.3 enum edma\_bandwidth\_t

Enumerator

*kEDMA\_BandwidthStallNone* No eDMA engine stalls.  
*kEDMA\_BandwidthStall4Cycle* eDMA engine stalls for 4 cycles after each read/write.  
*kEDMA\_BandwidthStall8Cycle* eDMA engine stalls for 8 cycles after each read/write.

### 18.6.4 enum edma\_channel\_link\_type\_t

Enumerator

*kEDMA\_LinkNone* No channel link.  
*kEDMA\_MinorLink* Channel link after each minor loop.  
*kEDMA\_MajorLink* Channel link while major loop count exhausted.

### 18.6.5 anonymous enum

Enumerator

*kEDMA\_DoneFlag* DONE flag, set while transfer finished, CITER value exhausted.  
*kEDMA\_ErrorFlag* eDMA error flag, an error occurred in a transfer  
*kEDMA\_InterruptFlag* eDMA interrupt flag, set while an interrupt occurred of this channel

### 18.6.6 anonymous enum

Enumerator

*kEDMA\_DestinationBusErrorFlag* Bus error on destination address.  
*kEDMA\_SourceBusErrorFlag* Bus error on the source address.  
*kEDMA\_ScatterGatherErrorFlag* Error on the Scatter/Gather address, not 32byte aligned.  
*kEDMA\_NbytesErrorFlag* NBYTES/CITER configuration error.

*kEDMA\_DestinationOffsetErrorFlag* Destination offset not aligned with destination size.  
*kEDMA\_DestinationAddressErrorFlag* Destination address not aligned with destination size.  
*kEDMA\_SourceOffsetErrorFlag* Source offset not aligned with source size.  
*kEDMA\_SourceAddressErrorFlag* Source address not aligned with source size.  
*kEDMA\_ErrorChannelFlag* Error channel number of the cancelled channel number.  
*kEDMA\_ChannelPriorityErrorFlag* Channel priority is not unique.  
*kEDMA\_TransferCanceledFlag* Transfer cancelled.  
*kEDMA\_ValidFlag* No error occurred, this bit is 0. Otherwise, it is 1.

### 18.6.7 enum edma\_interrupt\_enable\_t

Enumerator

*kEDMA\_ErrorInterruptEnable* Enable interrupt while channel error occurs.  
*kEDMA\_MajorInterruptEnable* Enable interrupt while major count exhausted.  
*kEDMA\_HalfInterruptEnable* Enable interrupt while major count to half value.

### 18.6.8 enum edma\_transfer\_type\_t

Enumerator

*kEDMA\_MemoryToMemory* Transfer from memory to memory.  
*kEDMA\_PeripheralToMemory* Transfer from peripheral to memory.  
*kEDMA\_MemoryToPeripheral* Transfer from memory to peripheral.  
*kEDMA\_PeripheralToPeripheral* Transfer from Peripheral to peripheral.

### 18.6.9 anonymous enum

Enumerator

*kStatus\_EDMA\_QueueFull* TCD queue is full.  
*kStatus\_EDMA\_Busy* Channel is busy and can't handle the transfer request.

## 18.7 Function Documentation

### 18.7.1 void EDMA\_Init ( DMA\_Type \* *base*, const edma\_config\_t \* *config* )

This function ungates the eDMA clock and configures the eDMA peripheral according to the configuration structure.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>config</i>	A pointer to the configuration structure, see "edma_config_t".

Note

This function enables the minor loop map feature.

### 18.7.2 void EDMA\_Deinit ( DMA\_Type \* *base* )

This function gates the eDMA clock.

Parameters

<i>base</i>	eDMA peripheral base address.
-------------	-------------------------------

### 18.7.3 void EDMA\_InstallTCD ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_tcd\_t \* *tcd* )

Parameters

<i>base</i>	EDMA peripheral base address.
<i>channel</i>	EDMA channel number.
<i>tcd</i>	Point to TCD structure.

### 18.7.4 void EDMA\_GetDefaultConfig ( edma\_config\_t \* *config* )

This function sets the configuration structure to default values. The default configuration is set to the following values.

```
* config.enableContinuousLinkMode = false;
* config.enableHaltOnError = true;
* config.enableRoundRobinArbitration = false;
* config.enableDebugMode = false;
*
```

Parameters

<i>config</i>	A pointer to the eDMA configuration structure.
---------------	--

### 18.7.5 static void EDMA\_EnableContinuousChannelLinkMode ( DMA\_Type \* *base*, bool *enable* ) [inline], [static]

Note

Do not use continuous link mode with a channel linking to itself if there is only one minor loop iteration per service request, for example, if the channel's NBYTES value is the same as either the source or destination size. The same data transfer profile can be achieved by simply increasing the NBYTES value, which provides more efficient, faster processing.

Parameters

<i>base</i>	EDMA peripheral base address.
<i>enable</i>	true is enable, false is disable.

### 18.7.6 static void EDMA\_EnableMinorLoopMapping ( DMA\_Type \* *base*, bool *enable* ) [inline], [static]

The TCDn.word2 is redefined to include individual enable fields, an offset field, and the NBYTES field.

Parameters

<i>base</i>	EDMA peripheral base address.
<i>enable</i>	true is enable, false is disable.

### 18.7.7 void EDMA\_ResetChannel ( DMA\_Type \* *base*, uint32\_t *channel* )

This function sets TCD registers for this channel to default values.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

## Note

This function must not be called while the channel transfer is ongoing or it causes unpredictable results.

This function enables the auto stop request feature.

### 18.7.8 void EDMA\_SetTransferConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_transfer\_config\_t \* *config*, edma\_tcd\_t \* *nextTcd* )

This function configures the transfer attribute, including source address, destination address, transfer size, address offset, and so on. It also configures the scatter gather feature if the user supplies the TCD address. Example:

```
* edma_transfer_t config;
* edma_tcd_t tcd;
* config.srcAddr = ...;
* config.destAddr = ...;
* ...
* EDMA_SetTransferConfig(DMA0, channel, &config, &tcd);
*
```

## Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>config</i>	Pointer to eDMA transfer configuration structure.
<i>nextTcd</i>	Point to TCD structure. It can be NULL if users do not want to enable scatter/gather feature.

## Note

If nextTcd is not NULL, it means scatter gather feature is enabled and DREQ bit is cleared in the previous transfer configuration, which is set in the eDMA\_ResetChannel.

### 18.7.9 void EDMA\_SetMinorOffsetConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_minor\_offset\_config\_t \* *config* )

The minor offset means that the signed-extended value is added to the source address or destination address after each minor loop.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>config</i>	A pointer to the minor offset configuration structure.

### **18.7.10 void EDMA\_SetChannelPreemptionConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_channel\_Preemption\_config\_t \* *config* )**

This function configures the channel preemption attribute and the priority of the channel.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number
<i>config</i>	A pointer to the channel preemption configuration structure.

### **18.7.11 void EDMA\_SetChannelLink ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_channel\_link\_type\_t *linkType*, uint32\_t *linkedChannel* )**

This function configures either the minor link or the major link mode. The minor link means that the channel link is triggered every time CITER decreases by 1. The major link means that the channel link is triggered when the CITER is exhausted.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>linkType</i>	A channel link type, which can be one of the following: <ul style="list-style-type: none"> <li>• kEDMA_LinkNone</li> <li>• kEDMA_MinorLink</li> <li>• kEDMA_MajorLink</li> </ul>

<i>linkedChannel</i>	The linked channel number.
----------------------	----------------------------

## Note

Users should ensure that DONE flag is cleared before calling this interface, or the configuration is invalid.

### 18.7.12 void EDMA\_SetBandWidth ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_bandwidth\_t *bandWidth* )

Because the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. The bandwidth forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch.

## Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>bandWidth</i>	A bandwidth setting, which can be one of the following: <ul style="list-style-type: none"> <li>• kEDMABandwidthStallNone</li> <li>• kEDMABandwidthStall4Cycle</li> <li>• kEDMABandwidthStall8Cycle</li> </ul>

### 18.7.13 void EDMA\_SetModulo ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_modulo\_t *srcModulo*, edma\_modulo\_t *destModulo* )

This function defines a specific address range specified to be the value after (SADDR + SOFF)/(DADDR + DOFF) calculation is performed or the original register value. It provides the ability to implement a circular data queue easily.

## Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

<i>srcModulo</i>	A source modulo value.
<i>destModulo</i>	A destination modulo value.

**18.7.14 static void EDMA\_EnableAsyncRequest ( DMA\_Type \* *base*, uint32\_t *channel*, bool *enable* ) [inline], [static]**

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>enable</i>	The command to enable (true) or disable (false).

**18.7.15 static void EDMA\_EnableAutoStopRequest ( DMA\_Type \* *base*, uint32\_t *channel*, bool *enable* ) [inline], [static]**

If enabling the auto stop request, the eDMA hardware automatically disables the hardware channel request.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>enable</i>	The command to enable (true) or disable (false).

**18.7.16 void EDMA\_EnableChannelInterrupts ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )**

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>mask</i>	The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type.

**18.7.17 void EDMA\_DisableChannelInterrupts ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )**

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>mask</i>	The mask of the interrupt source to be set. Use the defined edma_interrupt_enable_t type.

### 18.7.18 void EDMA\_SetMajorOffsetConfig ( DMA\_Type \* *base*, uint32\_t *channel*, int32\_t *sourceOffset*, int32\_t *destOffset* )

Adjustment value added to the source address at the completion of the major iteration count

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	edma channel number.
<i>sourceOffset</i>	source address offset will be applied to source address after major loop done.
<i>destOffset</i>	destination address offset will be applied to source address after major loop done.

### 18.7.19 void EDMA\_TcdReset ( edma\_tcd\_t \* *tcd* )

This function sets all fields for this TCD structure to default value.

Parameters

<i>tcd</i>	Pointer to the TCD structure.
------------	-------------------------------

Note

This function enables the auto stop request feature.

### 18.7.20 void EDMA\_TcdSetTransferConfig ( edma\_tcd\_t \* *tcd*, const edma\_transfer\_config\_t \* *config*, edma\_tcd\_t \* *nextTcd* )

The TCD is a transfer control descriptor. The content of the TCD is the same as the hardware TCD registers. The TCD is used in the scatter-gather mode. This function configures the TCD transfer attribute, including source address, destination address, transfer size, address offset, and so on. It also configures the scatter gather feature if the user supplies the next TCD address. Example:

```

*   edma_transfer_t config = {
*   ...
*   }
*   edma_tcd_t tcd __aligned(32);
*   edma_tcd_t nextTcd __aligned(32);
*   EDMA_TcdSetTransferConfig(&tcd, &config, &nextTcd);
*

```

## Parameters

<i>tcd</i>	Pointer to the TCD structure.
<i>config</i>	Pointer to eDMA transfer configuration structure.
<i>nextTcd</i>	Pointer to the next TCD structure. It can be NULL if users do not want to enable scatter/gather feature.

## Note

TCD address should be 32 bytes aligned or it causes an eDMA error.

If the nextTcd is not NULL, the scatter gather feature is enabled and DREQ bit is cleared in the previous transfer configuration, which is set in the EDMA\_TcdReset.

### 18.7.21 void EDMA\_TcdSetMinorOffsetConfig ( *edma\_tcd\_t \* tcd, const edma\_minor\_offset\_config\_t \* config* )

A minor offset is a signed-extended value added to the source address or a destination address after each minor loop.

## Parameters

<i>tcd</i>	A point to the TCD structure.
<i>config</i>	A pointer to the minor offset configuration structure.

### 18.7.22 void EDMA\_TcdSetChannelLink ( *edma\_tcd\_t \* tcd, edma\_channel\_link\_type\_t linkType, uint32\_t linkedChannel* )

This function configures either a minor link or a major link. The minor link means the channel link is triggered every time CITER decreases by 1. The major link means that the channel link is triggered when the CITER is exhausted.

## Note

Users should ensure that DONE flag is cleared before calling this interface, or the configuration is invalid.

Parameters

<i>tcd</i>	Point to the TCD structure.
<i>linkType</i>	Channel link type, it can be one of: <ul style="list-style-type: none"> <li>• kEDMA_LinkNone</li> <li>• kEDMA_MinorLink</li> <li>• kEDMA_MajorLink</li> </ul>
<i>linkedChannel</i>	The linked channel number.

### 18.7.23 static void EDMA\_TcdSetBandWidth ( *edma\_tcd\_t \* tcd*, *edma\_bandwidth\_t bandwidth* ) [inline], [static]

Because the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. The bandwidth forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch.

Parameters

<i>tcd</i>	A pointer to the TCD structure.
<i>bandWidth</i>	A bandwidth setting, which can be one of the following: <ul style="list-style-type: none"> <li>• kEDMABandwidthStallNone</li> <li>• kEDMABandwidthStall4Cycle</li> <li>• kEDMABandwidthStall8Cycle</li> </ul>

### 18.7.24 void EDMA\_TcdSetModulo ( *edma\_tcd\_t \* tcd*, *edma\_modulo\_t srcModulo*, *edma\_modulo\_t destModulo* )

This function defines a specific address range specified to be the value after (SADDR + SOFF)/(DADDR + DOFF) calculation is performed or the original register value. It provides the ability to implement a circular data queue easily.

Parameters

<i>tcd</i>	A pointer to the TCD structure.
------------	---------------------------------

<i>srcModulo</i>	A source modulo value.
<i>destModulo</i>	A destination modulo value.

### 18.7.25 static void EDMA\_TcdEnableAutoStopRequest ( *edma\_tcd\_t \* tcd, bool enable* ) [inline], [static]

If enabling the auto stop request, the eDMA hardware automatically disables the hardware channel request.

Parameters

<i>tcd</i>	A pointer to the TCD structure.
<i>enable</i>	The command to enable (true) or disable (false).

### 18.7.26 void EDMA\_TcdEnableInterrupts ( *edma\_tcd\_t \* tcd, uint32\_t mask* )

Parameters

<i>tcd</i>	Point to the TCD structure.
<i>mask</i>	The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type.

### 18.7.27 void EDMA\_TcdDisableInterrupts ( *edma\_tcd\_t \* tcd, uint32\_t mask* )

Parameters

<i>tcd</i>	Point to the TCD structure.
<i>mask</i>	The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type.

### 18.7.28 void EDMA\_TcdSetMajorOffsetConfig ( *edma\_tcd\_t \* tcd, int32\_t sourceOffset, int32\_t destOffset* )

Adjustment value added to the source address at the completion of the major iteration count

Parameters

<i>tcd</i>	A point to the TCD structure.
<i>sourceOffset</i>	source address offset will be applied to source address after major loop done.
<i>destOffset</i>	destination address offset will be applied to source address after major loop done.

### **18.7.29 static void EDMA\_EnableChannelRequest ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function enables the hardware channel request.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

### **18.7.30 static void EDMA\_DisableChannelRequest ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function disables the hardware channel request.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

### **18.7.31 static void EDMA\_TriggerChannelStart ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function starts a minor loop transfer.

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

### 18.7.32 **uint32\_t EDMA\_GetRemainingMajorLoopCount ( DMA\_Type \* *base*,                   uint32\_t *channel* )**

This function checks the TCD (Task Control Descriptor) status for a specified eDMA channel and returns the number of major loop count that has not finished.

## Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

## Returns

Major loop count which has not been transferred yet for the current TCD.

## Note

1. This function can only be used to get unfinished major loop count of transfer without the next TCD, or it might be inaccuracy.
  1. The unfinished/remaining transfer bytes cannot be obtained directly from registers while the channel is running. Because to calculate the remaining bytes, the initial NBYTES configured in DMA\_TCDn\_NBYTES\_MLNO register is needed while the eDMA IP does not support getting it while a channel is active. In another word, the NBYTES value reading is always the actual (decrementing) NBYTES value the dma\_engine is working with while a channel is running. Consequently, to get the remaining transfer bytes, a software-saved initial value of NBYTES (for example copied before enabling the channel) is needed. The formula to calculate it is shown below: RemainingBytes = RemainingMajorLoopCount \* NBYTE-S(initially configured)

### 18.7.33 static uint32\_t EDMA\_GetErrorStatusFlags ( DMA\_Type \* *base* ) [inline], [static]

## Parameters

<i>base</i>	eDMA peripheral base address.
-------------	-------------------------------

## Returns

The mask of error status flags. Users need to use the \_edma\_error\_status\_flags type to decode the return variables.

### 18.7.34 uint32\_t EDMA\_GetChannelStatusFlags ( DMA\_Type \* *base*, uint32\_t *channel* )

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

Returns

The mask of channel status flags. Users need to use the `_edma_channel_status_flags` type to decode the return variables.

### 18.7.35 void EDMA\_ClearChannelStatusFlags ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )

Parameters

<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.
<i>mask</i>	The mask of channel status to be cleared. Users need to use the defined <code>_edma_channel_status_flags</code> type.

### 18.7.36 void EDMA\_CreateHandle ( edma\_handle\_t \* *handle*, DMA\_Type \* *base*, uint32\_t *channel* )

This function is called if using the transactional API for eDMA. This function initializes the internal state of the eDMA handle.

Parameters

<i>handle</i>	eDMA handle pointer. The eDMA handle stores callback function and parameters.
<i>base</i>	eDMA peripheral base address.
<i>channel</i>	eDMA channel number.

### 18.7.37 void EDMA\_InstallTCDMemory ( edma\_handle\_t \* *handle*, edma\_tcd\_t \* *tcdPool*, uint32\_t *tcdSize* )

This function is called after the EDMA\_CreateHandle to use scatter/gather feature. This function shall only be used while users need to use scatter gather mode. Scatter gather mode enables EDMA to load a new transfer control block (tcd) in hardware, and automatically reconfigure that DMA channel for a

new transfer. Users need to prepare tcd memory and also configure tcds using interface EDMA\_SubmitTransfer.

Parameters

<i>handle</i>	eDMA handle pointer.
<i>tcdPool</i>	A memory pool to store TCDs. It must be 32 bytes aligned.
<i>tcdSize</i>	The number of TCD slots.

### 18.7.38 void EDMA\_SetCallback ( *edma\_handle\_t \* handle, edma\_callback callback, void \* userData* )

This callback is called in the eDMA IRQ handler. Use the callback to do something after the current major loop transfer completes. This function will be called every time one tcd finished transfer.

Parameters

<i>handle</i>	eDMA handle pointer.
<i>callback</i>	eDMA callback function pointer.
<i>userData</i>	A parameter for the callback function.

### 18.7.39 void EDMA\_PrepTransferConfig ( *edma\_transfer\_config\_t \* config, void \* srcAddr, uint32\_t srcWidth, int16\_t srcOffset, void \* destAddr, uint32\_t destWidth, int16\_t destOffset, uint32\_t bytesEachRequest, uint32\_t transferBytes* )

This function prepares the transfer configuration structure according to the user input.

Parameters

<i>config</i>	The user configuration structure of type <i>edma_transfer_t</i> .
<i>srcAddr</i>	eDMA transfer source address.
<i>srcWidth</i>	eDMA transfer source address width(bytes).
<i>srcOffset</i>	source address offset.
<i>destAddr</i>	eDMA transfer destination address.
<i>destWidth</i>	eDMA transfer destination address width(bytes).
<i>destOffset</i>	destination address offset.
<i>bytesEachRequest</i>	eDMA transfer bytes per channel request.
<i>transferBytes</i>	eDMA transfer bytes to be transferred.

## Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error (SAE).

**18.7.40 void EDMA\_PrepTransfer ( *edma\_transfer\_config\_t \* config, void \* srcAddr, uint32\_t srcWidth, void \* destAddr, uint32\_t destWidth, uint32\_t bytesEachRequest, uint32\_t transferBytes, edma\_transfer\_type\_t transferType* )**

This function prepares the transfer configuration structure according to the user input.

## Parameters

<i>config</i>	The user configuration structure of type <code>edma_transfer_t</code> .
<i>srcAddr</i>	eDMA transfer source address.
<i>srcWidth</i>	eDMA transfer source address width(bytes).
<i>destAddr</i>	eDMA transfer destination address.
<i>destWidth</i>	eDMA transfer destination address width(bytes).
<i>bytesEachRequest</i>	eDMA transfer bytes per channel request.
<i>transferBytes</i>	eDMA transfer bytes to be transferred.
<i>transferType</i>	eDMA transfer type.

## Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error (SAE).

**18.7.41 status\_t EDMA\_SubmitTransfer ( *edma\_handle\_t \* handle, const edma\_transfer\_config\_t \* config* )**

This function submits the eDMA transfer request according to the transfer configuration structure. In scatter gather mode, call this function will add a configured tcd to the circular list of tcd pool. The tcd pools is setup by call function `EDMA_InstallTCDMemory` before.

Parameters

<i>handle</i>	eDMA handle pointer.
<i>config</i>	Pointer to eDMA transfer configuration structure.

Return values

<i>kStatus_EDMA_Success</i>	It means submit transfer request succeed.
<i>kStatus_EDMA_Queue-Full</i>	It means TCD queue is full. Submit transfer request is not allowed.
<i>kStatus_EDMA_Busy</i>	It means the given channel is busy, need to submit request later.

#### 18.7.42 void EDMA\_StartTransfer ( *edma\_handle\_t \* handle* )

This function enables the channel request. Users can call this function after submitting the transfer request or before submitting the transfer request.

Parameters

<i>handle</i>	eDMA handle pointer.
---------------	----------------------

#### 18.7.43 void EDMA\_StopTransfer ( *edma\_handle\_t \* handle* )

This function disables the channel request to pause the transfer. Users can call [EDMA\\_StartTransfer\(\)](#) again to resume the transfer.

Parameters

<i>handle</i>	eDMA handle pointer.
---------------	----------------------

#### 18.7.44 void EDMA\_AbortTransfer ( *edma\_handle\_t \* handle* )

This function disables the channel request and clear transfer status bits. Users can submit another transfer after calling this API.

Parameters

<i>handle</i>	DMA handle pointer.
---------------	---------------------

#### 18.7.45 static uint32\_t EDMA\_GetUnusedTCDNumber ( *edma\_handle\_t \* handle* ) [**inline**], [**static**]

This function gets current tcd index which is run. If the TCD pool pointer is NULL, it will return 0.

Parameters

<i>handle</i>	DMA handle pointer.
---------------	---------------------

Returns

The unused tcd slot number.

#### 18.7.46 static uint32\_t EDMA\_GetNextTCDAccount ( *edma\_handle\_t \* handle* ) [**inline**], [**static**]

This function gets the next tcd address. If this is last TCD, return 0.

Parameters

<i>handle</i>	DMA handle pointer.
---------------	---------------------

Returns

The next TCD address.

#### 18.7.47 void EDMA\_HandleIRQ ( *edma\_handle\_t \* handle* )

This function clears the channel major interrupt flag and calls the callback function if it is not NULL.

Note: For the case using TCD queue, when the major iteration count is exhausted, additional operations are performed. These include the final address adjustments and reloading of the BITER field into the CITER. Assertion of an optional interrupt request also occurs at this time, as does a possible fetch of a new TCD from memory using the scatter/gather address pointer included in the descriptor (if scatter/gather is enabled).

For instance, when the time interrupt of TCD[0] happens, the TCD[1] has already been loaded into the eDMA engine. As sga and sga\_index are calculated based on the DLAST\_SGA bitfield lies in the TCD\_CSR register, the sga\_index in this case should be 2 (DLAST\_SGA of TCD[1] stores the address of TCD[2]). Thus, the "tcdUsed" updated should be (tcdUsed - 2U) which indicates the number of TCDs can be loaded in the memory pool (because TCD[0] and TCD[1] have been loaded into the eDMA engine at this point already.).

For the last two continuous ISRs in a scatter/gather process, they both load the last TCD (The last ISR does not load a new TCD) from the memory pool to the eDMA engine when major loop completes. Therefore, ensure that the header and tcdUsed updated are identical for them. tcdUsed are both 0 in this case as no TCD to be loaded.

See the "eDMA basic data flow" in the eDMA Functional description section of the Reference Manual for further details.

### Parameters

<i>handle</i>	eDMA handle pointer.
---------------	----------------------

# Chapter 19

## eLCDIF: Enhanced LCD Interface

### 19.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Enhanced LCD Interface(eLCDIF)

The Enhanced LCD Interface supports MPU mode, VSYNC mode, RGB mode (or DOTCLK mode), and DVI mode. The current eLCDIF driver only supports RGB mode.

### 19.2 Typical use case

#### 19.2.1 Frame buffer update

The function [ELCDIF\\_SetNextBufferAddr](#) sets the next frame to show to eLCDIF, the eLCDIF loads the new frame and sets the interrupt [kELCDIF\\_CurFrameDone](#). If no new frame is set, the old one is displayed.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/elcdif

#### 19.2.2 Alpha surface

The alpha surface can be enabled to add an extra overlay on the normal display buffer. In this example, the alpha surface is enabled, and the alpha value is updated after every frame loaded to eLCDIF.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/elcdif

## Data Structures

- struct [elcdif\\_pixel\\_format\\_reg\\_t](#)  
*The register value when using different pixel format. [More...](#)*
- struct [elcdif\\_rgb\\_mode\\_config\\_t](#)  
*eLCDIF configure structure for RGB mode (DOTCLK mode). [More...](#)*
- struct [elcdif\\_as\\_buffer\\_config\\_t](#)  
*eLCDIF alpha surface buffer configuration. [More...](#)*
- struct [elcdif\\_as\\_blend\\_config\\_t](#)  
*eLCDIF alpha surface blending configuration. [More...](#)*

## Enumerations

- enum `_elcdif_polarity_flags` {
   
  `kELCDIF_VsyncActiveLow` = 0U,
   
  `kELCDIF_HsyncActiveLow` = 0U,
   
  `kELCDIF_DataEnableActiveLow` = 0U,
   
  `kELCDIF_DriveDataOnFallingClkEdge` = 0U,
   
  `kELCDIF_VsyncActiveHigh` = LCDIF\_VDCTRL0\_VSYNC\_POL\_MASK,
   
  `kELCDIF_HsyncActiveHigh` = LCDIF\_VDCTRL0\_HSYNC\_POL\_MASK,
   
  `kELCDIF_DataEnableActiveHigh` = LCDIF\_VDCTRL0\_ENABLE\_POL\_MASK,
   
  `kELCDIF_DriveDataOnRisingClkEdge` = LCDIF\_VDCTRL0\_DOTCLK\_POL\_MASK }
   
    *eLCDIF signal polarity flags*
- enum `_elcdif_interrupt_enable` {
   
  `kELCDIF_BusMasterErrorInterruptEnable` = LCDIF\_CTRL1\_BM\_ERROR\_IRQ\_EN\_MASK,
   
  `kELCDIF_TxFifoOverflowInterruptEnable` = LCDIF\_CTRL1\_OVERFLOW\_IRQ\_EN\_MASK,
   
  `kELCDIF_TxFifoUnderflowInterruptEnable` = LCDIF\_CTRL1\_UNDERFLOW\_IRQ\_EN\_MASK,
   
  `kELCDIF_CurFrameDoneInterruptEnable`,
   
  `kELCDIF_VsyncEdgeInterruptEnable` }
   
    *The eLCDIF interrupts to enable.*
- enum `_elcdif_interrupt_flags` {
   
  `kELCDIF_BusMasterError` = LCDIF\_CTRL1\_BM\_ERROR\_IRQ\_MASK,
   
  `kELCDIF_TxFifoOverflow` = LCDIF\_CTRL1\_OVERFLOW\_IRQ\_MASK,
   
  `kELCDIF_TxFifoUnderflow` = LCDIF\_CTRL1\_UNDERFLOW\_IRQ\_MASK,
   
  `kELCDIF_CurFrameDone`,
   
  `kELCDIF_VsyncEdge` = LCDIF\_CTRL1\_VSYNC\_EDGE\_IRQ\_MASK }
   
    *The eLCDIF interrupt status flags.*
- enum `_elcdif_status_flags` {
   
  `kELCDIF_LFifoFull` = LCDIF\_STAT\_LFIFO\_FULL\_MASK,
   
  `kELCDIF_LFifoEmpty` = LCDIF\_STAT\_LFIFO\_EMPTY\_MASK,
   
  `kELCDIF_TxFifoFull` = LCDIF\_STAT\_TXFIFO\_FULL\_MASK,
   
  `kELCDIF_TxFifoEmpty` = LCDIF\_STAT\_TXFIFO\_EMPTY\_MASK }
   
    *eLCDIF status flags*
- enum `elcdif_pixel_format_t` {
   
  `kELCDIF_PixelFormatRAW8` = 0,
   
  `kELCDIF_PixelFormatRGB565` = 1,
   
  `kELCDIF_PixelFormatRGB666` = 2,
   
  `kELCDIF_PixelFormatXRGB8888` = 3,
   
  `kELCDIF_PixelFormatRGB888` = 4 }
   
    *The pixel format.*
- enum `elcdif_lcd_data_bus_t` {
   
  `kELCDIF_DataBus8Bit` = LCDIF\_CTRL\_LCD\_DATABUS\_WIDTH(1),
   
  `kELCDIF_DataBus16Bit` = LCDIF\_CTRL\_LCD\_DATABUS\_WIDTH(0),
   
  `kELCDIF_DataBus18Bit` = LCDIF\_CTRL\_LCD\_DATABUS\_WIDTH(2),
   
  `kELCDIF_DataBus24Bit` = LCDIF\_CTRL\_LCD\_DATABUS\_WIDTH(3) }
   
    *The LCD data bus type.*
- enum `elcdif_as_pixel_format_t` {

```

kELCDIF_AsPixelFormatARGB888 = 0x0,
kELCDIF_AsPixelFormatRGB888 = 0x4,
kELCDIF_AsPixelFormatARGB1555 = 0x8,
kELCDIF_AsPixelFormatARGB4444 = 0x9,
kELCDIF_AsPixelFormatRGB555 = 0xC,
kELCDIF_AsPixelFormatRGB444 = 0xD,
kELCDIF_AsPixelFormatRGB565 = 0xE }

    eLCDIF alpha surface pixel format.
• enum elcdif_alpha_mode_t {
    kELCDIF_AlphaEmbedded,
    kELCDIF_AlphaOverride,
    kELCDIF_AlphaMultiply,
    kELCDIF_AlphaRop }

    eLCDIF alpha mode during blending.
• enum elcdif_rop_mode_t {
    kELCDIF_RopMaskAs = 0x0,
    kELCDIF_RopMaskNotAs = 0x1,
    kELCDIF_RopMaskAsNot = 0x2,
    kELCDIF_RopMergeAs = 0x3,
    kELCDIF_RopMergeNotAs = 0x4,
    kELCDIF_RopMergeAsNot = 0x5,
    kELCDIF_RopNotCopyAs = 0x6,
    kELCDIF_RopNot = 0x7,
    kELCDIF_RopNotMaskAs = 0x8,
    kELCDIF_RopNotMergeAs = 0x9,
    kELCDIF_RopXorAs = 0xA,
    kELCDIF_RopNotXorAs = 0xB }

    eLCDIF ROP mode during blending.
• enum elcdif_lut_t {
    kELCDIF_Lut0 = 0,
    kELCDIF_Lut1 }

    eLCDIF LUT

```

## Driver version

- #define FSL\_ELCDIF\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 5))  
*eLCDIF driver version*

## eLCDIF initialization and de-initialization

- void ELCIDIF\_RgbModeInit (LCDIF\_Type \*base, const elcdif\_rgb\_mode\_config\_t \*config)  
*Initializes the eLCDIF to work in RGB mode (DOTCLK mode).*
- void ELCIDIF\_RgbModeGetDefaultConfig (elcdif\_rgb\_mode\_config\_t \*config)  
*Gets the eLCDIF default configuration structure for RGB (DOTCLK) mode.*
- void ELCIDIF\_Deinit (LCDIF\_Type \*base)  
*Deinitializes the eLCDIF peripheral.*

## Module operation

- void **ELCDIF\_RgbModeSetPixelFormat** (LCDIF\_Type \*base, elcdif\_pixel\_format\_t pixelFormat)  
*Set the pixel format in RGB (DOTCLK) mode.*
- static void **ELCDIF\_RgbModeStart** (LCDIF\_Type \*base)  
*Start to display in RGB (DOTCLK) mode.*
- void **ELCDIF\_RgbModeStop** (LCDIF\_Type \*base)  
*Stop display in RGB (DOTCLK) mode and wait until finished.*
- static void **ELCDIF\_SetNextBufferAddr** (LCDIF\_Type \*base, uint32\_t bufferAddr)  
*Set the next frame buffer address to display.*
- void **ELCDIF\_Reset** (LCDIF\_Type \*base)  
*Reset the eLCDIF peripheral.*

## Status

- static uint32\_t **ELCDIF\_GetCrcValue** (const LCDIF\_Type \*base)  
*Get the CRC value of the frame sent out.*
- static uint32\_t **ELCDIF\_GetBusMasterErrorAddr** (const LCDIF\_Type \*base)  
*Get the bus master error virtual address.*
- static uint32\_t **ELCDIF\_GetStatus** (const LCDIF\_Type \*base)  
*Get the eLCDIF status.*
- static uint32\_t **ELCDIF\_GetLfFifoCount** (const LCDIF\_Type \*base)  
*Get current count in Latency buffer (LFIFO).*

## Interrupts

- static void **ELCDIF\_EnableInterrupts** (LCDIF\_Type \*base, uint32\_t mask)  
*Enables eLCDIF interrupt requests.*
- static void **ELCDIF\_DisableInterrupts** (LCDIF\_Type \*base, uint32\_t mask)  
*Disables eLCDIF interrupt requests.*
- static uint32\_t **ELCDIF\_GetInterruptStatus** (const LCDIF\_Type \*base)  
*Get eLCDIF interrupt pending status.*
- static void **ELCDIF\_ClearInterruptStatus** (LCDIF\_Type \*base, uint32\_t mask)  
*Clear eLCDIF interrupt pending status.*

## LUT

The Lookup Table (LUT) is used to expand the 8 bits pixel to 24 bits pixel before output to external display.

There are two 256x24 bits LUT memory in LCDIF, the LSB of frame buffer address determines which memory to use.

- static void **ELCDIF\_EnableLut** (LCDIF\_Type \*base, bool enable)  
*Enable or disable the LUT.*
- status\_t **ELCDIF\_UpdateLut** (LCDIF\_Type \*base, elcdif\_lut\_t lut, uint16\_t startIndex, const uint32\_t \*lutData, uint16\_t count)  
*Load the LUT value.*

## 19.3 Data Structure Documentation

### 19.3.1 struct elcdif\_pixel\_format\_reg\_t

These register bits control the pixel format:

- CTRL[DATA\_FORMAT\_24\_BIT]
- CTRL[DATA\_FORMAT\_18\_BIT]
- CTRL[DATA\_FORMAT\_16\_BIT]
- CTRL[WORD\_LENGTH]
- CTRL1[BYTE\_PACKING\_FORMAT]

#### Data Fields

- uint32\_t regCtrl  
*Value of register CTRL.*
- uint32\_t regCtrl1  
*Value of register CTRL1.*

#### Field Documentation

- (1) uint32\_t elcdif\_pixel\_format\_reg\_t::regCtrl
- (2) uint32\_t elcdif\_pixel\_format\_reg\_t::regCtrl1

### 19.3.2 struct elcdif\_rgb\_mode\_config\_t

#### Data Fields

- uint16\_t panelWidth  
*Display panel width, pixels per line.*
- uint16\_t panelHeight  
*Display panel height, how many lines per panel.*
- uint8\_t hsw  
*HSYNC pulse width.*
- uint8\_t hfp  
*Horizontal front porch.*
- uint8\_t hbp  
*Horizontal back porch.*
- uint8\_t vsw  
*VSYNC pulse width.*
- uint8\_t vfp  
*Vertical front porch.*
- uint8\_t vbp  
*Vertical back porch.*
- uint32\_t polarityFlags  
*OR'ed value of \_elcdif\_polarity\_flags, used to control the signal polarity.*
- uint32\_t bufferAddr

- *Frame buffer address.*
- `elcdif_pixel_format_t pixelFormat`  
*Pixel format.*
- `elcdif_lcd_data_bus_t dataBus`  
*LCD data bus.*

## Field Documentation

- (1) `uint16_t elcdif_rgb_mode_config_t::panelWidth`
- (2) `uint16_t elcdif_rgb_mode_config_t::panelHeight`
- (3) `uint8_t elcdif_rgb_mode_config_t::hsw`
- (4) `uint8_t elcdif_rgb_mode_config_t::hfp`
- (5) `uint8_t elcdif_rgb_mode_config_t::hbp`
- (6) `uint8_t elcdif_rgb_mode_config_t::vsw`
- (7) `uint8_t elcdif_rgb_mode_config_t::vfp`
- (8) `uint8_t elcdif_rgb_mode_config_t::vbp`
- (9) `uint32_t elcdif_rgb_mode_config_t::polarityFlags`
- (10) `uint32_t elcdif_rgb_mode_config_t::bufferAddr`
- (11) `elcdif_pixel_format_t elcdif_rgb_mode_config_t::pixelFormat`
- (12) `elcdif_lcd_data_bus_t elcdif_rgb_mode_config_t::dataBus`

### 19.3.3 struct elcdif\_as\_buffer\_config\_t

#### Data Fields

- `uint32_t bufferAddr`  
*Buffer address.*
- `elcdif_as_pixel_format_t pixelFormat`  
*Pixel format.*

**Field Documentation**

- (1) `uint32_t elcdif_as_buffer_config_t::bufferAddr`
- (2) `elcdif_as_pixel_format_t elcdif_as_buffer_config_t::pixelFormat`

**19.3.4 struct elcdif\_as\_blend\_config\_t****Data Fields**

- `uint8_t alpha`  
*User defined alpha value, only used when `alphaMode` is `kELCDIF_AlphaOverride` or `kELCDIF_AlphaRop`.*
- `bool invertAlpha`  
*Set true to invert the alpha.*
- `elcdif_alpha_mode_t alphaMode`  
*Alpha mode.*
- `elcdif_rop_mode_t ropMode`  
*ROP mode, only valid when `alphaMode` is `kELCDIF_AlphaRop`.*

**Field Documentation**

- (1) `uint8_t elcdif_as_blend_config_t::alpha`
- (2) `bool elcdif_as_blend_config_t::invertAlpha`
- (3) `elcdif_alpha_mode_t elcdif_as_blend_config_t::alphaMode`
- (4) `elcdif_rop_mode_t elcdif_as_blend_config_t::ropMode`

**19.4 Enumeration Type Documentation****19.4.1 enum \_elcdif\_polarity\_flags**

Enumerator

`kELCDIF_VsyncActiveLow` VSYNC active low.`kELCDIF_HsyncActiveLow` HSYNC active low.`kELCDIF_DataEnableActiveLow` Data enable line active low.`kELCDIF_DriveDataOnFallingClkEdge` Drive data on falling clock edge, capture data on rising clock edge.`kELCDIF_VsyncActiveHigh` VSYNC active high.`kELCDIF_HsyncActiveHigh` HSYNC active high.`kELCDIF_DataEnableActiveHigh` Data enable line active high.`kELCDIF_DriveDataOnRisingClkEdge` Drive data on falling clock edge, capture data on rising clock edge.

### 19.4.2 enum \_elcdif\_interrupt\_enable

Enumerator

- kELCDIF\_BusMasterErrorInterruptEnable* Bus master error interrupt.
- kELCDIF\_TxFifoOverflowInterruptEnable* TXFIFO overflow interrupt.
- kELCDIF\_TxFifoUnderflowInterruptEnable* TXFIFO underflow interrupt.
- kELCDIF\_CurFrameDoneInterruptEnable* Interrupt when hardware enters vertical blanking state.
- kELCDIF\_VsyncEdgeInterruptEnable* Interrupt when hardware encounters VSYNC edge.

### 19.4.3 enum \_elcdif\_interrupt\_flags

Enumerator

- kELCDIF\_BusMasterError* Bus master error interrupt.
- kELCDIF\_TxFifoOverflow* TXFIFO overflow interrupt.
- kELCDIF\_TxFifoUnderflow* TXFIFO underflow interrupt.
- kELCDIF\_CurFrameDone* Interrupt when hardware enters vertical blanking state.
- kELCDIF\_VsyncEdge* Interrupt when hardware encounters VSYNC edge.

### 19.4.4 enum \_elcdif\_status\_flags

Enumerator

- kELCDIF\_LFifoFull* LFIFO full.
- kELCDIF\_LFifoEmpty* LFIFO empty.
- kELCDIF\_TxFifoFull* TXFIFO full.
- kELCDIF\_TxFifoEmpty* TXFIFO empty.

### 19.4.5 enum elcdif\_pixel\_format\_t

This enumerator should be defined together with the array s\_pixelFormatReg. To support new pixel format, enhance this enumerator and s\_pixelFormatReg.

Enumerator

- kELCDIF\_PixelFormatRAW8* RAW 8 bit, four data use 32 bits.
- kELCDIF\_PixelFormatRGB565* RGB565, two pixel use 32 bits.
- kELCDIF\_PixelFormatRGB666* RGB666 unpacked, one pixel uses 32 bits, high byte unused, upper 2 bits of other bytes unused.

***kLCDIF\_PixelFormatXRGB8888*** XRGB8888 unpacked, one pixel uses 32 bits, high byte unused.

***kLCDIF\_PixelFormatRGB888*** RGB888 packed, one pixel uses 24 bits.

#### 19.4.6 enum elcdif\_lcd\_data\_bus\_t

Enumerator

***kLCDIF\_DataBus8Bit*** 8-bit data bus.

***kLCDIF\_DataBus16Bit*** 16-bit data bus, support RGB565.

***kLCDIF\_DataBus18Bit*** 18-bit data bus, support RGB666.

***kLCDIF\_DataBus24Bit*** 24-bit data bus, support RGB888.

#### 19.4.7 enum elcdif\_as\_pixel\_format\_t

Enumerator

***kLCDIF\_AsPixelFormatARGB8888*** 32-bit pixels with alpha.

***kLCDIF\_AsPixelFormatRGB888*** 32-bit pixels without alpha (unpacked 24-bit format)

***kLCDIF\_AsPixelFormatARGB1555*** 16-bit pixels with alpha.

***kLCDIF\_AsPixelFormatARGB4444*** 16-bit pixels with alpha.

***kLCDIF\_AsPixelFormatRGB555*** 16-bit pixels without alpha.

***kLCDIF\_AsPixelFormatRGB444*** 16-bit pixels without alpha.

***kLCDIF\_AsPixelFormatRGB565*** 16-bit pixels without alpha.

#### 19.4.8 enum elcdif\_alpha\_mode\_t

Enumerator

***kLCDIF\_AlphaEmbedded*** The alpha surface pixel alpha value will be used for blend.

***kLCDIF\_AlphaOverride*** The user defined alpha value will be used for blend directly.

***kLCDIF\_AlphaMultiply*** The alpha surface pixel alpha value scaled the user defined alpha value will be used for blend, for example, pixel alpha set to 200, user defined alpha set to 100, then the result alpha is  $200 * 100 / 255$ .

***kLCDIF\_AlphaRop*** Raster operation.

#### 19.4.9 enum elcdif\_rop\_mode\_t

Explanation:

- AS: Alpha surface
- PS: Process surface
- nAS: Alpha surface NOT value
- nPS: Process surface NOT value

Enumerator

*kELCDIF\_RopMaskAs* AS AND PS.  
*kELCDIF\_RopMaskNotAs* nAS AND PS.  
*kELCDIF\_RopMaskAsNot* AS AND nPS.  
*kELCDIF\_RopMergeAs* AS OR PS.  
*kELCDIF\_RopMergeNotAs* nAS OR PS.  
*kELCDIF\_RopMergeAsNot* AS OR nPS.  
*kELCDIF\_RopNotCopyAs* nAS.  
*kELCDIF\_RopNot* nPS.  
*kELCDIF\_RopNotMaskAs* AS NAND PS.  
*kELCDIF\_RopNotMergeAs* AS NOR PS.  
*kELCDIF\_RopXorAs* AS XOR PS.  
*kELCDIF\_RopNotXorAs* AS XNOR PS.

#### 19.4.10 enum elcdif\_lut\_t

The Lookup Table (LUT) is used to expand the 8 bits pixel to 24 bits pixel before output to external display.

There are two 256x24 bits LUT memory in LCDIF, the LSB of frame buffer address determines which memory to use.

Enumerator

*kELCDIF\_Lut0* LUT 0.  
*kELCDIF\_Lut1* LUT 1.

### 19.5 Function Documentation

#### 19.5.1 void ELCDIF\_RgbModelInit ( LCDIF\_Type \* *base*, const elcdif\_rgb\_mode\_config\_t \* *config* )

This function un gates the eLCDIF clock and configures the eLCDIF peripheral according to the configuration structure.

## Parameters

<i>base</i>	eLCDIF peripheral base address.
<i>config</i>	Pointer to the configuration structure.

**19.5.2 void ELCDIF\_RgbModeGetDefaultConfig ( elcdif\_rgb\_mode\_config\_t \* *config* )**

This function sets the configuration structure to default values. The default configuration is set to the following values.

```
config->panelWidth = 480U;
config->panelHeight = 272U;
config->hsw = 41;
config->hfp = 4;
config->hbp = 8;
config->vsw = 10;
config->vfp = 4;
config->vbp = 2;
config->polarityFlags = kELCDIF_VsyncActiveLow |
                        kELCDIF_HsyncActiveLow |
                        kELCDIF_DataEnableActiveLow |
                        kELCDIF_DriveDataOnFallingClkEdge;
config->bufferAddr = 0U;
config->pixelFormat = kELCDIF_PixelFormatRGB888;
config->dataBus = kELCDIF_DataBus24Bit;
```

## Parameters

<i>config</i>	Pointer to the eLCDIF configuration structure.
---------------	--

**19.5.3 void ELCDIF\_Deinit ( LCDIF\_Type \* *base* )**

## Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

**19.5.4 void ELCDIF\_RgbModeSetPixelFormat ( LCDIF\_Type \* *base*, elcdif\_pixel\_format\_t *pixelFormat* )**

Parameters

<i>base</i>	eLCDIF peripheral base address.
<i>pixelFormat</i>	The pixel format.

#### 19.5.5 static void ELCDIF\_RgbModeStart ( LCDIF\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

#### 19.5.6 void ELCDIF\_RgbModeStop ( LCDIF\_Type \* *base* )

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

#### 19.5.7 static void ELCDIF\_SetNextBufferAddr ( LCDIF\_Type \* *base*, uint32\_t *bufferAddr* ) [inline], [static]

Parameters

<i>base</i>	eLCDIF peripheral base address.
<i>bufferAddr</i>	The frame buffer address to set.

#### 19.5.8 void ELCDIF\_Reset ( LCDIF\_Type \* *base* )

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

**19.5.9 static uint32\_t ELCDIF\_GetCrcValue ( const LCDIF\_Type \* *base* )  
[inline], [static]**

When a frame is sent complete (the interrupt [kELCDIF\\_CurFrameDone](#) assert), this function can be used to get the CRC value of the frame sent.

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

Returns

The CRC value.

Note

The CRC value is dependent on the LCD\_DATABUS\_WIDTH.

#### 19.5.10 static uint32\_t ELCDIF\_GetBusMasterErrorAddr ( const LCDIF\_Type \* *base* ) [inline], [static]

When bus master error occurs (the interrupt kELCDIF\_BusMasterError assert), this function can get the virtual address at which the AXI master received an error response from the slave.

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

Returns

The error virtual address.

#### 19.5.11 static uint32\_t ELCDIF\_GetStatus ( const LCDIF\_Type \* *base* ) [inline], [static]

The status flags are returned as a mask value, application could check the corresponding bit. Example:

```
uint32_t statusFlags;
statusFlags = ELCDIF_GetStatus(LCDIF);

if (kELCDIF_LFifoFull & statusFlags)
{
}

if (kELCDIF_TxFifoEmpty & statusFlags)
{
}
```

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

Returns

The mask value of status flags, it is OR'ed value of `_elcdif_status_flags`.

#### 19.5.12 static uint32\_t ELCDIF\_GetLFifoCount ( const LCDIF\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

Returns

The LFIFO current count

#### 19.5.13 static void ELCDIF\_EnableInterrupts ( LCDIF\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	eLCDIF peripheral base address.
<i>mask</i>	interrupt source, OR'ed value of <code>_elcdif_interrupt_enable</code> .

#### 19.5.14 static void ELCDIF\_DisableInterrupts ( LCDIF\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

<i>mask</i>	interrupt source, OR'ed value of _elcdif_interrupt_enable.
-------------	--

**19.5.15 static uint32\_t ELCDIF\_GetInterruptStatus ( const LCDIF\_Type \* *base* )  
[inline], [static]**

Parameters

<i>base</i>	eLCDIF peripheral base address.
-------------	---------------------------------

Returns

Interrupt pending status, OR'ed value of \_elcdif\_interrupt\_flags.

**19.5.16 static void ELCDIF\_ClearInterruptStatus ( LCDIF\_Type \* *base*, uint32\_t  
*mask* ) [inline], [static]**

Parameters

<i>base</i>	eLCDIF peripheral base address.
<i>mask</i>	of the flags to clear, OR'ed value of _elcdif_interrupt_flags.

**19.5.17 static void ELCDIF\_EnableLut ( LCDIF\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	eLCDIF peripheral base address.
<i>enable</i>	True to enable, false to disable.

**19.5.18 status\_t ELCDIF\_UpdateLut ( LCDIF\_Type \* *base*, elcdif\_lut\_t *lut*, uint16\_t  
*startIndex*, const uint32\_t \* *lutData*, uint16\_t *count* )**

This function loads the LUT value to the specific LUT memory, user can specify the start entry index.

## Parameters

<i>base</i>	eLCDIF peripheral base address.
<i>lut</i>	Which LUT to load.
<i>startIndex</i>	The start index of the LUT entry to update.
<i>lutData</i>	The LUT data to load.
<i>count</i>	Count of <i>lutData</i> .

## Return values

<i>kStatus_Success</i>	Initialization success.
<i>kStatus_InvalidArgument</i>	Wrong argument.

# Chapter 20

## ENC: Quadrature Encoder/Decoder

### 20.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Quadrature Encoder/Decoder (ENC) module of MCUXpresso SDK devices.

This section describes the programming interface of the ENC Peripheral driver. The ENC driver configures the ENC module and provides a functional interface for the user to build the ENC application.

### 20.2 Function groups

#### 20.2.1 Initialization and De-initialization

This function group initializes default configuration structure for the ENC counter and initializes ENC counter with the normal configuration and de-initialize ENC module. Some APIs are also created to control the features.

#### 20.2.2 Status

This function group get/clear the ENC status.

#### 20.2.3 Interrupts

This function group enable/disable the ENC interrupts.

#### 20.2.4 Value Operation

This function group get the counter/hold value of positions.

### 20.3 Typical use case

#### 20.3.1 Polling Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/enc

### Data Structures

- struct [enc\\_config\\_t](#)

- Define user configuration structure for ENC module. [More...](#)
- struct `enc_self_test_config_t`  
Define configuration structure for self test module. [More...](#)

## Enumerations

- enum `_enc_interrupt_enable` {
   
`kENC_HOMETransitionInterruptEnable` = (1U << 0U),
   
`kENC_INDEXPulseInterruptEnable` = (1U << 1U),
   
`kENC_WatchdogTimeoutInterruptEnable` = (1U << 2U),
   
`kENC_PositionCompareInerruptEnable` = (1U << 3U),
   
`kENC_PositionRollOverInterruptEnable` = (1U << 5U),
   
`kENC_PositionRollUnderInterruptEnable` = (1U << 6U) }
   
*Interrupt enable/disable mask.*
- enum `_enc_status_flags` {
   
`kENC_HOMETransitionFlag` = (1U << 0U),
   
`kENC_INDEXPulseFlag` = (1U << 1U),
   
`kENC_WatchdogTimeoutFlag` = (1U << 2U),
   
`kENC_PositionCompareFlag` = (1U << 3U),
   
`kENC_PositionRollOverFlag` = (1U << 5U),
   
`kENC_PositionRollUnderFlag` = (1U << 6U),
   
`kENC_LastCountDirectionFlag` = (1U << 7U) }
   
*Status flag mask.*
- enum `_enc_signal_status_flags` {
   
`kENC_RawHOMEStatusFlag` = ENC\_IMR\_HOME\_MASK,
   
`kENC_RawINDEXStatusFlag` = ENC\_IMR\_INDEX\_MASK,
   
`kENC_RawPHBStatusFlag` = ENC\_IMR\_PHB\_MASK,
   
`kENC_RawPHAXStatusFlag` = ENC\_IMR\_PHA\_MASK,
   
`kENC_FilteredHOMEStatusFlag` = ENC\_IMR\_FHOM\_MASK,
   
`kENC_FilteredINDEXStatusFlag` = ENC\_IMR\_FIND\_MASK,
   
`kENC_FilteredPHBStatusFlag` = ENC\_IMR\_FPHB\_MASK,
   
`kENC_FilteredPHASStatusFlag` = ENC\_IMR\_FPHA\_MASK }  
*Signal status flag mask.*
- enum `enc_home_trigger_mode_t` {
   
`kENC_HOMETriggerDisabled` = 0U,
   
`kENC_HOMETriggerOnRisingEdge`,
   
`kENC_HOMETriggerOnFallingEdge` }
   
*Define HOME signal's trigger mode.*
- enum `enc_index_trigger_mode_t` {
   
`kENC_INDEXTriggerDisabled` = 0U,
   
`kENC_INDEXTriggerOnRisingEdge`,
   
`kENC_INDEXTriggerOnFallingEdge` }
   
*Define INDEX signal's trigger mode.*
- enum `enc_decoder_work_mode_t` {
   
`kENC_DecoderWorkAsNormalMode` = 0U,
   
`kENC_DecoderWorkAsSignalPhaseCountMode` }
   
*Define type for decoder work mode.*

- enum `enc_position_match_mode_t` {
   
  `kENC_POSMATCHOnPositionCounterEqualToComapreValue` = 0U,
   
  `kENC_POSMATCHOnReadingAnyPositionCounter` }
   
*Define type for the condition of POSMATCH pulses.*
- enum `enc_revolution_count_condition_t` {
   
  `kENC_RevolutionCountOnINDEXPulse` = 0U,
   
  `kENC_RevolutionCountOnRollOverModulus` }
   
*Define type for determining how the revolution counter (REV) is incremented/decremented.*
- enum `enc_self_test_direction_t` {
   
  `kENC_SelfTestDirectionPositive` = 0U,
   
  `kENC_SelfTestDirectionNegative` }
   
*Define type for direction of self test generated signal.*
- enum `enc_filter_prescaler_t` {
   
  `kENC_FilterPrescalerDiv1` = 0U,
   
  `kENC_FilterPrescalerDiv2` = 1U,
   
  `kENC_FilterPrescalerDiv4` = 2U,
   
  `kENC_FilterPrescalerDiv8` = 3U,
   
  `kENC_FilterPrescalerDiv16` = 4U,
   
  `kENC_FilterPrescalerDiv32` = 5U,
   
  `kENC_FilterPrescalerDiv64` = 6U,
   
  `kENC_FilterPrescalerDiv128` = 7U }
   
*Define input filter prescaler value.*

## Initialization and De-initialization

- void `ENC_Init` (`ENC_Type` \*base, const `enc_config_t` \*config)
   
*Initialization for the ENC module.*
- void `ENC_Deinit` (`ENC_Type` \*base)
   
*De-initialization for the ENC module.*
- void `ENC_GetDefaultConfig` (`enc_config_t` \*config)
   
*Get an available pre-defined settings for ENC's configuration.*
- void `ENC_DoSoftwareLoadInitialPositionValue` (`ENC_Type` \*base)
   
*Load the initial position value to position counter.*
- void `ENC_SetSelfTestConfig` (`ENC_Type` \*base, const `enc_self_test_config_t` \*config)
   
*Enable and configure the self test function.*
- void `ENC_EnableWatchdog` (`ENC_Type` \*base, bool enable)
   
*Enable watchdog for ENC module.*
- void `ENC_SetInitialPositionValue` (`ENC_Type` \*base, `uint32_t` value)
   
*Set initial position value for ENC module.*

## Status

- `uint32_t ENC_GetStatusFlags` (`ENC_Type` \*base)
   
*Get the status flags.*
- void `ENC_ClearStatusFlags` (`ENC_Type` \*base, `uint32_t` mask)
   
*Clear the status flags.*
- static `uint16_t ENC_GetSignalStatusFlags` (`ENC_Type` \*base)
   
*Get the signals' real-time status.*

## Interrupts

- void `ENC_EnableInterrupts` (ENC\_Type \*base, uint32\_t mask)  
*Enable the interrupts.*
- void `ENC_DisableInterrupts` (ENC\_Type \*base, uint32\_t mask)  
*Disable the interrupts.*
- uint32\_t `ENC_GetEnabledInterrupts` (ENC\_Type \*base)  
*Get the enabled interrupts' flags.*

## Value Operation

- uint32\_t `ENCGetPositionValue` (ENC\_Type \*base)  
*Get the current position counter's value.*
- uint32\_t `ENCGetHoldPositionValue` (ENC\_Type \*base)  
*Get the hold position counter's value.*
- static uint16\_t `ENCGetPositionDifferenceValue` (ENC\_Type \*base)  
*Get the position difference counter's value.*
- static uint16\_t `ENCGetHoldPositionDifferenceValue` (ENC\_Type \*base)  
*Get the hold position difference counter's value.*
- static uint16\_t `ENCGetRevolutionValue` (ENC\_Type \*base)  
*Get the position revolution counter's value.*
- static uint16\_t `ENCGetHoldRevolutionValue` (ENC\_Type \*base)  
*Get the hold position revolution counter's value.*

## 20.4 Data Structure Documentation

### 20.4.1 struct enc\_config\_t

#### Data Fields

- bool `enableReverseDirection`  
*Enable reverse direction counting.*
- `enc_decoder_work_mode_t` `decoderWorkMode`  
*Enable signal phase count mode.*
- `enc_home_trigger_mode_t` `HOMETriggerMode`  
*Enable HOME to initialize position counters.*
- `enc_index_trigger_mode_t` `INDEXTriggerMode`  
*Enable INDEX to initialize position counters.*
- bool `enableTRIGGERClearPositionCounter`  
*Clear POSD, REV, UPOS and LPOS on rising edge of TRIGGER, or not.*
- bool `enableTRIGGERClearHoldPositionCounter`  
*Enable update of hold registers on rising edge of TRIGGER, or not.*
- bool `enableWatchdog`  
*Enable the watchdog to detect if the target is moving or not.*
- uint16\_t `watchdogTimeoutValue`  
*Watchdog timeout count value.*
- `enc_filter_prescaler_t` `filterPrescaler`  
*Input filter prescaler.*
- uint16\_t `filterCount`  
*Input Filter Sample Count.*

- `uint16_t filterSamplePeriod`  
*Input Filter Sample Period.*
- `enc_position_match_mode_t positionMatchMode`  
*The condition of POSMATCH pulses.*
- `uint32_t positionCompareValue`  
*Position compare value.*
- `enc_revolution_count_condition_t revolutionCountCondition`  
*Revolution Counter Modulus Enable.*
- `bool enableModuloCountMode`  
*Enable Modulo Counting.*
- `uint32_t positionModulusValue`  
*Position modulus value.*
- `uint32_t positionInitialValue`  
*Position initial value.*

## Field Documentation

- (1) `bool enc_config_t::enableReverseDirection`
- (2) `enc_decoder_work_mode_t enc_config_t::decoderWorkMode`
- (3) `enc_home_trigger_mode_t enc_config_t::HOMETriggerMode`
- (4) `enc_index_trigger_mode_t enc_config_t::INDEXTriggerMode`
- (5) `bool enc_config_t::enableTRIGGERClearPositionCounter`
- (6) `bool enc_config_t::enableWatchdog`
- (7) `uint16_t enc_config_t::watchdogTimeoutValue`

It stores the timeout count for the quadrature decoder module watchdog timer. This field is only available when "enableWatchdog" = true. The available value is a 16-bit unsigned number.

- (8) `enc_filter_prescaler_t enc_config_t::filterPrescaler`
- (9) `uint16_t enc_config_t::filterCount`

This value should be chosen to reduce the probability of noisy samples causing an incorrect transition to be recognized. The value represent the number of consecutive samples that must agree prior to the input filter accepting an input transition. A value of 0x0 represents 3 samples. A value of 0x7 represents 10 samples. The Available range is 0 - 7.

- (10) `uint16_t enc_config_t::filterSamplePeriod`

This value should be set such that the sampling period is larger than the period of the expected noise. This value represents the sampling period (in IPBus clock cycles) of the decoder input signals. The available range is 0 - 255.

(11) **enc\_position\_match\_mode\_t enc\_config\_t::positionMatchMode**

(12) **uint32\_t enc\_config\_t::positionCompareValue**

The available value is a 32-bit number.

(13) **enc\_revolution\_count\_condition\_t enc\_config\_t::revolutionCountCondition**

(14) **bool enc\_config\_t::enableModuloCountMode**

(15) **uint32\_t enc\_config\_t::positionModulusValue**

This value would be available only when "enableModuloCountMode" = true. The available value is a 32-bit number.

(16) **uint32\_t enc\_config\_t::positionInitialValue**

The available value is a 32-bit number.

#### 20.4.2 struct enc\_self\_test\_config\_t

The self test module provides a quadrature test signal to the inputs of the quadrature decoder module. This is a factory test feature. It is also useful to customers' software development and testing.

#### Data Fields

- **enc\_self\_test\_direction\_t signalDirection**  
*Direction of self test generated signal.*
- **uint16\_t signalCount**  
*Hold the number of quadrature advances to generate.*
- **uint16\_t signalPeriod**  
*Hold the period of quadrature phase in IPBus clock cycles.*

#### Field Documentation

(1) **enc\_self\_test\_direction\_t enc\_self\_test\_config\_t::signalDirection**

(2) **uint16\_t enc\_self\_test\_config\_t::signalCount**

The available range is 0 - 255.

(3) **uint16\_t enc\_self\_test\_config\_t::signalPeriod**

The available range is 0 - 31.

## 20.5 Enumeration Type Documentation

### 20.5.1 enum \_enc\_interrupt\_enable

Enumerator

*kENC\_HOMETransitionInterruptEnable* HOME interrupt enable.

*kENC\_INDEXPulseInterruptEnable* INDEX pulse interrupt enable.

*kENC\_WatchdogTimeoutInterruptEnable* Watchdog timeout interrupt enable.

*kENC\_PositionCompareInerruptEnable* Position compare interrupt enable.

*kENC\_PositionRollOverInterruptEnable* Roll-over interrupt enable.

*kENC\_PositionRollUnderInterruptEnable* Roll-under interrupt enable.

### 20.5.2 enum \_enc\_status\_flags

These flags indicate the counter's events.

Enumerator

*kENC\_HOMETransitionFlag* HOME signal transition interrupt request.

*kENC\_INDEXPulseFlag* INDEX Pulse Interrupt Request.

*kENC\_WatchdogTimeoutFlag* Watchdog timeout interrupt request.

*kENC\_PositionCompareFlag* Position compare interrupt request.

*kENC\_PositionRollOverFlag* Roll-over interrupt request.

*kENC\_PositionRollUnderFlag* Roll-under interrupt request.

*kENC\_LastCountDirectionFlag* Last count was in the up direction, or the down direction.

### 20.5.3 enum \_enc\_signal\_status\_flags

These flags indicate the counter's signal.

Enumerator

*kENC\_RawHOMEStatusFlag* Raw HOME input.

*kENC\_RawINDEXStatusFlag* Raw INDEX input.

*kENC\_RawPHBStatusFlag* Raw PHASEB input.

*kENC\_RawPHAEXStatusFlag* Raw PHASEA input.

*kENC\_FilteredHOMESStatusFlag* The filtered version of HOME input.

*kENC\_FilteredINDEXStatusFlag* The filtered version of INDEX input.

*kENC\_FilteredPHBStatusFlag* The filtered version of PHASEB input.

*kENC\_FilteredPHASStatusFlag* The filtered version of PHASEA input.

## 20.5.4 enum enc\_home\_trigger\_mode\_t

The ENC would count the trigger from HOME signal line.

Enumerator

***kENC\_HOMETriggerDisabled*** HOME signal's trigger is disabled.

***kENC\_HOMETriggerOnRisingEdge*** Use positive going edge-to-trigger initialization of position counters.

***kENC\_HOMETriggerOnFallingEdge*** Use negative going edge-to-trigger initialization of position counters.

## 20.5.5 enum enc\_index\_trigger\_mode\_t

The ENC would count the trigger from INDEX signal line.

Enumerator

***kENC\_INDEXTriggerDisabled*** INDEX signal's trigger is disabled.

***kENC\_INDEXTriggerOnRisingEdge*** Use positive going edge-to-trigger initialization of position counters.

***kENC\_INDEXTriggerOnFallingEdge*** Use negative going edge-to-trigger initialization of position counters.

## 20.5.6 enum enc\_decoder\_work\_mode\_t

The normal work mode uses the standard quadrature decoder with PHASEA and PHASEB. When in signal phase count mode, a positive transition of the PHASEA input generates a count signal while the PHASEB input and the reverse direction control the counter direction. If the reverse direction is not enabled, PHASEB = 0 means counting up and PHASEB = 1 means counting down. Otherwise, the direction is reversed.

Enumerator

***kENC\_DecoderWorkAsNormalMode*** Use standard quadrature decoder with PHASEA and PHASEB.

***kENC\_DecoderWorkAsSignalPhaseCountMode*** PHASEA input generates a count signal while PHASEB input control the direction.

## 20.5.7 enum enc\_position\_match\_mode\_t

Enumerator

***kENC\_POSMATCHOnPositionCounterEqualToComapreValue*** POSMATCH pulses when a match occurs between the position counters (POS) and the compare value (COMP).

***kENC\_POSMATCHOnReadingAnyPositionCounter*** POSMATCH pulses when any position counter register is read.

### 20.5.8 enum enc\_revolution\_count\_condition\_t

Enumerator

***kENC\_RevolutionCountOnINDEXPulse*** Use INDEX pulse to increment/decrement revolution counter.

***kENC\_RevolutionCountOnRollOverModulus*** Use modulus counting roll-over/under to increment/decrement revolution counter.

### 20.5.9 enum enc\_self\_test\_direction\_t

Enumerator

***kENC\_SelfTestDirectionPositive*** Self test generates the signal in positive direction.

***kENC\_SelfTestDirectionNegative*** Self test generates the signal in negative direction.

### 20.5.10 enum enc\_filter\_prescaler\_t

The input filter prescaler value is to prescale the IPBus clock. (Frequency of FILT clock) = (Frequency of IPBus clock) /  $2^{\text{FILT\_PRSC}}$ .

Enumerator

***kENC\_FilterPrescalerDiv1*** Input filter prescaler is 1.

***kENC\_FilterPrescalerDiv2*** Input filter prescaler is 2.

***kENC\_FilterPrescalerDiv4*** Input filter prescaler is 4.

***kENC\_FilterPrescalerDiv8*** Input filter prescaler is 8.

***kENC\_FilterPrescalerDiv16*** Input filter prescaler is 16.

***kENC\_FilterPrescalerDiv32*** Input filter prescaler is 32.

***kENC\_FilterPrescalerDiv64*** Input filter prescaler is 64.

***kENC\_FilterPrescalerDiv128*** Input filter prescaler is 128.

## 20.6 Function Documentation

### 20.6.1 void ENC\_Init ( ***ENC\_Type \* base***, ***const enc\_config\_t \* config*** )

This function is to make the initialization for the ENC module. It should be called firstly before any operation to the ENC with the operations like:

- Enable the clock for ENC module.
- Configure the ENC's working attributes.

## Parameters

<i>base</i>	ENC peripheral base address.
<i>config</i>	Pointer to configuration structure. See to "enc_config_t".

**20.6.2 void ENC\_Deinit ( ENC\_Type \* *base* )**

This function is to make the de-initialization for the ENC module. It could be called when ENC is no longer used with the operations like:

- Disable the clock for ENC module.

## Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

**20.6.3 void ENC\_GetDefaultConfig ( enc\_config\_t \* *config* )**

This function initializes the ENC configuration structure with an available settings, the default value are:

```
* config->enableReverseDirection           = false;
* config->decoderWorkMode                 = kENC_DecoderWorkAsNormalMode
  ;
* config->HOMETriggerMode                = kENC_HOMETriggerDisabled;
* config->INDEXTriggerMode              = kENC_INDEXTriggerDisabled;
* config->enableTRIGGERClearPositionCounter = false;
* config->enableTRIGGERClearHoldPositionCounter = false;
* config->enableWatchdog                  = false;
* config->watchdogTimeoutValue          = 0U;
* config->filterCount                   = 0U;
* config->filterSamplePeriod           = 0U;
* config->positionMatchMode            =
  kENC_POSMATCHOnPositionCounterEqualToComapreValue;
* config->positionCompareValue         = 0xFFFFFFFFU;
* config->revolutionCountCondition     =
  kENC_RevolutionCountOnINDEXPulse;
* config->enableModuloCountMode        = false;
* config->positionModulusValue         = 0U;
* config->positionInitialValue         = 0U;
* config->prescalerValue               = kENC_ClockDiv1;
* config->enablePeriodMeasurementFunction = true;
*
```

## Parameters

<i>config</i>	Pointer to a variable of configuration structure. See to "enc_config_t".
---------------	--

#### 20.6.4 void ENC\_DoSoftwareLoadInitialPositionValue ( **ENC\_Type** \* *base* )

This function is to transfer the initial position value (UINIT and LINIT) contents to position counter (UP-OS and LPOS), so that to provide the consistent operation the position counter registers.

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

#### 20.6.5 void ENC\_SetSelfTestConfig ( **ENC\_Type** \* *base*, const **enc\_self\_test\_config\_t** \* *config* )

This function is to enable and configuration the self test function. It controls and sets the frequency of a quadrature signal generator. It provides a quadrature test signal to the inputs of the quadrature decoder module. It is a factory test feature; however, it may be useful to customers' software development and testing.

Parameters

<i>base</i>	ENC peripheral base address.
<i>config</i>	Pointer to configuration structure. See to "enc_self_test_config_t". Pass "NULL" to disable.

#### 20.6.6 void ENC\_EnableWatchdog ( **ENC\_Type** \* *base*, **bool** *enable* )

Parameters

<i>base</i>	ENC peripheral base address
<i>enable</i>	Enables or disables the watchdog

#### 20.6.7 void ENC\_SetInitialPositionValue ( **ENC\_Type** \* *base*, **uint32\_t** *value* )

Parameters

<i>base</i>	ENC peripheral base address
<i>value</i>	Positive initial value

### 20.6.8 `uint32_t ENC_GetStatusFlags ( ENC_Type * base )`

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

Mask value of status flags. For available mask, see to "\_enc\_status\_flags".

### 20.6.9 `void ENC_ClearStatusFlags ( ENC_Type * base, uint32_t mask )`

Parameters

<i>base</i>	ENC peripheral base address.
<i>mask</i>	Mask value of status flags to be cleared. For available mask, see to "_enc_status_flags".

### 20.6.10 `static uint16_t ENC_GetSignalStatusFlags ( ENC_Type * base ) [inline], [static]`

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

Mask value of signals' real-time status. For available mask, see to "\_enc\_signal\_status\_flags"

### 20.6.11 `void ENC_EnableInterrupts ( ENC_Type * base, uint32_t mask )`

Parameters

<i>base</i>	ENC peripheral base address.
<i>mask</i>	Mask value of interrupts to be enabled. For available mask, see to "_enc_interrupt_enable".

### 20.6.12 void ENC\_DisableInterrupts ( ENC\_Type \* *base*, uint32\_t *mask* )

Parameters

<i>base</i>	ENC peripheral base address.
<i>mask</i>	Mask value of interrupts to be disabled. For available mask, see to "_enc_interrupt_enable".

### 20.6.13 uint32\_t ENC\_GetEnabledInterrupts ( ENC\_Type \* *base* )

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

Mask value of enabled interrupts.

### 20.6.14 uint32\_t ENCGetPositionValue ( ENC\_Type \* *base* )

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

Current position counter's value.

### 20.6.15 uint32\_t ENCGetHoldPositionValue ( ENC\_Type \* *base* )

When any of the counter registers is read, the contents of each counter register is written to the corresponding hold register. Taking a snapshot of the counters' values provides a consistent view of a system position and a velocity to be attained.

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

Hold position counter's value.

#### **20.6.16 static uint16\_t ENC\_GetPositionDifferenceValue ( ENC\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

The position difference counter's value.

#### **20.6.17 static uint16\_t ENC\_GetHoldPositionDifferenceValue ( ENC\_Type \* *base* ) [inline], [static]**

When any of the counter registers is read, the contents of each counter register is written to the corresponding hold register. Taking a snapshot of the counters' values provides a consistent view of a system position and a velocity to be attained.

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

Hold position difference counter's value.

#### **20.6.18 static uint16\_t ENC\_GetRevolutionValue ( ENC\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

The position revolution counter's value.

#### 20.6.19 static uint16\_t ENC\_GetHoldRevolutionValue ( ENC\_Type \* *base* ) [inline], [static]

When any of the counter registers is read, the contents of each counter register is written to the corresponding hold register. Taking a snapshot of the counters' values provides a consistent view of a system position and a velocity to be attained.

Parameters

<i>base</i>	ENC peripheral base address.
-------------	------------------------------

Returns

Hold position revolution counter's value.

# Chapter 21

## ENET: Ethernet MAC Driver

### 21.1 Overview

The MCUXpresso SDK provides a peripheral driver for the 10/100 Mbps Ethernet MAC (ENET) module of MCUXpresso SDK devices.

#### ENET: Ethernet MAC Driver {EthernetMACDriver}

### 21.2 Operations of Ethernet MAC Driver

#### 21.2.1 MII interface Operation

The MII interface is the interface connected with MAC and PHY. the Serial management interface - MII management interface should be set before any access to the external PHY chip register. Call [ENET\\_SetSMI\(\)](#) to initialize the MII management interface. Use [ENET\\_StartSMIRead\(\)](#), [ENET\\_StartSMIWrite\(\)](#), and [ENET\\_ReadSMIData\(\)](#) to read/write to PHY registers. This function group sets up the MII and serial management SMI interface, gets data from the SMI interface, and starts the SMI read and write command. Use [ENET\\_SetMII\(\)](#) to configure the MII before successfully getting data from the external PHY.

#### 21.2.2 MAC address filter

This group sets/gets the ENET mac address and the multicast group address filter. [ENET\\_AddMulticastGroup\(\)](#) should be called to add the ENET MAC to the multicast group. The IEEE 1588 feature requires receiving the PTP message.

#### 21.2.3 Other Basic control Operations

This group has the receive active API [ENET\\_ActiveRead\(\)](#) for single and multiple rings. The [ENET\\_AVBConfigure\(\)](#) is provided to configure the AVB features to support the AVB frames transmission. Note that due to the AVB frames transmission scheme being a credit-based TX scheme, it is only supported with the Enhanced buffer descriptors. Because of this, the AVB configuration should only be done with the Enhanced buffer descriptor. When the AVB feature is required, make sure the the "ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE" is defined before using this feature.

#### 21.2.4 Transactional Operation

For ENET receive, the [ENET\\_GetRxFrameSize\(\)](#) function needs to be called to get the received data size. Then, call the [ENET\\_ReadFrame\(\)](#) function to get the received data. If the received error occurs, call the

`ENET_GetRxErrBeforeReadFrame()` function after `ENET_GetRxFrameSize()` and before `ENET_ReadFrame()` functions to get the detailed error information.

For ENET transmit, call the `ENET_SendFrame()` function to send the data out. The transmit data error information is only accessible for the IEEE 1588 enhanced buffer descriptor mode. When the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` is defined, the `ENET_GetTxErrAfterSendFrame()` can be used to get the detail transmit error information. The transmit error information can only be updated by uDMA after the data is transmitted. The `ENET_GetTxErrAfterSendFrame()` function is recommended to be called on the transmit interrupt handler.

If send/read frame with zero-copy mechanism is needed, there're special APIs like `ENET_GetRxFrame()` and `ENET_StartTxFrame()`. The send frame zero-copy APIs can't be used mixed with `ENET_SendFrame()` for the same ENET peripheral, same as read frame zero-copy APIs.

## 21.2.5 PTP IEEE 1588 Feature Operation

This function group configures the PTP IEEE 1588 feature, starts/stops/gets/sets/adjusts the PTP IEEE 1588 timer, gets the receive/transmit frame timestamp, and PTP IEEE 1588 timer channel feature setting.

The `ENET_Ptp1588Configure()` function needs to be called when the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` is defined and the IEEE 1588 feature is required.

## 21.3 Typical use case

### 21.3.1 ENET Initialization, receive, and transmit operations

For the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` undefined use case, use the legacy type buffer descriptor transmit/receive the frame as follows. Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/enet`. For the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` defined use case, add the PTP IEEE 1588 configuration to enable the PTP IEEE 1588 feature. The initialization occurs as follows. Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/enet`

## Modules

- [ENET CMSIS Driver](#)

## Data Structures

- struct `enet_rx_bd_struct_t`  
*Defines the receive buffer descriptor structure for the little endian system. [More...](#)*
- struct `enet_tx_bd_struct_t`  
*Defines the enhanced transmit buffer descriptor structure for the little endian system. [More...](#)*
- struct `enet_data_error_stats_t`  
*Defines the ENET data error statistics structure. [More...](#)*
- struct `enet_rx_frame_error_t`  
*Defines the Rx frame error structure. [More...](#)*

- struct `enet_transfer_stats_t`  
*Defines the ENET transfer statistics structure.* [More...](#)
- struct `enet_frame_info_t`  
*Defines the frame info structure.* [More...](#)
- struct `enet_tx_dirty_ring_t`  
*Defines the ENET transmit dirty addresses ring/queue structure.* [More...](#)
- struct `enet_buffer_config_t`  
*Defines the receive buffer descriptor configuration structure.* [More...](#)
- struct `enet_intcoalesce_config_t`  
*Defines the interrupt coalescing configure structure.* [More...](#)
- struct `enet_config_t`  
*Defines the basic configuration structure for the ENET device.* [More...](#)
- struct `enet_tx_bd_ring_t`  
*Defines the ENET transmit buffer descriptor ring/queue structure.* [More...](#)
- struct `enet_rx_bd_ring_t`  
*Defines the ENET receive buffer descriptor ring/queue structure.* [More...](#)
- struct `enet_handle_t`  
*Defines the ENET handler structure.* [More...](#)

## Macros

- #define `ENET_BUFFDESCRIPTOR_RX_ERR_MASK`  
*Defines the receive error status flag mask.*

## Typedefs

- typedef void \*(\*`enet_rx_alloc_callback_t`)(ENET\_Type \*base, void \*userData, uint8\_t ringId)  
*Defines the ENET Rx memory buffer alloc function pointer.*
- typedef void(\*`enet_rx_free_callback_t`)(ENET\_Type \*base, void \*buffer, void \*userData, uint8\_t ringId)  
*Defines the ENET Rx memory buffer free function pointer.*
- typedef void(\*`enet_callback_t`)(ENET\_Type \*base, enet\_handle\_t \*handle, enet\_event\_t event, enet\_frame\_info\_t \*frameInfo, void \*userData)  
*ENET callback function.*
- typedef void(\*`enet_isr_t`)(ENET\_Type \*base, enet\_handle\_t \*handle)  
*Define interrupt IRQ handler.*

## Enumerations

- enum {
   
`kStatus_ENET_InitMemoryFail,`  
`kStatus_ENET_RxFrameError` = MAKE\_STATUS(kStatusGroup\_ENET, 1U),  
`kStatus_ENET_RxFrameFail` = MAKE\_STATUS(kStatusGroup\_ENET, 2U),  
`kStatus_ENET_RxFrameEmpty` = MAKE\_STATUS(kStatusGroup\_ENET, 3U),  
`kStatus_ENET_RxFrameDrop` = MAKE\_STATUS(kStatusGroup\_ENET, 4U),  
`kStatus_ENET_TxFrameOverLen` = MAKE\_STATUS(kStatusGroup\_ENET, 5U),  
`kStatus_ENET_TxFrameBusy` = MAKE\_STATUS(kStatusGroup\_ENET, 6U),  
`kStatus_ENET_TxFrameFail` = MAKE\_STATUS(kStatusGroup\_ENET, 7U) }

*Defines the status return codes for transaction.*

- enum `enet_mii_mode_t` {
   
    `kENET_MiiMode` = 0U,
   
    `kENET_RmiiMode` = 1U }
   
    *Defines the MII/RMII/RGMII mode for data interface between the MAC and the PHY.*
- enum `enet_mii_speed_t` {
   
    `kENET_MiiSpeed10M` = 0U,
   
    `kENET_MiiSpeed100M` = 1U }
   
    *Defines the 10/100/1000 Mbps speed for the MII data interface.*
- enum `enet_mii_duplex_t` {
   
    `kENET_MiiHalfDuplex` = 0U,
   
    `kENET_MiiFullDuplex` }
   
    *Defines the half or full duplex for the MII data interface.*
- enum `enet_mii_write_t` {
   
    `kENET_MiiWriteNoCompliant` = 0U,
   
    `kENET_MiiWriteValidFrame` }
   
    *Define the MII opcode for normal MDIO\_CLAUSES\_22 Frame.*
- enum `enet_mii_read_t` {
   
    `kENET_MiiReadValidFrame` = 2U,
   
    `kENET_MiiReadNoCompliant` = 3U }
   
    *Defines the read operation for the MII management frame.*
- enum `enet_mii_extend_opcode` {
   
    `kENET_MiiAddrWrite_C45` = 0U,
   
    `kENET_MiiWriteFrame_C45` = 1U,
   
    `kENET_MiiReadFrame_C45` = 3U }
   
    *Define the MII opcode for extended MDIO\_CLAUSES\_45 Frame.*
- enum `enet_special_control_flag_t` {
   
    `kENET_ControlFlowControlEnable` = 0x0001U,
   
    `kENET_ControlRxPayloadCheckEnable` = 0x0002U,
   
    `kENET_ControlRxPadRemoveEnable` = 0x0004U,
   
    `kENET_ControlRxBroadCastRejectEnable` = 0x0008U,
   
    `kENET_ControlMacAddrInsert` = 0x0010U,
   
    `kENET_ControlStoreAndFwdDisable` = 0x0020U,
   
    `kENET_ControlSMIPreambleDisable` = 0x0040U,
   
    `kENET_ControlPromiscuousEnable` = 0x0080U,
   
    `kENET_ControlMIILoopEnable` = 0x0100U,
   
    `kENET_ControlVLANTagEnable` = 0x0200U }
   
    *Defines a special configuration for ENET MAC controller.*
- enum `enet_interrupt_enable_t` {

```

kENET_BabrInterrupt = ENET_EIR_BABR_MASK,
kENET_BabtInterrupt = ENET_EIR_BABT_MASK,
kENET_GraceStopInterrupt = ENET_EIR_GRA_MASK,
kENET_TxFrameInterrupt = ENET_EIR_TXF_MASK,
kENET_TxBufferInterrupt = ENET_EIR_TXB_MASK,
kENET_RxFrameInterrupt = ENET_EIR_RXF_MASK,
kENET_RxBufferInterrupt = ENET_EIR_RXB_MASK,
kENET_MiiInterrupt = ENET_EIR_MII_MASK,
kENET_EBusERInterrupt = ENET_EIR_EBERR_MASK,
kENET_LateCollisionInterrupt = ENET_EIR_LC_MASK,
kENET_RetryLimitInterrupt = ENET_EIR_RL_MASK,
kENET_UnderrunInterrupt = ENET_EIR_UN_MASK,
kENET_PayloadRxInterrupt = ENET_EIR_PLR_MASK,
kENET_WakeupInterrupt = ENET_EIR_WAKEUP_MASK,
kENET_TsAvailInterrupt = ENET_EIR_TS_AVAIL_MASK,
kENET_TsTimerInterrupt = ENET_EIR_TS_TIMER_MASK }

```

*List of interrupts supported by the peripheral.*

- enum `enet_event_t` {
   
kENET\_RxEvent,  
kENET\_TxEvent,  
kENET\_ErrEvent,  
kENET\_WakeUpEvent,  
kENET\_TimeStampEvent,  
kENET\_TimeStampAvailEvent }

*Defines the common interrupt event for callback use.*

- enum `enet_tx_accelerator_t` {
   
kENET\_TxAccelIsShift16Enabled = ENET\_TACC\_SHIFT16\_MASK,  
kENET\_TxAccelIpCheckEnabled = ENET\_TACC\_IPCHK\_MASK,  
kENET\_TxAccelProtoCheckEnabled = ENET\_TACC\_PROCHK\_MASK }

*Defines the transmit accelerator configuration.*

- enum `enet_rx_accelerator_t` {
   
kENET\_RxAccelPadRemoveEnabled = ENET\_RACC\_PADREM\_MASK,  
kENET\_RxAccelIpCheckEnabled = ENET\_RACC\_IPDIS\_MASK,  
kENET\_RxAccelProtoCheckEnabled = ENET\_RACC\_PRODIS\_MASK,  
kENET\_RxAccelMacCheckEnabled = ENET\_RACC\_LINEDIS\_MASK,  
kENET\_RxAccelIsShift16Enabled = ENET\_RACC\_SHIFT16\_MASK }

*Defines the receive accelerator configuration.*

## Functions

- `uint32_t ENET_GetInstance (ENET_Type *base)`  
*Get the ENET instance from peripheral base address.*

## Variables

- const `clock_ip_name_t s_enetClock []`  
*Pointers to enet clocks for each instance.*

## Driver version

- `#define FSL_ENET_DRIVER_VERSION (MAKE_VERSION(2, 7, 0))`  
*Defines the driver version.*

## Control and status region bit masks of the receive buffer descriptor.

Defines the queue number.

- `#define ENET_BUFFDESCRIPTOR_RX_EMPTY_MASK 0x8000U`  
*Empty bit mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_SOFTOWNER1_MASK 0x4000U`  
*Software owner one mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_WRAP_MASK 0x2000U`  
*Next buffer descriptor is the start address.*
- `#define ENET_BUFFDESCRIPTOR_RX_SOFTOWNER2_MASK 0x1000U`  
*Software owner two mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_LAST_MASK 0x0800U`  
*Last BD of the frame mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_MISS_MASK 0x0100U`  
*Received because of the promiscuous mode.*
- `#define ENET_BUFFDESCRIPTOR_RX_BROADCAST_MASK 0x0080U`  
*Broadcast packet mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_MULTICAST_MASK 0x0040U`  
*Multicast packet mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_LENVLIOLATE_MASK 0x0020U`  
*Length violation mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_NOOCTET_MASK 0x0010U`  
*Non-octet aligned frame mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_CRC_MASK 0x0004U`  
*CRC error mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_OVERRUN_MASK 0x0002U`  
*FIFO overrun mask.*
- `#define ENET_BUFFDESCRIPTOR_RX_TRUNC_MASK 0x0001U`  
*Frame is truncated mask.*

## Control and status bit masks of the transmit buffer descriptor.

- `#define ENET_BUFFDESCRIPTOR_TX_READY_MASK 0x8000U`  
*Ready bit mask.*
- `#define ENET_BUFFDESCRIPTOR_TX_SOFTOWNER1_MASK 0x4000U`  
*Software owner one mask.*
- `#define ENET_BUFFDESCRIPTOR_TX_WRAP_MASK 0x2000U`  
*Wrap buffer descriptor mask.*
- `#define ENET_BUFFDESCRIPTOR_TX_SOFTOWNER2_MASK 0x1000U`  
*Software owner two mask.*
- `#define ENET_BUFFDESCRIPTOR_TX_LAST_MASK 0x0800U`  
*Last BD of the frame mask.*
- `#define ENET_BUFFDESCRIPTOR_TX_TRANSMITCRC_MASK 0x0400U`  
*Transmit CRC mask.*

## Defines some Ethernet parameters.

- #define ENET\_FRAME\_MAX\_FRAMELEN 1518U  
*Default maximum Ethernet frame size without VLAN tag.*
- #define ENET\_FRAME\_VLAN\_TAGLEN 4U  
*Ethernet single VLAN tag size.*
- #define ENET\_FRAME\_CRC\_LEN 4U  
*CRC size in a frame.*
- #define ENET\_FRAME\_TX\_LEN\_LIMITATION(x) (((x)->RCR & ENET\_RCR\_MAX\_FL\_MASK) >> ENET\_RCR\_MAX\_FL\_SHIFT) - ENET\_FRAME\_CRC\_LEN)
- #define ENET\_FIFO\_MIN\_RX\_FULL 5U  
*ENET minimum receive FIFO full.*
- #define ENET\_RX\_MIN\_BUFFERSIZE 256U  
*ENET minimum buffer size.*
- #define ENET\_PHY\_MAXADDRESS (ENET\_MMFR\_PA\_MASK >> ENET\_MMFR\_PA\_SHIFT)  
*Maximum PHY address.*
- #define ENET\_TX\_INTERRUPT ((uint32\_t)kENET\_TxFrameInterrupt | (uint32\_t)kENET\_TxBufferInterrupt)  
*Enet Tx interrupt flag.*
- #define ENET\_RX\_INTERRUPT ((uint32\_t)kENET\_RxFrameInterrupt | (uint32\_t)kENET\_RxBufferInterrupt)  
*Enet Rx interrupt flag.*
- #define ENET\_TS\_INTERRUPT ((uint32\_t)kENET\_TsTimerInterrupt | (uint32\_t)kENET\_TsAvailInterrupt)  
*Enet timestamp interrupt flag.*
- #define ENET\_ERR\_INTERRUPT  
*Enet error interrupt flag.*

## Initialization and De-initialization

- void ENET\_GetDefaultConfig (enet\_config\_t \*config)  
*Gets the ENET default configuration structure.*
- status\_t ENET\_Up (ENET\_Type \*base, enet\_handle\_t \*handle, const enet\_config\_t \*config, const enet\_buffer\_config\_t \*bufferConfig, uint8\_t \*macAddr, uint32\_t srcClock\_Hz)  
*Initializes the ENET module.*
- status\_t ENET\_Init (ENET\_Type \*base, enet\_handle\_t \*handle, const enet\_config\_t \*config, const enet\_buffer\_config\_t \*bufferConfig, uint8\_t \*macAddr, uint32\_t srcClock\_Hz)  
*Initializes the ENET module.*
- void ENET\_Down (ENET\_Type \*base)  
*Stops the ENET module.*
- void ENET\_Deinit (ENET\_Type \*base)  
*Deinitializes the ENET module.*
- static void ENET\_Reset (ENET\_Type \*base)  
*Resets the ENET module.*

## MII interface operation

- void ENET\_SetMII (ENET\_Type \*base, enet\_mii\_speed\_t speed, enet\_mii\_duplex\_t duplex)  
*Sets the ENET MII speed and duplex.*

- void **ENET\_SetSMI** (ENET\_Type \*base, uint32\_t srcClock\_Hz, bool isPreambleDisabled)
 

*Sets the ENET SMI(serial management interface)- MII management interface.*
- static bool **ENET\_GetSMI** (ENET\_Type \*base)
 

*Gets the ENET SMI- MII management interface configuration.*
- static uint32\_t **ENET\_ReadSMIData** (ENET\_Type \*base)
 

*Reads data from the PHY register through an SMI interface.*
- static void **ENET\_StartSMIWrite** (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, **enet\_mii-write\_t** operation, uint16\_t data)
 

*Sends the MDIO IEEE802.3 Clause 22 format write command.*
- static void **ENET\_StartSMIRead** (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, **enet\_mii-read\_t** operation)
 

*Sends the MDIO IEEE802.3 Clause 22 format read command.*
- status\_t **ENET\_MDIOWrite** (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, uint16\_t data)
 

*MDIO write with IEEE802.3 Clause 22 format.*
- status\_t **ENET\_MDIORead** (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, uint16\_t \*pData)
 

*MDIO read with IEEE802.3 Clause 22 format.*
- static void **ENET\_StartExtC45SMIWriteReg** (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t regAddr)
 

*Sends the MDIO IEEE802.3 Clause 45 format write register command.*
- static void **ENET\_StartExtC45SMIWriteData** (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t data)
 

*Sends the MDIO IEEE802.3 Clause 45 format write data command.*
- static void **ENET\_StartExtC45SMIReadData** (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr)
 

*Sends the MDIO IEEE802.3 Clause 45 format read data command.*
- status\_t **ENET\_MDIOC45Write** (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t regAddr, uint16\_t data)
 

*MDIO write with IEEE802.3 Clause 45 format.*
- status\_t **ENET\_MDIOC45Read** (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t regAddr, uint16\_t \*pData)
 

*MDIO read with IEEE802.3 Clause 45 format.*

## MAC Address Filter

- void **ENET\_SetMacAddr** (ENET\_Type \*base, uint8\_t \*macAddr)
 

*Sets the ENET module Mac address.*
- void **ENET\_GetMacAddr** (ENET\_Type \*base, uint8\_t \*macAddr)
 

*Gets the ENET module Mac address.*
- void **ENET\_AddMulticastGroup** (ENET\_Type \*base, uint8\_t \*address)
 

*Adds the ENET device to a multicast group.*
- void **ENET\_LeaveMulticastGroup** (ENET\_Type \*base, uint8\_t \*address)
 

*Moves the ENET device from a multicast group.*

## Other basic operation

- static void **ENET\_ActiveRead** (ENET\_Type \*base)
 

*Activates frame reception for multiple rings.*
- static void **ENET\_EnableSleepMode** (ENET\_Type \*base, bool enable)
 

*Enables/disables the MAC to enter sleep mode.*

- static void [ENET\\_GetAccelFunction](#) (ENET\_Type \*base, uint32\_t \*txAccelOption, uint32\_t \*rxAccelOption)

*Gets ENET transmit and receive accelerator functions from MAC controller.*

## Interrupts.

- static void [ENET\\_EnableInterrupts](#) (ENET\_Type \*base, uint32\_t mask)  
*Enables the ENET interrupt.*
- static void [ENET\\_DisableInterrupts](#) (ENET\_Type \*base, uint32\_t mask)  
*Disables the ENET interrupt.*
- static uint32\_t [ENET\\_GetInterruptStatus](#) (ENET\_Type \*base)  
*Gets the ENET interrupt status flag.*
- static void [ENET\\_ClearInterruptStatus](#) (ENET\_Type \*base, uint32\_t mask)  
*Clears the ENET interrupt events status flag.*
- void [ENET\\_SetRxISRHandler](#) (ENET\_Type \*base, enet\_isr\_t ISRHandler)  
*Set the second level Rx IRQ handler.*
- void [ENET\\_SetTxISRHandler](#) (ENET\_Type \*base, enet\_isr\_t ISRHandler)  
*Set the second level Tx IRQ handler.*
- void [ENET\\_SetErrISRHandler](#) (ENET\_Type \*base, enet\_isr\_t ISRHandler)  
*Set the second level Err IRQ handler.*

## Transactional operation

- void [ENET\\_GetRxErrBeforeReadFrame](#) (enet\_handle\_t \*handle, enet\_data\_error\_stats\_t \*eErrorStatic, uint8\_t ringId)  
*Gets the error statistics of a received frame for ENET specified ring.*
- void [ENET\\_GetStatistics](#) (ENET\_Type \*base, enet\_transfer\_stats\_t \*statistics)  
*Gets statistical data in transfer.*
- status\_t [ENET\\_GetRxFrameSize](#) (enet\_handle\_t \*handle, uint32\_t \*length, uint8\_t ringId)  
*Gets the size of the read frame for specified ring.*
- status\_t [ENET\\_ReadFrame](#) (ENET\_Type \*base, enet\_handle\_t \*handle, uint8\_t \*data, uint32\_t length, uint8\_t ringId, uint32\_t \*ts)  
*Reads a frame from the ENET device.*
- status\_t [ENET\\_SendFrame](#) (ENET\_Type \*base, enet\_handle\_t \*handle, const uint8\_t \*data, uint32\_t length, uint8\_t ringId, bool tsFlag, void \*context)  
*Transmits an ENET frame for specified ring.*
- status\_t [ENET\\_SetTxReclaim](#) (enet\_handle\_t \*handle, bool isEnabled, uint8\_t ringId)  
*Enable or disable tx descriptors reclaim mechanism.*
- void [ENET\\_ReclaimTxDescriptor](#) (ENET\_Type \*base, enet\_handle\_t \*handle, uint8\_t ringId)  
*Reclaim tx descriptors.*
- status\_t [ENET\\_GetRxFrame](#) (ENET\_Type \*base, enet\_handle\_t \*handle, enet\_rx\_frame\_struct\_t \*rxFrame, uint8\_t ringId)  
*Receives one frame in specified BD ring with zero copy.*
- status\_t [ENET\\_StartTxFrame](#) (ENET\_Type \*base, enet\_handle\_t \*handle, enet\_tx\_frame\_struct\_t \*txFrame, uint8\_t ringId)  
*Sends one frame in specified BD ring with zero copy.*
- void [ENET\\_TransmitIRQHandler](#) (ENET\_Type \*base, enet\_handle\_t \*handle)  
*The transmit IRQ handler.*
- void [ENET\\_ReceiveIRQHandler](#) (ENET\_Type \*base, enet\_handle\_t \*handle)  
*The receive IRQ handler.*

- void [ENET\\_ErrorIRQHandler](#) (ENET\_Type \*base, enet\_handle\_t \*handle)  
*Some special IRQ handler including the error, mii, wakeup irq handler.*
- void [ENET\\_Ptp1588IRQHandler](#) (ENET\_Type \*base)  
*the common IRQ handler for the 1588 irq handler.*
- void [ENET\\_CommonFrame0IRQHandler](#) (ENET\_Type \*base)  
*the common IRQ handler for the tx/rx/error etc irq handler.*

## 21.4 Data Structure Documentation

### 21.4.1 struct enet\_rx\_bd\_struct\_t

#### Data Fields

- uint16\_t **length**  
*Buffer descriptor data length.*
- uint16\_t **control**  
*Buffer descriptor control and status.*
- uint32\_t **buffer**  
*Data buffer pointer.*

#### Field Documentation

- (1) `uint16_t enet_rx_bd_struct_t::length`
- (2) `uint16_t enet_rx_bd_struct_t::control`
- (3) `uint32_t enet_rx_bd_struct_t::buffer`

### 21.4.2 struct enet\_tx\_bd\_struct\_t

#### Data Fields

- uint16\_t **length**  
*Buffer descriptor data length.*
- uint16\_t **control**  
*Buffer descriptor control and status.*
- uint32\_t **buffer**  
*Data buffer pointer.*

**Field Documentation**

- (1) `uint16_t enet_tx_bd_struct_t::length`
- (2) `uint16_t enet_tx_bd_struct_t::control`
- (3) `uint32_t enet_tx_bd_struct_t::buffer`

**21.4.3 struct enet\_data\_error\_stats\_t****Data Fields**

- `uint32_t statsRxLenGreaterErr`  
*Receive length greater than RCR[MAX\_FL].*
- `uint32_t statsRxAlignErr`  
*Receive non-octet alignment.*
- `uint32_t statsRxFcsErr`  
*Receive CRC error.*
- `uint32_t statsRxOverRunErr`  
*Receive over run.*
- `uint32_t statsRxTruncateErr`  
*Receive truncate.*

**Field Documentation**

- (1) `uint32_t enet_data_error_stats_t::statsRxLenGreaterErr`
- (2) `uint32_t enet_data_error_stats_t::statsRxFcsErr`
- (3) `uint32_t enet_data_error_stats_t::statsRxOverRunErr`
- (4) `uint32_t enet_data_error_stats_t::statsRxTruncateErr`

**21.4.4 struct enet\_rx\_frame\_error\_t****Data Fields**

- `bool statsRxTruncateErr: 1`  
*Receive truncate.*
- `bool statsRxOverRunErr: 1`  
*Receive over run.*
- `bool statsRxFcsErr: 1`  
*Receive CRC error.*
- `bool statsRxAlignErr: 1`  
*Receive non-octet alignment.*
- `bool statsRxLenGreaterErr: 1`  
*Receive length greater than RCR[MAX\_FL].*

## Field Documentation

- (1) **bool enet\_rx\_frame\_error\_t::statsRxTruncateErr**
- (2) **bool enet\_rx\_frame\_error\_t::statsRxOverRunErr**
- (3) **bool enet\_rx\_frame\_error\_t::statsRxFcsErr**
- (4) **bool enet\_rx\_frame\_error\_t::statsRxAlignErr**
- (5) **bool enet\_rx\_frame\_error\_t::statsRxLenGreaterErr**

### 21.4.5 struct enet\_transfer\_stats\_t

#### Data Fields

- **uint32\_t statsRxFrameCount**  
*Rx frame number.*
- **uint32\_t statsRxFrameOk**  
*Good Rx frame number.*
- **uint32\_t statsRxCrcErr**  
*Rx frame number with CRC error.*
- **uint32\_t statsRxAlignErr**  
*Rx frame number with alignment error.*
- **uint32\_t statsRxDropInvalidSFD**  
*Dropped frame number due to invalid SFD.*
- **uint32\_t statsRxFifoOverflowErr**  
*Rx FIFO overflow count.*
- **uint32\_t statsTxFrameCount**  
*Tx frame number.*
- **uint32\_t statsTxFrameOk**  
*Good Tx frame number.*
- **uint32\_t statsTxCrcAlignErr**  
*The transmit frame is error.*
- **uint32\_t statsTxFifoUnderRunErr**  
*Tx FIFO underrun count.*

**Field Documentation**

- (1) `uint32_t enet_transfer_stats_t::statsRxFrameCount`
- (2) `uint32_t enet_transfer_stats_t::statsRxFrameOk`
- (3) `uint32_t enet_transfer_stats_t::statsRxCrcErr`
- (4) `uint32_t enet_transfer_stats_t::statsRxAlignErr`
- (5) `uint32_t enet_transfer_stats_t::statsRxDropInvalidSFD`
- (6) `uint32_t enet_transfer_stats_t::statsRxFifoOverflowErr`
- (7) `uint32_t enet_transfer_stats_t::statsTxFrameCount`
- (8) `uint32_t enet_transfer_stats_t::statsTxFrameOk`
- (9) `uint32_t enet_transfer_stats_t::statsTxCrcAlignErr`
- (10) `uint32_t enet_transfer_stats_t::statsTxFifoUnderRunErr`

**21.4.6 struct enet\_frame\_info\_t****Data Fields**

- `void * context`  
*User specified data.*

**21.4.7 struct enet\_tx\_dirty\_ring\_t****Data Fields**

- `enet_frame_info_t * txDirtyBase`  
*Dirty buffer descriptor base address pointer.*
- `uint16_t txGenIdx`  
*tx generate index.*
- `uint16_t txConsumIdx`  
*tx consume index.*
- `uint16_t txRingLen`  
*tx ring length.*
- `bool isFull`  
*tx ring is full flag.*

**Field Documentation**

- (1) `enet_frame_info_t* enet_tx_dirty_ring_t::txDirtyBase`
- (2) `uint16_t enet_tx_dirty_ring_t::txGenIdx`
- (3) `uint16_t enet_tx_dirty_ring_t::txConsumIdx`
- (4) `uint16_t enet_tx_dirty_ring_t::txRingLen`
- (5) `bool enet_tx_dirty_ring_t::isFull`

**21.4.8 struct enet\_buffer\_config\_t**

Note that for the internal DMA requirements, the buffers have a corresponding alignment requirements.

1. The aligned receive and transmit buffer size must be evenly divisible by ENET\_BUFF\_ALIGNMENT. when the data buffers are in cacheable region when cache is enabled, all those size should be aligned to the maximum value of "ENET\_BUFF\_ALIGNMENT" and the cache line size.
2. The aligned transmit and receive buffer descriptor start address must be at least 64 bit aligned. However, it's recommended to be evenly divisible by ENET\_BUFF\_ALIGNMENT. buffer descriptors should be put in non-cacheable region when cache is enabled.
3. The aligned transmit and receive data buffer start address must be evenly divisible by ENET\_BUFF\_ALIGNMENT. Receive buffers should be continuous with the total size equal to "rxBdNumber \* rxBuffSizeAlign". Transmit buffers should be continuous with the total size equal to "txBdNumber \* txBuffSizeAlign". when the data buffers are in cacheable region when cache is enabled, all those size should be aligned to the maximum value of "ENET\_BUFF\_ALIGNMENT" and the cache line size.

**Data Fields**

- `uint16_t rxBdNumber`  
*Receive buffer descriptor number.*
- `uint16_t txBdNumber`  
*Transmit buffer descriptor number.*
- `uint16_t rxBuffSizeAlign`  
*Aligned receive data buffer size.*
- `uint16_t txBuffSizeAlign`  
*Aligned transmit data buffer size.*
- `volatile enet_rx_bd_struct_t * rxBdStartAddrAlign`  
*Aligned receive buffer descriptor start address: should be non-cacheable.*
- `volatile enet_tx_bd_struct_t * txBdStartAddrAlign`  
*Aligned transmit buffer descriptor start address: should be non-cacheable.*
- `uint8_t * rxBufferAlign`  
*Receive data buffer start address.*
- `uint8_t * txBufferAlign`  
*Transmit data buffer start address.*
- `bool rxMaintainEnable`

- *Receive buffer cache maintain.*
- **bool txMaintainEnable**  
*Transmit buffer cache maintain.*
- **enet\_frame\_info\_t \* txFrameInfo**  
*Transmit frame information start address.*

## Field Documentation

- (1) **uint16\_t enet\_buffer\_config\_t::rxBdNumber**
- (2) **uint16\_t enet\_buffer\_config\_t::txBdNumber**
- (3) **uint16\_t enet\_buffer\_config\_t::rxBuffSizeAlign**
- (4) **uint16\_t enet\_buffer\_config\_t::txBuffSizeAlign**
- (5) **volatile enet\_rx\_bd\_struct\_t\* enet\_buffer\_config\_t::rxBdStartAddrAlign**
- (6) **volatile enet\_tx\_bd\_struct\_t\* enet\_buffer\_config\_t::txBdStartAddrAlign**
- (7) **uint8\_t\* enet\_buffer\_config\_t::rxBufferAlign**
- (8) **uint8\_t\* enet\_buffer\_config\_t::txBufferAlign**
- (9) **bool enet\_buffer\_config\_t::rxMaintainEnable**
- (10) **bool enet\_buffer\_config\_t::txMaintainEnable**
- (11) **enet\_frame\_info\_t\* enet\_buffer\_config\_t::txFrameInfo**

### 21.4.9 struct enet\_intcoalesce\_config\_t

## Data Fields

- **uint8\_t txCoalesceFrameCount [FSL\_FEATURE\_ENET\_QUEUE]**  
*Transmit interrupt coalescing frame count threshold.*
- **uint16\_t txCoalesceTimeCount [FSL\_FEATURE\_ENET\_QUEUE]**  
*Transmit interrupt coalescing timer count threshold.*
- **uint8\_t rxCoalesceFrameCount [FSL\_FEATURE\_ENET\_QUEUE]**  
*Receive interrupt coalescing frame count threshold.*
- **uint16\_t rxCoalesceTimeCount [FSL\_FEATURE\_ENET\_QUEUE]**  
*Receive interrupt coalescing timer count threshold.*

**Field Documentation**

- (1) `uint8_t enet_intcoalesce_config_t::txCoalesceFrameCount[FSL_FEATURE_ENET_QUEUE]`
- (2) `uint16_t enet_intcoalesce_config_t::txCoalesceTimeCount[FSL_FEATURE_ENET_QUEUE]`
- (3) `uint8_t enet_intcoalesce_config_t::rxCoalesceFrameCount[FSL_FEATURE_ENET_QUEUE]`
- (4) `uint16_t enet_intcoalesce_config_t::rxCoalesceTimeCount[FSL_FEATURE_ENET_QUEUE]`

**21.4.10 struct enet\_config\_t**

Note:

1. macSpecialConfig is used for a special control configuration, A logical OR of "enet\_special\_control\_flag\_t". For a special configuration for MAC, set this parameter to 0.
2. txWatermark is used for a cut-through operation. It is in steps of 64 bytes: 0/1 - 64 bytes written to TX FIFO before transmission of a frame begins. 2 - 128 bytes written to TX FIFO .... 3 - 192 bytes written to TX FIFO .... The maximum of txWatermark is 0x2F - 4032 bytes written to TX FIFO .... txWatermark allows minimizing the transmit latency to set the txWatermark to 0 or 1 or for larger bus access latency 3 or larger due to contention for the system bus.
3. rxFifoFullThreshold is similar to the txWatermark for cut-through operation in RX. It is in 64-bit words. The minimum is ENET\_FIFO\_MIN\_RX\_FULL and the maximum is 0xFF. If the end of the frame is stored in FIFO and the frame size if smaller than the txWatermark, the frame is still transmitted. The rule is the same for rxFifoFullThreshold in the receive direction.
4. When "kENET\_ControlFlowControlEnable" is set in the macSpecialConfig, ensure that the pauseDuration, rxFifoEmptyThreshold, and rxFifoStatEmptyThreshold are set for flow control enabled case.
5. When "kENET\_ControlStoreAndFwdDisabled" is set in the macSpecialConfig, ensure that the rxFifoFullThreshold and txFifoWatermark are set for store and forward disable.
6. The rxAccelerConfig and txAccelerConfig default setting with 0 - accelerator are disabled. The "enet\_tx\_accelerator\_t" and "enet\_rx\_accelerator\_t" are recommended to be used to enable the transmit and receive accelerator. After the accelerators are enabled, the store and forward feature should be enabled. As a result, kENET\_ControlStoreAndFwdDisabled should not be set.
7. The intCoalesceCfg can be used in the rx or tx enabled cases to decrease the CPU loading.

**Data Fields**

- `uint32_t macSpecialConfig`  
*Mac special configuration.*
- `uint32_t interrupt`  
*Mac interrupt source.*
- `uint16_t rxMaxFrameLen`  
*Receive maximum frame length.*
- `enet_mii_mode_t miiMode`  
*MII mode.*
- `enet_mii_speed_t miiSpeed`

- **`enet_mii_duplex_t miiDuplex`**  
*MII Speed.*
- **`uint8_t rxAccelerConfig`**  
*Receive accelerator; A logical OR of "enet\_rx\_accelerator\_t".*
- **`uint8_t txAccelerConfig`**  
*Transmit accelerator; A logical OR of "enet\_rx\_accelerator\_t".*
- **`uint16_t pauseDuration`**  
*For flow control enabled case: Pause duration.*
- **`uint8_t rxFifoEmptyThreshold`**  
*For flow control enabled case: when RX FIFO level reaches this value, it makes MAC generate XOFF pause frame.*
- **`uint8_t rxFifoStatEmptyThreshold`**  
*For flow control enabled case: number of frames in the receive FIFO, independent of size, that can be accept.*
- **`uint8_t rxFifoFullThreshold`**  
*For store and forward disable case, the data required in RX FIFO to notify the MAC receive ready status.*
- **`uint8_t txFifoWatermark`**  
*For store and forward disable case, the data required in TX FIFO before a frame transmit start.*
- **`enet_intcoalesce_config_t * intCoalesceCfg`**  
*If the interrupt coalesce is not required in the ring n(0,1,2), please set to NULL.*
- **`uint8_t ringNum`**  
*Number of used rings.*
- **`enet_rx_alloc_callback_t rxBuffAlloc`**  
*Callback function to alloc memory, must be provided for zero-copy Rx.*
- **`enet_rx_free_callback_t rxBuffFree`**  
*Callback function to free memory, must be provided for zero-copy Rx.*
- **`enet_callback_t callback`**  
*General callback function.*
- **`void * userData`**  
*Callback function parameter.*

## Field Documentation

### (1) `uint32_t enet_config_t::macSpecialConfig`

A logical OR of "enet\_special\_control\_flag\_t".

### (2) `uint32_t enet_config_t::interrupt`

A logical OR of "enet\_interrupt\_enable\_t".

- (3) `uint16_t enet_config_t::rxMaxFrameLen`
- (4) `enet_mii_mode_t enet_config_t::miiMode`
- (5) `enet_mii_speed_t enet_config_t::miiSpeed`
- (6) `enet_mii_duplex_t enet_config_t::miiDuplex`
- (7) `uint8_t enet_config_t::rxAccelerConfig`
- (8) `uint8_t enet_config_t::txAccelerConfig`
- (9) `uint16_t enet_config_t::pauseDuration`
- (10) `uint8_t enet_config_t::rxFifoEmptyThreshold`
- (11) `uint8_t enet_config_t::rxFifoStatEmptyThreshold`

If the limit is reached, reception continues and a pause frame is triggered.

- (12) `uint8_t enet_config_t::rxFifoFullThreshold`
- (13) `uint8_t enet_config_t::txFifoWatermark`
- (14) `enet_intcoalesce_config_t* enet_config_t::intCoalesceCfg`
- (15) `uint8_t enet_config_t::ringNum`

default with 1 – single ring.

- (16) `enet_rx_alloc_callback_t enet_config_t::rxBuffAlloc`
- (17) `enet_rx_free_callback_t enet_config_t::rxBuffFree`
- (18) `enet_callback_t enet_config_t::callback`
- (19) `void* enet_config_t::userData`

#### 21.4.11 struct enet\_tx\_bd\_ring\_t

### Data Fields

- volatile `enet_tx_bd_struct_t * txBdBase`  
*Buffer descriptor base address pointer.*
- `uint16_t txGenIdx`  
*The current available transmit buffer descriptor pointer.*
- `uint16_t txConsumIdx`  
*Transmit consume index.*
- volatile `uint16_t txDescUsed`  
*Transmit descriptor used number.*

- `uint16_t txRingLen`  
*Transmit ring length.*

**Field Documentation**

- (1) `volatile enet_tx_bd_struct_t* enet_tx_bd_ring_t::txBdBase`
- (2) `uint16_t enet_tx_bd_ring_t::txGenIdx`
- (3) `uint16_t enet_tx_bd_ring_t::txConsumIdx`
- (4) `volatile uint16_t enet_tx_bd_ring_t::txDescUsed`
- (5) `uint16_t enet_tx_bd_ring_t::txRingLen`

**21.4.12 struct enet\_rx\_bd\_ring\_t****Data Fields**

- `volatile enet_rx_bd_struct_t * rxBdBase`  
*Buffer descriptor base address pointer.*
- `uint16_t rxGenIdx`  
*The current available receive buffer descriptor pointer.*
- `uint16_t rxRingLen`  
*Receive ring length.*

**Field Documentation**

- (1) `volatile enet_rx_bd_struct_t* enet_rx_bd_ring_t::rxBdBase`
- (2) `uint16_t enet_rx_bd_ring_t::rxGenIdx`
- (3) `uint16_t enet_rx_bd_ring_t::rxRingLen`

**21.4.13 struct \_enet\_handle****Data Fields**

- `enet_rx_bd_ring_t rxBdRing` [FSL\_FEATURE\_ENET\_QUEUE]  
*Receive buffer descriptor.*
- `enet_tx_bd_ring_t txBdRing` [FSL\_FEATURE\_ENET\_QUEUE]  
*Transmit buffer descriptor.*
- `uint16_t rxBuffSizeAlign` [FSL\_FEATURE\_ENET\_QUEUE]  
*Receive buffer size alignment.*
- `uint16_t txBuffSizeAlign` [FSL\_FEATURE\_ENET\_QUEUE]  
*Transmit buffer size alignment.*
- `bool rxMaintainEnable` [FSL\_FEATURE\_ENET\_QUEUE]  
*Receive buffer cache maintain.*
- `bool txMaintainEnable` [FSL\_FEATURE\_ENET\_QUEUE]

- *Transmit buffer cache maintain.*
- **uint8\_t ringNum**  
*Number of used rings.*
- **enet\_callback\_t callback**  
*Callback function.*
- **void \* userData**  
*Callback function parameter.*
- **enet\_tx\_dirty\_ring\_t txDirtyRing** [FSL\_FEATURE\_ENET\_QUEUE]  
*Ring to store tx frame information.*
- **bool txReclaimEnable** [FSL\_FEATURE\_ENET\_QUEUE]  
*Tx reclaim enable flag.*
- **enet\_rx\_alloc\_callback\_t rxBuffAlloc**  
*Callback function to alloc memory for zero copy Rx.*
- **enet\_rx\_free\_callback\_t rxBuffFree**  
*Callback function to free memory for zero copy Rx.*
- **uint8\_t multicastCount** [64]  
*Multicast collisions counter.*

## Field Documentation

- (1) **enet\_rx\_bd\_ring\_t enet\_handle\_t::rxBdRing** [FSL\_FEATURE\_ENET\_QUEUE]
- (2) **enet\_tx\_bd\_ring\_t enet\_handle\_t::txBdRing** [FSL\_FEATURE\_ENET\_QUEUE]
- (3) **uint16\_t enet\_handle\_t::rxBuffSizeAlign** [FSL\_FEATURE\_ENET\_QUEUE]
- (4) **uint16\_t enet\_handle\_t::txBuffSizeAlign** [FSL\_FEATURE\_ENET\_QUEUE]
- (5) **bool enet\_handle\_t::rxMaintainEnable** [FSL\_FEATURE\_ENET\_QUEUE]
- (6) **bool enet\_handle\_t::txMaintainEnable** [FSL\_FEATURE\_ENET\_QUEUE]
- (7) **uint8\_t enet\_handle\_t::ringNum**
- (8) **enet\_callback\_t enet\_handle\_t::callback**
- (9) **void\* enet\_handle\_t::userData**
- (10) **enet\_tx\_dirty\_ring\_t enet\_handle\_t::txDirtyRing** [FSL\_FEATURE\_ENET\_QUEUE]
- (11) **bool enet\_handle\_t::txReclaimEnable** [FSL\_FEATURE\_ENET\_QUEUE]
- (12) **enet\_rx\_alloc\_callback\_t enet\_handle\_t::rxBuffAlloc**
- (13) **enet\_rx\_free\_callback\_t enet\_handle\_t::rxBuffFree**

## 21.5 Macro Definition Documentation

- 21.5.1 `#define FSL_ENET_DRIVER_VERSION (MAKE_VERSION(2, 7, 0))`
- 21.5.2 `#define ENET_BUFFDESCRIPTOR_RX_EMPTY_MASK 0x8000U`
- 21.5.3 `#define ENET_BUFFDESCRIPTOR_RX_SOFTOWNER1_MASK 0x4000U`
- 21.5.4 `#define ENET_BUFFDESCRIPTOR_RX_WRAP_MASK 0x2000U`
- 21.5.5 `#define ENET_BUFFDESCRIPTOR_RX_SOFTOWNER2_Mask 0x1000U`
- 21.5.6 `#define ENET_BUFFDESCRIPTOR_RX_LAST_MASK 0x0800U`
- 21.5.7 `#define ENET_BUFFDESCRIPTOR_RX_MISS_MASK 0x0100U`
- 21.5.8 `#define ENET_BUFFDESCRIPTOR_RX_BROADCAST_MASK 0x0080U`
- 21.5.9 `#define ENET_BUFFDESCRIPTOR_RX_MULTICAST_MASK 0x0040U`
- 21.5.10 `#define ENET_BUFFDESCRIPTOR_RX_LENVIOLATE_MASK 0x0020U`
- 21.5.11 `#define ENET_BUFFDESCRIPTOR_RX_NOOCTET_MASK 0x0010U`
- 21.5.12 `#define ENET_BUFFDESCRIPTOR_RX_CRC_MASK 0x0004U`
- 21.5.13 `#define ENET_BUFFDESCRIPTOR_RX_OVERRUN_MASK 0x0002U`
- 21.5.14 `#define ENET_BUFFDESCRIPTOR_RX_TRUNC_MASK 0x0001U`
- 21.5.15 `#define ENET_BUFFDESCRIPTOR_TX_READY_MASK 0x8000U`
- 21.5.16 `#define ENET_BUFFDESCRIPTOR_TX_SOFTOWENER1_MASK 0x4000U`
- 21.5.17 `#define ENET_BUFFDESCRIPTOR_TX_WRAP_MASK 0x2000U`
- 21.5.18 `#define ENET_BUFFDESCRIPTOR_TX_SOFTOWENER2_MASK 0x1000U`
- 21.5.19 `#define ENET_BUFFDESCRIPTOR_TX_LAST_MASK 0x0800U`
- 21.5.20 ~~`#define ENET_BUFFDESCRIPTOR_TX_TRANMITCRC_MASK 0x0400U`~~
- 21.5.21 `#define ENET_BUFFDESCRIPTOR_RX_ERR_MASK`

```
(ENET_BUFFDESCRIPTOR_RX_TRUNC_MASK |
 ENET_BUFFDESCRIPTOR_RX_OVERRUN_MASK | \
 ENET_BUFFDESCRIPTOR_RX_LENVLIOLATE_MASK |
 ENET_BUFFDESCRIPTOR_RX_NOOCTET_MASK |
 ENET_BUFFDESCRIPTOR_RX_CRC_MASK)
```

**21.5.22 #define ENET\_FRAME\_MAX\_FRAMELEN 1518U**

**21.5.23 #define ENET\_FRAME\_VLAN\_TAGLEN 4U**

**21.5.24 #define ENET\_FRAME\_CRC\_LEN 4U**

**21.5.25 #define ENET\_FIFO\_MIN\_RX\_FULL 5U**

**21.5.26 #define ENET\_RX\_MIN\_BUFFERSIZE 256U**

**21.5.27 #define ENET\_PHY\_MAXADDRESS (ENET\_MMFR\_PA\_MASK >>  
ENET\_MMFR\_PA\_SHIFT)**

**21.5.28 #define ENET\_TX\_INTERRUPT ((uint32\_t)kENET\_TxFrameInterrupt |  
(uint32\_t)kENET\_TxBufferInterrupt)**

**21.5.29 #define ENET\_RX\_INTERRUPT ((uint32\_t)kENET\_RxFrameInterrupt |  
(uint32\_t)kENET\_RxBufferInterrupt)**

**21.5.30 #define ENET\_TS\_INTERRUPT ((uint32\_t)kENET\_TsTimerInterrupt |  
(uint32\_t)kENET\_TsAvailInterrupt)**

**21.5.31 #define ENET\_ERR\_INTERRUPT**

**Value:**

```
((uint32_t)kENET_BabrInterrupt | (uint32_t)
 kENET_BabtInterrupt | (uint32_t)kENET_EBusERInterrupt | \
 (uint32_t)kENET_LateCollisionInterrupt | (uint32_t)
 kENET_RetryLimitInterrupt | \
 (uint32_t)kENET_UnderrunInterrupt | (uint32_t)
 kENET_PayloadRxInterrupt)
```

## 21.6 Typedef Documentation

- 21.6.1 `typedef void*(* enet_rx_alloc_callback_t)(ENET_Type *base, void *userData, uint8_t ringId)`
- 21.6.2 `typedef void(* enet_rx_free_callback_t)(ENET_Type *base, void *buffer, void *userData, uint8_t ringId)`
- 21.6.3 `typedef void(* enet_callback_t)(ENET_Type *base, enet_handle_t *handle, enet_event_t event, enet_frame_info_t *frameInfo, void *userData)`
- 21.6.4 `typedef void(* enet_isr_t)(ENET_Type *base, enet_handle_t *handle)`

## 21.7 Enumeration Type Documentation

### 21.7.1 anonymous enum

Enumerator

- kStatus\_ENET\_InitMemoryFail* Init fails since buffer memory is not enough.
- kStatus\_ENET\_RxFrameError* A frame received but data error happen.
- kStatus\_ENET\_RxFrameFail* Failed to receive a frame.
- kStatus\_ENET\_RxFrameEmpty* No frame arrive.
- kStatus\_ENET\_RxFrameDrop* Rx frame is dropped since no buffer memory.
- kStatus\_ENET\_TxFrameOverLen* Tx frame over length.
- kStatus\_ENET\_TxFrameBusy* Tx buffer descriptors are under process.
- kStatus\_ENET\_TxFrameFail* Transmit frame fail.

### 21.7.2 enum enet\_mii\_mode\_t

Enumerator

- kENET\_MiiMode* MII mode for data interface.
- kENET\_RmiiMode* RMII mode for data interface.

### 21.7.3 enum enet\_mii\_speed\_t

Notice: "kENET\_MiiSpeed1000M" only supported when mii mode is "kENET\_RgmiiMode".

Enumerator

- kENET\_MiiSpeed10M* Speed 10 Mbps.
- kENET\_MiiSpeed100M* Speed 100 Mbps.

## 21.7.4 enum enet\_mii\_duplex\_t

Enumerator

*kENET\_MiiHalfDuplex* Half duplex mode.

*kENET\_MiiFullDuplex* Full duplex mode.

## 21.7.5 enum enet\_mii\_write\_t

Enumerator

*kENET\_MiiWriteNoCompliant* Write frame operation, but not MII-compliant.

*kENET\_MiiWriteValidFrame* Write frame operation for a valid MII management frame.

## 21.7.6 enum enet\_mii\_read\_t

Enumerator

*kENET\_MiiReadValidFrame* Read frame operation for a valid MII management frame.

*kENET\_MiiReadNoCompliant* Read frame operation, but not MII-compliant.

## 21.7.7 enum enet\_mii\_extend\_opcode

Enumerator

*kENET\_MiiAddrWrite\_C45* Address Write operation.

*kENET\_MiiWriteFrame\_C45* Write frame operation for a valid MII management frame.

*kENET\_MiiReadFrame\_C45* Read frame operation for a valid MII management frame.

## 21.7.8 enum enet\_special\_control\_flag\_t

These control flags are provided for special user requirements. Normally, these control flags are unused for ENET initialization. For special requirements, set the flags to macSpecialConfig in the [enet\\_config\\_t](#). The kENET\_ControlStoreAndFwdDisable is used to disable the FIFO store and forward. FIFO store and forward means that the FIFO read/send is started when a complete frame is stored in TX/RX FIFO. If this flag is set, configure rxFifoFullThreshold and txFifoWatermark in the [enet\\_config\\_t](#).

Enumerator

*kENET\_ControlFlowControlEnable* Enable ENET flow control: pause frame.

*kENET\_ControlRxPayloadCheckEnable* Enable ENET receive payload length check.

*kENET\_ControlRxPadRemoveEnable* Padding is removed from received frames.

*kENET\_ControlRxBroadCastRejectEnable* Enable broadcast frame reject.

*kENET\_ControlMacAddrInsert* Enable MAC address insert.

*kENET\_ControlStoreAndFwdDisable* Enable FIFO store and forward.

*kENET\_ControlSMIPreambleDisable* Enable SMI preamble.

*kENET\_ControlPromiscuousEnable* Enable promiscuous mode.

*kENET\_ControlMIILoopEnable* Enable ENET MII loop back.

*kENET\_ControlVLANTagEnable* Enable normal VLAN (single vlan tag).

### 21.7.9 enum enet\_interrupt\_enable\_t

This enumeration uses one-bit encoding to allow a logical OR of multiple members. Members usually map to interrupt enable bits in one or more peripheral registers.

Enumerator

*kENET\_BabRInterrupt* Babbling receive error interrupt source.

*kENET\_BabTInterrupt* Babbling transmit error interrupt source.

*kENET\_GraceStopInterrupt* Graceful stop complete interrupt source.

*kENET\_TxFrameInterrupt* TX FRAME interrupt source.

*kENET\_TxBufferInterrupt* TX BUFFER interrupt source.

*kENET\_RxFrameInterrupt* RX FRAME interrupt source.

*kENET\_RxBufferInterrupt* RX BUFFER interrupt source.

*kENET\_MiiInterrupt* MII interrupt source.

*kENET\_EBusERInterrupt* Ethernet bus error interrupt source.

*kENET\_LateCollisionInterrupt* Late collision interrupt source.

*kENET\_RetryLimitInterrupt* Collision Retry Limit interrupt source.

*kENET\_UnderrunInterrupt* Transmit FIFO underrun interrupt source.

*kENET\_PayloadRxInterrupt* Payload Receive error interrupt source.

*kENET\_WakeupInterrupt* WAKEUP interrupt source.

*kENET\_TsAvailInterrupt* TS AVAIL interrupt source for PTP.

*kENET\_TsTimerInterrupt* TS WRAP interrupt source for PTP.

### 21.7.10 enum enet\_event\_t

Enumerator

*kENET\_RxEvent* Receive event.

*kENET\_TxEvent* Transmit event.

*kENET\_ErrEvent* Error event: BABR/BABT/EBERR/LC/RL/UN/PLR .

*kENET\_WakeUpEvent* Wake up from sleep mode event.

*kENET\_TimeStampEvent* Time stamp event.

*kENET\_TimeStampAvailEvent* Time stamp available event.

### 21.7.11 enum enet\_tx\_accelerator\_t

Enumerator

- kENET\_TxAccelIsShift16Enabled*** Transmit FIFO shift-16.
- kENET\_TxAccelIpCheckEnabled*** Insert IP header checksum.
- kENET\_TxAccelProtoCheckEnabled*** Insert protocol checksum.

### 21.7.12 enum enet\_rx\_accelerator\_t

Enumerator

- kENET\_RxAccelPadRemoveEnabled*** Padding removal for short IP frames.
- kENET\_RxAccelIpCheckEnabled*** Discard with wrong IP header checksum.
- kENET\_RxAccelProtoCheckEnabled*** Discard with wrong protocol checksum.
- kENET\_RxAccelMacCheckEnabled*** Discard with Mac layer errors.
- kENET\_RxAccelIsShift16Enabled*** Receive FIFO shift-16.

## 21.8 Function Documentation

### 21.8.1 uint32\_t ENET\_GetInstance ( ENET\_Type \* *base* )

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

Returns

ENET instance.

### 21.8.2 void ENET\_GetDefaultConfig ( enet\_config\_t \* *config* )

The purpose of this API is to get the default ENET MAC controller configure structure for [ENET\\_Init\(\)](#). User may use the initialized structure unchanged in [ENET\\_Init\(\)](#), or modify some fields of the structure before calling [ENET\\_Init\(\)](#). Example:

```
enet_config_t config;
ENET_GetDefaultConfig(&config);
```

## Parameters

<i>config</i>	The ENET mac controller configuration structure pointer.
---------------	--

**21.8.3 status\_t ENET\_Up ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, const enet\_config\_t \* *config*, const enet\_buffer\_config\_t \* *bufferConfig*, uint8\_t \* *macAddr*, uint32\_t *srcClock\_Hz* )**

This function initializes the module with the ENET configuration.

## Note

ENET has two buffer descriptors legacy buffer descriptors and enhanced IEEE 1588 buffer descriptors. The legacy descriptor is used by default. To use the IEEE 1588 feature, use the enhanced IEEE 1588 buffer descriptor by defining "ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE" and calling ENET\_Ptp1588Configure() to configure the 1588 feature and related buffers after calling [ENET\\_Up\(\)](#).

## Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	ENET handler pointer.
<i>config</i>	ENET mac configuration structure pointer. The "enet_config_t" type mac configuration return from ENET_GetDefaultConfig can be used directly. It is also possible to verify the Mac configuration using other methods.
<i>bufferConfig</i>	ENET buffer configuration structure pointer. The buffer configuration should be prepared for ENET Initialization. It is the start address of "ringNum" enet_buffer_config structures. To support added multi-ring features in some soc and compatible with the previous enet driver version. For single ring supported, this bufferConfig is a buffer configure structure pointer, for multi-ring supported and used case, this bufferConfig pointer should be a buffer configure structure array pointer.

<i>macAddr</i>	ENET mac address of Ethernet device. This MAC address should be provided.
<i>srcClock_Hz</i>	The internal module clock source for MII clock.

Return values

<i>kStatus_Success</i>	Succeed to initialize the ethernet driver.
<i>kStatus_ENET_Init-MemoryFail</i>	Init fails since buffer memory is not enough.

#### 21.8.4 status\_t ENET\_Init( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, const enet\_config\_t \* *config*, const enet\_buffer\_config\_t \* *bufferConfig*, uint8\_t \* *macAddr*, uint32\_t *srcClock\_Hz* )

This function ungates the module clock and initializes it with the ENET configuration.

Note

ENET has two buffer descriptors legacy buffer descriptors and enhanced IEEE 1588 buffer descriptors. The legacy descriptor is used by default. To use the IEEE 1588 feature, use the enhanced IEEE 1588 buffer descriptor by defining "ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE" and calling ENET\_Ptp1588Configure() to configure the 1588 feature and related buffers after calling [ENET\\_Init\(\)](#).

Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	ENET handler pointer.
<i>config</i>	ENET mac configuration structure pointer. The "enet_config_t" type mac configuration return from ENET_GetDefaultConfig can be used directly. It is also possible to verify the Mac configuration using other methods.
<i>bufferConfig</i>	ENET buffer configuration structure pointer. The buffer configuration should be prepared for ENET Initialization. It is the start address of "ringNum" enet_buffer_config structures. To support added multi-ring features in some soc and compatible with the previous enet driver version. For single ring supported, this bufferConfig is a buffer configure structure pointer, for multi-ring supported and used case, this bufferConfig pointer should be a buffer configure structure array pointer.

<i>macAddr</i>	ENET mac address of Ethernet device. This MAC address should be provided.
<i>srcClock_Hz</i>	The internal module clock source for MII clock.

Return values

<i>kStatus_Success</i>	Succeed to initialize the ethernet driver.
<i>kStatus_ENET_Init-MemoryFail</i>	Init fails since buffer memory is not enough.

### 21.8.5 void ENET\_Down ( ENET\_Type \* *base* )

This function disables the ENET module.

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

### 21.8.6 void ENET\_Deinit ( ENET\_Type \* *base* )

This function gates the module clock, clears ENET interrupts, and disables the ENET module.

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

### 21.8.7 static void ENET\_Reset ( ENET\_Type \* *base* ) [inline], [static]

This function restores the ENET module to reset state. Note that this function sets all registers to reset state. As a result, the ENET module can't work after calling this function.

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

### 21.8.8 void ENET\_SetMII ( ENET\_Type \* *base*, enet\_mii\_speed\_t *speed*, enet\_mii\_duplex\_t *duplex* )

This API is provided to dynamically change the speed and duplex for MAC.

Parameters

<i>base</i>	ENET peripheral base address.
<i>speed</i>	The speed of the RMII mode.
<i>duplex</i>	The duplex of the RMII mode.

### 21.8.9 void ENET\_SetSMI ( ENET\_Type \* *base*, uint32\_t *srcClock\_Hz*, bool *isPreambleDisabled* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>srcClock_Hz</i>	This is the ENET module clock frequency. See clock distribution.
<i>isPreambleDisabled</i>	The preamble disable flag. <ul style="list-style-type: none"> <li>• true Enables the preamble.</li> <li>• false Disables the preamble.</li> </ul>

### 21.8.10 static bool ENET\_GetSMI ( ENET\_Type \* *base* ) [inline], [static]

This API is used to get the SMI configuration to check whether the MII management interface has been set.

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

Returns

The SMI setup status true or false.

### 21.8.11 static uint32\_t ENET\_ReadSMIData ( ENET\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

Returns

The data read from PHY

**21.8.12 static void ENET\_StartSMIWrite ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, enet\_mii\_write\_t *operation*, uint16\_t *data* ) [inline], [static]**

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIOWrite\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

<i>base</i>	ENET peripheral base address.
<i>phyAddr</i>	The PHY address. Range from 0 ~ 31.
<i>regAddr</i>	The PHY register address. Range from 0 ~ 31.
<i>operation</i>	The write operation.
<i>data</i>	The data written to PHY.

**21.8.13 static void ENET\_StartSMIRead ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, enet\_mii\_read\_t *operation* ) [inline], [static]**

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIORRead\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

<i>base</i>	ENET peripheral base address.
<i>phyAddr</i>	The PHY address. Range from 0 ~ 31.

<i>regAddr</i>	The PHY register address. Range from 0 ~ 31.
<i>operation</i>	The read operation.

### 21.8.14 status\_t ENET\_MDIOWrite ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, uint16\_t *data* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>phyAddr</i>	The PHY address. Range from 0 ~ 31.
<i>regAddr</i>	The PHY register. Range from 0 ~ 31.
<i>data</i>	The data written to PHY.

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 21.8.15 status\_t ENET\_MDIORead ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, uint16\_t \* *pData* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>phyAddr</i>	The PHY address. Range from 0 ~ 31.
<i>regAddr</i>	The PHY register. Range from 0 ~ 31.
<i>pData</i>	The data read from PHY.

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 21.8.16 static void ENET\_StartExtC45SMIWriteReg ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *regAddr* ) [inline], [static]

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIOC45Write\(\)](#)/[ENET\\_MDIOC45Read\(\)](#) can be called. For

customized requirements, implement with combining separated APIs.

Parameters

<i>base</i>	ENET peripheral base address.
<i>portAddr</i>	The MDIO port address(PHY address).
<i>devAddr</i>	The device address.
<i>regAddr</i>	The PHY register address.

### 21.8.17 static void ENET\_StartExtC45SMIWriteData ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *data* ) [inline], [static]

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIOC45Write\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

<i>base</i>	ENET peripheral base address.
<i>portAddr</i>	The MDIO port address(PHY address).
<i>devAddr</i>	The device address.
<i>data</i>	The data written to PHY.

### 21.8.18 static void ENET\_StartExtC45SMIReadData ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr* ) [inline], [static]

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIOC45Read\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

<i>base</i>	ENET peripheral base address.
<i>portAddr</i>	The MDIO port address(PHY address).
<i>devAddr</i>	The device address.

### 21.8.19 status\_t ENET\_MDIOC45Write ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *regAddr*, uint16\_t *data* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>portAddr</i>	The MDIO port address(PHY address).
<i>devAddr</i>	The device address.
<i>regAddr</i>	The PHY register address.
<i>data</i>	The data written to PHY.

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 21.8.20 status\_t ENET\_MDIOD45Read ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *regAddr*, uint16\_t \* *pData* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>portAddr</i>	The MDIO port address(PHY address).
<i>devAddr</i>	The device address.
<i>regAddr</i>	The PHY register address.
<i>pData</i>	The data read from PHY.

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 21.8.21 void ENET\_SetMacAddr ( ENET\_Type \* *base*, uint8\_t \* *macAddr* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>macAddr</i>	The six-byte Mac address pointer. The pointer is allocated by application and input into the API.

**21.8.22 void ENET\_GetMacAddr ( ENET\_Type \* *base*, uint8\_t \* *macAddr* )**

Parameters

<i>base</i>	ENET peripheral base address.
<i>macAddr</i>	The six-byte Mac address pointer. The pointer is allocated by application and input into the API.

**21.8.23 void ENET\_AddMulticastGroup ( ENET\_Type \* *base*, uint8\_t \* *address* )**

Parameters

<i>base</i>	ENET peripheral base address.
<i>address</i>	The six-byte multicast group address which is provided by application.

**21.8.24 void ENET\_LeaveMulticastGroup ( ENET\_Type \* *base*, uint8\_t \* *address* )**

Parameters

<i>base</i>	ENET peripheral base address.
<i>address</i>	The six-byte multicast group address which is provided by application.

**21.8.25 static void ENET\_ActiveRead ( ENET\_Type \* *base* ) [inline],  
[static]**

This function is to active the enet read process.

Note

This must be called after the MAC configuration and state are ready. It must be called after the [ENET\\_Init\(\)](#). This should be called when the frame reception is required.

## Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

**21.8.26 static void ENET\_EnableSleepMode ( ENET\_Type \* *base*, bool *enable* ) [inline], [static]**

This function is used to set the MAC enter sleep mode. When entering sleep mode, the magic frame wakeup interrupt should be enabled to wake up MAC from the sleep mode and reset it to normal mode.

## Parameters

<i>base</i>	ENET peripheral base address.
<i>enable</i>	True enable sleep mode, false disable sleep mode.

**21.8.27 static void ENET\_GetAccelFunction ( ENET\_Type \* *base*, uint32\_t \* *txAccelOption*, uint32\_t \* *rxAccelOption* ) [inline], [static]**

## Parameters

<i>base</i>	ENET peripheral base address.
<i>txAccelOption</i>	The transmit accelerator option. The "enet_tx_accelerator_t" is recommended to be used to as the mask to get the exact the accelerator option.
<i>rxAccelOption</i>	The receive accelerator option. The "enet_rx_accelerator_t" is recommended to be used to as the mask to get the exact the accelerator option.

**21.8.28 static void ENET\_EnableInterrupts ( ENET\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

This function enables the ENET interrupt according to the provided mask. The mask is a logical OR of enumeration members. See [enet\\_interrupt\\_enable\\_t](#). For example, to enable the TX frame interrupt and RX frame interrupt, do the following.

```
*     ENET_EnableInterrupts(ENET, kENET_TxFrameInterrupt |  
*                           kENET_RxFrameInterrupt);  
*
```

## Parameters

<i>base</i>	ENET peripheral base address.
<i>mask</i>	ENET interrupts to enable. This is a logical OR of the enumeration <a href="#">enet_interrupt_enable_t</a> .

**21.8.29 static void ENET\_DisableInterrupts ( ENET\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

This function disables the ENET interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [enet\\_interrupt\\_enable\\_t](#). For example, to disable the TX frame interrupt and RX frame interrupt, do the following.

```
*     ENET_DisableInterrupts(ENET, kENET_TxFrameInterrupt |
    kENET_RxFrameInterrupt);
*
```

## Parameters

<i>base</i>	ENET peripheral base address.
<i>mask</i>	ENET interrupts to disable. This is a logical OR of the enumeration <a href="#">enet_interrupt_enable_t</a> .

**21.8.30 static uint32\_t ENET\_GetInterruptStatus ( ENET\_Type \* *base* )  
[inline], [static]**

## Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

## Returns

The event status of the interrupt source. This is the logical OR of members of the enumeration [enet\\_interrupt\\_enable\\_t](#).

**21.8.31 static void ENET\_ClearInterruptStatus ( ENET\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

This function clears enabled ENET interrupts according to the provided mask. The mask is a logical OR of enumeration members. See the [enet\\_interrupt\\_enable\\_t](#). For example, to clear the TX frame interrupt and RX frame interrupt, do the following.

```
*     ENET_ClearInterruptStatus(ENET,
    kENET_TxFrameInterrupt | kENET_RxFrameInterrupt);
*
```

## Parameters

<i>base</i>	ENET peripheral base address.
<i>mask</i>	ENET interrupt source to be cleared. This is the logical OR of members of the enumeration <a href="#">enet_interrupt_enable_t</a> .

**21.8.32 void ENET\_SetRxISRHandler ( ENET\_Type \* *base*, enet\_isr\_t *ISRHandler* )**

## Parameters

<i>base</i>	ENET peripheral base address.
<i>ISRHandler</i>	The handler to install.

**21.8.33 void ENET\_SetTxISRHandler ( ENET\_Type \* *base*, enet\_isr\_t *ISRHandler* )**

## Parameters

<i>base</i>	ENET peripheral base address.
<i>ISRHandler</i>	The handler to install.

**21.8.34 void ENET\_SetErrISRHandler ( ENET\_Type \* *base*, enet\_isr\_t *ISRHandler* )**

## Parameters

<i>base</i>	ENET peripheral base address.
<i>ISRHandler</i>	The handler to install.

**21.8.35 void ENET\_GetRxErrBeforeReadFrame ( enet\_handle\_t \* *handle*, enet\_data\_error\_stats\_t \* *eErrorStatic*, uint8\_t *ringId* )**

This API must be called after the ENET\_GetRxFrameSize and before the [ENET\\_ReadFrame\(\)](#). If the ENET\_GetRxFrameSize returns kStatus\_ENET\_RxFrameError, the ENET\_GetRxErrBeforeReadFrame can be used to get the exact error statistics. This is an example.

```

*     status = ENET_GetRxFrameSize(&g_handle, &length, 0);
*     if (status == kStatus_ENET_RxFrameError)
*     {
*         Comments: Get the error information of the received frame.
*         ENET_GetRxErrBeforeReadFrame(&g_handle, &eErrStatic, 0);
*         Comments: update the receive buffer.
*         ENET_ReadFrame(EXAMPLE_ENET, &g_handle, NULL, 0);
*     }
*

```

## Parameters

<i>handle</i>	The ENET handler structure pointer. This is the same handler pointer used in the ENET_Init.
<i>eErrorStatic</i>	The error statistics structure pointer.
<i>ringId</i>	The ring index, range from 0 ~ (FSL_FEATURE_ENET_INSTANCE_QUEUEEn(x) - 1).

**21.8.36 void ENET\_GetStatistics ( ENET\_Type \* *base*, enet\_transfer\_stats\_t \* *statistics* )**

## Parameters

<i>base</i>	ENET peripheral base address.
<i>statistics</i>	The statistics structure pointer.

**21.8.37 status\_t ENET\_GetRxFrameSize ( enet\_handle\_t \* *handle*, uint32\_t \* *length*, uint8\_t *ringId* )**

This function gets a received frame size from the ENET buffer descriptors.

## Note

The FCS of the frame is automatically removed by MAC and the size is the length without the FCS. After calling ENET\_GetRxFrameSize, [ENET\\_ReadFrame\(\)](#) should be called to receive frame and update the BD if the result is not "kStatus\_ENET\_RxFrameEmpty".

## Parameters

<i>handle</i>	The ENET handler structure. This is the same handler pointer used in the ENET_Init.
<i>length</i>	The length of the valid frame received.
<i>ringId</i>	The ring index or ring number.

## Return values

<i>kStatus_ENET_RxFrame-Empty</i>	No frame received. Should not call ENET_ReadFrame to read frame.
<i>kStatus_ENET_RxFrame-Error</i>	Data error happens. ENET_ReadFrame should be called with NULL data and NULL length to update the receive buffers.
<i>kStatus_Success</i>	Receive a frame Successfully then the ENET_ReadFrame should be called with the right data buffer and the captured data length input.

### 21.8.38 status\_t ENET\_ReadFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, uint8\_t \* *data*, uint32\_t *length*, uint8\_t *ringId*, uint32\_t \* *ts* )

This function reads a frame (both the data and the length) from the ENET buffer descriptors. User can get timestamp through ts pointer if the ts is not NULL.

## Note

It doesn't store the timestamp in the receive timestamp queue. The ENET\_GetRxFrameSize should be used to get the size of the prepared data buffer. This API uses memcpy to copy data from DMA buffer to application buffer, 4 bytes aligned data buffer in 32 bits platforms provided by user may let compiler use optimization instruction to reduce time consumption. This is an example:

```

*      uint32_t length;
*      enet_handle_t g_handle;
*      Comments: Get the received frame size firstly.
*      status = ENET_GetRxFrameSize(&g_handle, &length, 0);
*      if (length != 0)
*      {
*          Comments: Allocate memory here with the size of "length"
*          uint8_t *data = memory allocate interface;
*          if (!data)
*          {
*              ENET_ReadFrame(ENET, &g_handle, NULL, 0, 0, NULL);
*              Comments: Add the console warning log.
*          }
*          else
*          {
*              status = ENET_ReadFrame(ENET, &g_handle, data, length, 0, NULL);
*              Comments: Call stack input API to deliver the data to stack
*          }
*      }
*      else if (status == kStatus_ENET_RxFrameError)
{
    Comments: Update the received buffer when a error frame is received.
}

```

```

*           ENET_ReadFrame(ENET, &g_handle, NULL, 0, 0, NULL);
*
*       }
*

```

## Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler structure. This is the same handler pointer used in the ENET_Init.
<i>data</i>	The data buffer provided by user to store the frame which memory size should be at least "length".
<i>length</i>	The size of the data buffer which is still the length of the received frame.
<i>ringId</i>	The ring index or ring number.
<i>ts</i>	The timestamp address to store received timestamp.

## Returns

The execute status, successful or failure.

### 21.8.39 status\_t ENET\_SendFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, const uint8\_t \* *data*, uint32\_t *length*, uint8\_t *ringId*, bool *tsFlag*, void \* *context* )

## Note

The CRC is automatically appended to the data. Input the data to send without the CRC. This API uses memcpy to copy data from DMA buffer to application buffer, 4 bytes aligned data buffer in 32 bits platforms provided by user may let compiler use optimization instruction to reduce time consumption.

## Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler pointer. This is the same handler pointer used in the ENET_Init.
<i>data</i>	The data buffer provided by user to send.
<i>length</i>	The length of the data to send.

<i>ringId</i>	The ring index or ring number.
<i>tsFlag</i>	Timestamp enable flag.
<i>context</i>	Used by user to handle some events after transmit over.

Return values

<i>kStatus_Success</i>	Send frame succeed.
<i>kStatus_ENET_TxFrameBusy</i>	Transmit buffer descriptor is busy under transmission. The transmit busy happens when the data send rate is over the MAC capacity. The waiting mechanism is recommended to be added after each call return with <i>kStatus_ENET_TxFrameBusy</i> .

#### 21.8.40 **status\_t ENET\_SetTxReclaim ( enet\_handle\_t \* *handle*, bool *isEnable*, uint8\_t *ringId* )**

Note

This function must be called when no pending send frame action. Set enable if you want to reclaim context or timestamp in interrupt.

Parameters

<i>handle</i>	The ENET handler pointer. This is the same handler pointer used in the ENET_Init.
<i>isEnable</i>	Enable or disable flag.
<i>ringId</i>	The ring index or ring number.

Return values

<i>kStatus_Success</i>	Succeed to enable/disable Tx reclaim.
<i>kStatus_Fail</i>	Fail to enable/disable Tx reclaim.

#### 21.8.41 **void ENET\_ReclaimTxDescriptor ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, uint8\_t *ringId* )**

This function is used to update the tx descriptor status and store the tx timestamp when the 1588 feature is enabled. This is called by the transmit interrupt IRQ handler after the complete of a frame transmission.

## Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler pointer. This is the same handler pointer used in the ENET_Init.
<i>ringId</i>	The ring index or ring number.

**21.8.42 status\_t ENET\_GetRxFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, enet\_rx\_frame\_struct\_t \* *rxFrame*, uint8\_t *ringId* )**

This function uses the user-defined allocation and free callbacks. Every time application gets one frame through this function, driver stores the buffer address(es) in enet\_buffer\_struct\_t and allocate new buffer(s) for the BD(s). If there's no memory buffer in the pool, this function drops current one frame to keep the Rx frame in BD ring is as fresh as possible.

## Note

Application must provide a memory pool including at least BD number + n buffers in order for this function to work properly, because each BD must always take one buffer while driver is running, then other extra n buffer(s) can be taken by application. Here n is the ceil(max\_frame\_length(set by RCR) / bd\_rx\_size(set by MRBR)). Application must also provide an array structure in rxFrame->rxBuffArray with n index to receive one complete frame in any case.

## Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler pointer. This is the same handler pointer used in the ENET_Init.
<i>rxFrame</i>	The received frame information structure provided by user.
<i>ringId</i>	The ring index or ring number.

## Return values

<i>kStatus_Success</i>	Succeed to get one frame and allocate new memory for Rx buffer.
<i>kStatus_ENET_RxFrame-Empty</i>	There's no Rx frame in the BD.

<i>kStatus_ENET_RxFrame-Error</i>	There's issue in this receiving.
<i>kStatus_ENET_RxFrame-Drop</i>	There's no new buffer memory for BD, drop this frame.

### 21.8.43 status\_t ENET\_StartTxFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, enet\_tx\_frame\_struct\_t \* *txFrame*, uint8\_t *ringId* )

This function supports scattered buffer transmit, user needs to provide the buffer array.

#### Note

Tx reclaim should be enabled to ensure the Tx buffer ownership can be given back to application after Tx is over.

#### Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler pointer. This is the same handler pointer used in the ENET_Init.
<i>txFrame</i>	The Tx frame structure.
<i>ringId</i>	The ring index or ring number.

#### Return values

<i>kStatus_Success</i>	Succeed to send one frame.
<i>kStatus_ENET_TxFrame-Busy</i>	The BD is not ready for Tx or the reclaim operation still not finishes.
<i>kStatus_ENET_TxFrame-OverLen</i>	The Tx frame length is over max ethernet frame length.

### 21.8.44 void ENET\_TransmitIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle* )

#### Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler pointer.

#### 21.8.45 void ENET\_ReceiveIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler pointer.

#### 21.8.46 void ENET\_ErrorIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle* )

Parameters

<i>base</i>	ENET peripheral base address.
<i>handle</i>	The ENET handler pointer.

#### 21.8.47 void ENET\_Ptp1588IRQHandler ( ENET\_Type \* *base* )

This is used for the 1588 timer interrupt.

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

#### 21.8.48 void ENET\_CommonFrame0IRQHandler ( ENET\_Type \* *base* )

This is used for the combined tx/rx/error interrupt for single/mutli-ring (frame 0).

Parameters

<i>base</i>	ENET peripheral base address.
-------------	-------------------------------

## 21.9 Variable Documentation

### 21.9.1 const clock\_ip\_name\_t s\_enetClock[]

## 21.10 ENET CMSIS Driver

This section describes the programming interface of the ENET Cortex Microcontroller Software Interface Standard (CMSIS) driver. This driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method see <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The ENET CMSIS driver includes transactional APIs.

Transactional APIs are transaction target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code accessing the hardware registers.

### 21.10.1 Typical use case

```
void ENET_SignalEvent_t(uint32_t event)
{
    if (event == ARM_ETH_MAC_EVENT_RX_FRAME)
    {
        uint32_t size;
        uint32_t len;

        /* Get the Frame size */
        size = EXAMPLE_ENET.GetRxFrameSize();
        /* Call ENET_ReadFrame when there is a received frame. */
        if (size != 0)
        {
            /* Received valid frame. Deliver the rx buffer with the size equal to length. */
            uint8_t *data = (uint8_t *)malloc(size);
            if (data)
            {
                len = EXAMPLE_ENET.ReadFrame(data, size);
                if (size == len)
                {
                    /* Increase the received frame numbers. */
                    if (g_rxIndex < ENET_EXAMPLE_LOOP_COUNT)
                    {
                        g_rxIndex++;
                    }
                }
                free(data);
            }
        }
    }
    if (event == ARM_ETH_MAC_EVENT_TX_FRAME)
    {
        g_testTxNum++;
    }
}

/* Initialize the ENET module. */
EXAMPLE_ENET.Initialize(ENET_SignalEvent_t);
EXAMPLE_ENET.PowerControl(ARM_POWER_FULL);
EXAMPLE_ENET.SetMacAddress((ARM_ETH_MAC_ADDR *)g_macAddr);
EXAMPLE_ENET.Control(ARM_ETH_MAC_CONFIGURE, linkInfo.speed << ARM_ETH_MAC_SPEED_Pos |
                     linkInfo.duplex << ARM_ETH_MAC_DUPLEX_Pos | ARM_ETH_MAC_ADDRESS_BROADCAST);
EXAMPLE_ENET_PHY.PowerControl(ARM_POWER_FULL);
```

```

EXAMPLE_ENET_PHY.SetMode(ARM_ETH_PHY_AUTO_NEGOTIATE);
EXAMPLE_ENET.Control(ARM_ETH_MAC_CONTROL_RX, 1);
EXAMPLE_ENET.Control(ARM_ETH_MAC_CONTROL_TX, 1);
if (EXAMPLE_ENET_PHY.GetLinkState() == ARM_ETH_LINK_UP)
{
    linkInfo = EXAMPLE_ENET_PHY.GetLinkInfo();
}
else
{
    PRINTF("\r\nPHY Link down, please check the cable connection and link partner setting.\r\n");
}

/* Build broadcast for sending. */
ENET_BuildBroadCastFrame();

while (1)
{
    /* Check the total number of received number. */
    if (g_rxCheckIdx != g_rxIndex)
    {
        PRINTF("The %d frame has been successfully received!\r\n", g_rxIndex);
        g_rxCheckIdx = g_rxIndex;
    }
    if ( g_testTxNum && (g_txCheckIdx != g_testTxNum) )
    {
        g_txCheckIdx = g_testTxNum;
        PRINTF("The %d frame transmitted success!\r\n", g_txCheckIdx);
    }
    /* Get the Frame size */
    if (txnumber < ENET_EXAMPLE_LOOP_COUNT)
    {
        txnumber++;
        /* Send a multicast frame when the PHY is link up. */
        if (EXAMPLE_ENET.SendFrame(&g_frame[0], ENET_DATA_LENGTH, ARM_ETH_MAC_TX_FRAME_EVENT) ==
ARM_DRIVER_OK)
        {
            for (uint32_t count = 0; count < 0x3FF; count++)
            {
                __ASM("nop");
            }
        }
        else
        {
            PRINTF("\r\nTransmit frame failed!\r\n");
        }
    }
}
}

```

# Chapter 22

## EWM: External Watchdog Monitor Driver

### 22.1 Overview

The MCUXpresso SDK provides a peripheral driver for the External Watchdog (EWM) Driver module of MCUXpresso SDK devices.

### 22.2 Typical use case

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ewm

### Data Structures

- struct `ewm_config_t`  
*Data structure for EWM configuration. [More...](#)*

### Enumerations

- enum `ewm_lpo_clock_source_t`{  
    `kEWM_LpoClockSource0` = 0U,  
    `kEWM_LpoClockSource1` = 1U,  
    `kEWM_LpoClockSource2` = 2U,  
    `kEWM_LpoClockSource3` = 3U }  
*Describes EWM clock source.*
- enum `_ewm_interrupt_enable_t` { `kEWM_InterruptEnable` = `EWM_CTRL_INTEN_MASK` }  
*EWM interrupt configuration structure with default settings all disabled.*
- enum `_ewm_status_flags_t` { `kEWM_RunningFlag` = `EWM_CTRL_EWMEN_MASK` }  
*EWM status flags.*

### Driver version

- #define `FSL_EWM_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 3)`)  
*EWM driver version 2.0.3.*

### EWM initialization and de-initialization

- void `EWM_Init` (`EWM_Type *base`, const `ewm_config_t *config`)  
*Initializes the EWM peripheral.*
- void `EWM_Deinit` (`EWM_Type *base`)  
*Deinitializes the EWM peripheral.*
- void `EWM_GetDefaultConfig` (`ewm_config_t *config`)  
*Initializes the EWM configuration structure.*

## EWM functional Operation

- static void [EWM\\_EnableInterrupts](#) (EWM\_Type \*base, uint32\_t mask)  
*Enables the EWM interrupt.*
- static void [EWM\\_DisableInterrupts](#) (EWM\_Type \*base, uint32\_t mask)  
*Disables the EWM interrupt.*
- static uint32\_t [EWM\\_GetStatusFlags](#) (EWM\_Type \*base)  
*Gets all status flags.*
- void [EWM\\_Refresh](#) (EWM\_Type \*base)  
*Services the EWM.*

## 22.3 Data Structure Documentation

### 22.3.1 struct ewm\_config\_t

This structure is used to configure the EWM.

#### Data Fields

- bool [enableEwm](#)  
*Enable EWM module.*
- bool [enableEwmInput](#)  
*Enable EWM\_in input.*
- bool [setInputAssertLogic](#)  
*EWM\_in signal assertion state.*
- bool [enableInterrupt](#)  
*Enable EWM interrupt.*
- [ewm\\_lpo\\_clock\\_source\\_t clockSource](#)  
*Clock source select.*
- uint8\_t [prescaler](#)  
*Clock prescaler value.*
- uint8\_t [compareLowValue](#)  
*Compare low-register value.*
- uint8\_t [compareHighValue](#)  
*Compare high-register value.*

## 22.4 Macro Definition Documentation

### 22.4.1 #define FSL\_EWM\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 3))

## 22.5 Enumeration Type Documentation

### 22.5.1 enum ewm\_lpo\_clock\_source\_t

Enumerator

- kEWM\_LpoClockSource0** EWM clock sourced from lpo\_clk[0].
- kEWM\_LpoClockSource1** EWM clock sourced from lpo\_clk[1].
- kEWM\_LpoClockSource2** EWM clock sourced from lpo\_clk[2].

***kEWM\_LpoClockSource3*** EWM clock sourced from lpo\_clk[3].

## 22.5.2 enum \_ewm\_interrupt\_enable\_t

This structure contains the settings for all of EWM interrupt configurations.

Enumerator

***kEWM\_InterruptEnable*** Enable the EWM to generate an interrupt.

## 22.5.3 enum \_ewm\_status\_flags\_t

This structure contains the constants for the EWM status flags for use in the EWM functions.

Enumerator

***kEWM\_RunningFlag*** Running flag, set when EWM is enabled.

## 22.6 Function Documentation

### 22.6.1 void EWM\_Init ( **EWM\_Type** \* *base*, **const ewm\_config\_t** \* *config* )

This function is used to initialize the EWM. After calling, the EWM runs immediately according to the configuration. Note that, except for the interrupt enable control bit, other control bits and registers are write once after a CPU reset. Modifying them more than once generates a bus transfer error.

This is an example.

```
*     ewm_config_t config;
*     EWM_GetDefaultConfig(&config);
*     config.compareHighValue = 0xAAU;
*     EWM_Init(ewm_base, &config);
*
```

Parameters

<i>base</i>	EWM peripheral base address
<i>config</i>	The configuration of the EWM

### 22.6.2 void EWM\_Deinit ( **EWM\_Type** \* *base* )

This function is used to shut down the EWM.

Parameters

<i>base</i>	EWM peripheral base address
-------------	-----------------------------

### 22.6.3 void EWM\_GetDefaultConfig ( *ewm\_config\_t* \* *config* )

This function initializes the EWM configuration structure to default values. The default values are as follows.

```
*     ewmConfig->enableEwm = true;
*     ewmConfig->enableEwmInput = false;
*     ewmConfig->setInputAssertLogic = false;
*     ewmConfig->enableInterrupt = false;
*     ewmConfig->ewm_lpo_clock_source_t = kEWM_LpoClockSource0;
*     ewmConfig->prescaler = 0;
*     ewmConfig->compareLowValue = 0;
*     ewmConfig->compareHighValue = 0xFEU;
*
```

Parameters

<i>config</i>	Pointer to the EWM configuration structure.
---------------	---

See Also

[ewm\\_config\\_t](#)

### 22.6.4 static void EWM\_EnableInterrupts ( *EWM\_Type* \* *base*, *uint32\_t* *mask* ) [inline], [static]

This function enables the EWM interrupt.

Parameters

<i>base</i>	EWM peripheral base address
<i>mask</i>	The interrupts to enable The parameter can be combination of the following source if defined <ul style="list-style-type: none"><li>• kEWM InterruptEnable</li></ul>

### 22.6.5 static void EWM\_DisableInterrupts ( *EWM\_Type* \* *base*, *uint32\_t* *mask* ) [inline], [static]

This function disables the EWM interrupt.

## Parameters

<i>base</i>	EWM peripheral base address
<i>mask</i>	The interrupts to disable The parameter can be combination of the following source if defined <ul style="list-style-type: none"> <li>• kEWM_InterruptEnable</li> </ul>

## 22.6.6 static uint32\_t EWM\_GetStatusFlags ( EWM\_Type \* *base* ) [inline], [static]

This function gets all status flags.

This is an example for getting the running flag.

```
*     uint32_t status;
*     status = EWM_GetStatusFlags(ewm_base) & kEWM_RunningFlag;
*
```

## Parameters

<i>base</i>	EWM peripheral base address
-------------	-----------------------------

## Returns

State of the status flag: asserted (true) or not-asserted (false).

## See Also

[\\_ewm\\_status\\_flags\\_t](#)

- True: a related status flag has been set.
- False: a related status flag is not set.

## 22.6.7 void EWM\_Refresh ( EWM\_Type \* *base* )

This function resets the EWM counter to zero.

## Parameters

<i>base</i>	EWM peripheral base address
-------------	-----------------------------

# Chapter 23

## FlexCAN: Flex Controller Area Network Driver

### 23.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Flex Controller Area Network (FlexCAN) module of MCUXpresso SDK devices.

### Modules

- [FlexCAN Driver](#)
- [FlexCAN eDMA Driver](#)

## 23.2 FlexCAN Driver

### 23.2.1 Overview

This section describes the programming interface of the FlexCAN driver. The FlexCAN driver configures FlexCAN module and provides functional and transactional interfaces to build the FlexCAN application.

### 23.2.2 Typical use case

#### 23.2.2.1 Message Buffer Send Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/flexcan

#### 23.2.2.2 Message Buffer Receive Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/flexcan

#### 23.2.2.3 Receive FIFO Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/flexcan

## Data Structures

- struct [flexcan\\_frame\\_t](#)  
*FlexCAN message frame structure. [More...](#)*
- struct [flexcan\\_fd\\_frame\\_t](#)  
*CAN FD message frame structure. [More...](#)*
- struct [flexcan\\_timing\\_config\\_t](#)  
*FlexCAN protocol timing characteristic configuration structure. [More...](#)*
- struct [flexcan\\_config\\_t](#)  
*FlexCAN module configuration structure. [More...](#)*
- struct [flexcan\\_rx\\_mb\\_config\\_t](#)  
*FlexCAN Receive Message Buffer configuration structure. [More...](#)*
- struct [flexcan\\_rx\\_fifo\\_config\\_t](#)  
*FlexCAN Legacy Rx FIFO configuration structure. [More...](#)*
- struct [flexcan\\_mb\\_transfer\\_t](#)  
*FlexCAN Message Buffer transfer. [More...](#)*
- struct [flexcan\\_fifo\\_transfer\\_t](#)  
*FlexCAN Rx FIFO transfer. [More...](#)*
- struct [flexcan\\_handle\\_t](#)  
*FlexCAN handle structure. [More...](#)*

## Macros

- #define **DLC\_LENGTH\_DECODE**(dlc) (((dlc) <= 8U) ? (dlc) : (((dlc) <= 12U) ? (((dlc)-6U) \* 4U) : (((dlc)-11U) \* 16U)))  
*FlexCAN frame length helper macro.*
- #define **FLEXCAN\_ID\_STD**(id) (((uint32\_t)((uint32\_t)(id)) << CAN\_ID\_STD\_SHIFT)) & CAN\_ID\_STD\_MASK)  
*FlexCAN Frame ID helper macro.*
- #define **FLEXCAN\_ID\_EXT**(id)  
*Extend Frame ID helper macro.*
- #define **FLEXCAN\_RX\_MB\_STD\_MASK**(id, rtr, ide)  
*FlexCAN Rx Message Buffer Mask helper macro.*
- #define **FLEXCAN\_RX\_MB\_EXT\_MASK**(id, rtr, ide)  
*Extend Rx Message Buffer Mask helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A**(id, rtr, ide)  
*FlexCAN Legacy Rx FIFO Mask helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_HIGH**(id, rtr, ide)  
*Standard Rx FIFO Mask helper macro Type B upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_LOW**(id, rtr, ide)  
*Standard Rx FIFO Mask helper macro Type B lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_HIGH**(id) (((uint32\_t)(id)&0x7F8) << 21)  
*Standard Rx FIFO Mask helper macro Type C upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_HIGH**(id) (((uint32\_t)(id)&0x7F8) << 13)  
*Standard Rx FIFO Mask helper macro Type C mid-upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_LOW**(id) (((uint32\_t)(id)&0x7F8) << 5)  
*Standard Rx FIFO Mask helper macro Type C mid-lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_LOW**(id) (((uint32\_t)(id)&0x7F8) >> 3)  
*Standard Rx FIFO Mask helper macro Type C lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_A**(id, rtr, ide)  
*Extend Rx FIFO Mask helper macro Type A helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_HIGH**(id, rtr, ide)  
*Extend Rx FIFO Mask helper macro Type B upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_LOW**(id, rtr, ide)  
*Extend Rx FIFO Mask helper macro Type B lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_HIGH**(id) ((FLEXCAN\_ID\_EXT(id) & 0x1FE00000) << 3)  
*Extend Rx FIFO Mask helper macro Type C upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_HIGH**(id)  
*Extend Rx FIFO Mask helper macro Type C mid-upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_LOW**(id)  
*Extend Rx FIFO Mask helper macro Type C mid-lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_LOW**(id) ((FLEXCAN\_ID\_EXT(id) & 0x1FE00000) >> 21)  
*Extend Rx FIFO Mask helper macro Type C lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_A**(id, rtr, ide) **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A**(id, rtr, ide)  
*FlexCAN Rx FIFO Filter helper macro.*

- `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_B_HIGH(id, rtr, ide)`  
*Standard Rx FIFO Filter helper macro Type B upper part helper macro.*
- `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_B_LOW(id, rtr, ide)`  
*Standard Rx FIFO Filter helper macro Type B lower part helper macro.*
- `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_HIGH(id)`  
*Standard Rx FIFO Filter helper macro Type C upper part helper macro.*
- `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_MID_HIGH(id)`  
*Standard Rx FIFO Filter helper macro Type C mid-upper part helper macro.*
- `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_MID_LOW(id)`  
*Standard Rx FIFO Filter helper macro Type C mid-lower part helper macro.*
- `#define FLEXCAN_RX_FIFO_STD_FILTER_TYPE_C_LOW(id)`  
*Standard Rx FIFO Filter helper macro Type C lower part helper macro.*
- `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_A(id, rtr, ide) FLEXCAN_RX_FIFO_EXT_-MASK_TYPE_A(id, rtr, ide)`  
*Extend Rx FIFO Filter helper macro Type A helper macro.*
- `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_B_HIGH(id, rtr, ide)`  
*Extend Rx FIFO Filter helper macro Type B upper part helper macro.*
- `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_B_LOW(id, rtr, ide)`  
*Extend Rx FIFO Filter helper macro Type B lower part helper macro.*
- `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_HIGH(id)`  
*Extend Rx FIFO Filter helper macro Type C upper part helper macro.*
- `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_MID_HIGH(id)`  
*Extend Rx FIFO Filter helper macro Type C mid-upper part helper macro.*
- `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_MID_LOW(id)`  
*Extend Rx FIFO Filter helper macro Type C mid-lower part helper macro.*
- `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_LOW(id) FLEXCAN_RX_FIFO_EXT_-MASK_TYPE_C_LOW(id)`  
*Extend Rx FIFO Filter helper macro Type C lower part helper macro.*
- `#define FLEXCAN_ERROR_AND_STATUS_INIT_FLAG`  
*FlexCAN interrupt/status flag helper macro.*
- `#define FLEXCAN_MEMORY_ENHANCED_RX_FIFO_INIT_FLAG (0U)`  
*FlexCAN Enhanced Rx FIFO base address helper macro.*
- `#define FLEXCAN_CALLBACK(x) void(x)(CAN_Type * base, flexcan_handle_t * handle, status_t status, uint32_t result, void *userData)`  
*FlexCAN transfer callback function.*

## Enumerations

- enum {
   
kStatus\_FLEXCAN\_TxBusy = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 0),
   
kStatus\_FLEXCAN\_TxIdle = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 1),
   
kStatus\_FLEXCAN\_TxSwitchToRx,
   
kStatus\_FLEXCAN\_RxBusy = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 3),
   
kStatus\_FLEXCAN\_RxIdle = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 4),
   
kStatus\_FLEXCAN\_RxOverflow = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 5),
   
kStatus\_FLEXCAN\_RxFifoBusy = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 6),
   
kStatus\_FLEXCAN\_RxFifoIdle = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 7),
   
kStatus\_FLEXCAN\_RxFifoOverflow = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 8),
   
kStatus\_FLEXCAN\_RxFifoWarning = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 9),
   
kStatus\_FLEXCAN\_RxFifoDisabled,
   
kStatus\_FLEXCAN\_ErrorStatus = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 11),
   
kStatus\_FLEXCAN\_WakeUp = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 12),
   
kStatus\_FLEXCAN\_UnHandled = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 13),
   
kStatus\_FLEXCAN\_RxRemote = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 14) }
- FlexCAN transfer status.*
- enum **flexcan\_frame\_format\_t** {
   
kFLEXCAN\_FrameFormatStandard = 0x0U,
   
kFLEXCAN\_FrameFormatExtend = 0x1U }
- FlexCAN frame format.*
- enum **flexcan\_frame\_type\_t** {
   
kFLEXCAN\_FrameTypeData = 0x0U,
   
kFLEXCAN\_FrameTypeRemote = 0x1U }
- FlexCAN frame type.*
- enum **flexcan\_clock\_source\_t** {
   
kFLEXCAN\_ClkSrcOsc = 0x0U,
   
kFLEXCAN\_ClkSrcPeri = 0x1U,
   
kFLEXCAN\_ClkSrc0 = 0x0U,
   
kFLEXCAN\_ClkSrc1 = 0x1U }
- FlexCAN clock source.*
- enum **flexcan\_wake\_up\_source\_t** {
   
kFLEXCAN\_WakeupSrcUnfiltered = 0x0U,
   
kFLEXCAN\_WakeupSrcFiltered = 0x1U }
- FlexCAN wake up source.*
- enum **flexcan\_rx\_fifo\_filter\_type\_t** {
   
kFLEXCAN\_RxFifoFilterTypeA = 0x0U,
   
kFLEXCAN\_RxFifoFilterTypeB,
   
kFLEXCAN\_RxFifoFilterTypeC,
   
kFLEXCAN\_RxFifoFilterTypeD = 0x3U }
- FlexCAN Rx Fifo Filter type.*
- enum **flexcan\_mb\_size\_t** {

```
kFLEXCAN_8BperMB = 0x0U,
kFLEXCAN_16BperMB = 0x1U,
kFLEXCAN_32BperMB = 0x2U,
kFLEXCAN_64BperMB = 0x3U }
```

*FlexCAN Message Buffer Payload size.*

- enum `_flexcan_fd_frame_length` {
   
kFLEXCAN\_0BperFrame = 0x0U,
   
kFLEXCAN\_1BperFrame,
   
kFLEXCAN\_2BperFrame,
   
kFLEXCAN\_3BperFrame,
   
kFLEXCAN\_4BperFrame,
   
kFLEXCAN\_5BperFrame,
   
kFLEXCAN\_6BperFrame,
   
kFLEXCAN\_7BperFrame,
   
kFLEXCAN\_8BperFrame,
   
kFLEXCAN\_12BperFrame,
   
kFLEXCAN\_16BperFrame,
   
kFLEXCAN\_20BperFrame,
   
kFLEXCAN\_24BperFrame,
   
kFLEXCAN\_32BperFrame,
   
kFLEXCAN\_48BperFrame,
   
kFLEXCAN\_64BperFrame }

*FlexCAN CAN FD frame supporting data length (available DLC values).*

- enum `flexcan_rx_fifo_priority_t` {
   
kFLEXCAN\_RxFifoPrioLow = 0x0U,
   
kFLEXCAN\_RxFifoPrioHigh = 0x1U }
  - enum `_flexcan_interrupt_enable` {
   
kFLEXCAN\_BusOffInterruptEnable = CAN\_CTRL1\_BOFFMSK\_MASK,
   
kFLEXCAN\_ErrorInterruptEnable = CAN\_CTRL1\_ERRMSK\_MASK,
   
kFLEXCAN\_TxWarningInterruptEnable = CAN\_CTRL1\_TWRNMSK\_MASK,
   
kFLEXCAN\_RxWarningInterruptEnable = CAN\_CTRL1\_RWRNMSK\_MASK,
   
kFLEXCAN\_WakeUpInterruptEnable = CAN\_MCR\_WAKMSK\_MASK,
   
kFLEXCAN\_FDErrorInterruptEnable = CAN\_CTRL2\_ERRMSK\_FAST\_MASK }
- FlexCAN interrupt enable enumerations.*
- enum `_flexcan_flags` {

```

kFLEXCAN_ErrorOverrunFlag = CAN_ESR1_ERROVR_MASK,
kFLEXCAN_FDErrorIntFlag = CAN_ESR1_ERRINT_FAST_MASK,
kFLEXCAN_BusoffDoneIntFlag = CAN_ESR1_BOFFDONEINT_MASK,
kFLEXCAN_SynchFlag = CAN_ESR1_SYNCH_MASK,
kFLEXCAN_TxWarningIntFlag = CAN_ESR1_TWRNINT_MASK,
kFLEXCAN_RxWarningIntFlag = CAN_ESR1_RWRNINT_MASK,
kFLEXCAN_IdleFlag = CAN_ESR1_IDLE_MASK,
kFLEXCAN_FaultConfinementFlag = CAN_ESR1_FLTCONF_MASK,
kFLEXCAN_TransmittingFlag = CAN_ESR1_TX_MASK,
kFLEXCAN_ReceivingFlag = CAN_ESR1_RX_MASK,
kFLEXCAN_BusOffIntFlag = CAN_ESR1_BOFFINT_MASK,
kFLEXCAN_ErrorIntFlag = CAN_ESR1_ERRINT_MASK,
kFLEXCAN_WakeUpIntFlag = CAN_ESR1_WAKINT_MASK }

```

*FlexCAN status flags.*

- enum `_flexcan_error_flags` {

```

kFLEXCAN_FDStuffingError = CAN_ESR1_STFERR_FAST_MASK,
kFLEXCAN_FDFormError = CAN_ESR1_FRMERR_FAST_MASK,
kFLEXCAN_FDCrcError = CAN_ESR1_CRCERR_FAST_MASK,
kFLEXCAN_FDBit0Error = CAN_ESR1_BIT0ERR_FAST_MASK,
kFLEXCAN_FDBit1Error = (int)CAN_ESR1_BIT1ERR_FAST_MASK,
kFLEXCAN_TxErrorWarningFlag = CAN_ESR1_TXWRN_MASK,
kFLEXCAN_RxErrorWarningFlag = CAN_ESR1_RXWRN_MASK,
kFLEXCAN_StuffingError = CAN_ESR1_STFERR_MASK,
kFLEXCAN_FormError = CAN_ESR1_FRMERR_MASK,
kFLEXCAN_CrcError = CAN_ESR1_CRCERR_MASK,
kFLEXCAN_AckError = CAN_ESR1_ACKERR_MASK,
kFLEXCAN_Bit0Error = CAN_ESR1_BIT0ERR_MASK,
kFLEXCAN_Bit1Error = CAN_ESR1_BIT1ERR_MASK }

```

*FlexCAN error status flags.*

- enum {

```

kFLEXCAN_RxFifoOverflowFlag = CAN_IFLAG1_BUF7I_MASK,
kFLEXCAN_RxFifoWarningFlag = CAN_IFLAG1_BUF6I_MASK,
kFLEXCAN_RxFifoFrameAvlFlag = CAN_IFLAG1_BUF5I_MASK }

```

*FlexCAN Legacy Rx FIFO status flags.*

## Driver version

- #define `FSL_FLEXCAN_DRIVER_VERSION` (`MAKE_VERSION(2, 11, 1)`)

*FlexCAN driver version.*

## Initialization and deinitialization

- bool `FLEXCAN_IsInstanceHasFDMode` (`CAN_Type *base`)

*Determine whether the FlexCAN instance support CAN FD mode at run time.*

- void **FLEXCAN\_EnterFreezeMode** (CAN\_Type \*base)  
*Enter FlexCAN Freeze Mode.*
- void **FLEXCAN\_ExitFreezeMode** (CAN\_Type \*base)  
*Exit FlexCAN Freeze Mode.*
- uint32\_t **FLEXCANGetInstance** (CAN\_Type \*base)  
*Get the FlexCAN instance from peripheral base address.*
- bool **FLEXCAN\_CalculateImprovedTimingValues** (CAN\_Type \*base, uint32\_t bitRate, uint32\_t sourceClock\_Hz, flexcan\_timing\_config\_t \*pTimingConfig)  
*Calculates the improved timing values by specific bit Rates for classical CAN.*
- void **FLEXCAN\_Init** (CAN\_Type \*base, const flexcan\_config\_t \*pConfig, uint32\_t sourceClock\_Hz)  
*Initializes a FlexCAN instance.*
- bool **FLEXCAN\_FDCalculateImprovedTimingValues** (CAN\_Type \*base, uint32\_t bitRate, uint32\_t bitRateFD, uint32\_t sourceClock\_Hz, flexcan\_timing\_config\_t \*pTimingConfig)  
*Calculates the improved timing values by specific bit rates for CANFD.*
- void **FLEXCAN\_FDInit** (CAN\_Type \*base, const flexcan\_config\_t \*pConfig, uint32\_t sourceClock\_Hz, flexcan\_mb\_size\_t dataSize, bool brs)  
*Initializes a FlexCAN instance.*
- void **FLEXCAN\_Deinit** (CAN\_Type \*base)  
*De-initializes a FlexCAN instance.*
- void **FLEXCAN\_GetDefaultConfig** (flexcan\_config\_t \*pConfig)  
*Gets the default configuration structure.*

## Configuration.

- void **FLEXCAN\_SetTimingConfig** (CAN\_Type \*base, const flexcan\_timing\_config\_t \*pConfig)  
*Sets the FlexCAN classical CAN protocol timing characteristic.*
- status\_t **FLEXCAN\_SetBitRate** (CAN\_Type \*base, uint32\_t sourceClock\_Hz, uint32\_t bitRate\_Bps)  
*Set bit rate of FlexCAN classical CAN frame or CAN FD frame nominal phase.*
- void **FLEXCAN\_SetFDTimingConfig** (CAN\_Type \*base, const flexcan\_timing\_config\_t \*pConfig)  
*Sets the FlexCAN CANFD data phase timing characteristic.*
- status\_t **FLEXCAN\_SetFDBitRate** (CAN\_Type \*base, uint32\_t sourceClock\_Hz, uint32\_t bitRate\_N\_Bps, uint32\_t bitRateD\_Bps)  
*Set bit rate of FlexCAN FD frame.*
- void **FLEXCAN\_SetRxMbGlobalMask** (CAN\_Type \*base, uint32\_t mask)  
*Sets the FlexCAN receive message buffer global mask.*
- void **FLEXCAN\_SetRxFifoGlobalMask** (CAN\_Type \*base, uint32\_t mask)  
*Sets the FlexCAN receive FIFO global mask.*
- void **FLEXCAN\_SetRxIndividualMask** (CAN\_Type \*base, uint8\_t maskIdx, uint32\_t mask)  
*Sets the FlexCAN receive individual mask.*
- void **FLEXCAN\_SetTxMbConfig** (CAN\_Type \*base, uint8\_t mbIdx, bool enable)  
*Configures a FlexCAN transmit message buffer.*
- void **FLEXCAN\_SetFDTxMbConfig** (CAN\_Type \*base, uint8\_t mbIdx, bool enable)  
*Configures a FlexCAN transmit message buffer.*
- void **FLEXCAN\_SetRxMbConfig** (CAN\_Type \*base, uint8\_t mbIdx, const flexcan\_rx\_mb\_config\_t \*pRxMbConfig, bool enable)  
*Configures a FlexCAN Receive Message Buffer.*
- void **FLEXCAN\_SetFDRxMbConfig** (CAN\_Type \*base, uint8\_t mbIdx, const flexcan\_rx\_mb\_-

- `config_t *pRxMbConfig, bool enable)`  
*Configures a FlexCAN Receive Message Buffer.*
- void `FLEXCAN_SetRxFifoConfig (CAN_Type *base, const flexcan_rx_fifo_config_t *pRxFifoConfig, bool enable)`  
*Configures the FlexCAN Legacy Rx FIFO.*

## Status

- static uint32\_t `FLEXCAN_GetStatusFlags (CAN_Type *base)`  
*Gets the FlexCAN module interrupt flags.*
- static void `FLEXCAN_ClearStatusFlags (CAN_Type *base, uint32_t mask)`  
*Clears status flags with the provided mask.*
- static void `FLEXCAN_GetBusErrCount (CAN_Type *base, uint8_t *txErrBuf, uint8_t *rxErrBuf)`  
*Gets the FlexCAN Bus Error Counter value.*
- static uint64\_t `FLEXCAN_GetMbStatusFlags (CAN_Type *base, uint64_t mask)`  
*Gets the FlexCAN Message Buffer interrupt flags.*
- static void `FLEXCAN_ClearMbStatusFlags (CAN_Type *base, uint64_t mask)`  
*Clears the FlexCAN Message Buffer interrupt flags.*

## Interrupts

- static void `FLEXCAN_EnableInterrupts (CAN_Type *base, uint32_t mask)`  
*Enables FlexCAN interrupts according to the provided mask.*
- static void `FLEXCAN_DisableInterrupts (CAN_Type *base, uint32_t mask)`  
*Disables FlexCAN interrupts according to the provided mask.*
- static void `FLEXCAN_EnableMbInterrupts (CAN_Type *base, uint64_t mask)`  
*Enables FlexCAN Message Buffer interrupts.*
- static void `FLEXCAN_DisableMbInterrupts (CAN_Type *base, uint64_t mask)`  
*Disables FlexCAN Message Buffer interrupts.*

## DMA Control

- void `FLEXCAN_EnableRxFifoDMA (CAN_Type *base, bool enable)`  
*Enables or disables the FlexCAN Rx FIFO DMA request.*
- static uintptr\_t `FLEXCAN_GetRxFifoHeadAddr (CAN_Type *base)`  
*Gets the Rx FIFO Head address.*

## Bus Operations

- static void `FLEXCAN_Enable (CAN_Type *base, bool enable)`  
*Enables or disables the FlexCAN module operation.*
- `status_t FLEXCAN_WriteTxMb (CAN_Type *base, uint8_t mbIdx, const flexcan_frame_t *pTxFrame)`  
*Writes a FlexCAN Message to the Transmit Message Buffer.*
- `status_t FLEXCAN_ReadRxMb (CAN_Type *base, uint8_t mbIdx, flexcan_frame_t *pRxFrame)`

- *Reads a FlexCAN Message from Receive Message Buffer.*  
**status\_t FLEXCAN\_WriteFDTxMb** (CAN\_Type \*base, uint8\_t mbIdx, const flexcan\_fd\_frame\_t \*pTxFrame)
  - *Writes a FlexCAN FD Message to the Transmit Message Buffer.*
- **status\_t FLEXCAN\_ReadFDRxMb** (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_fd\_frame\_t \*pRxFrame)
  - *Reads a FlexCAN FD Message from Receive Message Buffer.*
- **status\_t FLEXCAN\_ReadRxFifo** (CAN\_Type \*base, flexcan\_frame\_t \*pRxFrame)
  - *Reads a FlexCAN Message from Legacy Rx FIFO.*

## Transactional

- **status\_t FLEXCAN\_TransferFDSendBlocking** (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_fd\_frame\_t \*pTxFrame)
  - *Performs a polling send transaction on the CAN bus.*
- **status\_t FLEXCAN\_TransferFDReceiveBlocking** (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_fd\_frame\_t \*pRxFrame)
  - *Performs a polling receive transaction on the CAN bus.*
- **status\_t FLEXCAN\_TransferFDSendNonBlocking** (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_mb\_transfer\_t \*pMbXfer)
  - *Sends a message using IRQ.*
- **status\_t FLEXCAN\_TransferFDReceiveNonBlocking** (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_mb\_transfer\_t \*pMbXfer)
  - *Receives a message using IRQ.*
- **void FLEXCAN\_TransferFDAbortSend** (CAN\_Type \*base, flexcan\_handle\_t \*handle, uint8\_t mbIdx)
  - *Aborts the interrupt driven message send process.*
- **void FLEXCAN\_TransferFDAbortReceive** (CAN\_Type \*base, flexcan\_handle\_t \*handle, uint8\_t mbIdx)
  - *Aborts the interrupt driven message receive process.*
- **status\_t FLEXCAN\_TransferSendBlocking** (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_frame\_t \*pTxFrame)
  - *Performs a polling send transaction on the CAN bus.*
- **status\_t FLEXCAN\_TransferReceiveBlocking** (CAN\_Type \*base, uint8\_t mbIdx, flexcan\_frame\_t \*pRxFrame)
  - *Performs a polling receive transaction on the CAN bus.*
- **status\_t FLEXCAN\_TransferReceiveFifoBlocking** (CAN\_Type \*base, flexcan\_frame\_t \*pRxFrame)
  - *Performs a polling receive transaction from Legacy Rx FIFO on the CAN bus.*
- **void FLEXCAN\_TransferCreateHandle** (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_transfer\_callback\_t callback, void \*userData)
  - *Initializes the FlexCAN handle.*
- **status\_t FLEXCAN\_TransferSendNonBlocking** (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_mb\_transfer\_t \*pMbXfer)
  - *Sends a message using IRQ.*
- **status\_t FLEXCAN\_TransferReceiveNonBlocking** (CAN\_Type \*base, flexcan\_handle\_t \*handle, flexcan\_mb\_transfer\_t \*pMbXfer)
  - *Receives a message using IRQ.*

- `status_t FLEXCAN_TransferReceiveFifoNonBlocking (CAN_Type *base, flexcan_handle_t *handle, flexcan_fifo_transfer_t *pFifoXfer)`  
*Receives a message from Rx FIFO using IRQ.*
- `status_t FLEXCAN_TransferGetReceiveFifoCount (CAN_Type *base, flexcan_handle_t *handle, size_t *count)`  
*Gets the Legacy Rx Fifo transfer status during a interrupt non-blocking receive.*
- `uint32_t FLEXCAN_GetTimeStamp (flexcan_handle_t *handle, uint8_t mbIdx)`  
*Gets the detail index of Mailbox's Timestamp by handle.*
- `void FLEXCAN_TransferAbortSend (CAN_Type *base, flexcan_handle_t *handle, uint8_t mbIdx)`  
*Aborts the interrupt driven message send process.*
- `void FLEXCAN_TransferAbortReceive (CAN_Type *base, flexcan_handle_t *handle, uint8_t mbIdx)`  
*Aborts the interrupt driven message receive process.*
- `void FLEXCAN_TransferAbortReceiveFifo (CAN_Type *base, flexcan_handle_t *handle)`  
*Aborts the interrupt driven message receive from Rx FIFO process.*
- `void FLEXCAN_TransferHandleIRQ (CAN_Type *base, flexcan_handle_t *handle)`  
*FlexCAN IRQ handle function.*

## 23.2.3 Data Structure Documentation

### 23.2.3.1 struct flexcan\_frame\_t

#### Field Documentation

- (1) `uint32_t flexcan_frame_t::timestamp`
- (2) `uint32_t flexcan_frame_t::length`
- (3) `uint32_t flexcan_frame_t::type`
- (4) `uint32_t flexcan_frame_t::format`
- (5) `uint32_t flexcan_frame_t::__pad0__`
- (6) `uint32_t flexcan_frame_t::idhit`
- (7) `uint32_t flexcan_frame_t::id`
- (8) `uint32_t flexcan_frame_t::dataWord0`
- (9) `uint32_t flexcan_frame_t::dataWord1`
- (10) `uint8_t flexcan_frame_t::dataByte3`
- (11) `uint8_t flexcan_frame_t::dataByte2`
- (12) `uint8_t flexcan_frame_t::dataByte1`
- (13) `uint8_t flexcan_frame_t::dataByte0`
- (14) `uint8_t flexcan_frame_t::dataByte7`
- (15) `uint8_t flexcan_frame_t::dataByte6`
- (16) `uint8_t flexcan_frame_t::dataByte5`
- (17) `uint8_t flexcan_frame_t::dataByte4`

### 23.2.3.2 struct flexcan\_fd\_frame\_t

The CAN FD message supporting up to sixty four bytes can be used for a data frame, depending on the length selected for the message buffers. The length should be a enumeration member, see [`\_flexcan\_fd\_frame\_length`](#).

## Field Documentation

(1) `uint32_t flexcan_fd_frame_t::timestamp`

(2) `uint32_t flexcan_fd_frame_t::length`

user can use `DLC_LENGTH_DECODE(length)` macro to get the number of valid data bytes.

(3) `uint32_t flexcan_fd_frame_t::type`

(4) `uint32_t flexcan_fd_frame_t::format`

(5) `uint32_t flexcan_fd_frame_t::srr`

(6) `uint32_t flexcan_fd_frame_t::__pad0__`

(7) `uint32_t flexcan_fd_frame_t::esi`

(8) `uint32_t flexcan_fd_frame_t::brs`

(9) `uint32_t flexcan_fd_frame_t::edl`

(10) `uint32_t flexcan_fd_frame_t::id`

(11) `uint32_t flexcan_fd_frame_t::dataWord[16]`

(12) `uint8_t flexcan_fd_frame_t::dataByte3`

(13) `uint8_t flexcan_fd_frame_t::dataByte2`

(14) `uint8_t flexcan_fd_frame_t::dataByte1`

(15) `uint8_t flexcan_fd_frame_t::dataByte0`

(16) `uint8_t flexcan_fd_frame_t::dataByte7`

(17) `uint8_t flexcan_fd_frame_t::dataByte6`

(18) `uint8_t flexcan_fd_frame_t::dataByte5`

(19) `uint8_t flexcan_fd_frame_t::dataByte4`

### 23.2.3.3 struct flexcan\_timing\_config\_t

#### Data Fields

- `uint16_t preDivider`

*Classic CAN or CAN FD nominal phase bit rate prescaler.*

- `uint8_t rJumpwidth`

*Classic CAN or CAN FD nominal phase Re-sync Jump Width.*

- `uint8_t phaseSeg1`

- *Classic CAN or CAN FD nominal phase Segment 1.*
- `uint8_t phaseSeg2`  
*Classic CAN or CAN FD nominal phase Segment 2.*
- `uint8_t propSeg`  
*Classic CAN or CAN FD nominal phase Propagation Segment.*
- `uint16_t fpreDivider`  
*CAN FD data phase bit rate prescaler.*
- `uint8_t frJumpwidth`  
*CAN FD data phase Re-sync Jump Width.*
- `uint8_t fphaseSeg1`  
*CAN FD data phase Phase Segment 1.*
- `uint8_t fphaseSeg2`  
*CAN FD data phase Phase Segment 2.*
- `uint8_t fpropSeg`  
*CAN FD data phase Propagation Segment.*

### Field Documentation

- (1) `uint16_t flexcan_timing_config_t::preDivider`
- (2) `uint8_t flexcan_timing_config_t::rJumpwidth`
- (3) `uint8_t flexcan_timing_config_t::phaseSeg1`
- (4) `uint8_t flexcan_timing_config_t::phaseSeg2`
- (5) `uint8_t flexcan_timing_config_t::propSeg`
- (6) `uint16_t flexcan_timing_config_t::fpreDivider`
- (7) `uint8_t flexcan_timing_config_t::frJumpwidth`
- (8) `uint8_t flexcan_timing_config_t::fphaseSeg1`
- (9) `uint8_t flexcan_timing_config_t::fphaseSeg2`
- (10) `uint8_t flexcan_timing_config_t::fpropSeg`

#### 23.2.3.4 struct flexcan\_config\_t

**Deprecated** Do not use the baudRate. It has been superceded bitRate

Do not use the baudRateFD. It has been superceded bitRateFD

### Data Fields

- `flexcan_clock_source_t clkSrc`  
*Clock source for FlexCAN Protocol Engine.*
- `flexcan_wake_up_source_t wakeupSrc`  
*Wake up source selection.*
- `uint8_t maxMbNum`

*The maximum number of Message Buffers used by user.*

- bool **enableLoopBack**  
*Enable or Disable Loop Back Self Test Mode.*
- bool **enableTimerSync**  
*Enable or Disable Timer Synchronization.*
- bool **enableSelfWakeup**  
*Enable or Disable Self Wakeup Mode.*
- bool **enableIndividMask**  
*Enable or Disable Rx Individual Mask and Queue feature.*
- bool **disableSelfReception**  
*Enable or Disable Self Reflection.*
- bool **enableListenOnlyMode**  
*Enable or Disable Listen Only Mode.*
- bool **enableSupervisorMode**  
*Enable or Disable Supervisor Mode, enable this mode will make registers allow only Supervisor access.*
- bool **enableDoze**  
*Enable or Disable Doze Mode.*
- uint32\_t **baudRate**  
*FlexCAN bit rate in bps, for classical CAN or CANFD nominal phase.*
- uint32\_t **baudRateFD**  
*FlexCAN FD bit rate in bps, for CANFD data phase.*
- uint32\_t **bitRate**  
*FlexCAN bit rate in bps, for classical CAN or CANFD nominal phase.*
- uint32\_t **bitRateFD**  
*FlexCAN FD bit rate in bps, for CANFD data phase.*

## Field Documentation

- (1) `uint32_t flexcan_config_t::baudRate`
- (2) `uint32_t flexcan_config_t::baudRateFD`
- (3) `uint32_t flexcan_config_t::bitRate`
- (4) `uint32_t flexcan_config_t::bitRateFD`
- (5) `flexcan_clock_source_t flexcan_config_t::clkSrc`
- (6) `flexcan_wake_up_source_t flexcan_config_t::wakeupSrc`
- (7) `uint8_t flexcan_config_t::maxMbNum`
- (8) `bool flexcan_config_t::enableLoopBack`
- (9) `bool flexcan_config_t::enableTimerSync`
- (10) `bool flexcan_config_t::enableSelfWakeup`
- (11) `bool flexcan_config_t::enableIndividMask`
- (12) `bool flexcan_config_t::disableSelfReception`
- (13) `bool flexcan_config_t::enableListenOnlyMode`
- (14) `bool flexcan_config_t::enableSupervisorMode`
- (15) `bool flexcan_config_t::enableDoze`

### 23.2.3.5 struct flexcan\_rx\_mb\_config\_t

This structure is used as the parameter of [FLEXCAN\\_SetRxMbConfig\(\)](#) function. The [FLEXCAN\\_SetRxMbConfig\(\)](#) function is used to configure FlexCAN Receive Message Buffer. The function abort previous receiving process, clean the Message Buffer and activate the Rx Message Buffer using given Message Buffer setting.

## Data Fields

- `uint32_t id`  
*CAN Message Buffer Frame Identifier, should be set using [FLEXCAN\\_ID\\_EXT\(\)](#) or [FLEXCAN\\_ID\\_STD\(\)](#) macro.*
- `flexcan_frame_format_t format`  
*CAN Frame Identifier format(Standard or Extend).*
- `flexcan_frame_type_t type`  
*CAN Frame Type(Data or Remote).*

**Field Documentation**

- (1) `uint32_t flexcan_rx_mb_config_t::id`
- (2) `flexcan_frame_format_t flexcan_rx_mb_config_t::format`
- (3) `flexcan_frame_type_t flexcan_rx_mb_config_t::type`

**23.2.3.6 struct flexcan\_rx\_fifo\_config\_t****Data Fields**

- `uint32_t * idFilterTable`  
*Pointer to the FlexCAN Legacy Rx FIFO identifier filter table.*
- `uint8_t idFilterNum`  
*The FlexCAN Legacy Rx FIFO Filter elements quantity.*
- `flexcan_rx_fifo_filter_type_t idFilterType`  
*The FlexCAN Legacy Rx FIFO Filter type.*
- `flexcan_rx_fifo_priority_t priority`  
*The FlexCAN Legacy Rx FIFO receive priority.*

**Field Documentation**

- (1) `uint32_t* flexcan_rx_fifo_config_t::idFilterTable`
- (2) `uint8_t flexcan_rx_fifo_config_t::idFilterNum`
- (3) `flexcan_rx_fifo_filter_type_t flexcan_rx_fifo_config_t::idFilterType`
- (4) `flexcan_rx_fifo_priority_t flexcan_rx_fifo_config_t::priority`

**23.2.3.7 struct flexcan\_mb\_transfer\_t****Data Fields**

- `flexcan_frame_t * frame`  
*The buffer of CAN Message to be transfer.*
- `uint8_t mbIdx`  
*The index of Message buffer used to transfer Message.*

**Field Documentation**

- (1) `flexcan_frame_t* flexcan_mb_transfer_t::frame`
- (2) `uint8_t flexcan_mb_transfer_t::mbIdx`

**23.2.3.8 struct flexcan\_fifo\_transfer\_t****Data Fields**

- `flexcan_frame_t * frame`

- **size\_t frameNum**  
*The buffer of CAN Message to be received from Legacy Rx FIFO.*
- **size\_t frameNum**  
*Number of CAN Message need to be received from Legacy or Enhanced Rx FIFO.*

## Field Documentation

- (1) **flexcan\_frame\_t\* flexcan\_fifo\_transfer\_t::frame**
- (2) **size\_t flexcan\_fifo\_transfer\_t::frameNum**

### 23.2.3.9 struct \_flexcan\_handle

FlexCAN handle structure definition.

## Data Fields

- **flexcan\_transfer\_callback\_t callback**  
*Callback function.*
- **void \*userData**  
*FlexCAN callback function parameter.*
- **flexcan\_frame\_t \*volatile mbFrameBuf [CAN\_WORD1\_COUNT]**  
*The buffer for received CAN data from Message Buffers.*
- **flexcan\_fd\_frame\_t \*volatile mbFDFrameBuf [CAN\_WORD1\_COUNT]**  
*The buffer for received CAN FD data from Message Buffers.*
- **flexcan\_frame\_t \*volatile rxFifoFrameBuf**  
*The buffer for received CAN data from Legacy Rx FIFO.*
- **size\_t rxFifoFrameNum**  
*The number of CAN messages remaining to be received from Legacy or Enhanced Rx FIFO.*
- **size\_t rxFifoTransferTotalNum**  
*Total CAN Message number need to be received from Legacy or Enhanced Rx FIFO.*
- **volatile uint8\_t mbState [CAN\_WORD1\_COUNT]**  
*Message Buffer transfer state.*
- **volatile uint8\_t rxFifoState**  
*Rx FIFO transfer state.*
- **volatile uint32\_t timestamp [CAN\_WORD1\_COUNT]**  
*Mailbox transfer timestamp.*

## Field Documentation

- (1) `flexcan_transfer_callback_t flexcan_handle_t::callback`
- (2) `void* flexcan_handle_t::userData`
- (3) `flexcan_frame_t* volatile flexcan_handle_t::mbFrameBuf[CAN_WORD1_COUNT]`
- (4) `flexcan_fd_frame_t* volatile flexcan_handle_t::mbFDFrameBuf[CAN_WORD1_COUNT]`
- (5) `flexcan_frame_t* volatile flexcan_handle_t::rxFifoFrameBuf`
- (6) `size_t flexcan_handle_t::rxFifoFrameNum`
- (7) `size_t flexcan_handle_t::rxFifoTransferTotalNum`
- (8) `volatile uint8_t flexcan_handle_t::mbState[CAN_WORD1_COUNT]`
- (9) `volatile uint8_t flexcan_handle_t::rxFifoState`
- (10) `volatile uint32_t flexcan_handle_t::timestamp[CAN_WORD1_COUNT]`

## 23.2.4 Macro Definition Documentation

**23.2.4.1 #define FSL\_FLEXCAN\_DRIVER\_VERSION (MAKE\_VERSION(2, 11, 1))**

**23.2.4.2 #define DLC\_LENGTH\_DECODE( *dlic* ) (((dlic) <= 8U) ? (dlic) : (((dlic) <= 12U) ? ((dlic)-6U) \* 4U) : (((dlic)-11U) \* 16U)))**

**23.2.4.3 #define FLEXCAN\_ID\_STD( *id* ) (((uint32\_t)((uint32\_t)(*id*)) << CAN\_ID\_STD\_SHIFT)) & CAN\_ID\_STD\_MASK)**

Standard Frame ID helper macro.

**23.2.4.4 #define FLEXCAN\_ID\_EXT( *id* )**

**Value:**

```
((uint32_t)((uint32_t)(id)) << CAN_ID_EXT_SHIFT)) & \
(CAN_ID_EXT_MASK | CAN_ID_STD_MASK))
```

**23.2.4.5 #define FLEXCAN\_RX\_MB\_STD\_MASK( *id*, *rtr*, *ide* )**

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
FLEXCAN_ID_STD(id))
```

Standard Rx Message Buffer Mask helper macro.

#### 23.2.4.6 #define FLEXCAN\_RX\_MB\_EXT\_MASK( *id*, *rtr*, *ide* )

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
FLEXCAN_ID_EXT(id)
```

#### 23.2.4.7 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A( *id*, *rtr*, *ide* )

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
(FLEXCAN_ID_STD(id) << 1))
```

Standard Rx FIFO Mask helper macro Type A helper macro.

#### 23.2.4.8 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_HIGH( *id*, *rtr*, *ide* )

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
(((uint32_t)(id)&0x7FF) << 19))
```

#### 23.2.4.9 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_LOW( *id*, *rtr*, *ide* )

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 15) | (uint32_t)((uint32_t)(ide) << 14)) | \
(((uint32_t)(id)&0x7FF) << 3))
```

- 23.2.4.10 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_HIGH( *id* ) (((uint32\_t)(*id*)&0x7F8) << 21)**
- 23.2.4.11 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_HIGH( *id* ) (((uint32\_t)(*id*)&0x7F8) << 13)**
- 23.2.4.12 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_LOW( *id* ) (((uint32\_t)(*id*)&0x7F8) << 5)**
- 23.2.4.13 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_LOW( *id* ) (((uint32\_t)(*id*)&0x7F8) >> 3)**
- 23.2.4.14 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_A( *id*, *rtr*, *ide* )**

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
  (FLEXCAN\_ID\_EXT(id) << 1))
```

- 23.2.4.15 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_HIGH( *id*, *rtr*, *ide* )**

**Value:**

```
( \
  ((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
  ((FLEXCAN\_ID\_EXT(id) & 0x1FFF8000) \
  << 1)) \ \
```

- 23.2.4.16 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_LOW( *id*, *rtr*, *ide* )**

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 15) | (uint32_t)((uint32_t)(ide) << 14)) | \
  ((FLEXCAN\_ID\_EXT(id) & 0x1FFF8000) >>
  15)) \
```

- 23.2.4.17 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_HIGH( *id* ) (([FLEXCAN\\_ID\\_EXT](#)(*id*) & 0x1FE00000) << 3)**

- 23.2.4.18 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_HIGH( *id* )**

**Value:**

```
((FLEXCAN\_ID\_EXT(id) & 0x1FE00000) >>
  5) \
```

**23.2.4.19 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_LOW( *id* )****Value:**

```
((FLEXCAN_ID_EXT(id) & 0x1FE00000) >> 13) \
```

**23.2.4.20 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_LOW( *id* ) ((FLEXCAN\_ID\_EXT(*id*) & 0x1FE00000) >> 21)****23.2.4.21 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_A( *id*, *rtr*, *ide* ) FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A(*id*, *rtr*, *ide*)**

Standard Rx FIFO Filter helper macro Type A helper macro.

**23.2.4.22 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_B\_HIGH( *id*, *rtr*, *ide* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_HIGH(id, rtr, ide) \
```

**23.2.4.23 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_B\_LOW( *id*, *rtr*, *ide* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_LOW(id, rtr, ide) \
```

**23.2.4.24 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_HIGH( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_HIGH(id) \
```

**23.2.4.25 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_MID\_HIGH( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_HIGH(id) \
```

**23.2.4.26 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_MID\_LOW( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_LOW(           \
    id)
```

**23.2.4.27 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_LOW( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_LOW(           \
    id)
```

**23.2.4.28 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_A( *id*, *rtr*, *ide* ) FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_A(*id*, *rtr*, *ide*)****23.2.4.29 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_B\_HIGH( *id*, *rtr*, *ide* )****Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_HIGH(           \
    id, rtr, ide)
```

**23.2.4.30 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_B\_LOW( *id*, *rtr*, *ide* )****Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_LOW(           \
    id, rtr, ide)
```

**23.2.4.31 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_HIGH( *id* )****Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_HIGH(           \
    id)
```

**23.2.4.32 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_MID\_HIGH( *id* )****Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_HIGH(           \
    id)
```

**23.2.4.33 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_MID\_LOW( *id* )****Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_LOW(           \
    id)
```

**23.2.4.34 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_LOW( *id* ) FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_LOW(id)****23.2.4.35 #define FLEXCAN\_ERROR\_AND\_STATUS\_INIT\_FLAG****Value:**

```
((uint32_t)kFLEXCAN_ErrorOverrunFlag | (uint32_t)
    kFLEXCAN_FDErrorIntFlag | (uint32_t)
    kFLEXCAN_BusoffDoneIntFlag | \
(uint32_t)kFLEXCAN_TxWarningIntFlag | (uint32_t)
    kFLEXCAN_RxWarningIntFlag | (uint32_t)
    kFLEXCAN_BusOffIntFlag | \
(uint32_t)kFLEXCAN_ErrorIntFlag | FLEXCAN_MEMORY_ERROR_INIT_FLAG)
```

**23.2.4.36 #define FLEXCAN\_MEMORY\_ENHANCED\_RX\_FIFO\_INIT\_FLAG (0U)****23.2.4.37 #define FLEXCAN\_CALLBACK( *x* ) void(*x*)(CAN\_Type \* **base**, flexcan\_handle\_t  
\* **handle**, status\_t **status**, uint32\_t **result**, void \***userData**)**

The FlexCAN transfer callback returns a value from the underlying layer. If the status equals to kStatus\_FLEXCAN\_ErrorStatus, the result parameter is the Content of FlexCAN status register which can be used to get the working status(or error status) of FlexCAN module. If the status equals to other FlexCAN Message Buffer transfer status, the result is the index of Message Buffer that generate transfer event. If the status equals to other FlexCAN Message Buffer transfer status, the result is meaningless and should be Ignored.

## 23.2.5 Enumeration Type Documentation

### 23.2.5.1 anonymous enum

Enumerator

*kStatus\_FLEXCAN\_TxBusy* Tx Message Buffer is Busy.  
*kStatus\_FLEXCAN\_TxIdle* Tx Message Buffer is Idle.  
*kStatus\_FLEXCAN\_TxSwitchToRx* Remote Message is send out and Message buffer changed to Receive one.  
*kStatus\_FLEXCAN\_RxBusy* Rx Message Buffer is Busy.  
*kStatus\_FLEXCAN\_RxIdle* Rx Message Buffer is Idle.  
*kStatus\_FLEXCAN\_RxOverflow* Rx Message Buffer is Overflowed.  
*kStatus\_FLEXCAN\_RxFifoBusy* Rx Message FIFO is Busy.  
*kStatus\_FLEXCAN\_RxFifoIdle* Rx Message FIFO is Idle.  
*kStatus\_FLEXCAN\_RxFifoOverflow* Rx Message FIFO is overflowed.  
*kStatus\_FLEXCAN\_RxFifoWarning* Rx Message FIFO is almost overflowed.  
*kStatus\_FLEXCAN\_RxFifoDisabled* Rx Message FIFO is disabled during reading.  
*kStatus\_FLEXCAN\_ErrorStatus* FlexCAN Module Error and Status.  
*kStatus\_FLEXCAN\_WakeUp* FlexCAN is waken up from STOP mode.  
*kStatus\_FLEXCAN\_UnHandled* UnHadled Interrupt asserted.  
*kStatus\_FLEXCAN\_RxRemote* Rx Remote Message Received in Mail box.

### 23.2.5.2 enum flexcan\_frame\_format\_t

Enumerator

*kFLEXCAN\_FrameFormatStandard* Standard frame format attribute.  
*kFLEXCAN\_FrameFormatExtend* Extend frame format attribute.

### 23.2.5.3 enum flexcan\_frame\_type\_t

Enumerator

*kFLEXCAN\_FrameTypeData* Data frame type attribute.  
*kFLEXCAN\_FrameTypeRemote* Remote frame type attribute.

### 23.2.5.4 enum flexcan\_clock\_source\_t

**Deprecated** Do not use the kFLEXCAN\_ClkSrcOs. It has been superceded kFLEXCAN\_ClkSrc0  
Do not use the kFLEXCAN\_ClkSrcPeri. It has been superceded kFLEXCAN\_ClkSrc1

Enumerator

***kFLEXCAN\_ClkSrcOsc*** FlexCAN Protocol Engine clock from Oscillator.

***kFLEXCAN\_ClkSrcPeri*** FlexCAN Protocol Engine clock from Peripheral Clock.

***kFLEXCAN\_ClkSrc0*** FlexCAN Protocol Engine clock selected by user as SRC == 0.

***kFLEXCAN\_ClkSrc1*** FlexCAN Protocol Engine clock selected by user as SRC == 1.

### 23.2.5.5 enum flexcan\_wake\_up\_source\_t

Enumerator

***kFLEXCAN\_WakeupSrcUnfiltered*** FlexCAN uses unfiltered Rx input to detect edge.

***kFLEXCAN\_WakeupSrcFiltered*** FlexCAN uses filtered Rx input to detect edge.

### 23.2.5.6 enum flexcan\_rx\_fifo\_filter\_type\_t

Enumerator

***kFLEXCAN\_RxFifoFilterTypeA*** One full ID (standard and extended) per ID Filter element.

***kFLEXCAN\_RxFifoFilterTypeB*** Two full standard IDs or two partial 14-bit ID slices per ID Filter Table element.

***kFLEXCAN\_RxFifoFilterTypeC*** Four partial 8-bit Standard or extended ID slices per ID Filter Table element.

***kFLEXCAN\_RxFifoFilterTypeD*** All frames rejected.

### 23.2.5.7 enum flexcan\_mb\_size\_t

Enumerator

***kFLEXCAN\_8BperMB*** Selects 8 bytes per Message Buffer.

***kFLEXCAN\_16BperMB*** Selects 16 bytes per Message Buffer.

***kFLEXCAN\_32BperMB*** Selects 32 bytes per Message Buffer.

***kFLEXCAN\_64BperMB*** Selects 64 bytes per Message Buffer.

### 23.2.5.8 enum \_flexcan\_fd\_frame\_length

For Tx, when the Data size corresponding to DLC value stored in the MB selected for transmission is larger than the MB Payload size, FlexCAN adds the necessary number of bytes with constant 0xCC pattern to complete the expected DLC. For Rx, when the Data size corresponding to DLC value received from the CAN bus is larger than the MB Payload size, the high order bytes that do not fit the Payload size will lose.

Enumerator

***kFLEXCAN\_0BperFrame*** Frame contains 0 valid data bytes.

<i>kFLEXCAN_1BperFrame</i>	Frame contains 1 valid data bytes.
<i>kFLEXCAN_2BperFrame</i>	Frame contains 2 valid data bytes.
<i>kFLEXCAN_3BperFrame</i>	Frame contains 3 valid data bytes.
<i>kFLEXCAN_4BperFrame</i>	Frame contains 4 valid data bytes.
<i>kFLEXCAN_5BperFrame</i>	Frame contains 5 valid data bytes.
<i>kFLEXCAN_6BperFrame</i>	Frame contains 6 valid data bytes.
<i>kFLEXCAN_7BperFrame</i>	Frame contains 7 valid data bytes.
<i>kFLEXCAN_8BperFrame</i>	Frame contains 8 valid data bytes.
<i>kFLEXCAN_12BperFrame</i>	Frame contains 12 valid data bytes.
<i>kFLEXCAN_16BperFrame</i>	Frame contains 16 valid data bytes.
<i>kFLEXCAN_20BperFrame</i>	Frame contains 20 valid data bytes.
<i>kFLEXCAN_24BperFrame</i>	Frame contains 24 valid data bytes.
<i>kFLEXCAN_32BperFrame</i>	Frame contains 32 valid data bytes.
<i>kFLEXCAN_48BperFrame</i>	Frame contains 48 valid data bytes.
<i>kFLEXCAN_64BperFrame</i>	Frame contains 64 valid data bytes.

### 23.2.5.9 enum flexcan\_rx\_fifo\_priority\_t

The matching process starts from the Rx MB(or Enhanced/Legacy Rx FIFO) with higher priority. If no MB(or Enhanced/Legacy Rx FIFO filter) is satisfied, the matching process goes on with the Enhanced-/Legacy Rx FIFO(or Rx MB) with lower priority.

Enumerator

<i>kFLEXCAN_RxFifoPrioLow</i>	Matching process start from Rx Message Buffer first.
<i>kFLEXCAN_RxFifoPrioHigh</i>	Matching process start from Enhanced/Legacy Rx FIFO first.

### 23.2.5.10 enum \_flexcan\_interrupt\_enable

This provides constants for the FlexCAN interrupt enable enumerations for use in the FlexCAN functions.

Note

FlexCAN Message Buffers and Legacy Rx FIFO interrupts not included in.

Enumerator

<i>kFLEXCAN_BusOffInterruptEnable</i>	Bus Off interrupt, use bit 15.
<i>kFLEXCAN_ErrorInterruptEnable</i>	CAN Error interrupt, use bit 14.
<i>kFLEXCAN_TxWarningInterruptEnable</i>	Tx Warning interrupt, use bit 11.
<i>kFLEXCAN_RxWarningInterruptEnable</i>	Rx Warning interrupt, use bit 10.
<i>kFLEXCAN_WakeUpInterruptEnable</i>	Self Wake Up interrupt, use bit 26.
<i>kFLEXCAN_FDErrorInterruptEnable</i>	CAN FD Error interrupt, use bit 31.

### 23.2.5.11 enum \_flexcan\_flags

This provides constants for the FlexCAN status flags for use in the FlexCAN functions.

Note

The CPU read action clears the bits corresponding to the FLEXCAN\_ErrorFlag macro, therefore user need to read status flags and distinguish which error is occur using [\\_flexcan\\_error\\_flags](#) enumerations.

Enumerator

- kFLEXCAN\_ErrorOverrunFlag*** Error Overrun Status.
- kFLEXCAN\_FDErrorIntFlag*** CAN FD Error Interrupt Flag.
- kFLEXCAN\_BusoffDoneIntFlag*** Bus Off process completed Interrupt Flag.
- kFLEXCAN\_SynchFlag*** CAN Synchronization Status.
- kFLEXCAN\_TxWarningIntFlag*** Tx Warning Interrupt Flag.
- kFLEXCAN\_RxWarningIntFlag*** Rx Warning Interrupt Flag.
- kFLEXCAN\_IdleFlag*** FlexCAN In IDLE Status.
- kFLEXCAN\_FaultConfinementFlag*** FlexCAN Fault Confinement State.
- kFLEXCAN\_TransmittingFlag*** FlexCAN In Transmission Status.
- kFLEXCAN\_ReceivingFlag*** FlexCAN In Reception Status.
- kFLEXCAN\_BusOffIntFlag*** Bus Off Interrupt Flag.
- kFLEXCAN\_ErrorIntFlag*** CAN Error Interrupt Flag.
- kFLEXCAN\_WakeUpIntFlag*** Self Wake-Up Interrupt Flag.

### 23.2.5.12 enum \_flexcan\_error\_flags

The FlexCAN Error Status enumerations is used to report current error of the FlexCAN bus. This enumerations should be used with KFLEXCAN\_ErrorFlag in [\\_flexcan\\_flags](#) enumerations to determine which error is generated.

Enumerator

- kFLEXCAN\_FDStuffingError*** Stuffing Error.
- kFLEXCAN\_FDFormError*** Form Error.
- kFLEXCAN\_FDCrcError*** Cyclic Redundancy Check Error.
- kFLEXCAN\_FDBit0Error*** Unable to send dominant bit.
- kFLEXCAN\_FDBit1Error*** Unable to send recessive bit.
- kFLEXCAN\_TxErrorWarningFlag*** Tx Error Warning Status.
- kFLEXCAN\_RxErrorWarningFlag*** Rx Error Warning Status.
- kFLEXCAN\_StuffingError*** Stuffing Error.
- kFLEXCAN\_FormError*** Form Error.
- kFLEXCAN\_CrcError*** Cyclic Redundancy Check Error.
- kFLEXCAN\_AckError*** Received no ACK on transmission.
- kFLEXCAN\_Bit0Error*** Unable to send dominant bit.
- kFLEXCAN\_Bit1Error*** Unable to send recessive bit.

### 23.2.5.13 anonymous enum

The FlexCAN Legacy Rx FIFO Status enumerations are used to determine the status of the Rx FIFO. Because Rx FIFO occupy the MB0 ~ MB7 (Rx Fifo filter also occupies more Message Buffer space), Rx FIFO status flags are mapped to the corresponding Message Buffer status flags.

Enumerator

- kFLEXCAN\_RxFifoOverflowFlag* Rx FIFO overflow flag.
- kFLEXCAN\_RxFifoWarningFlag* Rx FIFO almost full flag.
- kFLEXCAN\_RxFifoFrameAvlFlag* Frames available in Rx FIFO flag.

## 23.2.6 Function Documentation

### 23.2.6.1 **bool FLEXCAN\_IsInstanceHasFDMode ( CAN\_Type \* *base* )**

Note

Use this API only if different soc parts share the SOC part name macro define. Otherwise, a different SOC part name can be used to determine at compile time whether the FlexCAN instance supports CAN FD mode or not. If need use this API to determine if CAN FD mode is supported, the FLEXCAN\_Init function needs to be executed first, and then call this API and use the return to value determines whether to supports CAN FD mode, if return true, continue calling FLEXCAN\_FDIInit to enable CAN FD mode.

Parameters

<i>base</i>	FlexCAN peripheral base address.
-------------	----------------------------------

Returns

return TRUE if instance support CAN FD mode, FALSE if instance only support classic CAN (2.0) mode.

### 23.2.6.2 **void FLEXCAN\_EnterFreezeMode ( CAN\_Type \* *base* )**

This function makes the FlexCAN work under Freeze Mode.

Parameters

<i>base</i>	FlexCAN peripheral base address.
-------------	----------------------------------

### 23.2.6.3 void FLEXCAN\_ExitFreezeMode ( CAN\_Type \* *base* )

This function makes the FlexCAN leave Freeze Mode.

Parameters

<i>base</i>	FlexCAN peripheral base address.
-------------	----------------------------------

### 23.2.6.4 uint32\_t FLEXCANGetInstance ( CAN\_Type \* *base* )

Parameters

<i>base</i>	FlexCAN peripheral base address.
-------------	----------------------------------

Returns

FlexCAN instance.

### 23.2.6.5 bool FLEXCAN\_CalculateImprovedTimingValues ( CAN\_Type \* *base*, uint32\_t *bitRate*, uint32\_t *sourceClock\_Hz*, flexcan\_timing\_config\_t \* *pTimingConfig* )

This function use to calculates the Classical CAN timing values according to the given bit rate. The Calculated timing values will be set in CTRL1/CBT/ENCBT register. The calculation is based on the recommendation of the CiA 301 v4.2.0 and previous version document.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>bitRate</i>	The classical CAN speed in bps defined by user, should be less than or equal to 1-Mbps.
<i>sourceClock_Hz</i>	The Source clock frequency in Hz.

<i>pTimingConfig</i>	Pointer to the FlexCAN timing configuration structure.
----------------------	--

## Returns

TRUE if timing configuration found, FALSE if failed to find configuration.

### 23.2.6.6 void FLEXCAN\_Init ( CAN\_Type \* *base*, const flexcan\_config\_t \* *pConfig*, uint32\_t *sourceClock\_Hz* )

This function initializes the FlexCAN module with user-defined settings. This example shows how to set up the `flexcan_config_t` parameters and how to call the `FLEXCAN_Init` function by passing in these parameters.

```
*     flexcan_config_t flexcanConfig;
*     flexcanConfig.clkSrc          = kFLEXCAN_ClkSrc0;
*     flexcanConfig.bitRate         = 1000000U;
*     flexcanConfig.maxMbNum       = 16;
*     flexcanConfig.enableLoopBack = false;
*     flexcanConfig.enableSelfWakeup = false;
*     flexcanConfig.enableIndividMask = false;
*     flexcanConfig.enableDoze      = false;
*     flexcanConfig.disableSelfReception = false;
*     flexcanConfig.enableListenOnlyMode = false;
*     flexcanConfig.timingConfig    = timingConfig;
*     FLEXCAN_Init(CAN0, &flexcanConfig, 40000000UL);
*
```

## Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>pConfig</i>	Pointer to the user-defined configuration structure.
<i>sourceClock_Hz</i>	FlexCAN Protocol Engine clock source frequency in Hz.

### 23.2.6.7 bool FLEXCAN\_FDCalculateImprovedTimingValues ( CAN\_Type \* *base*, uint32\_t *bitRate*, uint32\_t *bitRateFD*, uint32\_t *sourceClock\_Hz*, flexcan\_timing\_config\_t \* *pTimingConfig* )

This function use to calculates the CANFD timing values according to the given nominal phase bit rate and data phase bit rate. The Calculated timing values will be set in CBT/ENCBT and FDCBT/EDCBT registers. The calculation is based on the recommendation of the CiA 1301 v1.0.0 document.

## Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>bitRate</i>	The CANFD bus control speed in bps defined by user.
<i>bitRateFD</i>	The CAN FD data phase speed in bps defined by user. Equal to bitRate means disable bit rate switching.
<i>sourceClock_Hz</i>	The Source clock frequency in Hz.
<i>pTimingConfig</i>	Pointer to the FlexCAN timing configuration structure.

## Returns

TRUE if timing configuration found, FALSE if failed to find configuration

### 23.2.6.8 void FLEXCAN\_FDInit ( CAN\_Type \* *base*, const flexcan\_config\_t \* *pConfig*, uint32\_t *sourceClock\_Hz*, flexcan\_mb\_size\_t *dataSize*, bool *brs* )

This function initializes the FlexCAN module with user-defined settings. This example shows how to set up the `flexcan_config_t` parameters and how to call the `FLEXCAN_FDInit` function by passing in these parameters.

```
*   flexcanConfig_t flexcanConfig;
*   flexcanConfig.clkSrc          = kFLEXCAN_ClkSrc0;
*   flexcanConfig.bitRate         = 1000000U;
*   flexcanConfig.bitRateFD       = 2000000U;
*   flexcanConfig.maxMbNum        = 16;
*   flexcanConfig.enableLoopBack  = false;
*   flexcanConfig.enableSelfWakeUp = false;
*   flexcanConfig.enableIndividMask = false;
*   flexcanConfig.disableSelfReception = false;
*   flexcanConfig.enableListenOnlyMode = false;
*   flexcanConfig.enableDoze       = false;
*   flexcanConfig.timingConfig     = timingConfig;
*   FLEXCAN_FDInit(CAN0, &flexcanConfig, 80000000UL,
*                  kFLEXCAN_16BperMB, true);
*
```

## Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>pConfig</i>	Pointer to the user-defined configuration structure.

<i>sourceClock_-Hz</i>	FlexCAN Protocol Engine clock source frequency in Hz.
<i>dataSize</i>	FlexCAN Message Buffer payload size. The actual transmitted or received CAN FD frame data size needs to be less than or equal to this value.
<i>brs</i>	True if bit rate switch is enabled in FD mode.

### 23.2.6.9 void FLEXCAN\_Deinit ( CAN\_Type \* *base* )

This function disables the FlexCAN module clock and sets all register values to the reset value.

Parameters

<i>base</i>	FlexCAN peripheral base address.
-------------	----------------------------------

### 23.2.6.10 void FLEXCAN\_GetDefaultConfig ( flexcan\_config\_t \* *pConfig* )

This function initializes the FlexCAN configuration structure to default values. The default values are as follows. *flexcanConfig->clkSrc* = kFLEXCAN\_ClkSrc0; *flexcanConfig->bitRate* = 1000000U; *flexcanConfig->bitRateFD* = 2000000U; *flexcanConfig->maxMbNum* = 16; *flexcanConfig->enableLoopBack* = false; *flexcanConfig->enableSelfWakeup* = false; *flexcanConfig->enableIndividMask* = false; *flexcanConfig->disableSelfReception* = false; *flexcanConfig->enableListenOnlyMode* = false; *flexcanConfig->enableDoze* = false; *flexcanConfig->enableMemoryErrorControl* = true; *flexcanConfig->enableNon-CorrectableErrorEnterFreeze* = true; *flexcanConfig.timingConfig* = *timingConfig*;

Parameters

<i>pConfig</i>	Pointer to the FlexCAN configuration structure.
----------------	---

### 23.2.6.11 void FLEXCAN\_SetTimingConfig ( CAN\_Type \* *base*, const flexcan\_timing\_config\_t \* *pConfig* )

This function gives user settings to classical CAN or CAN FD nominal phase timing characteristic. The function is for an experienced user. For less experienced users, call the [FLEXCAN\\_SetBitRate\(\)](#) instead.

Note

Calling [FLEXCAN\\_SetTimingConfig\(\)](#) overrides the bit rate set in [FLEXCAN\\_Init\(\)](#) or [FLEXCAN\\_SetBitRate\(\)](#).

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>pConfig</i>	Pointer to the timing configuration structure.

### 23.2.6.12 status\_t FLEXCAN\_SetBitRate ( CAN\_Type \* *base*, uint32\_t *sourceClock\_Hz*, uint32\_t *bitRate\_Bps* )

This function set the bit rate of classical CAN frame or CAN FD frame nominal phase base on [FLEXCAN\\_CalculateImprovedTimingValues\(\)](#) API calculated timing values.

Note

Calling [FLEXCAN\\_SetBitRate\(\)](#) overrides the bit rate set in [FLEXCAN\\_Init\(\)](#).

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>sourceClock_Hz</i>	Source Clock in Hz.
<i>bitRate_Bps</i>	Bit rate in Bps.

Returns

kStatus\_Success - Set CAN baud rate (only Nominal phase) successfully.

### 23.2.6.13 void FLEXCAN\_SetFDTimingConfig ( CAN\_Type \* *base*, const flexcan\_timing\_config\_t \* *pConfig* )

This function gives user settings to CANFD data phase timing characteristic. The function is for an experienced user. For less experienced users, call the [FLEXCAN\\_SetFDBitRate\(\)](#) to set both Nominal-/Data bit Rate instead.

Note

Calling [FLEXCAN\\_SetFDTimingConfig\(\)](#) overrides the data phase bit rate set in [FLEXCAN\\_FDIInit\(\)](#)/FLEXCAN\_SetFDBitRate().

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>pConfig</i>	Pointer to the timing configuration structure.

### 23.2.6.14 status\_t FLEXCAN\_SetFDBitRate ( CAN\_Type \* *base*, uint32\_t *sourceClock\_Hz*, uint32\_t *bitRateN\_Bps*, uint32\_t *bitRateD\_Bps* )

This function set the baud rate of FLEXCAN FD base on [FLEXCAN\\_FDCalculateImprovedTimingValues\(\)](#) API calculated timing values.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>sourceClock_Hz</i>	Source Clock in Hz.
<i>bitRateN_Bps</i>	Nominal bit Rate in Bps.
<i>bitRateD_Bps</i>	Data bit Rate in Bps.

Returns

kStatus\_Success - Set CAN FD bit rate (include Nominal and Data phase) successfully.

### 23.2.6.15 void FLEXCAN\_SetRxMbGlobalMask ( CAN\_Type \* *base*, uint32\_t *mask* )

This function sets the global mask for the FlexCAN message buffer in a matching process. The configuration is only effective when the Rx individual mask is disabled in the [FLEXCAN\\_Init\(\)](#).

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	Rx Message Buffer Global Mask value.

### 23.2.6.16 void FLEXCAN\_SetRxFifoGlobalMask ( CAN\_Type \* *base*, uint32\_t *mask* )

This function sets the global mask for FlexCAN FIFO in a matching process.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	Rx Fifo Global Mask value.

### 23.2.6.17 void FLEXCAN\_SetRxIndividualMask ( CAN\_Type \* *base*, uint8\_t *maskIdx*, uint32\_t *mask* )

This function sets the individual mask for the FlexCAN matching process. The configuration is only effective when the Rx individual mask is enabled in the [FLEXCAN\\_Init\(\)](#). If the Rx FIFO is disabled, the individual mask is applied to the corresponding Message Buffer. If the Rx FIFO is enabled, the individual mask for Rx FIFO occupied Message Buffer is applied to the Rx Filter with the same index. Note that only the first 32 individual masks can be used as the Rx FIFO filter mask.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>maskIdx</i>	The Index of individual Mask.
<i>mask</i>	Rx Individual Mask value.

### 23.2.6.18 void FLEXCAN\_SetTxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, bool *enable* )

This function aborts the previous transmission, cleans the Message Buffer, and configures it as a Transmit Message Buffer.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The Message Buffer index.
<i>enable</i>	Enable/disable Tx Message Buffer. <ul style="list-style-type: none"> <li>• true: Enable Tx Message Buffer.</li> <li>• false: Disable Tx Message Buffer.</li> </ul>

### 23.2.6.19 void FLEXCAN\_SetFDTxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, bool *enable* )

This function aborts the previous transmission, cleans the Message Buffer, and configures it as a Transmit Message Buffer.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The Message Buffer index.
<i>enable</i>	Enable/disable Tx Message Buffer. <ul style="list-style-type: none"> <li>• true: Enable Tx Message Buffer.</li> <li>• false: Disable Tx Message Buffer.</li> </ul>

### 23.2.6.20 void FLEXCAN\_SetRxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_rx\_mb\_config\_t \* *pRxMbConfig*, bool *enable* )

This function cleans a FlexCAN build-in Message Buffer and configures it as a Receive Message Buffer.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The Message Buffer index.
<i>pRxMbConfig</i>	Pointer to the FlexCAN Message Buffer configuration structure.
<i>enable</i>	Enable/disable Rx Message Buffer. <ul style="list-style-type: none"> <li>• true: Enable Rx Message Buffer.</li> <li>• false: Disable Rx Message Buffer.</li> </ul>

### 23.2.6.21 void FLEXCAN\_SetFDRxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_rx\_mb\_config\_t \* *pRxMbConfig*, bool *enable* )

This function cleans a FlexCAN build-in Message Buffer and configures it as a Receive Message Buffer.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The Message Buffer index.
<i>pRxMbConfig</i>	Pointer to the FlexCAN Message Buffer configuration structure.
<i>enable</i>	Enable/disable Rx Message Buffer. <ul style="list-style-type: none"> <li>• true: Enable Rx Message Buffer.</li> <li>• false: Disable Rx Message Buffer.</li> </ul>

### 23.2.6.22 void FLEXCAN\_SetRxFifoConfig ( CAN\_Type \* *base*, const flexcan\_rx\_fifo\_config\_t \* *pRxFifoConfig*, bool *enable* )

This function configures the FlexCAN Rx FIFO with given configuration.

Note

Legacy Rx FIFO only can receive classic CAN message.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>pRxFifoConfig</i>	Pointer to the FlexCAN Legacy Rx FIFO configuration structure. Can be NULL when enable parameter is false.
<i>enable</i>	Enable/disable Legacy Rx FIFO. <ul style="list-style-type: none"> <li>• true: Enable Legacy Rx FIFO.</li> <li>• false: Disable Legacy Rx FIFO.</li> </ul>

### 23.2.6.23 static uint32\_t FLEXCAN\_GetStatusFlags ( CAN\_Type \* *base* ) [inline], [static]

This function gets all FlexCAN status flags. The flags are returned as the logical OR value of the enumerators [\\_flexcan\\_flags](#). To check the specific status, compare the return value with enumerators in [\\_flexcan\\_flags](#).

Parameters

<i>base</i>	FlexCAN peripheral base address.
-------------	----------------------------------

Returns

FlexCAN status flags which are ORed by the enumerators in the [\\_flexcan\\_flags](#).

### 23.2.6.24 static void FLEXCAN\_ClearStatusFlags ( CAN\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function clears the FlexCAN status flags with a provided mask. An automatically cleared flag can't be cleared by this function.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	The status flags to be cleared, it is logical OR value of <a href="#">_flexcan_flags</a> .

### 23.2.6.25 static void FLEXCAN\_GetBusErrCount ( CAN\_Type \* *base*, uint8\_t \* *txErrBuf*, uint8\_t \* *rxErrBuf* ) [inline], [static]

This function gets the FlexCAN Bus Error Counter value for both Tx and Rx direction. These values may be needed in the upper layer error handling.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>txErrBuf</i>	Buffer to store Tx Error Counter value.
<i>rxErrBuf</i>	Buffer to store Rx Error Counter value.

### 23.2.6.26 static uint64\_t FLEXCAN\_GetMbStatusFlags ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function gets the interrupt flags of a given Message Buffers.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	The ORed FlexCAN Message Buffer mask.

Returns

The status of given Message Buffers.

### 23.2.6.27 static void FLEXCAN\_ClearMbStatusFlags ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function clears the interrupt flags of a given Message Buffers.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	The ORed FlexCAN Message Buffer mask.

### 23.2.6.28 static void FLEXCAN\_EnableInterrupts ( CAN\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the FlexCAN interrupts according to the provided mask. The mask is a logical OR of enumeration members, see [\\_flexcan\\_interrupt\\_enable](#).

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	The interrupts to enable. Logical OR of <a href="#">_flexcan_interrupt_enable</a> .

### 23.2.6.29 static void FLEXCAN\_DisableInterrupts ( CAN\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function disables the FlexCAN interrupts according to the provided mask. The mask is a logical OR of enumeration members, see [\\_flexcan\\_interrupt\\_enable](#).

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	The interrupts to disable. Logical OR of <a href="#">_flexcan_interrupt_enable</a> .

### 23.2.6.30 static void FLEXCAN\_EnableMbInterrupts ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function enables the interrupts of given Message Buffers.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	The ORed FlexCAN Message Buffer mask.

**23.2.6.31 static void FLEXCAN\_DisableMbInterrupts ( CAN\_Type \* *base*, uint64\_t *mask* )  
[inline], [static]**

This function disables the interrupts of given Message Buffers.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mask</i>	The ORed FlexCAN Message Buffer mask.

### 23.2.6.32 void FLEXCAN\_EnableRxFifoDMA ( CAN\_Type \* *base*, bool *enable* )

This function enables or disables the DMA feature of FlexCAN build-in Rx FIFO.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>enable</i>	true to enable, false to disable.

### 23.2.6.33 static uintptr\_t FLEXCAN\_GetRxFifoHeadAddr ( CAN\_Type \* *base* ) [inline], [static]

This function returns the FlexCAN Rx FIFO Head address, which is mainly used for the DMA/eDMA use case.

Parameters

<i>base</i>	FlexCAN peripheral base address.
-------------	----------------------------------

Returns

FlexCAN Rx FIFO Head address.

### 23.2.6.34 static void FLEXCAN\_Enable ( CAN\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the FlexCAN module.

Parameters

<i>base</i>	FlexCAN base pointer.
-------------	-----------------------

<i>enable</i>	true to enable, false to disable.
---------------	-----------------------------------

### 23.2.6.35 status\_t FLEXCAN\_WriteTxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_frame\_t \* *pTxFrame* )

This function writes a CAN Message to the specified Transmit Message Buffer and changes the Message Buffer state to start CAN Message transmit. After that the function returns immediately.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The FlexCAN Message Buffer index.
<i>pTxFrame</i>	Pointer to CAN message frame to be sent.

Return values

<i>kStatus_Success</i>	- Write Tx Message Buffer Successfully.
<i>kStatus_Fail</i>	- Tx Message Buffer is currently in use.

### 23.2.6.36 status\_t FLEXCAN\_ReadRxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *pRxFrame* )

This function reads a CAN message from a specified Receive Message Buffer. The function fills a receive CAN message frame structure with just received data and activates the Message Buffer again. The function returns immediately.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The FlexCAN Message Buffer index.
<i>pRxFrame</i>	Pointer to CAN message frame structure for reception.

Return values

<i>kStatus_Success</i>	- Rx Message Buffer is full and has been read successfully.
<i>kStatus_FLEXCAN_Rx-Overflow</i>	- Rx Message Buffer is already overflowed and has been read successfully.
<i>kStatus_Fail</i>	- Rx Message Buffer is empty.

### 23.2.6.37 status\_t FLEXCAN\_WriteFDTxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_fd\_frame\_t \* *pTxFrame* )

This function writes a CAN FD Message to the specified Transmit Message Buffer and changes the Message Buffer state to start CAN FD Message transmit. After that the function returns immediately.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The FlexCAN FD Message Buffer index.
<i>pTxFrame</i>	Pointer to CAN FD message frame to be sent.

Return values

<i>kStatus_Success</i>	- Write Tx Message Buffer Successfully.
<i>kStatus_Fail</i>	- Tx Message Buffer is currently in use.

### 23.2.6.38 status\_t FLEXCAN\_ReadFDRxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_fd\_frame\_t \* *pRxFrame* )

This function reads a CAN FD message from a specified Receive Message Buffer. The function fills a receive CAN FD message frame structure with just received data and activates the Message Buffer again. The function returns immediately.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>mbIdx</i>	The FlexCAN FD Message Buffer index.
<i>pRxFrame</i>	Pointer to CAN FD message frame structure for reception.

Return values

<i>kStatus_Success</i>	- Rx Message Buffer is full and has been read successfully.
<i>kStatus_FLEXCAN_Rx-Overflow</i>	- Rx Message Buffer is already overflowed and has been read successfully.
<i>kStatus_Fail</i>	- Rx Message Buffer is empty.

### 23.2.6.39 status\_t FLEXCAN\_ReadRxFifo ( CAN\_Type \* *base*, flexcan\_frame\_t \* *pRxFrame* )

This function reads a CAN message from the FlexCAN Legacy Rx FIFO.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>pRxFrame</i>	Pointer to CAN message frame structure for reception.

Return values

<i>kStatus_Success</i>	- Read Message from Rx FIFO successfully.
<i>kStatus_Fail</i>	- Rx FIFO is not enabled.

### 23.2.6.40 status\_t FLEXCAN\_TransferFDSendBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_fd\_frame\_t \* *pTxFrame* )

Note

A transfer handle does not need to be created before calling this API.

Parameters

<i>base</i>	FlexCAN peripheral base pointer.
<i>mbIdx</i>	The FlexCAN FD Message Buffer index.
<i>pTxFrame</i>	Pointer to CAN FD message frame to be sent.

Return values

<i>kStatus_Success</i>	- Write Tx Message Buffer Successfully.
<i>kStatus_Fail</i>	- Tx Message Buffer is currently in use.

### 23.2.6.41 status\_t FLEXCAN\_TransferFDReceiveBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_fd\_frame\_t \* *pRxFrame* )

Note

A transfer handle does not need to be created before calling this API.

Parameters

<i>base</i>	FlexCAN peripheral base pointer.
<i>mbIdx</i>	The FlexCAN FD Message Buffer index.
<i>pRxFrame</i>	Pointer to CAN FD message frame structure for reception.

Return values

<i>kStatus_Success</i>	- Rx Message Buffer is full and has been read successfully.
<i>kStatus_FLEXCAN_Rx-Overflow</i>	- Rx Message Buffer is already overflowed and has been read successfully.
<i>kStatus_Fail</i>	- Rx Message Buffer is empty.

### 23.2.6.42 status\_t FLEXCAN\_TransferFDSendNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *pMbXfer* )

This function sends a message using IRQ. This is a non-blocking function, which returns right away. When messages have been sent out, the send callback function is called.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>pMbXfer</i>	FlexCAN FD Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> .

Return values

<i>kStatus_Success</i>	Start Tx Message Buffer sending process successfully.
<i>kStatus_Fail</i>	Write Tx Message Buffer failed.
<i>kStatus_FLEXCAN_Tx-Busy</i>	Tx Message Buffer is in use.

### 23.2.6.43 status\_t FLEXCAN\_TransferFDReceiveNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *pMbXfer* )

This function receives a message using IRQ. This is non-blocking function, which returns right away. When the message has been received, the receive callback function is called.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>pMbXfer</i>	FlexCAN FD Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> .

Return values

<i>kStatus_Success</i>	- Start Rx Message Buffer receiving process successfully.
<i>kStatus_FLEXCAN_Rx-Busy</i>	- Rx Message Buffer is in use.

#### 23.2.6.44 void FLEXCAN\_TransferFDAbortSend ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )

This function aborts the interrupt driven message send process.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>mbIdx</i>	The FlexCAN FD Message Buffer index.

#### 23.2.6.45 void FLEXCAN\_TransferFDAbortReceive ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )

This function aborts the interrupt driven message receive process.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>mbIdx</i>	The FlexCAN FD Message Buffer index.

#### 23.2.6.46 status\_t FLEXCAN\_TransferSendBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *pTxFrame* )

## Note

A transfer handle does not need to be created before calling this API.

## Parameters

<i>base</i>	FlexCAN peripheral base pointer.
<i>mbIdx</i>	The FlexCAN Message Buffer index.
<i>pTxFrame</i>	Pointer to CAN message frame to be sent.

## Return values

<i>kStatus_Success</i>	- Write Tx Message Buffer Successfully.
<i>kStatus_Fail</i>	- Tx Message Buffer is currently in use.

### 23.2.6.47 status\_t FLEXCAN\_TransferReceiveBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *pRxFrame* )

## Note

A transfer handle does not need to be created before calling this API.

## Parameters

<i>base</i>	FlexCAN peripheral base pointer.
<i>mbIdx</i>	The FlexCAN Message Buffer index.
<i>pRxFrame</i>	Pointer to CAN message frame structure for reception.

## Return values

<i>kStatus_Success</i>	- Rx Message Buffer is full and has been read successfully.
<i>kStatus_FLEXCAN_Rx-Overflow</i>	- Rx Message Buffer is already overflowed and has been read successfully.
<i>kStatus_Fail</i>	- Rx Message Buffer is empty.

### 23.2.6.48 status\_t FLEXCAN\_TransferReceiveFifoBlocking ( CAN\_Type \* *base*, flexcan\_frame\_t \* *pRxFrame* )

## Note

A transfer handle does not need to be created before calling this API.

Parameters

<i>base</i>	FlexCAN peripheral base pointer.
<i>pRxFrame</i>	Pointer to CAN message frame structure for reception.

Return values

<i>kStatus_Success</i>	- Read Message from Rx FIFO successfully.
<i>kStatus_Fail</i>	- Rx FIFO is not enabled.

### 23.2.6.49 void FLEXCAN\_TransferCreateHandle ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the FlexCAN handle, which can be used for other FlexCAN transactional APIs. Usually, for a specified FlexCAN instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

### 23.2.6.50 status\_t FLEXCAN\_TransferSendNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *pMbXfer* )

This function sends a message using IRQ. This is a non-blocking function, which returns right away. When messages have been sent out, the send callback function is called.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>pMbXfer</i>	FlexCAN Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> .

Return values

<i>kStatus_Success</i>	Start Tx Message Buffer sending process successfully.
<i>kStatus_Fail</i>	Write Tx Message Buffer failed.
<i>kStatus_FLEXCAN_Tx-Busy</i>	Tx Message Buffer is in use.

### 23.2.6.51 status\_t FLEXCAN\_TransferReceiveNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *pMbXfer* )

This function receives a message using IRQ. This is non-blocking function, which returns right away. When the message has been received, the receive callback function is called.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>pMbXfer</i>	FlexCAN Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> .

Return values

<i>kStatus_Success</i>	- Start Rx Message Buffer receiving process successfully.
<i>kStatus_FLEXCAN_Rx-Busy</i>	- Rx Message Buffer is in use.

### 23.2.6.52 status\_t FLEXCAN\_TransferReceiveFifoNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_fifo\_transfer\_t \* *pFifoXfer* )

This function receives a message using IRQ. This is a non-blocking function, which returns right away. When all messages have been received, the receive callback function is called.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>pFifoXfer</i>	FlexCAN Rx FIFO transfer structure. See the <a href="#">flexcan_fifo_transfer_t</a> .

Return values

<i>kStatus_Success</i>	- Start Rx FIFO receiving process successfully.
<i>kStatus_FLEXCAN_Rx-FifoBusy</i>	- Rx FIFO is currently in use.

### 23.2.6.53 **status\_t FLEXCAN\_TransferGetReceiveFifoCount ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, size\_t \* *count* )**

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>count</i>	Number of CAN messages receive so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

### 23.2.6.54 **uint32\_t FLEXCAN\_GetTimeStamp ( flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )**

Then function can only be used when calling non-blocking Data transfer (TX/RX) API, After TX/R-X data transfer done (User can get the status by handler's callback function), we can get the detail index of Mailbox's timestamp by handle, Detail non-blocking data transfer API (TX/RX) contain. -FLEXCAN\_TransferSendNonBlocking -FLEXCAN\_TransferFDSendNonBlocking -FLEXCAN\_TransferReceiveNonBlocking -FLEXCAN\_TransferFDReceiveNonBlocking -FLEXCAN\_TransferReceiveFifoNonBlocking

Parameters

<i>handle</i>	FlexCAN handle pointer.
<i>mbIdx</i>	The FlexCAN Message Buffer index.

Return values

<i>the</i>	index of mailbox 's timestamp stored in the handle.
------------	---

### 23.2.6.55 void FLEXCAN\_TransferAbortSend ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )

This function aborts the interrupt driven message send process.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>mbIdx</i>	The FlexCAN Message Buffer index.

### 23.2.6.56 void FLEXCAN\_TransferAbortReceive ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )

This function aborts the interrupt driven message receive process.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>mbIdx</i>	The FlexCAN Message Buffer index.

### 23.2.6.57 void FLEXCAN\_TransferAbortReceiveFifo ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle* )

This function aborts the interrupt driven message receive from Rx FIFO process.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.

### 23.2.6.58 void FLEXCAN\_TransferHandleIRQ ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle* )

This function handles the FlexCAN Error, the Message Buffer, and the Rx FIFO IRQ request.

## Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.

## 23.3 FlexCAN eDMA Driver

### 23.3.1 Overview

#### Data Structures

- struct `flexcan_edma_handle_t`  
*FlexCAN eDMA handle. [More...](#)*

#### TypeDefs

- typedef void(\* `flexcan_edma_transfer_callback_t`)  
(CAN\_Type \*base, flexcan\_edma\_handle\_t  
\*handle, `status_t` status, void \*userData)  
*FlexCAN transfer callback function.*

#### Driver version

- #define `FSL_FLEXCAN_EDMA_DRIVER_VERSION` (MAKE\_VERSION(2, 11, 0))  
*FlexCAN EDMA driver version.*

#### eDMA transactional

- void `FLEXCAN_TransferCreateHandleEDMA` (CAN\_Type \*base, flexcan\_edma\_handle\_t  
\*handle, `flexcan_edma_transfer_callback_t` callback, void \*userData, `edma_handle_t` \*rxFifo-  
EdmaHandle)  
*Initializes the FlexCAN handle, which is used in transactional functions.*
- void `FLEXCAN_PrepareTransfConfiguration` (CAN\_Type \*base, `flexcan_fifo_transfer_t` \*pFifo-  
Xfer, `edma_transfer_config_t` \*pEdmaConfig)  
*Prepares the eDMA transfer configuration for FLEXCAN Legacy RX FIFO.*
- `status_t FLEXCAN_StartTransferDatafromRxFIFO` (CAN\_Type \*base, flexcan\_edma\_handle\_t  
\*handle, `edma_transfer_config_t` \*pEdmaConfig)  
*Start Transfer Data from the FLEXCAN Legacy Rx FIFO using eDMA.*
- `status_t FLEXCAN_TransferReceiveFifoEDMA` (CAN\_Type \*base, flexcan\_edma\_handle\_t  
\*handle, `flexcan_fifo_transfer_t` \*pFifoXfer)  
*Receives the CAN Message from the Legacy Rx FIFO using eDMA.*
- `status_t FLEXCAN_TransferGetReceiveFifoCountEMDA` (CAN\_Type \*base, flexcan\_edma\_handle\_t  
\*handle, size\_t \*count)  
*Gets the Legacy Rx Fifo transfer status during a interrupt non-blocking receive.*
- void `FLEXCAN_TransferAbortReceiveFifoEDMA` (CAN\_Type \*base, flexcan\_edma\_handle\_t  
\*handle)  
*Aborts the receive Legacy/Enhanced Rx FIFO process which used eDMA.*

### 23.3.2 Data Structure Documentation

#### 23.3.2.1 struct \_flexcan\_edma\_handle

##### Data Fields

- **flexcan\_edma\_transfer\_callback\_t callback**  
*Callback function.*
- **void \*userData**  
*FlexCAN callback function parameter.*
- **edma\_handle\_t \*rxFifoEdmaHandle**  
*The EDMA handler for Rx FIFO.*
- **volatile uint8\_t rxFifoState**  
*Rx FIFO transfer state.*
- **size\_t frameNum**  
*The number of messages that need to be received.*

##### Field Documentation

- (1) **flexcan\_edma\_transfer\_callback\_t flexcan\_edma\_handle\_t::callback**
- (2) **void\* flexcan\_edma\_handle\_t::userData**
- (3) **edma\_handle\_t\* flexcan\_edma\_handle\_t::rxFifoEdmaHandle**
- (4) **volatile uint8\_t flexcan\_edma\_handle\_t::rxFifoState**
- (5) **size\_t flexcan\_edma\_handle\_t::frameNum**

### 23.3.3 Macro Definition Documentation

#### 23.3.3.1 #define FSL\_FLEXCAN\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 11, 0))

### 23.3.4 Typedef Documentation

#### 23.3.4.1 **typedef void(\* flexcan\_edma\_transfer\_callback\_t)(CAN\_Type \*base, flexcan\_edma\_handle\_t \*handle, status\_t status, void \*userData)**

### 23.3.5 Function Documentation

#### 23.3.5.1 **void FLEXCAN\_TransferCreateHandleEDMA ( CAN\_Type \* base, flexcan\_edma\_handle\_t \* handle, flexcan\_edma\_transfer\_callback\_t callback, void \* userData, edma\_handle\_t \* rxFifoEdmaHandle )**

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	Pointer to flexcan_edma_handle_t structure.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.
<i>rxFifoEdmaHandle</i>	User-requested DMA handle for Rx FIFO DMA transfer.

### 23.3.5.2 void FLEXCAN\_PreparesTransfConfiguration ( CAN\_Type \* *base*, flexcan\_fifo\_transfer\_t \* *pFifoXfer*, edma\_transfer\_config\_t \* *pEdmaConfig* )

This function prepares the eDMA transfer configuration structure according to FLEXCAN Legacy RX FIFO.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>pFifoXfer</i>	FlexCAN Rx FIFO EDMA transfer structure, see <a href="#">flexcan_fifo_transfer_t</a> .
<i>pEdmaConfig</i>	The user configuration structure of type edma_transfer_t.

### 23.3.5.3 status\_t FLEXCAN\_StartTransferDatafromRxFIFO ( CAN\_Type \* *base*, flexcan\_edma\_handle\_t \* *handle*, edma\_transfer\_config\_t \* *pEdmaConfig* )

This function to Update edma transfer configuration and Start eDMA transfer

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	Pointer to flexcan_edma_handle_t structure.
<i>pEdmaConfig</i>	The user configuration structure of type edma_transfer_t.

Return values

<i>kStatus_Success</i>	if succeed, others failed.
------------------------	----------------------------

<i>kStatus_FLEXCAN_Rx-FifoBusy</i>	Previous transfer ongoing.
------------------------------------	----------------------------

### 23.3.5.4 status\_t FLEXCAN\_TransferReceiveFifoEDMA ( CAN\_Type \* *base*, flexcan\_edma\_handle\_t \* *handle*, flexcan\_fifo\_transfer\_t \* *pFifoXfer* )

This function receives the CAN Message using eDMA. This is a non-blocking function, which returns right away. After the CAN Message is received, the receive callback function is called.

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	Pointer to flexcan_edma_handle_t structure.
<i>pFifoXfer</i>	FlexCAN Rx FIFO EDMA transfer structure, see <a href="#">flexcan_fifo_transfer_t</a> .

Return values

<i>kStatus_Success</i>	if succeed, others failed.
<i>kStatus_FLEXCAN_Rx-FifoBusy</i>	Previous transfer ongoing.

### 23.3.5.5 status\_t FLEXCAN\_TransferGetReceiveFifoCountEMDA ( CAN\_Type \* *base*, flexcan\_edma\_handle\_t \* *handle*, size\_t \* *count* )

Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	FlexCAN handle pointer.
<i>count</i>	Number of CAN messages receive so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

### 23.3.5.6 void FLEXCAN\_TransferAbortReceiveFifoEDMA ( CAN\_Type \* *base*, flexcan\_edma\_handle\_t \* *handle* )

This function aborts the receive Legacy/Enhanced Rx FIFO process which used eDMA.

## Parameters

<i>base</i>	FlexCAN peripheral base address.
<i>handle</i>	Pointer to flexcan_edma_handle_t structure.

# Chapter 24

## FlexIO: FlexIO Driver

### 24.1 Overview

The MCUXpresso SDK provides a generic driver and multiple protocol-specific FlexIO drivers for the FlexIO module of MCUXpresso SDK devices.

### Modules

- [FlexIO Camera Driver](#)
- [FlexIO Driver](#)
- [FlexIO I2C Master Driver](#)
- [FlexIO I2S Driver](#)
- [FlexIO MCU Interface LCD Driver](#)
- [FlexIO SPI Driver](#)
- [FlexIO UART Driver](#)

## 24.2 FlexIO Driver

### 24.2.1 Overview

#### Data Structures

- struct `flexio_config_t`  
*Define FlexIO user configuration structure. [More...](#)*
- struct `flexio_timer_config_t`  
*Define FlexIO timer configuration structure. [More...](#)*
- struct `flexio_shifter_config_t`  
*Define FlexIO shifter configuration structure. [More...](#)*

#### Macros

- #define `FLEXIO_TIMER_TRIGGER_SEL_PININPUT`(x) ((uint32\_t)(x) << 1U)  
*Calculate FlexIO timer trigger.*

#### Typedefs

- typedef void(\* `flexio_isr_t` )(void \*base, void \*handle)  
*typedef for FlexIO simulated driver interrupt handler.*

#### Enumerations

- enum `flexio_timer_trigger_polarity_t` {
   
*kFLEXIO\_TimerTriggerPolarityActiveHigh = 0x0U,*
  
*kFLEXIO\_TimerTriggerPolarityActiveLow = 0x1U }*
  
*Define time of timer trigger polarity.*
- enum `flexio_timer_trigger_source_t` {
   
*kFLEXIO\_TimerTriggerSourceExternal = 0x0U,*
  
*kFLEXIO\_TimerTriggerSourceInternal = 0x1U }*
  
*Define type of timer trigger source.*
- enum `flexio_pin_config_t` {
   
*kFLEXIO\_PinConfigOutputDisabled = 0x0U,*
  
*kFLEXIO\_PinConfigOpenDrainOrBidirection = 0x1U,*
  
*kFLEXIO\_PinConfigBidirectionOutputData = 0x2U,*
  
*kFLEXIO\_PinConfigOutput = 0x3U }*
  
*Define type of timer/shifter pin configuration.*
- enum `flexio_pin_polarity_t` {
   
*kFLEXIO\_PinActiveHigh = 0x0U,*
  
*kFLEXIO\_PinActiveLow = 0x1U }*
  
*Definition of pin polarity.*

- enum `flexio_timer_mode_t` {
   
  `kFLEXIO_TimerModeDisabled` = 0x0U,
   
  `kFLEXIO_TimerModeDual8BitBaudBit` = 0x1U,
   
  `kFLEXIO_TimerModeDual8BitPWM` = 0x2U,
   
  `kFLEXIO_TimerModeSingle16Bit` = 0x3U }
   
    *Define type of timer work mode.*
- enum `flexio_timer_output_t` {
   
  `kFLEXIO_TimerOutputOneNotAffectedByReset` = 0x0U,
   
  `kFLEXIO_TimerOutputZeroNotAffectedByReset` = 0x1U,
   
  `kFLEXIO_TimerOutputOneAffectedByReset` = 0x2U,
   
  `kFLEXIO_TimerOutputZeroAffectedByReset` = 0x3U }
   
    *Define type of timer initial output or timer reset condition.*
- enum `flexio_timer_decrement_source_t` {
   
  `kFLEXIO_TimerDecSrcOnFlexIOClockShiftTimerOutput` = 0x0U,
   
  `kFLEXIO_TimerDecSrcOnTriggerInputShiftTimerOutput`,
   
  `kFLEXIO_TimerDecSrcOnPinInputShiftPinInput`,
   
  `kFLEXIO_TimerDecSrcOnTriggerInputShiftTriggerInput` }
   
    *Define type of timer decrement.*
- enum `flexio_timer_reset_condition_t` {
   
  `kFLEXIO_TimerResetNever` = 0x0U,
   
  `kFLEXIO_TimerResetOnTimerPinEqualToTimerOutput` = 0x2U,
   
  `kFLEXIO_TimerResetOnTimerTriggerEqualToTimerOutput` = 0x3U,
   
  `kFLEXIO_TimerResetOnTimerPinRisingEdge` = 0x4U,
   
  `kFLEXIO_TimerResetOnTimerTriggerRisingEdge` = 0x6U,
   
  `kFLEXIO_TimerResetOnTimerTriggerBothEdge` = 0x7U }
   
    *Define type of timer reset condition.*
- enum `flexio_timer_disable_condition_t` {
   
  `kFLEXIO_TimerDisableNever` = 0x0U,
   
  `kFLEXIO_TimerDisableOnPreTimerDisable` = 0x1U,
   
  `kFLEXIO_TimerDisableOnTimerCompare` = 0x2U,
   
  `kFLEXIO_TimerDisableOnTimerCompareTriggerLow` = 0x3U,
   
  `kFLEXIO_TimerDisableOnPinBothEdge` = 0x4U,
   
  `kFLEXIO_TimerDisableOnPinBothEdgeTriggerHigh` = 0x5U,
   
  `kFLEXIO_TimerDisableOnTriggerFallingEdge` = 0x6U }
   
    *Define type of timer disable condition.*
- enum `flexio_timer_enable_condition_t` {
   
  `kFLEXIO_TimerEnabledAlways` = 0x0U,
   
  `kFLEXIO_TimerEnableOnPrevTimerEnable` = 0x1U,
   
  `kFLEXIO_TimerEnableOnTriggerHigh` = 0x2U,
   
  `kFLEXIO_TimerEnableOnTriggerHighPinHigh` = 0x3U,
   
  `kFLEXIO_TimerEnableOnPinRisingEdge` = 0x4U,
   
  `kFLEXIO_TimerEnableOnPinRisingEdgeTriggerHigh` = 0x5U,
   
  `kFLEXIO_TimerEnableOnTriggerRisingEdge` = 0x6U,
   
  `kFLEXIO_TimerEnableOnTriggerBothEdge` = 0x7U }
   
    *Define type of timer enable condition.*
- enum `flexio_timer_stop_bit_condition_t` {

```
kFLEXIO_TimerStopBitDisabled = 0x0U,
kFLEXIO_TimerStopBitEnableOnTimerCompare = 0x1U,
kFLEXIO_TimerStopBitEnableOnTimerDisable = 0x2U,
kFLEXIO_TimerStopBitEnableOnTimerCompareDisable = 0x3U }
```

*Define type of timer stop bit generate condition.*

- enum `flexio_timer_start_bit_condition_t` {
 kFLEXIO\_TimerStartBitDisabled = 0x0U,
 kFLEXIO\_TimerStartBitEnabled = 0x1U }

*Define type of timer start bit generate condition.*

- enum `flexio_timer_output_state_t` {
 kFLEXIO\_PwmLow = 0,
 kFLEXIO\_PwmHigh }

*FlexIO as PWM channel output state.*

- enum `flexio_shifter_timer_polarity_t` {
 kFLEXIO\_ShifterTimerPolarityOnPositive = 0x0U,
 kFLEXIO\_ShifterTimerPolarityOnNegative = 0x1U }

*Define type of timer polarity for shifter control.*

- enum `flexio_shifter_mode_t` {
 kFLEXIO\_ShifterDisabled = 0x0U,
 kFLEXIO\_ShifterModeReceive = 0x1U,
 kFLEXIO\_ShifterModeTransmit = 0x2U,
 kFLEXIO\_ShifterModeMatchStore = 0x4U,
 kFLEXIO\_ShifterModeMatchContinuous = 0x5U,
 kFLEXIO\_ShifterModeState = 0x6U,
 kFLEXIO\_ShifterModeLogic = 0x7U }

*Define type of shifter working mode.*

- enum `flexio_shifter_input_source_t` {
 kFLEXIO\_ShifterInputFromPin = 0x0U,
 kFLEXIO\_ShifterInputFromNextShifterOutput = 0x1U }

*Define type of shifter input source.*

- enum `flexio_shifter_stop_bit_t` {
 kFLEXIO\_ShifterStopBitDisable = 0x0U,
 kFLEXIO\_ShifterStopBitLow = 0x2U,
 kFLEXIO\_ShifterStopBitHigh = 0x3U }

*Define of STOP bit configuration.*

- enum `flexio_shifter_start_bit_t` {
 kFLEXIO\_ShifterStartBitDisabledLoadDataOnEnable = 0x0U,
 kFLEXIO\_ShifterStartBitDisabledLoadDataOnShift = 0x1U,
 kFLEXIO\_ShifterStartBitLow = 0x2U,
 kFLEXIO\_ShifterStartBitHigh = 0x3U }

*Define type of START bit configuration.*

- enum `flexio_shifter_buffer_type_t` {

```

kFLEXIO_ShifterBuffer = 0x0U,
kFLEXIO_ShifterBufferBitSwapped = 0x1U,
kFLEXIO_ShifterBufferByteSwapped = 0x2U,
kFLEXIO_ShifterBufferBitByteSwapped = 0x3U,
kFLEXIO_ShifterBufferNibbleByteSwapped = 0x4U,
kFLEXIO_ShifterBufferHalfWordSwapped = 0x5U,
kFLEXIO_ShifterBufferNibbleSwapped = 0x6U }

```

*Define FlexIO shifter buffer type.*

## Variables

- FLEXIO\_Type \*const **s\_flexioBases** []
   
*Pointers to flexio bases for each instance.*
- const **clock\_ip\_name\_t s\_flexioClocks** []
   
*Pointers to flexio clocks for each instance.*

## Driver version

- #define **FSL\_FLEXIO\_DRIVER\_VERSION** (MAKE\_VERSION(2, 2, 0))
   
*FlexIO driver version.*

## FlexIO Initialization and De-initialization

- void **FLEXIO\_GetDefaultConfig** (**flexio\_config\_t** \*userConfig)
   
*Gets the default configuration to configure the FlexIO module.*
- void **FLEXIO\_Init** (FLEXIO\_Type \*base, const **flexio\_config\_t** \*userConfig)
   
*Configures the FlexIO with a FlexIO configuration.*
- void **FLEXIO\_Deinit** (FLEXIO\_Type \*base)
   
*Gates the FlexIO clock.*
- uint32\_t **FLEXIOGetInstance** (FLEXIO\_Type \*base)
   
*Get instance number for FLEXIO module.*

## FlexIO Basic Operation

- void **FLEXIO\_Reset** (FLEXIO\_Type \*base)
   
*Resets the FlexIO module.*
- static void **FLEXIO\_Enable** (FLEXIO\_Type \*base, bool enable)
   
*Enables the FlexIO module operation.*
- static uint32\_t **FLEXIO\_ReadPinInput** (FLEXIO\_Type \*base)
   
*Reads the input data on each of the FlexIO pins.*
- static uint8\_t **FLEXIO\_GetShifterState** (FLEXIO\_Type \*base)
   
*Gets the current state pointer for state mode use.*
- void **FLEXIO\_SetShifterConfig** (FLEXIO\_Type \*base, uint8\_t index, const **flexio\_shifter\_config\_t** \*shifterConfig)
   
*Configures the shifter with the shifter configuration.*

- void **FLEXIO\_SetTimerConfig** (FLEXIO\_Type \*base, uint8\_t index, const **flexio\_timer\_config\_t** \*timerConfig)  
*Configures the timer with the timer configuration.*
- static void **FLEXIO\_SetClockMode** (FLEXIO\_Type \*base, uint8\_t index, **flexio\_timer\_decrement-source\_t** clocksource)  
*This function set the value of the prescaler on flexio channels.*

## FlexIO Interrupt Operation

- static void **FLEXIO\_EnableShifterStatusInterrupts** (FLEXIO\_Type \*base, uint32\_t mask)  
*Enables the shifter status interrupt.*
- static void **FLEXIO\_DisableShifterStatusInterrupts** (FLEXIO\_Type \*base, uint32\_t mask)  
*Disables the shifter status interrupt.*
- static void **FLEXIO\_EnableShifterErrorInterrupts** (FLEXIO\_Type \*base, uint32\_t mask)  
*Enables the shifter error interrupt.*
- static void **FLEXIO\_DisableShifterErrorInterrupts** (FLEXIO\_Type \*base, uint32\_t mask)  
*Disables the shifter error interrupt.*
- static void **FLEXIO\_EnableTimerStatusInterrupts** (FLEXIO\_Type \*base, uint32\_t mask)  
*Enables the timer status interrupt.*
- static void **FLEXIO\_DisableTimerStatusInterrupts** (FLEXIO\_Type \*base, uint32\_t mask)  
*Disables the timer status interrupt.*

## FlexIO Status Operation

- static uint32\_t **FLEXIO\_GetShifterStatusFlags** (FLEXIO\_Type \*base)  
*Gets the shifter status flags.*
- static void **FLEXIO\_ClearShifterStatusFlags** (FLEXIO\_Type \*base, uint32\_t mask)  
*Clears the shifter status flags.*
- static uint32\_t **FLEXIO\_GetShifterErrorFlags** (FLEXIO\_Type \*base)  
*Gets the shifter error flags.*
- static void **FLEXIO\_ClearShifterErrorFlags** (FLEXIO\_Type \*base, uint32\_t mask)  
*Clears the shifter error flags.*
- static uint32\_t **FLEXIO\_GetTimerStatusFlags** (FLEXIO\_Type \*base)  
*Gets the timer status flags.*
- static void **FLEXIO\_ClearTimerStatusFlags** (FLEXIO\_Type \*base, uint32\_t mask)  
*Clears the timer status flags.*

## FlexIO DMA Operation

- static void **FLEXIO\_EnableShifterStatusDMA** (FLEXIO\_Type \*base, uint32\_t mask, bool enable)  
*Enables/disables the shifter status DMA.*
- uint32\_t **FLEXIO\_GetShifterBufferAddress** (FLEXIO\_Type \*base, **flexio\_shifter\_buffer\_type\_t** type, uint8\_t index)  
*Gets the shifter buffer address for the DMA transfer usage.*
- **status\_t FLEXIO\_RegisterHandleIRQ** (void \*base, void \*handle, **flexio\_isr\_t** isr)  
*Registers the handle and the interrupt handler for the FlexIO-simulated peripheral.*
- **status\_t FLEXIO\_UnregisterHandleIRQ** (void \*base)

*Unregisters the handle and the interrupt handler for the FlexIO-simulated peripheral.*

## 24.2.2 Data Structure Documentation

### 24.2.2.1 struct flexio\_config\_t

#### Data Fields

- bool `enableFlexio`  
*Enable/disable FlexIO module.*
- bool `enableInDoze`  
*Enable/disable FlexIO operation in doze mode.*
- bool `enableInDebug`  
*Enable/disable FlexIO operation in debug mode.*
- bool `enableFastAccess`  
*Enable/disable fast access to FlexIO registers, fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*

#### Field Documentation

##### (1) bool `flexio_config_t::enableFastAccess`

### 24.2.2.2 struct flexio\_timer\_config\_t

#### Data Fields

- `uint32_t triggerSelect`  
*The internal trigger selection number using MACROS.*
- `flexio_timer_trigger_polarity_t triggerPolarity`  
*Trigger Polarity.*
- `flexio_timer_trigger_source_t triggerSource`  
*Trigger Source, internal (see 'trgsel') or external.*
- `flexio_pin_config_t pinConfig`  
*Timer Pin Configuration.*
- `uint32_t pinSelect`  
*Timer Pin number Select.*
- `flexio_pin_polarity_t pinPolarity`  
*Timer Pin Polarity.*
- `flexio_timer_mode_t timerMode`  
*Timer work Mode.*
- `flexio_timer_output_t timerOutput`  
*Configures the initial state of the Timer Output and whether it is affected by the Timer reset.*
- `flexio_timer_decrement_source_t timerDecrement`  
*Configures the source of the Timer decrement and the source of the Shift clock.*
- `flexio_timer_reset_condition_t timerReset`  
*Configures the condition that causes the timer counter (and optionally the timer output) to be reset.*

- **flexio\_timer\_disable\_condition\_t timerDisable**  
Configures the condition that causes the Timer to be *disabled and stop decrementing*.
- **flexio\_timer\_enable\_condition\_t timerEnable**  
Configures the condition that causes the Timer to be *enabled and start decrementing*.
- **flexio\_timer\_stop\_bit\_condition\_t timerStop**  
*Timer STOP Bit generation.*
- **flexio\_timer\_start\_bit\_condition\_t timerStart**  
*Timer STRAT Bit generation.*
- **uint32\_t timerCompare**  
*Value for Timer Compare N Register.*

### Field Documentation

- (1) **uint32\_t flexio\_timer\_config\_t::triggerSelect**
- (2) **flexio\_timer\_trigger\_polarity\_t flexio\_timer\_config\_t::triggerPolarity**
- (3) **flexio\_timer\_trigger\_source\_t flexio\_timer\_config\_t::triggerSource**
- (4) **flexio\_pin\_config\_t flexio\_timer\_config\_t::pinConfig**
- (5) **uint32\_t flexio\_timer\_config\_t::pinSelect**
- (6) **flexio\_pin\_polarity\_t flexio\_timer\_config\_t::pinPolarity**
- (7) **flexio\_timer\_mode\_t flexio\_timer\_config\_t::timerMode**
- (8) **flexio\_timer\_output\_t flexio\_timer\_config\_t::timerOutput**
- (9) **flexio\_timer\_decrement\_source\_t flexio\_timer\_config\_t::timerDecrement**
- (10) **flexio\_timer\_reset\_condition\_t flexio\_timer\_config\_t::timerReset**
- (11) **flexio\_timer\_disable\_condition\_t flexio\_timer\_config\_t::timerDisable**
- (12) **flexio\_timer\_enable\_condition\_t flexio\_timer\_config\_t::timerEnable**
- (13) **flexio\_timer\_stop\_bit\_condition\_t flexio\_timer\_config\_t::timerStop**
- (14) **flexio\_timer\_start\_bit\_condition\_t flexio\_timer\_config\_t::timerStart**
- (15) **uint32\_t flexio\_timer\_config\_t::timerCompare**

### 24.2.2.3 struct flexio\_shifter\_config\_t

#### Data Fields

- **uint32\_t timerSelect**  
Selects which Timer is used for controlling the

- *logic/shift register and generating the Shift clock.*  
• **flexio\_shifter\_timer\_polarity\_t timerPolarity**  
    *Timer Polarity.*
- **flexio\_pin\_config\_t pinConfig**  
    *Shifter Pin Configuration.*
- **uint32\_t pinSelect**  
    *Shifter Pin number Select.*
- **flexio\_pin\_polarity\_t pinPolarity**  
    *Shifter Pin Polarity.*
- **flexio\_shifter\_mode\_t shifterMode**  
    *Configures the mode of the Shifter.*
- **uint32\_t parallelWidth**  
    *Configures the parallel width when using parallel mode.*
- **flexio\_shifter\_input\_source\_t inputSource**  
    *Selects the input source for the shifter.*
- **flexio\_shifter\_stop\_bit\_t shifterStop**  
    *Shifter STOP bit.*
- **flexio\_shifter\_start\_bit\_t shifterStart**  
    *Shifter START bit.*

## Field Documentation

- (1) `uint32_t flexio_shifter_config_t::timerSelect`
- (2) `flexio_shifter_timer_polarity_t flexio_shifter_config_t::timerPolarity`
- (3) `flexio_pin_config_t flexio_shifter_config_t::pinConfig`
- (4) `uint32_t flexio_shifter_config_t::pinSelect`
- (5) `flexio_pin_polarity_t flexio_shifter_config_t::pinPolarity`
- (6) `flexio_shifter_mode_t flexio_shifter_config_t::shifterMode`
- (7) `uint32_t flexio_shifter_config_t::parallelWidth`
- (8) `flexio_shifter_input_source_t flexio_shifter_config_t::inputSource`
- (9) `flexio_shifter_stop_bit_t flexio_shifter_config_t::shifterStop`
- (10) `flexio_shifter_start_bit_t flexio_shifter_config_t::shifterStart`

## 24.2.3 Macro Definition Documentation

24.2.3.1 `#define FSL_FLEXIO_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))`

24.2.3.2 `#define FLEXIO_TIMER_TRIGGER_SEL_PININPUT( x ) ((uint32_t)(x) << 1U)`

## 24.2.4 Typedef Documentation

24.2.4.1 `typedef void(* flexio_isr_t)(void *base, void *handle)`

## 24.2.5 Enumeration Type Documentation

### 24.2.5.1 enum flexio\_timer\_trigger\_polarity\_t

Enumerator

*kFLEXIO\_TimerTriggerPolarityActiveHigh* Active high.

*kFLEXIO\_TimerTriggerPolarityActiveLow* Active low.

### 24.2.5.2 enum flexio\_timer\_trigger\_source\_t

Enumerator

*kFLEXIO\_TimerTriggerSourceExternal* External trigger selected.

*kFLEXIO\_TimerTriggerSourceInternal* Internal trigger selected.

#### 24.2.5.3 enum flexio\_pin\_config\_t

Enumerator

*kFLEXIO\_PinConfigOutputDisabled* Pin output disabled.

*kFLEXIO\_PinConfigOpenDrainOrBidirection* Pin open drain or bidirectional output enable.

*kFLEXIO\_PinConfigBidirectionOutputData* Pin bidirectional output data.

*kFLEXIO\_PinConfigOutput* Pin output.

#### 24.2.5.4 enum flexio\_pin\_polarity\_t

Enumerator

*kFLEXIO\_PinActiveHigh* Active high.

*kFLEXIO\_PinActiveLow* Active low.

#### 24.2.5.5 enum flexio\_timer\_mode\_t

Enumerator

*kFLEXIO\_TimerModeDisabled* Timer Disabled.

*kFLEXIO\_TimerModeDual8BitBaudBit* Dual 8-bit counters baud/bit mode.

*kFLEXIO\_TimerModeDual8BitPWM* Dual 8-bit counters PWM mode.

*kFLEXIO\_TimerModeSingle16Bit* Single 16-bit counter mode.

#### 24.2.5.6 enum flexio\_timer\_output\_t

Enumerator

*kFLEXIO\_TimerOutputOneNotAffectedByReset* Logic one when enabled and is not affected by timer reset.

*kFLEXIO\_TimerOutputZeroNotAffectedByReset* Logic zero when enabled and is not affected by timer reset.

*kFLEXIO\_TimerOutputOneAffectedByReset* Logic one when enabled and on timer reset.

*kFLEXIO\_TimerOutputZeroAffectedByReset* Logic zero when enabled and on timer reset.

#### 24.2.5.7 enum flexio\_timer\_decrement\_source\_t

Enumerator

*kFLEXIO\_TimerDecSrcOnFlexIOClockShiftTimerOutput* Decrement counter on FlexIO clock, Shift clock equals Timer output.

***kFLEXIO\_TimerDecSrcOnTriggerInputShiftTimerOutput*** Decrement counter on Trigger input (both edges), Shift clock equals Timer output.

***kFLEXIO\_TimerDecSrcOnPinInputShiftPinInput*** Decrement counter on Pin input (both edges), Shift clock equals Pin input.

***kFLEXIO\_TimerDecSrcOnTriggerInputShiftTriggerInput*** Decrement counter on Trigger input (both edges), Shift clock equals Trigger input.

#### 24.2.5.8 enum flexio\_timer\_reset\_condition\_t

Enumerator

***kFLEXIO\_TimerResetNever*** Timer never reset.

***kFLEXIO\_TimerResetOnTimerPinEqualToTimerOutput*** Timer reset on Timer Pin equal to Timer Output.

***kFLEXIO\_TimerResetOnTimerTriggerEqualToTimerOutput*** Timer reset on Timer Trigger equal to Timer Output.

***kFLEXIO\_TimerResetOnTimerPinRisingEdge*** Timer reset on Timer Pin rising edge.

***kFLEXIO\_TimerResetOnTimerTriggerRisingEdge*** Timer reset on Trigger rising edge.

***kFLEXIO\_TimerResetOnTimerTriggerBothEdge*** Timer reset on Trigger rising or falling edge.

#### 24.2.5.9 enum flexio\_timer\_disable\_condition\_t

Enumerator

***kFLEXIO\_TimerDisableNever*** Timer never disabled.

***kFLEXIO\_TimerDisableOnPreTimerDisable*** Timer disabled on Timer N-1 disable.

***kFLEXIO\_TimerDisableOnTimerCompare*** Timer disabled on Timer compare.

***kFLEXIO\_TimerDisableOnTimerCompareTriggerLow*** Timer disabled on Timer compare and Trigger Low.

***kFLEXIO\_TimerDisableOnPinBothEdge*** Timer disabled on Pin rising or falling edge.

***kFLEXIO\_TimerDisableOnPinBothEdgeTriggerHigh*** Timer disabled on Pin rising or falling edge provided Trigger is high.

***kFLEXIO\_TimerDisableOnTriggerFallingEdge*** Timer disabled on Trigger falling edge.

#### 24.2.5.10 enum flexio\_timer\_enable\_condition\_t

Enumerator

***kFLEXIO\_TimerEnabledAlways*** Timer always enabled.

***kFLEXIO\_TimerEnableOnPrevTimerEnable*** Timer enabled on Timer N-1 enable.

***kFLEXIO\_TimerEnableOnTriggerHigh*** Timer enabled on Trigger high.

***kFLEXIO\_TimerEnableOnTriggerHighPinHigh*** Timer enabled on Trigger high and Pin high.

***kFLEXIO\_TimerEnableOnPinRisingEdge*** Timer enabled on Pin rising edge.

***kFLEXIO\_TimerEnableOnPinRisingEdgeTriggerHigh*** Timer enabled on Pin rising edge and Trigger high.

***kFLEXIO\_TimerEnableOnTriggerRisingEdge*** Timer enabled on Trigger rising edge.

***kFLEXIO\_TimerEnableOnTriggerBothEdge*** Timer enabled on Trigger rising or falling edge.

#### 24.2.5.11 enum flexio\_timer\_stop\_bit\_condition\_t

Enumerator

***kFLEXIO\_TimerStopBitDisabled*** Stop bit disabled.

***kFLEXIO\_TimerStopBitEnableOnTimerCompare*** Stop bit is enabled on timer compare.

***kFLEXIO\_TimerStopBitEnableOnTimerDisable*** Stop bit is enabled on timer disable.

***kFLEXIO\_TimerStopBitEnableOnTimerCompareDisable*** Stop bit is enabled on timer compare and timer disable.

#### 24.2.5.12 enum flexio\_timer\_start\_bit\_condition\_t

Enumerator

***kFLEXIO\_TimerStartBitDisabled*** Start bit disabled.

***kFLEXIO\_TimerStartBitEnabled*** Start bit enabled.

#### 24.2.5.13 enum flexio\_timer\_output\_state\_t

Enumerator

***kFLEXIO\_PwmLow*** The output state of PWM channel is low.

***kFLEXIO\_PwmHigh*** The output state of PWM channel is high.

#### 24.2.5.14 enum flexio\_shifter\_timer\_polarity\_t

Enumerator

***kFLEXIO\_ShifterTimerPolarityOnPositive*** Shift on positive edge of shift clock.

***kFLEXIO\_ShifterTimerPolarityOnNegative*** Shift on negative edge of shift clock.

#### 24.2.5.15 enum flexio\_shifter\_mode\_t

Enumerator

***kFLEXIO\_ShifterDisabled*** Shifter is disabled.

***kFLEXIO\_ShifterModeReceive*** Receive mode.  
***kFLEXIO\_ShifterModeTransmit*** Transmit mode.  
***kFLEXIO\_ShifterModeMatchStore*** Match store mode.  
***kFLEXIO\_ShifterModeMatchContinuous*** Match continuous mode.  
***kFLEXIO\_ShifterModeState*** SHIFTBUF contents are used for storing programmable state attributes.  
***kFLEXIO\_ShifterModeLogic*** SHIFTBUF contents are used for implementing programmable logic look up table.

#### 24.2.5.16 enum flexio\_shifter\_input\_source\_t

Enumerator

***kFLEXIO\_ShifterInputFromPin*** Shifter input from pin.  
***kFLEXIO\_ShifterInputFromNextShifterOutput*** Shifter input from Shifter N+1.

#### 24.2.5.17 enum flexio\_shifter\_stop\_bit\_t

Enumerator

***kFLEXIO\_ShifterStopBitDisable*** Disable shifter stop bit.  
***kFLEXIO\_ShifterStopBitLow*** Set shifter stop bit to logic low level.  
***kFLEXIO\_ShifterStopBitHigh*** Set shifter stop bit to logic high level.

#### 24.2.5.18 enum flexio\_shifter\_start\_bit\_t

Enumerator

***kFLEXIO\_ShifterStartBitDisabledLoadDataOnEnable*** Disable shifter start bit, transmitter loads data on enable.  
***kFLEXIO\_ShifterStartBitDisabledLoadDataOnShift*** Disable shifter start bit, transmitter loads data on first shift.  
***kFLEXIO\_ShifterStartBitLow*** Set shifter start bit to logic low level.  
***kFLEXIO\_ShifterStartBitHigh*** Set shifter start bit to logic high level.

#### 24.2.5.19 enum flexio\_shifter\_buffer\_type\_t

Enumerator

***kFLEXIO\_ShifterBuffer*** Shifter Buffer N Register.  
***kFLEXIO\_ShifterBufferBitSwapped*** Shifter Buffer N Bit Byte Swapped Register.  
***kFLEXIO\_ShifterBufferByteSwapped*** Shifter Buffer N Byte Swapped Register.

***kFLEXIO\_ShifterBufferBitByteSwapped*** Shifter Buffer N Bit Swapped Register.  
***kFLEXIO\_ShifterBufferNibbleByteSwapped*** Shifter Buffer N Nibble Byte Swapped Register.  
***kFLEXIO\_ShifterBufferHalfWordSwapped*** Shifter Buffer N Half Word Swapped Register.  
***kFLEXIO\_ShifterBufferNibbleSwapped*** Shifter Buffer N Nibble Swapped Register.

## 24.2.6 Function Documentation

### 24.2.6.1 void FLEXIO\_GetDefaultConfig ( *flexio\_config\_t \* userConfig* )

The configuration can used directly to call the FLEXIO\_Configure().

Example:

```
flexio_config_t config;
FLEXIO_GetDefaultConfig(&config);
```

Parameters

<i>userConfig</i>	pointer to <i>flexio_config_t</i> structure
-------------------	---

### 24.2.6.2 void FLEXIO\_Init ( *FLEXIO\_Type \* base, const flexio\_config\_t \* userConfig* )

The configuration structure can be filled by the user or be set with default values by [FLEXIO\\_GetDefaultConfig\(\)](#).

Example

```
flexio_config_t config = {
.enableFlexio = true,
.enableInDoze = false,
.enableInDebug = true,
.enableFastAccess = false
};
FLEXIO_Configure(base, &config);
```

Parameters

<i>base</i>	FlexIO peripheral base address
<i>userConfig</i>	pointer to <i>flexio_config_t</i> structure

### 24.2.6.3 void FLEXIO\_Deinit ( *FLEXIO\_Type \* base* )

Call this API to stop the FlexIO clock.

## Note

After calling this API, call the FLEXIO\_Init to use the FlexIO module.

## Parameters

<i>base</i>	FlexIO peripheral base address
-------------	--------------------------------

**24.2.6.4 uint32\_t FLEXIO\_GetInstance ( FLEXIO\_Type \* *base* )**

## Parameters

<i>base</i>	FLEXIO peripheral base address.
-------------	---------------------------------

**24.2.6.5 void FLEXIO\_Reset ( FLEXIO\_Type \* *base* )**

## Parameters

<i>base</i>	FlexIO peripheral base address
-------------	--------------------------------

**24.2.6.6 static void FLEXIO\_Enable ( FLEXIO\_Type \* *base*, bool *enable* ) [inline], [static]**

## Parameters

<i>base</i>	FlexIO peripheral base address
<i>enable</i>	true to enable, false to disable.

**24.2.6.7 static uint32\_t FLEXIO\_ReadPinInput ( FLEXIO\_Type \* *base* ) [inline], [static]**

## Parameters

<i>base</i>	FlexIO peripheral base address
-------------	--------------------------------

## Returns

FlexIO pin input data

24.2.6.8 **static uint8\_t FLEXIO\_GetShifterState ( FLEXIO\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	FlexIO peripheral base address
-------------	--------------------------------

Returns

current State pointer

#### 24.2.6.9 void FLEXIO\_SetShifterConfig ( FLEXIO\_Type \* *base*, uint8\_t *index*, const flexio\_shifter\_config\_t \* *shifterConfig* )

The configuration structure covers both the SHIFTCTL and SHIFTCFG registers. To configure the shifter to the proper mode, select which timer controls the shifter to shift, whether to generate start bit/stop bit, and the polarity of start bit and stop bit.

Example

```
flexio_shifter_config_t config = {
    .timerSelect = 0,
    .timerPolarity = kFLEXIO_ShifterTimerPolarityOnPositive,
    .pinConfig = kFLEXIO_PinConfigOpenDrainOrBidirection,
    .pinPolarity = kFLEXIO_PinActiveLow,
    .shifterMode = kFLEXIO_ShifterModeTransmit,
    .inputSource = kFLEXIO_ShifterInputFromPin,
    .shifterStop = kFLEXIO_ShifterStopBitHigh,
    .shifterStart = kFLEXIO_ShifterStartBitLow
};
FLEXIO_SetShifterConfig(base, &config);
```

Parameters

<i>base</i>	FlexIO peripheral base address
<i>index</i>	Shifter index
<i>shifterConfig</i>	Pointer to <a href="#">flexio_shifter_config_t</a> structure

#### 24.2.6.10 void FLEXIO\_SetTimerConfig ( FLEXIO\_Type \* *base*, uint8\_t *index*, const flexio\_timer\_config\_t \* *timerConfig* )

The configuration structure covers both the TIMCTL and TIMCFG registers. To configure the timer to the proper mode, select trigger source for timer and the timer pin output and the timing for timer.

Example

```
flexio_timer_config_t config = {
    .triggerSelect = FLEXIO_TIMER_TRIGGER_SEL_SHIFTnSTAT(0),
    .triggerPolarity = kFLEXIO_TimerTriggerPolarityActiveLow,
    .triggerSource = kFLEXIO_TimerTriggerSourceInternal,
```

```

.pinConfig = kFLEXIO_PinConfigOpenDrainOrBidirection,
.pinSelect = 0,
.pinPolarity = kFLEXIO_PinActiveHigh,
.timerMode = kFLEXIO_TimerModeDual8BitBaudBit,
.timerOutput = kFLEXIO_TimerOutputZeroNotAffectedByReset,
.timerDecrement = kFLEXIO_TimerDecSrcOnFlexIOClockShiftTimerOutput

,
.timerReset = kFLEXIO_TimerResetOnTimerPinEqualToTimerOutput,
.timerDisable = kFLEXIO_TimerDisableOnTimerCompare,
.timerEnable = kFLEXIO_TimerEnableOnTriggerHigh,
.timerStop = kFLEXIO_TimerStopBitEnableOnTimerDisable,
.timerStart = kFLEXIO_TimerStartBitEnabled
};

FLEXIO_SetTimerConfig(base, &config);

```

Parameters

<i>base</i>	FlexIO peripheral base address
<i>index</i>	Timer index
<i>timerConfig</i>	Pointer to the <code>flexio_timer_config_t</code> structure

#### 24.2.6.11 static void FLEXIO\_SetClockMode ( **FLEXIO\_Type** \* *base*, **uint8\_t** *index*, **flexio\_timer\_decrement\_source\_t** *clocksource* ) [inline], [static]

Parameters

<i>base</i>	Pointer to the FlexIO simulated peripheral type.
<i>clocksource</i>	Set clock value

#### 24.2.6.12 static void FLEXIO\_EnableShifterStatusInterrupts ( **FLEXIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

The interrupt generates when the corresponding SSF is set.

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The shifter status mask which can be calculated by $(1 \ll \text{shifter index})$

Note

For multiple shifter status interrupt enable, for example, two shifter status enable, can calculate the mask by using  $((1 \ll \text{shifter index}0) | (1 \ll \text{shifter index}1))$

#### 24.2.6.13 static void FLEXIO\_DisableShifterStatusInterrupts ( **FLEXIO\_Type** \* *base*,                   **uint32\_t** *mask* ) [inline], [static]

The interrupt won't generate when the corresponding SSF is set.

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The shifter status mask which can be calculated by ( $1 << \text{shifter index}$ )

Note

For multiple shifter status interrupt enable, for example, two shifter status enable, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 24.2.6.14 static void FLEXIO\_EnableShifterErrorInterrupts ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

The interrupt generates when the corresponding SEF is set.

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The shifter error mask which can be calculated by ( $1 << \text{shifter index}$ )

Note

For multiple shifter error interrupt enable, for example, two shifter error enable, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 24.2.6.15 static void FLEXIO\_DisableShifterErrorInterrupts ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

The interrupt won't generate when the corresponding SEF is set.

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The shifter error mask which can be calculated by ( $1 << \text{shifter index}$ )

Note

For multiple shifter error interrupt enable, for example, two shifter error enable, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 24.2.6.16 static void FLEXIO\_EnableTimerStatusInterrupts ( FLEXIO\_Type \* *base*,                   uint32\_t *mask* ) [inline], [static]

The interrupt generates when the corresponding SSF is set.

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The timer status mask which can be calculated by ( $1 << \text{timer index}$ )

Note

For multiple timer status interrupt enable, for example, two timer status enable, can calculate the mask by using  $((1 << \text{timer index}0) | (1 << \text{timer index}1))$

#### 24.2.6.17 static void FLEXIO\_DisableTimerStatusInterrupts ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

The interrupt won't generate when the corresponding SSF is set.

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The timer status mask which can be calculated by ( $1 << \text{timer index}$ )

Note

For multiple timer status interrupt enable, for example, two timer status enable, can calculate the mask by using  $((1 << \text{timer index}0) | (1 << \text{timer index}1))$

#### 24.2.6.18 static uint32\_t FLEXIO\_GetShifterStatusFlags ( FLEXIO\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	FlexIO peripheral base address
-------------	--------------------------------

Returns

Shifter status flags

#### 24.2.6.19 static void FLEXIO\_ClearShifterStatusFlags ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The shifter status mask which can be calculated by ( $1 << \text{shifter index}$ )

Note

For clearing multiple shifter status flags, for example, two shifter status flags, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 24.2.6.20 static uint32\_t FLEXIO\_GetShifterErrorFlags ( FLEXIO\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	FlexIO peripheral base address
-------------	--------------------------------

Returns

Shifter error flags

#### 24.2.6.21 static void FLEXIO\_ClearShifterErrorFlags ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The shifter error mask which can be calculated by ( $1 << \text{shifter index}$ )

Note

For clearing multiple shifter error flags, for example, two shifter error flags, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 24.2.6.22 static uint32\_t FLEXIO\_GetTimerStatusFlags ( FLEXIO\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	FlexIO peripheral base address
-------------	--------------------------------

Returns

Timer status flags

#### 24.2.6.23 static void FLEXIO\_ClearTimerStatusFlags ( **FLEXIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The timer status mask which can be calculated by $(1 << \text{timer index})$

Note

For clearing multiple timer status flags, for example, two timer status flags, can calculate the mask by using  $((1 << \text{timer index}0) | (1 << \text{timer index}1))$

#### 24.2.6.24 static void FLEXIO\_EnableShifterStatusDMA ( **FLEXIO\_Type** \* *base*, **uint32\_t** *mask*, **bool enable** ) [inline], [static]

The DMA request generates when the corresponding SSF is set.

Note

For multiple shifter status DMA enables, for example, calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

Parameters

<i>base</i>	FlexIO peripheral base address
<i>mask</i>	The shifter status mask which can be calculated by $(1 << \text{shifter index})$

<i>enable</i>	True to enable, false to disable.
---------------	-----------------------------------

#### 24.2.6.25 **uint32\_t FLEXIO\_GetShifterBufferAddress ( FLEXIO\_Type \* *base*, flexio\_shifter\_buffer\_type\_t *type*, uint8\_t *index* )**

Parameters

<i>base</i>	FlexIO peripheral base address
<i>type</i>	Shifter type of flexio_shifter_buffer_type_t
<i>index</i>	Shifter index

Returns

Corresponding shifter buffer index

#### 24.2.6.26 **status\_t FLEXIO\_RegisterHandleIRQ ( void \* *base*, void \* *handle*, flexio\_isr\_t *isr* )**

Parameters

<i>base</i>	Pointer to the FlexIO simulated peripheral type.
<i>handle</i>	Pointer to the handler for FlexIO simulated peripheral.
<i>isr</i>	FlexIO simulated peripheral interrupt handler.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

#### 24.2.6.27 **status\_t FLEXIO\_UnregisterHandleIRQ ( void \* *base* )**

Parameters

<i>base</i>	Pointer to the FlexIO simulated peripheral type.
-------------	--

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

## 24.2.7 Variable Documentation

24.2.7.1 **FLEXIO\_Type\* const s\_flexioBases[]**

24.2.7.2 **const clock\_ip\_name\_t s\_flexioClocks[]**

## 24.3 FlexIO Camera Driver

### 24.3.1 Overview

The MCUXpresso SDK provides a driver for the camera function using Flexible I/O.

FlexIO Camera driver includes functional APIs and eDMA transactional APIs. Functional APIs target low level APIs. Users can use functional APIs for FlexIO Camera initialization/configuration/operation purpose. Using the functional API requires knowledge of the FlexIO Camera peripheral and how to organize functional APIs to meet the requirements of the application. All functional API use the `FLEXIO_CAMERA_Type` \* as the first parameter. FlexIO Camera functional operation groups provide the functional APIs set.

eDMA transactional APIs target high-level APIs. Users can use the transactional API to enable the peripheral quickly and can also use in the application if the code size and performance of transactional APIs satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the `flexio_camera_edma_handle_t` as the second parameter. Users need to initialize the handle by calling the `FLEXIO_CAMERA_TransferCreateHandleEDMA()` API.

eDMA transactional APIs support asynchronous receive. This means that the functions `FLEXIO_CAMERA_TransferReceiveEDMA()` set up an interrupt for data receive. When the receive is complete, the upper layer is notified through a callback function with the status `kStatus_FLEXIO_CAMERA_RxIdle`.

### 24.3.2 Typical use case

#### 24.3.2.1 FlexIO Camera Receive using eDMA method

```

volatile uint32_t isEDMAGetOnePictureFinish = false;
edma_handle_t g_edmaHandle;
flexio_camera_edma_handle_t g_cameraEdmaHandle;
edma_config_t edmaConfig;
FLEXIO_CAMERA_Type g_FlexioCameraDevice = {.flexioBase = FLEXIO0,
                                             .datPinStartIdx = 24U, /* fxio_pin 24 -31 are used. */
                                             .pclkPinIdx = 1U,    /* fxio_pin 1 is used as pclk pin. */
                                             .hrefPinIdx = 18U,   /* flexio_pin 18 is used as href pin. */
                                             .shifterStartIdx = 0U, /* Shifter 0 = 7 are used. */
                                             .shifterCount = 8U,
                                             .timerIdx = 0U};

flexio_camera_config_t cameraConfig;

/* Configure DMAMUX */
DMAMUX_Init(DMAMUX0);
/* Configure DMA */
EDMA_GetDefaultConfig(&edmaConfig);
EDMA_Init(DMA0, &edmaConfig);

DMAMUX_SetSource(DMAMUX0, DMA_CHN_FLEXIO_TO_FRAMEBUFF, (g_FlexioCameraDevice.
                                                       shifterStartIdx + 1U));
DMAMUX_EnableChannel(DMAMUX0, DMA_CHN_FLEXIO_TO_FRAMEBUFF);
EDMA_CreateHandle(&g_edmaHandle, DMA0, DMA_CHN_FLEXIO_TO_FRAMEBUFF);

FLEXIO_CAMERA_GetDefaultConfig(&cameraConfig);
FLEXIO_CAMERA_Init(&g_FlexioCameraDevice, &cameraConfig);
/* Clear all the flag. */

```

```

FLEXIO_CAMERA_ClearStatusFlags(&g_FlexioCameraDevice,
                               kFLEXIO_CAMERA_RxDataRegFullFlag |
                               kFLEXIO_CAMERA_RxErrorFlag);
FLEXIO_ClearTimerStatusFlags(FLEXIO0, 0xFF);
FLEXIO_CAMERA_TransferCreateHandleEDMA(&g_FlexioCameraDevice, &
                                       g_cameraEdmaHandle, FLEXIO_CAMERA_UserCallback, NULL,
                                       &g_edmaHandle);
cameraTransfer.dataAddress = (uint32_t)u16CameraFrameBuffer;
cameraTransfer.dataNum = sizeof(u16CameraFrameBuffer);
FLEXIO_CAMERA_TransferReceiveEDMA(&g_FlexioCameraDevice, &
                                   g_cameraEdmaHandle, &cameraTransfer);
while (!(isEDMAGetOnePictureFinish))
{
    ;
}
/* A callback function is also needed */
void FLEXIO_CAMERA_UserCallback(FLEXIO_CAMERA_Type *base,
                                 flexio_camera_edma_handle_t *handle,
                                 status_t status,
                                 void *userData)
{
    userData = userData;
    /* eDMA Transfer finished */
    if (kStatus_FLEXIO_CAMERA_RxIdle == status)
    {
        isEDMAGetOnePictureFinish = true;
    }
}

```

## Modules

- FlexIO eDMA Camera Driver

## Data Structures

- struct **FLEXIO\_CAMERA\_Type**  
*Define structure of configuring the FlexIO Camera device.* [More...](#)
- struct **flexio\_camera\_config\_t**  
*Define FlexIO Camera user configuration structure.* [More...](#)
- struct **flexio\_camera\_transfer\_t**  
*Define FlexIO Camera transfer structure.* [More...](#)

## Macros

- #define **FLEXIO\_CAMERA\_PARALLEL\_DATA\_WIDTH** (8U)  
*Define the Camera CPI interface is constantly 8-bit width.*

## Enumerations

- enum {
 kStatus\_FLEXIO\_CAMERA\_RxBusy = MAKE\_STATUS(kStatusGroup\_FLEXIO\_CAMERA,

```

0),
kStatus_FLEXIO_CAMERA_RxIdle = MAKE_STATUS(kStatusGroup_FLEXIO_CAMERA, 1)
}

Error codes for the Camera driver.
• enum _flexio_camera_status_flags {
    kFLEXIO_CAMERA_RxDataRegFullFlag = 0x1U,
    kFLEXIO_CAMERA_RxErrorFlag = 0x2U }

```

*Define FlexIO Camera status mask.*

## Driver version

- #define FSL\_FLEXIO\_CAMERA\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 3))
 *FlexIO Camera driver version 2.1.3.*

## Initialization and configuration

- void FLEXIO\_CAMERA\_Init (FLEXIO\_CAMERA\_Type \*base, const flexio\_camera\_config\_t \*config)
 *Ungates the FlexIO clock, resets the FlexIO module, and configures the FlexIO Camera.*
- void FLEXIO\_CAMERA\_Deinit (FLEXIO\_CAMERA\_Type \*base)
 *Resets the FLEXIO\_CAMERA shifer and timer config.*
- void FLEXIO\_CAMERA\_GetDefaultConfig (flexio\_camera\_config\_t \*config)
 *Gets the default configuration to configure the FlexIO Camera.*
- static void FLEXIO\_CAMERA\_Enable (FLEXIO\_CAMERA\_Type \*base, bool enable)
 *Enables/disables the FlexIO Camera module operation.*

## Status

- uint32\_t FLEXIO\_CAMERA\_GetStatusFlags (FLEXIO\_CAMERA\_Type \*base)
 *Gets the FlexIO Camera status flags.*
- void FLEXIO\_CAMERA\_ClearStatusFlags (FLEXIO\_CAMERA\_Type \*base, uint32\_t mask)
 *Clears the receive buffer full flag manually.*

## Interrupts

- void FLEXIO\_CAMERA\_EnableInterrupt (FLEXIO\_CAMERA\_Type \*base)
 *Switches on the interrupt for receive buffer full event.*
- void FLEXIO\_CAMERA\_DisableInterrupt (FLEXIO\_CAMERA\_Type \*base)
 *Switches off the interrupt for receive buffer full event.*

## DMA support

- static void FLEXIO\_CAMERA\_EnableRxDMA (FLEXIO\_CAMERA\_Type \*base, bool enable)

*Enables/disables the FlexIO Camera receive DMA.*

- static uint32\_t **FLEXIO\_CAMERA\_GetRxBufferAddress** (**FLEXIO\_CAMERA\_Type** \*base)  
*Gets the data from the receive buffer.*

### 24.3.3 Data Structure Documentation

#### 24.3.3.1 struct **FLEXIO\_CAMERA\_Type**

##### Data Fields

- **FLEXIO\_Type \* flexioBase**  
*FlexIO module base address.*
- **uint32\_t datPinStartIdx**  
*First data pin (D0) index for flexio\_camera.*
- **uint32\_t pclkPinIdx**  
*Pixel clock pin (PCLK) index for flexio\_camera.*
- **uint32\_t hrefPinIdx**  
*Horizontal sync pin (HREF) index for flexio\_camera.*
- **uint32\_t shifterStartIdx**  
*First shifter index used for flexio\_camera data FIFO.*
- **uint32\_t shifterCount**  
*The count of shifters that are used as flexio\_camera data FIFO.*
- **uint32\_t timerIdx**  
*Timer index used for flexio\_camera in FlexIO.*

##### Field Documentation

(1) **FLEXIO\_Type\* FLEXIO\_CAMERA\_Type::flexioBase**

(2) **uint32\_t FLEXIO\_CAMERA\_Type::datPinStartIdx**

Then the successive following FLEXIO\_CAMERA\_DATA\_WIDTH-1 pins are used as D1-D7.

- (3) **uint32\_t FLEXIO\_CAMERA\_Type::pclkPinIdx**
- (4) **uint32\_t FLEXIO\_CAMERA\_Type::hrefPinIdx**
- (5) **uint32\_t FLEXIO\_CAMERA\_Type::shifterStartIdx**
- (6) **uint32\_t FLEXIO\_CAMERA\_Type::shifterCount**
- (7) **uint32\_t FLEXIO\_CAMERA\_Type::timerIdx**

#### 24.3.3.2 struct **flexio\_camera\_config\_t**

##### Data Fields

- **bool enablecamera**  
*Enable/disable FlexIO Camera TX & RX.*

- bool `enableInDoze`  
*Enable/disable FlexIO operation in doze mode.*
- bool `enableInDebug`  
*Enable/disable FlexIO operation in debug mode.*
- bool `enableFastAccess`  
*Enable/disable fast access to FlexIO registers,  
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*

### Field Documentation

- (1) `bool flexio_camera_config_t::enablecamera`
- (2) `bool flexio_camera_config_t::enableFastAccess`

### 24.3.3.3 struct `flexio_camera_transfer_t`

#### Data Fields

- `uint32_t dataAddress`  
*Transfer buffer.*
- `uint32_t dataNum`  
*Transfer num.*

### 24.3.4 Macro Definition Documentation

#### 24.3.4.1 #define `FSL_FLEXIO_CAMERA_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 3)`)

#### 24.3.4.2 #define `FLEXIO_CAMERA_PARALLEL_DATA_WIDTH` (`8U`)

### 24.3.5 Enumeration Type Documentation

#### 24.3.5.1 anonymous enum

Enumerator

- `kStatus_FLEXIO_CAMERA_RxBusy` Receiver is busy.  
`kStatus_FLEXIO_CAMERA_RxIdle` Camera receiver is idle.

#### 24.3.5.2 enum `_flexio_camera_status_flags`

Enumerator

- `kFLEXIO_CAMERA_RxDataRegFullFlag` Receive buffer full flag.  
`kFLEXIO_CAMERA_RxErrorFlag` Receive buffer error flag.

## 24.3.6 Function Documentation

24.3.6.1 `void FLEXIO_CAMERA_Init( FLEXIO_CAMERA_Type * base, const flexio_camera_config_t * config )`

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_CAMERA_Type</a> structure
<i>config</i>	Pointer to <a href="#">flexio_camera_config_t</a> structure

#### 24.3.6.2 void FLEXIO\_CAMERA\_Deinit ( [FLEXIO\\_CAMERA\\_Type](#) \* *base* )

Note

After calling this API, call [FLEXIO\\_CAMERA\\_Init](#) to use the FlexIO Camera module.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_CAMERA_Type</a> structure
-------------	---

#### 24.3.6.3 void FLEXIO\_CAMERA\_GetDefaultConfig ( [flexio\\_camera\\_config\\_t](#) \* *config* )

The configuration can be used directly for calling the [FLEXIO\\_CAMERA\\_Init\(\)](#). Example:

```
flexio_camera_config_t config;
FLEXIO\_CAMERA\_GetDefaultConfig(&userConfig);
```

Parameters

<i>config</i>	Pointer to the <a href="#">flexio_camera_config_t</a> structure
---------------	---

#### 24.3.6.4 static void FLEXIO\_CAMERA\_Enable ( [FLEXIO\\_CAMERA\\_Type](#) \* *base*, [bool](#) *enable* ) [inline], [static]

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_CAMERA_Type</a>
<i>enable</i>	True to enable, false does not have any effect.

#### 24.3.6.5 [uint32\\_t](#) FLEXIO\_CAMERA\_GetStatusFlags ( [FLEXIO\\_CAMERA\\_Type](#) \* *base* )

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_CAMERA_Type</a> structure
-------------	---

Returns

FlexIO shifter status flags

- FLEXIO\_SHIFTSTAT\_SSF\_MASK
- 0

#### 24.3.6.6 void [FLEXIO\\_CAMERA\\_ClearStatusFlags](#) ( [FLEXIO\\_CAMERA\\_Type](#) \* *base*, [uint32\\_t](#) *mask* )

Parameters

<i>base</i>	Pointer to the device.
<i>mask</i>	status flag The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• kFLEXIO_CAMERA_RxDataRegFullFlag</li> <li>• kFLEXIO_CAMERA_RxErrorFlag</li> </ul>

#### 24.3.6.7 void [FLEXIO\\_CAMERA\\_EnableInterrupt](#) ( [FLEXIO\\_CAMERA\\_Type](#) \* *base* )

Parameters

<i>base</i>	Pointer to the device.
-------------	------------------------

#### 24.3.6.8 void [FLEXIO\\_CAMERA\\_DisableInterrupt](#) ( [FLEXIO\\_CAMERA\\_Type](#) \* *base* )

Parameters

<i>base</i>	Pointer to the device.
-------------	------------------------

#### 24.3.6.9 static void [FLEXIO\\_CAMERA\\_EnableRxDMA](#) ( [FLEXIO\\_CAMERA\\_Type](#) \* *base*, [bool](#) *enable* ) [inline], [static]

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_CAMERA_Type</a> structure
<i>enable</i>	True to enable, false to disable.

The FlexIO Camera mode can't work without the DMA or eDMA support. Usually, it needs at least two DMA or eDMA channels, one for transferring data from Camera, such as 0V7670 to FlexIO buffer, another is for transferring data from FlexIO buffer to LCD.

#### 24.3.6.10 static uint32\_t FLEXIO\_CAMERA\_GetRxBufferAddress ( FLEXIO\_CAMERA\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	Pointer to the device.
-------------	------------------------

Returns

data Pointer to the buffer that keeps the data with count of *base*->shifterCount .

## 24.3.7 FlexIO eDMA Camera Driver

### 24.3.7.1 Overview

#### Data Structures

- struct `flexio_camera_edma_handle_t`  
*Camera eDMA handle. [More...](#)*

#### TypeDefs

- typedef void(\* `flexio_camera_edma_transfer_callback_t`)(`FLEXIO_CAMERA_Type` \*base, `flexio_camera_edma_handle_t` \*handle, `status_t` status, void \*userData)  
*Camera transfer callback function.*

#### Driver version

- #define `FSL_FLEXIO_CAMERA_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 3)`)  
*FlexIO Camera EDMA driver version 2.1.3.*

#### eDMA transactional

- `status_t FLEXIO_CAMERA_TransferCreateHandleEDMA` (`FLEXIO_CAMERA_Type` \*base, `flexio_camera_edma_handle_t` \*handle, `flexio_camera_edma_transfer_callback_t` callback, void \*userData, `edma_handle_t` \*rxEdmaHandle)  
*Initializes the Camera handle, which is used in transactional functions.*
- `status_t FLEXIO_CAMERA_TransferReceiveEDMA` (`FLEXIO_CAMERA_Type` \*base, `flexio_camera_edma_handle_t` \*handle, `flexio_camera_transfer_t` \*xfer)  
*Receives data using eDMA.*
- `void FLEXIO_CAMERA_TransferAbortReceiveEDMA` (`FLEXIO_CAMERA_Type` \*base, `flexio_camera_edma_handle_t` \*handle)  
*Aborts the receive data which used the eDMA.*
- `status_t FLEXIO_CAMERA_TransferGetReceiveCountEDMA` (`FLEXIO_CAMERA_Type` \*base, `flexio_camera_edma_handle_t` \*handle, `size_t` \*count)  
*Gets the remaining bytes to be received.*

### 24.3.7.2 Data Structure Documentation

#### 24.3.7.2.1 struct \_flexio\_camera\_edma\_handle

Forward declaration of the handle typedef.

#### Data Fields

- `flexio_camera_edma_transfer_callback_t` callback

- *Callback function.*
- `void *userData`  
*Camera callback function parameter.*
- `size_t rxSize`  
*Total bytes to be received.*
- `edma_handle_t *rxEdmaHandle`  
*The eDMA RX channel used.*
- `uint8_t nbytes`  
*eDMA minor byte transfer count initially configured.*
- `volatile uint8_t rxState`  
*RX transfer state.*

## Field Documentation

- (1) `flexio_camera_edma_transfer_callback_t flexio_camera_edma_handle_t::callback`
- (2) `void* flexio_camera_edma_handle_t::userData`
- (3) `size_t flexio_camera_edma_handle_t::rxSize`
- (4) `edma_handle_t* flexio_camera_edma_handle_t::rxEdmaHandle`
- (5) `uint8_t flexio_camera_edma_handle_t::nbytes`

### 24.3.7.3 Macro Definition Documentation

24.3.7.3.1 `#define FSL_FLEXIO_CAMERA_EDMA_DRIVER_VERSION(MAKE_VERSION(2, 1, 3))`

### 24.3.7.4 Typedef Documentation

24.3.7.4.1 `typedef void(* flexio_camera_edma_transfer_callback_t)(FLEXIO_CAMERA_Type  
*base, flexio_camera_edma_handle_t *handle, status_t status, void *userData)`

### 24.3.7.5 Function Documentation

24.3.7.5.1 `status_t FLEXIO_CAMERA_TransferCreateHandleEDMA ( FLEXIO_CAMERA_Type  
* base, flexio_camera_edma_handle_t * handle, flexio_camera_edma_transfer-  
_callback_t callback, void * userData, edma_handle_t * rxEdmaHandle  
)`

#### Parameters

<code>base</code>	Pointer to the <a href="#">FLEXIO_CAMERA_Type</a> .
-------------------	---

<i>handle</i>	Pointer to flexio_camera_edma_handle_t structure.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.
<i>rxEdmaHandle</i>	User requested DMA handle for RX DMA transfer.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO Camera eDMA type/handle table out of range.

#### 24.3.7.5.2 status\_t FLEXIO\_CAMERA\_TransferReceiveEDMA ( FLEXIO\_CAMERA\_Type \* *base*, flexio\_camera\_edma\_handle\_t \* *handle*, flexio\_camera\_transfer\_t \* *xfer* )

This function receives data using eDMA. This is a non-blocking function, which returns right away. When all data is received, the receive callback function is called.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_CAMERA_Type</a> .
<i>handle</i>	Pointer to the flexio_camera_edma_handle_t structure.
<i>xfer</i>	Camera eDMA transfer structure, see <a href="#">flexio_camera_transfer_t</a> .

Return values

<i>kStatus_Success</i>	if succeeded, others failed.
<i>kStatus_CAMERA_Rx-Busy</i>	Previous transfer on going.

#### 24.3.7.5.3 void FLEXIO\_CAMERA\_TransferAbortReceiveEDMA ( FLEXIO\_CAMERA\_Type \* *base*, flexio\_camera\_edma\_handle\_t \* *handle* )

This function aborts the receive data which used the eDMA.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_CAMERA_Type</a> .
-------------	---

<i>handle</i>	Pointer to the flexio_camera_edma_handle_t structure.
---------------	---

**24.3.7.5.4 status\_t FLEXIO\_CAMERA\_TransferGetReceiveCountEDMA ( FLEXIO\_CAMERA\_Type \* *base*, flexio\_camera\_edma\_handle\_t \* *handle*, size\_t \* *count* )**

This function gets the number of bytes still not received.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_CAMERA_Type</a> .
<i>handle</i>	Pointer to the flexio_camera_edma_handle_t structure.
<i>count</i>	Number of bytes sent so far by the non-blocking transaction.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_InvalidArgument</i>	The count parameter is invalid.

## 24.4 FlexIO I2C Master Driver

### 24.4.1 Overview

The MCUXpresso SDK provides a peripheral driver for I2C master function using Flexible I/O module of MCUXpresso SDK devices.

The FlexIO I2C master driver includes functional APIs and transactional APIs.

Functional APIs target low level APIs. Functional APIs can be used for the FlexIO I2C master initialization/configuration/operation for the optimization/customization purpose. Using the functional APIs requires the knowledge of the FlexIO I2C master peripheral and how to organize functional APIs to meet the application requirements. The FlexIO I2C master functional operation groups provide the functional APIs set.

Transactional APIs target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code using the functional APIs or accessing the hardware registers.

Transactional APIs support an asynchronous transfer. This means that the functions [FLEXIO\\_I2C\\_MasterTransferNonBlocking\(\)](#) set up the interrupt non-blocking transfer. When the transfer completes, the upper layer is notified through a callback function with the kStatus\_Success status.

### 24.4.2 Typical use case

#### 24.4.2.1 FlexIO I2C master transfer using an interrupt method

```
flexio_i2c_master_handle_t g_m_handle;
flexio_i2c_master_config_t masterConfig;
flexio_i2c_master_transfer_t masterXfer;
volatile bool completionFlag = false;
const uint8_t sendData[] = [.....];
FLEXIO_I2C_Type i2cDev;

void FLEXIO_I2C_MasterCallback(FLEXIO_I2C_Type *base, status_t status, void *
    userData)
{
    userData = userData;

    if (kStatus_Success == status)
    {
        completionFlag = true;
    }
}

void main(void)
{
    //...

    FLEXIO_I2C_MasterGetDefaultConfig(&masterConfig);

    FLEXIO_I2C_MasterInit(&i2cDev, &user_config);
    FLEXIO_I2C_MasterTransferCreateHandle(&i2cDev, &g_m_handle,
        FLEXIO_I2C_MasterCallback, NULL);
}
```

```

// Prepares to send.
masterXfer.slaveAddress = g_accel_address[0];
masterXfer.direction = kI2C_Read;
masterXfer.subaddress = &who_am_i_reg;
masterXfer.subaddressSize = 1;
masterXfer.data = &who_am_i_value;
masterXfer.dataSize = 1;
masterXfer.flags = kI2C_TransferDefaultFlag;

// Sends out.
FLEXIO_I2C_MasterTransferNonBlocking(&i2cDev, &g_m_handle, &
    masterXfer);

// Wait for sending is complete.
while (!completionFlag)
{
}

// ...
}

```

## Data Structures

- struct **FLEXIO\_I2C\_Type**  
*Define FlexIO I2C master access structure typedef.* [More...](#)
- struct **flexio\_i2c\_master\_config\_t**  
*Define FlexIO I2C master user configuration structure.* [More...](#)
- struct **flexio\_i2c\_master\_transfer\_t**  
*Define FlexIO I2C master transfer structure.* [More...](#)
- struct **flexio\_i2c\_master\_handle\_t**  
*Define FlexIO I2C master handle structure.* [More...](#)

## Macros

- #define **I2C\_RETRY\_TIMES** 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*

## TypeDefs

- typedef void(\* **flexio\_i2c\_master\_transfer\_callback\_t** )(FLEXIO\_I2C\_Type \*base, flexio\_i2c\_master\_handle\_t \*handle, **status\_t** status, void \*userData)  
*FlexIO I2C master transfer callback typedef.*

## Enumerations

- enum {
 **kStatus\_FLEXIO\_I2C\_Busy** = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2C, 0),
 **kStatus\_FLEXIO\_I2C\_Idle** = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2C, 1),
 **kStatus\_FLEXIO\_I2C\_Nak** = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2C, 2),
 }

- `kStatus_FLEXIO_I2C_Timeout` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2C, 3) }
- FlexIO I2C transfer status.*
- enum `_flexio_i2c_master_interrupt` {
   
    `kFLEXIO_I2C_TxEmptyInterruptEnable` = 0x1U,
   
    `kFLEXIO_I2C_RxFullInterruptEnable` = 0x2U }
- Define FlexIO I2C master interrupt mask.*
- enum `_flexio_i2c_master_status_flags` {
   
    `kFLEXIO_I2C_TxEmptyFlag` = 0x1U,
   
    `kFLEXIO_I2C_RxFullFlag` = 0x2U,
   
    `kFLEXIO_I2C_ReceiveNakFlag` = 0x4U }
- Define FlexIO I2C master status mask.*
- enum `flexio_i2c_direction_t` {
   
    `kFLEXIO_I2C_Write` = 0x0U,
   
    `kFLEXIO_I2C_Read` = 0x1U }
- Direction of master transfer.*

## Driver version

- #define `FSL_FLEXIO_I2C_MASTER_DRIVER_VERSION` (MAKE\_VERSION(2, 5, 0))

## Initialization and deinitialization

- `status_t FLEXIO_I2C_CheckForBusyBus (FLEXIO_I2C_Type *base)`
  
    *Make sure the bus isn't already pulled down.*
- `status_t FLEXIO_I2C_MasterInit (FLEXIO_I2C_Type *base, flexio_i2c_master_config_t *masterConfig, uint32_t srcClock_Hz)`
  
    *Ungates the FlexIO clock, resets the FlexIO module, and configures the FlexIO I2C hardware configuration.*
- `void FLEXIO_I2C_MasterDeinit (FLEXIO_I2C_Type *base)`
  
    *De-initializes the FlexIO I2C master peripheral.*
- `void FLEXIO_I2C_MasterGetDefaultConfig (flexio_i2c_master_config_t *masterConfig)`
  
    *Gets the default configuration to configure the FlexIO module.*
- `static void FLEXIO_I2C_MasterEnable (FLEXIO_I2C_Type *base, bool enable)`
  
    *Enables/disables the FlexIO module operation.*

## Status

- `uint32_t FLEXIO_I2C_MasterGetStatusFlags (FLEXIO_I2C_Type *base)`
  
    *Gets the FlexIO I2C master status flags.*
- `void FLEXIO_I2C_MasterClearStatusFlags (FLEXIO_I2C_Type *base, uint32_t mask)`
  
    *Clears the FlexIO I2C master status flags.*

## Interrupts

- `void FLEXIO_I2C_MasterEnableInterrupts (FLEXIO_I2C_Type *base, uint32_t mask)`

- Enables the FlexIO i2c master interrupt requests.
- void **FLEXIO\_I2C\_MasterDisableInterrupts** (**FLEXIO\_I2C\_Type** \*base, **uint32\_t** mask)  
Disables the FlexIO I2C master interrupt requests.

## Bus Operations

- void **FLEXIO\_I2C\_MasterSetBaudRate** (**FLEXIO\_I2C\_Type** \*base, **uint32\_t** baudRate\_Bps, **uint32\_t** srcClock\_Hz)  
Sets the FlexIO I2C master transfer baudrate.
- void **FLEXIO\_I2C\_MasterStart** (**FLEXIO\_I2C\_Type** \*base, **uint8\_t** address, **flexio\_i2c\_direction\_t** direction)  
Sends START + 7-bit address to the bus.
- void **FLEXIO\_I2C\_MasterStop** (**FLEXIO\_I2C\_Type** \*base)  
Sends the stop signal on the bus.
- void **FLEXIO\_I2C\_MasterRepeatedStart** (**FLEXIO\_I2C\_Type** \*base)  
Sends the repeated start signal on the bus.
- void **FLEXIO\_I2C\_MasterAbortStop** (**FLEXIO\_I2C\_Type** \*base)  
Sends the stop signal when transfer is still on-going.
- void **FLEXIO\_I2C\_MasterEnableAck** (**FLEXIO\_I2C\_Type** \*base, **bool** enable)  
Configures the sent ACK/NAK for the following byte.
- **status\_t FLEXIO\_I2C\_MasterSetTransferCount** (**FLEXIO\_I2C\_Type** \*base, **uint16\_t** count)  
Sets the number of bytes to be transferred from a start signal to a stop signal.
- static void **FLEXIO\_I2C\_MasterWriteByte** (**FLEXIO\_I2C\_Type** \*base, **uint32\_t** data)  
Writes one byte of data to the I2C bus.
- static **uint8\_t FLEXIO\_I2C\_MasterReadByte** (**FLEXIO\_I2C\_Type** \*base)  
Reads one byte of data from the I2C bus.
- **status\_t FLEXIO\_I2C\_MasterWriteBlocking** (**FLEXIO\_I2C\_Type** \*base, **const uint8\_t** \*txBuff, **uint8\_t** txSize)  
Sends a buffer of data in bytes.
- **status\_t FLEXIO\_I2C\_MasterReadBlocking** (**FLEXIO\_I2C\_Type** \*base, **uint8\_t** \*rxBuff, **uint8\_t** rxSize)  
Receives a buffer of bytes.
- **status\_t FLEXIO\_I2C\_MasterTransferBlocking** (**FLEXIO\_I2C\_Type** \*base, **flexio\_i2c\_master\_transfer\_t** \*xfer)  
Performs a master polling transfer on the I2C bus.

## Transactional

- **status\_t FLEXIO\_I2C\_MasterTransferCreateHandle** (**FLEXIO\_I2C\_Type** \*base, **flexio\_i2c\_master\_handle\_t** \*handle, **flexio\_i2c\_master\_transfer\_callback\_t** callback, **void** \*userData)  
Initializes the I2C handle which is used in transactional functions.
- **status\_t FLEXIO\_I2C\_MasterTransferNonBlocking** (**FLEXIO\_I2C\_Type** \*base, **flexio\_i2c\_master\_handle\_t** \*handle, **flexio\_i2c\_master\_transfer\_t** \*xfer)  
Performs a master interrupt non-blocking transfer on the I2C bus.
- **status\_t FLEXIO\_I2C\_MasterTransferGetCount** (**FLEXIO\_I2C\_Type** \*base, **flexio\_i2c\_master\_handle\_t** \*handle, **size\_t** \*count)  
Gets the master transfer status during a interrupt non-blocking transfer.

- void **FLEXIO\_I2C\_MasterTransferAbort** (**FLEXIO\_I2C\_Type** \*base, **flexio\_i2c\_master\_handle\_t** \*handle)  
*Aborts an interrupt non-blocking transfer early.*
- void **FLEXIO\_I2C\_MasterTransferHandleIRQ** (void \*i2cType, void \*i2cHandle)  
*Master interrupt handler.*

## 24.4.3 Data Structure Documentation

### 24.4.3.1 struct FLEXIO\_I2C\_Type

#### Data Fields

- **FLEXIO\_Type** \* **flexioBase**  
*FlexIO base pointer.*
- **uint8\_t** **SDAPinIndex**  
*Pin select for I2C SDA.*
- **uint8\_t** **SCLPinIndex**  
*Pin select for I2C SCL.*
- **uint8\_t** **shifterIndex** [2]  
*Shifter index used in FlexIO I2C.*
- **uint8\_t** **timerIndex** [3]  
*Timer index used in FlexIO I2C.*
- **uint32\_t** **baudrate**  
*Master transfer baudrate, used to calculate delay time.*

#### Field Documentation

- (1) **FLEXIO\_Type\*** **FLEXIO\_I2C\_Type::flexioBase**
- (2) **uint8\_t** **FLEXIO\_I2C\_Type::SDAPinIndex**
- (3) **uint8\_t** **FLEXIO\_I2C\_Type::SCLPinIndex**
- (4) **uint8\_t** **FLEXIO\_I2C\_Type::shifterIndex[2]**
- (5) **uint8\_t** **FLEXIO\_I2C\_Type::timerIndex[3]**
- (6) **uint32\_t** **FLEXIO\_I2C\_Type::baudrate**

### 24.4.3.2 struct flexio\_i2c\_master\_config\_t

#### Data Fields

- **bool** **enableMaster**  
*Enables the FlexIO I2C peripheral at initialization time.*
- **bool** **enableInDoze**  
*Enable/disable FlexIO operation in doze mode.*
- **bool** **enableInDebug**  
*Enable/disable FlexIO operation in debug mode.*

- bool `enableFastAccess`  
Enable/disable fast access to FlexIO registers, fast access requires  
*the FlexIO clock to be at least twice the frequency of the bus clock.*
- uint32\_t `baudRate_Bps`  
*Baud rate in Bps.*

### Field Documentation

- (1) bool `flexio_i2c_master_config_t::enableMaster`
- (2) bool `flexio_i2c_master_config_t::enableInDoze`
- (3) bool `flexio_i2c_master_config_t::enableInDebug`
- (4) bool `flexio_i2c_master_config_t::enableFastAccess`
- (5) uint32\_t `flexio_i2c_master_config_t::baudRate_Bps`

### 24.4.3.3 struct flexio\_i2c\_master\_transfer\_t

#### Data Fields

- uint32\_t `flags`  
*Transfer flag which controls the transfer, reserved for FlexIO I2C.*
- uint8\_t `slaveAddress`  
*7-bit slave address.*
- `flexio_i2c_direction_t direction`  
*Transfer direction, read or write.*
- uint32\_t `subaddress`  
*Sub address.*
- uint8\_t `subaddressSize`  
*Size of command buffer.*
- uint8\_t volatile \* `data`  
*Transfer buffer.*
- volatile size\_t `dataSize`  
*Transfer size.*

### Field Documentation

- (1) uint32\_t `flexio_i2c_master_transfer_t::flags`
- (2) uint8\_t `flexio_i2c_master_transfer_t::slaveAddress`
- (3) `flexio_i2c_direction_t flexio_i2c_master_transfer_t::direction`
- (4) uint32\_t `flexio_i2c_master_transfer_t::subaddress`

Transferred MSB first.

- (5) `uint8_t flexio_i2c_master_transfer_t::subaddressSize`
- (6) `uint8_t volatile* flexio_i2c_master_transfer_t::data`
- (7) `volatile size_t flexio_i2c_master_transfer_t::dataSize`

#### 24.4.3.4 struct \_flexio\_i2c\_master\_handle

FlexIO I2C master handle typedef.

#### Data Fields

- `flexio_i2c_master_transfer_t transfer`  
*FlexIO I2C master transfer copy.*
- `size_t transferSize`  
*Total bytes to be transferred.*
- `uint8_t state`  
*Transfer state maintained during transfer.*
- `flexio_i2c_master_transfer_callback_t completionCallback`  
*Callback function called at transfer event.*
- `void *userData`  
*Callback parameter passed to callback function.*
- `bool needRestart`  
*Whether master needs to send re-start signal.*

#### Field Documentation

- (1) `flexio_i2c_master_transfer_t flexio_i2c_master_handle_t::transfer`
- (2) `size_t flexio_i2c_master_handle_t::transferSize`
- (3) `uint8_t flexio_i2c_master_handle_t::state`
- (4) `flexio_i2c_master_transfer_callback_t flexio_i2c_master_handle_t::completionCallback`

Callback function called at transfer event.

- (5) `void* flexio_i2c_master_handle_t::userData`
- (6) `bool flexio_i2c_master_handle_t::needRestart`

#### 24.4.4 Macro Definition Documentation

**24.4.4.1 `#define I2C_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`**

#### 24.4.5 Typedef Documentation

**24.4.5.1 `typedef void(* flexio_i2c_master_transfer_callback_t)(FLEXIO_I2C_Type *base, flexio_i2c_master_handle_t *handle, status_t status, void *userData)`**

#### 24.4.6 Enumeration Type Documentation

##### 24.4.6.1 anonymous enum

Enumerator

*kStatus\_FLEXIO\_I2C\_Busy* I2C is busy doing transfer.

*kStatus\_FLEXIO\_I2C\_Idle* I2C is busy doing transfer.

*kStatus\_FLEXIO\_I2C\_Nak* NAK received during transfer.

*kStatus\_FLEXIO\_I2C\_Timeout* Timeout polling status flags.

##### 24.4.6.2 enum \_flexio\_i2c\_master\_interrupt

Enumerator

*kFLEXIO\_I2C\_TxEmptyInterruptEnable* Tx buffer empty interrupt enable.

*kFLEXIO\_I2C\_RxFullInterruptEnable* Rx buffer full interrupt enable.

##### 24.4.6.3 enum \_flexio\_i2c\_master\_status\_flags

Enumerator

*kFLEXIO\_I2C\_TxEmptyFlag* Tx shifter empty flag.

*kFLEXIO\_I2C\_RxFullFlag* Rx shifter full/Transfer complete flag.

*kFLEXIO\_I2C\_ReceiveNakFlag* Receive NAK flag.

#### 24.4.6.4 enum flexio\_i2c\_direction\_t

Enumerator

**kFLEXIO\_I2C\_Write** Master send to slave.

**kFLEXIO\_I2C\_Read** Master receive from slave.

#### 24.4.7 Function Documentation

##### 24.4.7.1 status\_t FLEXIO\_I2C\_CheckForBusyBus ( FLEXIO\_I2C\_Type \* *base* )

Check the FLEXIO pin status to see whether either of SDA and SCL pin is pulled down.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure..
-------------	--

Return values

<i>kStatus_Success</i>	
<i>kStatus_FLEXIO_I2C_Busy</i>	

##### 24.4.7.2 status\_t FLEXIO\_I2C\_MasterInit ( FLEXIO\_I2C\_Type \* *base*, flexio\_i2c\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

Example

```
FLEXIO_I2C_Type base = {
    .flexioBase = FLEXIO,
    .SDAPinIndex = 0,
    .SCLPinIndex = 1,
    .shifterIndex = {0,1},
    .timerIndex = {0,1}
};
flexio_i2c_master_config_t config = {
    .enableInDoze = false,
    .enableInDebug = true,
    .enableFastAccess = false,
    .baudRate_Bps = 100000
};
FLEXIO_I2C_MasterInit(base, &config, srcClock_Hz);
```

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>masterConfig</i>	Pointer to <a href="#">flexio_i2c_master_config_t</a> structure.
<i>srcClock_Hz</i>	FlexIO source clock in Hz.

Return values

<i>kStatus_Success</i>	Initialization successful
<i>kStatus_InvalidArgument</i>	The source clock exceed upper range limitation

#### 24.4.7.3 void [FLEXIO\\_I2C\\_MasterDeinit](#) ( [FLEXIO\\_I2C\\_Type](#) \* *base* )

Calling this API Resets the FlexIO I2C master shifer and timer config, module can't work unless the [FLEXIO\\_I2C\\_MasterInit](#) is called.

Parameters

<i>base</i>	pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
-------------	---

#### 24.4.7.4 void [FLEXIO\\_I2C\\_MasterGetDefaultConfig](#) ( [flexio\\_i2c\\_master\\_config\\_t](#) \* *masterConfig* )

The configuration can be used directly for calling the [FLEXIO\\_I2C\\_MasterInit\(\)](#).

Example:

```
flexio_i2c_master_config_t config;
FLEXIO\_I2C\_MasterGetDefaultConfig(&config);
```

Parameters

<i>masterConfig</i>	Pointer to <a href="#">flexio_i2c_master_config_t</a> structure.
---------------------	--

#### 24.4.7.5 static void [FLEXIO\\_I2C\\_MasterEnable](#) ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [bool](#) *enable* ) [inline], [static]

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>enable</i>	Pass true to enable module, false does not have any effect.

#### 24.4.7.6 `uint32_t FLEXIO_I2C_MasterGetStatusFlags ( FLEXIO_I2C_Type * base )`

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure
-------------	--

Returns

Status flag, use status flag to AND [\\_flexio\\_i2c\\_master\\_status\\_flags](#) can get the related status.

#### 24.4.7.7 `void FLEXIO_I2C_MasterClearStatusFlags ( FLEXIO_I2C_Type * base, uint32_t mask )`

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>mask</i>	Status flag. The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• kFLEXIO_I2C_RxFullFlag</li> <li>• kFLEXIO_I2C_ReceiveNakFlag</li> </ul>

#### 24.4.7.8 `void FLEXIO_I2C_MasterEnableInterrupts ( FLEXIO_I2C_Type * base, uint32_t mask )`

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>mask</i>	Interrupt source. Currently only one interrupt request source: <ul style="list-style-type: none"> <li>• kFLEXIO_I2C_TransferCompleteInterruptEnable</li> </ul>

#### 24.4.7.9 `void FLEXIO_I2C_MasterDisableInterrupts ( FLEXIO_I2C_Type * base, uint32_t mask )`

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>mask</i>	Interrupt source.

#### 24.4.7.10 void FLEXIO\_I2C\_MasterSetBaudRate ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [uint32\\_t](#) *baudRate\_Bps*, [uint32\\_t](#) *srcClock\_Hz* )

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure
<i>baudRate_Bps</i>	the baud rate value in HZ
<i>srcClock_Hz</i>	source clock in HZ

#### 24.4.7.11 void FLEXIO\_I2C\_MasterStart ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [uint8\\_t](#) *address*, [flexio\\_i2c\\_direction\\_t](#) *direction* )

Note

This API should be called when the transfer configuration is ready to send a START signal and 7-bit address to the bus. This is a non-blocking API, which returns directly after the address is put into the data register but the address transfer is not finished on the bus. Ensure that the kFLEXIO\_I2C\_RxFullFlag status is asserted before calling this API.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>address</i>	7-bit address.
<i>direction</i>	transfer direction. This parameter is one of the values in <a href="#">flexio_i2c_direction_t</a> : <ul style="list-style-type: none"> <li>• kFLEXIO_I2C_Write: Transmit</li> <li>• kFLEXIO_I2C_Read: Receive</li> </ul>

#### 24.4.7.12 void FLEXIO\_I2C\_MasterStop ( [FLEXIO\\_I2C\\_Type](#) \* *base* )

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
-------------	---

#### 24.4.7.13 void FLEXIO\_I2C\_MasterRepeatedStart ( [FLEXIO\\_I2C\\_Type](#) \* *base* )

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
-------------	---

#### 24.4.7.14 void FLEXIO\_I2C\_MasterAbortStop ( [FLEXIO\\_I2C\\_Type](#) \* *base* )

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
-------------	---

#### 24.4.7.15 void FLEXIO\_I2C\_MasterEnableAck ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [bool](#) *enable* )

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>enable</i>	True to configure send ACK, false configure to send NAK.

#### 24.4.7.16 [status\\_t](#) FLEXIO\_I2C\_MasterSetTransferCount ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [uint16\\_t](#) *count* )

Note

Call this API before a transfer begins because the timer generates a number of clocks according to the number of bytes that need to be transferred.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
-------------	---

<i>count</i>	Number of bytes need to be transferred from a start signal to a re-start/stop signal
--------------	--

Return values

<i>kStatus_Success</i>	Successfully configured the count.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.

#### 24.4.7.17 static void FLEXIO\_I2C\_MasterWriteByte ( **FLEXIO\_I2C\_Type** \* *base*, **uint32\_t** *data* ) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is put into the data register but the data transfer is not finished on the bus. Ensure that the TxEmptyFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to <b>FLEXIO_I2C_Type</b> structure.
<i>data</i>	a byte of data.

#### 24.4.7.18 static uint8\_t FLEXIO\_I2C\_MasterReadByte ( **FLEXIO\_I2C\_Type** \* *base* ) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is read from the data register. Ensure that the data is ready in the register.

Parameters

<i>base</i>	Pointer to <b>FLEXIO_I2C_Type</b> structure.
-------------	--

Returns

data byte read.

#### 24.4.7.19 status\_t FLEXIO\_I2C\_MasterWriteBlocking ( **FLEXIO\_I2C\_Type** \* *base*, const **uint8\_t** \* *txBuff*, **uint8\_t** *txSize* )

## Note

This function blocks via polling until all bytes have been sent.

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>txBuff</i>	The data bytes to send.
<i>txSize</i>	The number of data bytes to send.

## Return values

<i>kStatus_Success</i>	Successfully write data.
<i>kStatus_FLEXIO_I2C_-Nak</i>	Receive NAK during writing data.
<i>kStatus_FLEXIO_I2C_-Timeout</i>	Timeout polling status flags.

#### 24.4.7.20 status\_t FLEXIO\_I2C\_MasterReadBlocking ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [uint8\\_t](#) \* *rxBuff*, [uint8\\_t](#) *rxSize* )

## Note

This function blocks via polling until all bytes have been received.

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>rxBuff</i>	The buffer to store the received bytes.
<i>rxSize</i>	The number of data bytes to be received.

## Return values

<i>kStatus_Success</i>	Successfully read data.
<i>kStatus_FLEXIO_I2C_-Timeout</i>	Timeout polling status flags.

#### 24.4.7.21 status\_t FLEXIO\_I2C\_MasterTransferBlocking ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [flexio\\_i2c\\_master\\_transfer\\_t](#) \* *xfer* )

## Note

The API does not return until the transfer succeeds or fails due to receiving NAK.

## Parameters

<i>base</i>	pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>xfer</i>	pointer to <a href="#">flexio_i2c_master_transfer_t</a> structure.

## Returns

status of status\_t.

**24.4.7.22 status\_t FLEXIO\_I2C\_MasterTransferCreateHandle ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [flexio\\_i2c\\_master\\_handle\\_t](#) \* *handle*, [flexio\\_i2c\\_master\\_transfer\\_callback\\_t](#) *callback*, void \* *userData* )**

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>handle</i>	Pointer to <a href="#">flexio_i2c_master_handle_t</a> structure to store the transfer state.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User param passed to the callback function.

## Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/isr table out of range.

**24.4.7.23 status\_t FLEXIO\_I2C\_MasterTransferNonBlocking ( [FLEXIO\\_I2C\\_Type](#) \* *base*, [flexio\\_i2c\\_master\\_handle\\_t](#) \* *handle*, [flexio\\_i2c\\_master\\_transfer\\_t](#) \* *xfer* )**

## Note

The API returns immediately after the transfer initiates. Call [FLEXIO\\_I2C\\_MasterTransferGetCount](#) to poll the transfer status to check whether the transfer is finished. If the return status is not [kStatus\\_FLEXIO\\_I2C\\_Busy](#), the transfer is finished.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure
<i>handle</i>	Pointer to <a href="#">flexio_i2c_master_handle_t</a> structure which stores the transfer state
<i>xfer</i>	pointer to <a href="#">flexio_i2c_master_transfer_t</a> structure

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_FLEXIO_I2C_Busy</i>	FlexIO I2C is not idle, is running another transfer.

#### 24.4.7.24 `status_t FLEXIO_I2C_MasterTransferGetCount ( FLEXIO_I2C_Type * base, flexio_i2c_master_handle_t * handle, size_t * count )`

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure.
<i>handle</i>	Pointer to <a href="#">flexio_i2c_master_handle_t</a> structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	<i>count</i> is Invalid.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.
<i>kStatus_Success</i>	Successfully return the count.

#### 24.4.7.25 `void FLEXIO_I2C_MasterTransferAbort ( FLEXIO_I2C_Type * base, flexio_i2c_master_handle_t * handle )`

Note

This API can be called at any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure
<i>handle</i>	Pointer to <a href="#">flexio_i2c_master_handle_t</a> structure which stores the transfer state

**24.4.7.26 void FLEXIO\_I2C\_MasterTransferHandleIRQ ( void \* *i2cType*, void \* *i2cHandle* )**

Parameters

<i>i2cType</i>	Pointer to <a href="#">FLEXIO_I2C_Type</a> structure
<i>i2cHandle</i>	Pointer to <a href="#">flexio_i2c_master_transfer_t</a> structure

## 24.5 FlexIO I2S Driver

### 24.5.1 Overview

The MCUXpresso SDK provides a peripheral driver for I2S function using Flexible I/O module of MCUXpresso SDK devices.

The FlexIO I2S driver includes functional APIs and transactional APIs.

Functional APIs are feature/property target low level APIs.

Functional APIs can be used for FlexIO I2S initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the FlexIO I2S peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. FlexIO I2S functional operation groups provide the functional APIs set.

Transactional APIs are transaction target high level APIs. The transactional APIs can be used to enable the peripheral and also in the application if the code size and performance of transactional APIs can satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the sai\_handle\_t as the first parameter. Initialize the handle by calling the FlexIO\_I2S\_TransferTxCreateHandle() or FlexIO\_I2S\_TransferRxCreateHandle() API.

Transactional APIs support asynchronous transfer. This means that the functions [FLEXIO\\_I2S\\_TransferSendNonBlocking\(\)](#) and [FLEXIO\\_I2S\\_TransferReceiveNonBlocking\(\)](#) set up an interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the kStatus\_FLEXIO\_I2S\_TxIdle and kStatus\_FLEXIO\_I2S\_RxIdle status.

### 24.5.2 Typical use case

#### 24.5.2.1 FlexIO I2S send/receive using an interrupt method

```
sai_handle_t g_saiTxHandle;
sai_config_t user_config;
sai_transfer_t sendXfer;
volatile bool txFinished;
volatile bool rxFinished;
const uint8_t sendData[] = [.....];

void FLEXIO_I2S_UserCallback(sai_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_I2S_TxIdle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_I2S_TxGetDefaultConfig(&user_config);
```

```

FLEXIO_I2S_TxInit(FLEXIO_I2S0, &user_config);
FLEXIO_I2S_TransferTxCreateHandle(FLEXIO_I2S0, &g_saiHandle,
    FLEXIO_I2S_UserCallback, NULL);

//Configures the SAI format.
FLEXIO_I2S_TransferTxSetTransferFormat(FLEXIO_I2S0, &g_saiHandle, mclkSource, mclk);

// Prepares to send.
sendXfer.data = sendData
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_I2S_TransferSendNonBlocking(FLEXIO_I2S0, &g_saiHandle, &
    sendXfer);

// Waiting to send is finished.
while (!txFinished)
{
}

// ...
}

```

#### 24.5.2.2 FLEXIO\_I2S send/receive using a DMA method

```

sai_handle_t g_saiHandle;
dma_handle_t g_saiTxDmaHandle;
dma_handle_t g_saiRxDmaHandle;
sai_config_t user_config;
sai_transfer_t sendXfer;
volatile bool txFinished;
uint8_t sendData[] = ...;

void FLEXIO_I2S_UserCallback(sai_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_I2S_TxIdle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_I2S_TxGetDefaultConfig(&user_config);
    FLEXIO_I2S_TxInit(FLEXIO_I2S0, &user_config);

    // Sets up the DMA.
    DMAMUX_Init(DMAMUX0);
    DMAMUX_SetSource(DMAMUX0, FLEXIO_I2S_TX_DMA_CHANNEL, FLEXIO_I2S_TX_DMA_REQUEST);
    DMAMUX_EnableChannel(DMAMUX0, FLEXIO_I2S_TX_DMA_CHANNEL);

    DMA_Init(DMA0);

    /* Creates the DMA handle. */
    DMA_TransferTxCreateHandle(&g_saiTxDmaHandle, DMA0, FLEXIO_I2S_TX_DMA_CHANNEL);

    FLEXIO_I2S_TransferTxCreateHandleDMA(FLEXIO_I2S0, &g_saiTxDmaHandle, FLEXIO_I2S_UserCallback, NULL);

    // Prepares to send.
    sendXfer.data = sendData
}

```

```

sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_I2S_TransferSendDMA(&g_saiHandle, &sendXfer);

// Waiting to send is finished.
while (!txFinished)
{
}

// ...
}

```

## Modules

- FlexIO eDMA I2S Driver

## Data Structures

- struct **FLEXIO\_I2S\_Type**  
*Define FlexIO I2S access structure typedef.* [More...](#)
- struct **flexio\_i2s\_config\_t**  
*FlexIO I2S configure structure.* [More...](#)
- struct **flexio\_i2s\_format\_t**  
*FlexIO I2S audio format, FlexIO I2S only support the same format in Tx and Rx.* [More...](#)
- struct **flexio\_i2s\_transfer\_t**  
*Define FlexIO I2S transfer structure.* [More...](#)
- struct **flexio\_i2s\_handle\_t**  
*Define FlexIO I2S handle structure.* [More...](#)

## Macros

- #define **I2S\_RETRY\_TIMES** 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*
- #define **FLEXIO\_I2S\_XFER\_QUEUE\_SIZE** (4U)  
*FlexIO I2S transfer queue size, user can refine it according to use case.*

## Typedefs

- typedef void(\* **flexio\_i2s\_callback\_t** )(FLEXIO\_I2S\_Type \*base, flexio\_i2s\_handle\_t \*handle, status\_t status, void \*userData)  
*FlexIO I2S xfer callback prototype.*

## Enumerations

- enum {
   
kStatus\_FLEXIO\_I2S\_Idle = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2S, 0),
   
kStatus\_FLEXIO\_I2S\_TxBusy = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2S, 1),
   
kStatus\_FLEXIO\_I2S\_RxBusy = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2S, 2),
   
kStatus\_FLEXIO\_I2S\_Error = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2S, 3),
   
kStatus\_FLEXIO\_I2S\_QueueFull = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2S, 4),
   
kStatus\_FLEXIO\_I2S\_Timeout }
   
*FlexIO I2S transfer status.*
- enum **flexio\_i2s\_master\_slave\_t** {
   
kFLEXIO\_I2S\_Master = 0x0U,
   
kFLEXIO\_I2S\_Slave = 0x1U }
   
*Master or slave mode.*
- enum {
   
kFLEXIO\_I2S\_TxDataRegEmptyInterruptEnable = 0x1U,
   
kFLEXIO\_I2S\_RxDataRegFullInterruptEnable = 0x2U }
   
*\_flexio\_i2s\_interrupt\_enable Define FlexIO I2S interrupt mask.*
- enum {
   
kFLEXIO\_I2S\_TxDataRegEmptyFlag = 0x1U,
   
kFLEXIO\_I2S\_RxDataRegFullFlag = 0x2U }
   
*\_flexio\_i2s\_status\_flags Define FlexIO I2S status mask.*
- enum **flexio\_i2s\_sample\_rate\_t** {
   
kFLEXIO\_I2S\_SampleRate8KHz = 8000U,
   
kFLEXIO\_I2S\_SampleRate11025Hz = 11025U,
   
kFLEXIO\_I2S\_SampleRate12KHz = 12000U,
   
kFLEXIO\_I2S\_SampleRate16KHz = 16000U,
   
kFLEXIO\_I2S\_SampleRate22050Hz = 22050U,
   
kFLEXIO\_I2S\_SampleRate24KHz = 24000U,
   
kFLEXIO\_I2S\_SampleRate32KHz = 32000U,
   
kFLEXIO\_I2S\_SampleRate44100Hz = 44100U,
   
kFLEXIO\_I2S\_SampleRate48KHz = 48000U,
   
kFLEXIO\_I2S\_SampleRate96KHz = 96000U }
   
*Audio sample rate.*
- enum **flexio\_i2s\_word\_width\_t** {
   
kFLEXIO\_I2S\_WordWidth8bits = 8U,
   
kFLEXIO\_I2S\_WordWidth16bits = 16U,
   
kFLEXIO\_I2S\_WordWidth24bits = 24U,
   
kFLEXIO\_I2S\_WordWidth32bits = 32U }
   
*Audio word width.*

## Driver version

- #define **FSL\_FLEXIO\_I2S\_DRIVER\_VERSION** (MAKE\_VERSION(2, 2, 0))
   
*FlexIO I2S driver version 2.2.0.*

## Initialization and deinitialization

- void **FLEXIO\_I2S\_Init** (**FLEXIO\_I2S\_Type** \*base, const **flexio\_i2s\_config\_t** \*config)  
*Initializes the FlexIO I2S.*
- void **FLEXIO\_I2S\_GetDefaultConfig** (**flexio\_i2s\_config\_t** \*config)  
*Sets the FlexIO I2S configuration structure to default values.*
- void **FLEXIO\_I2S\_Deinit** (**FLEXIO\_I2S\_Type** \*base)  
*De-initializes the FlexIO I2S.*
- static void **FLEXIO\_I2S\_Enable** (**FLEXIO\_I2S\_Type** \*base, bool enable)  
*Enables/disables the FlexIO I2S module operation.*

## Status

- uint32\_t **FLEXIO\_I2S\_GetStatusFlags** (**FLEXIO\_I2S\_Type** \*base)  
*Gets the FlexIO I2S status flags.*

## Interrupts

- void **FLEXIO\_I2S\_EnableInterrupts** (**FLEXIO\_I2S\_Type** \*base, uint32\_t mask)  
*Enables the FlexIO I2S interrupt.*
- void **FLEXIO\_I2S\_DisableInterrupts** (**FLEXIO\_I2S\_Type** \*base, uint32\_t mask)  
*Disables the FlexIO I2S interrupt.*

## DMA Control

- static void **FLEXIO\_I2S\_TxEnableDMA** (**FLEXIO\_I2S\_Type** \*base, bool enable)  
*Enables/disables the FlexIO I2S Tx DMA requests.*
- static void **FLEXIO\_I2S\_RxEnableDMA** (**FLEXIO\_I2S\_Type** \*base, bool enable)  
*Enables/disables the FlexIO I2S Rx DMA requests.*
- static uint32\_t **FLEXIO\_I2S\_TxGetDataRegisterAddress** (**FLEXIO\_I2S\_Type** \*base)  
*Gets the FlexIO I2S send data register address.*
- static uint32\_t **FLEXIO\_I2S\_RxGetDataRegisterAddress** (**FLEXIO\_I2S\_Type** \*base)  
*Gets the FlexIO I2S receive data register address.*

## Bus Operations

- void **FLEXIO\_I2S\_MasterSetFormat** (**FLEXIO\_I2S\_Type** \*base, **flexio\_i2s\_format\_t** \*format, uint32\_t srcClock\_Hz)  
*Configures the FlexIO I2S audio format in master mode.*
- void **FLEXIO\_I2S\_SlaveSetFormat** (**FLEXIO\_I2S\_Type** \*base, **flexio\_i2s\_format\_t** \*format)  
*Configures the FlexIO I2S audio format in slave mode.*
- status\_t **FLEXIO\_I2S\_WriteBlocking** (**FLEXIO\_I2S\_Type** \*base, uint8\_t bitWidth, uint8\_t \*txData, size\_t size)  
*Sends data using a blocking method.*
- static void **FLEXIO\_I2S\_WriteData** (**FLEXIO\_I2S\_Type** \*base, uint8\_t bitWidth, uint32\_t data)

- Writes data into a data register.  
 • `status_t FLEXIO_I2S_ReadBlocking (FLEXIO_I2S_Type *base, uint8_t bitWidth, uint8_t *rxData, size_t size)`  
*Receives a piece of data using a blocking method.*
- static `uint32_t FLEXIO_I2S_ReadData (FLEXIO_I2S_Type *base)`  
*Reads a data from the data register.*

## Transactional

- void `FLEXIO_I2S_TransferTxCreateHandle (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_callback_t callback, void *userData)`  
*Initializes the FlexIO I2S handle.*
- void `FLEXIO_I2S_TransferSetFormat (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_format_t *format, uint32_t srcClock_Hz)`  
*Configures the FlexIO I2S audio format.*
- void `FLEXIO_I2S_TransferRxCreateHandle (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_callback_t callback, void *userData)`  
*Initializes the FlexIO I2S receive handle.*
- `status_t FLEXIO_I2S_TransferSendNonBlocking (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_transfer_t *xfer)`  
*Performs an interrupt non-blocking send transfer on FlexIO I2S.*
- `status_t FLEXIO_I2S_TransferReceiveNonBlocking (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_transfer_t *xfer)`  
*Performs an interrupt non-blocking receive transfer on FlexIO I2S.*
- void `FLEXIO_I2S_TransferAbortSend (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle)`  
*Aborts the current send.*
- void `FLEXIO_I2S_TransferAbortReceive (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle)`  
*Aborts the current receive.*
- `status_t FLEXIO_I2S_TransferGetSendCount (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, size_t *count)`  
*Gets the remaining bytes to be sent.*
- `status_t FLEXIO_I2S_TransferGetReceiveCount (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, size_t *count)`  
*Gets the remaining bytes to be received.*
- void `FLEXIO_I2S_TransferTxHandleIRQ (void *i2sBase, void *i2sHandle)`  
*Tx interrupt handler.*
- void `FLEXIO_I2S_TransferRxHandleIRQ (void *i2sBase, void *i2sHandle)`  
*Rx interrupt handler.*

## 24.5.3 Data Structure Documentation

### 24.5.3.1 struct FLEXIO\_I2S\_Type

#### Data Fields

- `FLEXIO_Type * flexioBase`  
*FlexIO base pointer.*

- `uint8_t txPinIndex`  
*Tx data pin index in FlexIO pins.*
- `uint8_t rxPinIndex`  
*Rx data pin index.*
- `uint8_t bclkPinIndex`  
*Bit clock pin index.*
- `uint8_t fsPinIndex`  
*Frame sync pin index.*
- `uint8_t txShifterIndex`  
*Tx data shifter index.*
- `uint8_t rxShifterIndex`  
*Rx data shifter index.*
- `uint8_t bclkTimerIndex`  
*Bit clock timer index.*
- `uint8_t fsTimerIndex`  
*Frame sync timer index.*

#### 24.5.3.2 struct flexio\_i2s\_config\_t

##### Data Fields

- `bool enableI2S`  
*Enable FlexIO I2S.*
- `flexio_i2s_master_slave_t masterSlave`  
*Master or slave.*
- `flexio_pin_polarity_t txPinPolarity`  
*Tx data pin polarity, active high or low.*
- `flexio_pin_polarity_t rxPinPolarity`  
*Rx data pin polarity.*
- `flexio_pin_polarity_t bclkPinPolarity`  
*Bit clock pin polarity.*
- `flexio_pin_polarity_t fsPinPolarity`  
*Frame sync pin polarity.*
- `flexio_shifter_timer_polarity_t txTimerPolarity`  
*Tx data valid on bclk rising or falling edge.*
- `flexio_shifter_timer_polarity_t rxTimerPolarity`  
*Rx data valid on bclk rising or falling edge.*

#### 24.5.3.3 struct flexio\_i2s\_format\_t

##### Data Fields

- `uint8_t bitWidth`  
*Bit width of audio data, always 8/16/24/32 bits.*
- `uint32_t sampleRate_Hz`  
*Sample rate of the audio data.*

#### 24.5.3.4 struct flexio\_i2s\_transfer\_t

##### Data Fields

- `uint8_t * data`  
*Data buffer start pointer.*
- `size_t dataSize`  
*Bytes to be transferred.*

##### Field Documentation

(1) `size_t flexio_i2s_transfer_t::dataSize`

#### 24.5.3.5 struct \_flexio\_i2s\_handle

##### Data Fields

- `uint32_t state`  
*Internal state.*
- `flexio_i2s_callback_t callback`  
*Callback function called at transfer event.*
- `void * userData`  
*Callback parameter passed to callback function.*
- `uint8_t bitWidth`  
*Bit width for transfer, 8/16/24/32bits.*
- `flexio_i2s_transfer_t queue [FLEXIO_I2S_XFER_QUEUE_SIZE]`  
*Transfer queue storing queued transfer.*
- `size_t transferSize [FLEXIO_I2S_XFER_QUEUE_SIZE]`  
*Data bytes need to transfer.*
- `volatile uint8_t queueUser`  
*Index for user to queue transfer.*
- `volatile uint8_t queueDriver`  
*Index for driver to get the transfer data and size.*

## 24.5.4 Macro Definition Documentation

**24.5.4.1 #define FSL\_FLEXIO\_I2S\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 0))**

**24.5.4.2 #define I2S\_RETRY\_TIMES 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/**

**24.5.4.3 #define FLEXIO\_I2S\_XFER\_QUEUE\_SIZE (4U)**

## 24.5.5 Enumeration Type Documentation

### 24.5.5.1 anonymous enum

Enumerator

*kStatus\_FLEXIO\_I2S\_Idle* FlexIO I2S is in idle state.

*kStatus\_FLEXIO\_I2S\_TxBusy* FlexIO I2S Tx is busy.

*kStatus\_FLEXIO\_I2S\_RxBusy* FlexIO I2S Rx is busy.

*kStatus\_FLEXIO\_I2S\_Error* FlexIO I2S error occurred.

*kStatus\_FLEXIO\_I2S\_QueueFull* FlexIO I2S transfer queue is full.

*kStatus\_FLEXIO\_I2S\_Timeout* FlexIO I2S timeout polling status flags.

### 24.5.5.2 enum flexio\_i2s\_master\_slave\_t

Enumerator

*kFLEXIO\_I2S\_Master* Master mode.

*kFLEXIO\_I2S\_Slave* Slave mode.

### 24.5.5.3 anonymous enum

Enumerator

*kFLEXIO\_I2S\_TxDataRegEmptyInterruptEnable* Transmit buffer empty interrupt enable.

*kFLEXIO\_I2S\_RxDataRegFullInterruptEnable* Receive buffer full interrupt enable.

### 24.5.5.4 anonymous enum

Enumerator

*kFLEXIO\_I2S\_TxDataRegEmptyFlag* Transmit buffer empty flag.

*kFLEXIO\_I2S\_RxDataRegFullFlag* Receive buffer full flag.

#### 24.5.5.5 enum flexio\_i2s\_sample\_rate\_t

Enumerator

*kFLEXIO\_I2S\_SampleRate8KHz* Sample rate 8000Hz.  
*kFLEXIO\_I2S\_SampleRate11025Hz* Sample rate 11025Hz.  
*kFLEXIO\_I2S\_SampleRate12KHz* Sample rate 12000Hz.  
*kFLEXIO\_I2S\_SampleRate16KHz* Sample rate 16000Hz.  
*kFLEXIO\_I2S\_SampleRate22050Hz* Sample rate 22050Hz.  
*kFLEXIO\_I2S\_SampleRate24KHz* Sample rate 24000Hz.  
*kFLEXIO\_I2S\_SampleRate32KHz* Sample rate 32000Hz.  
*kFLEXIO\_I2S\_SampleRate44100Hz* Sample rate 44100Hz.  
*kFLEXIO\_I2S\_SampleRate48KHz* Sample rate 48000Hz.  
*kFLEXIO\_I2S\_SampleRate96KHz* Sample rate 96000Hz.

#### 24.5.5.6 enum flexio\_i2s\_word\_width\_t

Enumerator

*kFLEXIO\_I2S\_WordWidth8bits* Audio data width 8 bits.  
*kFLEXIO\_I2S\_WordWidth16bits* Audio data width 16 bits.  
*kFLEXIO\_I2S\_WordWidth24bits* Audio data width 24 bits.  
*kFLEXIO\_I2S\_WordWidth32bits* Audio data width 32 bits.

### 24.5.6 Function Documentation

#### 24.5.6.1 void FLEXIO\_I2S\_Init ( FLEXIO\_I2S\_Type \* *base*, const flexio\_i2s\_config\_t \* *config* )

This API configures FlexIO pins and shifter to I2S and configures the FlexIO I2S with a configuration structure. The configuration structure can be filled by the user, or be set with default values by [FLEXIO\\_I2S\\_GetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the FlexIO I2S driver. Otherwise, any access to the FlexIO I2S module can cause hard fault because the clock is not enabled.

Parameters

---

<i>base</i>	FlexIO I2S base pointer
<i>config</i>	FlexIO I2S configure structure.

#### 24.5.6.2 void FLEXIO\_I2S\_GetDefaultConfig ( flexio\_i2s\_config\_t \* *config* )

The purpose of this API is to get the configuration structure initialized for use in [FLEXIO\\_I2S\\_Init\(\)](#). Users may use the initialized structure unchanged in [FLEXIO\\_I2S\\_Init\(\)](#) or modify some fields of the structure before calling [FLEXIO\\_I2S\\_Init\(\)](#).

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

#### 24.5.6.3 void FLEXIO\_I2S\_Deinit ( FLEXIO\_I2S\_Type \* *base* )

Calling this API resets the FlexIO I2S shifter and timer config. After calling this API, call the [FLEXO\\_I2S\\_Init](#) to use the FlexIO I2S module.

Parameters

<i>base</i>	FlexIO I2S base pointer
-------------	-------------------------

#### 24.5.6.4 static void FLEXIO\_I2S\_Enable ( FLEXIO\_I2S\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a>
<i>enable</i>	True to enable, false dose not have any effect.

#### 24.5.6.5 uint32\_t FLEXIO\_I2S\_GetStatusFlags ( FLEXIO\_I2S\_Type \* *base* )

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure
-------------	--

Returns

Status flag, which are ORed by the enumerators in the \_flexio\_i2s\_status\_flags.

#### 24.5.6.6 void FLEXIO\_I2S\_EnableInterrupts ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [uint32\\_t](#) *mask* )

This function enables the FlexIO UART interrupt.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure
<i>mask</i>	interrupt source

#### 24.5.6.7 void FLEXIO\_I2S\_DisableInterrupts ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [uint32\\_t](#) *mask* )

This function disables the FlexIO UART interrupt.

Parameters

<i>base</i>	pointer to <a href="#">FLEXIO_I2S_Type</a> structure
<i>mask</i>	interrupt source

#### 24.5.6.8 static void FLEXIO\_I2S\_TxEnableDMA ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [bool](#) *enable* ) [inline], [static]

Parameters

<i>base</i>	FlexIO I2S base pointer
<i>enable</i>	True means enable DMA, false means disable DMA.

#### 24.5.6.9 static void FLEXIO\_I2S\_RxEnableDMA ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [bool](#) *enable* ) [inline], [static]

Parameters

<i>base</i>	FlexIO I2S base pointer
<i>enable</i>	True means enable DMA, false means disable DMA.

#### 24.5.6.10 static uint32\_t FLEXIO\_I2S\_TxGetDataRegisterAddress ( FLEXIO\_I2S\_Type \* *base* ) [inline], [static]

This function returns the I2S data register address, mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure
-------------	--

Returns

FlexIO i2s send data register address.

#### 24.5.6.11 static uint32\_t FLEXIO\_I2S\_RxGetDataRegisterAddress ( FLEXIO\_I2S\_Type \* *base* ) [inline], [static]

This function returns the I2S data register address, mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure
-------------	--

Returns

FlexIO i2s receive data register address.

#### 24.5.6.12 void FLEXIO\_I2S\_MasterSetFormat ( FLEXIO\_I2S\_Type \* *base*, flexio\_i2s\_format\_t \* *format*, uint32\_t *srcClock\_Hz* )

Audio format can be changed in run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure
<i>format</i>	Pointer to FlexIO I2S audio data format structure.
<i>srcClock_Hz</i>	I2S master clock source frequency in Hz.

#### 24.5.6.13 void [FLEXIO\\_I2S\\_SlaveSetFormat](#) ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [flexio\\_i2s\\_format\\_t](#) \* *format* )

Audio format can be changed in run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure
<i>format</i>	Pointer to FlexIO I2S audio data format structure.

#### 24.5.6.14 status\_t [FLEXIO\\_I2S\\_WriteBlocking](#) ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [uint8\\_t](#) *bitWidth*, [uint8\\_t](#) \* *txData*, [size\\_t](#) *size* )

Note

This function blocks via polling until data is ready to be sent.

Parameters

<i>base</i>	FlexIO I2S base pointer.
<i>bitWidth</i>	How many bits in a audio word, usually 8/16/24/32 bits.
<i>txData</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

Return values

<i>kStatus_Success</i>	Successfully write data.
<i>kStatus_FLEXIO_I2C_Timeout</i>	Timeout polling status flags.

#### 24.5.6.15 static void [FLEXIO\\_I2S\\_WriteData](#) ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [uint8\\_t](#) *bitWidth*, [uint32\\_t](#) *data* ) [inline], [static]

Parameters

<i>base</i>	FlexIO I2S base pointer.
<i>bitWidth</i>	How many bits in a audio word, usually 8/16/24/32 bits.
<i>data</i>	Data to be written.

#### 24.5.6.16 status\_t FLEXIO\_I2S\_ReadBlocking ( **FLEXIO\_I2S\_Type** \* *base*, **uint8\_t** *bitWidth*, **uint8\_t** \* *rxData*, **size\_t** *size* )

Note

This function blocks via polling until data is ready to be sent.

Parameters

<i>base</i>	FlexIO I2S base pointer
<i>bitWidth</i>	How many bits in a audio word, usually 8/16/24/32 bits.
<i>rxData</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

Return values

<i>kStatus_Success</i>	Successfully read data.
<i>kStatus_FLEXIO_I2C_Timeout</i>	Timeout polling status flags.

#### 24.5.6.17 static uint32\_t FLEXIO\_I2S\_ReadData ( **FLEXIO\_I2S\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	FlexIO I2S base pointer
-------------	-------------------------

Returns

Data read from data register.

**24.5.6.18 void FLEXIO\_I2S\_TransferTxCreateHandle ( FLEXIO\_I2S\_Type \* *base*,  
flexio\_i2s\_handle\_t \* *handle*, flexio\_i2s\_callback\_t *callback*, void \* *userData* )**

This function initializes the FlexIO I2S handle which can be used for other FlexIO I2S transactional APIs. Call this API once to get the initialized handle.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure
<i>handle</i>	Pointer to <a href="#">flexio_i2s_handle_t</a> structure to store the transfer state.
<i>callback</i>	FlexIO I2S callback function, which is called while finished a block.
<i>userData</i>	User parameter for the FlexIO I2S callback.

**24.5.6.19 void FLEXIO\_I2S\_TransferSetFormat ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [flexio\\_i2s\\_handle\\_t](#) \* *handle*, [flexio\\_i2s\\_format\\_t](#) \* *format*, [uint32\\_t](#) *srcClock\_Hz* )**

Audio format can be changed at run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure.
<i>handle</i>	FlexIO I2S handle pointer.
<i>format</i>	Pointer to audio data format structure.
<i>srcClock_Hz</i>	FlexIO I2S bit clock source frequency in Hz. This parameter should be 0 while in slave mode.

**24.5.6.20 void FLEXIO\_I2S\_TransferRxCreateHandle ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [flexio\\_i2s\\_handle\\_t](#) \* *handle*, [flexio\\_i2s\\_callback\\_t](#) *callback*, [void](#) \* *userData* )**

This function initializes the FlexIO I2S handle which can be used for other FlexIO I2S transactional APIs. Call this API once to get the initialized handle.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure.
<i>handle</i>	Pointer to <a href="#">flexio_i2s_handle_t</a> structure to store the transfer state.
<i>callback</i>	FlexIO I2S callback function, which is called while finished a block.
<i>userData</i>	User parameter for the FlexIO I2S callback.

**24.5.6.21 [status\\_t](#) FLEXIO\_I2S\_TransferSendNonBlocking ( [FLEXIO\\_I2S\\_Type](#) \* *base*, [flexio\\_i2s\\_handle\\_t](#) \* *handle*, [flexio\\_i2s\\_transfer\\_t](#) \* *xfer* )**

## Note

The API returns immediately after transfer initiates. Call FLEXIO\_I2S\_GetRemainingBytes to poll the transfer status and check whether the transfer is finished. If the return status is 0, the transfer is finished.

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure.
<i>handle</i>	Pointer to <a href="#">flexio_i2s_handle_t</a> structure which stores the transfer state
<i>xfer</i>	Pointer to <a href="#">flexio_i2s_transfer_t</a> structure

## Return values

<i>kStatus_Success</i>	Successfully start the data transmission.
<i>kStatus_FLEXIO_I2S_Tx-Busy</i>	Previous transmission still not finished, data not all written to TX register yet.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

#### 24.5.6.22 `status_t FLEXIO_I2S_TransferReceiveNonBlocking ( FLEXIO_I2S_Type * base, flexio_i2s_handle_t * handle, flexio_i2s_transfer_t * xfer )`

## Note

The API returns immediately after transfer initiates. Call FLEXIO\_I2S\_GetRemainingBytes to poll the transfer status to check whether the transfer is finished. If the return status is 0, the transfer is finished.

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure.
<i>handle</i>	Pointer to <a href="#">flexio_i2s_handle_t</a> structure which stores the transfer state
<i>xfer</i>	Pointer to <a href="#">flexio_i2s_transfer_t</a> structure

## Return values

<i>kStatus_Success</i>	Successfully start the data receive.
------------------------	--------------------------------------

<i>kStatus_FLEXIO_I2S_-RxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

#### 24.5.6.23 void FLEXIO\_I2S\_TransferAbortSend ( **FLEXIO\_I2S\_Type** \* *base*, **flexio\_i2s\_handle\_t** \* *handle* )

Note

This API can be called at any time when interrupt non-blocking transfer initiates to abort the transfer in a early time.

Parameters

<i>base</i>	Pointer to <b>FLEXIO_I2S_Type</b> structure.
<i>handle</i>	Pointer to <b>flexio_i2s_handle_t</b> structure which stores the transfer state

#### 24.5.6.24 void FLEXIO\_I2S\_TransferAbortReceive ( **FLEXIO\_I2S\_Type** \* *base*, **flexio\_i2s\_handle\_t** \* *handle* )

Note

This API can be called at any time when interrupt non-blocking transfer initiates to abort the transfer in a early time.

Parameters

<i>base</i>	Pointer to <b>FLEXIO_I2S_Type</b> structure.
<i>handle</i>	Pointer to <b>flexio_i2s_handle_t</b> structure which stores the transfer state

#### 24.5.6.25 **status\_t** FLEXIO\_I2S\_TransferGetSendCount ( **FLEXIO\_I2S\_Type** \* *base*, **flexio\_i2s\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	Pointer to <b>FLEXIO_I2S_Type</b> structure.
<i>handle</i>	Pointer to <b>flexio_i2s_handle_t</b> structure which stores the transfer state
<i>count</i>	Bytes sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

#### 24.5.6.26 status\_t FLEXIO\_I2S\_TransferGetReceiveCount ( **FLEXIO\_I2S\_Type** \* *base*, **flexio\_i2s\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	Pointer to <b>FLEXIO_I2S_Type</b> structure.
<i>handle</i>	Pointer to <b>flexio_i2s_handle_t</b> structure which stores the transfer state
<i>count</i>	Bytes received.

Returns

*count* Bytes received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

#### 24.5.6.27 void FLEXIO\_I2S\_TransferTxHandleIRQ ( **void** \* *i2sBase*, **void** \* *i2sHandle* )

Parameters

<i>i2sBase</i>	Pointer to <b>FLEXIO_I2S_Type</b> structure.
<i>i2sHandle</i>	Pointer to <b>flexio_i2s_handle_t</b> structure

#### 24.5.6.28 void FLEXIO\_I2S\_TransferRxHandleIRQ ( **void** \* *i2sBase*, **void** \* *i2sHandle* )

## Parameters

<i>i2sBase</i>	Pointer to <a href="#">FLEXIO_I2S_Type</a> structure.
<i>i2sHandle</i>	Pointer to <code>flexio_i2s_handle_t</code> structure.

## 24.5.7 FlexIO eDMA I2S Driver

### 24.5.7.1 Overview

#### Data Structures

- struct `flexio_i2s_edma_handle_t`

*FlexIO I2S DMA transfer handle, users should not touch the content of the handle.* [More...](#)

#### TypeDefs

- typedef void(\* `flexio_i2s_edma_callback_t`)(`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle, `status_t` status, void \*userData)

*FlexIO I2S eDMA transfer callback function for finish and error.*

#### Driver version

- #define `FSL_FLEXIO_I2S_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 7)`)  
*FlexIO I2S EDMA driver version 2.1.7.*

#### eDMA Transactional

- void `FLEXIO_I2S_TransferTxCreateHandleEDMA` (`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle, `flexio_i2s_edma_callback_t` callback, void \*userData, `edma_handle_t` \*dmaHandle)  
*Initializes the FlexIO I2S eDMA handle.*
- void `FLEXIO_I2S_TransferRxCreateHandleEDMA` (`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle, `flexio_i2s_edma_callback_t` callback, void \*userData, `edma_handle_t` \*dmaHandle)  
*Initializes the FlexIO I2S Rx eDMA handle.*
- void `FLEXIO_I2S_TransferSetFormatEDMA` (`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle, `flexio_i2s_format_t` \*format, uint32\_t srcClock\_Hz)  
*Configures the FlexIO I2S Tx audio format.*
- `status_t FLEXIO_I2S_TransferSendEDMA` (`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle, `flexio_i2s_transfer_t` \*xfer)  
*Performs a non-blocking FlexIO I2S transfer using DMA.*
- `status_t FLEXIO_I2S_TransferReceiveEDMA` (`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle, `flexio_i2s_transfer_t` \*xfer)  
*Performs a non-blocking FlexIO I2S receive using eDMA.*
- void `FLEXIO_I2S_TransferAbortSendEDMA` (`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle)  
*Aborts a FlexIO I2S transfer using eDMA.*
- void `FLEXIO_I2S_TransferAbortReceiveEDMA` (`FLEXIO_I2S_Type` \*base, `flexio_i2s_edma_handle_t` \*handle)  
*Aborts a FlexIO I2S receive using eDMA.*

- **status\_t FLEXIO\_I2S\_TransferGetSendCountEDMA** (**FLEXIO\_I2S\_Type** \*base, **flexio\_i2s\_edma\_handle\_t** \*handle, **size\_t** \*count)  
*Gets the remaining bytes to be sent.*
- **status\_t FLEXIO\_I2S\_TransferGetReceiveCountEDMA** (**FLEXIO\_I2S\_Type** \*base, **flexio\_i2s\_edma\_handle\_t** \*handle, **size\_t** \*count)  
*Get the remaining bytes to be received.*

## 24.5.7.2 Data Structure Documentation

### 24.5.7.2.1 struct \_flexio\_i2s\_edma\_handle

#### Data Fields

- **edma\_handle\_t \* dmaHandle**  
*DMA handler for FlexIO I2S send.*
- **uint8\_t bytesPerFrame**  
*Bytes in a frame.*
- **uint8\_t nbytes**  
*eDMA minor byte transfer count initially configured.*
- **uint32\_t state**  
*Internal state for FlexIO I2S eDMA transfer.*
- **flexio\_i2s\_edma\_callback\_t callback**  
*Callback for users while transfer finish or error occurred.*
- **void \* userData**  
*User callback parameter.*
- **edma\_tcd\_t tcd** [**FLEXIO\_I2S\_XFER\_QUEUE\_SIZE+1U**]  
*TCD pool for eDMA transfer.*
- **flexio\_i2s\_transfer\_t queue** [**FLEXIO\_I2S\_XFER\_QUEUE\_SIZE**]  
*Transfer queue storing queued transfer.*
- **size\_t transferSize** [**FLEXIO\_I2S\_XFER\_QUEUE\_SIZE**]  
*Data bytes need to transfer.*
- **volatile uint8\_t queueUser**  
*Index for user to queue transfer.*
- **volatile uint8\_t queueDriver**  
*Index for driver to get the transfer data and size.*

## Field Documentation

- (1) `uint8_t flexio_i2s_edma_handle_t::nbytes`
- (2) `edma_tcd_t flexio_i2s_edma_handle_t::tcd[FLEXIO_I2S_XFER_QUEUE_SIZE+1U]`
- (3) `flexio_i2s_transfer_t flexio_i2s_edma_handle_t::queue[FLEXIO_I2S_XFER_QUEUE_SIZE]`
- (4) `volatile uint8_t flexio_i2s_edma_handle_t::queueUser`

### 24.5.7.3 Macro Definition Documentation

**24.5.7.3.1 #define FSL\_FLEXIO\_I2S\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 7))**

### 24.5.7.4 Function Documentation

**24.5.7.4.1 void FLEXIO\_I2S\_TransferTxCreateHandleEDMA ( FLEXIO\_I2S\_Type \* *base*, flexio\_i2s\_edma\_handle\_t \* *handle*, flexio\_i2s\_edma\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *dmaHandle* )**

This function initializes the FlexIO I2S master DMA handle which can be used for other FlexIO I2S master transactional APIs. Usually, for a specified FlexIO I2S instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S eDMA handle pointer.
<i>callback</i>	FlexIO I2S eDMA callback function called while finished a block.
<i>userData</i>	User parameter for callback.
<i>dmaHandle</i>	eDMA handle for FlexIO I2S. This handle is a static value allocated by users.

**24.5.7.4.2 void FLEXIO\_I2S\_TransferRxCreateHandleEDMA ( FLEXIO\_I2S\_Type \* *base*, flexio\_i2s\_edma\_handle\_t \* *handle*, flexio\_i2s\_edma\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *dmaHandle* )**

This function initializes the FlexIO I2S slave DMA handle which can be used for other FlexIO I2S master transactional APIs. Usually, for a specified FlexIO I2S instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S eDMA handle pointer.
<i>callback</i>	FlexIO I2S eDMA callback function called while finished a block.
<i>userData</i>	User parameter for callback.
<i>dmaHandle</i>	eDMA handle for FlexIO I2S. This handle is a static value allocated by users.

**24.5.7.4.3 void FLEXIO\_I2S\_TransferSetFormatEDMA ( FLEXIO\_I2S\_Type \* *base*, flexio\_i2s\_edma\_handle\_t \* *handle*, flexio\_i2s\_format\_t \* *format*, uint32\_t *srcClock\_Hz* )**

Audio format can be changed in run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to format.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S eDMA handle pointer
<i>format</i>	Pointer to FlexIO I2S audio data format structure.
<i>srcClock_Hz</i>	FlexIO I2S clock source frequency in Hz, it should be 0 while in slave mode.

**24.5.7.4.4 status\_t FLEXIO\_I2S\_TransferSendEDMA ( FLEXIO\_I2S\_Type \* *base*, flexio\_i2s\_edma\_handle\_t \* *handle*, flexio\_i2s\_transfer\_t \* *xfer* )**

Note

This interface returned immediately after transfer initiates. Users should call FLEXIO\_I2S\_GetTransferStatus to poll the transfer status and check whether the FlexIO I2S transfer is finished.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a FlexIO I2S eDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input arguments is invalid.
<i>kStatus_TxBusy</i>	FlexIO I2S is busy sending data.

#### 24.5.7.4.5 status\_t FLEXIO\_I2S\_TransferReceiveEDMA ( **FLEXIO\_I2S\_Type \* base,** **flexio\_i2s\_edma\_handle\_t \* handle, flexio\_i2s\_transfer\_t \* xfer** )

Note

This interface returned immediately after transfer initiates. Users should call FLEXIO\_I2S\_GetReceiveRemainingBytes to poll the transfer status and check whether the FlexIO I2S transfer is finished.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a FlexIO I2S eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input arguments is invalid.
<i>kStatus_RxBusy</i>	FlexIO I2S is busy receiving data.

#### 24.5.7.4.6 void FLEXIO\_I2S\_TransferAbortSendEDMA ( **FLEXIO\_I2S\_Type \* base,** **flexio\_i2s\_edma\_handle\_t \* handle** )

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.

#### 24.5.7.4.7 void FLEXIO\_I2S\_TransferAbortReceiveEDMA ( **FLEXIO\_I2S\_Type \* base,** **flexio\_i2s\_edma\_handle\_t \* handle** )

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.

#### 24.5.7.4.8 status\_t FLEXIO\_I2S\_TransferGetSendCountEDMA ( **FLEXIO\_I2S\_Type** \* *base*, **flexio\_i2s\_edma\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>count</i>	Bytes sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

#### 24.5.7.4.9 status\_t FLEXIO\_I2S\_TransferGetReceiveCountEDMA ( **FLEXIO\_I2S\_Type** \* *base*, **flexio\_i2s\_edma\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>count</i>	Bytes received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

## 24.6 FlexIO MCU Interface LCD Driver

### 24.6.1 Overview

The MCUXpresso SDK provides a peripheral driver for LCD (8080 or 6800 interface) function using Flexible I/O module of MCUXpresso SDK devices.

The FlexIO LCD driver supports both 8-bit and 16-bit data bus, 8080 and 6800 interface. User could change the macro FLEXIO\_MCULCD\_DATA\_BUS\_WIDTH to choose 8-bit data bus or 16-bit data bus.

The FlexIO LCD driver supports three kinds of data transfer:

1. Send a data array. For example, send the LCD image data to the LCD controller.
2. Send a value many times. For example, send 0 many times to clean the LCD screen.
3. Read data into a data array. For example, read image from LCD controller.

The FlexIO LCD driver includes functional APIs and transactional APIs.

Functional APIs are feature/property target low level APIs. Functional APIs can be used for FlexIO LCD initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the FlexIO LCD peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. FlexIO LCD functional operation groups provide the functional APIs set.

Transactional APIs are transaction target high level APIs. The transactional APIs can be used to enable the peripheral and also in the application if the code size and performance of transactional APIs can satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code.

Transactional APIs support asynchronous transfer. This means that the function [FLEXIO\\_MCULCD\\_TransferNonBlocking](#) sets up an interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the kStatus\_FLEXIO\_MCULCD\_Idle status.

### 24.6.2 Typical use case

#### 24.6.2.1 FlexIO LCD send/receive using functional APIs

This example shows how to send command, or write and read data using the functional APIs. The data bus is 16-bit.

```
uint16_t dataToSend[] = { ... };
uint16_t dataToReceive[] = { ... };

FLEXIO_MCULCD_Type flexioLcdDev;
flexio_MCULCD_transfer_t xfer;
flexio_MCULCD_config_t config;

FLEXIO_MCULCD_GetDefaultConfig(&config);
FLEXIO_MCULCD_Init(&flexioLcdDev, &config, 120000000);

// Method 1:
FLEXIO_MCULCD_StartTransfer(&flexioLcdDev);
```

```

FLEXIO_MCULCD_WriteCommandBlocking(&flexioLcdDev, command1);
FLEXIO_MCULCD_StopTransfer(&flexioLcdDev);

// Method 2:
xfer.command = command1;
xfer.dataCount = 0; // Only send command, no data transfer.
FLEXIO_MCULCD_TransferBlocking(&flexioLcdDev, &xfer);

// Method 1:
FLEXIO_MCULCD_StartTransfer(&flexioLcdDev);
FLEXIO_MCULCD_WriteCommandBlocking(&flexioLcdDev, command2);
FLEXIO_MCULCD_WriteDataArrayBlocking(&flexioLcdDev, dataToSend, sizeof(
    dataToSend));
FLEXIO_MCULCD_StopTransfer(&flexioLcdDev);

// Method 2:
xfer.command = command2;
xfer.mode = kFLEXIO_MCULCD_WriteArray;
xfer.dataAddrOrSameValue = (uint32_t)dataToSend;
xfer.dataCount = sizeof(dataToSend);
FLEXIO_MCULCD_TransferBlocking(&flexioLcdDev, &xfer);

// Method 1:
FLEXIO_MCULCD_StartTransfer(&flexioLcdDev);
FLEXIO_MCULCD_WriteCommandBlocking(&flexioLcdDev, command2);
FLEXIO_MCULCD_WriteSameValueBlocking(&flexioLcdDev, value, 1000); //
    Send value 1000 times
FLEXIO_MCULCD_StopTransfer(&flexioLcdDev);

// Method 2:
xfer.command = command2;
xfer.mode = kFLEXIO_MCULCD_WriteSameValue;
xfer.dataAddrOrSameValue = value;
xfer.dataCount = 1000;
FLEXIO_MCULCD_TransferBlocking(&flexioLcdDev, &xfer);

// Method 1:
FLEXIO_MCULCD_StartTransfer(&flexioLcdDev);
FLEXIO_MCULCD_WriteCommandBlocking(&flexioLcdDev, command3);
FLEXIO_MCULCD_ReadDataArrayBlocking(&flexioLcdDev, dataToReceive, sizeof(
    dataToReceive));
FLEXIO_MCULCD_StopTransfer(&flexioLcdDev);

// Method 2:
xfer.command = command3;
xfer.mode = kFLEXIO_MCULCD_ReadArray;
xfer.dataAddrOrSameValue = (uint32_t)dataToReceive;
xfer.dataCount = sizeof(dataToReceive);
FLEXIO_MCULCD_TransferBlocking(&flexioLcdDev, &xfer);

```

#### 24.6.2.2 FlexIO LCD send/receive using interrupt transactional APIs

```

flexio_MCULCD_handle_t handle;
volatile bool completeFlag = false;

void flexioLcdCallback(FLEXIO_MCULCD_Type *base, flexio_MCULCD_handle_t *handle,
    status_t status, void *userData)
{
    if (kStatus_FLEXIO_MCULCD_Idle == status)
    {
        completeFlag = true;
    }
}

void main(void)

```

```

{
    // Init the FlexIO LCD driver.
    FLEXIO_MCULCD_Init(...);

    // Create the transactional handle.
    FLEXIO_MCULCD_TransferCreateHandle(&flexioLcdDev, &handle,
        flexioLcdCallback, NULL);

    xfer.command = command1;
    xfer.dataCount = 0; // Only send command, no data transfer.
    completeFlag = false;
    FLEXIO_MCULCD_TransferNonBlocking(&flexioLcdDev, &xfer);

    // When only send method, it is not necessary to wait for the callback,
    // because the command is sent using a blocking method internally. The
    // command has been sent out after the function FLEXIO_MCULCD_TransferNonBlocking
    // returns.
    while (!completeFlag)
    {
    }

    xfer.command = command2;
    xfer.mode = kFLEXIO_MCULCD_WriteArray;
    xfer.dataAddrOrSameValue = (uint32_t)dataToSend;
    xfer.dataCount = sizeof(dataToSend);
    completeFlag = false;
    FLEXIO_MCULCD_TransferNonBlocking(&flexioLcdDev, &handle, &xfer);

    while (!completeFlag)
    {
    }

    xfer.command = command2;
    xfer.mode = kFLEXIO_MCULCD_WriteSameValue;
    xfer.dataAddrOrSameValue = value;
    xfer.dataCount = 1000;
    completeFlag = false;
    FLEXIO_MCULCD_TransferNonBlocking(&flexioLcdDev, &handle, &xfer);

    while (!completeFlag)
    {
    }

    xfer.command = command3;
    xfer.mode = kFLEXIO_MCULCD_ReadArray;
    xfer.dataAddrOrSameValue = (uint32_t)dataToReceive;
    xfer.dataCount = sizeof(dataToReceive);
    completeFlag = false;
    FLEXIO_MCULCD_TransferNonBlocking(&flexioLcdDev, &handle, &xfer);

    while (!completeFlag)
    {
    }
}

```

## Modules

- [FlexIO eDMA MCU Interface LCD Driver](#)

*SDK provide eDMA transactional APIs to transfer data using eDMA, the eDMA method is similar with interrupt transactional method.*

## Data Structures

- struct **FLEXIO\_MCULCD\_Type**  
*Define FlexIO MCULCD access structure typedef.* [More...](#)
- struct **flexio\_mculed\_config\_t**  
*Define FlexIO MCULCD configuration structure.* [More...](#)
- struct **flexio\_mculed\_transfer\_t**  
*Define FlexIO MCULCD transfer structure.* [More...](#)
- struct **flexio\_mculed\_handle\_t**  
*Define FlexIO MCULCD handle structure.* [More...](#)

## Macros

- #define **FLEXIO\_MCULCD\_WAIT\_COMPLETE\_TIME** 512  
*The delay time to wait for FLEXIO transmit complete.*
- #define **FLEXIO\_MCULCD\_DATA\_BUS\_WIDTH** 16UL  
*The data bus width, must be 8 or 16.*

## TypeDefs

- typedef void(\* **flexio\_mculed\_pin\_func\_t** )(bool set)  
*Function to set or clear the CS and RS pin.*
- typedef void(\* **flexio\_mculed\_transfer\_callback\_t** )(FLEXIO\_MCULCD\_Type \*base, flexio\_mculed\_handle\_t \*handle, status\_t status, void \*userData)  
*FlexIO MCULCD callback for finished transfer.*

## Enumerations

- enum {
 kStatus\_FLEXIO\_MCULCD\_Idle = MAKE\_STATUS(kStatusGroup\_FLEXIO\_MCULCD, 0),
 kStatus\_FLEXIO\_MCULCD\_Busy = MAKE\_STATUS(kStatusGroup\_FLEXIO\_MCULCD, 1),
 kStatus\_FLEXIO\_MCULCD\_Error = MAKE\_STATUS(kStatusGroup\_FLEXIO\_MCULCD, 2) }
 *FlexIO LCD transfer status.*
- enum **flexio\_mculed\_pixel\_format\_t** {
 kFLEXIO\_MCULCD\_RGB565 = 0,
 kFLEXIO\_MCULCD\_BGR565,
 kFLEXIO\_MCULCD\_RGB888,
 kFLEXIO\_MCULCD\_BGR888 }
 *Define FlexIO MCULCD pixel format.*
- enum **flexio\_mculed\_bus\_t** {
 kFLEXIO\_MCULCD\_8080,
 kFLEXIO\_MCULCD\_6800 }
 *Define FlexIO MCULCD bus type.*
- enum **\_flexio\_mculed\_interrupt\_enable** {
 kFLEXIO\_MCULCD\_TxEmptyInterruptEnable = (1U << 0U),

- `kFLEXIO_MCULCD_RxFullInterruptEnable = (1U << 1U) }`  
*Define FlexIO MCULCD interrupt mask.*
- enum `_flexio_mculed_status_flags {`  
`kFLEXIO_MCULCD_TxEmptyFlag = (1U << 0U),`  
`kFLEXIO_MCULCD_RxFullFlag = (1U << 1U) }`  
*Define FlexIO MCULCD status mask.*
- enum `_flexio_mculed_dma_enable {`  
`kFLEXIO_MCULCD_TxDmaEnable = 0x1U,`  
`kFLEXIO_MCULCD_RxDmaEnable = 0x2U }`  
*Define FlexIO MCULCD DMA mask.*
- enum `flexio_mculed_transfer_mode_t {`  
`kFLEXIO_MCULCD_ReadArray,`  
`kFLEXIO_MCULCD_WriteArray,`  
`kFLEXIO_MCULCD_WriteSameValue }`  
*Transfer mode.*

## Driver version

- `#define FSL_FLEXIO_MCULCD_DRIVER_VERSION (MAKE_VERSION(2, 0, 8))`  
*FlexIO MCULCD driver version.*

## FlexIO MCULCD Configuration

- `status_t FLEXIO_MCULCD_Init (FLEXIO_MCULCD_Type *base, flexio_mculed_config_t *config, uint32_t srcClock_Hz)`  
*Ungates the FlexIO clock, resets the FlexIO module, configures the FlexIO MCULCD hardware, and configures the FlexIO MCULCD with FlexIO MCULCD configuration.*
- void `FLEXIO_MCULCD_Deinit (FLEXIO_MCULCD_Type *base)`  
*Resets the FLEXIO\_MCULCD timer and shifter configuration.*
- void `FLEXIO_MCULCD_GetDefaultConfig (flexio_mculed_config_t *config)`  
*Gets the default configuration to configure the FlexIO MCULCD.*

## Status

- `uint32_t FLEXIO_MCULCD_GetStatusFlags (FLEXIO_MCULCD_Type *base)`  
*Gets FlexIO MCULCD status flags.*
- void `FLEXIO_MCULCD_ClearStatusFlags (FLEXIO_MCULCD_Type *base, uint32_t mask)`  
*Clears FlexIO MCULCD status flags.*

## Interrupts

- void `FLEXIO_MCULCD_EnableInterrupts (FLEXIO_MCULCD_Type *base, uint32_t mask)`  
*Enables the FlexIO MCULCD interrupt.*
- void `FLEXIO_MCULCD_DisableInterrupts (FLEXIO_MCULCD_Type *base, uint32_t mask)`

*Disables the FlexIO MCULCD interrupt.*

## DMA Control

- static void **FLEXIO\_MCULCD\_EnableTxDMA** (**FLEXIO\_MCULCD\_Type** \*base, bool enable)  
*Enables/disables the FlexIO MCULCD transmit DMA.*
- static void **FLEXIO\_MCULCD\_EnableRxDMA** (**FLEXIO\_MCULCD\_Type** \*base, bool enable)  
*Enables/disables the FlexIO MCULCD receive DMA.*
- static uint32\_t **FLEXIO\_MCULCD\_GetTxDataRegisterAddress** (**FLEXIO\_MCULCD\_Type** \*base)  
*Gets the FlexIO MCULCD transmit data register address.*
- static uint32\_t **FLEXIO\_MCULCD\_GetRxDataRegisterAddress** (**FLEXIO\_MCULCD\_Type** \*base)  
*Gets the FlexIO MCULCD receive data register address.*

## Bus Operations

- status\_t **FLEXIO\_MCULCD\_SetBaudRate** (**FLEXIO\_MCULCD\_Type** \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Set desired baud rate.*
- void **FLEXIO\_MCULCD\_SetSingleBeatWriteConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Configures the FLEXIO MCULCD to multiple beats write mode.*
- void **FLEXIO\_MCULCD\_ClearSingleBeatWriteConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Clear the FLEXIO MCULCD multiple beats write mode configuration.*
- void **FLEXIO\_MCULCD\_SetSingleBeatReadConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Configures the FLEXIO MCULCD to multiple beats read mode.*
- void **FLEXIO\_MCULCD\_ClearSingleBeatReadConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Clear the FLEXIO MCULCD multiple beats read mode configuration.*
- void **FLEXIO\_MCULCD\_SetMultiBeatsWriteConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Configures the FLEXIO MCULCD to multiple beats write mode.*
- void **FLEXIO\_MCULCD\_ClearMultiBeatsWriteConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Clear the FLEXIO MCULCD multiple beats write mode configuration.*
- void **FLEXIO\_MCULCD\_SetMultiBeatsReadConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Configures the FLEXIO MCULCD to multiple beats read mode.*
- void **FLEXIO\_MCULCD\_ClearMultiBeatsReadConfig** (**FLEXIO\_MCULCD\_Type** \*base)  
*Clear the FLEXIO MCULCD multiple beats read mode configuration.*
- static void **FLEXIO\_MCULCD\_Enable** (**FLEXIO\_MCULCD\_Type** \*base, bool enable)  
*Enables/disables the FlexIO MCULCD module operation.*
- uint32\_t **FLEXIO\_MCULCD\_ReadData** (**FLEXIO\_MCULCD\_Type** \*base)  
*Read data from the FLEXIO MCULCD RX shifter buffer.*
- static void **FLEXIO\_MCULCD\_WriteData** (**FLEXIO\_MCULCD\_Type** \*base, uint32\_t data)  
*Write data into the FLEXIO MCULCD TX shifter buffer.*
- static void **FLEXIO\_MCULCD\_StartTransfer** (**FLEXIO\_MCULCD\_Type** \*base)  
*Assert the nCS to start transfer.*
- static void **FLEXIO\_MCULCD\_StopTransfer** (**FLEXIO\_MCULCD\_Type** \*base)  
*De-assert the nCS to stop transfer.*
- void **FLEXIO\_MCULCD\_WaitTransmitComplete** (void)  
*Wait for transmit data send out finished.*

- void `FLEXIO_MCULCD_WriteCommandBlocking` (`FLEXIO_MCULCD_Type` \*base, `uint32_t` command)
 

*Send command in blocking way.*
- void `FLEXIO_MCULCD_WriteDataArrayBlocking` (`FLEXIO_MCULCD_Type` \*base, const `void *data`, `size_t size`)
 

*Send data array in blocking way.*
- void `FLEXIO_MCULCD_ReadDataArrayBlocking` (`FLEXIO_MCULCD_Type` \*base, `void *data`, `size_t size`)
 

*Read data into array in blocking way.*
- void `FLEXIO_MCULCD_WriteSameValueBlocking` (`FLEXIO_MCULCD_Type` \*base, `uint32_t sameValue`, `size_t size`)
 

*Send the same value many times in blocking way.*
- void `FLEXIO_MCULCD_TransferBlocking` (`FLEXIO_MCULCD_Type` \*base, `flexio_mculed_transfer_t *xfer`)
 

*Performs a polling transfer.*

## Transactional

- `status_t FLEXIO_MCULCD_TransferCreateHandle` (`FLEXIO_MCULCD_Type` \*base, `flexio_mculed_handle_t *handle`, `flexio_mculed_transfer_callback_t callback`, `void *userData`)
 

*Initializes the FlexIO MCULCD handle, which is used in transactional functions.*
- `status_t FLEXIO_MCULCD_TransferNonBlocking` (`FLEXIO_MCULCD_Type` \*base, `flexio_mculed_handle_t *handle`, `flexio_mculed_transfer_t *xfer`)
 

*Transfer data using IRQ.*
- void `FLEXIO_MCULCD_TransferAbort` (`FLEXIO_MCULCD_Type` \*base, `flexio_mculed_handle_t *handle`)
 

*Aborts the data transfer, which used IRQ.*
- `status_t FLEXIO_MCULCD_TransferGetCount` (`FLEXIO_MCULCD_Type` \*base, `flexio_mculed_handle_t *handle`, `size_t *count`)
 

*Gets the data transfer status which used IRQ.*
- void `FLEXIO_MCULCD_TransferHandleIRQ` (`void *base`, `void *handle`)
 

*FlexIO MCULCD IRQ handler function.*

### 24.6.3 Data Structure Documentation

#### 24.6.3.1 struct `FLEXIO_MCULCD_Type`

##### Data Fields

- `FLEXIO_Type * flexioBase`

*FlexIO base pointer.*
- `flexio_mculed_bus_t busType`

*The bus type, 8080 or 6800.*
- `uint8_t dataPinStartIndex`

*Start index of the data pin, the FlexIO pin dataPinStartIndex to (dataPinStartIndex + FLEXIO\_MCULCD\_DATA\_BUS\_WIDTH - 1) will be used for data transfer.*

- `uint8_t ENWRPinIndex`  
*Pin select for WR(8080 mode), EN(6800 mode).*
- `uint8_t RDPinIndex`  
*Pin select for RD(8080 mode), not used in 6800 mode.*
- `uint8_t txShifterStartIndex`  
*Start index of shifters used for data write, it must be 0 or 4.*
- `uint8_t txShifterEndIndex`  
*End index of shifters used for data write.*
- `uint8_t rxShifterStartIndex`  
*Start index of shifters used for data read.*
- `uint8_t rxShifterEndIndex`  
*End index of shifters used for data read, it must be 3 or 7.*
- `uint8_t timerIndex`  
*Timer index used in FlexIO MCULCD.*
- `flexio_mculed_pin_func_t setCSPin`  
*Function to set or clear the CS pin.*
- `flexio_mculed_pin_func_t setRSPin`  
*Function to set or clear the RS pin.*
- `flexio_mculed_pin_func_t setRDWRPin`  
*Function to set or clear the RD/WR pin, only used in 6800 mode.*

## Field Documentation

- (1) `FLEXIO_Type* FLEXIO_MCULCD_Type::flexioBase`
- (2) `flexio_mculed_bus_t FLEXIO_MCULCD_Type::busType`
- (3) `uint8_t FLEXIO_MCULCD_Type::dataPinStartIndex`

Only support data bus width 8 and 16.

- (4) `uint8_t FLEXIO_MCULCD_Type::ENWRPinIndex`
- (5) `uint8_t FLEXIO_MCULCD_Type::RDPinIndex`
- (6) `uint8_t FLEXIO_MCULCD_Type::txShifterStartIndex`
- (7) `uint8_t FLEXIO_MCULCD_Type::txShifterEndIndex`
- (8) `uint8_t FLEXIO_MCULCD_Type::rxShifterStartIndex`
- (9) `uint8_t FLEXIO_MCULCD_Type::rxShifterEndIndex`
- (10) `uint8_t FLEXIO_MCULCD_Type::timerIndex`
- (11) `flexio_mculed_pin_func_t FLEXIO_MCULCD_Type::setCSPin`
- (12) `flexio_mculed_pin_func_t FLEXIO_MCULCD_Type::setRSPin`
- (13) `flexio_mculed_pin_func_t FLEXIO_MCULCD_Type::setRDWRPin`

#### 24.6.3.2 struct flexio\_mculed\_config\_t

##### Data Fields

- `bool enable`  
*Enable/disable FlexIO MCULCD after configuration.*
- `bool enableInDoze`  
*Enable/disable FlexIO operation in doze mode.*
- `bool enableInDebug`  
*Enable/disable FlexIO operation in debug mode.*
- `bool enableFastAccess`  
*Enable/disable fast access to FlexIO registers,  
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*
- `uint32_t baudRate_Bps`  
*Baud rate in bit-per-second for all data lines combined.*

**Field Documentation**

- (1) **bool flexio\_mculed\_config\_t::enable**
- (2) **bool flexio\_mculed\_config\_t::enableInDoze**
- (3) **bool flexio\_mculed\_config\_t::enableInDebug**
- (4) **bool flexio\_mculed\_config\_t::enableFastAccess**
- (5) **uint32\_t flexio\_mculed\_config\_t::baudRate\_Bps**

**24.6.3.3 struct flexio\_mculed\_transfer\_t****Data Fields**

- **uint32\_t command**  
*Command to send.*
- **flexio\_mculed\_transfer\_mode\_t mode**  
*Transfer mode.*
- **uint32\_t dataAddrOrSameValue**  
*When sending the same value for many times, this is the value to send.*
- **size\_t dataSize**  
*How many bytes to transfer.*

**Field Documentation**

- (1) **uint32\_t flexio\_mculed\_transfer\_t::command**
- (2) **flexio\_mculed\_transfer\_mode\_t flexio\_mculed\_transfer\_t::mode**
- (3) **uint32\_t flexio\_mculed\_transfer\_t::dataAddrOrSameValue**

When writing or reading array, this is the address of the data array.

- (4) **size\_t flexio\_mculed\_transfer\_t::dataSize**

**24.6.3.4 struct \_flexio\_mculed\_handle**

typedef for flexio\_mculed\_handle\_t in advance.

**Data Fields**

- **uint32\_t dataAddrOrSameValue**  
*When sending the same value for many times, this is the value to send.*
- **size\_t dataCount**  
*Total count to be transferred.*
- **volatile size\_t remainingCount**  
*Remaining count to transfer.*
- **volatile uint32\_t state**

*FlexIO MCULCD internal state.*

- **flexio\_mculed\_transfer\_callback\_t completionCallback**  
*FlexIO MCULCD transfer completed callback.*
- **void \*userData**  
*Callback parameter.*

## Field Documentation

(1) **uint32\_t flexio\_mculed\_handle\_t::dataAddrOrSameValue**

When writing or reading array, this is the address of the data array.

(2) **size\_t flexio\_mculed\_handle\_t::dataCount**

(3) **volatile size\_t flexio\_mculed\_handle\_t::remainingCount**

(4) **volatile uint32\_t flexio\_mculed\_handle\_t::state**

(5) **flexio\_mculed\_transfer\_callback\_t flexio\_mculed\_handle\_t::completionCallback**

(6) **void\* flexio\_mculed\_handle\_t::userData**

## 24.6.4 Macro Definition Documentation

**24.6.4.1 #define FSL\_FLEXIO\_MCULCD\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 8))**

**24.6.4.2 #define FLEXIO\_MCULCD\_WAIT\_COMPLETE\_TIME 512**

Currently there is no method to detect whether the data has been sent out from the shifter, so the driver use a software delay for this. When the data is written to shifter buffer, the driver call the delay function to wait for the data shift out. If this value is too small, then the last few bytes might be lost when writing data using interrupt method or DMA method.

## 24.6.5 Typedef Documentation

**24.6.5.1 typedef void(\* flexio\_mculed\_pin\_func\_t)(bool set)**

**24.6.5.2 typedef void(\* flexio\_mculed\_transfer\_callback\_t)(FLEXIO\_MCULCD\_Type  
 \*base, flexio\_mculed\_handle\_t \*handle, status\_t status, void \*userData)**

When transfer finished, the callback function is called and returns the status as kStatus\_FLEXIO\_MCULCD\_Idle.

## 24.6.6 Enumeration Type Documentation

### 24.6.6.1 anonymous enum

Enumerator

- kStatus\_FLEXIO\_MCULCD\_Idle*** FlexIO LCD is idle.
- kStatus\_FLEXIO\_MCULCD\_Busy*** FlexIO LCD is busy.
- kStatus\_FLEXIO\_MCULCD\_Error*** FlexIO LCD error occurred.

### 24.6.6.2 enum flexio\_mculed\_pixel\_format\_t

Enumerator

- kFLEXIO\_MCULCD\_RGB565*** RGB565, 16-bit.
- kFLEXIO\_MCULCD\_BGR565*** BGR565, 16-bit.
- kFLEXIO\_MCULCD\_RGB888*** RGB888, 24-bit.
- kFLEXIO\_MCULCD\_BGR888*** BGR888, 24-bit.

### 24.6.6.3 enum flexio\_mculed\_bus\_t

Enumerator

- kFLEXIO\_MCULCD\_8080*** Using Intel 8080 bus.
- kFLEXIO\_MCULCD\_6800*** Using Motorola 6800 bus.

### 24.6.6.4 enum \_flexio\_mculed\_interrupt\_enable

Enumerator

- kFLEXIO\_MCULCD\_TxEmptyInterruptEnable*** Transmit buffer empty interrupt enable.
- kFLEXIO\_MCULCD\_RxFullInterruptEnable*** Receive buffer full interrupt enable.

### 24.6.6.5 enum \_flexio\_mculed\_status\_flags

Enumerator

- kFLEXIO\_MCULCD\_TxEmptyFlag*** Transmit buffer empty flag.
- kFLEXIO\_MCULCD\_RxFullFlag*** Receive buffer full flag.

#### 24.6.6.6 enum \_flexio\_mculed\_dma\_enable

Enumerator

*kFLEXIO\_MCULCD\_TxDmaEnable* Tx DMA request source.

*kFLEXIO\_MCULCD\_RxDmaEnable* Rx DMA request source.

#### 24.6.6.7 enum flexio\_mculed\_transfer\_mode\_t

Enumerator

*kFLEXIO\_MCULCD\_ReadArray* Read data into an array.

*kFLEXIO\_MCULCD\_WriteArray* Write data from an array.

*kFLEXIO\_MCULCD\_WriteSameValue* Write the same value many times.

### 24.6.7 Function Documentation

#### 24.6.7.1 status\_t FLEXIO\_MCULCD\_Init ( FLEXIO\_MCULCD\_Type \* *base*, flexio\_mculed\_config\_t \* *config*, uint32\_t *srcClock\_Hz* )

The configuration structure can be filled by the user, or be set with default values by the [FLEXIO\\_MCULCD\\_GetDefaultConfig](#).

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>config</i>	Pointer to the <a href="#">flexio_mculed_config_t</a> structure.
<i>srcClock_Hz</i>	FlexIO source clock in Hz.

Return values

<i>kStatus_Success</i>	Initialization success.
<i>kStatus_InvalidArgument</i>	Initialization failed because of invalid argument.

#### 24.6.7.2 void FLEXIO\_MCULCD\_Deinit ( FLEXIO\_MCULCD\_Type \* *base* )

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

**24.6.7.3 void FLEXIO\_MCULCD\_GetDefaultConfig ( [flexio\\_mculed\\_config\\_t](#) \* *config* )**

The default configuration value is:

```
* config->enable = true;
* config->enableInDoze = false;
* config->enableInDebug = true;
* config->enableFastAccess = true;
* config->baudRate_Bps = 96000000U;
*
```

Parameters

<i>config</i>	Pointer to the <a href="#">flexio_mculed_config_t</a> structure.
---------------	--

**24.6.7.4 uint32\_t FLEXIO\_MCULCD\_GetStatusFlags ( [FLEXIO\\_MCULCD\\_Type](#) \* *base* )**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
-------------	--

Returns

status flag; OR'ed value or the [\\_flexio\\_mculed\\_status\\_flags](#).

Note

Don't use this function with DMA APIs.

**24.6.7.5 void FLEXIO\_MCULCD\_ClearStatusFlags ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, uint32\_t *mask* )**

Parameters

---

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>mask</i>	Status to clear, it is the OR'ed value of <a href="#">_flexio_mculed_status_flags</a> .

Note

Don't use this function with DMA APIs.

#### 24.6.7.6 void FLEXIO\_MCULCD\_EnableInterrupts ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [uint32\\_t](#) *mask* )

This function enables the FlexIO MCULCD interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>mask</i>	Interrupts to enable, it is the OR'ed value of <a href="#">_flexio_mculed_interrupt_enable</a> .

#### 24.6.7.7 void FLEXIO\_MCULCD\_DisableInterrupts ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [uint32\\_t](#) *mask* )

This function disables the FlexIO MCULCD interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>mask</i>	Interrupts to disable, it is the OR'ed value of <a href="#">_flexio_mculed_interrupt_enable</a> .

#### 24.6.7.8 static void FLEXIO\_MCULCD\_EnableTxDMA ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [bool](#) *enable* ) [inline], [static]

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>enable</i>	True means enable DMA, false means disable DMA.

#### 24.6.7.9 static void FLEXIO\_MCULCD\_EnableRxDMA ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [bool](#) *enable* ) [inline], [static]

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>enable</i>	True means enable DMA, false means disable DMA.

#### 24.6.7.10 static uint32\_t FLEXIO\_MCULCD\_GetTxDataRegisterAddress ( FLEXIO\_MCULCD\_Type \* *base* ) [inline], [static]

This function returns the MCULCD data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
-------------	--

Returns

FlexIO MCULCD transmit data register address.

#### 24.6.7.11 static uint32\_t FLEXIO\_MCULCD\_GetRxDataRegisterAddress ( FLEXIO\_MCULCD\_Type \* *base* ) [inline], [static]

This function returns the MCULCD data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
-------------	--

Returns

FlexIO MCULCD receive data register address.

#### 24.6.7.12 status\_t FLEXIO\_MCULCD\_SetBaudRate ( FLEXIO\_MCULCD\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClock\_Hz* )

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>baudRate_Bps</i>	Desired baud rate in bit-per-second for all data lines combined.
<i>srcClock_Hz</i>	FLEXIO clock frequency in Hz.

Return values

<i>kStatus_Success</i>	Set successfully.
<i>kStatus_InvalidArgument</i>	Could not set the baud rate.

#### 24.6.7.13 void FLEXIO\_MCULCD\_SetSingleBeatWriteConfig ( [FLEXIO\\_MCULCD\\_Type](#) \* *base* )

At the begining multiple beats write operation, the FLEXIO MCULCD is configured to multiple beats write mode using this function. After write operation, the configuration is cleared by [FLEXIO\\_MCULCD\\_ClearSingleBeatWriteConfig](#).

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### 24.6.7.14 void FLEXIO\_MCULCD\_ClearSingleBeatWriteConfig ( [FLEXIO\\_MCULCD\\_Type](#) \* *base* )

Clear the write configuration set by [FLEXIO\\_MCULCD\\_SetSingleBeatWriteConfig](#).

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### 24.6.7.15 void FLEXIO\_MCULCD\_SetSingleBeatReadConfig ( [FLEXIO\\_MCULCD\\_Type](#) \* *base* )

At the begining or multiple beats read operation, the FLEXIO MCULCD is configured to multiple beats read mode using this function. After read operation, the configuration is cleared by [FLEXIO\\_MCULCD\\_ClearSingleBeatReadConfig](#).

[\\_ClearSingleBeatReadConfig.](#)

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### **24.6.7.16 void FLEXIO\_MCULCD\_ClearSingleBeatReadConfig ( FLEXIO\_MCULCD\_Type \* *base* )**

Clear the read configuration set by [FLEXIO\\_MCULCD\\_SetSingleBeatReadConfig](#).

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### **24.6.7.17 void FLEXIO\_MCULCD\_SetMultiBeatsWriteConfig ( FLEXIO\_MCULCD\_Type \* *base* )**

At the begining multiple beats write operation, the FLEXIO MCULCD is configured to multiple beats write mode using this function. After write operation, the configuration is cleared by [FLEXIO\\_MCULCD\\_ClearMultiBeatsWriteConfig](#).

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### **24.6.7.18 void FLEXIO\_MCULCD\_ClearMultiBeatsWriteConfig ( FLEXIO\_MCULCD\_Type \* *base* )**

Clear the write configuration set by [FLEXIO\\_MCULCD\\_SetMultiBeatsWriteConfig](#).

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### **24.6.7.19 void FLEXIO\_MCULCD\_SetMultiBeatsReadConfig ( FLEXIO\_MCULCD\_Type \* *base* )**

At the begining or multiple beats read operation, the FLEXIO MCULCD is configured to multiple beats read mode using this function. After read operation, the configuration is cleared by FLEXIO\_MCULCD\_ClearMultBeatsReadConfig.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### **24.6.7.20 void FLEXIO\_MCULCD\_ClearMultiBeatsReadConfig ( FLEXIO\_MCULCD\_Type \* *base* )**

Clear the read configuration set by FLEXIO\_MCULCD\_SetMultiBeatsReadConfig.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
-------------	---

Note

This is an internal used function, upper layer should not use.

#### **24.6.7.21 static void FLEXIO\_MCULCD\_Enable ( FLEXIO\_MCULCD\_Type \* *base*, bool *enable* ) [inline], [static]**

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> .
<i>enable</i>	True to enable, false does not have any effect.

**24.6.7.22 uint32\_t FLEXIO\_MCULCD\_ReadData ( FLEXIO\_MCULCD\_Type \* *base* )**

Read data from the RX shift buffer directly, it does no check whether the buffer is empty or not.

If the data bus width is 8-bit:

```
* uint8_t value;
* value = (uint8_t)FLEXIO_MCULCD_ReadData(base);
*
```

If the data bus width is 16-bit:

```
* uint16_t value;
* value = (uint16_t)FLEXIO_MCULCD_ReadData(base);
*
```

## Note

This function returns the RX shifter buffer value (32-bit) directly. The return value should be converted according to data bus width.

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
-------------	--

## Returns

The data read out.

## Note

Don't use this function with DMA APIs.

**24.6.7.23 static void FLEXIO\_MCULCD\_WriteData ( FLEXIO\_MCULCD\_Type \* *base*, uint32\_t *data* ) [inline], [static]**

Write data into the TX shift buffer directly, it does no check whether the buffer is full or not.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>data</i>	The data to write.

Note

Don't use this function with DMA APIs.

**24.6.7.24 static void FLEXIO\_MCULCD\_StartTransfer ( FLEXIO\_MCULCD\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
-------------	--

**24.6.7.25 static void FLEXIO\_MCULCD\_StopTransfer ( FLEXIO\_MCULCD\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
-------------	--

**24.6.7.26 void FLEXIO\_MCULCD\_WaitTransmitComplete ( void )**

Currently there is no effective method to wait for the data send out from the shiter, so here use a while loop to wait.

Note

This is an internal used function.

**24.6.7.27 void FLEXIO\_MCULCD\_WriteCommandBlocking ( FLEXIO\_MCULCD\_Type \* *base*, uint32\_t *command* )**

This function sends the command and returns when the command has been sent out.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>command</i>	The command to send.

#### **24.6.7.28 void FLEXIO\_MCULCD\_WriteDataArrayBlocking ( FLEXIO\_MCULCD\_Type \* *base*, const void \* *data*, size\_t *size* )**

This function sends the data array and returns when the data sent out.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>data</i>	The data array to send.
<i>size</i>	How many bytes to write.

#### **24.6.7.29 void FLEXIO\_MCULCD\_ReadDataArrayBlocking ( FLEXIO\_MCULCD\_Type \* *base*, void \* *data*, size\_t *size* )**

This function reads the data into array and returns when the data read finished.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>data</i>	The array to save the data.
<i>size</i>	How many bytes to read.

#### **24.6.7.30 void FLEXIO\_MCULCD\_WriteSameValueBlocking ( FLEXIO\_MCULCD\_Type \* *base*, uint32\_t *sameValue*, size\_t *size* )**

This function sends the same value many times. It could be used to clear the LCD screen. If the data bus width is 8, this function will send LSB 8 bits of *sameValue* for *size* times. If the data bus is 16, this function will send LSB 16 bits of *sameValue* for *size* / 2 times.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>sameValue</i>	The same value to send.
<i>size</i>	How many bytes to send.

#### 24.6.7.31 void FLEXIO\_MCULCD\_TransferBlocking ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [flexio\\_mculed\\_transfer\\_t](#) \* *xfer* )

Note

The API does not return until the transfer finished.

Parameters

<i>base</i>	pointer to <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>xfer</i>	pointer to <a href="#">flexio_mculed_transfer_t</a> structure.

#### 24.6.7.32 status\_t FLEXIO\_MCULCD\_TransferCreateHandle ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [flexio\\_mculed\\_handle\\_t](#) \* *handle*, [flexio\\_mculed\\_transfer\\_callback\\_t](#) *callback*, [void](#) \* *userData* )

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>handle</i>	Pointer to the <a href="#">flexio_mculed_handle_t</a> structure to store the transfer state.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

#### 24.6.7.33 status\_t FLEXIO\_MCULCD\_TransferNonBlocking ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [flexio\\_mculed\\_handle\\_t](#) \* *handle*, [flexio\\_mculed\\_transfer\\_t](#) \* *xfer* )

This function sends data using IRQ. This is a non-blocking function, which returns right away. When all data is sent out/received, the callback function is called.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>handle</i>	Pointer to the flexio_mculed_handle_t structure to store the transfer state.
<i>xfer</i>	FlexIO MCULCD transfer structure. See <a href="#">flexio_mculed_transfer_t</a> .

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_MCULCD_Busy</i>	MCULCD is busy with another transfer.

#### 24.6.7.34 void FLEXIO\_MCULCD\_TransferAbort ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [flexio\\_mculed\\_handle\\_t](#) \* *handle* )

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>handle</i>	Pointer to the flexio_mculed_handle_t structure to store the transfer state.

#### 24.6.7.35 status\_t FLEXIO\_MCULCD\_TransferGetCount ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [flexio\\_mculed\\_handle\\_t](#) \* *handle*, [size\\_t](#) \* *count* )

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>handle</i>	Pointer to the flexio_mculed_handle_t structure to store the transfer state.
<i>count</i>	How many bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_Success</i>	Get the transferred count Successfully.
<i>kStatus_NoTransferIn-Progress</i>	No transfer in process.

#### 24.6.7.36 void FLEXIO\_MCULCD\_TransferHandleIRQ ( [void](#) \* *base*, [void](#) \* *handle* )

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_mculed_handle_t</code> structure to store the transfer state.

## 24.6.8 FlexIO eDMA MCU Interface LCD Driver

SDK provide eDMA transactional APIs to transfer data using eDMA, the eDMA method is similar with interrupt transactional method.

### 24.6.8.1 Overview

Note

eDMA transactional functions use multiple beats method for better performance, in contrast, the blocking functions and interrupt functions use single beat method. The function [FLEXIO\\_MCULCD\\_ReadData](#), [FLEXIO\\_MCULCD\\_WriteData](#), [FLEXIO\\_MCULCD\\_GetStatusFlags](#), and [FLEXIO\\_MCULCD\\_ClearStatusFlags](#) are only used for single beat case, so don't use these functions to work together with eDMA functions.

## FlexIO eDMA MCU Interface LCD Driver

### FLEXIO LCD send/receive using a DMA method

```
flexio_MCULCD_edma_handle_t handle;
volatile bool completeFlag = false;
edma_handle_t rxEdmaHandle;
edma_handle_t txEdmaHandle;

void flexioLcdCallback(FLEXIO_MCULCD_Type *base, flexio_MCULCD_edma_handle_t *handle,
                      status_t status, void *userData)
{
    if (kStatus_FLEXIO_MCULCD_Idle == status)
    {
        completeFlag = true;
    }
}

void main(void)
{
    // Create the edma Handle.
    EDMA_CreateHandle(&rxEdmaHandle, DMA0, channel);
    EDMA_CreateHandle(&txEdmaHandle, DMA0, channel);

    // Configure the DMAMUX.
    // ...
    // rxEdmaHandle should use the last FlexIO RX shifters as DMA request source.
    // txEdmaHandle should use the first FlexIO TX shifters as DMA request source.

    // Init the FlexIO LCD driver.
    FLEXIO_MCULCD_Init(...);

    // Create the transactional handle.
    FLEXIO_MCULCD_TransferCreateHandleEDMA(&flexioLcdDev, &handle,
                                           flexioLcdCallback, NULL, &txEdmaHandle, &rxEdmaHandle);

    xfer.command = command2;
    xfer.mode = kFLEXIO_MCULCD_WriteArray;
    xfer.dataAddrOrSameValue = (uint32_t)dataToSend;
    xfer.dataCount = sizeof(dataToSend);
    completeFlag = false;
    FLEXIO_MCULCD_TransferEDMA(&flexioLcdDev, &handle, &xfer);
```

```

while (!completeFlag)
{
}

xfer.command = command2;
xfer.mode = kFLEXIO_MCULCD_WriteSameValue;
xfer.dataAddrOrSameValue = value;
xfer.dataCount = 1000;
completeFlag = false;
FLEXIO_MCULCD_TransferEDMA(&flexioLcdDev, &handle, &xfer);

while (!completeFlag)
{
}

xfer.command = command3;
xfer.mode = kFLEXIO_MCULCD_ReadArray;
xfer.dataAddrOrSameValue = (uint32_t)dataToReceive;
xfer.dataCount = sizeof(dataToReceive);
completeFlag = false;
FLEXIO_MCULCD_TransferEDMA(&flexioLcdDev, &handle, &xfer);

while (!completeFlag)
{
}
}
}

```

## Data Structures

- struct [flexio\\_mculedma\\_handle\\_t](#)

*FlexIO MCULCD eDMA transfer handle, users should not touch the content of the handle.* [More...](#)

## Macros

- #define [FSL\\_FLEXIO\\_MCULCD\\_EDMA\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 0, 4))  
*FlexIO MCULCD EDMA driver version.*

## TypeDefs

- typedef void(\* [flexio\\_mculedma\\_transfer\\_callback\\_t](#))([FLEXIO\\_MCULCD\\_Type](#) \*base, [flexio\\_mculedma\\_handle\\_t](#) \*handle, [status\\_t](#) status, void \*userData)  
*FlexIO MCULCD master callback for transfer complete.*

## eDMA Transactional

- [status\\_t FLEXIO\\_MCULCD\\_TransferCreateHandleEDMA](#) ([FLEXIO\\_MCULCD\\_Type](#) \*base, [flexio\\_mculedma\\_handle\\_t](#) \*handle, [flexio\\_mculedma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*txDmaHandle, [edma\\_handle\\_t](#) \*rxDmaHandle)  
*Initializes the FLEXIO MCULCD master eDMA handle.*
- [status\\_t FLEXIO\\_MCULCD\\_TransferEDMA](#) ([FLEXIO\\_MCULCD\\_Type](#) \*base, [flexio\\_mculedma\\_handle\\_t](#) \*handle, [flexio\\_mculedma\\_transfer\\_t](#) \*xfer)  
*Performs a non-blocking FlexIO MCULCD transfer using eDMA.*

- void **FLEXIO\_MCULCD\_TransferAbortEDMA** (**FLEXIO\_MCULCD\_Type** \*base, **flexio\_mculedma\_handle\_t** \*handle)  
*Aborts a FlexIO MCULCD transfer using eDMA.*
- **status\_t FLEXIO\_MCULCD\_TransferGetCountEDMA** (**FLEXIO\_MCULCD\_Type** \*base, **flexio\_mculedma\_handle\_t** \*handle, **size\_t** \*count)  
*Gets the remaining bytes for FlexIO MCULCD eDMA transfer.*

## 24.6.8.2 Data Structure Documentation

### 24.6.8.2.1 struct \_flexio\_mculedma\_handle

typedef for **flexio\_mculedma\_handle\_t** in advance.

#### Data Fields

- **FLEXIO\_MCULCD\_Type \* base**  
*Pointer to the **FLEXIO\_MCULCD\_Type**.*
- **uint8\_t txShifterNum**  
*Number of shifters used for TX.*
- **uint8\_t rxShifterNum**  
*Number of shifters used for RX.*
- **uint32\_t minorLoopBytes**  
*eDMA transfer minor loop bytes.*
- **edma\_modulo\_t txEdmaModulo**  
*Modulo value for the FlexIO shifter buffer access.*
- **edma\_modulo\_t rxEdmaModulo**  
*Modulo value for the FlexIO shifter buffer access.*
- **uint32\_t dataAddrOrSameValue**  
*When sending the same value for many times, this is the value to send.*
- **size\_t dataCount**  
*Total count to be transferred.*
- volatile **size\_t remainingCount**  
*Remaining count still not transferred.*
- volatile **uint32\_t state**  
*FlexIO MCULCD driver internal state.*
- **edma\_handle\_t \* txDmaHandle**  
*DMA handle for MCULCD TX.*
- **edma\_handle\_t \* rxDmaHandle**  
*DMA handle for MCULCD RX.*
- **flexio\_mculedma\_transfer\_callback\_t completionCallback**  
*Callback for MCULCD DMA transfer.*
- **void \* userData**  
*User Data for MCULCD DMA callback.*

## Field Documentation

- (1) `FLEXIO_MCULCD_Type* flexio_mculcd_edma_handle_t::base`
- (2) `uint8_t flexio_mculcd_edma_handle_t::txShifterNum`
- (3) `uint8_t flexio_mculcd_edma_handle_t::rxShifterNum`
- (4) `uint32_t flexio_mculcd_edma_handle_t::minorLoopBytes`
- (5) `edma_modulo_t flexio_mculcd_edma_handle_t::txEdmaModulo`
- (6) `edma_modulo_t flexio_mculcd_edma_handle_t::rxEdmaModulo`
- (7) `uint32_t flexio_mculcd_edma_handle_t::dataAddrOrSameValue`

When writing or reading array, this is the address of the data array.

- (8) `size_t flexio_mculcd_edma_handle_t::dataCount`
- (9) `volatile size_t flexio_mculcd_edma_handle_t::remainingCount`
- (10) `volatile uint32_t flexio_mculcd_edma_handle_t::state`

### 24.6.8.3 Macro Definition Documentation

**24.6.8.3.1 #define FSL\_FLEXIO\_MCULCD\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 4))**

### 24.6.8.4 Typedef Documentation

**24.6.8.4.1 typedef void(\* flexio\_mculcd\_edma\_transfer\_callback\_t)(FLEXIO\_MCULCD\_Type \*base, flexio\_mculcd\_edma\_handle\_t \*handle, status\_t status, void \*userData)**

When transfer finished, the callback function is called and returns the `status` as `kStatus_FLEXIO_MCULCD_Idle`.

### 24.6.8.5 Function Documentation

**24.6.8.5.1 status\_t FLEXIO\_MCULCD\_TransferCreateHandleEDMA ( FLEXIO\_MCULCD\_Type \* base, flexio\_mculcd\_edma\_handle\_t \* handle, flexio\_mculcd\_edma\_transfer\_callback\_t callback, void \* userData, edma\_handle\_t \* txDmaHandle, edma\_handle\_t \* rxDmaHandle )**

This function initializes the FLEXO MCULCD master eDMA handle which can be used for other FLEXO MCULCD transactional APIs. For a specified FLEXO MCULCD instance, call this API once to get the initialized handle.

## Parameters

<i>base</i>	Pointer to <b>FLEXIO_MCULCD_Type</b> structure.
<i>handle</i>	Pointer to <b>flexio_mculedma_handle_t</b> structure to store the transfer state.
<i>callback</i>	MCULCD transfer complete callback, NULL means no callback.
<i>userData</i>	callback function parameter.
<i>txDmaHandle</i>	User requested eDMA handle for FlexIO MCULCD eDMA TX, the DMA request source of this handle should be the first of TX shifters.
<i>rxDmaHandle</i>	User requested eDMA handle for FlexIO MCULCD eDMA RX, the DMA request source of this handle should be the last of RX shifters.

## Return values

<i>kStatus_Success</i>	Successfully create the handle.
------------------------	---------------------------------

**24.6.8.5.2 status\_t FLEXIO\_MCULCD\_TransferEDMA ( **FLEXIO\_MCULCD\_Type** \* *base*, **flexio\_mculedma\_handle\_t** \* *handle*, **flexio\_mculed\_transfer\_t** \* *xfer* )**

This function returns immediately after transfer initiates. To check whether the transfer is completed, user could:

1. Use the transfer completed callback;
2. Polling function **FLEXIO\_MCULCD\_GetTransferCountEDMA**

## Parameters

<i>base</i>	pointer to <b>FLEXIO_MCULCD_Type</b> structure.
<i>handle</i>	pointer to <b>flexio_mculedma_handle_t</b> structure to store the transfer state.
<i>xfer</i>	Pointer to FlexIO MCULCD transfer structure.

## Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_MCULCD_Busy</i>	FlexIO MCULCD is not idle, it is running another transfer.

**24.6.8.5.3 void FLEXIO\_MCULCD\_TransferAbortEDMA ( **FLEXIO\_MCULCD\_Type** \* *base*, **flexio\_mculedma\_handle\_t** \* *handle* )**

Parameters

<i>base</i>	pointer to <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>handle</i>	FlexIO MCULCD eDMA handle pointer.

#### 24.6.8.5.4 status\_t FLEXIO\_MCULCD\_TransferGetCountEDMA ( [FLEXIO\\_MCULCD\\_Type](#) \* *base*, [flexio\\_mculcd\\_edma\\_handle\\_t](#) \**handle*, [size\\_t](#) \**count* )

Parameters

<i>base</i>	pointer to <a href="#">FLEXIO_MCULCD_Type</a> structure.
<i>handle</i>	FlexIO MCULCD eDMA handle pointer.
<i>count</i>	Number of count transferred so far by the eDMA transaction.

Return values

<i>kStatus_Success</i>	Get the transferred count Successfully.
<i>kStatus_NoTransferIn-Progress</i>	No transfer in process.

## 24.7 FlexIO SPI Driver

### 24.7.1 Overview

The MCUXpresso SDK provides a peripheral driver for an SPI function using the Flexible I/O module of MCUXpresso SDK devices.

FlexIO SPI driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for FlexIO SPI initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the FlexIO SPI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the [FLEXIO\\_SPI\\_Type](#) \*base as the first parameter. FlexIO SPI functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and also in the application if the code size and performance of transactional APIs can satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the flexio\_spi\_master\_handle\_t/flexio\_spi\_slave\_handle\_t as the second parameter. Initialize the handle by calling the [FLEXIO\\_SPI\\_MasterTransferCreateHandle\(\)](#) or [FLEXIO\\_SPI\\_SlaveTransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [FLEXIO\\_SPI\\_MasterTransferNonBlocking\(\)](#)/[FLEXIO\\_SPI\\_SlaveTransferNonBlocking\(\)](#) set up an interrupt for data transfer. When the transfer is complete, the upper layer is notified through a callback function with the kStatus\_FLEXIO\_SPI\_Idle status.

Note that the FlexIO SPI slave driver only supports discontinuous PCS access, which is a limitation. The FlexIO SPI slave driver can support continuous PCS, but the slave cannot adapt discontinuous and continuous PCS automatically. Users can change the timer disable mode in [FLEXIO\\_SPI\\_SlaveInit](#) manually, from kFLEXIO\_TimerDisableOnTimerCompare to kFLEXIO\_TimerDisableNever to enable a discontinuous PCS access. Only CPHA = 0 is supported.

### 24.7.2 Typical use case

#### 24.7.2.1 FlexIO SPI send/receive using an interrupt method

```
flexio_spi_master_handle_t g_spiHandle;
FLEXIO_SPI_Type spiDev;
volatile bool txFinished;
static uint8_t srcBuff[BUFFER_SIZE];
static uint8_t destBuff[BUFFER_SIZE];

void FLEXIO_SPI_MasterUserCallback(FLEXIO_SPI_Type *base, flexio_spi_master_handle_t *handle
    , status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_SPI_Idle == status)
    {
        txFinished = true;
    }
}
```

```

}

void main(void)
{
    //...
    flexio_spi_transfer_t xfer = {0};
    flexio_spi_master_config_t userConfig;

    FLEXIO_SPI_MasterGetDefaultConfig(&userConfig);
    userConfig.baudRate_Bps = 5000000U;

    spiDev.flexioBase = BOARD_FLEXIO_BASE;
    spiDev.SDOPinIndex = FLEXIO_SPI_MOSI_PIN;
    spiDev.SDIPinIndex = FLEXIO_SPI_MISO_PIN;
    spiDev.SCKPinIndex = FLEXIO_SPI_SCK_PIN;
    spiDev.CSnPinIndex = FLEXIO_SPI_CSn_PIN;
    spiDev.shifterIndex[0] = 0U;
    spiDev.shifterIndex[1] = 1U;
    spiDev.timerIndex[0] = 0U;
    spiDev.timerIndex[1] = 1U;

    FLEXIO_SPI_MasterInit(&spiDev, &userConfig, FLEXIO_CLOCK_FREQUENCY);

    xfer.txData = srcBuff;
    xfer.rxData = destBuff;
    xfer.dataSize = BUFFER_SIZE;
    xfer.flags = kFLEXIO_SPI_8bitMsb;
    FLEXIO_SPI_MasterTransferCreateHandle(&spiDev, &g_spiHandle,
                                         FLEXIO_SPI_MasterUserCallback, NULL);
    FLEXIO_SPI_MasterTransferNonBlocking(&spiDev, &g_spiHandle, &xfer);

    // Send finished.
    while (!txFinished)
    {
        // ...
    }
}

```

#### 24.7.2.2 FlexIO\_SPI Send/Receive in DMA way

```

dma_handle_t g_spiTxDmaHandle;
dma_handle_t g_spiRxDmaHandle;
flexio_spi_master_handle_t g_spiHandle;
FLEXIO_SPI_Type spiDev;
volatile bool txFinished;
static uint8_t srcBuff[BUFFER_SIZE];
static uint8_t destBuff[BUFFER_SIZE];
void FLEXIO_SPI_MasterUserCallback(FLEXIO_SPI_Type *base, flexio_spi_master_dma_handle_t
                                    *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_SPI_Idle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    flexio_spi_transfer_t xfer = {0};
    flexio_spi_master_config_t userConfig;

    FLEXIO_SPI_MasterGetDefaultConfig(&userConfig);

```

```

userConfig.baudRate_Bps = 500000U;

spiDev.flexioBase = BOARD_FLEXIO_BASE;
spiDev.SDOPinIndex = FLEXIO_SPI_MOSI_PIN;
spiDev.SDIPinIndex = FLEXIO_SPI_MISO_PIN;
spiDev.SCKPinIndex = FLEXIO_SPI_SCK_PIN;
spiDev.CSnPinIndex = FLEXIO_SPI_CSn_PIN;
spiDev.shifterIndex[0] = 0U;
spiDev.shifterIndex[1] = 1U;
spiDev.timerIndex[0] = 0U;
spiDev.timerIndex[1] = 1U;

/* Init DMAMUX. */
DMAMUX_Init(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR)

/* Init the DMA/EDMA module */
#if defined(FSL_FEATURE_SOC_DMA_COUNT) && FSL_FEATURE_SOC_DMA_COUNT > 0U
DMA_Init(EXAMPLE_FLEXIO_SPI_DMA_BASEADDR);
DMA_CreateHandle(&txHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR, FLEXIO_SPI_TX_DMA_CHANNEL);
DMA_CreateHandle(&rxHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR, FLEXIO_SPI_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_DMA_COUNT */

#if defined(FSL_FEATURE_SOC_EDMA_COUNT) && FSL_FEATURE_SOC_EDMA_COUNT > 0U
edma_config_t edmaConfig;

EDMA_GetDefaultConfig(&edmaConfig);
EDMA_Init(EXAMPLE_FLEXIO_SPI_DMA_BASEADDR, &edmaConfig);
EDMA_CreateHandle(&txHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR,
FLEXIO_SPI_TX_DMA_CHANNEL);
EDMA_CreateHandle(&rxHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR,
FLEXIO_SPI_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_EDMA_COUNT */

dma_request_source_tx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + spiDev.
shifterIndex[0]);
dma_request_source_rx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + spiDev.
shifterIndex[1]);

/* Requests DMA channels for transmit and receive. */
DMAMUX_SetSource(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR, FLEXIO_SPI_TX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_tx);
DMAMUX_SetSource(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR, FLEXIO_SPI_RX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_rx);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR,
FLEXIO_SPI_TX_DMA_CHANNEL);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR,
FLEXIO_SPI_RX_DMA_CHANNEL);

FLEXIO_SPI_MasterInit(&spiDev, &userConfig, FLEXIO_CLOCK_FREQUENCY);

/* Initializes the buffer. */
for (i = 0; i < BUFFER_SIZE; i++)
{
    srcBuff[i] = i;
}

/* Sends to the slave. */
xfer.txData = srcBuff;
xfer.rxData = destBuff;
xfer.dataSize = BUFFER_SIZE;
xfer.flags = kFLEXIO_SPI_8bitMsb;
FLEXIO_SPI_MasterTransferCreateHandleDMA(&spiDev, &g_spiHandle, FLEXIO_SPI_MasterUserCallback, NULL
, &g_spitxDmaHandle, &g_spirxDmaHandle);
FLEXIO_SPI_MasterTransferDMA(&spiDev, &g_spiHandle, &xfer);

// Send finished.
while (!txFinished)
{

```

```

    }
    // ...
}

```

## Modules

- FlexIO eDMA SPI Driver

## Data Structures

- struct **FLEXIO\_SPI\_Type**  
*Define FlexIO SPI access structure typedef. [More...](#)*
- struct **flexio\_spi\_master\_config\_t**  
*Define FlexIO SPI master configuration structure. [More...](#)*
- struct **flexio\_spi\_slave\_config\_t**  
*Define FlexIO SPI slave configuration structure. [More...](#)*
- struct **flexio\_spi\_transfer\_t**  
*Define FlexIO SPI transfer structure. [More...](#)*
- struct **flexio\_spi\_master\_handle\_t**  
*Define FlexIO SPI handle structure. [More...](#)*

## Macros

- #define **FLEXIO\_SPI\_DUMMYDATA** (0x00U)  
*FlexIO SPI dummy transfer data, the data is sent while txData is NULL.*
- #define **SPI\_RETRY\_TIMES** 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*
- #define **FLEXIO\_SPI\_XFER\_DATA\_FORMAT**(flag) ((flag) & (0x7U))  
*Get the transfer data format of width and bit order.*

## TypeDefs

- typedef flexio\_spi\_master\_handle\_t **flexio\_spi\_slave\_handle\_t**  
*Slave handle is the same with master handle.*
- typedef void(\* **flexio\_spi\_master\_transfer\_callback\_t** )(FLEXIO\_SPI\_Type \*base, flexio\_spi\_master\_handle\_t \*handle, status\_t status, void \*userData)  
*FlexIO SPI master callback for finished transmit.*
- typedef void(\* **flexio\_spi\_slave\_transfer\_callback\_t** )(FLEXIO\_SPI\_Type \*base, flexio\_spi\_slave\_handle\_t \*handle, status\_t status, void \*userData)  
*FlexIO SPI slave callback for finished transmit.*

## Enumerations

- enum {
   
kStatus\_FLEXIO\_SPI\_Busy = MAKE\_STATUS(kStatusGroup\_FLEXIO\_SPI, 1),
   
kStatus\_FLEXIO\_SPI\_Idle = MAKE\_STATUS(kStatusGroup\_FLEXIO\_SPI, 2),
   
kStatus\_FLEXIO\_SPI\_Error = MAKE\_STATUS(kStatusGroup\_FLEXIO\_SPI, 3),
   
kStatus\_FLEXIO\_SPI\_Timeout }
   
*Error codes for the FlexIO SPI driver.*
- enum **flexio\_spi\_clock\_phase\_t** {
   
kFLEXIO\_SPI\_ClockPhaseFirstEdge = 0x0U,
   
kFLEXIO\_SPI\_ClockPhaseSecondEdge = 0x1U }
   
*FlexIO SPI clock phase configuration.*
- enum **flexio\_spi\_shift\_direction\_t** {
   
kFLEXIO\_SPI\_MsbFirst = 0,
   
kFLEXIO\_SPI\_LsbFirst = 1 }
   
*FlexIO SPI data shifter direction options.*
- enum **flexio\_spi\_data\_bitcount\_mode\_t** {
   
kFLEXIO\_SPI\_8BitMode = 0x08U,
   
kFLEXIO\_SPI\_16BitMode = 0x10U,
   
kFLEXIO\_SPI\_32BitMode = 0x20U }
   
*FlexIO SPI data length mode options.*
- enum **\_flexio\_spi\_interrupt\_enable** {
   
kFLEXIO\_SPI\_TxEmptyInterruptEnable = 0x1U,
   
kFLEXIO\_SPI\_RxFullInterruptEnable = 0x2U }
   
*Define FlexIO SPI interrupt mask.*
- enum **\_flexio\_spi\_status\_flags** {
   
kFLEXIO\_SPI\_TxBufferEmptyFlag = 0x1U,
   
kFLEXIO\_SPI\_RxBufferFullFlag = 0x2U }
   
*Define FlexIO SPI status mask.*
- enum **\_flexio\_spi\_dma\_enable** {
   
kFLEXIO\_SPI\_TxDmaEnable = 0x1U,
   
kFLEXIO\_SPI\_RxDmaEnable = 0x2U,
   
kFLEXIO\_SPI\_DmaAllEnable = 0x3U }
   
*Define FlexIO SPI DMA mask.*
- enum **\_flexio\_spi\_transfer\_flags** {
   
kFLEXIO\_SPI\_8bitMsb = 0x0U,
   
kFLEXIO\_SPI\_8bitLsb = 0x1U,
   
kFLEXIO\_SPI\_16bitMsb = 0x2U,
   
kFLEXIO\_SPI\_16bitLsb = 0x3U,
   
kFLEXIO\_SPI\_32bitMsb = 0x4U,
   
kFLEXIO\_SPI\_32bitLsb = 0x5U,
   
kFLEXIO\_SPI\_csContinuous = 0x8U }
   
*Define FlexIO SPI transfer flags.*

## Driver version

- #define **FSL\_FLEXIO\_SPI\_DRIVER\_VERSION** (MAKE\_VERSION(2, 3, 2))  
*FlexIO SPI driver version.*

## FlexIO SPI Configuration

- void **FLEXIO\_SPI\_MasterInit** (**FLEXIO\_SPI\_Type** \*base, **flexio\_spi\_master\_config\_t** \*masterConfig, uint32\_t srcClock\_Hz)  
*Ungates the FlexIO clock, resets the FlexIO module, configures the FlexIO SPI master hardware, and configures the FlexIO SPI with FlexIO SPI master configuration.*
- void **FLEXIO\_SPI\_MasterDeinit** (**FLEXIO\_SPI\_Type** \*base)  
*Resets the FlexIO SPI timer and shifter config.*
- void **FLEXIO\_SPI\_MasterGetDefaultConfig** (**flexio\_spi\_master\_config\_t** \*masterConfig)  
*Gets the default configuration to configure the FlexIO SPI master.*
- void **FLEXIO\_SPI\_SlaveInit** (**FLEXIO\_SPI\_Type** \*base, **flexio\_spi\_slave\_config\_t** \*slaveConfig)  
*Ungates the FlexIO clock, resets the FlexIO module, configures the FlexIO SPI slave hardware configuration, and configures the FlexIO SPI with FlexIO SPI slave configuration.*
- void **FLEXIO\_SPI\_SlaveDeinit** (**FLEXIO\_SPI\_Type** \*base)  
*Gates the FlexIO clock.*
- void **FLEXIO\_SPI\_SlaveGetDefaultConfig** (**flexio\_spi\_slave\_config\_t** \*slaveConfig)  
*Gets the default configuration to configure the FlexIO SPI slave.*

## Status

- uint32\_t **FLEXIO\_SPI\_GetStatusFlags** (**FLEXIO\_SPI\_Type** \*base)  
*Gets FlexIO SPI status flags.*
- void **FLEXIO\_SPI\_ClearStatusFlags** (**FLEXIO\_SPI\_Type** \*base, uint32\_t mask)  
*Clears FlexIO SPI status flags.*

## Interrupts

- void **FLEXIO\_SPI\_EnableInterrupts** (**FLEXIO\_SPI\_Type** \*base, uint32\_t mask)  
*Enables the FlexIO SPI interrupt.*
- void **FLEXIO\_SPI\_DisableInterrupts** (**FLEXIO\_SPI\_Type** \*base, uint32\_t mask)  
*Disables the FlexIO SPI interrupt.*

## DMA Control

- void **FLEXIO\_SPI\_EnableDMA** (**FLEXIO\_SPI\_Type** \*base, uint32\_t mask, bool enable)  
*Enables/disables the FlexIO SPI transmit DMA.*
- static uint32\_t **FLEXIO\_SPI\_GetTxDataRegisterAddress** (**FLEXIO\_SPI\_Type** \*base, **flexio\_spi\_shift\_direction\_t** direction)  
*Gets the FlexIO SPI transmit data register address for MSB first transfer.*

- static uint32\_t **FLEXIO\_SPI\_GetRxDataRegisterAddress** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_shift\_direction\_t direction)

*Gets the FlexIO SPI receive data register address for the MSB first transfer.*

## Bus Operations

- static void **FLEXIO\_SPI\_Enable** (FLEXIO\_SPI\_Type \*base, bool enable)  
*Enables/disables the FlexIO SPI module operation.*
- void **FLEXIO\_SPI\_MasterSetBaudRate** (FLEXIO\_SPI\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClockHz)  
*Sets baud rate for the FlexIO SPI transfer, which is only used for the master.*
- static void **FLEXIO\_SPI\_WriteData** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_shift\_direction\_t direction, uint32\_t data)  
*Writes one byte of data, which is sent using the MSB method.*
- static uint32\_t **FLEXIO\_SPI\_ReadData** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_shift\_direction\_t direction)  
*Reads 8 bit/16 bit data.*
- status\_t **FLEXIO\_SPI\_WriteBlocking** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_shift\_direction\_t direction, const uint8\_t \*buffer, size\_t size)  
*Sends a buffer of data bytes.*
- status\_t **FLEXIO\_SPI\_ReadBlocking** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_shift\_direction\_t direction, uint8\_t \*buffer, size\_t size)  
*Receives a buffer of bytes.*
- status\_t **FLEXIO\_SPI\_MasterTransferBlocking** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_transfer\_t \*xfer)  
*Receives a buffer of bytes.*
- void **FLEXIO\_SPI\_FlushShifters** (FLEXIO\_SPI\_Type \*base)  
*Flush tx/rx shifters.*

## Transactional

- status\_t **FLEXIO\_SPI\_MasterTransferCreateHandle** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_master\_handle\_t \*handle, flexio\_spi\_master\_transfer\_callback\_t callback, void \*userData)  
*Initializes the FlexIO SPI Master handle, which is used in transactional functions.*
- status\_t **FLEXIO\_SPI\_MasterTransferNonBlocking** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_master\_handle\_t \*handle, flexio\_spi\_transfer\_t \*xfer)  
*Master transfer data using IRQ.*
- void **FLEXIO\_SPI\_MasterTransferAbort** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_master\_handle\_t \*handle)  
*Aborts the master data transfer, which used IRQ.*
- status\_t **FLEXIO\_SPI\_MasterTransferGetCount** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_master\_handle\_t \*handle, size\_t \*count)  
*Gets the data transfer status which used IRQ.*
- void **FLEXIO\_SPI\_MasterTransferHandleIRQ** (void \*spiType, void \*spiHandle)  
*FlexIO SPI master IRQ handler function.*
- status\_t **FLEXIO\_SPI\_SlaveTransferCreateHandle** (FLEXIO\_SPI\_Type \*base, flexio\_spi\_slave\_handle\_t \*handle, flexio\_spi\_slave\_transfer\_callback\_t callback, void \*userData)

*Initializes the FlexIO SPI Slave handle, which is used in transactional functions.*

- **status\_t FLEXIO\_SPI\_SlaveTransferNonBlocking** (**FLEXIO\_SPI\_Type** \*base, **flexio\_spi\_slave\_handle\_t** \*handle, **flexio\_spi\_transfer\_t** \*xfer)

*Slave transfer data using IRQ.*

- **static void FLEXIO\_SPI\_SlaveTransferAbort** (**FLEXIO\_SPI\_Type** \*base, **flexio\_spi\_slave\_handle\_t** \*handle)

*Aborts the slave data transfer which used IRQ, share same API with master.*

- **static status\_t FLEXIO\_SPI\_SlaveTransferGetCount** (**FLEXIO\_SPI\_Type** \*base, **flexio\_spi\_slave\_handle\_t** \*handle, **size\_t** \*count)

*Gets the data transfer status which used IRQ, share same API with master.*

- **void FLEXIO\_SPI\_SlaveTransferHandleIRQ** (void \*spiType, void \*spiHandle)

*FlexIO SPI slave IRQ handler function.*

## 24.7.3 Data Structure Documentation

### 24.7.3.1 struct FLEXIO\_SPI\_Type

#### Data Fields

- **FLEXIO\_Type** \* **flexioBase**  
*FlexIO base pointer.*
- **uint8\_t SDOPinIndex**  
*Pin select for data output.*
- **uint8\_t SDIPinIndex**  
*Pin select for data input.*
- **uint8\_t SCKPinIndex**  
*Pin select for clock.*
- **uint8\_t CSnPinIndex**  
*Pin select for enable.*
- **uint8\_t shifterIndex [2]**  
*Shifter index used in FlexIO SPI.*
- **uint8\_t timerIndex [2]**  
*Timer index used in FlexIO SPI.*

#### Field Documentation

(1) **FLEXIO\_Type\*** **FLEXIO\_SPI\_Type::flexioBase**

(2) **uint8\_t FLEXIO\_SPI\_Type::SDOPinIndex**

To set SDO pin in Hi-Z state, user needs to mux the pin as GPIO input and disable all pull up/down in application.

- (3) `uint8_t FLEXIO_SPI_Type::SDIPinIndex`
- (4) `uint8_t FLEXIO_SPI_Type::SCKPinIndex`
- (5) `uint8_t FLEXIO_SPI_Type::CSnPinIndex`
- (6) `uint8_t FLEXIO_SPI_Type::shifterIndex[2]`
- (7) `uint8_t FLEXIO_SPI_Type::timerIndex[2]`

#### 24.7.3.2 struct flexio\_spi\_master\_config\_t

##### Data Fields

- `bool enableMaster`  
*Enable/disable FlexIO SPI master after configuration.*
- `bool enableInDoze`  
*Enable/disable FlexIO operation in doze mode.*
- `bool enableInDebug`  
*Enable/disable FlexIO operation in debug mode.*
- `bool enableFastAccess`  
*Enable/disable fast access to FlexIO registers,  
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*
- `uint32_t baudRate_Bps`  
*Baud rate in Bps.*
- `flexio_spi_clock_phase_t phase`  
*Clock phase.*
- `flexio_spi_data_bitcount_mode_t dataMode`  
*8bit or 16bit mode.*

##### Field Documentation

- (1) `bool flexio_spi_master_config_t::enableMaster`
- (2) `bool flexio_spi_master_config_t::enableInDoze`
- (3) `bool flexio_spi_master_config_t::enableInDebug`
- (4) `bool flexio_spi_master_config_t::enableFastAccess`
- (5) `uint32_t flexio_spi_master_config_t::baudRate_Bps`
- (6) `flexio_spi_clock_phase_t flexio_spi_master_config_t::phase`
- (7) `flexio_spi_data_bitcount_mode_t flexio_spi_master_config_t::dataMode`

#### 24.7.3.3 struct flexio\_spi\_slave\_config\_t

##### Data Fields

- `bool enableSlave`

- **bool enableInDoze**  
*Enable/disable FlexIO SPI slave after configuration.*
- **bool enableInDebug**  
*Enable/disable FlexIO operation in doze mode.*
- **bool enableFastAccess**  
*Enable/disable FlexIO operation in debug mode.*
- **flexio\_spi\_clock\_phase\_t phase**  
*Enable/disable fast access to FlexIO registers,  
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*
- **flexio\_spi\_data\_bitcount\_mode\_t dataMode**  
*Clock phase.*
- **flexio\_spi\_data\_bitcount\_mode\_t dataMode**  
*8bit or 16bit mode.*

## Field Documentation

- (1) **bool flexio\_spi\_slave\_config\_t::enableSlave**
- (2) **bool flexio\_spi\_slave\_config\_t::enableInDoze**
- (3) **bool flexio\_spi\_slave\_config\_t::enableInDebug**
- (4) **bool flexio\_spi\_slave\_config\_t::enableFastAccess**
- (5) **flexio\_spi\_clock\_phase\_t flexio\_spi\_slave\_config\_t::phase**
- (6) **flexio\_spi\_data\_bitcount\_mode\_t flexio\_spi\_slave\_config\_t::dataMode**

### 24.7.3.4 struct flexio\_spi\_transfer\_t

#### Data Fields

- **uint8\_t \* txData**  
*Send buffer.*
- **uint8\_t \* rxData**  
*Receive buffer.*
- **size\_t dataSize**  
*Transfer bytes.*
- **uint8\_t flags**  
*FlexIO SPI control flag, MSB first or LSB first.*

## Field Documentation

- (1) `uint8_t* flexio_spi_transfer_t::txData`
- (2) `uint8_t* flexio_spi_transfer_t::rxData`
- (3) `size_t flexio_spi_transfer_t::dataSize`
- (4) `uint8_t flexio_spi_transfer_t::flags`

### 24.7.3.5 struct \_flexio\_spi\_master\_handle

typedef for `flexio_spi_master_handle_t` in advance.

## Data Fields

- `uint8_t * txData`  
*Transfer buffer.*
- `uint8_t * rxData`  
*Receive buffer.*
- `size_t transferSize`  
*Total bytes to be transferred.*
- `volatile size_t txRemainingBytes`  
*Send data remaining in bytes.*
- `volatile size_t rxRemainingBytes`  
*Receive data remaining in bytes.*
- `volatile uint32_t state`  
*FlexIO SPI internal state.*
- `uint8_t bytePerFrame`  
*SPI mode, 2bytes or 1byte in a frame.*
- `flexio_spi_shift_direction_t direction`  
*Shift direction.*
- `flexio_spi_master_transfer_callback_t callback`  
*FlexIO SPI callback.*
- `void * userData`  
*Callback parameter.*

## Field Documentation

- (1) `uint8_t* flexio_spi_master_handle_t::txData`
- (2) `uint8_t* flexio_spi_master_handle_t::rxData`
- (3) `size_t flexio_spi_master_handle_t::transferSize`
- (4) `volatile size_t flexio_spi_master_handle_t::txRemainingBytes`
- (5) `volatile size_t flexio_spi_master_handle_t::rxRemainingBytes`
- (6) `volatile uint32_t flexio_spi_master_handle_t::state`
- (7) `flexio_spi_shift_direction_t flexio_spi_master_handle_t::direction`
- (8) `flexio_spi_master_transfer_callback_t flexio_spi_master_handle_t::callback`
- (9) `void* flexio_spi_master_handle_t::userData`

## 24.7.4 Macro Definition Documentation

24.7.4.1 `#define FSL_FLEXIO_SPI_DRIVER_VERSION (MAKE_VERSION(2, 3, 2))`

24.7.4.2 `#define FLEXIO_SPI_DUMMYDATA (0x00U)`

24.7.4.3 `#define SPI_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`

24.7.4.4 `#define FLEXIO_SPI_XFER_DATA_FORMAT( flag ) ((flag) & (0x7U))`

## 24.7.5 Typedef Documentation

24.7.5.1 `typedef flexio_spi_master_handle_t flexio_spi_slave_handle_t`

## 24.7.6 Enumeration Type Documentation

### 24.7.6.1 anonymous enum

Enumerator

`kStatus_FLEXIO_SPI_Busy` FlexIO SPI is busy.

`kStatus_FLEXIO_SPI_Idle` SPI is idle.

`kStatus_FLEXIO_SPI_Error` FlexIO SPI error.

`kStatus_FLEXIO_SPI_Timeout` FlexIO SPI timeout polling status flags.

#### 24.7.6.2 enum flexio\_spi\_clock\_phase\_t

Enumerator

***kFLEXIO\_SPI\_ClockPhaseFirstEdge*** First edge on SPSCK occurs at the middle of the first cycle of a data transfer.

***kFLEXIO\_SPI\_ClockPhaseSecondEdge*** First edge on SPSCK occurs at the start of the first cycle of a data transfer.

#### 24.7.6.3 enum flexio\_spi\_shift\_direction\_t

Enumerator

***kFLEXIO\_SPI\_MsbFirst*** Data transfers start with most significant bit.

***kFLEXIO\_SPI\_LsbFirst*** Data transfers start with least significant bit.

#### 24.7.6.4 enum flexio\_spi\_data\_bitcount\_mode\_t

Enumerator

***kFLEXIO\_SPI\_8BitMode*** 8-bit data transmission mode.

***kFLEXIO\_SPI\_16BitMode*** 16-bit data transmission mode.

***kFLEXIO\_SPI\_32BitMode*** 32-bit data transmission mode.

#### 24.7.6.5 enum \_flexio\_spi\_interrupt\_enable

Enumerator

***kFLEXIO\_SPI\_TxEmptyInterruptEnable*** Transmit buffer empty interrupt enable.

***kFLEXIO\_SPI\_RxFullInterruptEnable*** Receive buffer full interrupt enable.

#### 24.7.6.6 enum \_flexio\_spi\_status\_flags

Enumerator

***kFLEXIO\_SPI\_TxBufferEmptyFlag*** Transmit buffer empty flag.

***kFLEXIO\_SPI\_RxBufferFullFlag*** Receive buffer full flag.

#### 24.7.6.7 enum \_flexio\_spi\_dma\_enable

Enumerator

- kFLEXIO\_SPI\_TxDmaEnable** Tx DMA request source.
- kFLEXIO\_SPI\_RxDmaEnable** Rx DMA request source.
- kFLEXIO\_SPI\_DmaAllEnable** All DMA request source.

#### 24.7.6.8 enum \_flexio\_spi\_transfer\_flags

Note

Use kFLEXIO\_SPI\_csContinuous and one of the other flags to OR together to form the transfer flag.

Enumerator

- kFLEXIO\_SPI\_8bitMsb** FlexIO SPI 8-bit MSB first.
- kFLEXIO\_SPI\_8bitLsb** FlexIO SPI 8-bit LSB first.
- kFLEXIO\_SPI\_16bitMsb** FlexIO SPI 16-bit MSB first.
- kFLEXIO\_SPI\_16bitLsb** FlexIO SPI 16-bit LSB first.
- kFLEXIO\_SPI\_32bitMsb** FlexIO SPI 32-bit MSB first.
- kFLEXIO\_SPI\_32bitLsb** FlexIO SPI 32-bit LSB first.
- kFLEXIO\_SPI\_csContinuous** Enable the CS signal continuous mode.

### 24.7.7 Function Documentation

#### 24.7.7.1 void FLEXIO\_SPI\_MasterInit ( FLEXIO\_SPI\_Type \* *base*,                                   flexio\_spi\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

The configuration structure can be filled by the user, or be set with default values by the [FLEXIO\\_SPI-MasterGetDefaultConfig\(\)](#).

Note

1.FlexIO SPI master only support CPOL = 0, which means clock inactive low. 2.For FlexIO SPI master, the input valid time is 1.5 clock cycles, for slave the output valid time is 2.5 clock cycles. So if FlexIO SPI master communicates with other spi IPs, the maximum baud rate is FlexIO clock frequency divided by  $2*2=4$ . If FlexIO SPI master communicates with FlexIO SPI slave, the maximum baud rate is FlexIO clock frequency divided by  $(1.5+2.5)*2=8$ .

#### Example

```
FLEXIO_SPI_Type spiDev = {
    .flexioBase = FLEXIO,
    .SDOPinIndex = 0,
    .SDIPinIndex = 1,
```

```

.SCKPinIndex = 2,
.CSnPinIndex = 3,
.shifterIndex = {0,1},
.timerIndex = {0,1}
};
flexio_spi_master_config_t config = {
.enableMaster = true,
.enableInDoze = false,
.enableInDebug = true,
.enableFastAccess = false,
.baudRate_Bps = 500000,
.phase = kFLEXIO_SPI_ClockPhaseFirstEdge,
.direction = kFLEXIO_SPI_MsbFirst,
.dataMode = kFLEXIO_SPI_8BitMode
};
FLEXIO_SPI_MasterInit(&spiDev, &config, srcClock_Hz);

```

#### Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>masterConfig</i>	Pointer to the <a href="#">flexio_spi_master_config_t</a> structure.
<i>srcClock_Hz</i>	FlexIO source clock in Hz.

#### 24.7.7.2 void FLEXIO\_SPI\_MasterDeinit ( [FLEXIO\\_SPI\\_Type](#) \* *base* )

#### Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> .
-------------	--

#### 24.7.7.3 void FLEXIO\_SPI\_MasterGetDefaultConfig ( [flexio\\_spi\\_master\\_config\\_t](#) \* *masterConfig* )

The configuration can be used directly by calling the [FLEXIO\\_SPI\\_MasterConfigure\(\)](#). Example:

```

flexio_spi_master_config_t masterConfig;
FLEXIO_SPI_MasterGetDefaultConfig(&masterConfig);

```

#### Parameters

<i>masterConfig</i>	Pointer to the <a href="#">flexio_spi_master_config_t</a> structure.
---------------------	--

#### 24.7.7.4 void FLEXIO\_SPI\_SlaveInit ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_slave\\_config\\_t](#) \* *slaveConfig* )

The configuration structure can be filled by the user, or be set with default values by the [FLEXIO\\_SPI\\_SlaveGetDefaultConfig\(\)](#).

## Note

1.Only one timer is needed in the FlexIO SPI slave. As a result, the second timer index is ignored. 2.- FlexIO SPI slave only support CPOL = 0, which means clock inactive low. 3.For FlexIO SPI master, the input valid time is 1.5 clock cycles, for slave the output valid time is 2.5 clock cycles. So if FlexIO SPI slave communicates with other spi IPs, the maximum baud rate is FlexIO clock frequency divided by  $3 \times 2 = 6$ . If FlexIO SPI slave communicates with FlexIO SPI master, the maximum baud rate is FlexIO clock frequency divided by  $(1.5 + 2.5) \times 2 = 8$ . Example

```
FLEXIO_SPI_Type spiDev = {
    .flexioBase = FLEXIO,
    .SDOPinIndex = 0,
    .SDIPinIndex = 1,
    .SCKPinIndex = 2,
    .CSnPinIndex = 3,
    .shifterIndex = {0,1},
    .timerIndex = {0}
};
flexio_spi_slave_config_t config = {
    .enableSlave = true,
    .enableInDoze = false,
    .enableInDebug = true,
    .enableFastAccess = false,
    .phase = kFLEXIO_SPI_ClockPhaseFirstEdge,
    .direction = kFLEXIO_SPI_MsbFirst,
    .dataMode = kFLEXIO_SPI_8BitMode
};
FLEXIO_SPI_SlaveInit(&spiDev, &config);
```

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>slaveConfig</i>	Pointer to the <a href="#">flexio_spi_slave_config_t</a> structure.

**24.7.7.5 void FLEXIO\_SPI\_SlaveDeinit ( FLEXIO\_SPI\_Type \* *base* )**

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> .
-------------	--

**24.7.7.6 void FLEXIO\_SPI\_SlaveGetDefaultConfig ( flexio\_spi\_slave\_config\_t \* *slaveConfig* )**

The configuration can be used directly for calling the [FLEXIO\\_SPI\\_SlaveConfigure\(\)](#). Example:

```
flexio_spi_slave_config_t slaveConfig;
FLEXIO_SPI_SlaveGetDefaultConfig(&slaveConfig);
```

Parameters

<i>slaveConfig</i>	Pointer to the <a href="#">flexio_spi_slave_config_t</a> structure.
--------------------	---

#### 24.7.7.7 `uint32_t FLEXIO_SPI_GetStatusFlags ( FLEXIO_SPI_Type * base )`

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
-------------	---

Returns

status flag; Use the status flag to AND the following flag mask and get the status.

- `kFLEXIO_SPI_TxEmptyFlag`
- `kFLEXIO_SPI_RxEmptyFlag`

#### 24.7.7.8 `void FLEXIO_SPI_ClearStatusFlags ( FLEXIO_SPI_Type * base, uint32_t mask )`

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>mask</i>	status flag The parameter can be any combination of the following values: <ul style="list-style-type: none"><li>• <code>kFLEXIO_SPI_TxEmptyFlag</code></li><li>• <code>kFLEXIO_SPI_RxEmptyFlag</code></li></ul>

#### 24.7.7.9 `void FLEXIO_SPI_EnableInterrupts ( FLEXIO_SPI_Type * base, uint32_t mask )`

This function enables the FlexIO SPI interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
-------------	---

<i>mask</i>	interrupt source. The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• kFLEXIO_SPI_RxFullInterruptEnable</li> <li>• kFLEXIO_SPI_TxEmptyInterruptEnable</li> </ul>
-------------	---

#### 24.7.7.10 void FLEXIO\_SPI\_DisableInterrupts ( FLEXIO\_SPI\_Type \* *base*, uint32\_t *mask* )

This function disables the FlexIO SPI interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>mask</i>	interrupt source The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• kFLEXIO_SPI_RxFullInterruptEnable</li> <li>• kFLEXIO_SPI_TxEmptyInterruptEnable</li> </ul>

#### 24.7.7.11 void FLEXIO\_SPI\_EnableDMA ( FLEXIO\_SPI\_Type \* *base*, uint32\_t *mask*, bool *enable* )

This function enables/disables the FlexIO SPI Tx DMA, which means that asserting the kFLEXIO\_SPI\_TxEmptyFlag does/doesn't trigger the DMA request.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>mask</i>	SPI DMA source.
<i>enable</i>	True means enable DMA, false means disable DMA.

#### 24.7.7.12 static uint32\_t FLEXIO\_SPI\_GetTxDataRegisterAddress ( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_shift\_direction\_t *direction* ) [inline], [static]

This function returns the SPI data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>direction</i>	Shift direction of MSB first or LSB first.

Returns

FlexIO SPI transmit data register address.

#### **24.7.7.13 static uint32\_t FLEXIO\_SPI\_GetRxDataRegisterAddress ( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_shift\_direction\_t *direction* ) [inline], [static]**

This function returns the SPI data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>direction</i>	Shift direction of MSB first or LSB first.

Returns

FlexIO SPI receive data register address.

#### **24.7.7.14 static void FLEXIO\_SPI\_Enable ( FLEXIO\_SPI\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> .
<i>enable</i>	True to enable, false does not have any effect.

#### **24.7.7.15 void FLEXIO\_SPI\_MasterSetBaudRate ( FLEXIO\_SPI\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClockHz* )**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>baudRate_Bps</i>	Baud Rate needed in Hz.
<i>srcClockHz</i>	SPI source clock frequency in Hz.

#### **24.7.7.16 static void FLEXIO\_SPI\_WriteData ( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_shift\_direction\_t *direction*, uint32\_t *data* ) [inline], [static]**

## Note

This is a non-blocking API, which returns directly after the data is put into the data register but the data transfer is not finished on the bus. Ensure that the TxEmptyFlag is asserted before calling this API.

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>direction</i>	Shift direction of MSB first or LSB first.
<i>data</i>	8/16/32 bit data.

#### 24.7.7.17 static uint32\_t FLEXIO\_SPI\_ReadData ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_shift\\_direction\\_t](#) *direction* ) [inline], [static]

## Note

This is a non-blocking API, which returns directly after the data is read from the data register. Ensure that the RxFullFlag is asserted before calling this API.

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>direction</i>	Shift direction of MSB first or LSB first.

## Returns

8 bit/16 bit data received.

#### 24.7.7.18 status\_t FLEXIO\_SPI\_WriteBlocking ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_shift\\_direction\\_t](#) *direction*, const [uint8\\_t](#) \* *buffer*, [size\\_t](#) *size* )

## Note

This function blocks using the polling method until all bytes have been sent.

## Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>direction</i>	Shift direction of MSB first or LSB first.
<i>buffer</i>	The data bytes to send.
<i>size</i>	The number of data bytes to send.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_FLEXIO_SPI_Timeout</i>	The transfer timed out and was aborted.

#### 24.7.7.19 status\_t FLEXIO\_SPI\_ReadBlocking ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_shift\\_direction\\_t](#) *direction*, [uint8\\_t](#) \* *buffer*, [size\\_t](#) *size* )

Note

This function blocks using the polling method until all bytes have been received.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>direction</i>	Shift direction of MSB first or LSB first.
<i>buffer</i>	The buffer to store the received bytes.
<i>size</i>	The number of data bytes to be received.
<i>direction</i>	Shift direction of MSB first or LSB first.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_FLEXIO_SPI_Timeout</i>	The transfer timed out and was aborted.

#### 24.7.7.20 status\_t FLEXIO\_SPI\_MasterTransferBlocking ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_transfer\\_t](#) \* *xfer* )

Note

This function blocks via polling until all bytes have been received.

Parameters

<i>base</i>	pointer to <a href="#">FLEXIO_SPI_Type</a> structure
<i>xfer</i>	FlexIO SPI transfer structure, see <a href="#">flexio_spi_transfer_t</a> .

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_FLEXIO_SPI_Timeout</i>	The transfer timed out and was aborted.

#### 24.7.7.21 void FLEXIO\_SPI\_FlushShifters ( [FLEXIO\\_SPI\\_Type](#) \* *base* )

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
-------------	---

#### 24.7.7.22 status\_t FLEXIO\_SPI\_MasterTransferCreateHandle ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_master\\_handle\\_t](#) \* *handle*, [flexio\\_spi\\_master\\_transfer\\_callback\\_t](#) *callback*, [void](#) \* *userData* )

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to the <a href="#">flexio_spi_master_handle_t</a> structure to store the transfer state.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

#### 24.7.7.23 status\_t FLEXIO\_SPI\_MasterTransferNonBlocking ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_master\\_handle\\_t](#) \* *handle*, [flexio\\_spi\\_transfer\\_t](#) \* *xfer* )

This function sends data using IRQ. This is a non-blocking function, which returns right away. When all data is sent out/received, the callback function is called.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_spi_master_handle_t</code> structure to store the transfer state.
<i>xfer</i>	FlexIO SPI transfer structure. See <a href="#">flexio_spi_transfer_t</a> .

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	SPI is not idle, is running another transfer.

**24.7.7.24 void FLEXIO\_SPI\_MasterTransferAbort ( `FLEXIO_SPI_Type * base,`  
`flexio_spi_master_handle_t * handle` )**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_spi_master_handle_t</code> structure to store the transfer state.

**24.7.7.25 status\_t FLEXIO\_SPI\_MasterTransferGetCount ( `FLEXIO_SPI_Type * base,`  
`flexio_spi_master_handle_t * handle, size_t * count` )**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_spi_master_handle_t</code> structure to store the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

**24.7.7.26 void FLEXIO\_SPI\_MasterTransferHandleIRQ ( `void * spiType, void * spiHandle`  
`)`**

Parameters

<i>spiType</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>spiHandle</i>	Pointer to the <a href="#">flexio_spi_master_handle_t</a> structure to store the transfer state.

**24.7.7.27 status\_t FLEXIO\_SPI\_SlaveTransferCreateHandle ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_slave\\_handle\\_t](#) \* *handle*, [flexio\\_spi\\_slave\\_transfer\\_callback\\_t](#) *callback*, [void](#) \* *userData* )**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to the <a href="#">flexio_spi_slave_handle_t</a> structure to store the transfer state.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

**24.7.7.28 status\_t FLEXIO\_SPI\_SlaveTransferNonBlocking ( [FLEXIO\\_SPI\\_Type](#) \* *base*, [flexio\\_spi\\_slave\\_handle\\_t](#) \* *handle*, [flexio\\_spi\\_transfer\\_t](#) \* *xfer* )**

This function sends data using IRQ. This is a non-blocking function, which returns right away. When all data is sent out/received, the callback function is called.

Parameters

<i>handle</i>	Pointer to the <a href="#">flexio_spi_slave_handle_t</a> structure to store the transfer state.
<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>xfer</i>	FlexIO SPI transfer structure. See <a href="#">flexio_spi_transfer_t</a> .

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	SPI is not idle; it is running another transfer.

24.7.7.29 **static void FLEXIO\_SPI\_SlaveTransferAbort( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_slave\_handle\_t \* *handle* ) [inline], [static]**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to the flexio_spi_slave_handle_t structure to store the transfer state.

**24.7.7.30 static status\_t FLEXIO\_SPI\_SlaveTransferGetCount ( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_slave\_handle\_t \* *handle*, size\_t \* *count* ) [inline], [static]**

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to the flexio_spi_slave_handle_t structure to store the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

**24.7.7.31 void FLEXIO\_SPI\_SlaveTransferHandleIRQ ( void \* *spiType*, void \* *spiHandle* )**

Parameters

<i>spiType</i>	Pointer to the <a href="#">FLEXIO_SPI_Type</a> structure.
<i>spiHandle</i>	Pointer to the flexio_spi_slave_handle_t structure to store the transfer state.

## 24.7.8 FlexIO eDMA SPI Driver

### 24.7.8.1 Overview

#### Data Structures

- struct `flexio_spi_master_edma_handle_t`

*FlexIO SPI eDMA transfer handle, users should not touch the content of the handle. [More...](#)*

#### TypeDefs

- typedef `flexio_spi_master_edma_handle_t flexio_spi_slave_edma_handle_t`  
*Slave handle is the same with master handle.*
- typedef void(\* `flexio_spi_master_edma_transfer_callback_t`)(`FLEXIO_SPI_Type` \*base, `flexio_spi_master_edma_handle_t` \*handle, `status_t` status, void \*userData)  
*FlexIO SPI master callback for finished transmit.*
- typedef void(\* `flexio_spi_slave_edma_transfer_callback_t`)(`FLEXIO_SPI_Type` \*base, `flexio_spi_slave_edma_handle_t` \*handle, `status_t` status, void \*userData)  
*FlexIO SPI slave callback for finished transmit.*

#### Driver version

- #define `FSL_FLEXIO_SPI_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))`  
*FlexIO SPI EDMA driver version.*

#### eDMA Transactional

- `status_t FLEXIO_SPI_MasterTransferCreateHandleEDMA (FLEXIO_SPI_Type *base, flexio_spi_master_edma_handle_t *handle, flexio_spi_master_edma_transfer_callback_t callback, void *userData, edma_handle_t *txHandle, edma_handle_t *rxHandle)`  
*Initializes the FlexIO SPI master eDMA handle.*
- `status_t FLEXIO_SPI_MasterTransferEDMA (FLEXIO_SPI_Type *base, flexio_spi_master_edma_handle_t *handle, flexio_spi_transfer_t *xfer)`  
*Performs a non-blocking FlexIO SPI transfer using eDMA.*
- `void FLEXIO_SPI_MasterTransferAbortEDMA (FLEXIO_SPI_Type *base, flexio_spi_master_edma_handle_t *handle)`  
*Aborts a FlexIO SPI transfer using eDMA.*
- `status_t FLEXIO_SPI_MasterTransferGetCountEDMA (FLEXIO_SPI_Type *base, flexio_spi_master_edma_handle_t *handle, size_t *count)`  
*Gets the number of bytes transferred so far using FlexIO SPI master eDMA.*
- static void `FLEXIO_SPI_SlaveTransferCreateHandleEDMA (FLEXIO_SPI_Type *base, flexio_spi_slave_edma_handle_t *handle, flexio_spi_slave_edma_transfer_callback_t callback, void *userData, edma_handle_t *txHandle, edma_handle_t *rxHandle)`  
*Initializes the FlexIO SPI slave eDMA handle.*

- `status_t FLEXIO_SPI_SlaveTransferEDMA (FLEXIO_SPI_Type *base, flexio_spi_slave_edma_handle_t *handle, flexio_spi_transfer_t *xfer)`  
`Performs a non-blocking FlexIO SPI transfer using eDMA.`
- `static void FLEXIO_SPI_SlaveTransferAbortEDMA (FLEXIO_SPI_Type *base, flexio_spi_slave_edma_handle_t *handle)`  
`Aborts a FlexIO SPI transfer using eDMA.`
- `static status_t FLEXIO_SPI_SlaveTransferGetCountEDMA (FLEXIO_SPI_Type *base, flexio_spi_slave_edma_handle_t *handle, size_t *count)`  
`Gets the number of bytes transferred so far using FlexIO SPI slave eDMA.`

## 24.7.8.2 Data Structure Documentation

### 24.7.8.2.1 struct \_flexio\_spi\_master\_edma\_handle

typedef for `flexio_spi_master_edma_handle_t` in advance.

#### Data Fields

- `size_t transferSize`  
`Total bytes to be transferred.`
- `uint8_t nbytes`  
`eDMA minor byte transfer count initially configured.`
- `bool txInProgress`  
`Send transfer in progress.`
- `bool rxInProgress`  
`Receive transfer in progress.`
- `edma_handle_t * txHandle`  
`DMA handler for SPI send.`
- `edma_handle_t * rxHandle`  
`DMA handler for SPI receive.`
- `flexio_spi_master_edma_transfer_callback_t callback`  
`Callback for SPI DMA transfer.`
- `void * userData`  
`User Data for SPI DMA callback.`

## Field Documentation

- (1) `size_t flexio_spi_master_edma_handle_t::transferSize`
- (2) `uint8_t flexio_spi_master_edma_handle_t::nbytes`

### 24.7.8.3 Macro Definition Documentation

**24.7.8.3.1 #define FSL\_FLEXIO\_SPI\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 3, 0))**

### 24.7.8.4 Typedef Documentation

**24.7.8.4.1 typedef flexio\_spi\_master\_edma\_handle\_t flexio\_spi\_slave\_edma\_handle\_t**

### 24.7.8.5 Function Documentation

**24.7.8.5.1 status\_t FLEXIO\_SPI\_MasterTransferCreateHandleEDMA ( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_master\_edma\_handle\_t \* *handle*, flexio\_spi\_master\_edma\_transfer\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *txHandle*, edma\_handle\_t \* *rxHandle* )**

This function initializes the FlexIO SPI master eDMA handle which can be used for other FlexIO SPI master transactional APIs. For a specified FlexIO SPI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to <code>flexio_spi_master_edma_handle_t</code> structure to store the transfer state.
<i>callback</i>	SPI callback, NULL means no callback.
<i>userData</i>	callback function parameter.
<i>txHandle</i>	User requested eDMA handle for FlexIO SPI RX eDMA transfer.
<i>rxHandle</i>	User requested eDMA handle for FlexIO SPI TX eDMA transfer.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO SPI eDMA type/handle table out of range.

**24.7.8.5.2 status\_t FLEXIO\_SPI\_MasterTransferEDMA ( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_master\_edma\_handle\_t \* *handle*, flexio\_spi\_transfer\_t \* *xfer* )**

## Note

This interface returns immediately after transfer initiates. Call FLEXIO\_SPI\_MasterGetTransferCountEDMA to poll the transfer status and check whether the FlexIO SPI transfer is finished.

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to <code>flexio_spi_master_edma_handle_t</code> structure to store the transfer state.
<i>xfer</i>	Pointer to FlexIO SPI transfer structure.

## Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	FlexIO SPI is not idle, is running another transfer.

#### 24.7.8.5.3 void FLEXIO\_SPI\_MasterTransferAbortEDMA ( `FLEXIO_SPI_Type * base,` `flexio_spi_master_edma_handle_t * handle` )

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	FlexIO SPI eDMA handle pointer.

#### 24.7.8.5.4 status\_t FLEXIO\_SPI\_MasterTransferGetCountEDMA ( `FLEXIO_SPI_Type * base,` `flexio_spi_master_edma_handle_t * handle, size_t * count` )

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	FlexIO SPI eDMA handle pointer.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

```
24.7.8.5.5 static void FLEXIO_SPI_SlaveTransferCreateHandleEDMA ( FLEXIO_SPI_Type * base,  
flexio_spi_slave_edma_handle_t * handle, flexio_spi_slave_edma_transfer_callback_t  
callback, void * userData, edma_handle_t * txHandle, edma_handle_t * rxHandle )  
[inline], [static]
```

This function initializes the FlexIO SPI slave eDMA handle.

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to <code>flexio_spi_slave_edma_handle_t</code> structure to store the transfer state.
<i>callback</i>	SPI callback, NULL means no callback.
<i>userData</i>	callback function parameter.
<i>txHandle</i>	User requested eDMA handle for FlexIO SPI TX eDMA transfer.
<i>rxHandle</i>	User requested eDMA handle for FlexIO SPI RX eDMA transfer.

**24.7.8.5.6 status\_t FLEXIO\_SPI\_SlaveTransferEDMA ( [FLEXIO\\_SPI\\_Type](#) \* *base*, `flexio_spi_slave_edma_handle_t` \* *handle*, `flexio_spi_transfer_t` \* *xfer* )**

## Note

This interface returns immediately after transfer initiates. Call `FLEXIO_SPI_SlaveGetTransferCountEDMA` to poll the transfer status and check whether the FlexIO SPI transfer is finished.

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to <code>flexio_spi_slave_edma_handle_t</code> structure to store the transfer state.
<i>xfer</i>	Pointer to FlexIO SPI transfer structure.

## Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	FlexIO SPI is not idle, is running another transfer.

**24.7.8.5.7 static void FLEXIO\_SPI\_SlaveTransferAbortEDMA ( [FLEXIO\\_SPI\\_Type](#) \* *base*, `flexio_spi_slave_edma_handle_t` \* *handle* ) [inline], [static]**

## Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	Pointer to <code>flexio_spi_slave_edma_handle_t</code> structure to store the transfer state.

**24.7.8.5.8 static status\_t FLEXIO\_SPI\_SlaveTransferGetCountEDMA ( FLEXIO\_SPI\_Type \* *base*, flexio\_spi\_slave\_edma\_handle\_t \* *handle*, size\_t \* *count* ) [inline], [static]**

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_SPI_Type</a> structure.
<i>handle</i>	FlexIO SPI eDMA handle pointer.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

## 24.8 FlexIO UART Driver

### 24.8.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Universal Asynchronous Receiver/Transmitter (UART) function using the Flexible I/O.

FlexIO UART driver includes functional APIs and transactional APIs. Functional APIs target low-level APIs. Functional APIs can be used for the FlexIO UART initialization/configuration/operation for optimization/customization purpose. Using the functional APIs requires the knowledge of the FlexIO UART peripheral and how to organize functional APIs to meet the application requirements. All functional API use the [FLEXIO\\_UART\\_Type](#) \* as the first parameter. FlexIO UART functional operation groups provide the functional APIs set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and also in the application if the code size and performance of transactional APIs satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the `flexio_uart_handle_t` as the second parameter. Initialize the handle by calling the [FLEXIO\\_UART\\_TransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions `FLEXIO_UART_SendNonBlocking()` and `FLEXIO_UART_ReceiveNonBlocking()` set up an interrupt for data transfer. When the transfer is complete, the upper layer is notified through a callback function with the `kStatus_FLEXIO_UART_TxIdle` and `kStatus_FLEXIO_UART_RxIdle` status.

Transactional receive APIs support the ring buffer. Prepare the memory for the ring buffer and pass in the start address and size through calling the `FLEXIO_UART_InstallRingBuffer()`. When the ring buffer is enabled, the received data is saved to the ring buffer in the background. The function `FLEXIO_UART_ReceiveNonBlocking()` first gets data from the ring buffer. If ring buffer does not have enough data, the function returns the data to the ring buffer and saves the received data to user memory. When all data is received, the upper layer is informed through a callback with the `kStatus_FLEXIO_UART_RxIdle` status.

If the receive ring buffer is full, the upper layer is informed through a callback with status `kStatus_FLEXIO_UART_RxRingBufferOverrun`. In the callback function, the upper layer reads data from the ring buffer. If not, the oldest data is overwritten by the new data.

The ring buffer size is specified when calling the `FLEXIO_UART_InstallRingBuffer`. Note that one byte is reserved for the ring buffer maintenance. Create a handle as follows.

```
FLEXIO_UART_InstallRingBuffer(&uartDev, &handle, &ringBuffer, 32);
```

In this example, the buffer size is 32. However, only 31 bytes are used for saving data.

### 24.8.2 Typical use case

#### 24.8.2.1 FlexIO UART send/receive using a polling method

```
uint8_t ch;
```

```

FLEXIO_UART_Type uartDev;
status_t result = kStatus_Success;
flexio_uart_user_config user_config;
FLEXIO_UART_GetDefaultConfig(&user_config);
user_config.baudRate_Bps = 115200U;
user_config.enableUart = true;

uartDev.flexioBase = BOARD_FLEXIO_BASE;
uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
uartDev.shifterIndex[0] = 0U;
uartDev.shifterIndex[1] = 1U;
uartDev.timerIndex[0] = 0U;
uartDev.timerIndex[1] = 1U;

result = FLEXIO_UART_Init(&uartDev, &user_config, 48000000U);
//Check if configuration is correct.
if(result != kStatus_Success)
{
    return;
}
FLEXIO_UART_WriteBlocking(&uartDev, txbuff, sizeof(txbuff));

while(1)
{
    FLEXIO_UART_ReadBlocking(&uartDev, &ch, 1);
    FLEXIO_UART_WriteBlocking(&uartDev, &ch, 1);
}

```

#### 24.8.2.2 FlexIO UART send/receive using an interrupt method

```

FLEXIO_UART_Type uartDev;
flexio_uart_handle_t g_uartHandle;
flexio_uart_config_t user_config;
flexio_uart_transfer_t sendXfer;
flexio_uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t sendData[] = ['H', 'e', 'l', 'l', 'o'];
uint8_t receiveData[32];

void FLEXIO_UART_UserCallback(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle,
    status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_UART_TxIdle == status)
    {
        txFinished = true;
    }

    if (kStatus_FLEXIO_UART_RxIdle == status)
    {
        rxFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableUart = true;
}

```

```

uartDev.flexioBase = BOARD_FLEXIO_BASE;
uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
uartDev.shifterIndex[0] = 0U;
uartDev.shifterIndex[1] = 1U;
uartDev.timerIndex[0] = 0U;
uartDev.timerIndex[1] = 1U;

result = FLEXIO_UART_Init(&uartDev, &user_config, 1200000000U);
//Check if configuration is correct.
if(result != kStatus_Success)
{
    return;
}

FLEXIO_UART_TransferCreateHandle(&uartDev, &g_uartHandle,
    FLEXIO_UART_UserCallback, NULL);

// Prepares to send.
sendXfer.data = sendData;
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_UART_SendNonBlocking(&uartDev, &g_uartHandle, &sendXfer);

// Send finished.
while (!txFinished)
{
}

// Prepares to receive.
receiveXfer.data = receiveData;
receiveXfer.dataSize = sizeof(receiveData)/sizeof(receiveData[0]);
rxFinished = false;

// Receives.
FLEXIO_UART_ReceiveNonBlocking(&uartDev, &g_uartHandle, &receiveXfer, NULL);

// Receive finished.
while (!rxFinished)
{
}

// ...
}

```

#### 24.8.2.3 FlexIO UART receive using the ringbuffer feature

```

#define RING_BUFFER_SIZE 64
#define RX_DATA_SIZE      32

FLEXIO_UART_Type uartDev;
flexio_uart_handle_t g_uartHandle;
flexio_uart_config_t user_config;
flexio_uart_transfer_t sendXfer;
flexio_uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t receiveData[RX_DATA_SIZE];
uint8_t ringBuffer[RING_BUFFER_SIZE];

void FLEXIO_UART_UserCallback(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle,
    status_t status, void *userData)
{

```

```

userData = userData;

if (kStatus_FLEXIO_UART_RxIdle == status)
{
    rxFinished = true;
}
}

void main(void)
{
    size_t bytesRead;
    //...

    FLEXIO_UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableUart = true;

    uartDev.flexioBase = BOARD_FLEXIO_BASE;
    uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
    uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
    uartDev.shifterIndex[0] = 0U;
    uartDev.shifterIndex[1] = 1U;
    uartDev.timerIndex[0] = 0U;
    uartDev.timerIndex[1] = 1U;

    result = FLEXIO_UART_Init(&uartDev, &user_config, 48000000U);
    //Check if configuration is correct.
    if(result != kStatus_Success)
    {
        return;
    }

    FLEXIO_UART_TransferCreateHandle(&uartDev, &g_uartHandle,
        FLEXIO_UART_UserCallback, NULL);
    FLEXIO_UART_InstallRingBuffer(&uartDev, &g_uartHandle, ringBuffer, RING_BUFFER_SIZE);

    // Receive is working in the background to the ring buffer.

    // Prepares to receive.
    receiveXfer.data = receiveData;
    receiveXfer.dataSize = RX_DATA_SIZE;
    rxFinished = false;

    // Receives.
    FLEXIO_UART_ReceiveNonBlocking(&uartDev, &g_uartHandle, &receiveXfer, &bytesRead);

    if (bytesRead == RX_DATA_SIZE) /* Have read enough data. */
    {
        ;
    }
    else
    {
        if (bytesRead) /* Received some data, process first. */
        {
            ;
        }

        // Receive finished.
        while (!rxFinished)
        {
        }
    }
}

// ...
}

```

#### 24.8.2.4 FlexIO UART send/receive using a DMA method

```

FLEXIO_UART_Type uartDev;
flexio_uart_handle_t g_uartHandle;
dma_handle_t g_uartTxDmaHandle;
dma_handle_t g_uartRxDmaHandle;
flexio_uart_config_t user_config;
flexio_uart_transfer_t sendXfer;
flexio_uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t sendData[] = {'H', 'e', 'l', 'l', 'o'};
uint8_t receiveData[32];

void FLEXIO_UART_UserCallback(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle,
    status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_UART_TxIdle == status)
    {
        txFinished = true;
    }

    if (kStatus_FLEXIO_UART_RxIdle == status)
    {
        rxFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableUart = true;

    uartDev.flexioBase = BOARD_FLEXIO_BASE;
    uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
    uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
    uartDev.shifterIndex[0] = 0U;
    uartDev.shifterIndex[1] = 1U;
    uartDev.timerIndex[0] = 0U;
    uartDev.timerIndex[1] = 1U;
    result = FLEXIO_UART_Init(&uartDev, &user_config, 48000000U);
    //Check if configuration is correct.
    if(result != kStatus_Success)
    {
        return;
    }

    /* Init DMAMUX. */
    DMAMUX_Init(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR);

    /* Init the DMA/EDMA module */
#if defined(FSL_FEATURE_SOC_DMA_COUNT) && FSL_FEATURE_SOC_DMA_COUNT > 0U
    DMA_Init(EXAMPLE_FLEXIO_UART_DMA_BASEADDR);
    DMA_CreateHandle(&g_uartTxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR, FLEXIO_UART_TX_DMA_CHANNEL);
    DMA_CreateHandle(&g_uartRxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR, FLEXIO_UART_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_DMA_COUNT */

#if defined(FSL_FEATURE_SOC_EDMA_COUNT) && FSL_FEATURE_SOC_EDMA_COUNT > 0U
    edma_config_t edmaConfig;

    EDMA_GetDefaultConfig(&edmaConfig);
    EDMA_Init(EXAMPLE_FLEXIO_UART_DMA_BASEADDR, &edmaConfig);

```

```

    EDMA_CreateHandle(&g_uartTxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR,
FLEXIO_UART_TX_DMA_CHANNEL);
    EDMA_CreateHandle(&g_uartRxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR,
FLEXIO_UART_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_EDMA_COUNT */

dma_request_source_tx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + uartDev.
shifterIndex[0]);
dma_request_source_rx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + uartDev.
shifterIndex[1]);

/* Requests DMA channels for transmit and receive. */
DMAMUX_SetSource(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR, FLEXIO_UART_TX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_tx);
DMAMUX_SetSource(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR, FLEXIO_UART_RX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_rx);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR,
FLEXIO_UART_TX_DMA_CHANNEL);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR,
FLEXIO_UART_RX_DMA_CHANNEL);

FLEXIO_UART_TransferCreateHandleDMA(&uartDev, &g_uartHandle, FLEXIO_UART_UserCallback, NULL, &
g_uartTxDmaHandle, &g_uartRxDmaHandle);

// Prepares to send.
sendXfer.data = sendData;
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_UART_SendDMA(&uartDev, &g_uartHandle, &sendXfer);

// Send finished.
while (!txFinished)
{
}

// Prepares to receive.
receiveXfer.data = receiveData;
receiveXfer.dataSize = sizeof(receiveData)/sizeof(receiveData[0]);
rxFinished = false;

// Receives.
FLEXIO_UART_ReceiveDMA(&uartDev, &g_uartHandle, &receiveXfer, NULL);

// Receive finished.
while (!rxFinished)
{
}

// ...
}

```

## Modules

- FlexIO eDMA UART Driver

## Data Structures

- struct **FLEXIO\_UART\_Type**  
*Define FlexIO UART access structure typedef.* [More...](#)

- struct `flexio_uart_config_t`  
*Define FlexIO UART user configuration structure. [More...](#)*
- struct `flexio_uart_transfer_t`  
*Define FlexIO UART transfer structure. [More...](#)*
- struct `flexio_uart_handle_t`  
*Define FLEXIO UART handle structure. [More...](#)*

## Macros

- #define `UART_RETRY_TIMES` 0U /\* Defining to zero means to keep waiting for the flag until it is assert/deassert. \*/  
*Retry times for waiting flag.*

## Typedefs

- typedef void(\* `flexio_uart_transfer_callback_t` )(FLEXIO\_UART\_Type \*base, flexio\_uart\_handle\_t \*handle, `status_t` status, void \*userData)  
*FlexIO UART transfer callback function.*

## Enumerations

- enum {
   
`kStatus_FLEXIO_UART_TxBusy` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_UART, 0),
   
`kStatus_FLEXIO_UART_RxBusy` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_UART, 1),
   
`kStatus_FLEXIO_UART_TxIdle` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_UART, 2),
   
`kStatus_FLEXIO_UART_RxIdle` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_UART, 3),
   
`kStatus_FLEXIO_UART_ERROR` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_UART, 4),
   
`kStatus_FLEXIO_UART_RxRingBufferOverrun`,
   
`kStatus_FLEXIO_UART_RxHardwareOverrun` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_UART, 6),
   
`kStatus_FLEXIO_UART_Timeout` = MAKE\_STATUS(kStatusGroup\_FLEXIO\_UART, 7),
   
`kStatus_FLEXIO_UART_BaudrateNotSupport` }
   
*Error codes for the UART driver.*
- enum `flexio_uart_bit_count_per_char_t` {
   
`kFLEXIO_UART_7BitsPerChar` = 7U,
   
`kFLEXIO_UART_8BitsPerChar` = 8U,
   
`kFLEXIO_UART_9BitsPerChar` = 9U }
   
*FlexIO UART bit count per char.*
- enum `_flexio_uart_interrupt_enable` {
   
`kFLEXIO_UART_TxDataRegEmptyInterruptEnable` = 0x1U,
   
`kFLEXIO_UART_RxDataRegFullInterruptEnable` = 0x2U }
   
*Define FlexIO UART interrupt mask.*
- enum `_flexio_uart_status_flags` {

```
kFLEXIO_UART_TxDataRegEmptyFlag = 0x1U,
kFLEXIO_UART_RxDataRegFullFlag = 0x2U,
kFLEXIO_UART_RxOverRunFlag = 0x4U }
```

*Define FlexIO UART status mask.*

## Driver version

- #define **FSL\_FLEXIO\_UART\_DRIVER\_VERSION** (MAKE\_VERSION(2, 4, 0))  
*FlexIO UART driver version.*

## Initialization and deinitialization

- **status\_t FLEXIO\_UART\_Init** (**FLEXIO\_UART\_Type** \*base, const **flexio\_uart\_config\_t** \*userConfig, **uint32\_t** srcClock\_Hz)  
*Ungates the FlexIO clock, resets the FlexIO module, configures FlexIO UART hardware, and configures the FlexIO UART with FlexIO UART configuration.*
- **void FLEXIO\_UART\_Deinit** (**FLEXIO\_UART\_Type** \*base)  
*Resets the FlexIO UART shifter and timer config.*
- **void FLEXIO\_UART\_GetDefaultConfig** (**flexio\_uart\_config\_t** \*userConfig)  
*Gets the default configuration to configure the FlexIO UART.*

## Status

- **uint32\_t FLEXIO\_UART\_GetStatusFlags** (**FLEXIO\_UART\_Type** \*base)  
*Gets the FlexIO UART status flags.*
- **void FLEXIO\_UART\_ClearStatusFlags** (**FLEXIO\_UART\_Type** \*base, **uint32\_t** mask)  
*Gets the FlexIO UART status flags.*

## Interrupts

- **void FLEXIO\_UART\_EnableInterrupts** (**FLEXIO\_UART\_Type** \*base, **uint32\_t** mask)  
*Enables the FlexIO UART interrupt.*
- **void FLEXIO\_UART\_DisableInterrupts** (**FLEXIO\_UART\_Type** \*base, **uint32\_t** mask)  
*Disables the FlexIO UART interrupt.*

## DMA Control

- **static uint32\_t FLEXIO\_UART\_GetTxDataRegisterAddress** (**FLEXIO\_UART\_Type** \*base)  
*Gets the FlexIO UART transmit data register address.*
- **static uint32\_t FLEXIO\_UART\_GetRxDataRegisterAddress** (**FLEXIO\_UART\_Type** \*base)  
*Gets the FlexIO UART receive data register address.*
- **static void FLEXIO\_UART\_EnableTxDMA** (**FLEXIO\_UART\_Type** \*base, **bool** enable)  
*Enables/disables the FlexIO UART transmit DMA.*
- **static void FLEXIO\_UART\_EnableRxDMA** (**FLEXIO\_UART\_Type** \*base, **bool** enable)

*Enables/disables the FlexIO UART receive DMA.*

## Bus Operations

- static void **FLEXIO\_UART\_Enable** (**FLEXIO\_UART\_Type** \*base, bool enable)  
*Enables/disables the FlexIO UART module operation.*
- static void **FLEXIO\_UART\_WriteByte** (**FLEXIO\_UART\_Type** \*base, const uint8\_t \*buffer)  
*Writes one byte of data.*
- static void **FLEXIO\_UART\_ReadByte** (**FLEXIO\_UART\_Type** \*base, uint8\_t \*buffer)  
*Reads one byte of data.*
- **status\_t FLEXIO\_UART\_WriteBlocking** (**FLEXIO\_UART\_Type** \*base, const uint8\_t \*txData, size\_t txSize)  
*Sends a buffer of data bytes.*
- **status\_t FLEXIO\_UART\_ReadBlocking** (**FLEXIO\_UART\_Type** \*base, uint8\_t \*rxData, size\_t rxSize)  
*Receives a buffer of bytes.*

## Transactional

- **status\_t FLEXIO\_UART\_TransferCreateHandle** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle, **flexio\_uart\_transfer\_callback\_t** callback, void \*userData)  
*Initializes the UART handle.*
- void **FLEXIO\_UART\_TransferStartRingBuffer** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle, uint8\_t \*ringBuffer, size\_t ringBufferSize)  
*Sets up the RX ring buffer.*
- void **FLEXIO\_UART\_TransferStopRingBuffer** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle)  
*Aborts the background transfer and uninstalls the ring buffer.*
- **status\_t FLEXIO\_UART\_TransferSendNonBlocking** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle, **flexio\_uart\_transfer\_t** \*xfer)  
*Transmits a buffer of data using the interrupt method.*
- void **FLEXIO\_UART\_TransferAbortSend** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle)  
*Aborts the interrupt-driven data transmit.*
- **status\_t FLEXIO\_UART\_TransferGetSendCount** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle, size\_t \*count)  
*Gets the number of bytes sent.*
- **status\_t FLEXIO\_UART\_TransferReceiveNonBlocking** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle, **flexio\_uart\_transfer\_t** \*xfer, size\_t \*receivedBytes)  
*Receives a buffer of data using the interrupt method.*
- void **FLEXIO\_UART\_TransferAbortReceive** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle)  
*Aborts the receive data which was using IRQ.*
- **status\_t FLEXIO\_UART\_TransferGetReceiveCount** (**FLEXIO\_UART\_Type** \*base, flexio\_uart\_handle\_t \*handle, size\_t \*count)  
*Gets the number of bytes received.*
- void **FLEXIO\_UART\_TransferHandleIRQ** (void \*uartType, void \*uartHandle)

*FlexIO UART IRQ handler function.*

## 24.8.3 Data Structure Documentation

### 24.8.3.1 struct FLEXIO\_UART\_Type

#### Data Fields

- `FLEXIO_Type * flexioBase`  
*FlexIO base pointer.*
- `uint8_t TxPinIndex`  
*Pin select for UART\_Tx.*
- `uint8_t RxPinIndex`  
*Pin select for UART\_Rx.*
- `uint8_t shifterIndex [2]`  
*Shifter index used in FlexIO UART.*
- `uint8_t timerIndex [2]`  
*Timer index used in FlexIO UART.*

#### Field Documentation

- (1) `FLEXIO_Type* FLEXIO_UART_Type::flexioBase`
- (2) `uint8_t FLEXIO_UART_Type::TxPinIndex`
- (3) `uint8_t FLEXIO_UART_Type::RxPinIndex`
- (4) `uint8_t FLEXIO_UART_Type::shifterIndex[2]`
- (5) `uint8_t FLEXIO_UART_Type::timerIndex[2]`

### 24.8.3.2 struct flexio\_uart\_config\_t

#### Data Fields

- `bool enableUart`  
*Enable/disable FlexIO UART TX & RX.*
- `bool enableInDoze`  
*Enable/disable FlexIO operation in doze mode.*
- `bool enableInDebug`  
*Enable/disable FlexIO operation in debug mode.*
- `bool enableFastAccess`  
*Enable/disable fast access to FlexIO registers,  
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*
- `uint32_t baudRate_Bps`  
*Baud rate in Bps.*
- `flexio_uart_bit_count_per_char_t bitCountPerChar`  
*number of bits, 7/8/9 -bit*

**Field Documentation**

- (1) **bool flexio\_uart\_config\_t::enableUart**
- (2) **bool flexio\_uart\_config\_t::enableFastAccess**
- (3) **uint32\_t flexio\_uart\_config\_t::baudRate\_Bps**

**24.8.3.3 struct flexio\_uart\_transfer\_t****Data Fields**

- **size\_t dataSize**  
*Transfer size.*
- **uint8\_t \* data**  
*The buffer of data to be transfer.*
- **uint8\_t \* rxData**  
*The buffer to receive data.*
- **const uint8\_t \* txData**  
*The buffer of data to be sent.*

**Field Documentation**

- (1) **uint8\_t\* flexio\_uart\_transfer\_t::data**
- (2) **uint8\_t\* flexio\_uart\_transfer\_t::rxData**
- (3) **const uint8\_t\* flexio\_uart\_transfer\_t::txData**

**24.8.3.4 struct \_flexio\_uart\_handle****Data Fields**

- **const uint8\_t \*volatile txData**  
*Address of remaining data to send.*
- **volatile size\_t txDataSize**  
*Size of the remaining data to send.*
- **uint8\_t \*volatile rxData**  
*Address of remaining data to receive.*
- **volatile size\_t rxDataSize**  
*Size of the remaining data to receive.*
- **size\_t txDataSizeAll**  
*Total bytes to be sent.*
- **size\_t rxDataSizeAll**  
*Total bytes to be received.*
- **uint8\_t \* rxRingBuffer**  
*Start address of the receiver ring buffer.*
- **size\_t rxRingBufferSize**  
*Size of the ring buffer.*
- **volatile uint16\_t rxRingBufferHead**  
*Index for the driver to store received data into ring buffer.*

- volatile uint16\_t **rxRingBufferTail**  
*Index for the user to get data from the ring buffer.*
- **flexio\_uart\_transfer\_callback\_t callback**  
*Callback function.*
- void \* **userData**  
*UART callback function parameter.*
- volatile uint8\_t **txState**  
*TX transfer state.*
- volatile uint8\_t **rxState**  
*RX transfer state.*

## Field Documentation

- (1) `const uint8_t* volatile flexio_uart_handle_t::txData`
- (2) `volatile size_t flexio_uart_handle_t::txDataSize`
- (3) `uint8_t* volatile flexio_uart_handle_t::rxData`
- (4) `volatile size_t flexio_uart_handle_t::rxDataSize`
- (5) `size_t flexio_uart_handle_t::txDataSizeAll`
- (6) `size_t flexio_uart_handle_t::rxDataSizeAll`
- (7) `uint8_t* flexio_uart_handle_t::rxRingBuffer`
- (8) `size_t flexio_uart_handle_t::rxRingBufferSize`
- (9) `volatile uint16_t flexio_uart_handle_t::rxRingBufferHead`
- (10) `volatile uint16_t flexio_uart_handle_t::rxRingBufferTail`
- (11) `flexio_uart_transfer_callback_t flexio_uart_handle_t::callback`
- (12) `void* flexio_uart_handle_t::userData`
- (13) `volatile uint8_t flexio_uart_handle_t::txState`

### 24.8.4 Macro Definition Documentation

24.8.4.1 `#define FSL_FLEXIO_UART_DRIVER_VERSION (MAKE_VERSION(2, 4, 0))`

24.8.4.2 `#define UART_RETRY_TIMES 0U /* Defining to zero means to keep waiting for the flag until it is assert/deassert. */`

### 24.8.5 Typedef Documentation

24.8.5.1 `typedef void(* flexio_uart_transfer_callback_t)(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle, status_t status, void *userData)`

### 24.8.6 Enumeration Type Documentation

#### 24.8.6.1 anonymous enum

Enumerator

`kStatus_FLEXIO_UART_TxBusy` Transmitter is busy.

`kStatus_FLEXIO_UART_RxBusy` Receiver is busy.

*kStatus\_FLEXIO\_UART\_TxIdle* UART transmitter is idle.  
*kStatus\_FLEXIO\_UART\_RxIdle* UART receiver is idle.  
*kStatus\_FLEXIO\_UART\_Error* ERROR happens on UART.  
*kStatus\_FLEXIO\_UART\_RxRingBufferOverrun* UART RX software ring buffer overrun.  
*kStatus\_FLEXIO\_UART\_RxHardwareOverrun* UART RX receiver overrun.  
*kStatus\_FLEXIO\_UART\_Timeout* UART times out.  
*kStatus\_FLEXIO\_UART\_BaudrateNotSupport* Baudrate is not supported in current clock source.

#### 24.8.6.2 enum flexio\_uart\_bit\_count\_per\_char\_t

Enumerator

*kFLEXIO\_UART\_7BitsPerChar* 7-bit data characters  
*kFLEXIO\_UART\_8BitsPerChar* 8-bit data characters  
*kFLEXIO\_UART\_9BitsPerChar* 9-bit data characters

#### 24.8.6.3 enum \_flexio\_uart\_interrupt\_enable

Enumerator

*kFLEXIO\_UART\_TxDataRegEmptyInterruptEnable* Transmit buffer empty interrupt enable.  
*kFLEXIO\_UART\_RxDataRegFullInterruptEnable* Receive buffer full interrupt enable.

#### 24.8.6.4 enum \_flexio\_uart\_status\_flags

Enumerator

*kFLEXIO\_UART\_TxDataRegEmptyFlag* Transmit buffer empty flag.  
*kFLEXIO\_UART\_RxDataRegFullFlag* Receive buffer full flag.  
*kFLEXIO\_UART\_RxOverRunFlag* Receive buffer over run flag.

### 24.8.7 Function Documentation

#### 24.8.7.1 status\_t FLEXIO\_UART\_Init ( FLEXIO\_UART\_Type \* base, const flexio\_uart\_config\_t \* userConfig, uint32\_t srcClock\_Hz )

The configuration structure can be filled by the user or be set with default values by [FLEXIO\\_UART\\_GetDefaultConfig\(\)](#).

Example

```

FLEXIO_UART_Type base = {
    .flexioBase = FLEXIO,
    .TxPinIndex = 0,
    .RxPinIndex = 1,
    .shifterIndex = {0,1},
    .timerIndex = {0,1}
};
flexio_uart_config_t config = {
    .enableInDoze = false,
    .enableInDebug = true,
    .enableFastAccess = false,
    .baudRate_Bps = 115200U,
    .bitCountPerChar = 8
};
FLEXIO_UART_Init(base, &config, srcClock_Hz);

```

#### Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>userConfig</i>	Pointer to the <a href="#">flexio_uart_config_t</a> structure.
<i>srcClock_Hz</i>	FlexIO source clock in Hz.

#### Return values

<i>kStatus_Success</i>	Configuration success.
<i>kStatus_FLEXIO_UART_BaudrateNotSupport</i>	Baudrate is not supported for current clock source frequency.

### 24.8.7.2 void [FLEXIO\\_UART\\_Deinit](#)( [FLEXIO\\_UART\\_Type](#) \* *base* )

#### Note

After calling this API, call the [FLEXIO\\_UART\\_Init](#) to use the FlexIO UART module.

#### Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a> structure
-------------	---

### 24.8.7.3 void [FLEXIO\\_UART\\_GetDefaultConfig](#)( [flexio\\_uart\\_config\\_t](#) \* *userConfig* )

The configuration can be used directly for calling the [FLEXIO\\_UART\\_Init\(\)](#). Example:

```

flexio_uart_config_t config;
FLEXIO_UART_GetDefaultConfig(&userConfig);

```

Parameters

<i>userConfig</i>	Pointer to the <a href="#">flexio_uart_config_t</a> structure.
-------------------	--

#### 24.8.7.4 `uint32_t FLEXIO_UART_GetStatusFlags ( FLEXIO_UART_Type * base )`

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
-------------	--

Returns

FlexIO UART status flags.

#### 24.8.7.5 `void FLEXIO_UART_ClearStatusFlags ( FLEXIO_UART_Type * base, uint32_t mask )`

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>mask</i>	Status flag. The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• <code>kFLEXIO_UART_TxDataRegEmptyFlag</code></li> <li>• <code>kFLEXIO_UART_RxEmptyFlag</code></li> <li>• <code>kFLEXIO_UART_RxOverRunFlag</code></li> </ul>

#### 24.8.7.6 `void FLEXIO_UART_EnableInterrupts ( FLEXIO_UART_Type * base, uint32_t mask )`

This function enables the FlexIO UART interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>mask</i>	Interrupt source.

#### 24.8.7.7 `void FLEXIO_UART_DisableInterrupts ( FLEXIO_UART_Type * base, uint32_t mask )`

This function disables the FlexIO UART interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>mask</i>	Interrupt source.

#### 24.8.7.8 static uint32\_t FLEXIO\_UART\_GetTxDataRegisterAddress ( FLEXIO\_UART\_Type \* *base* ) [inline], [static]

This function returns the UART data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
-------------	--

Returns

FlexIO UART transmit data register address.

#### 24.8.7.9 static uint32\_t FLEXIO\_UART\_GetRxDataRegisterAddress ( FLEXIO\_UART\_Type \* *base* ) [inline], [static]

This function returns the UART data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
-------------	--

Returns

FlexIO UART receive data register address.

#### 24.8.7.10 static void FLEXIO\_UART\_EnableTxDMA ( [FLEXIO\\_UART\\_Type](#) \* *base*, bool *enable* ) [inline], [static]

This function enables/disables the FlexIO UART Tx DMA, which means asserting the kFLEXIO\_UART\_TxDataRegEmptyFlag does/doesn't trigger the DMA request.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>enable</i>	True to enable, false to disable.

#### 24.8.7.11 static void FLEXIO\_UART\_EnableRxDMA ( [FLEXIO\\_UART\\_Type](#) \* *base*, *bool enable* ) [inline], [static]

This function enables/disables the FlexIO UART Rx DMA, which means asserting kFLEXIO\_UART\_RxDataRegFullFlag does/doesn't trigger the DMA request.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>enable</i>	True to enable, false to disable.

#### 24.8.7.12 static void FLEXIO\_UART\_Enable ( [FLEXIO\\_UART\\_Type](#) \* *base*, *bool enable* ) [inline], [static]

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> .
<i>enable</i>	True to enable, false does not have any effect.

#### 24.8.7.13 static void FLEXIO\_UART\_WriteByte ( [FLEXIO\\_UART\\_Type](#) \* *base*, *const uint8\_t* \* *buffer* ) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is put into the data register. Ensure that the TxEmptyFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
-------------	--

<i>buffer</i>	The data bytes to send.
---------------	-------------------------

#### 24.8.7.14 static void FLEXIO\_UART\_ReadByte ( FLEXIO\_UART\_Type \* *base*, uint8\_t \* *buffer* ) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is read from the data register. Ensure that the RxFullFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>buffer</i>	The buffer to store the received bytes.

#### 24.8.7.15 status\_t FLEXIO\_UART\_WriteBlocking ( FLEXIO\_UART\_Type \* *base*, const uint8\_t \* *txData*, size\_t *txSize* )

Note

This function blocks using the polling method until all bytes have been sent.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>txData</i>	The data bytes to send.
<i>txSize</i>	The number of data bytes to send.

Return values

<i>kStatus_FLEXIO_UART_Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully wrote all data.

#### 24.8.7.16 status\_t FLEXIO\_UART\_ReadBlocking ( FLEXIO\_UART\_Type \* *base*, uint8\_t \* *rxData*, size\_t *rxSize* )

Note

This function blocks using the polling method until all bytes have been received.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>rxData</i>	The buffer to store the received bytes.
<i>rxSize</i>	The number of data bytes to be received.

Return values

<i>kStatus_FLEXIO_UART_Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully received all data.

**24.8.7.17 status\_t FLEXIO\_UART\_TransferCreateHandle ( [FLEXIO\\_UART\\_Type](#) \* *base*, [flexio\\_uart\\_handle\\_t](#) \* *handle*, [flexio\\_uart\\_transfer\\_callback\\_t](#) *callback*, [void](#) \* *userData* )**

This function initializes the FlexIO UART handle, which can be used for other FlexIO UART transactional APIs. Call this API once to get the initialized handle.

The UART driver supports the "background" receiving, which means that users can set up a RX ring buffer optionally. Data received is stored into the ring buffer even when the user doesn't call the [FLEXIO\\_UART\\_TransferReceiveNonBlocking\(\)](#) API. If there is already data received in the ring buffer, users can get the received data from the ring buffer directly. The ring buffer is disabled if passing NULL as *ringBuffer*.

Parameters

<i>base</i>	to <a href="#">FLEXIO_UART_Type</a> structure.
<i>handle</i>	Pointer to the <a href="#">flexio_uart_handle_t</a> structure to store the transfer state.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

**24.8.7.18 void FLEXIO\_UART\_TransferStartRingBuffer ( [FLEXIO\\_UART\\_Type](#) \* *base*, [flexio\\_uart\\_handle\\_t](#) \* *handle*, [uint8\\_t](#) \* *ringBuffer*, [size\\_t](#) *ringBufferSize* )**

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received is stored into the ring buffer even when the user doesn't

call the `UART_ReceiveNonBlocking()` API. If there is already data received in the ring buffer, users can get the received data from the ring buffer directly.

#### Note

When using the RX ring buffer, one byte is reserved for internal use. In other words, if `ringBufferSize` is 32, only 31 bytes are used for saving data.

#### Parameters

<i>base</i>	Pointer to the <code>FLEXIO_UART_Type</code> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.
<i>ringBuffer</i>	Start address of ring buffer for background receiving. Pass NULL to disable the ring buffer.
<i>ringBufferSize</i>	Size of the ring buffer.

### 24.8.7.19 void FLEXIO\_UART\_TransferStopRingBuffer ( `FLEXIO_UART_Type * base,` `flexio_uart_handle_t * handle` )

This function aborts the background transfer and uninstalls the ring buffer.

#### Parameters

<i>base</i>	Pointer to the <code>FLEXIO_UART_Type</code> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.

### 24.8.7.20 status\_t FLEXIO\_UART\_TransferSendNonBlocking ( `FLEXIO_UART_Type * base,` `flexio_uart_handle_t * handle,` `flexio_uart_transfer_t * xfer` )

This function sends data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data to be written to the TX register. When all data is written to the TX register in ISR, the FlexIO UART driver calls the callback function and passes the `kStatus_FLEXIO_UART_TxIdle` as status parameter.

#### Note

The `kStatus_FLEXIO_UART_TxIdle` is passed to the upper layer when all data is written to the TX register. However, it does not ensure that all data is sent out.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.
<i>xfer</i>	FlexIO UART transfer structure. See <a href="#">flexio_uart_transfer_t</a> .

Return values

<i>kStatus_Success</i>	Successfully starts the data transmission.
<i>kStatus_UART_TxBusy</i>	Previous transmission still not finished, data not written to the TX register.

#### 24.8.7.21 void FLEXIO\_UART\_TransferAbortSend ( `FLEXIO_UART_Type * base`, `flexio_uart_handle_t * handle` )

This function aborts the interrupt-driven data sending. Get the `remainBytes` to find out how many bytes are still not sent out.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.

#### 24.8.7.22 `status_t FLEXIO_UART_TransferGetSendCount ( FLEXIO_UART_Type * base, flexio_uart_handle_t * handle, size_t * count )`

This function gets the number of bytes sent driven by interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.
<i>count</i>	Number of bytes sent so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferInProgress</i>	transfer has finished or no transfer in progress.
-------------------------------------	---

<i>kStatus_Success</i>	Successfully return the count.
------------------------	--------------------------------

#### 24.8.7.23 **status\_t FLEXIO\_UART\_TransferReceiveNonBlocking ( FLEXIO\_UART\_Type \* *base*, flexio\_uart\_handle\_t \* *handle*, flexio\_uart\_transfer\_t \* *xfer*, size\_t \* *receivedBytes* )**

This function receives data using the interrupt method. This is a non-blocking function, which returns without waiting for all data to be received. If the RX ring buffer is used and not empty, the data in ring buffer is copied and the parameter *receivedBytes* shows how many bytes are copied from the ring buffer. After copying, if the data in ring buffer is not enough to read, the receive request is saved by the UART driver. When new data arrives, the receive request is serviced first. When all data is received, the UART driver notifies the upper layer through a callback function and passes the status parameter *kStatus\_UART\_RxIdle*. For example, if the upper layer needs 10 bytes but there are only 5 bytes in the ring buffer, the 5 bytes are copied to *xfer->data*. This function returns with the parameter *receivedBytes* set to 5. For the last 5 bytes, newly arrived data is saved from the *xfer->data[5]*. When 5 bytes are received, the UART driver notifies upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to *xfer->data*. When all data is received, the upper layer is notified.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>handle</i>	Pointer to the <a href="#">flexio_uart_handle_t</a> structure to store the transfer state.
<i>xfer</i>	UART transfer structure. See <a href="#">flexio_uart_transfer_t</a> .
<i>receivedBytes</i>	Bytes received from the ring buffer directly.

Return values

<i>kStatus_Success</i>	Successfully queue the transfer into the transmit queue.
<i>kStatus_FLEXIO_UART_RxBusy</i>	Previous receive request is not finished.

#### 24.8.7.24 **void FLEXIO\_UART\_TransferAbortReceive ( FLEXIO\_UART\_Type \* *base*, flexio\_uart\_handle\_t \* *handle* )**

This function aborts the receive data which was using IRQ.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.

#### 24.8.7.25 `status_t FLEXIO_UART_TransferGetReceiveCount ( FLEXIO_UART_Type * base, flexio_uart_handle_t * handle, size_t * count )`

This function gets the number of bytes received driven by interrupt.

Parameters

<i>base</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.
<i>count</i>	Number of bytes received so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferInProgress</i>	transfer has finished or no transfer in progress.
<i>kStatus_Success</i>	Successfully return the count.

#### 24.8.7.26 `void FLEXIO_UART_TransferHandleIRQ ( void * uartType, void * uartHandle )`

This function processes the FlexIO UART transmit and receives the IRQ request.

Parameters

<i>uartType</i>	Pointer to the <a href="#">FLEXIO_UART_Type</a> structure.
<i>uartHandle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.

## 24.8.8 FlexIO eDMA UART Driver

### 24.8.8.1 Overview

#### Data Structures

- struct `flexio_uart_edma_handle_t`  
*UART eDMA handle.* [More...](#)

#### TypeDefs

- typedef void(\* `flexio_uart_edma_transfer_callback_t`)(`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle, `status_t` status, void \*userData)  
*UART transfer callback function.*

#### Driver version

- #define `FSL_FLEXIO_UART_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 4, 1)`)  
*FlexIO UART EDMA driver version.*

#### eDMA transactional

- `status_t FLEXIO_UART_TransferCreateHandleEDMA` (`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle, `flexio_uart_edma_transfer_callback_t` callback, void \*userData, `edma_handle_t` \*txEdmaHandle, `edma_handle_t` \*rxEdmaHandle)  
*Initializes the UART handle which is used in transactional functions.*
- `status_t FLEXIO_UART_TransferSendEDMA` (`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle, `flexio_uart_transfer_t` \*xfer)  
*Sends data using eDMA.*
- `status_t FLEXIO_UART_TransferReceiveEDMA` (`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle, `flexio_uart_transfer_t` \*xfer)  
*Receives data using eDMA.*
- `void FLEXIO_UART_TransferAbortSendEDMA` (`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle)  
*Aborts the sent data which using eDMA.*
- `void FLEXIO_UART_TransferAbortReceiveEDMA` (`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle)  
*Aborts the receive data which using eDMA.*
- `status_t FLEXIO_UART_TransferGetSendCountEDMA` (`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle, `size_t` \*count)  
*Gets the number of bytes sent out.*
- `status_t FLEXIO_UART_TransferGetReceiveCountEDMA` (`FLEXIO_UART_Type` \*base, `flexio_uart_edma_handle_t` \*handle, `size_t` \*count)  
*Gets the number of bytes received.*

### 24.8.8.2 Data Structure Documentation

#### 24.8.8.2.1 struct \_flexio\_uart\_edma\_handle

##### Data Fields

- `flexio_uart_edma_transfer_callback_t callback`  
*Callback function.*
- `void *userData`  
*UART callback function parameter.*
- `size_t txDataSizeAll`  
*Total bytes to be sent.*
- `size_t rxDataSizeAll`  
*Total bytes to be received.*
- `edma_handle_t *txEdmaHandle`  
*The eDMA TX channel used.*
- `edma_handle_t *rxEdmaHandle`  
*The eDMA RX channel used.*
- `uint8_t nbytes`  
*eDMA minor byte transfer count initially configured.*
- `volatile uint8_t txState`  
*TX transfer state.*
- `volatile uint8_t rxState`  
*RX transfer state.*

## Field Documentation

- (1) `flexio_uart_edma_transfer_callback_t flexio_uart_edma_handle_t::callback`
- (2) `void* flexio_uart_edma_handle_t::userData`
- (3) `size_t flexio_uart_edma_handle_t::txDataSizeAll`
- (4) `size_t flexio_uart_edma_handle_t::rxDataSizeAll`
- (5) `edma_handle_t* flexio_uart_edma_handle_t::txEdmaHandle`
- (6) `edma_handle_t* flexio_uart_edma_handle_t::rxEdmaHandle`
- (7) `uint8_t flexio_uart_edma_handle_t::nbytes`
- (8) `volatile uint8_t flexio_uart_edma_handle_t::txState`

### 24.8.8.3 Macro Definition Documentation

24.8.8.3.1 `#define FSL_FLEXIO_UART_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 4, 1))`

### 24.8.8.4 Typedef Documentation

24.8.8.4.1 `typedef void(* flexio_uart_edma_transfer_callback_t)(FLEXIO_UART_Type *base, flexio_uart_edma_handle_t *handle, status_t status, void *userData)`

### 24.8.8.5 Function Documentation

24.8.8.5.1 `status_t FLEXIO_UART_TransferCreateHandleEDMA ( FLEXIO_UART_Type * base, flexio_uart_edma_handle_t * handle, flexio_uart_edma_transfer_callback_t callback, void * userData, edma_handle_t * txEdmaHandle, edma_handle_t * rxEdmaHandle )`

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a> .
<i>handle</i>	Pointer to <a href="#">flexio_uart_edma_handle_t</a> structure.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.
<i>rxEdmaHandle</i>	User requested DMA handle for RX DMA transfer.
<i>txEdmaHandle</i>	User requested DMA handle for TX DMA transfer.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO SPI eDMA type/handle table out of range.

#### 24.8.8.5.2 status\_t [FLEXIO\\_UART\\_TransferSendEDMA](#) ( [FLEXIO\\_UART\\_Type](#) \* *base*, [flexio\\_uart\\_edma\\_handle\\_t](#) \* *handle*, [flexio\\_uart\\_transfer\\_t](#) \* *xfer* )

This function sends data using eDMA. This is a non-blocking function, which returns right away. When all data is sent out, the send callback function is called.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a>
<i>handle</i>	UART handle pointer.
<i>xfer</i>	UART eDMA transfer structure, see <a href="#">flexio_uart_transfer_t</a> .

Return values

<i>kStatus_Success</i>	if succeed, others failed.
<i>kStatus_FLEXIO_UART_TxBusy</i>	Previous transfer on going.

#### 24.8.8.5.3 status\_t [FLEXIO\\_UART\\_TransferReceiveEDMA](#) ( [FLEXIO\\_UART\\_Type](#) \* *base*, [flexio\\_uart\\_edma\\_handle\\_t](#) \* *handle*, [flexio\\_uart\\_transfer\\_t](#) \* *xfer* )

This function receives data using eDMA. This is a non-blocking function, which returns right away. When all data is received, the receive callback function is called.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a>
<i>handle</i>	Pointer to <code>flexio_uart_edma_handle_t</code> structure
<i>xfer</i>	UART eDMA transfer structure, see <a href="#">flexio_uart_transfer_t</a> .

Return values

<i>kStatus_Success</i>	if succeed, others failed.
<i>kStatus_UART_RxBusy</i>	Previous transfer on going.

#### 24.8.8.5.4 void FLEXIO\_UART\_TransferAbortSendEDMA ( `FLEXIO_UART_Type * base,` `flexio_uart_edma_handle_t * handle` )

This function aborts sent data which using eDMA.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a>
<i>handle</i>	Pointer to <code>flexio_uart_edma_handle_t</code> structure

#### 24.8.8.5.5 void FLEXIO\_UART\_TransferAbortReceiveEDMA ( `FLEXIO_UART_Type * base,` `flexio_uart_edma_handle_t * handle` )

This function aborts the receive data which using eDMA.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a>
<i>handle</i>	Pointer to <code>flexio_uart_edma_handle_t</code> structure

#### 24.8.8.5.6 status\_t FLEXIO\_UART\_TransferGetSendCountEDMA ( `FLEXIO_UART_Type * base,` `flexio_uart_edma_handle_t * handle, size_t * count` )

This function gets the number of bytes sent out.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a>
<i>handle</i>	Pointer to <code>flexio_uart_edma_handle_t</code> structure
<i>count</i>	Number of bytes sent so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferIn-Progress</i>	transfer has finished or no transfer in progress.
<i>kStatus_Success</i>	Successfully return the count.

#### **24.8.8.5.7 status\_t FLEXIO\_UART\_TransferGetReceiveCountEDMA ( `FLEXIO_UART_Type * base, flexio_uart_edma_handle_t * handle, size_t * count` )**

This function gets the number of bytes received.

Parameters

<i>base</i>	Pointer to <a href="#">FLEXIO_UART_Type</a>
<i>handle</i>	Pointer to <code>flexio_uart_edma_handle_t</code> structure
<i>count</i>	Number of bytes received so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferIn-Progress</i>	transfer has finished or no transfer in progress.
<i>kStatus_Success</i>	Successfully return the count.

# Chapter 25

## FLEXRAM: on-chip RAM manager

### 25.1 Overview

The MCUXpresso SDK provides a driver for the FLEXRAM module of MCUXpresso SDK devices.

The FLEXRAM module integrates the ITCM, DTCM, and OCRAM controllers, and supports parameterized RAM array and RAM array portioning.

This example code shows how to allocate RAM using the FLEXRAM driver.

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/flexram`.

### Data Structures

- struct `flexram_allocate_ram_t`  
*FLEXRAM allocate ocram, itcm, dtcm size.* [More...](#)

### Macros

- #define `FLEXRAM_ECC_ERROR_DETAILED_INFO` 0U /\* Define to zero means get raw ECC error information, which needs parse it by user. \*/  
*Get ECC error detailed information.*

### Enumerations

- enum {  
  `kFLEXRAM_BankNotUsed` = 0U,  
  `kFLEXRAM_BankOCRAM` = 1U,  
  `kFLEXRAM_BankDTCM` = 2U,  
  `kFLEXRAM_BankITCM` = 3U }  
*FLEXRAM bank type.*
- enum `flexram_bank_allocate_src_t` {  
  `kFLEXRAM_BankAllocateThroughHardwareFuse` = 0U,  
  `kFLEXRAM_BankAllocateThroughBankCfg` = 1U }  
*FLEXRAM bank allocate source.*
- enum {  
  `kFLEXRAM_Read` = 0U,  
  `kFLEXRAM_Write` = 1U }  
*Flexram write/read selection.*
- enum {  
  `kFLEXRAM_OCRAMAccessError` = `FLEXRAM_INT_STATUS_OCRAM_ERR_STATUS_MASK`,  
  `kFLEXRAM_DTCMAccessError` = `FLEXRAM_INT_STATUS_DTCM_ERR_STATUS_MASK`,  
  `kFLEXRAM_ITCMAccessError` = `FLEXRAM_INT_STATUS_ITCM_ERR_STATUS_MASK`,

```

kFLEXRAM_InterruptStatusAll }

    Interrupt status flag mask.
• enum flexram_tcm_access_mode_t {
    kFLEXRAM_TCMAccessFastMode = 0U,
    kFLEXRAM_TCMAccessWaitMode = 1U }

        FLEXRAM TCM access mode.
• enum {

    kFLEXRAM_TCMSize32KB = 32 * 1024U,
    kFLEXRAM_TCMSize64KB = 64 * 1024U,
    kFLEXRAM_TCMSize128KB = 128 * 1024U,
    kFLEXRAM_TCMSize256KB = 256 * 1024U,
    kFLEXRAM_TCMSize512KB = 512 * 1024U }

        FLEXRAM TCM support size.

```

## Functions

- **status\_t FLEXRAM\_AllocateRam** (**flexram\_allocate\_ram\_t** \*config)
   
FLEXRAM allocate on-chip ram for OCRAM,ITCM,DTCM This function is independent of FLEXRAM -  
Init, it can be called directly if ram re-allocate is needed.
- static void **FLEXRAM\_SetAllocateRamSrc** (**flexram\_bank\_allocate\_src\_t** src)
   
FLEXRAM set allocate on-chip ram source.
- static void **FLEXRAM\_SetTCMReadAccessMode** (FLEXRAM\_Type \*base, **flexram\_tcm\_access\_-**  
**\_mode\_t** mode)
   
FLEXRAM module sets TCM read access mode.
- static void **FLEXRAM\_SetTCMWriteAccessMode** (FLEXRAM\_Type \*base, **flexram\_tcm\_access\_-**  
**\_mode\_t** mode)
   
FLEXRAM module set TCM write access mode.
- static void **FLEXRAM\_EnableForceRamClockOn** (FLEXRAM\_Type \*base, bool enable)
   
FLEXRAM module force ram clock on.

## Driver version

- #define **FSL\_SOC\_FLEXRAM\_ALLOCATE\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 0, 2))
   
SOC\_FLEXRAM\_ALLOCATE driver version 2.0.2.

## Driver version

- #define **FSL\_FLEXRAM\_DRIVER\_VERSION** (**MAKE\_VERSION**(2U, 3U, 0U))
   
Driver version.

## Initialization and de-initialization

- void **FLEXRAM\_Init** (FLEXRAM\_Type \*base)
   
FLEXRAM module initialization function.
- void **FLEXRAM\_Deinit** (FLEXRAM\_Type \*base)
   
De-initializes the FLEXRAM.

## Status

- static uint32\_t **FLEXRAM\_GetInterruptStatus** (FLEXRAM\_Type \*base)

- static void **FLEXRAM\_ClearInterruptStatus** (FLEXRAM\_Type \*base, uint32\_t status)  
*FLEXRAM module clears interrupt status.*
- static void **FLEXRAM\_EnableInterruptStatus** (FLEXRAM\_Type \*base, uint32\_t status)  
*FLEXRAM module enables interrupt status.*
- static void **FLEXRAM\_DisableInterruptStatus** (FLEXRAM\_Type \*base, uint32\_t status)  
*FLEXRAM module disable interrupt status.*

## Interrupts

- static void **FLEXRAM\_EnableInterruptSignal** (FLEXRAM\_Type \*base, uint32\_t status)  
*FLEXRAM module enables interrupt.*
- static void **FLEXRAM\_DisableInterruptSignal** (FLEXRAM\_Type \*base, uint32\_t status)  
*FLEXRAM module disables interrupt.*

## 25.2 Data Structure Documentation

### 25.2.1 struct flexram\_allocate\_ram\_t

#### Data Fields

- const uint8\_t **ocramBankNum**  
*ocram banknumber which the SOC support*
- const uint8\_t **dtemBankNum**  
*dtcm bank number to allocate, the number should be power of 2*
- const uint8\_t **itcmBankNum**  
*itcm bank number to allocate, the number should be power of 2*

## 25.3 Macro Definition Documentation

### 25.3.1 #define FSL\_SOC\_FLEXRAM\_ALLOCATE\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 2))

### 25.3.2 #define FSL\_FLEXRAM\_DRIVER\_VERSION (MAKE\_VERSION(2U, 3U, 0U))

### 25.3.3 #define FLEXRAM\_ECC\_ERROR\_DETAILED\_INFO 0U /\* Define to zero means get raw ECC error information, which needs parse it by user. \*/

## 25.4 Enumeration Type Documentation

### 25.4.1 anonymous enum

Enumerator

- kFLEXRAM\_BankNotUsed** bank is not used
- kFLEXRAM\_BankOCRAM** bank is OCRAM
- kFLEXRAM\_BankDTCM** bank is DTCM

*kFLEXRAM\_BankITCM* bank is ITCM

#### 25.4.2 enum flexram\_bank\_allocate\_src\_t

Enumerator

*kFLEXRAM\_BankAllocateThroughHardwareFuse* allocate ram through hardware fuse value  
*kFLEXRAM\_BankAllocateThroughBankCfg* allocate ram through FLEXRAM\_BANK\_CFG

#### 25.4.3 anonymous enum

Enumerator

*kFLEXRAM\_Read* read  
*kFLEXRAM\_Write* write

#### 25.4.4 anonymous enum

Enumerator

*kFLEXRAM\_OCRAMAccessError* OCRAM accesses unallocated address.  
*kFLEXRAM\_DTCMAccessError* DTCM accesses unallocated address.  
*kFLEXRAM\_ITCMAccessError* ITCM accesses unallocated address.  
*kFLEXRAM\_InterruptStatusAll* all the interrupt status mask

#### 25.4.5 enum flexram\_tcm\_access\_mode\_t

Fast access mode expected to be finished in 1-cycle; Wait access mode expected to be finished in 2-cycle. Wait access mode is a feature of the flexram and it should be used when the CPU clock is too fast to finish TCM access in 1-cycle. Normally, fast mode is the default mode, the efficiency of the TCM access will better.

Enumerator

*kFLEXRAM\_TCMAccessFastMode* fast access mode  
*kFLEXRAM\_TCMAccessWaitMode* wait access mode

#### 25.4.6 anonymous enum

Enumerator

*kFLEXRAM\_TCMSize32KB* TCM total size be 32KB.

***kFLEXRAM\_TCMSize64KB*** TCM total size be 64KB.  
***kFLEXRAM\_TCMSize128KB*** TCM total size be 128KB.  
***kFLEXRAM\_TCMSize256KB*** TCM total size be 256KB.  
***kFLEXRAM\_TCMSize512KB*** TCM total size be 512KB.

## 25.5 Function Documentation

### 25.5.1 status\_t FLEXRAM\_AllocateRam ( flexram\_allocate\_ram\_t \* config )

Parameters

<i>config</i>	allocate configuration.
---------------	-------------------------

Return values

<i>kStatus_InvalidArgument</i>	the argument is invalid	<i>kStatus_Success</i>	allocate success
--------------------------------	-------------------------	------------------------	------------------

### 25.5.2 static void FLEXRAM\_SetAllocateRamSrc ( flexram\_bank\_allocate\_src\_t src ) [inline], [static]

Parameters

<i>src</i>	bank config source select value.
------------	----------------------------------

### 25.5.3 void FLEXRAM\_Init ( FLEXRAM\_Type \* base )

Parameters

<i>base</i>	FLEXRAM base address.
-------------	-----------------------

### 25.5.4 static uint32\_t FLEXRAM\_GetInterruptStatus ( FLEXRAM\_Type \* base ) [inline], [static]

Parameters

<i>base</i>	FLEXRAM base address.
-------------	-----------------------

**25.5.5 static void FLEXRAM\_ClearInterruptStatus ( FLEXRAM\_Type \* *base*, uint32\_t *status* ) [inline], [static]**

Parameters

<i>base</i>	FLEXRAM base address.
<i>status</i>	Status to be cleared.

**25.5.6 static void FLEXRAM\_EnableInterruptStatus ( FLEXRAM\_Type \* *base*, uint32\_t *status* ) [inline], [static]**

Parameters

<i>base</i>	FLEXRAM base address.
<i>status</i>	Status to be enabled.

**25.5.7 static void FLEXRAM\_DisableInterruptStatus ( FLEXRAM\_Type \* *base*, uint32\_t *status* ) [inline], [static]**

Parameters

<i>base</i>	FLEXRAM base address.
<i>status</i>	Status to be disabled.

**25.5.8 static void FLEXRAM\_EnableInterruptSignal ( FLEXRAM\_Type \* *base*, uint32\_t *status* ) [inline], [static]**

Parameters

<i>base</i>	FLEXRAM base address.
<i>status</i>	Status interrupt to be enabled.

**25.5.9 static void FLEXRAM\_DisableInterruptSignal ( FLEXRAM\_Type \* *base*, uint32\_t *status* ) [inline], [static]**

Parameters

<i>base</i>	FLEXRAM base address.
<i>status</i>	Status interrupt to be disabled.

**25.5.10 static void FLEXRAM\_SetTCMReadAccessMode ( FLEXRAM\_Type \* *base*, flexram\_tcm\_access\_mode\_t *mode* ) [inline], [static]**

Parameters

<i>base</i>	FLEXRAM base address.
<i>mode</i>	Access mode.

**25.5.11 static void FLEXRAM\_SetTCMWriteAccessMode ( FLEXRAM\_Type \* *base*, flexram\_tcm\_access\_mode\_t *mode* ) [inline], [static]**

Parameters

<i>base</i>	FLEXRAM base address.
<i>mode</i>	Access mode.

**25.5.12 static void FLEXRAM\_EnableForceRamClockOn ( FLEXRAM\_Type \* *base*, bool *enable* ) [inline], [static]**

## Parameters

<i>base</i>	FLEXRAM base address.
<i>enable</i>	Enable or disable clock force on.

# Chapter 26

## FLEXSPI: Flexible Serial Peripheral Interface Driver

### 26.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Flexible Serial Peripheral Interface (FLEXSPI) module of MCUXpresso SDK/i.MX devices.

FLEXSPI driver includes functional APIs and interrupt/EDMA non-blocking transactional APIs.

Functional APIs are feature/property target low level APIs. Functional APIs can be used for FLEXSPI initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the FLEXSPI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. FLEXSPI functional operation groups provide the functional API set.

Transactional APIs are transaction target high level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `flexspi_handle_t`/`flexspi_edma_handle_t` as the second parameter. Initialize the handle for interrupt non-blocking transfer by calling the `FLEXSPI_TransferCreateHandle` API. Initialize the handle for interrupt non-blocking transfer by calling the `FLEXSPI_TransferCreateHandleEDMA` API.

Transactional APIs support asynchronous transfer. This means that the functions `FLEXSPI_TransferNonBlocking()` and `FLEXSPI_TransferEDMA()` set up data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_FLEXSPI_Idle` status.

### Modules

- [FLEXSPI eDMA Driver](#)

### Data Structures

- `struct flexspi_config_t`  
*FLEXSPI configuration structure.* [More...](#)
- `struct flexspi_device_config_t`  
*External device configuration items.* [More...](#)
- `struct flexspi_transfer_t`  
*Transfer structure for FLEXSPI.* [More...](#)
- `struct flexspi_handle_t`  
*Transfer handle structure for FLEXSPI.* [More...](#)

### Macros

- `#define FLEXSPI_LUT_SEQ(cmd0, pad0, op0, cmd1, pad1, op1)`  
*Formula to form FLEXSPI instructions in LUT table.*

## Typedefs

- `typedef void(* flexspi_transfer_callback_t )(FLEXSPI_Type *base, flexspi_handle_t *handle, status_t status, void *userData)`  
*FLEXSPI transfer callback function.*

## Enumerations

- `enum {`  
 `kStatus_FLEXSPI_Busy = MAKE_STATUS(kStatusGroup_FLEXSPI, 0),`  
 `kStatus_FLEXSPI_SequenceExecutionTimeout = MAKE_STATUS(kStatusGroup_FLEXSPI, 1),`  
 `kStatus_FLEXSPI_IpCommandSequenceError = MAKE_STATUS(kStatusGroup_FLEXSPI, 2),`  
 `kStatus_FLEXSPI_IpCommandGrantTimeout = MAKE_STATUS(kStatusGroup_FLEXSPI, 3) }`  
*Status structure of FLEXSPI.*
- `enum {`  
 `kFLEXSPI_Command_STOP = 0x00U,`  
 `kFLEXSPI_Command_SDR = 0x01U,`  
 `kFLEXSPI_Command_RADDR_SDR = 0x02U,`  
 `kFLEXSPI_Command_CADDR_SDR = 0x03U,`  
 `kFLEXSPI_Command_MODE1_SDR = 0x04U,`  
 `kFLEXSPI_Command_MODE2_SDR = 0x05U,`  
 `kFLEXSPI_Command_MODE4_SDR = 0x06U,`  
 `kFLEXSPI_Command_MODE8_SDR = 0x07U,`  
 `kFLEXSPI_Command_WRITE_SDR = 0x08U,`  
 `kFLEXSPI_Command_READ_SDR = 0x09U,`  
 `kFLEXSPI_Command_LEARN_SDR = 0x0AU,`  
 `kFLEXSPI_Command_DATSZ_SDR = 0x0BU,`  
 `kFLEXSPI_Command_DUMMY_SDR = 0x0CU,`  
 `kFLEXSPI_Command_DUMMY_RWDS_SDR = 0x0DU,`  
 `kFLEXSPI_Command_DDR = 0x21U,`  
 `kFLEXSPI_Command_RADDR_DDR = 0x22U,`  
 `kFLEXSPI_Command_CADDR_DDR = 0x23U,`  
 `kFLEXSPI_Command_MODE1_DDR = 0x24U,`  
 `kFLEXSPI_Command_MODE2_DDR = 0x25U,`  
 `kFLEXSPI_Command_MODE4_DDR = 0x26U,`  
 `kFLEXSPI_Command_MODE8_DDR = 0x27U,`  
 `kFLEXSPI_Command_WRITE_DDR = 0x28U,`  
 `kFLEXSPI_Command_READ_DDR = 0x29U,`  
 `kFLEXSPI_Command_LEARN_DDR = 0x2AU,`  
 `kFLEXSPI_Command_DATSZ_DDR = 0x2BU,`  
 `kFLEXSPI_Command_DUMMY_DDR = 0x2CU,`  
 `kFLEXSPI_Command_DUMMY_RWDS_DDR = 0x2DU,`  
 `kFLEXSPI_Command_JUMP_ON_CS = 0x1FU }`  
*CMD definition of FLEXSPI, use to form LUT instruction, \_flexspi\_command.*
- `enum flexspi_pad_t {`

```
kFLEXSPI_1PAD = 0x00U,
kFLEXSPI_2PAD = 0x01U,
kFLEXSPI_4PAD = 0x02U,
kFLEXSPI_8PAD = 0x03U }
```

*pad definition of FLEXSPI, use to form LUT instruction.*

- enum `flexspi_flags_t` {
   
kFLEXSPI\_SequenceExecutionTimeoutFlag = FLEXSPI\_INTEN\_SEQTIMEOUTEN\_MASK,
 kFLEXSPI\_AhbBusTimeoutFlag = FLEXSPI\_INTEN\_AHBBUSTIMEOUTEN\_MASK,
 kFLEXSPI\_SckStoppedBecauseTxEmptyFlag,
 kFLEXSPI\_SckStoppedBecauseRxFullFlag,
 kFLEXSPI\_IpTxFifoWatermarkEmptyFlag = FLEXSPI\_INTEN\_IPTXWEEN\_MASK,
 kFLEXSPI\_IpRxFifoWatermarkAvailableFlag = FLEXSPI\_INTEN\_IPRXWAEN\_MASK,
 kFLEXSPI\_AhbCommandSequenceErrorFlag,
 kFLEXSPI\_IpCommandSequenceErrorFlag = FLEXSPI\_INTEN\_IPCMDERREN\_MASK,
 kFLEXSPI\_AhbCommandGrantTimeoutFlag,
 kFLEXSPI\_IpCommandGrantTimeoutFlag,
 kFLEXSPI\_IpCommandExecutionDoneFlag,
 kFLEXSPI\_AllInterruptFlags = 0xFFFFU }

*FLEXSPI interrupt status flags.*

- enum `flexspi_read_sample_clock_t` {
   
kFLEXSPI\_ReadSampleClkLoopbackInternally = 0x0U,
 kFLEXSPI\_ReadSampleClkLoopbackFromDqsPad = 0x1U,
 kFLEXSPI\_ReadSampleClkLoopbackFromSckPad = 0x2U,
 kFLEXSPI\_ReadSampleClkExternalInputFromDqsPad = 0x3U }

*FLEXSPI sample clock source selection for Flash Reading.*

- enum `flexspi_cs_interval_cycle_unit_t` {
   
kFLEXSPI\_CsIntervalUnit1SckCycle = 0x0U,
 kFLEXSPI\_CsIntervalUnit256SckCycle = 0x1U }

*FLEXSPI interval unit for flash device select.*

- enum `flexspi_ahb_write_wait_unit_t` {
   
kFLEXSPI\_AhbWriteWaitUnit2AhbCycle = 0x0U,
 kFLEXSPI\_AhbWriteWaitUnit8AhbCycle = 0x1U,
 kFLEXSPI\_AhbWriteWaitUnit32AhbCycle = 0x2U,
 kFLEXSPI\_AhbWriteWaitUnit128AhbCycle = 0x3U,
 kFLEXSPI\_AhbWriteWaitUnit512AhbCycle = 0x4U,
 kFLEXSPI\_AhbWriteWaitUnit2048AhbCycle = 0x5U,
 kFLEXSPI\_AhbWriteWaitUnit8192AhbCycle = 0x6U,
 kFLEXSPI\_AhbWriteWaitUnit32768AhbCycle = 0x7U }

*FLEXSPI AHB wait interval unit for writing.*

- enum `flexspi_ip_error_code_t` {

```

kFLEXSPI_IpCmdErrorNoError = 0x0U,
kFLEXSPI_IpCmdErrorJumpOnCsInIpCmd = 0x2U,
kFLEXSPI_IpCmdErrorUnknownOpCode = 0x3U,
kFLEXSPI_IpCmdErrorSdrDummyInDdrSequence = 0x4U,
kFLEXSPI_IpCmdErrorDdrDummyInSdrSequence = 0x5U,
kFLEXSPI_IpCmdErrorInvalidAddress = 0x6U,
kFLEXSPI_IpCmdErrorSequenceExecutionTimeout = 0xEU,
kFLEXSPI_IpCmdErrorFlashBoundaryAcrosss = 0xFU }

```

*Error Code when IP command Error detected.*

- enum `flexspi_ahb_error_code_t` {
 

```

kFLEXSPI_AhbCmdErrorNoError = 0x0U,
kFLEXSPI_AhbCmdErrorJumpOnCsInWriteCmd = 0x2U,
kFLEXSPI_AhbCmdErrorUnknownOpCode = 0x3U,
kFLEXSPI_AhbCmdErrorSdrDummyInDdrSequence = 0x4U,
kFLEXSPI_AhbCmdErrorDdrDummyInSdrSequence = 0x5U,
kFLEXSPI_AhbCmdSequenceExecutionTimeout = 0x6U }
```

*Error Code when AHB command Error detected.*

- enum `flexspi_port_t` {
 

```

kFLEXSPI_PortA1 = 0x0U,
kFLEXSPI_PortA2,
kFLEXSPI_PortB1,
kFLEXSPI_PortB2 }
```
- enum `flexspi_arb_command_source_t`

*FLEXSPI operation port select.*
- enum `flexspi_command_type_t`

*Trigger source of current command sequence granted by arbitrator.*

```

kFLEXSPI_Command,
kFLEXSPI_Config }
```

*Command type.*

## Driver version

- #define `FSL_FLEXSPI_DRIVER_VERSION` (`MAKE_VERSION(2, 5, 1)`)  
*FLEXSPI driver version.*

## Initialization and deinitialization

- `uint32_t FLEXSPIGetInstance (FLEXSPI_Type *base)`  
*Get the instance number for FLEXSPI.*
- `status_t FLEXSPI_CheckAndClearError (FLEXSPI_Type *base, uint32_t status)`  
*Check and clear IP command execution errors.*
- `void FLEXSPI_Init (FLEXSPI_Type *base, const flexspi_config_t *config)`  
*Initializes the FLEXSPI module and internal state.*
- `void FLEXSPI_GetDefaultConfig (flexspi_config_t *config)`  
*Gets default settings for FLEXSPI.*
- `void FLEXSPI_Deinit (FLEXSPI_Type *base)`  
*Deinitializes the FLEXSPI module.*

- void **FLEXSPI\_UpdateDllValue** (FLEXSPI\_Type \*base, **flexspi\_device\_config\_t** \*config, **flexspi\_port\_t** port)  
*Update FLEXSPI DLL value depending on currently flexspi root clock.*
- void **FLEXSPI\_SetFlashConfig** (FLEXSPI\_Type \*base, **flexspi\_device\_config\_t** \*config, **flexspi\_port\_t** port)  
*Configures the connected device parameter.*
- static void **FLEXSPI\_SoftwareReset** (FLEXSPI\_Type \*base)  
*Software reset for the FLEXSPI logic.*
- static void **FLEXSPI\_Enable** (FLEXSPI\_Type \*base, bool enable)  
*Enables or disables the FLEXSPI module.*

## Interrupts

- static void **FLEXSPI\_EnableInterrupts** (FLEXSPI\_Type \*base, uint32\_t mask)  
*Enables the FLEXSPI interrupts.*
- static void **FLEXSPI\_DisableInterrupts** (FLEXSPI\_Type \*base, uint32\_t mask)  
*Disable the FLEXSPI interrupts.*

## DMA control

- static void **FLEXSPI\_EnableTxDMA** (FLEXSPI\_Type \*base, bool enable)  
*Enables or disables FLEXSPI IP Tx FIFO DMA requests.*
- static void **FLEXSPI\_EnableRxDMA** (FLEXSPI\_Type \*base, bool enable)  
*Enables or disables FLEXSPI IP Rx FIFO DMA requests.*
- static uint32\_t **FLEXSPI\_GetTxFifoAddress** (FLEXSPI\_Type \*base)  
*Gets FLEXSPI IP tx fifo address for DMA transfer.*
- static uint32\_t **FLEXSPI\_GetRxFifoAddress** (FLEXSPI\_Type \*base)  
*Gets FLEXSPI IP rx fifo address for DMA transfer.*

## FIFO control

- static void **FLEXSPI\_ResetFifos** (FLEXSPI\_Type \*base, bool txFifo, bool rxFifo)  
*Clears the FLEXSPI IP FIFO logic.*
- static void **FLEXSPI\_GetFifoCounts** (FLEXSPI\_Type \*base, size\_t \*txCount, size\_t \*rxCount)  
*Gets the valid data entries in the FLEXSPI FIFOs.*

## Status

- static uint32\_t **FLEXSPI\_GetInterruptStatusFlags** (FLEXSPI\_Type \*base)  
*Get the FLEXSPI interrupt status flags.*
- static void **FLEXSPI\_ClearInterruptStatusFlags** (FLEXSPI\_Type \*base, uint32\_t mask)  
*Get the FLEXSPI interrupt status flags.*
- static **flexspi\_arb\_command\_source\_t** **FLEXSPI\_GetArbitratorCommandSource** (FLEXSPI\_Type \*base)  
*Gets the trigger source of current command sequence granted by arbitrator.*
- static **flexspi\_ip\_error\_code\_t** **FLEXSPI\_GetIPCommandErrorCode** (FLEXSPI\_Type \*base, uint8\_t \*index)  
*Gets the error code when IP command error detected.*
- static **flexspi\_ahb\_error\_code\_t** **FLEXSPI\_GetAHBCommandErrorCode** (FLEXSPI\_Type \*base, uint8\_t \*index)

- Gets the error code when AHB command error detected.
- static bool [FLEXSPI\\_GetBusIdleStatus](#) (FLEXSPI\_Type \*base)  
Returns whether the bus is idle.

## Bus Operations

- void [FLEXSPI\\_UpdateRxSampleClock](#) (FLEXSPI\_Type \*base, [flexspi\\_read\\_sample\\_clock\\_t](#) clockSource)  
*Update read sample clock source.*
- static void [FLEXSPI\\_EnableIPParallelMode](#) (FLEXSPI\_Type \*base, bool enable)  
*Enables/disables the FLEXSPI IP command parallel mode.*
- static void [FLEXSPI\\_EnableAHBParallelMode](#) (FLEXSPI\_Type \*base, bool enable)  
*Enables/disables the FLEXSPI AHB command parallel mode.*
- void [FLEXSPI\\_UpdateLUT](#) (FLEXSPI\_Type \*base, uint32\_t index, const uint32\_t \*cmd, uint32\_t count)  
*Updates the LUT table.*
- static void [FLEXSPI\\_WriteData](#) (FLEXSPI\_Type \*base, uint32\_t data, uint8\_t fifoIndex)  
*Writes data into FIFO.*
- static uint32\_t [FLEXSPI\\_ReadData](#) (FLEXSPI\_Type \*base, uint8\_t fifoIndex)  
*Receives data from data FIFO.*
- status\_t [FLEXSPI\\_WriteBlocking](#) (FLEXSPI\_Type \*base, uint8\_t \*buffer, size\_t size)  
*Sends a buffer of data bytes using blocking method.*
- status\_t [FLEXSPI\\_ReadBlocking](#) (FLEXSPI\_Type \*base, uint8\_t \*buffer, size\_t size)  
*Receives a buffer of data bytes using a blocking method.*
- status\_t [FLEXSPI\\_TransferBlocking](#) (FLEXSPI\_Type \*base, [flexspi\\_transfer\\_t](#) \*xfer)  
*Execute command to transfer a buffer data bytes using a blocking method.*

## Transactional

- void [FLEXSPI\\_TransferCreateHandle](#) (FLEXSPI\_Type \*base, [flexspi\\_handle\\_t](#) \*handle, [flexspi\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the FLEXSPI handle which is used in transactional functions.*
- status\_t [FLEXSPI\\_TransferNonBlocking](#) (FLEXSPI\_Type \*base, [flexspi\\_handle\\_t](#) \*handle, [flexspi\\_transfer\\_t](#) \*xfer)  
*Performs a interrupt non-blocking transfer on the FLEXSPI bus.*
- status\_t [FLEXSPI\\_TransferGetCount](#) (FLEXSPI\_Type \*base, [flexspi\\_handle\\_t](#) \*handle, size\_t \*count)  
*Gets the master transfer status during a interrupt non-blocking transfer.*
- void [FLEXSPI\\_TransferAbort](#) (FLEXSPI\_Type \*base, [flexspi\\_handle\\_t](#) \*handle)  
*Aborts an interrupt non-blocking transfer early.*
- void [FLEXSPI\\_TransferHandleIRQ](#) (FLEXSPI\_Type \*base, [flexspi\\_handle\\_t](#) \*handle)  
*Master interrupt handler.*

## 26.2 Data Structure Documentation

### 26.2.1 struct [flexspi\\_config\\_t](#)

#### Data Fields

- [flexspi\\_read\\_sample\\_clock\\_t](#) rxSampleClock

- Sample Clock source selection for Flash Reading.
- bool `enableSckFreeRunning`  
Enable/disable SCK output free-running.
- bool `enableCombination`  
Enable/disable combining PORT A and B Data Pins (*SIOA[3:0] and SIOB[3:0]*) to support Flash Octal mode.
- bool `enableDoze`  
Enable/disable doze mode support.
- bool `enableHalfSpeedAccess`  
Enable/disable divide by 2 of the clock for half speed commands.
- bool `enableSckBDiffOpt`  
Enable/disable SCKB pad use as SCKA differential clock output, when enable, Port B flash access is not available.
- bool `enableSameConfigForAll`  
Enable/disable same configuration for all connected devices when enabled, same configuration in *FLASHA1CRx* is applied to all.
- uint16\_t `seqTimeoutCycle`  
Timeout wait cycle for command sequence execution, timeout after *ahbGrantTimeoutCycle\*1024 serial root clock cycles*.
- uint8\_t `ipGrantTimeoutCycle`  
Timeout wait cycle for IP command grant, timeout after *ipGrantTimeoutCycle\*1024 AHB clock cycles*.
- uint8\_t `txWatermark`  
FLEXSPI IP transmit watermark value.
- uint8\_t `rxWatermark`  
FLEXSPI receive watermark value.
- bool `enableAHBWriteIpTxFifo`  
Enable AHB bus write access to IP TX FIFO.
- bool `enableAHBWriteIpRxFifo`  
Enable AHB bus write access to IP RX FIFO.
- uint8\_t `ahbGrantTimeoutCycle`  
Timeout wait cycle for AHB command grant, timeout after *ahbGrantTimeoutCycle\*1024 AHB clock cycles*.
- uint16\_t `ahbBusTimeoutCycle`  
Timeout wait cycle for AHB read/write access, timeout after *ahbBusTimeoutCycle\*1024 AHB clock cycles*.
- uint8\_t `resumeWaitCycle`  
Wait cycle for idle state before suspended command sequence resume, timeout after *ahbBusTimeoutCycle AHB clock cycles*.
- flexspi\_ahbBuffer\_config\_t `buffer` [FSL\_FEATURE\_FLEXSPI\_AHB\_BUFFER\_COUNT]  
AHB buffer size.
- bool `enableClearAHBBufferOpt`  
Enable/disable automatically clean AHB RX Buffer and TX Buffer when FLEXSPI returns STOP mode ACK.
- bool `enableReadAddressOpt`  
Enable/disable remove AHB read burst start address alignment limitation.
- bool `enableAHBPrefetch`  
Enable/disable AHB read prefetch feature, when enabled, FLEXSPI will fetch more data than current AHB burst.
- bool `enableAHBBufferable`  
Enable/disable AHB bufferable write access support, when enabled,

- FLEXSPI return before waiting for command execution finished.*
- **bool enableAHBCachable**  
*Enable AHB bus cachable read access support.*

## Field Documentation

- (1) **flexspi\_read\_sample\_clock\_t flexspi\_config\_t::rxSampleClock**
- (2) **bool flexspi\_config\_t::enableSckFreeRunning**
- (3) **bool flexspi\_config\_t::enableCombination**
- (4) **bool flexspi\_config\_t::enableDoze**
- (5) **bool flexspi\_config\_t::enableHalfSpeedAccess**
- (6) **bool flexspi\_config\_t::enableSckBDiffOpt**
- (7) **bool flexspi\_config\_t::enableSameConfigForAll**
- (8) **uint16\_t flexspi\_config\_t::seqTimeoutCycle**
- (9) **uint8\_t flexspi\_config\_t::ipGrantTimeoutCycle**
- (10) **uint8\_t flexspi\_config\_t::txWatermark**
- (11) **uint8\_t flexspi\_config\_t::rxWatermark**
- (12) **bool flexspi\_config\_t::enableAHBWriteIpTxFifo**
- (13) **bool flexspi\_config\_t::enableAHBWriteIpRxFifo**
- (14) **uint8\_t flexspi\_config\_t::ahbGrantTimeoutCycle**
- (15) **uint16\_t flexspi\_config\_t::ahbBusTimeoutCycle**
- (16) **uint8\_t flexspi\_config\_t::resumeWaitCycle**
- (17) **flexspi\_ahbBuffer\_config\_t flexspi\_config\_t::buffer[FSL\_FEATURE\_FLEXSPI\_AHB\_BUFFER\_COUNT]**
- (18) **bool flexspi\_config\_t::enableClearAHBBufferOpt**
- (19) **bool flexspi\_config\_t::enableReadAddressOpt**

when enable, there is no AHB read burst start address alignment limitation.

- (20) **bool flexspi\_config\_t::enableAHBPrefetch**
- (21) **bool flexspi\_config\_t::enableAHBBufferable**
- (22) **bool flexspi\_config\_t::enableAHBCachable**

### 26.2.2 struct flexspi\_device\_config\_t

#### Data Fields

- **uint32\_t flexspiRootClk**  
*FLEXSPI serial root clock.*
- **bool isSck2Enabled**  
*FLEXSPI use SCK2.*
- **uint32\_t flashSize**  
*Flash size in KByte.*
- **flexspi\_cs\_interval\_cycle\_unit\_t CSIntervalUnit**  
*CS interval unit, 1 or 256 cycle.*
- **uint16\_t CSInterval**  
*CS line assert interval, multiply CS interval unit to get the CS line assert interval cycles.*
- **uint8\_t CSHoldTime**  
*CS line hold time.*
- **uint8\_t CSSetupTime**  
*CS line setup time.*
- **uint8\_t dataValidTime**  
*Data valid time for external device.*
- **uint8\_t columnspace**  
*Column space size.*
- **bool enableWordAddress**  
*If enable word address.*
- **uint8\_t AWRSeqIndex**  
*Sequence ID for AHB write command.*
- **uint8\_t AWRSeqNumber**  
*Sequence number for AHB write command.*
- **uint8\_t ARDSeqIndex**  
*Sequence ID for AHB read command.*
- **uint8\_t ARDSeqNumber**  
*Sequence number for AHB read command.*
- **flexspi\_ahb\_write\_wait\_unit\_t AHBWriteWaitUnit**  
*AHB write wait unit.*
- **uint16\_t AHBWriteWaitInterval**  
*AHB write wait interval, multiply AHB write interval unit to get the AHB write wait cycles.*
- **bool enableWriteMask**  
*Enable/Disable FLEXSPI drive DQS pin as write mask when writing to external device.*

**Field Documentation**

- (1) `uint32_t flexspi_device_config_t::flexspiRootClk`
- (2) `bool flexspi_device_config_t::isSck2Enabled`
- (3) `uint32_t flexspi_device_config_t::flashSize`
- (4) `flexspi_cs_interval_cycle_unit_t flexspi_device_config_t::CSIntervalUnit`
- (5) `uint16_t flexspi_device_config_t::CSInterval`
- (6) `uint8_t flexspi_device_config_t::CSHoldTime`
- (7) `uint8_t flexspi_device_config_t::CSSetupTime`
- (8) `uint8_t flexspi_device_config_t::dataValidTime`
- (9) `uint8_t flexspi_device_config_t::columnspace`
- (10) `bool flexspi_device_config_t::enableWordAddress`
- (11) `uint8_t flexspi_device_config_t::AWRSeqIndex`
- (12) `uint8_t flexspi_device_config_t::AWRSeqNumber`
- (13) `uint8_t flexspi_device_config_t::ARDSeqIndex`
- (14) `uint8_t flexspi_device_config_t::ARDSeqNumber`
- (15) `flexspi_ahb_write_wait_unit_t flexspi_device_config_t::AHBWriteWaitUnit`
- (16) `uint16_t flexspi_device_config_t::AHBWriteWaitInterval`
- (17) `bool flexspi_device_config_t::enableWriteMask`

**26.2.3 struct flexspi\_transfer\_t****Data Fields**

- `uint32_t deviceAddress`  
*Operation device address.*
- `flexspi_port_t port`  
*Operation port.*
- `flexspi_command_type_t cmdType`  
*Execution command type.*
- `uint8_t seqIndex`  
*Sequence ID for command.*
- `uint8_t SeqNumber`  
*Sequence number for command.*

- `uint32_t * data`  
*Data buffer.*
- `size_t dataSize`  
*Data size in bytes.*

### Field Documentation

- (1) `uint32_t flexspi_transfer_t::deviceAddress`
- (2) `flexspi_port_t flexspi_transfer_t::port`
- (3) `flexspi_command_type_t flexspi_transfer_t::cmdType`
- (4) `uint8_t flexspi_transfer_t::seqIndex`
- (5) `uint8_t flexspi_transfer_t::SeqNumber`
- (6) `uint32_t* flexspi_transfer_t::data`
- (7) `size_t flexspi_transfer_t::dataSize`

### 26.2.4 struct \_flexspi\_handle

#### Data Fields

- `uint32_t state`  
*Internal state for FLEXSPI transfer.*
- `uint8_t * data`  
*Data buffer.*
- `size_t dataSize`  
*Remaining Data size in bytes.*
- `size_t transferTotalSize`  
*Total Data size in bytes.*
- `flexspi_transfer_callback_t completionCallback`  
*Callback for users while transfer finish or error occurred.*
- `void * userData`  
*FLEXSPI callback function parameter.*

### Field Documentation

- (1) `uint8_t* flexspi_handle_t::data`
- (2) `size_t flexspi_handle_t::dataSize`
- (3) `size_t flexspi_handle_t::transferTotalSize`
- (4) `void* flexspi_handle_t::userData`

## 26.3 Macro Definition Documentation

**26.3.1 #define FSL\_FLEXSPI\_DRIVER\_VERSION (MAKE\_VERSION(2, 5, 1))**

**26.3.2 #define FLEXSPI\_LUT\_SEQ( cmd0, pad0, op0, cmd1, pad1, op1 )**

**Value:**

```
(FLEXSPI_LUT_OPERAND0 (op0) | FLEXSPI_LUT_NUM_PADS0 (pad0) | FLEXSPI_LUT_OPCODE0 (cmd0) | FLEXSPI_LUT_OPERAND1
  (op1) | \
  FLEXSPI_LUT_NUM_PADS1 (pad1) | FLEXSPI_LUT_OPCODE1 (cmd1))
```

## 26.4 Typedef Documentation

**26.4.1 typedef void(\* flexspi\_transfer\_callback\_t)(FLEXSPI\_Type \*base,  
flexspi\_handle\_t \*handle, status\_t status, void \*userData)**

## 26.5 Enumeration Type Documentation

### 26.5.1 anonymous enum

Enumerator

**kStatus\_FLEXSPI\_Busy** FLEXSPI is busy.

**kStatus\_FLEXSPI\_SequenceExecutionTimeout** Sequence execution timeout error occurred during FLEXSPI transfer.

**kStatus\_FLEXSPI\_IpCommandSequenceError** IP command Sequence execution timeout error occurred during FLEXSPI transfer.

**kStatus\_FLEXSPI\_IpCommandGrantTimeout** IP command grant timeout error occurred during FLEXSPI transfer.

### 26.5.2 anonymous enum

Enumerator

**kFLEXSPI\_Command\_STOP** Stop execution, deassert CS.

**kFLEXSPI\_Command\_SDR** Transmit Command code to Flash, using SDR mode.

**kFLEXSPI\_Command\_RADDR\_SDR** Transmit Row Address to Flash, using SDR mode.

**kFLEXSPI\_Command\_CADDR\_SDR** Transmit Column Address to Flash, using SDR mode.

**kFLEXSPI\_Command\_MODE1\_SDR** Transmit 1-bit Mode bits to Flash, using SDR mode.

**kFLEXSPI\_Command\_MODE2\_SDR** Transmit 2-bit Mode bits to Flash, using SDR mode.

**kFLEXSPI\_Command\_MODE4\_SDR** Transmit 4-bit Mode bits to Flash, using SDR mode.

**kFLEXSPI\_Command\_MODE8\_SDR** Transmit 8-bit Mode bits to Flash, using SDR mode.

**kFLEXSPI\_Command\_WRITE\_SDR** Transmit Programming Data to Flash, using SDR mode.

**kFLEXSPI\_Command\_READ\_SDR** Receive Read Data from Flash, using SDR mode.

***kFLEXSPI\_Command\_LEARN\_SDR*** Receive Read Data or Preamble bit from Flash, SDR mode.

***kFLEXSPI\_Command\_DATSZ\_SDR*** Transmit Read/Program Data size (byte) to Flash, SDR mode.

***kFLEXSPI\_Command\_DUMMY\_SDR*** Leave data lines undriven by FlexSPI controller.

***kFLEXSPI\_Command\_DUMMY\_RWDS\_SDR*** Leave data lines undriven by FlexSPI controller, dummy cycles decided by RWDS.

***kFLEXSPI\_Command\_DDR*** Transmit Command code to Flash, using DDR mode.

***kFLEXSPI\_Command\_RADDR\_DDR*** Transmit Row Address to Flash, using DDR mode.

***kFLEXSPI\_Command\_CADDR\_DDR*** Transmit Column Address to Flash, using DDR mode.

***kFLEXSPI\_Command\_MODE1\_DDR*** Transmit 1-bit Mode bits to Flash, using DDR mode.

***kFLEXSPI\_Command\_MODE2\_DDR*** Transmit 2-bit Mode bits to Flash, using DDR mode.

***kFLEXSPI\_Command\_MODE4\_DDR*** Transmit 4-bit Mode bits to Flash, using DDR mode.

***kFLEXSPI\_Command\_MODE8\_DDR*** Transmit 8-bit Mode bits to Flash, using DDR mode.

***kFLEXSPI\_Command\_WRITE\_DDR*** Transmit Programming Data to Flash, using DDR mode.

***kFLEXSPI\_Command\_READ\_DDR*** Receive Read Data from Flash, using DDR mode.

***kFLEXSPI\_Command\_LEARN\_DDR*** Receive Read Data or Preamble bit from Flash, DDR mode.

***kFLEXSPI\_Command\_DATSZ\_DDR*** Transmit Read/Program Data size (byte) to Flash, DDR mode.

***kFLEXSPI\_Command\_DUMMY\_DDR*** Leave data lines undriven by FlexSPI controller.

***kFLEXSPI\_Command\_DUMMY\_RWDS\_DDR*** Leave data lines undriven by FlexSPI controller, dummy cycles decided by RWDS.

***kFLEXSPI\_Command\_JUMP\_ON\_CS*** Stop execution, deassert CS and save operand[7:0] as the instruction start pointer for next sequence.

### 26.5.3 enum flexspi\_pad\_t

Enumerator

***kFLEXSPI\_1PAD*** Transmit command/address and transmit/receive data only through DATA0/DATA1.

***kFLEXSPI\_2PAD*** Transmit command/address and transmit/receive data only through DATA[1:0].

***kFLEXSPI\_4PAD*** Transmit command/address and transmit/receive data only through DATA[3:0].

***kFLEXSPI\_8PAD*** Transmit command/address and transmit/receive data only through DATA[7:0].

### 26.5.4 enum flexspi\_flags\_t

Enumerator

***kFLEXSPI\_SequenceExecutionTimeoutFlag*** Sequence execution timeout.

***kFLEXSPI\_AhbBusTimeoutFlag*** AHB Bus timeout.

***kFLEXSPI\_SckStoppedBecauseTxEmptyFlag*** SCK is stopped during command sequence because Async TX FIFO empty.

***kFLEXSPI\_SckStoppedBecauseRxFullFlag*** SCK is stopped during command sequence because Async RX FIFO full.

***kFLEXSPI\_IpTxFifoWatermarkEmptyFlag*** IP TX FIFO WaterMark empty.

***kFLEXSPI\_IpRxFifoWatermarkAvailableFlag*** IP RX FIFO WaterMark available.

***kFLEXSPI\_AhbCommandSequenceErrorFlag*** AHB triggered Command Sequences Error.

***kFLEXSPI\_IpCommandSequenceErrorFlag*** IP triggered Command Sequences Error.

***kFLEXSPI\_AhbCommandGrantTimeoutFlag*** AHB triggered Command Sequences Grant Timeout.

***kFLEXSPI\_IpCommandGrantTimeoutFlag*** IP triggered Command Sequences Grant Timeout.

***kFLEXSPI\_IpCommandExecutionDoneFlag*** IP triggered Command Sequences Execution finished.

***kFLEXSPI\_AllInterruptFlags*** All flags.

## 26.5.5 enum flexspi\_read\_sample\_clock\_t

Enumerator

***kFLEXSPI\_ReadSampleClkLoopbackInternally*** Dummy Read strobe generated by FlexSPI Controller and loopback internally.

***kFLEXSPI\_ReadSampleClkLoopbackFromDqsPad*** Dummy Read strobe generated by FlexSPI Controller and loopback from DQS pad.

***kFLEXSPI\_ReadSampleClkLoopbackFromSckPad*** SCK output clock and loopback from SCK pad.

***kFLEXSPI\_ReadSampleClkExternalInputFromDqsPad*** Flash provided Read strobe and input from DQS pad.

## 26.5.6 enum flexspi\_cs\_interval\_cycle\_unit\_t

Enumerator

***kFLEXSPI\_CsIntervalUnit1SckCycle*** Chip selection interval: CSINTERVAL \* 1 serial clock cycle.

***kFLEXSPI\_CsIntervalUnit256SckCycle*** Chip selection interval: CSINTERVAL \* 256 serial clock cycle.

## 26.5.7 enum flexspi\_ahb\_write\_wait\_unit\_t

Enumerator

***kFLEXSPI\_AhbWriteWaitUnit2AhbCycle*** AWRWAIT unit is 2 ahb clock cycle.

***kFLEXSPI\_AhbWriteWaitUnit8AhbCycle*** AWRWAIT unit is 8 ahb clock cycle.  
***kFLEXSPI\_AhbWriteWaitUnit32AhbCycle*** AWRWAIT unit is 32 ahb clock cycle.  
***kFLEXSPI\_AhbWriteWaitUnit128AhbCycle*** AWRWAIT unit is 128 ahb clock cycle.  
***kFLEXSPI\_AhbWriteWaitUnit512AhbCycle*** AWRWAIT unit is 512 ahb clock cycle.  
***kFLEXSPI\_AhbWriteWaitUnit2048AhbCycle*** AWRWAIT unit is 2048 ahb clock cycle.  
***kFLEXSPI\_AhbWriteWaitUnit8192AhbCycle*** AWRWAIT unit is 8192 ahb clock cycle.  
***kFLEXSPI\_AhbWriteWaitUnit32768AhbCycle*** AWRWAIT unit is 32768 ahb clock cycle.

### 26.5.8 enum flexspi\_ip\_error\_code\_t

Enumerator

***kFLEXSPI\_IpCmdErrorNoError*** No error.  
***kFLEXSPI\_IpCmdErrorJumpOnCsInIpCmd*** IP command with JMP\_ON\_CS instruction used.  
***kFLEXSPI\_IpCmdErrorUnknownOpCode*** Unknown instruction opcode in the sequence.  
***kFLEXSPI\_IpCmdErrorSdrDummyInDdrSequence*** Instruction DUMMY\_SDR/DUMMY\_RW-DS\_SDR used in DDR sequence.  
***kFLEXSPI\_IpCmdErrorDdrDummyInSdrSequence*** Instruction DUMMY\_DDR/DUMMY\_RW-DS\_DDR used in SDR sequence.  
***kFLEXSPI\_IpCmdErrorInvalidAddress*** Flash access start address exceed the whole flash address range (A1/A2/B1/B2).  
***kFLEXSPI\_IpCmdErrorSequenceExecutionTimeout*** Sequence execution timeout.  
***kFLEXSPI\_IpCmdErrorFlashBoundaryAcrosss*** Flash boundary crossed.

### 26.5.9 enum flexspi\_ahb\_error\_code\_t

Enumerator

***kFLEXSPI\_AhbCmdErrorNoError*** No error.  
***kFLEXSPI\_AhbCmdErrorJumpOnCsInWriteCmd*** AHB Write command with JMP\_ON\_CS instruction used in the sequence.  
***kFLEXSPI\_AhbCmdErrorUnknownOpCode*** Unknown instruction opcode in the sequence.  
***kFLEXSPI\_AhbCmdErrorSdrDummyInDdrSequence*** Instruction DUMMY\_SDR/DUMMY\_R-WDS\_SDR used in DDR sequence.  
***kFLEXSPI\_AhbCmdErrorDdrDummyInSdrSequence*** Instruction DUMMY\_DDR/DUMMY\_R-WDS\_DDR used in SDR sequence.  
***kFLEXSPI\_AhbCmdSequenceExecutionTimeout*** Sequence execution timeout.

### 26.5.10 enum flexspi\_port\_t

Enumerator

***kFLEXSPI\_PortA1*** Access flash on A1 port.

- kFLEXSPI\_PortA2* Access flash on A2 port.
- kFLEXSPI\_PortB1* Access flash on B1 port.
- kFLEXSPI\_PortB2* Access flash on B2 port.

### 26.5.11 enum flexspi\_arb\_command\_source\_t

### 26.5.12 enum flexspi\_command\_type\_t

Enumerator

- kFLEXSPI\_Command* FlexSPI operation: Only command, both TX and Rx buffer are ignored.
- kFLEXSPI\_Config* FlexSPI operation: Configure device mode, the TX fifo size is fixed in LUT.

## 26.6 Function Documentation

### 26.6.1 uint32\_t FLEXSPI\_GetInstance ( **FLEXSPI\_Type** \* *base* )

Parameters

<i>base</i>	FLEXSPI base pointer.
-------------	-----------------------

### 26.6.2 status\_t FLEXSPI\_CheckAndClearError ( **FLEXSPI\_Type** \* *base*, **uint32\_t** *status* )

Parameters

<i>base</i>	FLEXSPI base pointer.
<i>status</i>	interrupt status.

### 26.6.3 void FLEXSPI\_Init ( **FLEXSPI\_Type** \* *base*, **const flexspi\_config\_t** \* *config* )

This function enables the clock for FLEXSPI and also configures the FLEXSPI with the input configure parameters. Users should call this function before any FLEXSPI operations.

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>config</i>	FLEXSPI configure structure.

#### 26.6.4 void FLEXSPI\_GetDefaultConfig ( *flexspi\_config\_t* \* *config* )

Parameters

<i>config</i>	FLEXSPI configuration structure.
---------------	----------------------------------

#### 26.6.5 void FLEXSPI\_Deinit ( *FLEXSPI\_Type* \* *base* )

Clears the FLEXSPI state and FLEXSPI module registers.

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

#### 26.6.6 void FLEXSPI\_UpdateDIIValue ( *FLEXSPI\_Type* \* *base*, *flexspi\_device\_config\_t* \* *config*, *flexspi\_port\_t* *port* )

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>config</i>	Flash configuration parameters.
<i>port</i>	FLEXSPI Operation port.

#### 26.6.7 void FLEXSPI\_SetFlashConfig ( *FLEXSPI\_Type* \* *base*, *flexspi\_device\_config\_t* \* *config*, *flexspi\_port\_t* *port* )

This function configures the connected device relevant parameters, such as the size, command, and so on. The flash configuration value cannot have a default value. The user needs to configure it according to the connected device.

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>config</i>	Flash configuration parameters.
<i>port</i>	FLEXSPI Operation port.

### 26.6.8 static void FLEXSPI\_SoftwareReset ( FLEXSPI\_Type \* *base* ) [inline], [static]

This function sets the software reset flags for both AHB and buffer domain and resets both AHB buffer and also IP FIFOs.

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

### 26.6.9 static void FLEXSPI\_Enable ( FLEXSPI\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>enable</i>	True means enable FLEXSPI, false means disable.

### 26.6.10 static void FLEXSPI\_EnableInterrupts ( FLEXSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>mask</i>	FLEXSPI interrupt source.

### 26.6.11 static void FLEXSPI\_DisableInterrupts ( FLEXSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>mask</i>	FLEXSPI interrupt source.

**26.6.12 static void FLEXSPI\_EnableTxDMA ( FLEXSPI\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>enable</i>	Enable flag for transmit DMA request. Pass true for enable, false for disable.

**26.6.13 static void FLEXSPI\_EnableRxDMA ( FLEXSPI\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>enable</i>	Enable flag for receive DMA request. Pass true for enable, false for disable.

**26.6.14 static uint32\_t FLEXSPI\_GetTxFifoAddress ( FLEXSPI\_Type \* *base* )  
[inline], [static]**

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

Return values

<i>The</i>	tx fifo address.
------------	------------------

**26.6.15 static uint32\_t FLEXSPI\_GetRxFifoAddress ( FLEXSPI\_Type \* *base* )  
[inline], [static]**

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

Return values

<i>The</i>	rx fifo address.
------------	------------------

### 26.6.16 static void FLEXSPI\_ResetFifos ( FLEXSPI\_Type \* *base*, bool *txFifo*, bool *rxFifo* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>txFifo</i>	Pass true to reset TX FIFO.
<i>rxFifo</i>	Pass true to reset RX FIFO.

### 26.6.17 static void FLEXSPI\_GetFifoCounts ( FLEXSPI\_Type \* *base*, size\_t \* *txCount*, size\_t \* *rxCount* ) [inline], [static]

Parameters

	<i>base</i>	FLEXSPI peripheral base address.
out	<i>txCount</i>	Pointer through which the current number of bytes in the transmit FIFO is returned. Pass NULL if this value is not required.
out	<i>rxCount</i>	Pointer through which the current number of bytes in the receive FIFO is returned. Pass NULL if this value is not required.

### 26.6.18 static uint32\_t FLEXSPI\_GetInterruptStatusFlags ( FLEXSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

Return values

<i>interrupt</i>	status flag, use status flag to AND <code>flexspi_flags_t</code> could get the related status.
------------------	--

### 26.6.19 static void FLEXSPI\_ClearInterruptStatusFlags ( `FLEXSPI_Type` \* *base*, `uint32_t` *mask* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>mask</i>	FLEXSPI interrupt source.

### 26.6.20 static `flexspi_arb_command_source_t` FLEXSPI\_GetArbitrator-CommandSource ( `FLEXSPI_Type` \* *base* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

Return values

<i>trigger</i>	source of current command sequence.
----------------	-------------------------------------

### 26.6.21 static `flexspi_ip_error_code_t` FLEXSPI\_GetIPCommandErrorCode ( `FLEXSPI_Type` \* *base*, `uint8_t` \* *index* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

<i>index</i>	Pointer to a uint8_t type variable to receive the sequence index when error detected.
--------------	---

Return values

<i>error</i>	code when IP command error detected.
--------------	--------------------------------------

### 26.6.22 static flexspi\_ahb\_error\_code\_t FLEXSPI\_GetAHBCommandErrorCode ( FLEXSPI\_Type \* *base*, uint8\_t \* *index* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>index</i>	Pointer to a uint8_t type variable to receive the sequence index when error detected.

Return values

<i>error</i>	code when AHB command error detected.
--------------	---------------------------------------

### 26.6.23 static bool FLEXSPI\_GetBusIdleStatus ( FLEXSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
-------------	----------------------------------

Return values

<i>true</i>	Bus is idle.
<i>false</i>	Bus is busy.

### 26.6.24 void FLEXSPI\_UpdateRxSampleClock ( FLEXSPI\_Type \* *base*, flexspi\_read\_sample\_clock\_t *clockSource* )

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>clockSource</i>	clockSource of type <a href="#">flexspi_read_sample_clock_t</a>

#### 26.6.25 static void FLEXSPI\_EnableIPParallelMode ( FLEXSPI\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>enable</i>	True means enable parallel mode, false means disable parallel mode.

#### 26.6.26 static void FLEXSPI\_EnableAHBParallelMode ( FLEXSPI\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>enable</i>	True means enable parallel mode, false means disable parallel mode.

#### 26.6.27 void FLEXSPI\_UpdateLUT ( FLEXSPI\_Type \* *base*, uint32\_t *index*, const uint32\_t \* *cmd*, uint32\_t *count* )

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>index</i>	From which index start to update. It could be any index of the LUT table, which also allows user to update command content inside a command. Each command consists of up to 8 instructions and occupy 4*32-bit memory.

<i>cmd</i>	Command sequence array.
<i>count</i>	Number of sequences.

**26.6.28 static void FLEXSPI\_WriteData ( FLEXSPI\_Type \* *base*, uint32\_t *data*, uint8\_t *fifoIndex* ) [inline], [static]**

Parameters

<i>base</i>	FLEXSPI peripheral base address
<i>data</i>	The data bytes to send
<i>fifoIndex</i>	Destination fifo index.

**26.6.29 static uint32\_t FLEXSPI\_ReadData ( FLEXSPI\_Type \* *base*, uint8\_t *fifoIndex* ) [inline], [static]**

Parameters

<i>base</i>	FLEXSPI peripheral base address
<i>fifoIndex</i>	Source fifo index.

Returns

The data in the FIFO.

**26.6.30 status\_t FLEXSPI\_WriteBlocking ( FLEXSPI\_Type \* *base*, uint8\_t \* *buffer*, size\_t *size* )**

Note

This function blocks via polling until all bytes have been sent.

Parameters

---

<i>base</i>	FLEXSPI peripheral base address
<i>buffer</i>	The data bytes to send
<i>size</i>	The number of data bytes to send

Return values

<i>kStatus_Success</i>	write success without error
<i>kStatus_FLEXSPI_SequenceExecutionTimeout</i>	sequence execution timeout
<i>kStatus_FLEXSPI_IpCommandSequenceError</i>	IP command sequence error detected
<i>kStatus_FLEXSPI_IpCommandGrantTimeout</i>	IP command grant timeout detected

### 26.6.31 **status\_t FLEXSPI\_ReadBlocking ( FLEXSPI\_Type \* *base*, uint8\_t \* *buffer*, size\_t *size* )**

Note

This function blocks via polling until all bytes have been sent.

Parameters

<i>base</i>	FLEXSPI peripheral base address
<i>buffer</i>	The data bytes to send
<i>size</i>	The number of data bytes to receive

Return values

<i>kStatus_Success</i>	read success without error
<i>kStatus_FLEXSPI_SequenceExecutionTimeout</i>	sequence execution timeout

<i>kStatus_FLEXSPI_Ip-CommandSequenceError</i>	IP command sequence error detected
<i>kStatus_FLEXSPI_Ip-CommandGrantTimeout</i>	IP command grant timeout detected

### 26.6.32 **status\_t FLEXSPI\_TransferBlocking ( FLEXSPI\_Type \* *base*, flexspi\_transfer\_t \* *xfer* )**

Parameters

<i>base</i>	FLEXSPI peripheral base address
<i>xfer</i>	pointer to the transfer structure.

Return values

<i>kStatus_Success</i>	command transfer success without error
<i>kStatus_FLEXSPI_SequenceExecutionTimeout</i>	sequence execution timeout
<i>kStatus_FLEXSPI_Ip-CommandSequenceError</i>	IP command sequence error detected
<i>kStatus_FLEXSPI_Ip-CommandGrantTimeout</i>	IP command grant timeout detected

### 26.6.33 **void FLEXSPI\_TransferCreateHandle ( FLEXSPI\_Type \* *base*, flexspi\_handle\_t \* *handle*, flexspi\_transfer\_callback\_t *callback*, void \* *userData* )**

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	pointer to flexspi_handle_t structure to store the transfer state.

<i>callback</i>	pointer to user callback function.
<i>userData</i>	user parameter passed to the callback function.

### 26.6.34 status\_t FLEXSPI\_TransferNonBlocking ( **FLEXSPI\_Type** \* *base*, **flexspi\_handle\_t** \* *handle*, **flexspi\_transfer\_t** \* *xfer* )

#### Note

Calling the API returns immediately after transfer initiates. The user needs to call FLEXSPI\_GetTransferCount to poll the transfer status to check whether the transfer is finished. If the return status is not kStatus\_FLEXSPI\_Busy, the transfer is finished. For FLEXSPI\_Read, the dataSize should be multiple of rx watermark level, or FLEXSPI could not read data properly.

#### Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	pointer to <b>flexspi_handle_t</b> structure which stores the transfer state.
<i>xfer</i>	pointer to <b>flexspi_transfer_t</b> structure.

#### Return values

<i>kStatus_Success</i>	Successfully start the data transmission.
<i>kStatus_FLEXSPI_Busy</i>	Previous transmission still not finished.

### 26.6.35 status\_t FLEXSPI\_TransferGetCount ( **FLEXSPI\_Type** \* *base*, **flexspi\_handle\_t** \* *handle*, **size\_t** \* *count* )

#### Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	pointer to <b>flexspi_handle_t</b> structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

#### Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

### 26.6.36 void FLEXSPI\_TransferAbort ( **FLEXSPI\_Type** \* *base*, **flexspi\_handle\_t** \* *handle* )

Note

This API can be called at any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	pointer to <b>flexspi_handle_t</b> structure which stores the transfer state

### 26.6.37 void FLEXSPI\_TransferHandleIRQ ( **FLEXSPI\_Type** \* *base*, **flexspi\_handle\_t** \* *handle* )

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	pointer to <b>flexspi_handle_t</b> structure.

## 26.7 FLEXSPI eDMA Driver

### 26.7.1 Overview

#### Data Structures

- struct `flexspi_edma_handle_t`

*FLEXSPI DMA transfer handle, users should not touch the content of the handle. [More...](#)*

#### TypeDefs

- typedef void(\* `flexspi_edma_callback_t` )(FLEXSPI\_Type \*base, flexspi\_edma\_handle\_t \*handle, `status_t` status, void \*userData)

*FLEXSPI eDMA transfer callback function for finish and error.*

#### Enumerations

- enum `flexspi_edma_transfer_nsize_t` {
   
    kFLEXPSI\_EDMA\_NSize1Bytes = 0x1U,
   
    kFLEXPSI\_EDMA\_NSize2Bytes = 0x2U,
   
    kFLEXPSI\_EDMA\_NSize4Bytes = 0x4U,
   
    kFLEXPSI\_EDMA\_NSize8Bytes = 0x8U,
   
    kFLEXPSI\_EDMA\_NSize32Bytes = 0x20U }

*eDMA transfer configuration*

#### Driver version

- #define `FSL_FLEXSPI_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 3)`)

*FLEXSPI EDMA driver version.*

#### FLEXSPI eDMA Transactional

- void `FLEXSPI_TransferCreateHandleEDMA` (FLEXSPI\_Type \*base, flexspi\_edma\_handle\_t \*handle, `flexspi_edma_callback_t` callback, void \*userData, `edma_handle_t` \*txDmaHandle, `edma_handle_t` \*rxDmaHandle)
   
*Initializes the FLEXSPI handle for transfer which is used in transactional functions and set the callback.*
- void `FLEXSPI_TransferUpdateSizeEDMA` (FLEXSPI\_Type \*base, flexspi\_edma\_handle\_t \*handle, `flexspi_edma_transfer_nsize_t` nsize)
   
*Update FLEXSPI EDMA transfer source data transfer size(SSIZE) and destination data transfer size(DSIZE).*
- `status_t FLEXSPI_TransferEDMA` (FLEXSPI\_Type \*base, flexspi\_edma\_handle\_t \*handle, `flexspi_transfer_t` \*xfer)
   
*Transfers FLEXSPI data using an eDMA non-blocking method.*

- void **FLEXSPI\_TransferAbortEDMA** (FLEXSPI\_Type \*base, flexspi\_edma\_handle\_t \*handle)  
*Aborts the transfer data using eDMA.*
- status\_t **FLEXSPI\_TransferGetTransferCountEDMA** (FLEXSPI\_Type \*base, flexspi\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets the transferred counts of transfer.*

## 26.7.2 Data Structure Documentation

### 26.7.2.1 struct \_flexspi\_edma\_handle

#### Data Fields

- **edma\_handle\_t \* txDmaHandle**  
*eDMA handler for FLEXSPI Tx.*
- **edma\_handle\_t \* rxDmaHandle**  
*eDMA handler for FLEXSPI Rx.*
- **size\_t transferSize**  
*Bytes need to transfer.*
- **flexspi\_edma\_transfer\_nsize\_t nsize**  
*eDMA SSIZE/DSIZE in each transfer.*
- **uint8\_t nbytes**  
*eDMA minor byte transfer count initially configured.*
- **uint8\_t count**  
*The transfer data count in a DMA request.*
- **uint32\_t state**  
*Internal state for FLEXSPI eDMA transfer.*
- **flexspi\_edma\_callback\_t completionCallback**  
*A callback function called after the eDMA transfer is finished.*
- **void \* userData**  
*User callback parameter.*

## Field Documentation

- (1) `edma_handle_t* flexspi_edma_handle_t::txDmaHandle`
- (2) `edma_handle_t* flexspi_edma_handle_t::rxDmaHandle`
- (3) `size_t flexspi_edma_handle_t::transferSize`
- (4) `flexspi_edma_transfer_nsize_t flexspi_edma_handle_t::nsize`
- (5) `uint8_t flexspi_edma_handle_t:: nbytes`
- (6) `uint8_t flexspi_edma_handle_t::count`
- (7) `uint32_t flexspi_edma_handle_t::state`
- (8) `flexspi_edma_callback_t flexspi_edma_handle_t::completionCallback`

### 26.7.3 Macro Definition Documentation

**26.7.3.1 #define FSL\_FLEXSPI\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 3, 3))**

### 26.7.4 Enumeration Type Documentation

#### 26.7.4.1 enum flexspi\_edma\_transfer\_nsize\_t

Enumerator

- kFLEXSPI\_EDMA\_N\_SIZE\_1Bytes* Source/Destination data transfer size is 1 byte every time.
- kFLEXSPI\_EDMA\_N\_SIZE\_2Bytes* Source/Destination data transfer size is 2 bytes every time.
- kFLEXSPI\_EDMA\_N\_SIZE\_4Bytes* Source/Destination data transfer size is 4 bytes every time.
- kFLEXSPI\_EDMA\_N\_SIZE\_8Bytes* Source/Destination data transfer size is 8 bytes every time.
- kFLEXSPI\_EDMA\_N\_SIZE\_32Bytes* Source/Destination data transfer size is 32 bytes every time.

### 26.7.5 Function Documentation

**26.7.5.1 void FLEXSPI\_TransferCreateHandleEDMA ( FLEXSPI\_Type \* base,  
                          flexspi\_edma\_handle\_t \* handle, flexspi\_edma\_callback\_t callback, void \*  
                          userData, edma\_handle\_t \* txDmaHandle, edma\_handle\_t \* rxDmaHandle )**

Parameters

---

<i>base</i>	FLEXSPI peripheral base address
<i>handle</i>	Pointer to flexspi_edma_handle_t structure
<i>callback</i>	FLEXSPI callback, NULL means no callback.
<i>userData</i>	User callback function data.
<i>txDmaHandle</i>	User requested DMA handle for TX DMA transfer.
<i>rxDmaHandle</i>	User requested DMA handle for RX DMA transfer.

#### 26.7.5.2 void FLEXSPI\_TransferUpdateSizeEDMA ( **FLEXSPI\_Type** \* *base*, **flexspi\_edma\_handle\_t** \* *handle*, **flexspi\_edma\_transfer\_nsize\_t** *nsize* )

Parameters

<i>base</i>	FLEXSPI peripheral base address
<i>handle</i>	Pointer to flexspi_edma_handle_t structure
<i>nsize</i>	FLEXSPI DMA transfer data transfer size(SSIZE/DSIZE), by default the size is kFLEXPSI_EDMAnSize1Bytes(one byte).

See Also

[flexspi\\_edma\\_transfer\\_nsize\\_t](#).

#### 26.7.5.3 status\_t FLEXSPI\_TransferEDMA ( **FLEXSPI\_Type** \* *base*, **flexspi\_edma\_handle\_t** \* *handle*, **flexspi\_transfer\_t** \* *xfer* )

This function writes/receives data to/from the FLEXSPI transmit/receive FIFO. This function is non-blocking.

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	Pointer to flexspi_edma_handle_t structure
<i>xfer</i>	FLEXSPI transfer structure.

Return values

<i>kStatus_FLEXSPI_Busy</i>	FLEXSPI is busy transfer.
<i>kStatus_InvalidArgument</i>	The watermark configuration is invalid, the watermark should be power of 2 to do successfully EDMA transfer.
<i>kStatus_Success</i>	FLEXSPI successfully start edma transfer.

#### 26.7.5.4 void FLEXSPI\_TransferAbortEDMA ( **FLEXSPI\_Type** \* *base*, **flexspi\_edma\_handle\_t** \* *handle* )

This function aborts the transfer data using eDMA.

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	Pointer to flexspi_edma_handle_t structure

#### 26.7.5.5 status\_t FLEXSPI\_TransferGetTransferCountEDMA ( **FLEXSPI\_Type** \* *base*, **flexspi\_edma\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	FLEXSPI peripheral base address.
<i>handle</i>	Pointer to flexspi_edma_handle_t structure.
<i>count</i>	Bytes transfer.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

# Chapter 27

## GPC: General Power Controller Driver

### 27.1 Overview

The MCUXpresso SDK provides a peripheral driver for the General Power Controller (GPC) module of MCUXpresso SDK devices.

API functions are provided to configure the system about working in dedicated power mode. There are mainly about enabling the power for memory, enabling the wakeup sources for STOP modes, and power up/down operations for various peripherals.

### Functions

- void [GPC\\_EnableIRQ](#) (GPC\_Type \*base, uint32\_t irqId)  
*Enable the IRQ.*
- void [GPC\\_DisableIRQ](#) (GPC\_Type \*base, uint32\_t irqId)  
*Disable the IRQ.*
- bool [GPC\\_GetIRQStatusFlag](#) (GPC\_Type \*base, uint32\_t irqId)  
*Get the IRQ/Event flag.*
- static void [GPC\\_RequestPdram0PowerDown](#) (GPC\_Type \*base, bool enable)  
*FLEXRAM PDRAM0 Power Gate Enable.*
- static void [GPC\\_RequestMEGAPowerOn](#) (GPC\_Type \*base, bool enable)  
*Requests the MEGA power switch sequence.*

### Driver version

- #define [FSL\\_GPC\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 1, 1))  
*GPC driver version 2.1.1.*

### 27.2 Macro Definition Documentation

#### 27.2.1 #define [FSL\\_GPC\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 1, 1))

### 27.3 Function Documentation

#### 27.3.1 void [GPC\\_EnableIRQ](#) ( GPC\_Type \* *base*, uint32\_t *irqId* )

Parameters

---

<i>base</i>	GPC peripheral base address.
<i>irqId</i>	ID number of IRQ to be enabled, available range is 32-159. 0-31 is available in some platforms.

### 27.3.2 void GPC\_DisableIRQ ( GPC\_Type \* *base*, uint32\_t *irqId* )

Parameters

<i>base</i>	GPC peripheral base address.
<i>irqId</i>	ID number of IRQ to be disabled, available range is 32-159. 0-31 is available in some platforms.

### 27.3.3 bool GPC\_GetIRQStatusFlag ( GPC\_Type \* *base*, uint32\_t *irqId* )

Parameters

<i>base</i>	GPC peripheral base address.
<i>irqId</i>	ID number of IRQ to be enabled, available range is 32-159. 0-31 is available in some platforms.

Returns

Indicated IRQ/Event is asserted or not.

### 27.3.4 static void GPC\_RequestPdram0PowerDown ( GPC\_Type \* *base*, bool *enable* ) [inline], [static]

This function configures the FLEXRAM PDRAM0 if it will keep power when cpu core is power down. When the PDRAM0 Power is 1, PDRAM0 will be power down once when CPU core is power down. When the PDRAM0 Power is 0, PDRAM0 will keep power on even if CPU core is power down. When CPU core is re-power up, the default setting is 1.

Parameters

<i>base</i>	GPC peripheral base address.
<i>enable</i>	Enable the request or not.

**27.3.5 static void GPC\_RequestMEGAPowerOn ( GPC\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	GPC peripheral base address.
<i>enable</i>	Enable the power on sequence, or the power down sequence.

# Chapter 28

## GPT: General Purpose Timer

### 28.1 Overview

The MCUXpresso SDK provides a driver for the General Purpose Timer (GPT) of MCUXpresso SDK devices.

### 28.2 Function groups

The gpt driver supports the generation of PWM signals, input capture, and setting up the timer match conditions.

#### 28.2.1 Initialization and deinitialization

The function [GPT\\_Init\(\)](#) initializes the gpt with specified configurations. The function [GPT\\_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the restart/free-run mode and input selection when running.

The function [GPT\\_Deinit\(\)](#) stops the timer and turns off the module clock.

### 28.3 Typical use case

#### 28.3.1 GPT interrupt example

Set up a channel to trigger a periodic interrupt after every 1 second. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/gpt

## Data Structures

- struct [gpt\\_config\\_t](#)  
*Structure to configure the running mode. [More...](#)*

## Enumerations

- enum [gpt\\_clock\\_source\\_t](#) {  
    kGPT\_ClockSource\_Off = 0U,  
    kGPT\_ClockSource\_Periph = 1U,  
    kGPT\_ClockSource\_HighFreq = 2U,  
    kGPT\_ClockSource\_Ext = 3U,  
    kGPT\_ClockSource\_LowFreq = 4U,  
    kGPT\_ClockSource\_Osc = 5U }

*List of clock sources.*

- enum `gpt_input_capture_channel_t` {
   
  `kGPT_InputCapture_Channel1` = 0U,
   
  `kGPT_InputCapture_Channel2` = 1U }
   
*List of input capture channel number.*
  - enum `gpt_input_operation_mode_t` {
   
  `kGPT_InputOperation_Disabled` = 0U,
   
  `kGPT_InputOperation_RiseEdge` = 1U,
   
  `kGPT_InputOperation_FallEdge` = 2U,
   
  `kGPT_InputOperation_BothEdge` = 3U }
   
*List of input capture operation mode.*
  - enum `gpt_output_compare_channel_t` {
   
  `kGPT_OutputCompare_Channel1` = 0U,
   
  `kGPT_OutputCompare_Channel2` = 1U,
   
  `kGPT_OutputCompare_Channel3` = 2U }
   
*List of output compare channel number.*
  - enum `gpt_output_operation_mode_t` {
   
  `kGPT_OutputOperation_Disconnected` = 0U,
   
  `kGPT_OutputOperation_Toggle` = 1U,
   
  `kGPT_OutputOperation_Clear` = 2U,
   
  `kGPT_OutputOperation_Set` = 3U,
   
  `kGPT_OutputOperation_Activelow` = 4U }
   
*List of output compare operation mode.*
  - enum `gpt_interrupt_enable_t` {
   
  `kGPT_OutputCompare1InterruptEnable` = GPT\_IR\_OF1IE\_MASK,
   
  `kGPT_OutputCompare2InterruptEnable` = GPT\_IR\_OF2IE\_MASK,
   
  `kGPT_OutputCompare3InterruptEnable` = GPT\_IR\_OF3IE\_MASK,
   
  `kGPT_InputCapture1InterruptEnable` = GPT\_IR\_IF1IE\_MASK,
   
  `kGPT_InputCapture2InterruptEnable` = GPT\_IR\_IF2IE\_MASK,
   
  `kGPT_RollOverFlagInterruptEnable` = GPT\_IR\_ROVIE\_MASK }
   
*List of GPT interrupts.*
  - enum `gpt_status_flag_t` {
   
  `kGPT_OutputCompare1Flag` = GPT\_SR\_OF1\_MASK,
   
  `kGPT_OutputCompare2Flag` = GPT\_SR\_OF2\_MASK,
   
  `kGPT_OutputCompare3Flag` = GPT\_SR\_OF3\_MASK,
   
  `kGPT_InputCapture1Flag` = GPT\_SR\_IF1\_MASK,
   
  `kGPT_InputCapture2Flag` = GPT\_SR\_IF2\_MASK,
   
  `kGPT_RollOverFlag` = GPT\_SR\_ROV\_MASK }
- Status flag.*

## Driver version

- #define `FSL_GPT_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 4)`)

## Initialization and deinitialization

- void `GPT_Init` (GPT\_Type \*base, const `gpt_config_t` \*initConfig)
   
*Initialize GPT to reset state and initialize running mode.*

- void **GPT\_Deinit** (GPT\_Type \*base)  
*Disables the module and gates the GPT clock.*
- void **GPT\_GetDefaultConfig** (gpt\_config\_t \*config)  
*Fills in the GPT configuration structure with default settings.*

## Software Reset

- static void **GPT\_SoftwareReset** (GPT\_Type \*base)  
*Software reset of GPT module.*

## Clock source and frequency control

- static void **GPT\_SetClockSource** (GPT\_Type \*base, gpt\_clock\_source\_t gptClkSource)  
*Set clock source of GPT.*
- static gpt\_clock\_source\_t **GPT\_GetClockSource** (GPT\_Type \*base)  
*Get clock source of GPT.*
- static void **GPT\_SetClockDivider** (GPT\_Type \*base, uint32\_t divider)  
*Set pre scaler of GPT.*
- static uint32\_t **GPT\_GetClockDivider** (GPT\_Type \*base)  
*Get clock divider in GPT module.*
- static void **GPT\_SetOscClockDivider** (GPT\_Type \*base, uint32\_t divider)  
*OSC 24M pre-scaler before selected by clock source.*
- static uint32\_t **GPT\_GetOscClockDivider** (GPT\_Type \*base)  
*Get OSC 24M clock divider in GPT module.*

## Timer Start and Stop

- static void **GPT\_StartTimer** (GPT\_Type \*base)  
*Start GPT timer.*
- static void **GPT\_StopTimer** (GPT\_Type \*base)  
*Stop GPT timer.*

## Read the timer period

- static uint32\_t **GPT\_GetCurrentTimerCount** (GPT\_Type \*base)  
*Reads the current GPT counting value.*

## GPT Input/Output Signal Control

- static void **GPT\_SetInputOperationMode** (GPT\_Type \*base, gpt\_input\_capture\_channel\_t channel, gpt\_input\_operation\_mode\_t mode)  
*Set GPT operation mode of input capture channel.*
- static gpt\_input\_operation\_mode\_t **GPT\_GetInputOperationMode** (GPT\_Type \*base, gpt\_input\_capture\_channel\_t channel)  
*Get GPT operation mode of input capture channel.*
- static uint32\_t **GPT\_GetInputCaptureValue** (GPT\_Type \*base, gpt\_input\_capture\_channel\_t channel)  
*Get GPT input capture value of certain channel.*
- static void **GPT\_SetOutputOperationMode** (GPT\_Type \*base, gpt\_output\_compare\_channel\_t channel, gpt\_output\_operation\_mode\_t mode)

- static `gpt_output_operation_mode_t GPT_GetOutputOperationMode` (`GPT_Type *base, gpt_output_compare_channel_t channel`)
 

*Set GPT operation mode of output compare channel.*
- static `void GPT_SetOutputCompareValue` (`GPT_Type *base, gpt_output_compare_channel_t channel, uint32_t value`)
 

*Get GPT operation mode of output compare channel.*
- static `uint32_t GPT_GetOutputCompareValue` (`GPT_Type *base, gpt_output_compare_channel_t channel`)
 

*Set GPT output compare value of output compare channel.*
- static `void GPT_ForceOutput` (`GPT_Type *base, gpt_output_compare_channel_t channel`)
 

*Get GPT output compare value of output compare channel.*
- static void `GPT_ForceOutput` (`GPT_Type *base, gpt_output_compare_channel_t channel`)
 

*Force GPT output action on output compare channel, ignoring comparator.*

## GPT Interrupt and Status Interface

- static void `GPT_EnableInterrupts` (`GPT_Type *base, uint32_t mask`)
 

*Enables the selected GPT interrupts.*
- static void `GPT_DisableInterrupts` (`GPT_Type *base, uint32_t mask`)
 

*Disables the selected GPT interrupts.*
- static `uint32_t GPT_GetEnabledInterrupts` (`GPT_Type *base`)
 

*Gets the enabled GPT interrupts.*

## Status Interface

- static `uint32_t GPT_GetStatusFlags` (`GPT_Type *base, gpt_status_flag_t flags`)
 

*Get GPT status flags.*
- static void `GPT_ClearStatusFlags` (`GPT_Type *base, gpt_status_flag_t flags`)
 

*Clears the GPT status flags.*

## 28.4 Data Structure Documentation

### 28.4.1 struct gpt\_config\_t

#### Data Fields

- `gpt_clock_source_t clockSource`

*clock source for GPT module.*
- `uint32_t divider`

*clock divider (prescaler+1) from clock source to counter.*
- `bool enableFreeRun`

*true: FreeRun mode, false: Restart mode.*
- `bool enableRunInWait`

*GPT enabled in wait mode.*
- `bool enableRunInStop`

*GPT enabled in stop mode.*
- `bool enableRunInDoze`

*GPT enabled in doze mode.*
- `bool enableRunInDbg`

*GPT enabled in debug mode.*

- bool `enableMode`

*true:* counter reset to 0 when enabled;  
*false:* counter retain its value when enabled.

**Field Documentation**

- (1) `gpt_clock_source_t gpt_config_t::clockSource`
- (2) `uint32_t gpt_config_t::divider`
- (3) `bool gpt_config_t::enableFreeRun`
- (4) `bool gpt_config_t::enableRunInWait`
- (5) `bool gpt_config_t::enableRunInStop`
- (6) `bool gpt_config_t::enableRunInDoze`
- (7) `bool gpt_config_t::enableRunInDbg`
- (8) `bool gpt_config_t::enableMode`

**28.5 Enumeration Type Documentation****28.5.1 enum gpt\_clock\_source\_t**

## Note

Actual number of clock sources is SoC dependent

## Enumerator

- kGPT\_ClockSource\_Off* GPT Clock Source Off.
- kGPT\_ClockSource\_Periph* GPT Clock Source from Peripheral Clock.
- kGPT\_ClockSource\_HighFreq* GPT Clock Source from High Frequency Reference Clock.
- kGPT\_ClockSource\_Ext* GPT Clock Source from external pin.
- kGPT\_ClockSource\_LowFreq* GPT Clock Source from Low Frequency Reference Clock.
- kGPT\_ClockSource\_Osc* GPT Clock Source from Crystal oscillator.

**28.5.2 enum gpt\_input\_capture\_channel\_t**

## Enumerator

- kGPT\_InputCapture\_Channel1* GPT Input Capture Channel1.
- kGPT\_InputCapture\_Channel2* GPT Input Capture Channel2.

### 28.5.3 enum gpt\_input\_operation\_mode\_t

Enumerator

*kGPT\_InputOperation\_Disabled* Don't capture.

*kGPT\_InputOperation\_RiseEdge* Capture on rising edge of input pin.

*kGPT\_InputOperation\_FallEdge* Capture on falling edge of input pin.

*kGPT\_InputOperation\_BothEdge* Capture on both edges of input pin.

### 28.5.4 enum gpt\_output\_compare\_channel\_t

Enumerator

*kGPT\_OutputCompare\_Channel1* Output Compare Channel1.

*kGPT\_OutputCompare\_Channel2* Output Compare Channel2.

*kGPT\_OutputCompare\_Channel3* Output Compare Channel3.

### 28.5.5 enum gpt\_output\_operation\_mode\_t

Enumerator

*kGPT\_OutputOperation\_Disconnected* Don't change output pin.

*kGPT\_OutputOperation\_Toggle* Toggle output pin.

*kGPT\_OutputOperation\_Clear* Set output pin low.

*kGPT\_OutputOperation\_Set* Set output pin high.

*kGPT\_OutputOperation\_Activelow* Generate a active low pulse on output pin.

### 28.5.6 enum gpt\_interrupt\_enable\_t

Enumerator

*kGPT\_OutputCompare1InterruptEnable* Output Compare Channel1 interrupt enable.

*kGPT\_OutputCompare2InterruptEnable* Output Compare Channel2 interrupt enable.

*kGPT\_OutputCompare3InterruptEnable* Output Compare Channel3 interrupt enable.

*kGPT\_InputCapture1InterruptEnable* Input Capture Channel1 interrupt enable.

*kGPT\_InputCapture2InterruptEnable* Input Capture Channell1 interrupt enable.

*kGPT\_RollOverFlagInterruptEnable* Counter rolled over interrupt enable.

### 28.5.7 enum gpt\_status\_flag\_t

Enumerator

- kGPT\_OutputCompare1Flag* Output compare channel 1 event.
- kGPT\_OutputCompare2Flag* Output compare channel 2 event.
- kGPT\_OutputCompare3Flag* Output compare channel 3 event.
- kGPT\_InputCapture1Flag* Input Capture channel 1 event.
- kGPT\_InputCapture2Flag* Input Capture channel 2 event.
- kGPT\_RollOverFlag* Counter reaches maximum value and rolled over to 0 event.

## 28.6 Function Documentation

### 28.6.1 void GPT\_Init ( *GPT\_Type* \* *base*, *const gpt\_config\_t* \* *initConfig* )

Parameters

<i>base</i>	GPT peripheral base address.
<i>initConfig</i>	GPT mode setting configuration.

### 28.6.2 void GPT\_Deinit ( *GPT\_Type* \* *base* )

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

### 28.6.3 void GPT\_GetDefaultConfig ( *gpt\_config\_t* \* *config* )

The default values are:

```
* config->clockSource = kGPT_ClockSource_Periph;
* config->divider = 1U;
* config->enableRunInStop = true;
* config->enableRunInWait = true;
* config->enableRunInDoze = false;
* config->enableRunInDbg = false;
* config->enableFreeRun = false;
* config->enableMode = true;
*
```

Parameters

<i>config</i>	Pointer to the user configuration structure.
---------------	--

#### 28.6.4 static void GPT\_SoftwareReset ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

#### 28.6.5 static void GPT\_SetClockSource ( **GPT\_Type** \* *base*, **gpt\_clock\_source\_t** *gptClkSource* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>gptClkSource</i>	Clock source (see <a href="#">gpt_clock_source_t</a> typedef enumeration).

#### 28.6.6 static **gpt\_clock\_source\_t** GPT\_GetClockSource ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

clock source (see [gpt\\_clock\\_source\\_t](#) typedef enumeration).

#### 28.6.7 static void GPT\_SetClockDivider ( **GPT\_Type** \* *base*, **uint32\_t** *divider* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>divider</i>	Divider of GPT (1-4096).

### 28.6.8 static uint32\_t GPT\_GetClockDivider ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

clock divider in GPT module (1-4096).

### 28.6.9 static void GPT\_SetOscClockDivider ( **GPT\_Type** \* *base*, uint32\_t *divider* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>divider</i>	OSC Divider(1-16).

### 28.6.10 static uint32\_t GPT\_GetOscClockDivider ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

OSC clock divider in GPT module (1-16).

### 28.6.11 static void GPT\_StartTimer ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

### 28.6.12 static void GPT\_StopTimer ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

### 28.6.13 static uint32\_t GPT\_GetCurrentTimerCount ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
-------------	------------------------------

Returns

Current GPT counter value.

### 28.6.14 static void GPT\_SetInputOperationMode ( **GPT\_Type** \* *base*, **gpt\_input\_capture\_channel\_t** *channel*, **gpt\_input\_operation\_mode\_t** *mode* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT capture channel (see <a href="#">gpt_input_capture_channel_t</a> typedef enumeration).
<i>mode</i>	GPT input capture operation mode (see <a href="#">gpt_input_operation_mode_t</a> typedef enumeration).

### 28.6.15 static **gpt\_input\_operation\_mode\_t** GPT\_GetInputOperationMode ( **GPT\_Type** \* *base*, **gpt\_input\_capture\_channel\_t** *channel* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT capture channel (see <a href="#">gpt_input_capture_channel_t</a> typedef enumeration).

Returns

GPT input capture operation mode (see [gpt\\_input\\_operation\\_mode\\_t](#) typedef enumeration).

### 28.6.16 static uint32\_t GPT\_GetInputCaptureValue ( **GPT\_Type** \* *base*, **gpt\_input\_capture\_channel\_t** *channel* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT capture channel (see <a href="#">gpt_input_capture_channel_t</a> typedef enumeration).

Returns

GPT input capture value.

### 28.6.17 static void GPT\_SetOutputOperationMode ( **GPT\_Type** \* *base*, **gpt\_output\_compare\_channel\_t** *channel*, **gpt\_output\_operation\_mode\_t** *mode* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration).
<i>mode</i>	GPT output operation mode (see <a href="#">gpt_output_operation_mode_t</a> typedef enumeration).

### 28.6.18 static **gpt\_output\_operation\_mode\_t** GPT\_GetOutputOperationMode ( **GPT\_Type** \* *base*, **gpt\_output\_compare\_channel\_t** *channel* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration).

Returns

GPT output operation mode (see [gpt\\_output\\_operation\\_mode\\_t](#) typedef enumeration).

**28.6.19 static void GPT\_SetOutputCompareValue ( GPT\_Type \* *base*, gpt\_output\_compare\_channel\_t *channel*, uint32\_t *value* ) [inline], [static]**

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration).
<i>value</i>	GPT output compare value.

**28.6.20 static uint32\_t GPT\_GetOutputCompareValue ( GPT\_Type \* *base*, gpt\_output\_compare\_channel\_t *channel* ) [inline], [static]**

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration).

Returns

GPT output compare value.

**28.6.21 static void GPT\_ForceOutput ( GPT\_Type \* *base*, gpt\_output\_compare\_channel\_t *channel* ) [inline], [static]**

Parameters

<i>base</i>	GPT peripheral base address.
<i>channel</i>	GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration).

### 28.6.22 static void GPT\_EnableInterrupts ( *GPT\_Type* \* *base*, *uint32\_t* *mask* ) [[inline](#)], [[static](#)]

Parameters

<i>base</i>	GPT peripheral base address.
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">gpt_interrupt_enable_t</a>

### 28.6.23 static void GPT\_DisableInterrupts ( *GPT\_Type* \* *base*, *uint32\_t* *mask* ) [[inline](#)], [[static](#)]

Parameters

<i>base</i>	GPT peripheral base address
<i>mask</i>	The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">gpt_interrupt_enable_t</a>

### 28.6.24 static *uint32\_t* GPT\_GetEnabledInterrupts ( *GPT\_Type* \* *base* ) [[inline](#)], [[static](#)]

Parameters

<i>base</i>	GPT peripheral base address
-------------	-----------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [gpt\\_interrupt\\_enable\\_t](#)

### 28.6.25 static *uint32\_t* GPT\_GetStatusFlags ( *GPT\_Type* \* *base*, *gpt\_status\_flag\_t* *flags* ) [[inline](#)], [[static](#)]

Parameters

<i>base</i>	GPT peripheral base address.
<i>flags</i>	GPT status flag mask (see <a href="#">gpt_status_flag_t</a> for bit definition).

Returns

GPT status, each bit represents one status flag.

### 28.6.26 static void GPT\_ClearStatusFlags ( GPT\_Type \* *base*, gpt\_status\_flag\_t *flags* ) [inline], [static]

Parameters

<i>base</i>	GPT peripheral base address.
<i>flags</i>	GPT status flag mask (see <a href="#">gpt_status_flag_t</a> for bit definition).

# Chapter 29

## GPIO: General-Purpose Input/Output Driver

### 29.1 Overview

The MCUXpresso SDK provides a peripheral driver for the General-Purpose Input/Output (GPIO) module of MCUXpresso SDK devices.

### 29.2 Typical use case

#### 29.2.1 Input Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/gpio

### Data Structures

- struct `gpio_pin_config_t`  
*GPIO Init structure definition.* [More...](#)

### Enumerations

- enum `gpio_pin_direction_t` {  
  `kGPIO_DigitalInput` = 0U,  
  `kGPIO_DigitalOutput` = 1U }  
*GPIO direction definition.*
- enum `gpio_interrupt_mode_t` {  
  `kGPIO_NoIntmode` = 0U,  
  `kGPIO_IntLowLevel` = 1U,  
  `kGPIO_IntHighLevel` = 2U,  
  `kGPIO_IntRisingEdge` = 3U,  
  `kGPIO_IntFallingEdge` = 4U,  
  `kGPIO_IntRisingOrFallingEdge` = 5U }  
*GPIO interrupt mode definition.*

### Driver version

- #define `FSL_GPIO_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 6)`)  
*GPIO driver version.*

### GPIO Initialization and Configuration functions

- void `GPIO_PinInit` (`GPIO_Type *base`, `uint32_t pin`, const `gpio_pin_config_t *Config`)  
*Initializes the GPIO peripheral according to the specified parameters in the initConfig.*

## GPIO Reads and Write Functions

- void **GPIO\_PinWrite** (GPIO\_Type \*base, uint32\_t pin, uint8\_t output)  
*Sets the output level of the individual GPIO pin to logic 1 or 0.*
- static void **GPIO\_WritePinOutput** (GPIO\_Type \*base, uint32\_t pin, uint8\_t output)  
*Sets the output level of the individual GPIO pin to logic 1 or 0.*
- static void **GPIO\_PortSet** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 1.*
- static void **GPIO\_SetPinsOutput** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 1.*
- static void **GPIO\_PortClear** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 0.*
- static void **GPIO\_ClearPinsOutput** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 0.*
- static void **GPIO\_PortToggle** (GPIO\_Type \*base, uint32\_t mask)  
*Reverses the current output logic of the multiple GPIO pins.*
- static uint32\_t **GPIO\_PinRead** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current input value of the GPIO port.*
- static uint32\_t **GPIO\_ReadPinInput** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current input value of the GPIO port.*

## GPIO Reads Pad Status Functions

- static uint8\_t **GPIO\_PinReadPadStatus** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current GPIO pin pad status.*
- static uint8\_t **GPIO\_ReadPadStatus** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current GPIO pin pad status.*

## Interrupts and flags management functions

- void **GPIO\_PinSetInterruptConfig** (GPIO\_Type \*base, uint32\_t pin, gpio\_interrupt\_mode\_t pinInterruptMode)  
*Sets the current pin interrupt mode.*
- static void **GPIO\_SetPinInterruptConfig** (GPIO\_Type \*base, uint32\_t pin, gpio\_interrupt\_mode\_t pinInterruptMode)  
*Sets the current pin interrupt mode.*
- static void **GPIO\_PortEnableInterrupts** (GPIO\_Type \*base, uint32\_t mask)  
*Enables the specific pin interrupt.*
- static void **GPIO\_EnableInterrupts** (GPIO\_Type \*base, uint32\_t mask)  
*Enables the specific pin interrupt.*
- static void **GPIO\_PortDisableInterrupts** (GPIO\_Type \*base, uint32\_t mask)  
*Disables the specific pin interrupt.*
- static void **GPIO\_DisableInterrupts** (GPIO\_Type \*base, uint32\_t mask)  
*Disables the specific pin interrupt.*
- static uint32\_t **GPIO\_PortGetInterruptFlags** (GPIO\_Type \*base)  
*Reads individual pin interrupt status.*
- static uint32\_t **GPIO\_GetPinsInterruptFlags** (GPIO\_Type \*base)  
*Reads individual pin interrupt status.*
- static void **GPIO\_PortClearInterruptFlags** (GPIO\_Type \*base, uint32\_t mask)  
*Clears pin interrupt flag.*
- static void **GPIO\_ClearPinsInterruptFlags** (GPIO\_Type \*base, uint32\_t mask)

*Clears pin interrupt flag.*

## 29.3 Data Structure Documentation

### 29.3.1 struct gpio\_pin\_config\_t

#### Data Fields

- `gpio_pin_direction_t direction`  
*Specifies the pin direction.*
- `uint8_t outputLogic`  
*Set a default output logic, which has no use in input.*
- `gpio_interrupt_mode_t interruptMode`  
*Specifies the pin interrupt mode, a value of `gpio_interrupt_mode_t`.*

#### Field Documentation

(1) `gpio_pin_direction_t gpio_pin_config_t::direction`

(2) `gpio_interrupt_mode_t gpio_pin_config_t::interruptMode`

## 29.4 Macro Definition Documentation

29.4.1 `#define FSL_GPIO_DRIVER_VERSION (MAKE_VERSION(2, 0, 6))`

## 29.5 Enumeration Type Documentation

### 29.5.1 enum gpio\_pin\_direction\_t

Enumerator

***kGPIO\_DigitalInput*** Set current pin as digital input.

***kGPIO\_DigitalOutput*** Set current pin as digital output.

### 29.5.2 enum gpio\_interrupt\_mode\_t

Enumerator

***kGPIO\_NoIntmode*** Set current pin general IO functionality.

***kGPIO\_IntLowLevel*** Set current pin interrupt is low-level sensitive.

***kGPIO\_IntHighLevel*** Set current pin interrupt is high-level sensitive.

***kGPIO\_IntRisingEdge*** Set current pin interrupt is rising-edge sensitive.

***kGPIO\_IntFallingEdge*** Set current pin interrupt is falling-edge sensitive.

***kGPIO\_IntRisingOrFallingEdge*** Enable the edge select bit to override the ICR register's configuration.

## 29.6 Function Documentation

29.6.1 `void GPIO_PinInit ( GPIO_Type * base, uint32_t pin, const gpio_pin_config_t * Config )`

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	Specifies the pin number
<i>Config</i>	pointer to a <a href="#">gpio_pin_config_t</a> structure that contains the configuration information.

## 29.6.2 void GPIO\_PinWrite ( **GPIO\_Type** \* *base*, **uint32\_t** *pin*, **uint8\_t** *output* )

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.
<i>output</i>	GPIOin output logic level. <ul style="list-style-type: none"> <li>• 0: corresponding pin output low-logic level.</li> <li>• 1: corresponding pin output high-logic level.</li> </ul>

## 29.6.3 static void GPIO\_WritePinOutput ( **GPIO\_Type** \* *base*, **uint32\_t** *pin*, **uint8\_t** *output* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinWrite](#).

## 29.6.4 static void GPIO\_PortSet ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
<i>mask</i>	GPIO pin number macro

## 29.6.5 static void GPIO\_SetPinsOutput ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PortSet](#).

29.6.6 **static void GPIO\_PortClear ( GPIO\_Type \* *base*, uint32\_t *mask* )**  
[**inline**], [**static**]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
<i>mask</i>	GPIO pin number macro

**29.6.7 static void GPIO\_ClearPinsOutput ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* )  
[inline], [static]**

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PortClear](#).

**29.6.8 static void GPIO\_PortToggle ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* )  
[inline], [static]**

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.)
<i>mask</i>	GPIO pin number macro

**29.6.9 static uint32\_t GPIO\_PinRead ( **GPIO\_Type** \* *base*, **uint32\_t** *pin* )  
[inline], [static]**

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.

Return values

<i>GPIO</i>	port input value.
-------------	-------------------

**29.6.10 static uint32\_t GPIO\_ReadPinInput ( **GPIO\_Type** \* *base*, **uint32\_t** *pin* )  
[inline], [static]**

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinRead](#).

29.6.11 **static uint8\_t GPIO\_PinReadPadStatus ( GPIO\_Type \* *base*, uint32\_t *pin* )**  
[**inline**], [**static**]

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.

Return values

<i>GPIO</i>	pin pad status value.
-------------	-----------------------

### 29.6.12 static uint8\_t GPIO\_ReadPadStatus ( *GPIO\_Type* \* *base*, *uint32\_t* *pin* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinReadPadStatus](#).

### 29.6.13 void GPIO\_PinSetInterruptConfig ( *GPIO\_Type* \* *base*, *uint32\_t* *pin*, *gpio\_interrupt\_mode\_t* *pinInterruptMode* )

Parameters

<i>base</i>	GPIO base pointer.
<i>pin</i>	GPIO port pin number.
<i>pinInterrupt-Mode</i>	pointer to a <a href="#">gpio_interrupt_mode_t</a> structure that contains the interrupt mode information.

### 29.6.14 static void GPIO\_SetPinInterruptConfig ( *GPIO\_Type* \* *base*, *uint32\_t* *pin*, *gpio\_interrupt\_mode\_t* *pinInterruptMode* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinSetInterruptConfig](#).

### 29.6.15 static void GPIO\_PortEnableInterrupts ( *GPIO\_Type* \* *base*, *uint32\_t* *mask* ) [inline], [static]

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

**29.6.16 static void GPIO\_EnableInterrupts ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

**29.6.17 static void GPIO\_PortDisableInterrupts ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

**29.6.18 static void GPIO\_DisableInterrupts ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PortDisableInterrupts](#).

**29.6.19 static uint32\_t GPIO\_PortGetInterruptFlags ( GPIO\_Type \* *base* )  
[inline], [static]**

Parameters

---

<i>base</i>	GPIO base pointer.
-------------	--------------------

Return values

<i>current</i>	pin interrupt status flag.
----------------	----------------------------

### 29.6.20 static uint32\_t GPIO\_GetPinsInterruptFlags ( **GPIO\_Type** \* *base* ) [**inline**], [**static**]

Parameters

<i>base</i>	GPIO base pointer.
-------------	--------------------

Return values

<i>current</i>	pin interrupt status flag.
----------------	----------------------------

### 29.6.21 static void GPIO\_PortClearInterruptFlags ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

### 29.6.22 static void GPIO\_ClearPinsInterruptFlags ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

<i>base</i>	GPIO base pointer.
<i>mask</i>	GPIO pin number macro.

# Chapter 30

## LPI2C: Low Power Inter-Integrated Circuit Driver

### 30.1 Overview

#### Modules

- LPI2C CMSIS Driver
- LPI2C FreeRTOS Driver
- LPI2C Master DMA Driver
- LPI2C Master Driver
- LPI2C Slave Driver

#### Macros

- #define `I2C_RETRY_TIMES` 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*

#### Enumerations

- enum {  
    `kStatus_LPI2C_Busy` = MAKE\_STATUS(kStatusGroup\_LPI2C, 0),  
    `kStatus_LPI2C_Idle` = MAKE\_STATUS(kStatusGroup\_LPI2C, 1),  
    `kStatus_LPI2C_Nak` = MAKE\_STATUS(kStatusGroup\_LPI2C, 2),  
    `kStatus_LPI2C_FifoError` = MAKE\_STATUS(kStatusGroup\_LPI2C, 3),  
    `kStatus_LPI2C_BitError` = MAKE\_STATUS(kStatusGroup\_LPI2C, 4),  
    `kStatus_LPI2C_ArbitrationLost` = MAKE\_STATUS(kStatusGroup\_LPI2C, 5),  
    `kStatus_LPI2C_PinLowTimeout`,  
    `kStatus_LPI2C_NoTransferInProgress`,  
    `kStatus_LPI2C_DmaRequestFail` = MAKE\_STATUS(kStatusGroup\_LPI2C, 8),  
    `kStatus_LPI2C_Timeout` = MAKE\_STATUS(kStatusGroup\_LPI2C, 9) }  
*LPI2C status return codes.*

#### Driver version

- #define `FSL_LPI2C_DRIVER_VERSION` (MAKE\_VERSION(2, 5, 0))  
*LPI2C driver version.*

## 30.2 Macro Definition Documentation

30.2.1 `#define FSL_LPI2C_DRIVER_VERSION (MAKE_VERSION(2, 5, 0))`

30.2.2 `#define I2C_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`

## 30.3 Enumeration Type Documentation

### 30.3.1 anonymous enum

Enumerator

*kStatus\_LPI2C\_Busy* The master is already performing a transfer.

*kStatus\_LPI2C\_Idle* The slave driver is idle.

*kStatus\_LPI2C\_Nak* The slave device sent a NAK in response to a byte.

*kStatus\_LPI2C\_FifoError* FIFO under run or overrun.

*kStatus\_LPI2C\_BitError* Transferred bit was not seen on the bus.

*kStatus\_LPI2C\_ArbitrationLost* Arbitration lost error.

*kStatus\_LPI2C\_PinLowTimeout* SCL or SDA were held low longer than the timeout.

*kStatus\_LPI2C\_NoTransferInProgress* Attempt to abort a transfer when one is not in progress.

*kStatus\_LPI2C\_DmaRequestFail* DMA request failed.

*kStatus\_LPI2C\_Timeout* Timeout polling status flags.

## 30.4 LPI2C Master Driver

### 30.4.1 Overview

#### Data Structures

- struct `lpi2c_master_config_t`  
*Structure with settings to initialize the LPI2C master module. [More...](#)*
- struct `lpi2c_data_match_config_t`  
*LPI2C master data match configuration structure. [More...](#)*
- struct `lpi2c_master_transfer_t`  
*Non-blocking transfer descriptor structure. [More...](#)*
- struct `lpi2c_master_handle_t`  
*Driver handle for master non-blocking APIs. [More...](#)*

#### Typedefs

- typedef void(\* `lpi2c_master_transfer_callback_t` )(LPI2C\_Type \*base, `lpi2c_master_handle_t` \*handle, `status_t` completionStatus, void \*userData)  
*Master completion callback function pointer type.*
- typedef void(\* `lpi2c_master_isr_t` )(LPI2C\_Type \*base, void \*handle)  
*Typedef for master interrupt handler, used internally for LPI2C master interrupt and EDMA transactional APIs.*

#### Enumerations

- enum `_lpi2c_master_flags` {
   
`kLPI2C_MasterTxReadyFlag` = LPI2C\_MSR\_TDF\_MASK,  
`kLPI2C_MasterRxReadyFlag` = LPI2C\_MSR\_RDF\_MASK,  
`kLPI2C_MasterEndOfPacketFlag` = LPI2C\_MSR\_EPF\_MASK,  
`kLPI2C_MasterStopDetectFlag` = LPI2C\_MSR\_SDF\_MASK,  
`kLPI2C_MasterNackDetectFlag` = LPI2C\_MSR\_NDF\_MASK,  
`kLPI2C_MasterArbitrationLostFlag` = LPI2C\_MSR\_ALF\_MASK,  
`kLPI2C_MasterFifoErrFlag` = LPI2C\_MSR\_FEF\_MASK,  
`kLPI2C_MasterPinLowTimeoutFlag` = LPI2C\_MSR\_PLTF\_MASK,  
`kLPI2C_MasterDataMatchFlag` = LPI2C\_MSR\_DMF\_MASK,  
`kLPI2C_MasterBusyFlag` = LPI2C\_MSR\_MBF\_MASK,  
`kLPI2C_MasterBusBusyFlag` = LPI2C\_MSR\_BBF\_MASK,  
`kLPI2C_MasterClearFlags`,  
`kLPI2C_MasterIrqFlags`,  
`kLPI2C_MasterErrorFlags` }
   
*LPI2C master peripheral flags.*
- enum `lpi2c_direction_t` {
   
`kLPI2C_Write` = 0U,  
`kLPI2C_Read` = 1U }

- *Direction of master and slave transfers.*
- enum `lpi2c_master_pin_config_t` {
   
  `kLPI2C_2PinOpenDrain` = 0x0U,
   
  `kLPI2C_2PinOutputOnly` = 0x1U,
   
  `kLPI2C_2PinPushPull` = 0x2U,
   
  `kLPI2C_4PinPushPull` = 0x3U,
   
  `kLPI2C_2PinOpenDrainWithSeparateSlave`,
   
  `kLPI2C_2PinOutputOnlyWithSeparateSlave`,
   
  `kLPI2C_2PinPushPullWithSeparateSlave`,
   
  `kLPI2C_4PinPushPullWithInvertedOutput` = 0x7U }
- LPI2C pin configuration.*
- enum `lpi2c_host_request_source_t` {
   
  `kLPI2C_HostRequestExternalPin` = 0x0U,
   
  `kLPI2C_HostRequestInputTrigger` = 0x1U }
- LPI2C master host request selection.*
- enum `lpi2c_host_request_polarity_t` {
   
  `kLPI2C_HostRequestPinActiveLow` = 0x0U,
   
  `kLPI2C_HostRequestPinActiveHigh` = 0x1U }
- LPI2C master host request pin polarity configuration.*
- enum `lpi2c_data_match_config_mode_t` {
   
  `kLPI2C_MatchDisabled` = 0x0U,
   
  `kLPI2C_1stWordEqualsM0OrM1` = 0x2U,
   
  `kLPI2C_AnyWordEqualsM0OrM1` = 0x3U,
   
  `kLPI2C_1stWordEqualsM0And2ndWordEqualsM1`,
   
  `kLPI2C_AnyWordEqualsM0AndNextWordEqualsM1`,
   
  `kLPI2C_1stWordAndM1EqualsM0AndM1`,
   
  `kLPI2C_AnyWordAndM1EqualsM0AndM1` }
- LPI2C master data match configuration modes.*
- enum `_lpi2c_master_transfer_flags` {
   
  `kLPI2C_TransferDefaultFlag` = 0x00U,
   
  `kLPI2C_TransferNoStartFlag` = 0x01U,
   
  `kLPI2C_TransferRepeatedStartFlag` = 0x02U,
   
  `kLPI2C_TransferNoStopFlag` = 0x04U }
- Transfer option flags.*

## Initialization and deinitialization

- void `LPI2C_MasterGetDefaultConfig` (`lpi2c_master_config_t` \*`masterConfig`)
   
    *Provides a default configuration for the LPI2C master peripheral.*
- void `LPI2C_MasterInit` (`LPI2C_Type` \*`base`, const `lpi2c_master_config_t` \*`masterConfig`, `uint32_t` `sourceClock_Hz`)
   
    *Initializes the LPI2C master peripheral.*
- void `LPI2C_MasterDeinit` (`LPI2C_Type` \*`base`)
   
    *Deinitializes the LPI2C master peripheral.*
- void `LPI2C_MasterConfigureDataMatch` (`LPI2C_Type` \*`base`, const `lpi2c_data_match_config_t` \*`matchConfig`)

*Configures LPI2C master data match feature.*

- **status\_t LPI2C\_MasterCheckAndClearError** (LPI2C\_Type \*base, uint32\_t status)
- **status\_t LPI2C\_CheckForBusyBus** (LPI2C\_Type \*base)
- static void **LPI2C\_MasterReset** (LPI2C\_Type \*base)

*Performs a software reset.*

- static void **LPI2C\_MasterEnable** (LPI2C\_Type \*base, bool enable)

*Enables or disables the LPI2C module as master.*

## Status

- static uint32\_t **LPI2C\_MasterGetStatusFlags** (LPI2C\_Type \*base)  
*Gets the LPI2C master status flags.*
- static void **LPI2C\_MasterClearStatusFlags** (LPI2C\_Type \*base, uint32\_t statusMask)  
*Clears the LPI2C master status flag state.*

## Interrupts

- static void **LPI2C\_MasterEnableInterrupts** (LPI2C\_Type \*base, uint32\_t interruptMask)  
*Enables the LPI2C master interrupt requests.*
- static void **LPI2C\_MasterDisableInterrupts** (LPI2C\_Type \*base, uint32\_t interruptMask)  
*Disables the LPI2C master interrupt requests.*
- static uint32\_t **LPI2C\_MasterGetEnabledInterrupts** (LPI2C\_Type \*base)  
*Returns the set of currently enabled LPI2C master interrupt requests.*

## DMA control

- static void **LPI2C\_MasterEnableDMA** (LPI2C\_Type \*base, bool enableTx, bool enableRx)  
*Enables or disables LPI2C master DMA requests.*
- static uint32\_t **LPI2C\_MasterGetTxFifoAddress** (LPI2C\_Type \*base)  
*Gets LPI2C master transmit data register address for DMA transfer.*
- static uint32\_t **LPI2C\_MasterGetRxFifoAddress** (LPI2C\_Type \*base)  
*Gets LPI2C master receive data register address for DMA transfer.*

## FIFO control

- static void **LPI2C\_MasterSetWatermarks** (LPI2C\_Type \*base, size\_t txWords, size\_t rxWords)  
*Sets the watermarks for LPI2C master FIFOs.*
- static void **LPI2C\_MasterGetFifoCounts** (LPI2C\_Type \*base, size\_t \*rxCount, size\_t \*txCount)  
*Gets the current number of words in the LPI2C master FIFOs.*

## Bus operations

- void **LPI2C\_MasterSetBaudRate** (LPI2C\_Type \*base, uint32\_t sourceClock\_Hz, uint32\_t baudRate\_Hz)

- Sets the I2C bus frequency for master transactions.
- static bool [LPI2C\\_MasterGetBusIdleState](#) (LPI2C\_Type \*base)  
Returns whether the bus is idle.
- [status\\_t LPI2C\\_MasterStart](#) (LPI2C\_Type \*base, uint8\_t address, [lpi2c\\_direction\\_t](#) dir)  
Sends a START signal and slave address on the I2C bus.
- static [status\\_t LPI2C\\_MasterRepeatedStart](#) (LPI2C\_Type \*base, uint8\_t address, [lpi2c\\_direction\\_t](#) dir)  
Sends a repeated START signal and slave address on the I2C bus.
- [status\\_t LPI2C\\_MasterSend](#) (LPI2C\_Type \*base, void \*txBuff, size\_t txSize)  
Performs a polling send transfer on the I2C bus.
- [status\\_t LPI2C\\_MasterReceive](#) (LPI2C\_Type \*base, void \*rxBuff, size\_t rxSize)  
Performs a polling receive transfer on the I2C bus.
- [status\\_t LPI2C\\_MasterStop](#) (LPI2C\_Type \*base)  
Sends a STOP signal on the I2C bus.
- [status\\_t LPI2C\\_MasterTransferBlocking](#) (LPI2C\_Type \*base, [lpi2c\\_master\\_transfer\\_t](#) \*transfer)  
Performs a master polling transfer on the I2C bus.

## Non-blocking

- void [LPI2C\\_MasterTransferCreateHandle](#) (LPI2C\_Type \*base, [lpi2c\\_master\\_handle\\_t](#) \*handle, [lpi2c\\_master\\_transfer\\_callback\\_t](#) callback, void \*userData)  
Creates a new handle for the LPI2C master non-blocking APIs.
- [status\\_t LPI2C\\_MasterTransferNonBlocking](#) (LPI2C\_Type \*base, [lpi2c\\_master\\_handle\\_t](#) \*handle, [lpi2c\\_master\\_transfer\\_t](#) \*transfer)  
Performs a non-blocking transaction on the I2C bus.
- [status\\_t LPI2C\\_MasterTransferGetCount](#) (LPI2C\_Type \*base, [lpi2c\\_master\\_handle\\_t](#) \*handle, size\_t \*count)  
Returns number of bytes transferred so far.
- void [LPI2C\\_MasterTransferAbort](#) (LPI2C\_Type \*base, [lpi2c\\_master\\_handle\\_t](#) \*handle)  
Terminates a non-blocking LPI2C master transmission early.

## IRQ handler

- void [LPI2C\\_MasterTransferHandleIRQ](#) (LPI2C\_Type \*base, void \*lpi2cMasterHandle)  
Reusable routine to handle master interrupts.

### 30.4.2 Data Structure Documentation

#### 30.4.2.1 struct lpi2c\_master\_config\_t

This structure holds configuration settings for the LPI2C peripheral. To initialize this structure to reasonable defaults, call the [LPI2C\\_MasterGetDefaultConfig\(\)](#) function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

## Data Fields

- bool `enableMaster`  
*Whether to enable master mode.*
  - bool `enableDoze`  
*Whether master is enabled in doze mode.*
  - bool `debugEnable`  
*Enable transfers to continue when halted in debug mode.*
  - bool `ignoreAck`  
*Whether to ignore ACK/NACK.*
  - `lpi2c_master_pin_config_t pinConfig`  
*The pin configuration option.*
  - `uint32_t baudRate_Hz`  
*Desired baud rate in Hertz.*
  - `uint32_t busIdleTimeout_ns`  
*Bus idle timeout in nanoseconds.*
  - `uint32_t pinLowTimeout_ns`  
*Pin low timeout in nanoseconds.*
  - `uint8_t sdaGlitchFilterWidth_ns`  
*Width in nanoseconds of glitch filter on SDA pin.*
  - `uint8_t sclGlitchFilterWidth_ns`  
*Width in nanoseconds of glitch filter on SCL pin.*
  - struct {
    - bool `enable`  
*Enable host request.*
    - `lpi2c_host_request_source_t source`  
*Host request source.*
    - `lpi2c_host_request_polarity_t polarity`  
*Host request pin polarity.*
} `hostRequest`
- Host request options.*

## Field Documentation

- (1) `bool lpi2c_master_config_t::enableMaster`
- (2) `bool lpi2c_master_config_t::enableDoze`
- (3) `bool lpi2c_master_config_t::debugEnable`
- (4) `bool lpi2c_master_config_t::ignoreAck`
- (5) `lpi2c_master_pin_config_t lpi2c_master_config_t::pinConfig`
- (6) `uint32_t lpi2c_master_config_t::baudRate_Hz`
- (7) `uint32_t lpi2c_master_config_t::busIdleTimeout_ns`

Set to 0 to disable.

(8) `uint32_t lpi2c_master_config_t::pinLowTimeout_ns`

Set to 0 to disable.

(9) `uint8_t lpi2c_master_config_t::sdaGlitchFilterWidth_ns`

Set to 0 to disable.

(10) `uint8_t lpi2c_master_config_t::sclGlitchFilterWidth_ns`

Set to 0 to disable.

(11) `bool lpi2c_master_config_t::enable`

(12) `lpi2c_host_request_source_t lpi2c_master_config_t::source`

(13) `lpi2c_host_request_polarity_t lpi2c_master_config_t::polarity`

(14) `struct { ... } lpi2c_master_config_t::hostRequest`

### 30.4.2.2 struct lpi2c\_data\_match\_config\_t

#### Data Fields

- `lpi2c_data_match_config_mode_t matchMode`  
*Data match configuration setting.*
- `bool rxDataMatchOnly`  
*When set to true, received data is ignored until a successful match.*
- `uint32_t match0`  
*Match value 0.*
- `uint32_t match1`  
*Match value 1.*

#### Field Documentation

(1) `lpi2c_data_match_config_mode_t lpi2c_data_match_config_t::matchMode`

(2) `bool lpi2c_data_match_config_t::rxDataMatchOnly`

(3) `uint32_t lpi2c_data_match_config_t::match0`

(4) `uint32_t lpi2c_data_match_config_t::match1`

### 30.4.2.3 struct \_lpi2c\_master\_transfer

This structure is used to pass transaction parameters to the [LPI2C\\_MasterTransferNonBlocking\(\)](#) API.

#### Data Fields

- `uint32_t flags`

- **uint16\_t slaveAddress**  
*The 7-bit slave address.*
- **lpi2c\_direction\_t direction**  
*Either `kLPI2C_Read` or `kLPI2C_Write`.*
- **uint32\_t subaddress**  
*Sub address.*
- **size\_t subaddressSize**  
*Length of sub address to send in bytes.*
- **void \* data**  
*Pointer to data to transfer.*
- **size\_t dataSize**  
*Number of bytes to transfer.*

## Field Documentation

(1) **uint32\_t lpi2c\_master\_transfer\_t::flags**

See enumeration `_lpi2c_master_transfer_flags` for available options. Set to 0 or `kLPI2C_TransferDefaultFlag` for normal transfers.

(2) **uint16\_t lpi2c\_master\_transfer\_t::slaveAddress**

(3) **lpi2c\_direction\_t lpi2c\_master\_transfer\_t::direction**

(4) **uint32\_t lpi2c\_master\_transfer\_t::subaddress**

Transferred MSB first.

(5) **size\_t lpi2c\_master\_transfer\_t::subaddressSize**

Maximum size is 4 bytes.

(6) **void\* lpi2c\_master\_transfer\_t::data**

(7) **size\_t lpi2c\_master\_transfer\_t::dataSize**

### 30.4.2.4 struct \_lpi2c\_master\_handle

Note

The contents of this structure are private and subject to change.

## Data Fields

- **uint8\_t state**  
*Transfer state machine current state.*
- **uint16\_t remainingBytes**  
*Remaining byte count in current state.*
- **uint8\_t \* buf**

- *Buffer pointer for current state.*
- `uint16_t commandBuffer [6]`  
*LPI2C command sequence.*
- `lpi2c_master_transfer_t transfer`  
*Copy of the current transfer info.*
- `lpi2c_master_transfer_callback_t completionCallback`  
*Callback function pointer.*
- `void *userData`  
*Application data passed to callback.*

## Field Documentation

- (1) `uint8_t lpi2c_master_handle_t::state`
- (2) `uint16_t lpi2c_master_handle_t::remainingBytes`
- (3) `uint8_t* lpi2c_master_handle_t::buf`
- (4) `uint16_t lpi2c_master_handle_t::commandBuffer[6]`

When all 6 command words are used: Start&addr&write[1 word] + subaddr[4 words] + restart&addr&read[1 word]

- (5) `lpi2c_master_transfer_t lpi2c_master_handle_t::transfer`
- (6) `lpi2c_master_transfer_callback_t lpi2c_master_handle_t::completionCallback`
- (7) `void* lpi2c_master_handle_t::userData`

## 30.4.3 Typedef Documentation

### 30.4.3.1 `typedef void(* lpi2c_master_transfer_callback_t)(LPI2C_Type *base, lpi2c_master_handle_t *handle, status_t completionStatus, void *userData)`

This callback is used only for the non-blocking master transfer API. Specify the callback you wish to use in the call to [LPI2C\\_MasterTransferCreateHandle\(\)](#).

Parameters

<code>base</code>	The LPI2C peripheral base address.
<code>completion-Status</code>	Either kStatus_Success or an error code describing how the transfer completed.

<i>userData</i>	Arbitrary pointer-sized value passed from the application.
-----------------	--

### 30.4.4 Enumeration Type Documentation

#### 30.4.4.1 enum \_lpi2c\_master\_flags

The following status register flags can be cleared:

- [kLPI2C\\_MasterEndOfPacketFlag](#)
- [kLPI2C\\_MasterStopDetectFlag](#)
- [kLPI2C\\_MasterNackDetectFlag](#)
- [kLPI2C\\_MasterArbitrationLostFlag](#)
- [kLPI2C\\_MasterFifoErrFlag](#)
- [kLPI2C\\_MasterPinLowTimeoutFlag](#)
- [kLPI2C\\_MasterDataMatchFlag](#)

All flags except [kLPI2C\\_MasterBusyFlag](#) and [kLPI2C\\_MasterBusBusyFlag](#) can be enabled as interrupts.

Note

These enums are meant to be OR'd together to form a bit mask.

Enumerator

- kLPI2C\_MasterTxReadyFlag* Transmit data flag.
- kLPI2C\_MasterRxReadyFlag* Receive data flag.
- kLPI2C\_MasterEndOfPacketFlag* End Packet flag.
- kLPI2C\_MasterStopDetectFlag* Stop detect flag.
- kLPI2C\_MasterNackDetectFlag* NACK detect flag.
- kLPI2C\_MasterArbitrationLostFlag* Arbitration lost flag.
- kLPI2C\_MasterFifoErrFlag* FIFO error flag.
- kLPI2C\_MasterPinLowTimeoutFlag* Pin low timeout flag.
- kLPI2C\_MasterDataMatchFlag* Data match flag.
- kLPI2C\_MasterBusyFlag* Master busy flag.
- kLPI2C\_MasterBusBusyFlag* Bus busy flag.
- kLPI2C\_MasterClearFlags* All flags which are cleared by the driver upon starting a transfer.
- kLPI2C\_MasterIrqFlags* IRQ sources enabled by the non-blocking transactional API.
- kLPI2C\_MasterErrorFlags* Errors to check for.

#### 30.4.4.2 enum lpi2c\_direction\_t

Enumerator

- kLPI2C\_Write* Master transmit.
- kLPI2C\_Read* Master receive.

### 30.4.4.3 enum lpi2c\_master\_pin\_config\_t

Enumerator

***kLPI2C\_2PinOpenDrain*** LPI2C Configured for 2-pin open drain mode.

***kLPI2C\_2PinOutputOnly*** LPI2C Configured for 2-pin output only mode (ultra-fast mode)

***kLPI2C\_2PinPushPull*** LPI2C Configured for 2-pin push-pull mode.

***kLPI2C\_4PinPushPull*** LPI2C Configured for 4-pin push-pull mode.

***kLPI2C\_2PinOpenDrainWithSeparateSlave*** LPI2C Configured for 2-pin open drain mode with separate LPI2C slave.

***kLPI2C\_2PinOutputOnlyWithSeparateSlave*** LPI2C Configured for 2-pin output only mode(ultra-fast mode) with separate LPI2C slave.

***kLPI2C\_2PinPushPullWithSeparateSlave*** LPI2C Configured for 2-pin push-pull mode with separate LPI2C slave.

***kLPI2C\_4PinPushPullWithInvertedOutput*** LPI2C Configured for 4-pin push-pull mode(inverted outputs)

### 30.4.4.4 enum lpi2c\_host\_request\_source\_t

Enumerator

***kLPI2C\_HostRequestExternalPin*** Select the LPI2C\_HREQ pin as the host request input.

***kLPI2C\_HostRequestInputTrigger*** Select the input trigger as the host request input.

### 30.4.4.5 enum lpi2c\_host\_request\_polarity\_t

Enumerator

***kLPI2C\_HostRequestPinActiveLow*** Configure the LPI2C\_HREQ pin active low.

***kLPI2C\_HostRequestPinActiveHigh*** Configure the LPI2C\_HREQ pin active high.

### 30.4.4.6 enum lpi2c\_data\_match\_config\_mode\_t

Enumerator

***kLPI2C\_MatchDisabled*** LPI2C Match Disabled.

***kLPI2C\_1stWordEqualsM0OrM1*** LPI2C Match Enabled and 1st data word equals MATCH0 OR MATCH1.

***kLPI2C\_AnyWordEqualsM0OrM1*** LPI2C Match Enabled and any data word equals MATCH0 OR MATCH1.

***kLPI2C\_1stWordEqualsM0And2ndWordEqualsM1*** LPI2C Match Enabled and 1st data word equals MATCH0, 2nd data equals MATCH1.

***kLPI2C\_AnyWordEqualsM0AndNextWordEqualsM1*** LPI2C Match Enabled and any data word equals MATCH0, next data equals MATCH1.

***kLPI2C\_1stWordAndM1EqualsM0AndM1*** LPI2C Match Enabled and 1st data word and MATCH0 equals MATCH0 and MATCH1.

***kLPI2C\_AnyWordAndM1EqualsM0AndM1*** LPI2C Match Enabled and any data word and MATCH0 equals MATCH0 and MATCH1.

### 30.4.4.7 enum \_lpi2c\_master\_transfer\_flags

Note

These enumerations are intended to be OR'd together to form a bit mask of options for the `_lpi2c_master_transfer::flags` field.

Enumerator

***kLPI2C\_TransferDefaultFlag*** Transfer starts with a start signal, stops with a stop signal.

***kLPI2C\_TransferNoStartFlag*** Don't send a start condition, address, and sub address.

***kLPI2C\_TransferRepeatedStartFlag*** Send a repeated start condition.

***kLPI2C\_TransferNoStopFlag*** Don't send a stop condition.

## 30.4.5 Function Documentation

### 30.4.5.1 void LPI2C\_MasterGetDefaultConfig ( `lpi2c_master_config_t * masterConfig` )

This function provides the following default configuration for the LPI2C master peripheral:

```
* masterConfig->enableMaster          = true;
* masterConfig->debugEnable         = false;
* masterConfig->ignoreAck           = false;
* masterConfig->pinConfig           = kLPI2C_2PinOpenDrain;
* masterConfig->baudRate_Hz        = 100000U;
* masterConfig->busIdleTimeout_ns   = 0;
* masterConfig->pinLowTimeout_ns    = 0;
* masterConfig->sdaGlitchFilterWidth_ns = 0;
* masterConfig->sclGlitchFilterWidth_ns = 0;
* masterConfig->hostRequest.enable   = false;
* masterConfig->hostRequest.source    = kLPI2C_HostRequestExternalPin;
* masterConfig->hostRequest.polarity   = kLPI2C_HostRequestPinActiveHigh;
*
```

After calling this function, you can override any settings in order to customize the configuration, prior to initializing the master driver with [LPI2C\\_MasterInit\(\)](#).

Parameters

<i>out</i>	<i>masterConfig</i>	User provided configuration structure for default values. Refer to <a href="#">lpi2c_master_config_t</a> .
------------	---------------------	--

### 30.4.5.2 void LPI2C\_MasterInit ( LPI2C\_Type \* *base*, const lpi2c\_master\_config\_t \* *masterConfig*, uint32\_t *sourceClock\_Hz* )

This function enables the peripheral clock and initializes the LPI2C master peripheral as described by the user provided configuration. A software reset is performed prior to configuration.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>masterConfig</i>	User provided peripheral configuration. Use <a href="#">LPI2C_MasterGetDefaultConfig()</a> to get a set of defaults that you can override.
<i>sourceClock_Hz</i>	Frequency in Hertz of the LPI2C functional clock. Used to calculate the baud rate divisors, filter widths, and timeout periods.

### 30.4.5.3 void LPI2C\_MasterDeinit ( LPI2C\_Type \* *base* )

This function disables the LPI2C master peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

### 30.4.5.4 void LPI2C\_MasterConfigureDataMatch ( LPI2C\_Type \* *base*, const lpi2c\_data\_match\_config\_t \* *matchConfig* )

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>matchConfig</i>	Settings for the data match feature.

### 30.4.5.5 static void LPI2C\_MasterReset ( LPI2C\_Type \* *base* ) [inline], [static]

Restores the LPI2C master peripheral to reset conditions.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

### 30.4.5.6 static void LPI2C\_MasterEnable ( LPI2C\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enable</i>	Pass true to enable or false to disable the specified LPI2C as master.

### 30.4.5.7 static uint32\_t LPI2C\_MasterGetStatusFlags ( LPI2C\_Type \* *base* ) [inline], [static]

A bit mask with the state of all LPI2C master status flags is returned. For each flag, the corresponding bit in the return value is set if the flag is asserted.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

State of the status flags:

- 1: related status flag is set.
- 0: related status flag is not set.

See Also

[\\_lpi2c\\_master\\_flags](#)

### 30.4.5.8 static void LPI2C\_MasterClearStatusFlags ( LPI2C\_Type \* *base*, uint32\_t *statusMask* ) [inline], [static]

The following status register flags can be cleared:

- [kLPI2C\\_MasterEndOfPacketFlag](#)
- [kLPI2C\\_MasterStopDetectFlag](#)
- [kLPI2C\\_MasterNackDetectFlag](#)
- [kLPI2C\\_MasterArbitrationLostFlag](#)

- `kLPI2C_MasterFifoErrFlag`
- `kLPI2C_MasterPinLowTimeoutFlag`
- `kLPI2C_MasterDataMatchFlag`

Attempts to clear other flags has no effect.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>statusMask</i>	A bitmask of status flags that are to be cleared. The mask is composed of <code>_lpi2c_master_flags</code> enumerators OR'd together. You may pass the result of a previous call to <a href="#">LPI2C_MasterGetStatusFlags()</a> .

See Also

[\\_lpi2c\\_master\\_flags](#).

#### 30.4.5.9 static void LPI2C\_MasterEnableInterrupts ( `LPI2C_Type * base`, `uint32_t interruptMask` ) [inline], [static]

All flags except `kLPI2C_MasterBusyFlag` and `kLPI2C_MasterBusBusyFlag` can be enabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to enable. See <code>_lpi2c_master_flags</code> for the set of constants that should be OR'd together to form the bit mask.

#### 30.4.5.10 static void LPI2C\_MasterDisableInterrupts ( `LPI2C_Type * base`, `uint32_t interruptMask` ) [inline], [static]

All flags except `kLPI2C_MasterBusyFlag` and `kLPI2C_MasterBusBusyFlag` can be disabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to disable. See <code>_lpi2c_master_flags</code> for the set of constants that should be OR'd together to form the bit mask.

#### 30.4.5.11 static uint32\_t LPI2C\_MasterGetEnabledInterrupts ( `LPI2C_Type * base` ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

A bitmask composed of \_lpi2c\_master\_flags enumerators OR'd together to indicate the set of enabled interrupts.

#### 30.4.5.12 static void LPI2C\_MasterEnableDMA ( LPI2C\_Type \* *base*, bool *enableTx*, bool *enableRx* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enableTx</i>	Enable flag for transmit DMA request. Pass true for enable, false for disable.
<i>enableRx</i>	Enable flag for receive DMA request. Pass true for enable, false for disable.

#### 30.4.5.13 static uint32\_t LPI2C\_MasterGetTxFifoAddress ( LPI2C\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

The LPI2C Master Transmit Data Register address.

#### 30.4.5.14 static uint32\_t LPI2C\_MasterGetRxFifoAddress ( LPI2C\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

The LPI2C Master Receive Data Register address.

#### 30.4.5.15 static void LPI2C\_MasterSetWatermarks ( *LPI2C\_Type* \* *base*, *size\_t* *txWords*, *size\_t* *rxWords* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>txWords</i>	Transmit FIFO watermark value in words. The <a href="#">kLPI2C_MasterTxReadyFlag</a> flag is set whenever the number of words in the transmit FIFO is equal or less than <i>txWords</i> . Writing a value equal or greater than the FIFO size is truncated.
<i>rxWords</i>	Receive FIFO watermark value in words. The <a href="#">kLPI2C_MasterRxReadyFlag</a> flag is set whenever the number of words in the receive FIFO is greater than <i>rxWords</i> . Writing a value equal or greater than the FIFO size is truncated.

#### 30.4.5.16 static void LPI2C\_MasterGetFifoCounts ( *LPI2C\_Type* \* *base*, *size\_t* \* *rxCount*, *size\_t* \* *txCount* ) [inline], [static]

Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>txCount</i>	Pointer through which the current number of words in the transmit FIFO is returned. Pass NULL if this value is not required.
out	<i>rxCount</i>	Pointer through which the current number of words in the receive FIFO is returned. Pass NULL if this value is not required.

#### 30.4.5.17 void LPI2C\_MasterSetBaudRate ( *LPI2C\_Type* \* *base*, *uint32\_t* *sourceClock\_Hz*, *uint32\_t* *baudRate\_Hz* )

The LPI2C master is automatically disabled and re-enabled as necessary to configure the baud rate. Do not call this function during a transfer, or the transfer is aborted.

## Note

Please note that the second parameter is the clock frequency of LPI2C module, the third parameter means user configured bus baudrate, this implementation is different from other I2C drivers which use baudrate configuration as second parameter and source clock frequency as third parameter.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>sourceClock_Hz</i>	LPI2C functional clock frequency in Hertz.
<i>baudRate_Hz</i>	Requested bus frequency in Hertz.

### 30.4.5.18 static bool LPI2C\_MasterGetBusIdleState ( LPI2C\_Type \* *base* ) [inline], [static]

Requires the master mode to be enabled.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Return values

<i>true</i>	Bus is busy.
<i>false</i>	Bus is idle.

### 30.4.5.19 status\_t LPI2C\_MasterStart ( LPI2C\_Type \* *base*, uint8\_t *address*, lpi2c\_direction\_t *dir* )

This function is used to initiate a new master mode transfer. First, the bus state is checked to ensure that another master is not occupying the bus. Then a START signal is transmitted, followed by the 7-bit address specified in the *address* parameter. Note that this function does not actually wait until the START and address are successfully sent on the bus before returning.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>address</i>	7-bit slave device address, in bits [6:0].
<i>dir</i>	Master transfer direction, either <a href="#">kLPI2C_Read</a> or <a href="#">kLPI2C_Write</a> . This parameter is used to set the R/w bit (bit 0) in the transmitted slave address.

Return values

<i>kStatus_Success</i>	START signal and address were successfully enqueued in the transmit FIFO.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.

### 30.4.5.20 static status\_t LPI2C\_MasterRepeatedStart ( LPI2C\_Type \* *base*, uint8\_t *address*, lpi2c\_direction\_t *dir* ) [inline], [static]

This function is used to send a Repeated START signal when a transfer is already in progress. Like [LPI2C\\_MasterStart\(\)](#), it also sends the specified 7-bit address.

Note

This function exists primarily to maintain compatible APIs between LPI2C and I2C drivers, as well as to better document the intent of code that uses these APIs.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>address</i>	7-bit slave device address, in bits [6:0].
<i>dir</i>	Master transfer direction, either <a href="#">kLPI2C_Read</a> or <a href="#">kLPI2C_Write</a> . This parameter is used to set the R/w bit (bit 0) in the transmitted slave address.

Return values

<i>kStatus_Success</i>	Repeated START signal and address were successfully enqueued in the transmit FIFO.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.

### 30.4.5.21 status\_t LPI2C\_MasterSend ( LPI2C\_Type \* *base*, void \* *txBuff*, size\_t *txSize* )

Sends up to *txSize* number of bytes to the previously addressed slave device. The slave may reply with a NAK to any byte in order to terminate the transfer early. If this happens, this function returns [kStatus\\_LPI2C\\_Nak](#).

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>txBuff</i>	The pointer to the data to be transferred.
<i>txSize</i>	The length in bytes of the data to be transferred.

Return values

<i>kStatus_Success</i>	Data was sent successfully.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or over run.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

### 30.4.5.22 status\_t LPI2C\_MasterReceive ( LPI2C\_Type \* *base*, void \* *rxBuff*, size\_t *rxSize* )

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>rxBuff</i>	The pointer to the data to be transferred.
<i>rxSize</i>	The length in bytes of the data to be transferred.

Return values

<i>kStatus_Success</i>	Data was received successfully.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or overrun.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

### 30.4.5.23 status\_t LPI2C\_MasterStop ( LPI2C\_Type \* *base* )

This function does not return until the STOP signal is seen on the bus, or an error occurs.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Return values

<i>kStatus_Success</i>	The STOP signal was successfully sent on the bus and the transaction terminated.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or overrun.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

### 30.4.5.24 status\_t LPI2C\_MasterTransferBlocking ( **LPI2C\_Type \* base,** **lpi2c\_master\_transfer\_t \* transfer** )

Note

The API does not return until the transfer succeeds or fails due to error happens during transfer.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>transfer</i>	Pointer to the transfer structure.

Return values

<i>kStatus_Success</i>	Data was received successfully.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or overrun.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

**30.4.5.25 void LPI2C\_MasterTransferCreateHandle ( *LPI2C\_Type* \* *base*,  
*lpi2c\_master\_handle\_t* \* *handle*, *lpi2c\_master\_transfer\_callback\_t* *callback*,  
*void* \* *userData* )**

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the [LPI2C\\_MasterTransferAbort\(\)](#) API shall be called.

#### Note

The function also enables the NVIC IRQ for the input LPI2C. Need to notice that on some SoCs the LPI2C IRQ is connected to INTMUX, in this case user needs to enable the associated INTMUX IRQ in application.

#### Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>handle</i>	Pointer to the LPI2C master driver handle.
	<i>callback</i>	User provided pointer to the asynchronous callback function.
	<i>userData</i>	User provided pointer to the application callback data.

**30.4.5.26 status\_t LPI2C\_MasterTransferNonBlocking ( *LPI2C\_Type* \* *base*,  
*lpi2c\_master\_handle\_t* \* *handle*, *lpi2c\_master\_transfer\_t* \* *transfer* )**

#### Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.
<i>transfer</i>	The pointer to the transfer descriptor.

#### Return values

<i>kStatus_Success</i>	The transaction was started successfully.
<i>kStatus_LPI2C_Busy</i>	Either another master is currently utilizing the bus, or a non-blocking transaction is already in progress.

**30.4.5.27 status\_t LPI2C\_MasterTransferGetCount ( *LPI2C\_Type* \* *base*,  
*lpi2c\_master\_handle\_t* \* *handle*, *size\_t* \* *count* )**

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>handle</i>	Pointer to the LPI2C master driver handle.
out	<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_Success</i>	
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

### 30.4.5.28 void LPI2C\_MasterTransferAbort ( LPI2C\_Type \* *base*, Ipi2c\_master\_handle\_t \* *handle* )

Note

It is not safe to call this function from an IRQ handler that has a higher priority than the LPI2C peripheral's IRQ priority.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.

Return values

<i>kStatus_Success</i>	A transaction was successfully aborted.
<i>kStatus_LPI2C_Idle</i>	There is not a non-blocking transaction currently in progress.

### 30.4.5.29 void LPI2C\_MasterTransferHandleIRQ ( LPI2C\_Type \* *base*, void \* *Ipi2cMasterHandle* )

Note

This function does not need to be called unless you are reimplementing the nonblocking API's interrupt handler routines to add special functionality.

## Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>lpi2cMasterHandle</i>	Pointer to the LPI2C master driver handle.

## 30.5 LPI2C Slave Driver

### 30.5.1 Overview

#### Data Structures

- struct `lpi2c_slave_config_t`  
*Structure with settings to initialize the LPI2C slave module. [More...](#)*
- struct `lpi2c_slave_transfer_t`  
*LPI2C slave transfer structure. [More...](#)*
- struct `lpi2c_slave_handle_t`  
*LPI2C slave handle structure. [More...](#)*

#### Typedefs

- typedef void(\* `lpi2c_slave_transfer_callback_t`)`(LPI2C_Type *base, lpi2c_slave_transfer_t *transfer, void *userData)`  
*Slave event callback function pointer type.*

#### Enumerations

- enum `_lpi2c_slave_flags` {
   
`kLPI2C_SlaveTxReadyFlag` = LPI2C\_SSR\_TDF\_MASK,  
`kLPI2C_SlaveRxReadyFlag` = LPI2C\_SSR\_RDF\_MASK,  
`kLPI2C_SlaveAddressValidFlag` = LPI2C\_SSR\_AVF\_MASK,  
`kLPI2C_SlaveTransmitAckFlag` = LPI2C\_SSR\_TAF\_MASK,  
`kLPI2C_SlaveRepeatedStartDetectFlag` = LPI2C\_SSR\_RSF\_MASK,  
`kLPI2C_SlaveStopDetectFlag` = LPI2C\_SSR\_SDF\_MASK,  
`kLPI2C_SlaveBitErrFlag` = LPI2C\_SSR\_BEF\_MASK,  
`kLPI2C_SlaveFifoErrFlag` = LPI2C\_SSR\_FEF\_MASK,  
`kLPI2C_SlaveAddressMatch0Flag` = LPI2C\_SSR\_AM0F\_MASK,  
`kLPI2C_SlaveAddressMatch1Flag` = LPI2C\_SSR\_AM1F\_MASK,  
`kLPI2C_SlaveGeneralCallFlag` = LPI2C\_SSR\_GCF\_MASK,  
`kLPI2C_SlaveBusyFlag` = LPI2C\_SSR\_SBF\_MASK,  
`kLPI2C_SlaveBusBusyFlag` = LPI2C\_SSR\_BBF\_MASK,  
`kLPI2C_SlaveClearFlags`,  
`kLPI2C_SlaveIrqFlags`,  
`kLPI2C_SlaveErrorFlags` = `kLPI2C_SlaveFifoErrFlag | kLPI2C_SlaveBitErrFlag` }
   
*LPI2C slave peripheral flags.*
- enum `lpi2c_slave_address_match_t` {
   
`kLPI2C_MatchAddress0` = 0U,  
`kLPI2C_MatchAddress0OrAddress1` = 2U,  
`kLPI2C_MatchAddress0ThroughAddress1` = 6U }
   
*LPI2C slave address match options.*

- enum `lpi2c_slave_transfer_event_t` {
   
  `kLPI2C_SlaveAddressMatchEvent` = 0x01U,
   
  `kLPI2C_SlaveTransmitEvent` = 0x02U,
   
  `kLPI2C_SlaveReceiveEvent` = 0x04U,
   
  `kLPI2C_SlaveTransmitAckEvent` = 0x08U,
   
  `kLPI2C_SlaveRepeatedStartEvent` = 0x10U,
   
  `kLPI2C_SlaveCompletionEvent` = 0x20U,
   
  `kLPI2C_SlaveAllEvents` }

*Set of events sent to the callback for non blocking slave transfers.*

## Slave initialization and deinitialization

- void `LPI2C_SlaveGetDefaultConfig` (`lpi2c_slave_config_t` \*slaveConfig)  
*Provides a default configuration for the LPI2C slave peripheral.*
- void `LPI2C_SlaveInit` (`LPI2C_Type` \*base, const `lpi2c_slave_config_t` \*slaveConfig, `uint32_t` sourceClock\_Hz)  
*Initializes the LPI2C slave peripheral.*
- void `LPI2C_SlaveDeinit` (`LPI2C_Type` \*base)  
*Deinitializes the LPI2C slave peripheral.*
- static void `LPI2C_SlaveReset` (`LPI2C_Type` \*base)  
*Performs a software reset of the LPI2C slave peripheral.*
- static void `LPI2C_SlaveEnable` (`LPI2C_Type` \*base, bool enable)  
*Enables or disables the LPI2C module as slave.*

## Slave status

- static `uint32_t` `LPI2C_SlaveGetStatusFlags` (`LPI2C_Type` \*base)  
*Gets the LPI2C slave status flags.*
- static void `LPI2C_SlaveClearStatusFlags` (`LPI2C_Type` \*base, `uint32_t` statusMask)  
*Clears the LPI2C status flag state.*

## Slave interrupts

- static void `LPI2C_SlaveEnableInterrupts` (`LPI2C_Type` \*base, `uint32_t` interruptMask)  
*Enables the LPI2C slave interrupt requests.*
- static void `LPI2C_SlaveDisableInterrupts` (`LPI2C_Type` \*base, `uint32_t` interruptMask)  
*Disables the LPI2C slave interrupt requests.*
- static `uint32_t` `LPI2C_SlaveGetEnabledInterrupts` (`LPI2C_Type` \*base)  
*Returns the set of currently enabled LPI2C slave interrupt requests.*

## Slave DMA control

- static void `LPI2C_SlaveEnableDMA` (`LPI2C_Type` \*base, bool enableAddressValid, bool enableRx, bool enableTx)

*Enables or disables the LPI2C slave peripheral DMA requests.*

## Slave bus operations

- static bool [LPI2C\\_SlaveGetBusIdleState](#) (LPI2C\_Type \*base)  
*Returns whether the bus is idle.*
- static void [LPI2C\\_SlaveTransmitAck](#) (LPI2C\_Type \*base, bool ackOrNack)  
*Transmits either an ACK or NAK on the I2C bus in response to a byte from the master.*
- static void [LPI2C\\_SlaveEnableAckStall](#) (LPI2C\_Type \*base, bool enable)  
*Enables or disables ACKSTALL.*
- static uint32\_t [LPI2C\\_SlaveGetReceivedAddress](#) (LPI2C\_Type \*base)  
*Returns the slave address sent by the I2C master.*
- status\_t [LPI2C\\_SlaveSend](#) (LPI2C\_Type \*base, void \*txBuff, size\_t txSize, size\_t \*actualTxSize)  
*Performs a polling send transfer on the I2C bus.*
- status\_t [LPI2C\\_SlaveReceive](#) (LPI2C\_Type \*base, void \*rxBuff, size\_t rxSize, size\_t \*actualRxSize)  
*Performs a polling receive transfer on the I2C bus.*

## Slave non-blocking

- void [LPI2C\\_SlaveTransferCreateHandle](#) (LPI2C\_Type \*base, lpi2c\_slave\_handle\_t \*handle, [lpi2c\\_slave\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Creates a new handle for the LPI2C slave non-blocking APIs.*
- status\_t [LPI2C\\_SlaveTransferNonBlocking](#) (LPI2C\_Type \*base, lpi2c\_slave\_handle\_t \*handle, uint32\_t eventMask)  
*Starts accepting slave transfers.*
- status\_t [LPI2C\\_SlaveTransferGetCount](#) (LPI2C\_Type \*base, lpi2c\_slave\_handle\_t \*handle, size\_t \*count)  
*Gets the slave transfer status during a non-blocking transfer.*
- void [LPI2C\\_SlaveTransferAbort](#) (LPI2C\_Type \*base, lpi2c\_slave\_handle\_t \*handle)  
*Aborts the slave non-blocking transfers.*

## Slave IRQ handler

- void [LPI2C\\_SlaveTransferHandleIRQ](#) (LPI2C\_Type \*base, lpi2c\_slave\_handle\_t \*handle)  
*Reusable routine to handle slave interrupts.*

### 30.5.2 Data Structure Documentation

#### 30.5.2.1 struct lpi2c\_slave\_config\_t

This structure holds configuration settings for the LPI2C slave peripheral. To initialize this structure to reasonable defaults, call the [LPI2C\\_SlaveGetDefaultConfig\(\)](#) function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

## Data Fields

- bool `enableSlave`  
*Enable slave mode.*
- uint8\_t `address0`  
*Slave's 7-bit address.*
- uint8\_t `address1`  
*Alternate slave 7-bit address.*
- `lpi2c_slave_address_match_t addressMatchMode`  
*Address matching options.*
- bool `filterDozeEnable`  
*Enable digital glitch filter in doze mode.*
- bool `filterEnable`  
*Enable digital glitch filter.*
- bool `enableGeneralCall`  
*Enable general call address matching.*
- bool `ignoreAck`  
*Continue transfers after a NACK is detected.*
- bool `enableReceivedAddressRead`  
*Enable reading the address received address as the first byte of data.*
- uint32\_t `sdaGlitchFilterWidth_ns`  
*Width in nanoseconds of the digital filter on the SDA signal.*
- uint32\_t `sclGlitchFilterWidth_ns`  
*Width in nanoseconds of the digital filter on the SCL signal.*
- uint32\_t `dataValidDelay_ns`  
*Width in nanoseconds of the data valid delay.*
- uint32\_t `clockHoldTime_ns`  
*Width in nanoseconds of the clock hold time.*
- bool `enableAck`  
*Enables SCL clock stretching during slave-transmit address byte(s) and slave-receiver address and data byte(s) to allow software to write the Transmit ACK Register before the ACK or NACK is transmitted.*
- bool `enableTx`  
*Enables SCL clock stretching when the transmit data flag is set during a slave-transmit transfer.*
- bool `enableRx`  
*Enables SCL clock stretching when receive data flag is set during a slave-receive transfer.*
- bool `enableAddress`  
*Enables SCL clock stretching when the address valid flag is asserted.*

## Field Documentation

- (1) `bool lpi2c_slave_config_t::enableSlave`
- (2) `uint8_t lpi2c_slave_config_t::address0`
- (3) `uint8_t lpi2c_slave_config_t::address1`
- (4) `lpi2c_slave_address_match_t lpi2c_slave_config_t::addressMatchMode`
- (5) `bool lpi2c_slave_config_t::filterDozeEnable`
- (6) `bool lpi2c_slave_config_t::filterEnable`
- (7) `bool lpi2c_slave_config_t::enableGeneralCall`
- (8) `bool lpi2c_slave_config_t::enableAck`

Clock stretching occurs when transmitting the 9th bit. When enableAckSCLStall is enabled, there is no need to set either enableRxDataSCLStall or enableAddressSCLStall.

- (9) `bool lpi2c_slave_config_t::enableTx`
- (10) `bool lpi2c_slave_config_t::enableRx`
- (11) `bool lpi2c_slave_config_t::enableAddress`
- (12) `bool lpi2c_slave_config_t::ignoreAck`
- (13) `bool lpi2c_slave_config_t::enableReceivedAddressRead`
- (14) `uint32_t lpi2c_slave_config_t::sdaGlitchFilterWidth_ns`

Set to 0 to disable.

- (15) `uint32_t lpi2c_slave_config_t::sclGlitchFilterWidth_ns`

Set to 0 to disable.

- (16) `uint32_t lpi2c_slave_config_t::dataValidDelay_ns`
- (17) `uint32_t lpi2c_slave_config_t::clockHoldTime_ns`

### 30.5.2.2 struct lpi2c\_slave\_transfer\_t

#### Data Fields

- `lpi2c_slave_transfer_event_t event`  
*Reason the callback is being invoked.*
- `uint8_t receivedAddress`  
*Matching address send by master.*

- `uint8_t * data`  
*Transfer buffer.*
- `size_t dataSize`  
*Transfer size.*
- `status_t completionStatus`  
*Success or error code describing how the transfer completed.*
- `size_t transferredCount`  
*Number of bytes actually transferred since start or last repeated start.*

## Field Documentation

- (1) `lpi2c_slave_transfer_event_t lpi2c_slave_transfer_t::event`
- (2) `uint8_t lpi2c_slave_transfer_t::receivedAddress`
- (3) `status_t lpi2c_slave_transfer_t::completionStatus`

Only applies for [kLPI2C\\_SlaveCompletionEvent](#).

- (4) `size_t lpi2c_slave_transfer_t::transferredCount`

### 30.5.2.3 struct \_lpi2c\_slave\_handle

Note

The contents of this structure are private and subject to change.

## Data Fields

- `lpi2c_slave_transfer_t transfer`  
*LPI2C slave transfer copy.*
- `bool isBusy`  
*Whether transfer is busy.*
- `bool wasTransmit`  
*Whether the last transfer was a transmit.*
- `uint32_t eventMask`  
*Mask of enabled events.*
- `uint32_t transferredCount`  
*Count of bytes transferred.*
- `lpi2c_slave_transfer_callback_t callback`  
*Callback function called at transfer event.*
- `void * userData`  
*Callback parameter passed to callback.*

## Field Documentation

- (1) `lpi2c_slave_transfer_t lpi2c_slave_handle_t::transfer`
- (2) `bool lpi2c_slave_handle_t::isBusy`
- (3) `bool lpi2c_slave_handle_t::wasTransmit`
- (4) `uint32_t lpi2c_slave_handle_t::eventMask`
- (5) `uint32_t lpi2c_slave_handle_t::transferredCount`
- (6) `lpi2c_slave_transfer_callback_t lpi2c_slave_handle_t::callback`
- (7) `void* lpi2c_slave_handle_t::userData`

## 30.5.3 Typedef Documentation

### 30.5.3.1 `typedef void(* lpi2c_slave_transfer_callback_t)(LPI2C_Type *base, lpi2c_slave_transfer_t *transfer, void *userData)`

This callback is used only for the slave non-blocking transfer API. To install a callback, use the LPI2C\_SlaveSetCallback() function after you have created a handle.

## Parameters

<i>base</i>	Base address for the LPI2C instance on which the event occurred.
<i>transfer</i>	Pointer to transfer descriptor containing values passed to and/or from the callback.
<i>userData</i>	Arbitrary pointer-sized value passed from the application.

**30.5.4 Enumeration Type Documentation****30.5.4.1 enum \_lpi2c\_slave\_flags**

The following status register flags can be cleared:

- [kLPI2C\\_SlaveRepeatedStartDetectFlag](#)
- [kLPI2C\\_SlaveStopDetectFlag](#)
- [kLPI2C\\_SlaveBitErrFlag](#)
- [kLPI2C\\_SlaveFifoErrFlag](#)

All flags except [kLPI2C\\_SlaveBusyFlag](#) and [kLPI2C\\_SlaveBusBusyFlag](#) can be enabled as interrupts.

## Note

These enumerations are meant to be OR'd together to form a bit mask.

## Enumerator

- kLPI2C\_SlaveTxReadyFlag* Transmit data flag.  
*kLPI2C\_SlaveRxReadyFlag* Receive data flag.  
*kLPI2C\_SlaveAddressValidFlag* Address valid flag.  
*kLPI2C\_SlaveTransmitAckFlag* Transmit ACK flag.  
*kLPI2C\_SlaveRepeatedStartDetectFlag* Repeated start detect flag.  
*kLPI2C\_SlaveStopDetectFlag* Stop detect flag.  
*kLPI2C\_SlaveBitErrFlag* Bit error flag.  
*kLPI2C\_SlaveFifoErrFlag* FIFO error flag.  
*kLPI2C\_SlaveAddressMatch0Flag* Address match 0 flag.  
*kLPI2C\_SlaveAddressMatch1Flag* Address match 1 flag.  
*kLPI2C\_SlaveGeneralCallFlag* General call flag.  
*kLPI2C\_SlaveBusyFlag* Master busy flag.  
*kLPI2C\_SlaveBusBusyFlag* Bus busy flag.  
*kLPI2C\_SlaveClearFlags* All flags which are cleared by the driver upon starting a transfer.  
*kLPI2C\_SlaveIrqFlags* IRQ sources enabled by the non-blocking transactional API.  
*kLPI2C\_SlaveErrorFlags* Errors to check for.

### 30.5.4.2 enum lpi2c\_slave\_address\_match\_t

Enumerator

**kLPI2C\_MatchAddress0** Match only address 0.

**kLPI2C\_MatchAddress0OrAddress1** Match either address 0 or address 1.

**kLPI2C\_MatchAddress0ThroughAddress1** Match a range of slave addresses from address 0 through address 1.

### 30.5.4.3 enum lpi2c\_slave\_transfer\_event\_t

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to [LPI2C\\_SlaveTransferNonBlocking\(\)](#) in order to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

Note

These enumerations are meant to be OR'd together to form a bit mask of events.

Enumerator

**kLPI2C\_SlaveAddressMatchEvent** Received the slave address after a start or repeated start.

**kLPI2C\_SlaveTransmitEvent** Callback is requested to provide data to transmit (slave-transmitter role).

**kLPI2C\_SlaveReceiveEvent** Callback is requested to provide a buffer in which to place received data (slave-receiver role).

**kLPI2C\_SlaveTransmitAckEvent** Callback needs to either transmit an ACK or NACK.

**kLPI2C\_SlaveRepeatedStartEvent** A repeated start was detected.

**kLPI2C\_SlaveCompletionEvent** A stop was detected, completing the transfer.

**kLPI2C\_SlaveAllEvents** Bit mask of all available events.

## 30.5.5 Function Documentation

### 30.5.5.1 void LPI2C\_SlaveGetDefaultConfig ( lpi2c\_slave\_config\_t \* *slaveConfig* )

This function provides the following default configuration for the LPI2C slave peripheral:

```
* slaveConfig->enableSlave          = true;
* slaveConfig->address0            = 0U;
* slaveConfig->address1            = 0U;
* slaveConfig->addressMatchMode   = kLPI2C_MatchAddress0;
* slaveConfig->filterDozeEnable   = true;
* slaveConfig->filterEnable        = true;
* slaveConfig->enableGeneralCall  = false;
* slaveConfig->sclStall.enableAck  = false;
* slaveConfig->sclStall.enableTx   = true;
* slaveConfig->sclStall.enableRx   = true;
* slaveConfig->sclStall.enableAddress = true;
```

```

* slaveConfig->ignoreAck          = false;
* slaveConfig->enableReceivedAddressRead = false;
* slaveConfig->sdaGlitchFilterWidth_ns   = 0;
* slaveConfig->sclGlitchFilterWidth_ns   = 0;
* slaveConfig->dataValidDelay_ns       = 0;
* slaveConfig->clockHoldTime_ns       = 0;
*

```

After calling this function, override any settings to customize the configuration, prior to initializing the master driver with [LPI2C\\_SlaveInit\(\)](#). Be sure to override at least the *address0* member of the configuration structure with the desired slave address.

Parameters

<i>out</i>	<i>slaveConfig</i>	User provided configuration structure that is set to default values. Refer to <a href="#">lpi2c_slave_config_t</a> .
------------	--------------------	--

### 30.5.5.2 void LPI2C\_SlaveInit ( LPI2C\_Type \* *base*, const lpi2c\_slave\_config\_t \* *slaveConfig*, uint32\_t *sourceClock\_Hz* )

This function enables the peripheral clock and initializes the LPI2C slave peripheral as described by the user provided configuration.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>slaveConfig</i>	User provided peripheral configuration. Use <a href="#">LPI2C_SlaveGetDefaultConfig()</a> to get a set of defaults that you can override.
<i>sourceClock_Hz</i>	Frequency in Hertz of the LPI2C functional clock. Used to calculate the filter widths, data valid delay, and clock hold time.

### 30.5.5.3 void LPI2C\_SlaveDeinit ( LPI2C\_Type \* *base* )

This function disables the LPI2C slave peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

### 30.5.5.4 static void LPI2C\_SlaveReset ( LPI2C\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

### 30.5.5.5 static void LPI2C\_SlaveEnable ( LPI2C\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enable</i>	Pass true to enable or false to disable the specified LPI2C as slave.

### 30.5.5.6 static uint32\_t LPI2C\_SlaveGetStatusFlags ( LPI2C\_Type \* *base* ) [inline], [static]

A bit mask with the state of all LPI2C slave status flags is returned. For each flag, the corresponding bit in the return value is set if the flag is asserted.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

State of the status flags:

- 1: related status flag is set.
- 0: related status flag is not set.

See Also

[\\_lpi2c\\_slave\\_flags](#)

### 30.5.5.7 static void LPI2C\_SlaveClearStatusFlags ( LPI2C\_Type \* *base*, uint32\_t *statusMask* ) [inline], [static]

The following status register flags can be cleared:

- [kLPI2C\\_SlaveRepeatedStartDetectFlag](#)
- [kLPI2C\\_SlaveStopDetectFlag](#)
- [kLPI2C\\_SlaveBitErrFlag](#)
- [kLPI2C\\_SlaveFifoErrFlag](#)

Attempts to clear other flags has no effect.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>statusMask</i>	A bitmask of status flags that are to be cleared. The mask is composed of <a href="#">_lpi2c_slave_flags</a> enumerators OR'd together. You may pass the result of a previous call to <a href="#">LPI2C_SlaveGetStatusFlags()</a> .

See Also

[\\_lpi2c\\_slave\\_flags](#).

### 30.5.5.8 static void LPI2C\_SlaveEnableInterrupts ( LPI2C\_Type \* *base*, uint32\_t *interruptMask* ) [inline], [static]

All flags except [kLPI2C\\_SlaveBusyFlag](#) and [kLPI2C\\_SlaveBusBusyFlag](#) can be enabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to enable. See <a href="#">_lpi2c_slave_flags</a> for the set of constants that should be OR'd together to form the bit mask.

### 30.5.5.9 static void LPI2C\_SlaveDisableInterrupts ( LPI2C\_Type \* *base*, uint32\_t *interruptMask* ) [inline], [static]

All flags except [kLPI2C\\_SlaveBusyFlag](#) and [kLPI2C\\_SlaveBusBusyFlag](#) can be disabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to disable. See <a href="#">_lpi2c_slave_flags</a> for the set of constants that should be OR'd together to form the bit mask.

### 30.5.5.10 static uint32\_t LPI2C\_SlaveGetEnabledInterrupts ( LPI2C\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

A bitmask composed of [\\_lpi2c\\_slave\\_flags](#) enumerators OR'd together to indicate the set of enabled interrupts.

### 30.5.5.11 static void LPI2C\_SlaveEnableDMA ( LPI2C\_Type \* *base*, bool *enableAddressValid*, bool *enableRx*, bool *enableTx* ) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enableAddressValid</i>	Enable flag for the address valid DMA request. Pass true for enable, false for disable. The address valid DMA request is shared with the receive data DMA request.
<i>enableRx</i>	Enable flag for the receive data DMA request. Pass true for enable, false for disable.
<i>enableTx</i>	Enable flag for the transmit data DMA request. Pass true for enable, false for disable.

### 30.5.5.12 static bool LPI2C\_SlaveGetBusIdleState ( LPI2C\_Type \* *base* ) [inline], [static]

Requires the slave mode to be enabled.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Return values

<i>true</i>	Bus is busy.
<i>false</i>	Bus is idle.

### 30.5.5.13 static void LPI2C\_SlaveTransmitAck ( LPI2C\_Type \* *base*, bool *ackOrNack* ) [inline], [static]

Use this function to send an ACK or NAK when the [KLPI2C\\_SlaveTransmitAckFlag](#) is asserted. This only happens if you enable the sclStall.enableAck field of the [lpi2c\\_slave\\_config\\_t](#) configuration structure used to initialize the slave peripheral.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>ackOrNack</i>	Pass true for an ACK or false for a NAK.

### 30.5.5.14 static void LPI2C\_SlaveEnableAckStall ( **LPI2C\_Type** \* *base*, **bool enable** ) [**inline**], [**static**]

When enables ACKSTALL, software can transmit either an ACK or NAK on the I2C bus in response to a byte from the master.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enable</i>	True will enable ACKSTALL, false will disable ACKSTALL.

### 30.5.5.15 static uint32\_t LPI2C\_SlaveGetReceivedAddress ( **LPI2C\_Type** \* *base* ) [**inline**], [**static**]

This function should only be called if the [kLPI2C\\_SlaveAddressValidFlag](#) is asserted.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

The 8-bit address matched by the LPI2C slave. Bit 0 contains the R/w direction bit, and the 7-bit slave address is in the upper 7 bits.

### 30.5.5.16 status\_t LPI2C\_SlaveSend ( **LPI2C\_Type** \* *base*, **void** \* *txBuff*, **size\_t** *txSize*, **size\_t** \* *actualTxSize* )

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>txBuff</i>	The pointer to the data to be transferred.
	<i>txSize</i>	The length in bytes of the data to be transferred.
out	<i>actualTxSize</i>	

Returns

Error or success status returned by API.

### 30.5.5.17 **status\_t LPI2C\_SlaveReceive ( LPI2C\_Type \* *base*, void \* *rxBuff*, size\_t *rxSize*, size\_t \* *actualRxSize* )**

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>rxBuff</i>	The pointer to the data to be transferred.
	<i>rxSize</i>	The length in bytes of the data to be transferred.
out	<i>actualRxSize</i>	

Returns

Error or success status returned by API.

### 30.5.5.18 **void LPI2C\_SlaveTransferCreateHandle ( LPI2C\_Type \* *base*, Ipi2c\_slave\_handle\_t \* *handle*, Ipi2c\_slave\_transfer\_callback\_t *callback*, void \* *userData* )**

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the [LPI2C\\_SlaveTransferAbort\(\)](#) API shall be called.

Note

The function also enables the NVIC IRQ for the input LPI2C. Need to notice that on some SoCs the LPI2C IRQ is connected to INTMUX, in this case user needs to enable the associated INTMUX IRQ in application.

## Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>handle</i>	Pointer to the LPI2C slave driver handle.
	<i>callback</i>	User provided pointer to the asynchronous callback function.
	<i>userData</i>	User provided pointer to the application callback data.

### 30.5.5.19 status\_t LPI2C\_SlaveTransferNonBlocking ( **LPI2C\_Type** \* *base*, **lpi2c\_slave\_handle\_t** \* *handle*, **uint32\_t** *eventMask* )

Call this API after calling I2C\_SlaveInit() and [LPI2C\\_SlaveTransferCreateHandle\(\)](#) to start processing transactions driven by an I2C master. The slave monitors the I2C bus and pass events to the callback that was passed into the call to [LPI2C\\_SlaveTransferCreateHandle\(\)](#). The callback is always invoked from the interrupt context.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of [lpi2c\\_slave\\_transfer\\_event\\_t](#) enumerators for the events you wish to receive. The [kLPI2C\\_SlaveTransmitEvent](#) and [kLPI2C\\_SlaveReceiveEvent](#) events are always enabled and do not need to be included in the mask. Alternatively, you can pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the [kLPI2C\\_SlaveAllEvents](#) constant is provided as a convenient way to enable all events.

## Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to <a href="#">lpi2c_slave_handle_t</a> structure which stores the transfer state.
<i>eventMask</i>	Bit mask formed by OR'ing together <a href="#">lpi2c_slave_transfer_event_t</a> enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and <a href="#">kLPI2C_SlaveAllEvents</a> to enable all events.

## Return values

<a href="#">kStatus_Success</a>	Slave transfers were successfully started.
<a href="#">kStatus_LPI2C_Busy</a>	Slave transfers have already been started on this handle.

### 30.5.5.20 status\_t LPI2C\_SlaveTransferGetCount ( **LPI2C\_Type** \* *base*, **lpi2c\_slave\_handle\_t** \* *handle*, **size\_t** \* *count* )

## Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>handle</i>	Pointer to i2c_slave_handle_t structure.
out	<i>count</i>	Pointer to a value to hold the number of bytes transferred. May be NULL if the count is not required.

## Return values

<i>kStatus_Success</i>	
<i>kStatus_NoTransferIn-Progress</i>	

**30.5.5.21 void LPI2C\_SlaveTransferAbort ( LPI2C\_Type \* *base*, Ipi2c\_slave\_handle\_t \* *handle* )**

## Note

This API could be called at any time to stop slave for handling the bus events.

## Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to lpi2c_slave_handle_t structure which stores the transfer state.

## Return values

<i>kStatus_Success</i>	
<i>kStatus_LPI2C_Idle</i>	

**30.5.5.22 void LPI2C\_SlaveTransferHandleIRQ ( LPI2C\_Type \* *base*, Ipi2c\_slave\_handle\_t \* *handle* )**

## Note

This function does not need to be called unless you are reimplementing the non blocking API's interrupt handler routines to add special functionality.

## Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to lpi2c_slave_handle_t structure which stores the transfer state.

## 30.6 LPI2C Master DMA Driver

### 30.6.1 Overview

#### Data Structures

- struct `lpi2c_master_edma_handle_t`  
*Driver handle for master DMA APIs.* [More...](#)

#### Typedefs

- `typedef void(* lpi2c_master_edma_transfer_callback_t)(LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, status_t completionStatus, void *userData)`  
*Master DMA completion callback function pointer type.*

#### Master DMA

- `void LPI2C_MasterCreateEDMAHandle (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, edma_handle_t *rxDmaHandle, edma_handle_t *txDmaHandle, lpi2c_master_edma_transfer_callback_t callback, void *userData)`  
*Create a new handle for the LPI2C master DMA APIs.*
- `status_t LPI2C_MasterTransferEDMA (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, lpi2c_master_transfer_t *transfer)`  
*Performs a non-blocking DMA-based transaction on the I2C bus.*
- `status_t LPI2C_MasterTransferGetCountEDMA (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, size_t *count)`  
*Returns number of bytes transferred so far.*
- `status_t LPI2C_MasterTransferAbortEDMA (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle)`  
*Terminates a non-blocking LPI2C master transmission early.*

### 30.6.2 Data Structure Documentation

#### 30.6.2.1 struct \_lpi2c\_master\_edma\_handle

Note

The contents of this structure are private and subject to change.

#### Data Fields

- `LPI2C_Type * base`  
*LPI2C base pointer.*
- `bool isBusy`

- *Transfer state machine current state.*
- `uint8_t nbytes`  
*eDMA minor byte transfer count initially configured.*
- `uint16_t commandBuffer[10]`  
*LPI2C command sequence.*
- `lpi2c_master_transfer_t transfer`  
*Copy of the current transfer info.*
- `lpi2c_master_edma_transfer_callback_t completionCallback`  
*Callback function pointer.*
- `void *userData`  
*Application data passed to callback.*
- `edma_handle_t *rx`  
*Handle for receive DMA channel.*
- `edma_handle_t *tx`  
*Handle for transmit DMA channel.*
- `edma_tcd_t tcds[3]`  
*Software TCD.*

## Field Documentation

- (1) `LPI2C_Type* lpi2c_master_edma_handle_t::base`
- (2) `bool lpi2c_master_edma_handle_t::isBusy`
- (3) `uint8_t lpi2c_master_edma_handle_t::nbytes`
- (4) `uint16_t lpi2c_master_edma_handle_t::commandBuffer[10]`

When all 10 command words are used: Start&addr&write[1 word] + subaddr[4 words] + restart&addr&read[1 word] + receive&Size[4 words]

- (5) `lpi2c_master_transfer_t lpi2c_master_edma_handle_t::transfer`
- (6) `lpi2c_master_edma_transfer_callback_t lpi2c_master_edma_handle_t::completionCallback`
- (7) `void* lpi2c_master_edma_handle_t::userData`
- (8) `edma_handle_t* lpi2c_master_edma_handle_t::rx`
- (9) `edma_handle_t* lpi2c_master_edma_handle_t::tx`
- (10) `edma_tcd_t lpi2c_master_edma_handle_t::tcds[3]`

Three are allocated to provide enough room to align to 32-bytes.

### 30.6.3 Typedef Documentation

30.6.3.1 **typedef void(\* Ipi2c\_master\_edma\_transfer\_callback\_t)(LPI2C\_Type \*base,  
Ipi2c\_master\_edma\_handle\_t \*handle, status\_t completionStatus, void  
\*userData)**

This callback is used only for the non-blocking master transfer API. Specify the callback you wish to use in the call to [LPI2C\\_MasterCreateEDMAHandle\(\)](#).

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Handle associated with the completed transfer.
<i>completion-Status</i>	Either kStatus_Success or an error code describing how the transfer completed.
<i>userData</i>	Arbitrary pointer-sized value passed from the application.

### 30.6.4 Function Documentation

**30.6.4.1 void LPI2C\_MasterCreateEDMAHandle ( LPI2C\_Type \* *base*, Ipi2c\_master\_edma\_handle\_t \* *handle*, edma\_handle\_t \* *rxDmaHandle*, edma\_handle\_t \* *txDmaHandle*, Ipi2c\_master\_edma\_transfer\_callback\_t *callback*, void \* *userData* )**

The creation of a handle is for use with the DMA APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the [LPI2C\\_MasterTransferAbort-EDMA\(\)](#) API shall be called.

For devices where the LPI2C send and receive DMA requests are OR'd together, the *txDmaHandle* parameter is ignored and may be set to NULL.

Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>handle</i>	Pointer to the LPI2C master driver handle.
	<i>rxDmaHandle</i>	Handle for the eDMA receive channel. Created by the user prior to calling this function.
	<i>txDmaHandle</i>	Handle for the eDMA transmit channel. Created by the user prior to calling this function.
	<i>callback</i>	User provided pointer to the asynchronous callback function.
	<i>userData</i>	User provided pointer to the application callback data.

**30.6.4.2 status\_t LPI2C\_MasterTransferEDMA ( LPI2C\_Type \* *base*, Ipi2c\_master\_edma\_handle\_t \* *handle*, Ipi2c\_master\_transfer\_t \* *transfer* )**

The callback specified when the *handle* was created is invoked when the transaction has completed.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.
<i>transfer</i>	The pointer to the transfer descriptor.

Return values

<i>kStatus_Success</i>	The transaction was started successfully.
<i>kStatus_LPI2C_Busy</i>	Either another master is currently utilizing the bus, or another DMA transaction is already in progress.

### 30.6.4.3 status\_t LPI2C\_MasterTransferGetCountEDMA ( *LPI2C\_Type \* base, lpi2c\_master\_edma\_handle\_t \* handle, size\_t \* count* )

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>handle</i>	Pointer to the LPI2C master driver handle.
<i>out</i>	<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_Success</i>	
<i>kStatus_NoTransferInProgress</i>	There is not a DMA transaction currently in progress.

### 30.6.4.4 status\_t LPI2C\_MasterTransferAbortEDMA ( *LPI2C\_Type \* base, lpi2c\_master\_edma\_handle\_t \* handle* )

Note

It is not safe to call this function from an IRQ handler that has a higher priority than the eDMA peripheral's IRQ priority.

## Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.

## Return values

<i>kStatus_Success</i>	A transaction was successfully aborted.
<i>kStatus_LPI2C_Idle</i>	There is not a DMA transaction currently in progress.

## 30.7 LPI2C FreeRTOS Driver

### 30.7.1 Overview

#### Driver version

- `#define FSL_LPI2C_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 3, 2))`  
*LPI2C FreeRTOS driver version.*

#### LPI2C RTOS Operation

- `status_t LPI2C_RRTOS_Init (lpi2c_rtos_handle_t *handle, LPI2C_Type *base, const lpi2c_master_config_t *masterConfig, uint32_t srcClock_Hz)`  
*Initializes LPI2C.*
- `status_t LPI2C_RRTOS_Deinit (lpi2c_rtos_handle_t *handle)`  
*Deinitializes the LPI2C.*
- `status_t LPI2C_RRTOS_Transfer (lpi2c_rtos_handle_t *handle, lpi2c_master_transfer_t *transfer)`  
*Performs I2C transfer.*

### 30.7.2 Macro Definition Documentation

#### 30.7.2.1 `#define FSL_LPI2C_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 3, 2))`

### 30.7.3 Function Documentation

#### 30.7.3.1 `status_t LPI2C_RRTOS_Init ( lpi2c_rtos_handle_t * handle, LPI2C_Type * base, const lpi2c_master_config_t * masterConfig, uint32_t srcClock_Hz )`

This function initializes the LPI2C module and related RTOS context.

Parameters

<code>handle</code>	The RTOS LPI2C handle, the pointer to an allocated space for RTOS context.
<code>base</code>	The pointer base address of the LPI2C instance to initialize.
<code>masterConfig</code>	Configuration structure to set-up LPI2C in master mode.
<code>srcClock_Hz</code>	Frequency of input clock of the LPI2C module.

Returns

status of the operation.

### 30.7.3.2 status\_t LPI2C\_RTOS\_Deinit ( *lpi2c\_rtos\_handle\_t \* handle* )

This function deinitializes the LPI2C module and related RTOS context.

Parameters

<i>handle</i>	The RTOS LPI2C handle.
---------------	------------------------

### 30.7.3.3 status\_t LPI2C\_RTOS\_Transfer ( *lpi2c\_rtos\_handle\_t \* handle,* *lpi2c\_master\_transfer\_t \* transfer* )

This function performs an I2C transfer using LPI2C module according to data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS LPI2C handle.
<i>transfer</i>	Structure specifying the transfer parameters.

Returns

status of the operation.

## 30.8 LPI2C CMSIS Driver

This section describes the programming interface of the LPI2C Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method see <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The LPI2C CMSIS driver includes transactional APIs.

Transactional APIs are transaction target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code accessing the hardware registers.

### 30.8.1 LPI2C CMSIS Driver

#### 30.8.1.1 Master Operation in interrupt transactional method

```
void I2C_MasterSignalEvent_t(uint32_t event)
{
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_MasterCompletionFlag = true;
    }
}
/*Init I2C0*/
Driver_I2C0.Initialize(I2C_MasterSignalEvent_t);

Driver_I2C0.PowerControl(ARM_POWER_FULL);

/*config transmit speed/
Driver_I2C0.Control(ARM_I2C_BUS_SPEED, ARM_I2C_BUS_SPEED_STANDARD);

/*start transmit*/
Driver_I2C0.MasterTransmit(I2C_MASTER_SLAVE_ADDR, g_master_buff, I2C_DATA_LENGTH, false);

/* Wait for transfer completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;
```

#### 30.8.1.2 Master Operation in DMA transactional method

```
void I2C_MasterSignalEvent_t(uint32_t event)
{
    /* Transfer done */
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_MasterCompletionFlag = true;
    }
}

/* DMAMux init and EDMA init. */
DMAMUX_Init(EXAMPLE_LPI2C_DMAMUX_BASEADDR);
```

```

edma_config_t edmaConfig;
EDMA_GetDefaultConfig(&edmaConfig);
EDMA_Init(EXAMPLE_LPI2C_DMA_BASEADDR, &edmaConfig);

/*Init I2C0*/
Driver_I2C0.Initialize(I2C_MasterSignalEvent_t);

Driver_I2C0.PowerControl(ARM_POWER_FULL);

/*config transmit speed*/
Driver_I2C0.Control(ARM_I2C_BUS_SPEED, ARM_I2C_BUS_SPEED_STANDARD);

/*start transfer*/
Driver_I2C0.MasterReceive(I2C_MASTER_SLAVE_ADDR, g_master_buff, I2C_DATA_LENGTH, false);

/* Wait for transfer completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;

```

### 30.8.1.3 Slave Operation in interrupt transactional method

```

void I2C_SlaveSignalEvent_t(uint32_t event)
{
    /* Transfer done */
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_SlaveCompletionFlag = true;
    }
}

/*Init I2C1*/
Driver_I2C1.Initialize(I2C_SlaveSignalEvent_t);

Driver_I2C1.PowerControl(ARM_POWER_FULL);

/*config slave addr*/
Driver_I2C1.Control(ARM_I2C_OWN_ADDRESS, I2C_MASTER_SLAVE_ADDR);

/*start transfer*/
Driver_I2C1.SlaveReceive(g_slave_buff, I2C_DATA_LENGTH);

/* Wait for transfer completed. */
while (!g_SlaveCompletionFlag)
{
}
g_SlaveCompletionFlag = false;

```

# Chapter 31

## LPSPI: Low Power Serial Peripheral Interface

### 31.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Low Power Serial Peripheral Interface (LPSPI) module of MCUXpresso SDK devices.

### Modules

- [LPSPI CMSIS Driver](#)
- [LPSPI FreeRTOS Driver](#)
- [LPSPI Peripheral driver](#)
- [LPSPI eDMA Driver](#)

## 31.2 LPSPI Peripheral driver

### 31.2.1 Overview

This section describes the programming interface of the LPSPI Peripheral driver. The LPSPI driver configures LPSPI module, provides the functional and transactional interfaces to build the LPSPI application.

### 31.2.2 Function groups

#### 31.2.2.1 LPSPI Initialization and De-initialization

This function group initializes the default configuration structure for master and slave, initializes the LPSPI master with a master configuration, initializes the LPSPI slave with a slave configuration, and de-initializes the LPSPI module.

#### 31.2.2.2 LPSPI Basic Operation

This function group enables/disables the LPSPI module both interrupt and DMA, gets the data register address for the DMA transfer, sets master and slave, starts and stops the transfer, and so on.

#### 31.2.2.3 LPSPI Transfer Operation

This function group controls the transfer, master send/receive data, and slave send/receive data.

#### 31.2.2.4 LPSPI Status Operation

This function group gets/clears the LPSPI status.

#### 31.2.2.5 LPSPI Block Transfer Operation

This function group transfers a block of data, gets the transfer status, and aborts the transfer.

### 31.2.3 Typical use case

#### 31.2.3.1 Master Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/lpspi

### 31.2.3.2 Slave Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/lpspi

## Data Structures

- struct `lpspi_master_config_t`  
*LPSPI master configuration structure. [More...](#)*
- struct `lpspi_slave_config_t`  
*LPSPI slave configuration structure. [More...](#)*
- struct `lpspi_transfer_t`  
*LPSPI master/slave transfer structure. [More...](#)*
- struct `lpspi_master_handle_t`  
*LPSPI master transfer handle structure used for transactional API. [More...](#)*
- struct `lpspi_slave_handle_t`  
*LPSPI slave transfer handle structure used for transactional API. [More...](#)*

## Macros

- #define `LPSPI_DUMMY_DATA` (0x00U)  
*LPSPI dummy data if no Tx data.*
- #define `SPI_RETRY_TIMES` 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*
- #define `LPSPI_MASTER_PCS_SHIFT` (4U)  
*LPSPI master PCS shift macro , internal used.*
- #define `LPSPI_MASTER_PCS_MASK` (0xF0U)  
*LPSPI master PCS shift macro , internal used.*
- #define `LPSPI_SLAVE_PCS_SHIFT` (4U)  
*LPSPI slave PCS shift macro , internal used.*
- #define `LPSPI_SLAVE_PCS_MASK` (0xF0U)  
*LPSPI slave PCS shift macro , internal used.*

## Typedefs

- typedef void(\* `lpspi_master_transfer_callback_t` )(LPSPI\_Type \*base, lpspi\_master\_handle\_t \*handle, `status_t` status, void \*userData)  
*Master completion callback function pointer type.*
- typedef void(\* `lpspi_slave_transfer_callback_t` )(LPSPI\_Type \*base, lpspi\_slave\_handle\_t \*handle, `status_t` status, void \*userData)  
*Slave completion callback function pointer type.*

## Enumerations

- enum {
   
kStatus\_LPSPI\_Busy = MAKE\_STATUS(kStatusGroup\_LPSPI, 0),
   
kStatus\_LPSPI\_Error = MAKE\_STATUS(kStatusGroup\_LPSPI, 1),
   
kStatus\_LPSPI\_Idle = MAKE\_STATUS(kStatusGroup\_LPSPI, 2),
   
kStatus\_LPSPI\_OutOfRange = MAKE\_STATUS(kStatusGroup\_LPSPI, 3),
   
kStatus\_LPSPI\_Timeout = MAKE\_STATUS(kStatusGroup\_LPSPI, 4) }
   
*Status for the LPSPI driver.*
  - enum \_lpspi\_flags {
   
kLPSPI\_TxDataRequestFlag = LPSPI\_SR\_TDF\_MASK,
   
kLPSPI\_RxDataReadyFlag = LPSPI\_SR\_RDF\_MASK,
   
kLPSPI\_WordCompleteFlag = LPSPI\_SR\_WCF\_MASK,
   
kLPSPI\_FrameCompleteFlag = LPSPI\_SR\_FCF\_MASK,
   
kLPSPI\_TransferCompleteFlag = LPSPI\_SR\_TCF\_MASK,
   
kLPSPI\_TransmitErrorFlag = LPSPI\_SR\_TEF\_MASK,
   
kLPSPI\_ReceiveErrorFlag = LPSPI\_SR\_REF\_MASK,
   
kLPSPI\_DataMatchFlag = LPSPI\_SR\_DMF\_MASK,
   
kLPSPI\_ModuleBusyFlag = LPSPI\_SR\_MBFI\_MASK,
   
kLPSPI\_AllStatusFlag }
   
*LPSPI status flags in SPIx\_SR register.*
  - enum \_lpspi\_interrupt\_enable {
   
kLPSPI\_TxInterruptEnable = LPSPI\_IER\_TDIE\_MASK,
   
kLPSPI\_RxInterruptEnable = LPSPI\_IER\_RDIE\_MASK,
   
kLPSPI\_WordCompleteInterruptEnable = LPSPI\_IER\_WCIE\_MASK,
   
kLPSPI\_FrameCompleteInterruptEnable = LPSPI\_IER\_FCIE\_MASK,
   
kLPSPI\_TransferCompleteInterruptEnable = LPSPI\_IER\_TCIE\_MASK,
   
kLPSPI\_TransmitErrorInterruptEnable = LPSPI\_IER\_TEIE\_MASK,
   
kLPSPI\_ReceiveErrorInterruptEnable = LPSPI\_IER\_REIE\_MASK,
   
kLPSPI\_DataMatchInterruptEnable = LPSPI\_IER\_DMIE\_MASK,
   
kLPSPI\_AllInterruptEnable }
   
*LPSPI interrupt source.*
  - enum \_lpspi\_dma\_enable {
   
kLPSPI\_TxDmaEnable = LPSPI\_DER\_TDDE\_MASK,
   
kLPSPI\_RxDmaEnable = LPSPI\_DER\_RDDE\_MASK }
  - enum lpspi\_master\_slave\_mode\_t {
   
kLPSPI\_Master = 1U,
   
kLPSPI\_Slave = 0U }
  - enum lpspi\_which\_pcs\_t {
   
kLPSPI\_Pcs0 = 0U,
   
kLPSPI\_Pcs1 = 1U,
   
kLPSPI\_Pcs2 = 2U,
   
kLPSPI\_Pcs3 = 3U }
- LPSPI Peripheral Chip Select (PCS) configuration (which PCS to configure).*

- enum `lpspi_pcs_polarity_config_t` {
   
  `kLPSPI_PcsActiveHigh` = 1U,
   
  `kLPSPI_PcsActiveLow` = 0U }

*LPSPI Peripheral Chip Select (PCS) Polarity configuration.*

- enum `_lpspi_pcs_polarity` {
   
  `kLPSPI_Pcs0ActiveLow` = 1U << 0,
   
  `kLPSPI_Pcs1ActiveLow` = 1U << 1,
   
  `kLPSPI_Pcs2ActiveLow` = 1U << 2,
   
  `kLPSPI_Pcs3ActiveLow` = 1U << 3,
   
  `kLPSPI_PcsAllActiveLow` = 0xFU }

*LPSPI Peripheral Chip Select (PCS) Polarity.*

- enum `lpspi_clock_polarity_t` {
   
  `kLPSPI_ClockPolarityActiveHigh` = 0U,
   
  `kLPSPI_ClockPolarityActiveLow` = 1U }

*LPSPI clock polarity configuration.*

- enum `lpspi_clock_phase_t` {
   
  `kLPSPI_ClockPhaseFirstEdge` = 0U,
   
  `kLPSPI_ClockPhaseSecondEdge` = 1U }

*LPSPI clock phase configuration.*

- enum `lpspi_shift_direction_t` {
   
  `kLPSPI_MsbFirst` = 0U,
   
  `kLPSPI_LsbFirst` = 1U }

*LPSPI data shifter direction options.*

- enum `lpspi_host_request_select_t` {
   
  `kLPSPI_HostReqExtPin` = 0U,
   
  `kLPSPI_HostReqInternalTrigger` = 1U }

*LPSPI Host Request select configuration.*

- enum `lpspi_match_config_t` {
   
  `kLPSI_MatchDisabled` = 0x0U,
   
  `kLPSI_1stWordEqualsM0orM1` = 0x2U,
   
  `kLPSI_AnyWordEqualsM0orM1` = 0x3U,
   
  `kLPSI_1stWordEqualsM0and2ndWordEqualsM1` = 0x4U,
   
  `kLPSI_AnyWordEqualsM0andNxtWordEqualsM1` = 0x5U,
   
  `kLPSI_1stWordAndM1EqualsM0andM1` = 0x6U,
   
  `kLPSI_AnyWordAndM1EqualsM0andM1` = 0x7U }

*LPSPI Match configuration options.*

- enum `lpspi_pin_config_t` {
   
  `kLPSPI_SdiInSdoOut` = 0U,
   
  `kLPSPI_SdiInSdiOut` = 1U,
   
  `kLPSPI_SdoInSdoOut` = 2U,
   
  `kLPSPI_SdoInSdiOut` = 3U }

*LPSPI pin (SDO and SDI) configuration.*

- enum `lpspi_data_out_config_t` {
   
  `kLpspiDataOutRetained` = 0U,
   
  `kLpspiDataOutTristate` = 1U }

*LPSPI data output configuration.*

- enum `lpspi_transfer_width_t` {

- `kLPSPI_SingleBitXfer` = 0U,  
`kLPSPI_TwoBitXfer` = 1U,  
`kLPSPI_FourBitXfer` = 2U }
- LPSPI transfer width configuration.*
- enum `lpspi_delay_type_t` {  
`kLPSPI_PcsToSck` = 1U,  
`kLPSPI_LastSckToPcs`,  
`kLPSPI_BetweenTransfer` }
- LPSPI delay type selection.*
- enum `_lpspi_transfer_config_flag_for_master` {  
`kLPSPI_MasterPcs0` = 0U << `LPSPI_MASTER_PCS_SHIFT`,  
`kLPSPI_MasterPcs1` = 1U << `LPSPI_MASTER_PCS_SHIFT`,  
`kLPSPI_MasterPcs2` = 2U << `LPSPI_MASTER_PCS_SHIFT`,  
`kLPSPI_MasterPcs3` = 3U << `LPSPI_MASTER_PCS_SHIFT`,  
`kLPSPI_MasterPcsContinuous` = 1U << 20,  
`kLPSPI_MasterByteSwap` }
- Use this enumeration for LPSPI master transfer configFlags.*
- enum `_lpspi_transfer_config_flag_for_slave` {  
`kLPSPI_SlavePcs0` = 0U << `LPSPI_SLAVE_PCS_SHIFT`,  
`kLPSPI_SlavePcs1` = 1U << `LPSPI_SLAVE_PCS_SHIFT`,  
`kLPSPI_SlavePcs2` = 2U << `LPSPI_SLAVE_PCS_SHIFT`,  
`kLPSPI_SlavePcs3` = 3U << `LPSPI_SLAVE_PCS_SHIFT`,  
`kLPSPI_SlaveByteSwap` }
- Use this enumeration for LPSPI slave transfer configFlags.*
- enum `_lpspi_transfer_state` {  
`kLPSPI_Idle` = 0x0U,  
`kLPSPI_Busy`,  
`kLPSPI_Error` }
- LPSPI transfer state, which is used for LPSPI transactional API state machine.*

## Variables

- volatile uint8\_t `g_lpSpiDummyData` []  
*Global variable for dummy data value setting.*

## Driver version

- #define `FSL_LPSPI_DRIVER_VERSION` (`MAKE_VERSION(2, 4, 5)`)  
*LPSPI driver version.*

## Initialization and deinitialization

- void `LPSPI_MasterInit` (`LPSPI_Type` \*base, const `lpspi_master_config_t` \*masterConfig, `uint32_t` srcClock\_Hz)

*Initializes the LPSPI master.*

- void [LPSPI\\_MasterGetDefaultConfig](#) ([lpspi\\_master\\_config\\_t](#) \*masterConfig)  
*Sets the [lpspi\\_master\\_config\\_t](#) structure to default values.*
- void [LPSPI\\_SlaveInit](#) (LPSPI\_Type \*base, const [lpspi\\_slave\\_config\\_t](#) \*slaveConfig)  
*LPSPI slave configuration.*
- void [LPSPI\\_SlaveGetDefaultConfig](#) ([lpspi\\_slave\\_config\\_t](#) \*slaveConfig)  
*Sets the [lpspi\\_slave\\_config\\_t](#) structure to default values.*
- void [LPSPI\\_Deinit](#) (LPSPI\_Type \*base)  
*De-initializes the LPSPI peripheral.*
- void [LPSPI\\_Reset](#) (LPSPI\_Type \*base)  
*Restores the LPSPI peripheral to reset state.*
- uint32\_t [LPSPIGetInstance](#) (LPSPI\_Type \*base)  
*Get the LPSPI instance from peripheral base address.*
- static void [LPSPI\\_Enable](#) (LPSPI\_Type \*base, bool enable)  
*Enables the LPSPI peripheral and sets the MCR MDIS to 0.*

## Status

- static uint32\_t [LPSPI\\_GetStatusFlags](#) (LPSPI\_Type \*base)  
*Gets the LPSPI status flag state.*
- static uint8\_t [LPSPI\\_GetTxFifoSize](#) (LPSPI\_Type \*base)  
*Gets the LPSPI Tx FIFO size.*
- static uint8\_t [LPSPI\\_GetRxFifoSize](#) (LPSPI\_Type \*base)  
*Gets the LPSPI Rx FIFO size.*
- static uint32\_t [LPSPI\\_GetTxFifoCount](#) (LPSPI\_Type \*base)  
*Gets the LPSPI Tx FIFO count.*
- static uint32\_t [LPSPI\\_GetRxFifoCount](#) (LPSPI\_Type \*base)  
*Gets the LPSPI Rx FIFO count.*
- static void [LPSPI\\_ClearStatusFlags](#) (LPSPI\_Type \*base, uint32\_t statusFlags)  
*Clears the LPSPI status flag.*

## Interrupts

- static void [LPSPI\\_EnableInterrupts](#) (LPSPI\_Type \*base, uint32\_t mask)  
*Enables the LPSPI interrupts.*
- static void [LPSPI\\_DisableInterrupts](#) (LPSPI\_Type \*base, uint32\_t mask)  
*Disables the LPSPI interrupts.*

## DMA Control

- static void [LPSPI\\_EnableDMA](#) (LPSPI\_Type \*base, uint32\_t mask)  
*Enables the LPSPI DMA request.*
- static void [LPSPI\\_DisableDMA](#) (LPSPI\_Type \*base, uint32\_t mask)  
*Disables the LPSPI DMA request.*
- static uint32\_t [LPSPI\\_GetTxRegisterAddress](#) (LPSPI\_Type \*base)  
*Gets the LPSPI Transmit Data Register address for a DMA operation.*
- static uint32\_t [LPSPI\\_GetRxRegisterAddress](#) (LPSPI\_Type \*base)

*Gets the LPSPI Receive Data Register address for a DMA operation.*

## Bus Operations

- bool [LPSPI\\_CheckTransferArgument](#) (LPSPI\_Type \*base, lpspi\_transfer\_t \*transfer, bool isEdma)  
*Check the argument for transfer.*
- static void [LPSPI\\_SetMasterSlaveMode](#) (LPSPI\_Type \*base, lpspi\_master\_slave\_mode\_t mode)  
*Configures the LPSPI for either master or slave.*
- static void [LPSPI\\_SelectTransferPCS](#) (LPSPI\_Type \*base, lpspi\_which\_pcs\_t select)  
*Configures the peripheral chip select used for the transfer.*
- static void [LPSPI\\_SetPCSContinous](#) (LPSPI\_Type \*base, bool IsContinous)  
*Set the PCS signal to continuous or uncontinuous mode.*
- static bool [LPSPI\\_IsMaster](#) (LPSPI\_Type \*base)  
*Returns whether the LPSPI module is in master mode.*
- static void [LPSPI\\_FlushFifo](#) (LPSPI\_Type \*base, bool flushTxFifo, bool flushRxFifo)  
*Flushes the LPSPI FIFOs.*
- static void [LPSPI\\_SetFifoWatermarks](#) (LPSPI\_Type \*base, uint32\_t txWater, uint32\_t rxWater)  
*Sets the transmit and receive FIFO watermark values.*
- static void [LPSPI\\_SetAllPcsPolarity](#) (LPSPI\_Type \*base, uint32\_t mask)  
*Configures all LPSPI peripheral chip select polarities simultaneously.*
- static void [LPSPI\\_SetFrameSize](#) (LPSPI\_Type \*base, uint32\_t frameSize)  
*Configures the frame size.*
- uint32\_t [LPSPI\\_MasterSetBaudRate](#) (LPSPI\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz, uint32\_t \*tcrPrescaleValue)  
*Sets the LPSPI baud rate in bits per second.*
- void [LPSPI\\_MasterSetDelayScaler](#) (LPSPI\_Type \*base, uint32\_t scaler, lpspi\_delay\_type\_t whichDelay)  
*Manually configures a specific LPSPI delay parameter (module must be disabled to change the delay values).*
- uint32\_t [LPSPI\\_MasterSetDelayTimes](#) (LPSPI\_Type \*base, uint32\_t delayTimeInNanoSec, lpspi\_delay\_type\_t whichDelay, uint32\_t srcClock\_Hz)  
*Calculates the delay based on the desired delay input in nanoseconds (module must be disabled to change the delay values).*
- static void [LPSPI\\_WriteData](#) (LPSPI\_Type \*base, uint32\_t data)  
*Writes data into the transmit data buffer.*
- static uint32\_t [LPSPI\\_ReadData](#) (LPSPI\_Type \*base)  
*Reads data from the data buffer.*
- void [LPSPI\\_SetDummyData](#) (LPSPI\_Type \*base, uint8\_t dummyData)  
*Set up the dummy data.*

## Transactional

- void [LPSPI\\_MasterTransferCreateHandle](#) (LPSPI\_Type \*base, lpspi\_master\_handle\_t \*handle, lpspi\_master\_transfer\_callback\_t callback, void \*userData)  
*Initializes the LPSPI master handle.*
- status\_t [LPSPI\\_MasterTransferBlocking](#) (LPSPI\_Type \*base, lpspi\_transfer\_t \*transfer)  
*LPSPI master transfer data using a polling method.*

- `status_t LPSPI_MasterTransferNonBlocking (LPSPI_Type *base, lpspi_master_handle_t *handle, lpspi_transfer_t *transfer)`  
*LPSPI master transfer data using an interrupt method.*
- `status_t LPSPI_MasterTransferGetCount (LPSPI_Type *base, lpspi_master_handle_t *handle, size_t *count)`  
*Gets the master transfer remaining bytes.*
- `void LPSPI_MasterTransferAbort (LPSPI_Type *base, lpspi_master_handle_t *handle)`  
*LPSPI master abort transfer which uses an interrupt method.*
- `void LPSPI_MasterTransferHandleIRQ (LPSPI_Type *base, lpspi_master_handle_t *handle)`  
*LPSPI Master IRQ handler function.*
- `void LPSPI_SlaveTransferCreateHandle (LPSPI_Type *base, lpspi_slave_handle_t *handle, lpspi_slave_transfer_callback_t callback, void *userData)`  
*Initializes the LPSPI slave handle.*
- `status_t LPSPI_SlaveTransferNonBlocking (LPSPI_Type *base, lpspi_slave_handle_t *handle, lpspi_transfer_t *transfer)`  
*LPSPI slave transfer data using an interrupt method.*
- `status_t LPSPI_SlaveTransferGetCount (LPSPI_Type *base, lpspi_slave_handle_t *handle, size_t *count)`  
*Gets the slave transfer remaining bytes.*
- `void LPSPI_SlaveTransferAbort (LPSPI_Type *base, lpspi_slave_handle_t *handle)`  
*LPSPI slave aborts a transfer which uses an interrupt method.*
- `void LPSPI_SlaveTransferHandleIRQ (LPSPI_Type *base, lpspi_slave_handle_t *handle)`  
*LPSPI Slave IRQ handler function.*

### 31.2.4 Data Structure Documentation

#### 31.2.4.1 struct lpspi\_master\_config\_t

##### Data Fields

- `uint32_t baudRate`  
*Baud Rate for LPSPI.*
- `uint32_t bitsPerFrame`  
*Bits per frame, minimum 8, maximum 4096.*
- `lpspi_clock_polarity_t cpol`  
*Clock polarity.*
- `lpspi_clock_phase_t cpha`  
*Clock phase.*
- `lpspi_shift_direction_t direction`  
*MSB or LSB data shift direction.*
- `uint32_t pcsToSckDelayInNanoSec`  
*PCS to SCK delay time in nanoseconds, setting to 0 sets the minimum delay.*
- `uint32_t lastSckToPcsDelayInNanoSec`  
*Last SCK to PCS delay time in nanoseconds, setting to 0 sets the minimum delay.*
- `uint32_t betweenTransferDelayInNanoSec`  
*After the SCK delay time with nanoseconds, setting to 0 sets the minimum delay.*
- `lpspi_which_pcs_t whichPcs`  
*Desired Peripheral Chip Select (PCS).*

- `lpspi_pcs_polarity_config_t pcsActiveHighOrLow`  
*Desired PCS active high or low.*
- `lpspi_pin_config_t pinCfg`  
*Configures which pins are used for input and output data during single bit transfers.*
- `lpspi_data_out_config_t dataOutConfig`  
*Configures if the output data is tristated between accesses (LPSPI\_PCS is negated).*
- `bool enableInputDelay`  
*Enable master to sample the input data on a delayed SCK.*

### Field Documentation

- (1) `uint32_t lpspi_master_config_t::baudRate`
- (2) `uint32_t lpspi_master_config_t::bitsPerFrame`
- (3) `lpspi_clock_polarity_t lpspi_master_config_t::cpol`
- (4) `lpspi_clock_phase_t lpspi_master_config_t::cpha`
- (5) `lpspi_shift_direction_t lpspi_master_config_t::direction`
- (6) `uint32_t lpspi_master_config_t::pcsToSckDelayInNanoSec`

It sets the boundary value if out of range.

- (7) `uint32_t lpspi_master_config_t::lastSckToPcsDelayInNanoSec`

It sets the boundary value if out of range.

- (8) `uint32_t lpspi_master_config_t::betweenTransferDelayInNanoSec`

It sets the boundary value if out of range.

- (9) `lpspi_which_pcs_t lpspi_master_config_t::whichPcs`
- (10) `lpspi_pin_config_t lpspi_master_config_t::pinCfg`
- (11) `lpspi_data_out_config_t lpspi_master_config_t::dataOutConfig`
- (12) `bool lpspi_master_config_t::enableInputDelay`

This can help improve slave setup time. Refer to device data sheet for specific time length.

### 31.2.4.2 struct lpspi\_slave\_config\_t

#### Data Fields

- `uint32_t bitsPerFrame`  
*Bits per frame, minimum 8, maximum 4096.*
- `lpspi_clock_polarity_t cpol`

- *Clock polarity.*  
• `lpspi_clock_phase_t cpha`
- *Clock phase.*  
• `lpspi_shift_direction_t direction`
- *MSB or LSB data shift direction.*  
• `lpspi_which_pcs_t whichPcs`
- *Desired Peripheral Chip Select (pcs)*  
• `lpspi_pcs_polarity_config_t pcsActiveHighOrLow`
- *Desired PCS active high or low.*  
• `lpspi_pin_config_t pinCfg`
- *Configures which pins are used for input and output data during single bit transfers.*  
• `lpspi_data_out_config_t dataOutConfig`
- *Configures if the output data is tristated between accesses (LPSPI\_PCS is negated).*

## Field Documentation

- (1) `uint32_t lpspi_slave_config_t::bitsPerFrame`
- (2) `lpspi_clock_polarity_t lpspi_slave_config_t::cpol`
- (3) `lpspi_clock_phase_t lpspi_slave_config_t::cpha`
- (4) `lpspi_shift_direction_t lpspi_slave_config_t::direction`
- (5) `lpspi_pin_config_t lpspi_slave_config_t::pinCfg`
- (6) `lpspi_data_out_config_t lpspi_slave_config_t::dataOutConfig`

### 31.2.4.3 struct lpspi\_transfer\_t

#### Data Fields

- `uint8_t * txData`  
*Send buffer.*
- `uint8_t * rxData`  
*Receive buffer.*
- `volatile size_t dataSize`  
*Transfer bytes.*
- `uint32_t configFlags`  
*Transfer transfer configuration flags.*

## Field Documentation

- (1) `uint8_t* lpspi_transfer_t::txData`
- (2) `uint8_t* lpspi_transfer_t::rxData`
- (3) `volatile size_t lpspi_transfer_t::dataSize`
- (4) `uint32_t lpspi_transfer_t::configFlags`

Set from `_lpspi_transfer_config_flag_for_master` if the transfer is used for master or `_lpspi_transfer_config_flag_for_slave` enumeration if the transfer is used for slave.

### 31.2.4.4 struct \_lpspi\_master\_handle

Forward declaration of the `_lpspi_master_handle` typedefs.

## Data Fields

- volatile bool `isPcsContinuous`  
*Is PCS continuous in transfer.*
- volatile bool `writeTcrInIsr`  
*A flag that whether should write TCR in ISR.*
- volatile bool `isByteSwap`  
*A flag that whether should byte swap.*
- volatile bool `isTxMask`  
*A flag that whether TCR[TXMSK] is set.*
- volatile uint16\_t `bytesPerFrame`  
*Number of bytes in each frame.*
- volatile uint8\_t `fifoSize`  
*FIFO dataSize.*
- volatile uint8\_t `rxWatermark`  
*Rx watermark.*
- volatile uint8\_t `bytesEachWrite`  
*Bytes for each write TDR.*
- volatile uint8\_t `bytesEachRead`  
*Bytes for each read RDR.*
- `uint8_t *volatile txData`  
*Send buffer.*
- `uint8_t *volatile rxData`  
*Receive buffer.*
- volatile size\_t `txRemainingByteCount`  
*Number of bytes remaining to send.*
- volatile size\_t `rxRemainingByteCount`  
*Number of bytes remaining to receive.*
- volatile uint32\_t `writeRegRemainingTimes`  
*Write TDR register remaining times.*
- volatile uint32\_t `readRegRemainingTimes`  
*Read RDR register remaining times.*

- `uint32_t totalByteCount`  
*Number of transfer bytes.*
- `uint32_t txBuffIfNull`  
*Used if the txData is NULL.*
- `volatile uint8_t state`  
*LPSPI transfer state , \_lpspi\_transfer\_state.*
- `lpspi_master_transfer_callback_t callback`  
*Completion callback.*
- `void * userData`  
*Callback user data.*

## Field Documentation

- (1) volatile bool `lpspi_master_handle_t::isPcsContinuous`
- (2) volatile bool `lpspi_master_handle_t::writeTcrInIsr`
- (3) volatile bool `lpspi_master_handle_t::isByteSwap`
- (4) volatile bool `lpspi_master_handle_t::isTxMask`
- (5) volatile uint8\_t `lpspi_master_handle_t::fifoSize`
- (6) volatile uint8\_t `lpspi_master_handle_t::rxWatermark`
- (7) volatile uint8\_t `lpspi_master_handle_t::bytesEachWrite`
- (8) volatile uint8\_t `lpspi_master_handle_t::bytesEachRead`
- (9) uint8\_t\* volatile `lpspi_master_handle_t::txData`
- (10) uint8\_t\* volatile `lpspi_master_handle_t::rxData`
- (11) volatile size\_t `lpspi_master_handle_t::txRemainingByteCount`
- (12) volatile size\_t `lpspi_master_handle_t::rxRemainingByteCount`
- (13) volatile uint32\_t `lpspi_master_handle_t::writeRegRemainingTimes`
- (14) volatile uint32\_t `lpspi_master_handle_t::readRegRemainingTimes`
- (15) uint32\_t `lpspi_master_handle_t::txBuffIfNull`
- (16) volatile uint8\_t `lpspi_master_handle_t::state`
- (17) `lpspi_master_transfer_callback_t lpspi_master_handle_t::callback`
- (18) void\* `lpspi_master_handle_t::userData`

### 31.2.4.5 struct \_lpspi\_slave\_handle

Forward declaration of the `_lpspi_slave_handle` typedefs.

## Data Fields

- volatile bool `isByteSwap`  
*A flag that whether should byte swap.*
- volatile uint8\_t `fifoSize`  
*FIFO dataSize.*
- volatile uint8\_t `rxWatermark`  
*Rx watermark.*

- volatile uint8\_t **bytesEachWrite**  
*Bytes for each write TDR.*
- volatile uint8\_t **bytesEachRead**  
*Bytes for each read RDR.*
- uint8\_t \*volatile **txData**  
*Send buffer.*
- uint8\_t \*volatile **rxData**  
*Receive buffer.*
- volatile size\_t **txRemainingByteCount**  
*Number of bytes remaining to send.*
- volatile size\_t **rxRemainingByteCount**  
*Number of bytes remaining to receive.*
- volatile uint32\_t **writeRegRemainingTimes**  
*Write TDR register remaining times.*
- volatile uint32\_t **readRegRemainingTimes**  
*Read RDR register remaining times.*
- uint32\_t **totalByteCount**  
*Number of transfer bytes.*
- volatile uint8\_t **state**  
*LPSPI transfer state , \_lpspi\_transfer\_state.*
- volatile uint32\_t **errorCount**  
*Error count for slave transfer.*
- **lpspi\_slave\_transfer\_callback\_t callback**  
*Completion callback.*
- void \* **userData**  
*Callback user data.*

## Field Documentation

- (1) volatile bool lpspi\_slave\_handle\_t::isByteSwap
- (2) volatile uint8\_t lpspi\_slave\_handle\_t::fifoSize
- (3) volatile uint8\_t lpspi\_slave\_handle\_t::rxWatermark
- (4) volatile uint8\_t lpspi\_slave\_handle\_t::bytesEachWrite
- (5) volatile uint8\_t lpspi\_slave\_handle\_t::bytesEachRead
- (6) uint8\_t\* volatile lpspi\_slave\_handle\_t::txData
- (7) uint8\_t\* volatile lpspi\_slave\_handle\_t::rxData
- (8) volatile size\_t lpspi\_slave\_handle\_t::txRemainingByteCount
- (9) volatile size\_t lpspi\_slave\_handle\_t::rxRemainingByteCount
- (10) volatile uint32\_t lpspi\_slave\_handle\_t::writeRegRemainingTimes
- (11) volatile uint32\_t lpspi\_slave\_handle\_t::readRegRemainingTimes
- (12) volatile uint8\_t lpspi\_slave\_handle\_t::state
- (13) volatile uint32\_t lpspi\_slave\_handle\_t::errorCount
- (14) lpspi\_slave\_transfer\_callback\_t lpspi\_slave\_handle\_t::callback
- (15) void\* lpspi\_slave\_handle\_t::userData

### 31.2.5 Macro Definition Documentation

31.2.5.1 #define FSL\_LPSPI\_DRIVER\_VERSION (MAKE\_VERSION(2, 4, 5))

31.2.5.2 #define LPSPI\_DUMMY\_DATA (0x00U)

Dummy data used for tx if there is not txData.

31.2.5.3 `#define SPI_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`

31.2.5.4 `#define LPSPI_MASTER_PCS_SHIFT (4U)`

31.2.5.5 `#define LPSPI_MASTER_PCS_MASK (0xF0U)`

31.2.5.6 `#define LPSPI_SLAVE_PCS_SHIFT (4U)`

31.2.5.7 `#define LPSPI_SLAVE_PCS_MASK (0xF0U)`

## 31.2.6 Typedef Documentation

31.2.6.1 `typedef void(* lpspi_master_transfer_callback_t)(LPSPI_Type *base, lpspi_master_handle_t *handle, status_t status, void *userData)`

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	Pointer to the handle for the LPSPI master.
<i>status</i>	Success or error code describing whether the transfer is completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

### 31.2.6.2 `typedef void(* lpspi_slave_transfer_callback_t)(LPSPI_Type *base, lpspi_slave_handle_t *handle, status_t status, void *userData)`

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	Pointer to the handle for the LPSPI slave.
<i>status</i>	Success or error code describing whether the transfer is completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

## 31.2.7 Enumeration Type Documentation

### 31.2.7.1 anonymous enum

Enumerator

*kStatus\_LPSPI\_Busy* LPSPI transfer is busy.  
*kStatus\_LPSPI\_Error* LPSPI driver error.  
*kStatus\_LPSPI\_Idle* LPSPI is idle.  
*kStatus\_LPSPI\_OutOfRange* LPSPI transfer out Of range.  
*kStatus\_LPSPI\_Timeout* LPSPI timeout polling status flags.

### 31.2.7.2 enum \_lpspi\_flags

Enumerator

*kLPSPI\_TxDataRequestFlag* Transmit data flag.  
*kLPSPI\_RxDataReadyFlag* Receive data flag.  
*kLPSPI\_WordCompleteFlag* Word Complete flag.  
*kLPSPI\_FrameCompleteFlag* Frame Complete flag.  
*kLPSPI\_TransferCompleteFlag* Transfer Complete flag.  
*kLPSPI\_TransmitErrorFlag* Transmit Error flag (FIFO underrun)  
*kLPSPI\_ReceiveErrorFlag* Receive Error flag (FIFO overrun)

*kLPSPI\_DataMatchFlag* Data Match flag.  
*kLPSPI\_ModuleBusyFlag* Module Busy flag.  
*kLPSPI\_AllStatusFlag* Used for clearing all w1c status flags.

### 31.2.7.3 enum \_lpspi\_interrupt\_enable

Enumerator

*kLPSPI\_TxInterruptEnable* Transmit data interrupt enable.  
*kLPSPI\_RxInterruptEnable* Receive data interrupt enable.  
*kLPSPI\_WordCompleteInterruptEnable* Word complete interrupt enable.  
*kLPSPI\_FrameCompleteInterruptEnable* Frame complete interrupt enable.  
*kLPSPI\_TransferCompleteInterruptEnable* Transfer complete interrupt enable.  
*kLPSPI\_TransmitErrorInterruptEnable* Transmit error interrupt enable(FIFO underrun)  
*kLPSPI\_ReceiveErrorInterruptEnable* Receive Error interrupt enable (FIFO overrun)  
*kLPSPI\_DataMatchInterruptEnable* Data Match interrupt enable.  
*kLPSPI\_AllInterruptEnable* All above interrupts enable.

### 31.2.7.4 enum \_lpspi\_dma\_enable

Enumerator

*kLPSPI\_TxDmaEnable* Transmit data DMA enable.  
*kLPSPI\_RxDmaEnable* Receive data DMA enable.

### 31.2.7.5 enum lpspi\_master\_slave\_mode\_t

Enumerator

*kLPSPI\_Master* LPSPI peripheral operates in master mode.  
*kLPSPI\_Slave* LPSPI peripheral operates in slave mode.

### 31.2.7.6 enum lpspi\_which\_pcs\_t

Enumerator

*kLPSPI\_Pcs0* PCS[0].  
*kLPSPI\_Pcs1* PCS[1].  
*kLPSPI\_Pcs2* PCS[2].  
*kLPSPI\_Pcs3* PCS[3].

### 31.2.7.7 enum lpspi\_pcs\_polarity\_config\_t

Enumerator

*kLPSPI\_PcsActiveHigh* PCS Active High (idles low)

*kLPSPI\_PcsActiveLow* PCS Active Low (idles high)

### 31.2.7.8 enum \_lpspi\_pcs\_polarity

Enumerator

*kLPSPI\_Pcs0ActiveLow* Pcs0 Active Low (idles high).

*kLPSPI\_Pcs1ActiveLow* Pcs1 Active Low (idles high).

*kLPSPI\_Pcs2ActiveLow* Pcs2 Active Low (idles high).

*kLPSPI\_Pcs3ActiveLow* Pcs3 Active Low (idles high).

*kLPSPI\_PcsAllActiveLow* Pcs0 to Pcs5 Active Low (idles high).

### 31.2.7.9 enum lpspi\_clock\_polarity\_t

Enumerator

*kLPSPI\_ClockPolarityActiveHigh* CPOL=0. Active-high LPSPI clock (idles low)

*kLPSPI\_ClockPolarityActiveLow* CPOL=1. Active-low LPSPI clock (idles high)

### 31.2.7.10 enum lpspi\_clock\_phase\_t

Enumerator

*kLPSPI\_ClockPhaseFirstEdge* CPHA=0. Data is captured on the leading edge of the SCK and changed on the following edge.

*kLPSPI\_ClockPhaseSecondEdge* CPHA=1. Data is changed on the leading edge of the SCK and captured on the following edge.

### 31.2.7.11 enum lpspi\_shift\_direction\_t

Enumerator

*kLPSPI\_MsbFirst* Data transfers start with most significant bit.

*kLPSPI\_LsbFirst* Data transfers start with least significant bit.

### 31.2.7.12 enum lpspi\_host\_request\_select\_t

Enumerator

*kLPSPI\_HostReqExtPin* Host Request is an ext pin.

*kLPSPI\_HostReqInternalTrigger* Host Request is an internal trigger.

### 31.2.7.13 enum lpspi\_match\_config\_t

Enumerator

*kLPSI\_MatchDisabled* LPSPI Match Disabled.

*kLPSI\_1stWordEqualsM0orM1* LPSPI Match Enabled.

*kLPSI\_AnyWordEqualsM0orM1* LPSPI Match Enabled.

*kLPSI\_1stWordEqualsM0and2ndWordEqualsM1* LPSPI Match Enabled.

*kLPSI\_AnyWordEqualsM0andNxtWordEqualsM1* LPSPI Match Enabled.

*kLPSI\_1stWordAndM1EqualsM0andM1* LPSPI Match Enabled.

*kLPSI\_AnyWordAndM1EqualsM0andM1* LPSPI Match Enabled.

### 31.2.7.14 enum lpspi\_pin\_config\_t

Enumerator

*kLPSPI\_SdiInSdoOut* LPSPI SDI input, SDO output.

*kLPSPI\_SdiInSdiOut* LPSPI SDI input, SDI output.

*kLPSPI\_SdoInSdoOut* LPSPI SDO input, SDO output.

*kLPSPI\_SdoInSdiOut* LPSPI SDO input, SDI output.

### 31.2.7.15 enum lpspi\_data\_out\_config\_t

Enumerator

*kLpspiDataOutRetained* Data out retains last value when chip select is de-asserted.

*kLpspiDataOutTristate* Data out is tristated when chip select is de-asserted.

### 31.2.7.16 enum lpspi\_transfer\_width\_t

Enumerator

*kLPSPI\_SingleBitXfer* 1-bit shift at a time, data out on SDO, in on SDI (normal mode)

*kLPSPI\_TwoBitXfer* 2-bits shift out on SDO/SDI and in on SDO/SDI

*kLPSPI\_FourBitXfer* 4-bits shift out on SDO/SDI/PCS[3:2] and in on SDO/SDI/PCS[3:2]

### 31.2.7.17 enum lpspi\_delay\_type\_t

Enumerator

*kLPSPI\_PcsToSck* PCS-to-SCK delay.

*kLPSPI\_LastSckToPcs* Last SCK edge to PCS delay.

*kLPSPI\_BetweenTransfer* Delay between transfers.

### 31.2.7.18 enum \_lpspi\_transfer\_config\_flag\_for\_master

Enumerator

*kLPSPI\_MasterPcs0* LPSPI master transfer use PCS0 signal.

*kLPSPI\_MasterPcs1* LPSPI master transfer use PCS1 signal.

*kLPSPI\_MasterPcs2* LPSPI master transfer use PCS2 signal.

*kLPSPI\_MasterPcs3* LPSPI master transfer use PCS3 signal.

*kLPSPI\_MasterPcsContinuous* Is PCS signal continuous.

*kLPSPI\_MasterByteSwap* Is master swap the byte. For example, when want to send data 1 2 3 4 5 6 7 8 (suppose you set lpspi\_shift\_direction\_t to MSB).

1. If you set bitPerFrame = 8 , no matter the kLPSPI\_MasterByteSwap flag is used or not, the waveform is 1 2 3 4 5 6 7 8.
2. If you set bitPerFrame = 16 : (1) the waveform is 2 1 4 3 6 5 8 7 if you do not use the kLPSPI\_MasterByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_MasterByteSwap flag.
3. If you set bitPerFrame = 32 : (1) the waveform is 4 3 2 1 8 7 6 5 if you do not use the kLPSPI\_MasterByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_MasterByteSwap flag.

### 31.2.7.19 enum \_lpspi\_transfer\_config\_flag\_for\_slave

Enumerator

*kLPSPI\_SlavePcs0* LPSPI slave transfer use PCS0 signal.

*kLPSPI\_SlavePcs1* LPSPI slave transfer use PCS1 signal.

*kLPSPI\_SlavePcs2* LPSPI slave transfer use PCS2 signal.

*kLPSPI\_SlavePcs3* LPSPI slave transfer use PCS3 signal.

*kLPSPI\_SlaveByteSwap* Is slave swap the byte. For example, when want to send data 1 2 3 4 5 6 7 8 (suppose you set lpspi\_shift\_direction\_t to MSB).

1. If you set bitPerFrame = 8 , no matter the kLPSPI\_SlaveByteSwap flag is used or not, the waveform is 1 2 3 4 5 6 7 8.
2. If you set bitPerFrame = 16 : (1) the waveform is 2 1 4 3 6 5 8 7 if you do not use the kLPSPI\_SlaveByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_SlaveByteSwap flag.

3. If you set bitPerFrame = 32 : (1) the waveform is 4 3 2 1 8 7 6 5 if you do not use the kLPSPI\_SlaveByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_SlaveByteSwap flag.

### 31.2.7.20 enum \_lpspi\_transfer\_state

Enumerator

**kLPSPI\_Idle** Nothing in the transmitter/receiver.

**kLPSPI\_Busy** Transfer queue is not finished.

**kLPSPI\_Error** Transfer error.

## 31.2.8 Function Documentation

### 31.2.8.1 void LPSPI\_MasterInit ( LPSPI\_Type \* *base*, const lpspi\_master\_config\_t \* *masterConfig*, uint32\_t *srcClock\_Hz* )

Parameters

<i>base</i>	LPSPI peripheral address.
<i>masterConfig</i>	Pointer to structure <a href="#">lpspi_master_config_t</a> .
<i>srcClock_Hz</i>	Module source input clock in Hertz

### 31.2.8.2 void LPSPI\_MasterGetDefaultConfig ( lpspi\_master\_config\_t \* *masterConfig* )

This API initializes the configuration structure for [LPSPI\\_MasterInit\(\)](#). The initialized structure can remain unchanged in [LPSPI\\_MasterInit\(\)](#), or can be modified before calling the [LPSPI\\_MasterInit\(\)](#). Example:

```
* lpspi_master_config_t masterConfig;
* LPSPI_MasterGetDefaultConfig(&masterConfig);
*
```

Parameters

<i>masterConfig</i>	pointer to <a href="#">lpspi_master_config_t</a> structure
---------------------	--

### 31.2.8.3 void LPSPI\_SlaveInit ( LPSPI\_Type \* *base*, const lpspi\_slave\_config\_t \* *slaveConfig* )

Parameters

<i>base</i>	LPSPI peripheral address.
<i>slaveConfig</i>	Pointer to a structure <a href="#">lpspi_slave_config_t</a> .

### 31.2.8.4 void LPSPI\_SlaveGetDefaultConfig ( [lpspi\\_slave\\_config\\_t](#) \* *slaveConfig* )

This API initializes the configuration structure for [LPSPI\\_SlaveInit\(\)](#). The initialized structure can remain unchanged in [LPSPI\\_SlaveInit\(\)](#) or can be modified before calling the [LPSPI\\_SlaveInit\(\)](#). Example:

```
* lpspi_slave_config_t slaveConfig;
* LPSPI_SlaveGetDefaultConfig(&slaveConfig);
*
```

Parameters

<i>slaveConfig</i>	pointer to <a href="#">lpspi_slave_config_t</a> structure.
--------------------	--

### 31.2.8.5 void LPSPI\_Deinit ( [LPSPI\\_Type](#) \* *base* )

Call this API to disable the LPSPI clock.

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

### 31.2.8.6 void LPSPI\_Reset ( [LPSPI\\_Type](#) \* *base* )

Note that this function sets all registers to reset state. As a result, the LPSPI module can't work after calling this API.

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

### 31.2.8.7 [uint32\\_t](#) LPSPI\_GetInstance ( [LPSPI\\_Type](#) \* *base* )

Parameters

<i>base</i>	LPSPI peripheral base address.
-------------	--------------------------------

Returns

LPSPI instance.

### 31.2.8.8 static void LPSPI\_Enable ( LPSPI\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
<i>enable</i>	Pass true to enable module, false to disable module.

### 31.2.8.9 static uint32\_t LPSPI\_GetStatusFlags ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The LPSPI status(in SR register).

### 31.2.8.10 static uint8\_t LPSPI\_GetTxFifoSize ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The LPSPI Tx FIFO size.

### 31.2.8.11 static uint8\_t LPSPI\_GetRxFifoSize ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The LPSPI Rx FIFO size.

### 31.2.8.12 static uint32\_t LPSPI\_GetTxFifoCount ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The number of words in the transmit FIFO.

### 31.2.8.13 static uint32\_t LPSPI\_GetRxFifoCount ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The number of words in the receive FIFO.

### 31.2.8.14 static void LPSPI\_ClearStatusFlags ( LPSPI\_Type \* *base*, uint32\_t *statusFlags* ) [inline], [static]

This function clears the desired status bit by using a write-1-to-clear. The user passes in the base and the desired status flag bit to clear. The list of status flags is defined in the \_lpspi\_flags. Example usage:

```
* LPSPI_ClearStatusFlags(base, kLPSPI_TxDataRequestFlag |
    kLPSPI_RxDataReadyFlag);
*
```

Parameters

<i>base</i>	LPSPI peripheral address.
<i>statusFlags</i>	The status flag used from type _lpspi_flags.

< The status flags are cleared by writing 1 (w1c).

### 31.2.8.15 static void LPSPI\_EnableInterrupts ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function configures the various interrupt masks of the LPSPI. The parameters are base and an interrupt mask. Note that, for Tx fill and Rx FIFO drain requests, enabling the interrupt request disables the DMA request.

```
* LPSPI_EnableInterrupts(base, kLPSPI_TxInterruptEnable |
    kLPSPI_RxInterruptEnable );
*
```

Parameters

<i>base</i>	LPSPI peripheral address.
<i>mask</i>	The interrupt mask; Use the enum _lpspi_interrupt_enable.

### 31.2.8.16 static void LPSPI\_DisableInterrupts ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

```
* LPSPI_DisableInterrupts(base, kLPSPI_TxInterruptEnable |
    kLPSPI_RxInterruptEnable );
*
```

Parameters

<i>base</i>	LPSPI peripheral address.
<i>mask</i>	The interrupt mask; Use the enum _lpspi_interrupt_enable.

### 31.2.8.17 static void LPSPI\_EnableDMA ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function configures the Rx and Tx DMA mask of the LPSPI. The parameters are base and a DMA mask.

```
* LPSPI_EnableDMA(base, kLPSPI_TxDmaEnable |
    kLPSPI_Rx_dmaEnable );
*
```

Parameters

<i>base</i>	LPSPI peripheral address.
<i>mask</i>	The interrupt mask; Use the enum _lpspi_dma_enable.

### 31.2.8.18 static void LPSPI\_DisableDMA ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function configures the Rx and Tx DMA mask of the LPSPI. The parameters are base and a DMA mask.

```
*   SPI_DisableDMA(base, kLPSPI_TxDmaEnable |
                  kLPSPI_Rx_dmaEnable);
*
```

Parameters

<i>base</i>	LPSPI peripheral address.
<i>mask</i>	The interrupt mask; Use the enum _lpspi_dma_enable.

### 31.2.8.19 static uint32\_t LPSPI\_GetTxRegisterAddress ( LPSPI\_Type \* *base* ) [inline], [static]

This function gets the LPSPI Transmit Data Register address because this value is needed for the DMA operation. This function can be used for either master or slave mode.

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The LPSPI Transmit Data Register address.

### 31.2.8.20 static uint32\_t LPSPI\_GetRxRegisterAddress ( LPSPI\_Type \* *base* ) [inline], [static]

This function gets the LPSPI Receive Data Register address because this value is needed for the DMA operation. This function can be used for either master or slave mode.

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The LPSPI Receive Data Register address.

### 31.2.8.21 **bool LPSPI\_CheckTransferArgument ( LPSPI\_Type \* *base*, lpspi\_transfer\_t \* *transfer*, bool *isEdma* )**

Parameters

<i>base</i>	LPSPI peripheral address.
<i>transfer</i>	the transfer struct to be used.
<i>isEdma</i>	True to check for EDMA transfer, false to check interrupt non-blocking transfer

Returns

Return true for right and false for wrong.

### 31.2.8.22 **static void LPSPI\_SetMasterSlaveMode ( LPSPI\_Type \* *base*, lpspi\_master\_slave\_mode\_t *mode* ) [inline], [static]**

Note that the CFGR1 should only be written when the LPSPI is disabled (LPSPIx\_CR\_MEN = 0).

Parameters

<i>base</i>	LPSPI peripheral address.
<i>mode</i>	Mode setting (master or slave) of type lpspi_master_slave_mode_t.

### 31.2.8.23 **static void LPSPI\_SelectTransferPCS ( LPSPI\_Type \* *base*, lpspi\_which\_pcs\_t *select* ) [inline], [static]**

Parameters

<i>base</i>	LPSPI peripheral address.
<i>select</i>	LPSPI Peripheral Chip Select (PCS) configuration.

### 31.2.8.24 static void LPSPI\_SetPCSContinuous ( LPSPI\_Type \* *base*, bool *IsContinuous* ) [inline], [static]

Note

In master mode, continuous transfer will keep the PCS asserted at the end of the frame size, until a command word is received that starts a new frame. So PCS must be set back to uncontinuous when transfer finishes. In slave mode, when continuous transfer is enabled, the LPSPI will only transmit the first frame size bits, after that the LPSPI will transmit received data back (assuming a 32-bit shift register).

Parameters

<i>base</i>	LPSPI peripheral address.
<i>IsContinuous</i>	True to set the transfer PCS to continuous mode, false to set to uncontinuous mode.

### 31.2.8.25 static bool LPSPI\_IsMaster ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

Returns true if the module is in master mode or false if the module is in slave mode.

### 31.2.8.26 static void LPSPI\_FlushFifo ( LPSPI\_Type \* *base*, bool *flushTxFifo*, bool *flushRxFifo* ) [inline], [static]

Parameters

<i>base</i>	LPSPI peripheral address.
<i>flushTxFifo</i>	Flushes (true) the Tx FIFO, else do not flush (false) the Tx FIFO.
<i>flushRxFifo</i>	Flushes (true) the Rx FIFO, else do not flush (false) the Rx FIFO.

### 31.2.8.27 static void LPSPI\_SetFifoWatermarks ( LPSPI\_Type \* *base*, uint32\_t *txWater*, uint32\_t *rxWater* ) [inline], [static]

This function allows the user to set the receive and transmit FIFO watermarks. The function does not compare the watermark settings to the FIFO size. The FIFO watermark should not be equal to or greater than the FIFO size. It is up to the higher level driver to make this check.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>txWater</i>	The TX FIFO watermark value. Writing a value equal or greater than the FIFO size is truncated.
<i>rxWater</i>	The RX FIFO watermark value. Writing a value equal or greater than the FIFO size is truncated.

### 31.2.8.28 static void LPSPI\_SetAllPcsPolarity ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Note that the CGR1 should only be written when the LPSPI is disabled (LPSPIx\_CR\_MEN = 0).

This is an example: PCS0 and PCS1 set to active low and other PCSs set to active high. Note that the number of PCS is device-specific.

```
* LPSPI_SetAllPcsPolarity(base, kLPSPI_Pcs0ActiveLow |
    kLPSPI_Pcs1ActiveLow);
*
```

Parameters

<i>base</i>	LPSPI peripheral address.
<i>mask</i>	The PCS polarity mask; Use the enum _lpspi_pcs_polarity.

### 31.2.8.29 static void LPSPI\_SetFrameSize ( LPSPI\_Type \* *base*, uint32\_t *frameSize* ) [inline], [static]

The minimum frame size is 8-bits and the maximum frame size is 4096-bits. If the frame size is less than or equal to 32-bits, the word size and frame size are identical. If the frame size is greater than 32-bits, the

word size is 32-bits for each word except the last (the last word contains the remainder bits if the frame size is not divisible by 32). The minimum word size is 2-bits. A frame size of 33-bits (or similar) is not supported.

Note 1: The transmit command register should be initialized before enabling the LPSPI in slave mode, although the command register does not update until after the LPSPI is enabled. After it is enabled, the transmit command register should only be changed if the LPSPI is idle.

Note 2: The transmit and command FIFO is a combined FIFO that includes both transmit data and command words. That means the TCR register should be written to when the Tx FIFO is not full.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>frameSize</i>	The frame size in number of bits.

### 31.2.8.30 `uint32_t LPSPI_MasterSetBaudRate ( LPSPI_Type * base, uint32_t baudRate_Bps, uint32_t srcClock_Hz, uint32_t * tcrPrescaleValue )`

This function takes in the desired bitsPerSec (baud rate) and calculates the nearest possible baud rate without exceeding the desired baud rate and returns the calculated baud rate in bits-per-second. It requires the caller to provide the frequency of the module source clock (in Hertz). Note that the baud rate does not go into effect until the Transmit Control Register (TCR) is programmed with the prescale value. Hence, this function returns the prescale tcrPrescaleValue parameter for later programming in the TCR. The higher level peripheral driver should alert the user of an out of range baud rate input.

Note that the LPSPI module must first be disabled before configuring this. Note that the LPSPI module must be configured for master mode before configuring this.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>baudRate_Bps</i>	The desired baud rate in bits per second.
<i>srcClock_Hz</i>	Module source input clock in Hertz.
<i>tcrPrescale-Value</i>	The TCR prescale value needed to program the TCR.

## Returns

The actual calculated baud rate. This function may also return a "0" if the LPSPI is not configured for master mode or if the LPSPI module is not disabled.

### **31.2.8.31 void LPSPI\_MasterSetDelayScaler ( *LPSPI\_Type* \* *base*, *uint32\_t* *scaler*, *lpspi\_delay\_type\_t* *whichDelay* )**

This function configures the following: SCK to PCS delay, or PCS to SCK delay, or The configurations must occur between the transfer delay.

The delay names are available in type *lpspi\_delay\_type\_t*.

The user passes the desired delay along with the delay value. This allows the user to directly set the delay values if they have pre-calculated them or if they simply wish to manually increment the value.

Note that the LPSPI module must first be disabled before configuring this. Note that the LPSPI module must be configured for master mode before configuring this.

## Parameters

<i>base</i>	LPSPI peripheral address.
<i>scaler</i>	The 8-bit delay value 0x00 to 0xFF (255).
<i>whichDelay</i>	The desired delay to configure, must be of type <i>lpspi_delay_type_t</i> .

### **31.2.8.32 *uint32\_t* LPSPI\_MasterSetDelayTimes ( *LPSPI\_Type* \* *base*, *uint32\_t* *delayTimeInNanoSec*, *lpspi\_delay\_type\_t* *whichDelay*, *uint32\_t* *srcClock\_Hz* )**

This function calculates the values for the following: SCK to PCS delay, or PCS to SCK delay, or The configurations must occur between the transfer delay.

The delay names are available in type *lpspi\_delay\_type\_t*.

The user passes the desired delay and the desired delay value in nano-seconds. The function calculates the value needed for the desired delay parameter and returns the actual calculated delay because an exact delay match may not be possible. In this case, the closest match is calculated without going below the desired delay value input. It is possible to input a very large delay value that exceeds the capability of the part, in which case the maximum supported delay is returned. It is up to the higher level peripheral driver to alert the user of an out of range delay input.

Note that the LPSPI module must be configured for master mode before configuring this. And note that the *delayTime* = *LPSPI\_clockSource* / (*PRESCALE* \* *Delay\_scaler*).

Parameters

<i>base</i>	LPSPI peripheral address.
<i>delayTimeIn-NanoSec</i>	The desired delay value in nano-seconds.
<i>whichDelay</i>	The desired delay to configuration, which must be of type lpspi_delay_type_t.
<i>srcClock_Hz</i>	Module source input clock in Hertz.

Returns

actual Calculated delay value in nano-seconds.

### 31.2.8.33 static void LPSPI\_WriteData ( LPSPI\_Type \* *base*, uint32\_t *data* ) [inline], [static]

This function writes data passed in by the user to the Transmit Data Register (TDR). The user can pass up to 32-bits of data to load into the TDR. If the frame size exceeds 32-bits, the user has to manage sending the data one 32-bit word at a time. Any writes to the TDR result in an immediate push to the transmit FIFO. This function can be used for either master or slave modes.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>data</i>	The data word to be sent.

### 31.2.8.34 static uint32\_t LPSPI\_ReadData ( LPSPI\_Type \* *base* ) [inline], [static]

This function reads the data from the Receive Data Register (RDR). This function can be used for either master or slave mode.

Parameters

<i>base</i>	LPSPI peripheral address.
-------------	---------------------------

Returns

The data read from the data buffer.

### 31.2.8.35 void LPSPI\_SetDummyData ( LPSPI\_Type \* *base*, uint8\_t *dummyData* )

Parameters

<i>base</i>	LPSPI peripheral address.
<i>dummyData</i>	Data to be transferred when tx buffer is NULL. Note: This API has no effect when LPSPI in slave interrupt mode, because driver will set the TXMSK bit to 1 if txData is NULL, no data is loaded from transmit FIFO and output pin is tristated.

**31.2.8.36 void LPSPI\_MasterTransferCreateHandle ( **LPSPI\_Type** \* *base*,  
**lpspi\_master\_handle\_t** \* *handle*, **lpspi\_master\_transfer\_callback\_t** *callback*,  
**void** \* *userData* )**

This function initializes the LPSPI handle, which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	LPSPI handle pointer to <b>lpspi_master_handle_t</b> .
<i>callback</i>	DSPI callback.
<i>userData</i>	callback function parameter.

**31.2.8.37 status\_t LPSPI\_MasterTransferBlocking ( **LPSPI\_Type** \* *base*, **lpspi\_transfer\_t** \* *transfer* )**

This function transfers data using a polling method. This is a blocking function, which does not return until all transfers have been completed.

Note: The transfer data size should be integer multiples of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not integer multiples of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>transfer</i>	pointer to <b>lpspi_transfer_t</b> structure.

Returns

status of **status\_t**.

### 31.2.8.38 status\_t LPSPI\_MasterTransferNonBlocking ( **LPSPI\_Type** \* *base*, **lpspi\_master\_handle\_t** \* *handle*, **lpspi\_transfer\_t** \* *transfer* )

This function transfers data using an interrupt method. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be integer multiples of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not integer multiples of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to <b>lpspi_master_handle_t</b> structure which stores the transfer state.
<i>transfer</i>	pointer to <b>lpspi_transfer_t</b> structure.

Returns

status of status\_t.

### 31.2.8.39 status\_t LPSPI\_MasterTransferGetCount ( **LPSPI\_Type** \* *base*, **lpspi\_master\_handle\_t** \* *handle*, **size\_t** \* *count* )

This function gets the master transfer remaining bytes.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to <b>lpspi_master_handle_t</b> structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Returns

status of status\_t.

### 31.2.8.40 void LPSPI\_MasterTransferAbort ( **LPSPI\_Type** \* *base*, **lpspi\_master\_handle\_t** \* *handle* )

This function aborts a transfer which uses an interrupt method.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to lpspi_master_handle_t structure which stores the transfer state.

### 31.2.8.41 void LPSPI\_MasterTransferHandleIRQ ( LPSPI\_Type \* *base*, lpspi\_master\_handle\_t \* *handle* )

This function processes the LPSPI transmit and receive IRQ.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to lpspi_master_handle_t structure which stores the transfer state.

### 31.2.8.42 void LPSPI\_SlaveTransferCreateHandle ( LPSPI\_Type \* *base*, lpspi\_slave\_handle\_t \* *handle*, lpspi\_slave\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the LPSPI handle, which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	LPSPI handle pointer to lpspi_slave_handle_t.
<i>callback</i>	DSPI callback.
<i>userData</i>	callback function parameter.

### 31.2.8.43 status\_t LPSPI\_SlaveTransferNonBlocking ( LPSPI\_Type \* *base*, lpspi\_slave\_handle\_t \* *handle*, lpspi\_transfer\_t \* *transfer* )

This function transfer data using an interrupt method. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be integer multiples of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not an integer multiple of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to <code>lpspi_slave_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	pointer to <code>lpspi_transfer_t</code> structure.

Returns

status of `status_t`.

### 31.2.8.44 `status_t LPSPI_SlaveTransferGetCount ( LPSPI_Type * base, lpspi_slave_handle_t * handle, size_t * count )`

This function gets the slave transfer remaining bytes.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to <code>lpspi_slave_handle_t</code> structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Returns

status of `status_t`.

### 31.2.8.45 `void LPSPI_SlaveTransferAbort ( LPSPI_Type * base, lpspi_slave_handle_t * handle )`

This function aborts a transfer which uses an interrupt method.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to <code>lpspi_slave_handle_t</code> structure which stores the transfer state.

### 31.2.8.46 `void LPSPI_SlaveTransferHandleIRQ ( LPSPI_Type * base, lpspi_slave_handle_t * handle )`

This function processes the LPSPI transmit and receives an IRQ.

Parameters

<i>base</i>	LPSPI peripheral address.
<i>handle</i>	pointer to lpspi_slave_handle_t structure which stores the transfer state.

### 31.2.9 Variable Documentation

#### 31.2.9.1 volatile uint8\_t g\_lpspiDummyData[]

## 31.3 LPSPI eDMA Driver

### 31.3.1 Overview

#### Data Structures

- struct `lpspi_master_edma_handle_t`  
*LPSPI master eDMA transfer handle structure used for transactional API.* [More...](#)
- struct `lpspi_slave_edma_handle_t`  
*LPSPI slave eDMA transfer handle structure used for transactional API.* [More...](#)

#### TypeDefs

- typedef void(\* `lpspi_master_edma_transfer_callback_t`)(LPSPI\_Type \*base, lpspi\_master\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*
- typedef void(\* `lpspi_slave_edma_transfer_callback_t`)(LPSPI\_Type \*base, lpspi\_slave\_edma\_handle\_t \*handle, status\_t status, void \*userData)  
*Completion callback function pointer type.*

#### Functions

- void `LPSPI_MasterTransferCreateHandleEDMA` (LPSPI\_Type \*base, lpspi\_master\_edma\_handle\_t \*handle, `lpspi_master_edma_transfer_callback_t` callback, void \*userData, `edma_handle_t` \*edmaRxRegToRxDataHandle, `edma_handle_t` \*edmaTxDataToTxRegHandle)  
*Initializes the LPSPI master eDMA handle.*
- status\_t `LPSPI_MasterTransferEDMA` (LPSPI\_Type \*base, lpspi\_master\_edma\_handle\_t \*handle, `lpspi_transfer_t` \*transfer)  
*LPSPI master transfer data using eDMA.*
- status\_t `LPSPI_MasterTransferPrepareEDMALite` (LPSPI\_Type \*base, lpspi\_master\_edma\_handle\_t \*handle, uint32\_t configFlags)  
*LPSPI master config transfer parameter while using eDMA.*
- status\_t `LPSPI_MasterTransferEDMALite` (LPSPI\_Type \*base, lpspi\_master\_edma\_handle\_t \*handle, `lpspi_transfer_t` \*transfer)  
*LPSPI master transfer data using eDMA without configs.*
- void `LPSPI_MasterTransferAbortEDMA` (LPSPI\_Type \*base, lpspi\_master\_edma\_handle\_t \*handle)  
*LPSPI master aborts a transfer which is using eDMA.*
- status\_t `LPSPI_MasterTransferGetCountEDMA` (LPSPI\_Type \*base, lpspi\_master\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets the master eDMA transfer remaining bytes.*
- void `LPSPI_SlaveTransferCreateHandleEDMA` (LPSPI\_Type \*base, lpspi\_slave\_edma\_handle\_t \*handle, `lpspi_slave_edma_transfer_callback_t` callback, void \*userData, `edma_handle_t` \*edmaRxRegToRxDataHandle, `edma_handle_t` \*edmaTxDataToTxRegHandle)  
*Initializes the LPSPI slave eDMA handle.*

- `status_t LPSPI_SlaveTransferEDMA (LPSPI_Type *base, lpspi_slave_edma_handle_t *handle, lpspi_transfer_t *transfer)`  
*LPSPI slave transfers data using eDMA.*
- `void LPSPI_SlaveTransferAbortEDMA (LPSPI_Type *base, lpspi_slave_edma_handle_t *handle)`  
*LPSPI slave aborts a transfer which is using eDMA.*
- `status_t LPSPI_SlaveTransferGetCountEDMA (LPSPI_Type *base, lpspi_slave_edma_handle_t *handle, size_t *count)`  
*Gets the slave eDMA transfer remaining bytes.*

## Driver version

- `#define FSL_LPSPI_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 4, 0))`  
*LPSPI EDMA driver version.*

### 31.3.2 Data Structure Documentation

#### 31.3.2.1 struct \_lpspi\_master\_edma\_handle

Forward declaration of the `_lpspi_master_edma_handle` typedefs.

#### Data Fields

- `volatile bool isPcsContinuous`  
*Is PCS continuous in transfer.*
- `volatile bool isByteSwap`  
*A flag that whether should byte swap.*
- `volatile uint8_t fifoSize`  
*FIFO dataSize.*
- `volatile uint8_t rxWatermark`  
*Rx watermark.*
- `volatile uint8_t bytesEachWrite`  
*Bytes for each write TDR.*
- `volatile uint8_t bytesEachRead`  
*Bytes for each read RDR.*
- `volatile uint8_t bytesLastRead`  
*Bytes for last read RDR.*
- `volatile bool isThereExtraRxBytes`  
*Is there extra RX byte.*
- `uint8_t *volatile txData`  
*Send buffer.*
- `uint8_t *volatile rxData`  
*Receive buffer.*
- `volatile size_t txRemainingByteCount`  
*Number of bytes remaining to send.*
- `volatile size_t rxRemainingByteCount`  
*Number of bytes remaining to receive.*
- `volatile uint32_t writeRegRemainingTimes`

- volatile uint32\_t **readRegRemainingTimes**  
*Write TDR register remaining times.*
- uint32\_t **totalByteCount**  
*Read RDR register remaining times.*
- uint32\_t **txBuffIfNull**  
*Number of transfer bytes.*
- uint32\_t **txBuffIfNull**  
*Used if there is not txData for DMA purpose.*
- uint32\_t **rxBuffIfNull**  
*Used if there is not rxData for DMA purpose.*
- uint32\_t **transmitCommand**  
*Used to write TCR for DMA purpose.*
- volatile uint8\_t **state**  
*LPSPI transfer state , \_lpspi\_transfer\_state.*
- uint8\_t **nbytes**  
*eDMA minor byte transfer count initially configured.*
- **lpspi\_master\_edma\_transfer\_callback\_t callback**  
*Completion callback.*
- void \* **userData**  
*Callback user data.*
- **edma\_handle\_t \* edmaRxRegToRxDataHandle**  
*edma\_handle\_t handle point used for RxReg to RxData buff*
- **edma\_handle\_t \* edmaTxDataToTxRegHandle**  
*edma\_handle\_t handle point used for TxData to TxReg buff*
- **edma\_tcd\_t lpspiSoftwareTCD [3]**  
*SoftwareTCD, internal used.*

## Field Documentation

- (1) volatile bool `lpspi_master_edma_handle_t::isPcsContinuous`
- (2) volatile bool `lpspi_master_edma_handle_t::isByteSwap`
- (3) volatile uint8\_t `lpspi_master_edma_handle_t::fifoSize`
- (4) volatile uint8\_t `lpspi_master_edma_handle_t::rxWatermark`
- (5) volatile uint8\_t `lpspi_master_edma_handle_t::bytesEachWrite`
- (6) volatile uint8\_t `lpspi_master_edma_handle_t::bytesEachRead`
- (7) volatile uint8\_t `lpspi_master_edma_handle_t::bytesLastRead`
- (8) volatile bool `lpspi_master_edma_handle_t::isThereExtraRxBytes`
- (9) uint8\_t\* volatile `lpspi_master_edma_handle_t::txData`
- (10) uint8\_t\* volatile `lpspi_master_edma_handle_t::rxData`
- (11) volatile size\_t `lpspi_master_edma_handle_t::txRemainingByteCount`
- (12) volatile size\_t `lpspi_master_edma_handle_t::rxRemainingByteCount`
- (13) volatile uint32\_t `lpspi_master_edma_handle_t::writeRegRemainingTimes`
- (14) volatile uint32\_t `lpspi_master_edma_handle_t::readRegRemainingTimes`
- (15) uint32\_t `lpspi_master_edma_handle_t::txBuffIfNull`
- (16) uint32\_t `lpspi_master_edma_handle_t::rxBuffIfNull`
- (17) uint32\_t `lpspi_master_edma_handle_t::transmitCommand`
- (18) volatile uint8\_t `lpspi_master_edma_handle_t::state`
- (19) uint8\_t `lpspi_master_edma_handle_t::nbytes`
- (20) `lpspi_master_edma_transfer_callback_t lpspi_master_edma_handle_t::callback`
- (21) void\* `lpspi_master_edma_handle_t::userData`

### 31.3.2.2 struct \_lpspi\_slave\_edma\_handle

Forward declaration of the `_lpspi_slave_edma_handle` typedefs.

## Data Fields

- volatile bool **isByteSwap**  
*A flag that whether should byte swap.*
- volatile uint8\_t **fifoSize**  
*FIFO dataSize.*
- volatile uint8\_t **rxWatermark**  
*Rx watermark.*
- volatile uint8\_t **bytesEachWrite**  
*Bytes for each write TDR.*
- volatile uint8\_t **bytesEachRead**  
*Bytes for each read RDR.*
- volatile uint8\_t **bytesLastRead**  
*Bytes for last read RDR.*
- volatile bool **isThereExtraRxBytes**  
*Is there extra RX byte.*
- uint8\_t **nbytes**  
*eDMA minor byte transfer count initially configured.*
- uint8\_t \*volatile **txData**  
*Send buffer.*
- uint8\_t \*volatile **rxData**  
*Receive buffer.*
- volatile size\_t **txRemainingByteCount**  
*Number of bytes remaining to send.*
- volatile size\_t **rxRemainingByteCount**  
*Number of bytes remaining to receive.*
- volatile uint32\_t **writeRegRemainingTimes**  
*Write TDR register remaining times.*
- volatile uint32\_t **readRegRemainingTimes**  
*Read RDR register remaining times.*
- uint32\_t **totalByteCount**  
*Number of transfer bytes.*
- uint32\_t **txBuffIfNull**  
*Used if there is not txData for DMA purpose.*
- uint32\_t **rxBuffIfNull**  
*Used if there is not rxData for DMA purpose.*
- volatile uint8\_t **state**  
*LPSPI transfer state.*
- uint32\_t **errorCount**  
*Error count for slave transfer.*
- **lpspi\_slave\_edma\_transfer\_callback\_t callback**  
*Completion callback.*
- void \* **userData**  
*Callback user data.*
- edma\_handle\_t \* **edmaRxRegToRxDataHandle**  
*edma\_handle\_t handle point used for RxReg to RxData buff*
- edma\_handle\_t \* **edmaTxDataToTxRegHandle**  
*edma\_handle\_t handle point used for TxData to TxReg*
- **edma\_tcd\_t lpspiSoftwareTCD [2]**  
*SoftwareTCD, internal used.*



**Field Documentation**

- (1) volatile bool lpspi\_slave\_edma\_handle\_t::isByteSwap
- (2) volatile uint8\_t lpspi\_slave\_edma\_handle\_t::fifoSize
- (3) volatile uint8\_t lpspi\_slave\_edma\_handle\_t::rxWatermark
- (4) volatile uint8\_t lpspi\_slave\_edma\_handle\_t::bytesEachWrite
- (5) volatile uint8\_t lpspi\_slave\_edma\_handle\_t::bytesEachRead
- (6) volatile uint8\_t lpspi\_slave\_edma\_handle\_t::bytesLastRead
- (7) volatile bool lpspi\_slave\_edma\_handle\_t::isThereExtraRxBytes
- (8) uint8\_t lpspi\_slave\_edma\_handle\_t::nbytes
- (9) uint8\_t\* volatile lpspi\_slave\_edma\_handle\_t::txData
- (10) uint8\_t\* volatile lpspi\_slave\_edma\_handle\_t::rxData
- (11) volatile size\_t lpspi\_slave\_edma\_handle\_t::txRemainingByteCount
- (12) volatile size\_t lpspi\_slave\_edma\_handle\_t::rxRemainingByteCount
- (13) volatile uint32\_t lpspi\_slave\_edma\_handle\_t::writeRegRemainingTimes
- (14) volatile uint32\_t lpspi\_slave\_edma\_handle\_t::readRegRemainingTimes
- (15) uint32\_t lpspi\_slave\_edma\_handle\_t::txBuffIfNull
- (16) uint32\_t lpspi\_slave\_edma\_handle\_t::rxBuffIfNull
- (17) volatile uint8\_t lpspi\_slave\_edma\_handle\_t::state
- (18) uint32\_t lpspi\_slave\_edma\_handle\_t::errorCount
- (19) lpspi\_slave\_edma\_transfer\_callback\_t lpspi\_slave\_edma\_handle\_t::callback
- (20) void\* lpspi\_slave\_edma\_handle\_t::userData

**31.3.3 Macro Definition Documentation****31.3.3.1 #define FSL\_LPSPI\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 4, 0))****31.3.4 Typedef Documentation****31.3.4.1 typedef void(\* lpspi\_master\_edma\_transfer\_callback\_t)(LPSPI\_Type \*base,  
lpspi\_master\_edma\_handle\_t \*handle, status\_t status, void \*userData)**

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	Pointer to the handle for the LPSPI master.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

### 31.3.4.2 **typedef void(\* lpspi\_slave\_edma\_transfer\_callback\_t)(LPSPI\_Type \*base, lpspi\_slave\_edma\_handle\_t \*handle, status\_t status, void \*userData)**

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	Pointer to the handle for the LPSPI slave.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

## 31.3.5 Function Documentation

### 31.3.5.1 **void LPSPI\_MasterTransferCreateHandleEDMA ( LPSPI\_Type \* *base*, lpspi\_master\_edma\_handle\_t \* *handle*, lpspi\_master\_edma\_transfer\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *edmaRxRegToRxDataHandle*, edma\_handle\_t \* *edmaTxDataToTxRegHandle* )**

This function initializes the LPSPI eDMA handle which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Note that the LPSPI eDMA has a separated (Rx and Tx as two sources) or shared (Rx and Tx are the same source) DMA request source. (1) For a separated DMA request source, enable and set the Rx DMAMUX source for edmaRxRegToRxDataHandle and Tx DMAMUX source for edmaTxDataToTxRegHandle. (2) For a shared DMA request source, enable and set the Rx/Tx DMAMUX source for edmaRxRegToRxDataHandle.

Parameters

<i>base</i>	LPSPI peripheral base address.
-------------	--------------------------------

<i>handle</i>	LPSPI handle pointer to <code>lpspi_master_edma_handle_t</code> .
<i>callback</i>	LPSPI callback.
<i>userData</i>	callback function parameter.
<i>edmaRxRegTo-RxDataHandle</i>	edmaRxRegToRxDataHandle pointer to <code>edma_handle_t</code> .
<i>edmaTxData-ToTxReg-Handle</i>	edmaTxDataToTxRegHandle pointer to <code>edma_handle_t</code> .

### 31.3.5.2 status\_t LPSPI\_MasterTransferEDMA ( `LPSPI_Type * base,` `lpspi_master_edma_handle_t * handle, lpspi_transfer_t * transfer` )

This function transfers data using eDMA. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be an integer multiple of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not an integer multiple of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <code>lpspi_master_edma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	pointer to <code>lpspi_transfer_t</code> structure.

Returns

status of `status_t`.

### 31.3.5.3 status\_t LPSPI\_MasterTransferPrepareEDMALite ( `LPSPI_Type * base,` `lpspi_master_edma_handle_t * handle, uint32_t configFlags` )

This function is preparing to transfer data using eDMA, work with `LPSPI_MasterTransferEDMALite`.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <code>lpspi_master_edma_handle_t</code> structure which stores the transfer state.
<i>configFlags</i>	transfer configuration flags. <code>_lpspi_transfer_config_flag_for_master</code> .

Returns

Indicates whether LPSPI master transfer was successful or not.

Return values

<i>kStatus_Success</i>	Execution successfully.
<i>kStatus_LPSPI_Busy</i>	The LPSPI device is busy.

### 31.3.5.4 `status_t LPSPI_MasterTransferEDMALite ( LPSPI_Type * base, lpspi_master_edma_handle_t * handle, lpspi_transfer_t * transfer )`

This function transfers data using eDMA. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note: This API is only for transfer through DMA without configuration. Before calling this API, you must call `LPSPI_MasterTransferPrepareEDMALite` to configure it once. The transfer data size should be an integer multiple of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not an integer multiple of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <code>lpspi_master_edma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	pointer to <code>lpspi_transfer_t</code> structure, config field is not used.

Returns

Indicates whether LPSPI master transfer was successful or not.

Return values

<i>kStatus_Success</i>	Execution successfully.
<i>kStatus_LPSPI_Busy</i>	The LPSPI device is busy.
<i>kStatus_InvalidArgument</i>	The transfer structure is invalid.

### 31.3.5.5 void LPSPI\_MasterTransferAbortEDMA ( **LPSPI\_Type** \* *base*, **lpspi\_master\_edma\_handle\_t** \* *handle* )

This function aborts a transfer which is using eDMA.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <b>lpspi_master_edma_handle_t</b> structure which stores the transfer state.

### 31.3.5.6 status\_t LPSPI\_MasterTransferGetCountEDMA ( **LPSPI\_Type** \* *base*, **lpspi\_master\_edma\_handle\_t** \* *handle*, **size\_t** \* *count* )

This function gets the master eDMA transfer remaining bytes.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <b>lpspi_master_edma_handle_t</b> structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the EDMA transaction.

Returns

status of **status\_t**.

### 31.3.5.7 void LPSPI\_SlaveTransferCreateHandleEDMA ( **LPSPI\_Type** \* *base*, **lpspi\_slave\_edma\_handle\_t** \* *handle*, **lpspi\_slave\_edma\_transfer\_callback\_t** *callback*, **void** \* *userData*, **edma\_handle\_t** \* *edmaRxRegToRxDataHandle*, **edma\_handle\_t** \* *edmaTxDataToTxRegHandle* )

This function initializes the LPSPI eDMA handle which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Note that LPSPI eDMA has a separated (Rx and Tx as two sources) or shared (Rx and Tx as the same source) DMA request source.

(1) For a separated DMA request source, enable and set the Rx DMAMUX source for edmaRxRegToRxDataHandle and Tx DMAMUX source for edmaTxDataToTxRegHandle. (2) For a shared DMA request source, enable and set the Rx/Rx DMAMUX source for edmaRxRegToRxDataHandle .

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	LPSPI handle pointer to <code>lpspi_slave_edma_handle_t</code> .
<i>callback</i>	LPSPI callback.
<i>userData</i>	callback function parameter.
<i>edmaRxRegTo-RxDataHandle</i>	edmaRxRegToRxDataHandle pointer to <code>edma_handle_t</code> .
<i>edmaTxData-ToTxReg-Handle</i>	edmaTxDataToTxRegHandle pointer to <code>edma_handle_t</code> .

### 31.3.5.8 `status_t LPSPI_SlaveTransferEDMA ( LPSPI_Type * base, lpspi_slave_edma_handle_t * handle, lpspi_transfer_t * transfer )`

This function transfers data using eDMA. This is a non-blocking function, which return right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be an integer multiple of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not an integer multiple of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <code>lpspi_slave_edma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	pointer to <code>lpspi_transfer_t</code> structure.

Returns

status of `status_t`.

### 31.3.5.9 `void LPSPI_SlaveTransferAbortEDMA ( LPSPI_Type * base, lpspi_slave_edma_handle_t * handle )`

This function aborts a transfer which is using eDMA.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to lpspi_slave_edma_handle_t structure which stores the transfer state.

### 31.3.5.10 status\_t LPSPI\_SlaveTransferGetCountEDMA ( **LPSPI\_Type** \* *base*, **lpspi\_slave\_edma\_handle\_t** \* *handle*, **size\_t** \* *count* )

This function gets the slave eDMA transfer remaining bytes.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to lpspi_slave_edma_handle_t structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the eDMA transaction.

Returns

status of status\_t.

## 31.4 LPSPI FreeRTOS Driver

### 31.4.1 Overview

#### Driver version

- #define `FSL_LPSPI_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))`  
*LPSPI FreeRTOS driver version 2.3.1.*

#### LPSPI RTOS Operation

- `status_t LPSPI_RTOS_Init (lpspi_rtos_handle_t *handle, LPSPI_Type *base, const lpspi_master_config_t *masterConfig, uint32_t srcClock_Hz)`  
*Initializes LPSPI.*
- `status_t LPSPI_RTOS_Deinit (lpspi_rtos_handle_t *handle)`  
*Deinitializes the LPSPI.*
- `status_t LPSPI_RTOS_Transfer (lpspi_rtos_handle_t *handle, lpspi_transfer_t *transfer)`  
*Performs SPI transfer.*

### 31.4.2 Macro Definition Documentation

#### 31.4.2.1 #define FSL\_LPSPI\_FREERTOS\_DRIVER\_VERSION (MAKE\_VERSION(2, 3, 1))

### 31.4.3 Function Documentation

#### 31.4.3.1 `status_t LPSPI_RTOS_Init ( lpspi_rtos_handle_t * handle, LPSPI_Type * base, const lpspi_master_config_t * masterConfig, uint32_t srcClock_Hz )`

This function initializes the LPSPI module and related RTOS context.

Parameters

<code>handle</code>	The RTOS LPSPI handle, the pointer to an allocated space for RTOS context.
<code>base</code>	The pointer base address of the LPSPI instance to initialize.
<code>masterConfig</code>	Configuration structure to set-up LPSPI in master mode.
<code>srcClock_Hz</code>	Frequency of input clock of the LPSPI module.

Returns

status of the operation.

### 31.4.3.2 status\_t LPSPI\_RTOS\_Deinit ( *Ipspi\_rtos\_handle\_t \* handle* )

This function deinitializes the LPSPI module and related RTOS context.

Parameters

<i>handle</i>	The RTOS LPSPI handle.
---------------	------------------------

### 31.4.3.3 status\_t LPSPI\_RTOS\_Transfer ( *lpspi\_rtos\_handle\_t* \* *handle*, *lpspi\_transfer\_t* \* *transfer* )

This function performs an SPI transfer according to data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS LPSPI handle.
<i>transfer</i>	Structure specifying the transfer parameters.

Returns

status of the operation.

## 31.5 LPSPI CMSIS Driver

This section describes the programming interface of the LPSPI Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.-keil.com/pack/doc/cmsis/Driver/html/index.html>.

### 31.5.1 Function groups

#### 31.5.1.1 LPSPI CMSIS GetVersion Operation

This function group will return the DSPI CMSIS Driver version to user.

#### 31.5.1.2 LPSPI CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

#### 31.5.1.3 LPSPI CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialized the instance in master mode or slave mode. And this API must be called before you configure an instance or after you Deinit an instance. The right steps to start an instance is that you must initialize the instance which been selected firstly, then you can power on the instance. After these all have been done, you can configure the instance by using control operation. If you want to Uninitialize the instance, you must power off the instance first.

#### 31.5.1.4 LPSPI Transfer Operation

This function group controls the transfer, master send/receive data, and slave send/receive data.

#### 31.5.1.5 LPSPI Status Operation

This function group gets the LPSPI transfer status.

#### 31.5.1.6 LPSPI CMSIS Control Operation

This function can select instance as master mode or slave mode, set baudrate for master mode transfer, get current baudrate of master mode transfer, set transfer data bits and set other control command.

## 31.5.2 Typical use case

### 31.5.2.1 Master Operation

```
/* Variables */
uint8_t masterRxData[TRANSFER_SIZE] = {0U};
uint8_t masterTxData[TRANSFER_SIZE] = {0U};

/*DSPI master init*/
Driver_SPI0.Initialize(DSPI_MasterSignalEvent_t);
Driver_SPI0.PowerControl(ARM_POWER_FULL);
Driver_SPI0.Control(ARM_SPI_MODE_MASTER, TRANSFER_BAUDRATE);

/* Start master transfer */
Driver_SPI0.Transfer(masterTxData, masterRxData, TRANSFER_SIZE);

/* Master power off */
Driver_SPI0.PowerControl(ARM_POWER_OFF);

/* Master uninitialize */
Driver_SPI0.Uninitialize();
```

### 31.5.2.2 Slave Operation

```
/* Variables */
uint8_t slaveRxData[TRANSFER_SIZE] = {0U};
uint8_t slaveTxData[TRANSFER_SIZE] = {0U};

/*DSPI slave init*/
Driver_SPI2.Initialize(DSPI_SlaveSignalEvent_t);
Driver_SPI2.PowerControl(ARM_POWER_FULL);
Driver_SPI2.Control(ARM_SPI_MODE_SLAVE, false);

/* Start slave transfer */
Driver_SPI2.Transfer(slaveTxData, slaveRxData, TRANSFER_SIZE);

/* slave power off */
Driver_SPI2.PowerControl(ARM_POWER_OFF);

/* slave uninitialize */
Driver_SPI2.Uninitialize();
```

## Chapter 32

# LPUART: Low Power Universal Asynchronous Receiver-/Transmitter Driver

### 32.1 Overview

#### Modules

- [LPUART CMSIS Driver](#)
- [LPUART Driver](#)
- [LPUART FreeRTOS Driver](#)
- [LPUART eDMA Driver](#)

## 32.2 LPUART Driver

### 32.2.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Low Power UART (LPUART) module of MCUXpresso SDK devices.

### 32.2.2 Typical use case

#### 32.2.2.1 LPUART Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/lpuart

## Data Structures

- struct [lpuart\\_config\\_t](#)  
*LPUART configuration structure. [More...](#)*
- struct [lpuart\\_transfer\\_t](#)  
*LPUART transfer structure. [More...](#)*
- struct [lpuart\\_handle\\_t](#)  
*LPUART handle structure. [More...](#)*

## Macros

- #define [UART\\_RETRY\\_TIMES](#) 0U /\* Defining to zero means to keep waiting for the flag until it is assert/deassert. \*/  
*Retry times for waiting flag.*

## Typedefs

- typedef void(\* [lpuart\\_transfer\\_callback\\_t](#))(LPUART\_Type \*base, lpuart\_handle\_t \*handle, [status\\_t](#) status, void \*userData)  
*LPUART transfer callback function.*

## Enumerations

- enum {
   
kStatus\_LPUART\_TxBusy = MAKE\_STATUS(kStatusGroup\_LPUART, 0),
   
kStatus\_LPUART\_RxBusy = MAKE\_STATUS(kStatusGroup\_LPUART, 1),
   
kStatus\_LPUART\_TxIdle = MAKE\_STATUS(kStatusGroup\_LPUART, 2),
   
kStatus\_LPUART\_RxIdle = MAKE\_STATUS(kStatusGroup\_LPUART, 3),
   
kStatus\_LPUART\_TxWatermarkTooLarge = MAKE\_STATUS(kStatusGroup\_LPUART, 4),
   
kStatus\_LPUART\_RxWatermarkTooLarge = MAKE\_STATUS(kStatusGroup\_LPUART, 5),
   
kStatus\_LPUART\_FlagCannotClearManually = MAKE\_STATUS(kStatusGroup\_LPUART, 6),
   
kStatus\_LPUART\_Error = MAKE\_STATUS(kStatusGroup\_LPUART, 7),
   
kStatus\_LPUART\_RxRingBufferOverrun,
   
kStatus\_LPUART\_RxHardwareOverrun = MAKE\_STATUS(kStatusGroup\_LPUART, 9),
   
kStatus\_LPUART\_NoiseError = MAKE\_STATUS(kStatusGroup\_LPUART, 10),
   
kStatus\_LPUART\_FramingError = MAKE\_STATUS(kStatusGroup\_LPUART, 11),
   
kStatus\_LPUART\_ParityError = MAKE\_STATUS(kStatusGroup\_LPUART, 12),
   
kStatus\_LPUART\_BaudrateNotSupport,
   
kStatus\_LPUART\_IdleLineDetected = MAKE\_STATUS(kStatusGroup\_LPUART, 14),
   
kStatus\_LPUART\_Timeout = MAKE\_STATUS(kStatusGroup\_LPUART, 15) }

*Error codes for the LPUART driver.*

- enum `lpuart_parity_mode_t` {
   
kLPUART\_ParityDisabled = 0x0U,
   
kLPUART\_ParityEven = 0x2U,
   
kLPUART\_ParityOdd = 0x3U }
- LPUART parity mode.*
- enum `lpuart_data_bits_t` {
   
kLPUART\_EightDataBits = 0x0U,
   
kLPUART\_SevenDataBits = 0x1U }
- LPUART data bits count.*
- enum `lpuart_stop_bit_count_t` {
   
kLPUART\_OneStopBit = 0U,
   
kLPUART\_TwoStopBit = 1U }
- LPUART stop bit count.*
- enum `lpuart_transmit_cts_source_t` {
   
kLPUART\_CtsSourcePin = 0U,
   
kLPUART\_CtsSourceMatchResult = 1U }
- LPUART transmit CTS source.*
- enum `lpuart_transmit_cts_config_t` {
   
kLPUART\_CtsSampleAtStart = 0U,
   
kLPUART\_CtsSampleAtIdle = 1U }
- LPUART transmit CTS configure.*
- enum `lpuart_idle_type_select_t` {
   
kLPUART\_IdleTypeStartBit = 0U,
   
kLPUART\_IdleTypeStopBit = 1U }
- LPUART idle flag type defines when the receiver starts counting.*
- enum `lpuart_idle_config_t` {

```
kLPUART_IdleCharacter1 = 0U,
kLPUART_IdleCharacter2 = 1U,
kLPUART_IdleCharacter4 = 2U,
kLPUART_IdleCharacter8 = 3U,
kLPUART_IdleCharacter16 = 4U,
kLPUART_IdleCharacter32 = 5U,
kLPUART_IdleCharacter64 = 6U,
kLPUART_IdleCharacter128 = 7U }
```

*LPUART idle detected configuration.*

- enum \_lpuart\_interrupt\_enable {

```
kLPUART_LinBreakInterruptEnable = (LPUART_BAUD_LBKDIIE_MASK >> 8U),
kLPUART_RxActiveEdgeInterruptEnable = (LPUART_BAUD_RXEDGIE_MASK >> 8U),
kLPUART_TxDataRegEmptyInterruptEnable = (LPUART_CTRL_TIE_MASK),
kLPUART_TransmissionCompleteInterruptEnable = (LPUART_CTRL_TCIE_MASK),
kLPUART_RxDataRegFullInterruptEnable = (LPUART_CTRL_RIE_MASK),
kLPUART_IdleLineInterruptEnable = (LPUART_CTRL_ILIE_MASK),
kLPUART_RxOverrunInterruptEnable = (LPUART_CTRL_ORIE_MASK),
kLPUART_NoiseErrorInterruptEnable = (LPUART_CTRL_NEIE_MASK),
kLPUART_FramingErrorInterruptEnable = (LPUART_CTRL_FEIE_MASK),
kLPUART_ParityErrorInterruptEnable = (LPUART_CTRL_PEIE_MASK),
kLPUART_Match1InterruptEnable = (LPUART_CTRL_MA1IE_MASK),
kLPUART_Match2InterruptEnable = (LPUART_CTRL_MA2IE_MASK),
kLPUART_TxFifoOverflowInterruptEnable = (LPUART_FIFO_TXOFE_MASK),
kLPUART_RxFifoUnderflowInterruptEnable = (LPUART_FIFO_RXUFE_MASK) }
```

*LPUART interrupt configuration structure, default settings all disabled.*

- enum \_lpuart\_flags {

```
kLPUART_TxDataRegEmptyFlag,
kLPUART_TransmissionCompleteFlag,
kLPUART_RxDataRegFullFlag = (LPUART_STAT_RDRF_MASK),
kLPUART_IdleLineFlag = (LPUART_STAT_IDLE_MASK),
kLPUART_RxOverrunFlag = (LPUART_STAT_OR_MASK),
kLPUART_NoiseErrorFlag = (LPUART_STAT_NF_MASK),
kLPUART_FramingErrorFlag,
kLPUART_ParityErrorFlag = (LPUART_STAT_PF_MASK),
kLPUART_LinBreakFlag = (LPUART_STAT_LBKDIF_MASK),
kLPUART_RxActiveEdgeFlag = (LPUART_STAT_RXEDGIF_MASK),
kLPUART_RxActiveFlag,
kLPUART_DataMatch1Flag,
kLPUART_DataMatch2Flag,
kLPUART_TxFifoEmptyFlag,
kLPUART_RxFifoEmptyFlag,
kLPUART_TxFifoOverflowFlag,
kLPUART_RxFifoUnderflowFlag }
```

*LPUART status flags.*

## Driver version

- #define **FSL\_LPUART\_DRIVER\_VERSION** (MAKE\_VERSION(2, 7, 3))  
*LPUART driver version.*

## Software Reset

- static void **LPUART\_SoftwareReset** (LPUART\_Type \*base)  
*Resets the LPUART using software.*

## Initialization and deinitialization

- **status\_t LPUART\_Init** (LPUART\_Type \*base, const **lpuart\_config\_t** \*config, uint32\_t srcClock\_Hz)  
*Initializes an LPUART instance with the user configuration structure and the peripheral clock.*
- void **LPUART\_Deinit** (LPUART\_Type \*base)  
*Deinitializes a LPUART instance.*
- void **LPUART\_GetDefaultConfig** (**lpuart\_config\_t** \*config)  
*Gets the default configuration structure.*

## Module configuration

- **status\_t LPUART\_SetBaudRate** (LPUART\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Sets the LPUART instance baudrate.*
- void **LPUART\_Enable9bitMode** (LPUART\_Type \*base, bool enable)  
*Enable 9-bit data mode for LPUART.*
- static void **LPUART\_SetMatchAddress** (LPUART\_Type \*base, uint16\_t address1, uint16\_t address2)  
*Set the LPUART address.*
- static void **LPUART\_EnableMatchAddress** (LPUART\_Type \*base, bool match1, bool match2)  
*Enable the LPUART match address feature.*
- static void **LPUART\_SetRxFifoWatermark** (LPUART\_Type \*base, uint8\_t water)  
*Sets the rx FIFO watermark.*
- static void **LPUART\_SetTxFifoWatermark** (LPUART\_Type \*base, uint8\_t water)  
*Sets the tx FIFO watermark.*

## Status

- uint32\_t **LPUART\_GetStatusFlags** (LPUART\_Type \*base)  
*Gets LPUART status flags.*
- **status\_t LPUART\_ClearStatusFlags** (LPUART\_Type \*base, uint32\_t mask)  
*Clears status flags with a provided mask.*

## Interrupts

- void [LPUART\\_EnableInterrupts](#) (LPUART\_Type \*base, uint32\_t mask)  
*Enables LPUART interrupts according to a provided mask.*
- void [LPUART\\_DisableInterrupts](#) (LPUART\_Type \*base, uint32\_t mask)  
*Disables LPUART interrupts according to a provided mask.*
- uint32\_t [LPUART\\_GetEnabledInterrupts](#) (LPUART\_Type \*base)  
*Gets enabled LPUART interrupts.*

## DMA Configuration

- static uintptr\_t [LPUART\\_GetDataRegisterAddress](#) (LPUART\_Type \*base)  
*Gets the LPUART data register address.*
- static void [LPUART\\_EnableTxDMA](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART transmitter DMA request.*
- static void [LPUART\\_EnableRxDMA](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART receiver DMA.*

## Bus Operations

- uint32\_t [LPUARTGetInstance](#) (LPUART\_Type \*base)  
*Get the LPUART instance from peripheral base address.*
- static void [LPUART\\_EnableTx](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART transmitter.*
- static void [LPUART\\_EnableRx](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART receiver.*
- static void [LPUART\\_WriteByte](#) (LPUART\_Type \*base, uint8\_t data)  
*Writes to the transmitter register.*
- static uint8\_t [LPUART\\_ReadByte](#) (LPUART\_Type \*base)  
*Reads the receiver register.*
- static uint8\_t [LPUART\\_GetRxFifoCount](#) (LPUART\_Type \*base)  
*Gets the rx FIFO data count.*
- static uint8\_t [LPUART\\_GetTxFifoCount](#) (LPUART\_Type \*base)  
*Gets the tx FIFO data count.*
- void [LPUART\\_SendAddress](#) (LPUART\_Type \*base, uint8\_t address)  
*Transmit an address frame in 9-bit data mode.*
- status\_t [LPUART\\_WriteBlocking](#) (LPUART\_Type \*base, const uint8\_t \*data, size\_t length)  
*Writes to the transmitter register using a blocking method.*
- status\_t [LPUART\\_ReadBlocking](#) (LPUART\_Type \*base, uint8\_t \*data, size\_t length)  
*Reads the receiver data register using a blocking method.*

## Transactional

- void [LPUART\\_TransferCreateHandle](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, [lpuart\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the LPUART handle.*

- `status_t LPUART_TransferSendNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer)`

*Transmits a buffer of data using the interrupt method.*
- `void LPUART_TransferStartRingBuffer (LPUART_Type *base, lpuart_handle_t *handle, uint8_t *ringBuffer, size_t ringBufferSize)`

*Sets up the RX ring buffer.*
- `void LPUART_TransferStopRingBuffer (LPUART_Type *base, lpuart_handle_t *handle)`

*Aborts the background transfer and uninstalls the ring buffer.*
- `size_t LPUART_TransferGetRxRingBufferLength (LPUART_Type *base, lpuart_handle_t *handle)`

*Get the length of received data in RX ring buffer.*
- `void LPUART_TransferAbortSend (LPUART_Type *base, lpuart_handle_t *handle)`

*Aborts the interrupt-driven data transmit.*
- `status_t LPUART_TransferGetSendCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)`

*Gets the number of bytes that have been sent out to bus.*
- `status_t LPUART_TransferReceiveNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer, size_t *receivedBytes)`

*Receives a buffer of data using the interrupt method.*
- `void LPUART_TransferAbortReceive (LPUART_Type *base, lpuart_handle_t *handle)`

*Aborts the interrupt-driven data receiving.*
- `status_t LPUART_TransferGetReceiveCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)`

*Gets the number of bytes that have been received.*
- `void LPUART_TransferHandleIRQ (LPUART_Type *base, void *irqHandle)`

*LPUART IRQ handle function.*
- `void LPUART_TransferHandleErrorIRQ (LPUART_Type *base, void *irqHandle)`

*LPUART Error IRQ handle function.*

### 32.2.3 Data Structure Documentation

#### 32.2.3.1 struct lpuart\_config\_t

##### Data Fields

- `uint32_t baudRate_Bps`

*LPUART baud rate.*
- `lpuart_parity_mode_t parityMode`

*Parity mode, disabled (default), even, odd.*
- `lpuart_data_bits_t dataBitsCount`

*Data bits count, eight (default), seven.*
- `bool isMsb`

*Data bits order, LSB (default), MSB.*
- `lpuart_stop_bit_count_t stopBitCount`

*Number of stop bits, 1 stop bit (default) or 2 stop bits.*
- `uint8_t txFifoWatermark`

*TX FIFO watermark.*
- `uint8_t rxFifoWatermark`

- `bool enableRxRTS`  
*RX RTS enable.*
- `bool enableTxCTS`  
*TX CTS enable.*
- `lpuart_transmit_cts_source_t txCtsSource`  
*TX CTS source.*
- `lpuart_transmit_cts_config_t txCtsConfig`  
*TX CTS configure.*
- `lpuart_idle_type_select_t rxIdleType`  
*RX IDLE type.*
- `lpuart_idle_config_t rxIdleConfig`  
*RX IDLE configuration.*
- `bool enableTx`  
*Enable TX.*
- `bool enableRx`  
*Enable RX.*

## Field Documentation

(1) `lpuart_idle_type_select_t lpuart_config_t::rxIdleType`

(2) `lpuart_idle_config_t lpuart_config_t::rxIdleConfig`

### 32.2.3.2 struct lpuart\_transfer\_t

#### Data Fields

- `size_t dataSize`  
*The byte count to be transfer.*
- `uint8_t * data`  
*The buffer of data to be transfer.*
- `uint8_t * rxData`  
*The buffer to receive data.*
- `const uint8_t * txData`  
*The buffer of data to be sent.*

## Field Documentation

- (1) `uint8_t* lpuart_transfer_t::data`
- (2) `uint8_t* lpuart_transfer_t::rxData`
- (3) `const uint8_t* lpuart_transfer_t::txData`
- (4) `size_t lpuart_transfer_t::dataSize`

### 32.2.3.3 struct \_lpuart\_handle

#### Data Fields

- `const uint8_t *volatile txData`  
*Address of remaining data to send.*
- `volatile size_t txDataSize`  
*Size of the remaining data to send.*
- `size_t txDataSizeAll`  
*Size of the data to send out.*
- `uint8_t *volatile rxData`  
*Address of remaining data to receive.*
- `volatile size_t rxDataSize`  
*Size of the remaining data to receive.*
- `size_t rxDataSizeAll`  
*Size of the data to receive.*
- `uint8_t * rxRingBuffer`  
*Start address of the receiver ring buffer.*
- `size_t rxRingBufferSize`  
*Size of the ring buffer.*
- `volatile uint16_t rxRingBufferHead`  
*Index for the driver to store received data into ring buffer.*
- `volatile uint16_t rxRingBufferTail`  
*Index for the user to get data from the ring buffer.*
- `lpuart_transfer_callback_t callback`  
*Callback function.*
- `void * userData`  
*LPUART callback function parameter.*
- `volatile uint8_t txState`  
*TX transfer state.*
- `volatile uint8_t rxState`  
*RX transfer state.*
- `bool isSevenDataBits`  
*Seven data bits flag.*



## Field Documentation

- (1) const uint8\_t\* volatile lpuart\_handle\_t::txData
- (2) volatile size\_t lpuart\_handle\_t::txDataSize
- (3) size\_t lpuart\_handle\_t::txDataSizeAll
- (4) uint8\_t\* volatile lpuart\_handle\_t::rxData
- (5) volatile size\_t lpuart\_handle\_t::rxDataSize
- (6) size\_t lpuart\_handle\_t::rxDataSizeAll
- (7) uint8\_t\* lpuart\_handle\_t::rxRingBuffer
- (8) size\_t lpuart\_handle\_t::rxRingBufferSize
- (9) volatile uint16\_t lpuart\_handle\_t::rxRingBufferHead
- (10) volatile uint16\_t lpuart\_handle\_t::rxRingBufferTail
- (11) lpuart\_transfer\_callback\_t lpuart\_handle\_t::callback
- (12) void\* lpuart\_handle\_t::userData
- (13) volatile uint8\_t lpuart\_handle\_t::txState
- (14) volatile uint8\_t lpuart\_handle\_t::rxState
- (15) bool lpuart\_handle\_t::isSevenDataBits

### 32.2.4 Macro Definition Documentation

32.2.4.1 #define FSL\_LPUART\_DRIVER\_VERSION (MAKE\_VERSION(2, 7, 3))

32.2.4.2 #define UART\_RETRY\_TIMES 0U /\* Defining to zero means to keep waiting for the flag until it is assert/deassert. \*/

### 32.2.5 Typedef Documentation

32.2.5.1 typedef void(\* lpuart\_transfer\_callback\_t)(LPUART\_Type \*base, lpuart\_handle\_t \*handle, status\_t status, void \*userData)

### 32.2.6 Enumeration Type Documentation

#### 32.2.6.1 anonymous enum

Enumerator

*kStatus\_LPUART\_RxBusy* RX busy.  
*kStatus\_LPUART\_TxIdle* LPUART transmitter is idle.  
*kStatus\_LPUART\_RxIdle* LPUART receiver is idle.  
*kStatus\_LPUART\_TxWatermarkTooLarge* TX FIFO watermark too large.  
*kStatus\_LPUART\_RxWatermarkTooLarge* RX FIFO watermark too large.  
*kStatus\_LPUART\_FlagCannotClearManually* Some flag can't manually clear.  
*kStatus\_LPUART\_Error* Error happens on LPUART.  
*kStatus\_LPUART\_RxRingBufferOverrun* LPUART RX software ring buffer overrun.  
*kStatus\_LPUART\_RxHardwareOverrun* LPUART RX receiver overrun.  
*kStatus\_LPUART\_NoiseError* LPUART noise error.  
*kStatus\_LPUART\_FramingError* LPUART framing error.  
*kStatus\_LPUART\_ParityError* LPUART parity error.  
*kStatus\_LPUART\_BaudrateNotSupport* Baudrate is not support in current clock source.  
*kStatus\_LPUART\_IdleLineDetected* IDLE flag.  
*kStatus\_LPUART\_Timeout* LPUART times out.

### 32.2.6.2 enum lpuart\_parity\_mode\_t

Enumerator

*kLPUART\_ParityDisabled* Parity disabled.  
*kLPUART\_ParityEven* Parity enabled, type even, bit setting: PE|PT = 10.  
*kLPUART\_ParityOdd* Parity enabled, type odd, bit setting: PE|PT = 11.

### 32.2.6.3 enum lpuart\_data\_bits\_t

Enumerator

*kLPUART\_EightDataBits* Eight data bit.  
*kLPUART\_SevenDataBits* Seven data bit.

### 32.2.6.4 enum lpuart\_stop\_bit\_count\_t

Enumerator

*kLPUART\_OneStopBit* One stop bit.  
*kLPUART\_TwoStopBit* Two stop bits.

### 32.2.6.5 enum lpuart\_transmit\_cts\_source\_t

Enumerator

*kLPUART\_CtsSourcePin* CTS resource is the LPUART\_CTS pin.

***kLPUART\_CtsSourceMatchResult*** CTS resource is the match result.

### 32.2.6.6 enum lpuart\_transmit\_cts\_config\_t

Enumerator

***kLPUART\_CtsSampleAtStart*** CTS input is sampled at the start of each character.

***kLPUART\_CtsSampleAtIdle*** CTS input is sampled when the transmitter is idle.

### 32.2.6.7 enum lpuart\_idle\_type\_select\_t

Enumerator

***kLPUART\_IdleTypeStartBit*** Start counting after a valid start bit.

***kLPUART\_IdleTypeStopBit*** Start counting after a stop bit.

### 32.2.6.8 enum lpuart\_idle\_config\_t

This structure defines the number of idle characters that must be received before the IDLE flag is set.

Enumerator

***kLPUART\_IdleCharacter1*** the number of idle characters.

***kLPUART\_IdleCharacter2*** the number of idle characters.

***kLPUART\_IdleCharacter4*** the number of idle characters.

***kLPUART\_IdleCharacter8*** the number of idle characters.

***kLPUART\_IdleCharacter16*** the number of idle characters.

***kLPUART\_IdleCharacter32*** the number of idle characters.

***kLPUART\_IdleCharacter64*** the number of idle characters.

***kLPUART\_IdleCharacter128*** the number of idle characters.

### 32.2.6.9 enum \_lpuart\_interrupt\_enable

This structure contains the settings for all LPUART interrupt configurations.

Enumerator

***kLPUART\_LinBreakInterruptEnable*** LIN break detect. bit 7

***kLPUART\_RxActiveEdgeInterruptEnable*** Receive Active Edge. bit 6

***kLPUART\_TxDataRegEmptyInterruptEnable*** Transmit data register empty. bit 23

***kLPUART\_TransmissionCompleteInterruptEnable*** Transmission complete. bit 22

***kLPUART\_RxDataRegFullInterruptEnable*** Receiver data register full. bit 21

*kLPUART\_IdleLineInterruptEnable* Idle line. bit 20  
*kLPUART\_RxOverrunInterruptEnable* Receiver Overrun. bit 27  
*kLPUART\_NoiseErrorInterruptEnable* Noise error flag. bit 26  
*kLPUART\_FramingErrorInterruptEnable* Framing error flag. bit 25  
*kLPUART\_ParityErrorInterruptEnable* Parity error flag. bit 24  
*kLPUART\_Match1InterruptEnable* Parity error flag. bit 15  
*kLPUART\_Match2InterruptEnable* Parity error flag. bit 14  
*kLPUART\_TxFifoOverflowInterruptEnable* Transmit FIFO Overflow. bit 9  
*kLPUART\_RxFifoUnderflowInterruptEnable* Receive FIFO Underflow. bit 8

### 32.2.6.10 enum \_lpuart\_flags

This provides constants for the LPUART status flags for use in the LPUART functions.

Enumerator

*kLPUART\_TxDataRegEmptyFlag* Transmit data register empty flag, sets when transmit buffer is empty. bit 23  
*kLPUART\_TransmissionCompleteFlag* Transmission complete flag, sets when transmission activity complete. bit 22  
*kLPUART\_RxDataRegFullFlag* Receive data register full flag, sets when the receive data buffer is full. bit 21  
*kLPUART\_IdleLineFlag* Idle line detect flag, sets when idle line detected. bit 20  
*kLPUART\_RxOverrunFlag* Receive Overrun, sets when new data is received before data is read from receive register. bit 19  
*kLPUART\_NoiseErrorFlag* Receive takes 3 samples of each received bit. If any of these samples differ, noise flag sets. bit 18  
*kLPUART\_FramingErrorFlag* Frame error flag, sets if logic 0 was detected where stop bit expected. bit 17  
*kLPUART\_ParityErrorFlag* If parity enabled, sets upon parity error detection. bit 16  
*kLPUART\_LinBreakFlag* LIN break detect interrupt flag, sets when LIN break char detected and LIN circuit enabled. bit 31  
*kLPUART\_RxActiveEdgeFlag* Receive pin active edge interrupt flag, sets when active edge detected. bit 30  
*kLPUART\_RxActiveFlag* Receiver Active Flag (RAF), sets at beginning of valid start. bit 24  
*kLPUART\_DataMatch1Flag* The next character to be read from LPUART\_DATA matches MA1. bit 15  
*kLPUART\_DataMatch2Flag* The next character to be read from LPUART\_DATA matches MA2. bit 14  
*kLPUART\_TxFifoEmptyFlag* TXEMPT bit, sets if transmit buffer is empty. bit 7  
*kLPUART\_RxFifoEmptyFlag* RXEMPT bit, sets if receive buffer is empty. bit 6  
*kLPUART\_TxFifoOverflowFlag* TXOF bit, sets if transmit buffer overflow occurred. bit 1  
*kLPUART\_RxFifoUnderflowFlag* RXUF bit, sets if receive buffer underflow occurred. bit 0

### 32.2.7 Function Documentation

#### 32.2.7.1 static void LPUART\_SoftwareReset ( LPUART\_Type \* *base* ) [inline], [static]

This function resets all internal logic and registers except the Global Register. Remains set until cleared by software.

## Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

### 32.2.7.2 status\_t LPUART\_Init ( LPUART\_Type \* *base*, const lpuart\_config\_t \* *config*, uint32\_t *srcClock\_Hz* )

This function configures the LPUART module with user-defined settings. Call the [LPUART\\_GetDefaultConfig\(\)](#) function to configure the configuration structure and get the default configuration. The example below shows how to use this API to configure the LPUART.

```
* lpuart_config_t lpuartConfig;
* lpuartConfig.baudRate_Bps = 115200U;
* lpuartConfig.parityMode = kLPUART_ParityDisabled;
* lpuartConfig.dataBitsCount = kLPUART_EightDataBits;
* lpuartConfig.isMsb = false;
* lpuartConfig.stopBitCount = kLPUART_OneStopBit;
* lpuartConfig.txFifoWatermark = 0;
* lpuartConfig.rxFifoWatermark = 1;
* LPUART_Init(LPUART1, &lpuartConfig, 20000000U);
*
```

## Parameters

<i>base</i>	LPUART peripheral base address.
<i>config</i>	Pointer to a user-defined configuration structure.
<i>srcClock_Hz</i>	LPUART clock source frequency in HZ.

## Return values

<i>kStatus_LPUART_BaudrateNotSupport</i>	Baudrate is not support in current clock source.
<i>kStatus_Success</i>	LPUART initialize succeed

### 32.2.7.3 void LPUART\_Deinit ( LPUART\_Type \* *base* )

This function waits for transmit to complete, disables TX and RX, and disables the LPUART clock.

## Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

### 32.2.7.4 void LPUART\_GetDefaultConfig ( lpuart\_config\_t \* *config* )

This function initializes the LPUART configuration structure to a default value. The default values are:  
: lpuartConfig->baudRate\_Bps = 115200U; lpuartConfig->parityMode = kLPUART\_ParityDisabled;  
lpuartConfig->dataBitsCount = kLPUART\_EightDataBits; lpuartConfig->isMsb = false; lpuartConfig->stopBitCount = kLPUART\_OneStopBit; lpuartConfig->txFifoWatermark = 0; lpuartConfig->rxFifoWatermark = 1; lpuartConfig->rxIdleType = kLPUART\_IdleTypeStartBit; lpuartConfig->rxIdleConfig = kLPUART\_IdleCharacter1; lpuartConfig->enableTx = false; lpuartConfig->enableRx = false;

Parameters

<i>config</i>	Pointer to a configuration structure.
---------------	---------------------------------------

### 32.2.7.5 status\_t LPUART\_SetBaudRate ( LPUART\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClock\_Hz* )

This function configures the LPUART module baudrate. This function is used to update the LPUART module baudrate after the LPUART module is initialized by the LPUART\_Init.

```
* LPUART_SetBaudRate(LPUART1, 115200U, 20000000U);
*
```

Parameters

<i>base</i>	LPUART peripheral base address.
<i>baudRate_Bps</i>	LPUART baudrate to be set.
<i>srcClock_Hz</i>	LPUART clock source frequency in HZ.

Return values

<i>kStatus_LPUART_BaudrateNotSupport</i>	Baudrate is not supported in the current clock source.
<i>kStatus_Success</i>	Set baudrate succeeded.

### 32.2.7.6 void LPUART\_Enable9bitMode ( LPUART\_Type \* *base*, bool *enable* )

This function set the 9-bit mode for LPUART module. The 9th bit is not used for parity thus can be modified by user.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>enable</i>	true to enable, false to disable.

### 32.2.7.7 static void LPUART\_SetMatchAddress ( LPUART\_Type \* *base*, uint16\_t *address1*, uint16\_t *address2* ) [inline], [static]

This function configures the address for LPUART module that works as slave in 9-bit data mode. One or two address fields can be configured. When the address field's match enable bit is set, the frame it receives with MSB being 1 is considered as an address frame, otherwise it is considered as data frame. Once the address frame matches one of slave's own addresses, this slave is addressed. This address frame and its following data frames are stored in the receive buffer, otherwise the frames will be discarded. To un-address a slave, just send an address frame with unmatched address.

Note

Any LPUART instance joined in the multi-slave system can work as slave. The position of the address mark is the same as the parity bit when parity is enabled for 8 bit and 9 bit data formats.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>address1</i>	LPUART slave address1.
<i>address2</i>	LPUART slave address2.

### 32.2.7.8 static void LPUART\_EnableMatchAddress ( LPUART\_Type \* *base*, bool *match1*, bool *match2* ) [inline], [static]

Parameters

<i>base</i>	LPUART peripheral base address.
<i>match1</i>	true to enable match address1, false to disable.
<i>match2</i>	true to enable match address2, false to disable.

### 32.2.7.9 static void LPUART\_SetRxFifoWatermark ( LPUART\_Type \* *base*, uint8\_t *water* ) [inline], [static]

Parameters

<i>base</i>	LPUART peripheral base address.
<i>water</i>	Rx FIFO watermark.

### 32.2.7.10 static void LPUART\_SetTxFifoWatermark ( LPUART\_Type \* *base*, uint8\_t *water* ) [inline], [static]

Parameters

<i>base</i>	LPUART peripheral base address.
<i>water</i>	Tx FIFO watermark.

### 32.2.7.11 uint32\_t LPUART\_GetStatusFlags ( LPUART\_Type \* *base* )

This function gets all LPUART status flags. The flags are returned as the logical OR value of the enumerators [\\_lpuart\\_flags](#). To check for a specific status, compare the return value with enumerators in the [\\_lpuart\\_flags](#). For example, to check whether the TX is empty:

```
*     if (kLPUART_TxDataRegEmptyFlag &
*         LPUART_GetStatusFlags(LPUART1))
*     {
*     ...
*     }
```

Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

Returns

LPUART status flags which are ORed by the enumerators in the [\\_lpuart\\_flags](#).

### 32.2.7.12 status\_t LPUART\_ClearStatusFlags ( LPUART\_Type \* *base*, uint32\_t *mask* )

This function clears LPUART status flags with a provided mask. Automatically cleared flags can't be cleared by this function. Flags that can only be cleared or set by hardware are: kLPUART\_TxDataRegEmptyFlag, kLPUART\_TransmissionCompleteFlag, kLPUART\_RxDataRegFullFlag, kLPUART\_RxActiveFlag, kLPUART\_NoiseErrorFlag, kLPUART\_ParityErrorFlag, kLPUART\_TxFifoEmptyFlag, kLPUART\_RxFifoEmptyFlag Note: This API should be called when the Tx/Rx is idle, otherwise it takes no effects.

## Parameters

<i>base</i>	LPUART peripheral base address.
<i>mask</i>	the status flags to be cleared. The user can use the enumerators in the <code>_lpuart_status_flag_t</code> to do the OR operation and get the mask.

## Returns

0 succeed, others failed.

## Return values

<i>kStatus_LPUART_Flag_CannotClearManually</i>	The flag can't be cleared by this function but it is cleared automatically by hardware.
<i>kStatus_Success</i>	Status in the mask are cleared.

**32.2.7.13 void LPUART\_EnableInterrupts ( LPUART\_Type \* *base*, uint32\_t *mask* )**

This function enables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See the [\\_lpuart\\_interrupt\\_enable](#). This examples shows how to enable TX empty interrupt and RX full interrupt:

```
*     LPUART_EnableInterrupts(LPUART1,
    kLPUART_TxDataRegEmptyInterruptEnable |
    kLPUART_RxDataRegFullInterruptEnable);
*
```

## Parameters

<i>base</i>	LPUART peripheral base address.
<i>mask</i>	The interrupts to enable. Logical OR of <a href="#">_lpuart_interrupt_enable</a> .

**32.2.7.14 void LPUART\_DisableInterrupts ( LPUART\_Type \* *base*, uint32\_t *mask* )**

This function disables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See [\\_lpuart\\_interrupt\\_enable](#). This example shows how to disable the TX empty interrupt and RX full interrupt:

```
*     LPUART_DisableInterrupts(LPUART1,
    kLPUART_TxDataRegEmptyInterruptEnable |
    kLPUART_RxDataRegFullInterruptEnable);
*
```

Parameters

<i>base</i>	LPUART peripheral base address.
<i>mask</i>	The interrupts to disable. Logical OR of <a href="#">_lpuart_interrupt_enable</a> .

### 32.2.7.15 uint32\_t LPUART\_GetEnabledInterrupts ( LPUART\_Type \* *base* )

This function gets the enabled LPUART interrupts. The enabled interrupts are returned as the logical OR value of the enumerators [\\_lpuart\\_interrupt\\_enable](#). To check a specific interrupt enable status, compare the return value with enumerators in [\\_lpuart\\_interrupt\\_enable](#). For example, to check whether the TX empty interrupt is enabled:

```
*     uint32_t enabledInterrupts = LPUART_GetEnabledInterrupts(LPUART1);
*
*     if (kLPUART_TxDataRegEmptyInterruptEnable & enabledInterrupts)
*     {
*         ...
*     }
```

Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

Returns

LPUART interrupt flags which are logical OR of the enumerators in [\\_lpuart\\_interrupt\\_enable](#).

### 32.2.7.16 static uintptr\_t LPUART\_GetDataRegisterAddress ( LPUART\_Type \* *base* ) [inline], [static]

This function returns the LPUART data register address, which is mainly used by the DMA/eDMA.

Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

Returns

LPUART data register addresses which are used both by the transmitter and receiver.

### 32.2.7.17 static void LPUART\_EnableTxDMA ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the transmit data register empty flag, STAT[TDRE], to generate DMA requests.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>enable</i>	True to enable, false to disable.

### 32.2.7.18 static void LPUART\_EnableRxDMA ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the receiver data register full flag, STAT[RDRF], to generate DMA requests.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>enable</i>	True to enable, false to disable.

### 32.2.7.19 uint32\_t LPUART\_GetInstance ( LPUART\_Type \* *base* )

Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

Returns

LPUART instance.

### 32.2.7.20 static void LPUART\_EnableTx ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the LPUART transmitter.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>enable</i>	True to enable, false to disable.

### 32.2.7.21 static void LPUART\_EnableRx ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the LPUART receiver.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>enable</i>	True to enable, false to disable.

### 32.2.7.22 static void LPUART\_WriteByte ( LPUART\_Type \* *base*, uint8\_t *data* ) [inline], [static]

This function writes data to the transmitter register directly. The upper layer must ensure that the TX register is empty or that the TX FIFO has room before calling this function.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>data</i>	Data write to the TX register.

### 32.2.7.23 static uint8\_t LPUART\_ReadByte ( LPUART\_Type \* *base* ) [inline], [static]

This function reads data from the receiver register directly. The upper layer must ensure that the receiver register is full or that the RX FIFO has data before calling this function.

Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

Returns

Data read from data register.

### 32.2.7.24 static uint8\_t LPUART\_GetRx\_fifoCount ( LPUART\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

Returns

rx FIFO data count.

### 32.2.7.25 static uint8\_t LPUART\_GetTxFifoCount ( LPUART\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

Returns

tx FIFO data count.

### 32.2.7.26 void LPUART\_SendAddress ( LPUART\_Type \* *base*, uint8\_t *address* )

Parameters

<i>base</i>	LPUART peripheral base address.
<i>address</i>	LPUART slave address.

### 32.2.7.27 status\_t LPUART\_WriteBlocking ( LPUART\_Type \* *base*, const uint8\_t \* *data*, size\_t *length* )

This function polls the transmitter register, first waits for the register to be empty or TX FIFO to have room, and writes data to the transmitter buffer, then waits for the dat to be sent out to the bus.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>data</i>	Start address of the data to write.
<i>length</i>	Size of the data to write.

Return values

<i>kStatus_LPUART_- Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully wrote all data.

### 32.2.7.28 **status\_t LPUART\_ReadBlocking ( LPUART\_Type \* *base*, uint8\_t \* *data*, size\_t *length* )**

This function polls the receiver register, waits for the receiver register full or receiver FIFO has data, and reads data from the TX register.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>data</i>	Start address of the buffer to store the received data.
<i>length</i>	Size of the buffer.

Return values

<i>kStatus_LPUART_Rx- HardwareOverrun</i>	Receiver overrun happened while receiving data.
<i>kStatus_LPUART_Noise- Error</i>	Noise error happened while receiving data.
<i>kStatus_LPUART_- FramingError</i>	Framing error happened while receiving data.
<i>kStatus_LPUART_Parity- Error</i>	Parity error happened while receiving data.
<i>kStatus_LPUART_- Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully received all data.

### 32.2.7.29 **void LPUART\_TransferCreateHandle ( LPUART\_Type \* *base*, Ipuart\_handle\_t \* *handle*, Ipuart\_transfer\_callback\_t *callback*, void \* *userData* )**

This function initializes the LPUART handle, which can be used for other LPUART transactional APIs. Usually, for a specified LPUART instance, call this API once to get the initialized handle.

The LPUART driver supports the "background" receiving, which means that user can set up an RX ring buffer optionally. Data received is stored into the ring buffer even when the user doesn't call the [LPUART\\_TransferReceiveNonBlocking\(\)](#) API. If there is already data received in the ring buffer, the user

can get the received data from the ring buffer directly. The ring buffer is disabled if passing NULL as `ringBuffer`.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>callback</i>	Callback function.
<i>userData</i>	User data.

### 32.2.7.30 `status_t LPUART_TransferSendNonBlocking ( LPUART_Type * base, Ipuart_handle_t * handle, Ipuart_transfer_t * xfer )`

This function send data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data written to the transmitter register. When all data is written to the TX register in the ISR, the LPUART driver calls the callback function and passes the `kStatus_LPUART_TxIdle` as status parameter.

Note

The `kStatus_LPUART_TxIdle` is passed to the upper layer when all data are written to the TX register. However, there is no check to ensure that all the data sent out. Before disabling the T-X, check the `kLPUART_TransmissionCompleteFlag` to ensure that the transmit is finished.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>xfer</i>	LPUART transfer structure, see <a href="#">Ipuart_transfer_t</a> .

Return values

<code>kStatus_Success</code>	Successfully start the data transmission.
<code>kStatus_LPUART_TxBusy</code>	Previous transmission still not finished, data not all written to the TX register.
<code>kStatus_InvalidArgument</code>	Invalid argument.

### 32.2.7.31 `void LPUART_TransferStartRingBuffer ( LPUART_Type * base, Ipuart_handle_t * handle, uint8_t * ringBuffer, size_t ringBufferSize )`

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received is stored into the ring buffer even when the user doesn't call the `UART_TransferReceiveNonBlocking()` API. If there is already data received in the ring buffer, the user can get the received data from the ring buffer directly.

#### Note

When using RX ring buffer, one byte is reserved for internal use. In other words, if `ringBufferSize` is 32, then only 31 bytes are used for saving data.

#### Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>ringBuffer</i>	Start address of ring buffer for background receiving. Pass NULL to disable the ring buffer.
<i>ringBufferSize</i>	size of the ring buffer.

### 32.2.7.32 void LPUART\_TransferStopRingBuffer ( `LPUART_Type * base, Ipuart_handle_t * handle` )

This function aborts the background transfer and uninstalls the ring buffer.

#### Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.

### 32.2.7.33 size\_t LPUART\_TransferGetRxRingBufferLength ( `LPUART_Type * base, Ipuart_handle_t * handle` )

#### Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.

#### Returns

Length of received data in RX ring buffer.

**32.2.7.34 void LPUART\_TransferAbortSend ( LPUART\_Type \* *base*, Ipuart\_handle\_t \* *handle* )**

This function aborts the interrupt driven data sending. The user can get the remainBtyes to find out how many bytes are not sent out.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.

### 32.2.7.35 status\_t LPUART\_TransferGetSendCount ( **LPUART\_Type \* base,**                  **Ipuart\_handle\_t \* handle, uint32\_t \* count** )

This function gets the number of bytes that have been sent out to bus by an interrupt method.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>count</i>	Send bytes count.

Return values

<i>kStatus_NoTransferInProgress</i>	No send in progress.
<i>kStatus_InvalidArgument</i>	Parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter <i>count</i> ;

### 32.2.7.36 status\_t LPUART\_TransferReceiveNonBlocking ( **LPUART\_Type \* base,**                  **Ipuart\_handle\_t \* handle, Ipuart\_transfer\_t \* xfer, size\_t \* receivedBytes** )

This function receives data using an interrupt method. This is a non-blocking function which returns without waiting to ensure that all data are received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter *receivedBytes* shows how many bytes are copied from the ring buffer. After copying, if the data in the ring buffer is not enough for read, the receive request is saved by the LPUART driver. When the new data arrives, the receive request is serviced first. When all data is received, the LPUART driver notifies the upper layer through a callback function and passes a status parameter *kStatus\_UART\_RxIdle*. For example, the upper layer needs 10 bytes but there are only 5 bytes in ring buffer. The 5 bytes are copied to *xfer->data*, which returns with the parameter *receivedBytes* set to 5. For the remaining 5 bytes, the newly arrived data is saved from *xfer->data[5]*. When 5 bytes are received, the LPUART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to *xfer->data*. When all data is received, the upper layer is notified.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>xfer</i>	LPUART transfer structure, see <code>uart_transfer_t</code> .
<i>receivedBytes</i>	Bytes received from the ring buffer directly.

Return values

<i>kStatus_Success</i>	Successfully queue the transfer into the transmit queue.
<i>kStatus_LPUART_Rx-Busy</i>	Previous receive request is not finished.
<i>kStatus_InvalidArgument</i>	Invalid argument.

### 32.2.7.37 void LPUART\_TransferAbortReceive ( `LPUART_Type * base, Ipuart_handle_t * handle` )

This function aborts the interrupt-driven data receiving. The user can get the remainBytes to find out how many bytes not received yet.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.

### 32.2.7.38 status\_t LPUART\_TransferGetReceiveCount ( `LPUART_Type * base, Ipuart_handle_t * handle, uint32_t * count` )

This function gets the number of bytes that have been received.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>count</i>	Receive bytes count.

Return values

<i>kStatus_NoTransferInProgress</i>	No receive in progress.
<i>kStatus_InvalidArgument</i>	Parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter <code>count</code> ;

### 32.2.7.39 void LPUART\_TransferHandleIRQ ( LPUART\_Type \* *base*, void \* *irqHandle* )

This function handles the LPUART transmit and receive IRQ request.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>irqHandle</i>	LPUART handle pointer.

### 32.2.7.40 void LPUART\_TransferHandleErrorIRQ ( LPUART\_Type \* *base*, void \* *irqHandle* )

This function handles the LPUART error IRQ request.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>irqHandle</i>	LPUART handle pointer.

## 32.3 LPUART eDMA Driver

### 32.3.1 Overview

#### Data Structures

- struct [lpuart\\_edma\\_handle\\_t](#)  
*LPUART eDMA handle.* [More...](#)

#### TypeDefs

- [typedef void\(\\* lpuart\\_edma\\_transfer\\_callback\\_t \)](#)(LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, [status\\_t](#) status, void \*userData)  
*LPUART transfer callback function.*

#### Driver version

- #define [FSL\\_LPUART\\_EDMA\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 6, 0))  
*LPUART EDMA driver version.*

#### eDMA transactional

- void [LPUART\\_TransferCreateHandleEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, [lpuart\\_edma\\_transfer\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*txEdmaHandle, [edma\\_handle\\_t](#) \*rxEdmaHandle)  
*Initializes the LPUART handle which is used in transactional functions.*
- [status\\_t LPUART\\_SendEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, [lpuart\\_transfer\\_t](#) \*xfer)  
*Sends data using eDMA.*
- [status\\_t LPUART\\_ReceiveEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, [lpuart\\_transfer\\_t](#) \*xfer)  
*Receives data using eDMA.*
- void [LPUART\\_TransferAbortSendEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle)  
*Aborts the sent data using eDMA.*
- void [LPUART\\_TransferAbortReceiveEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle)  
*Aborts the received data using eDMA.*
- [status\\_t LPUART\\_TransferGetSendCountEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of bytes written to the LPUART TX register.*
- [status\\_t LPUART\\_TransferGetReceiveCountEDMA](#) (LPUART\_Type \*base, lpuart\_edma\_handle\_t \*handle, uint32\_t \*count)  
*Gets the number of received bytes.*
- void [LPUART\\_TransferEdmaHandleIRQ](#) (LPUART\_Type \*base, void \*lpuartEdmaHandle)  
*LPUART eDMA IRQ handle function.*

### 32.3.2 Data Structure Documentation

#### 32.3.2.1 struct \_lpuart\_edma\_handle

##### Data Fields

- `lpuart_edma_transfer_callback_t callback`  
*Callback function.*
- `void *userData`  
*LPUART callback function parameter.*
- `size_t rxDataSizeAll`  
*Size of the data to receive.*
- `size_t txDataSizeAll`  
*Size of the data to send out.*
- `edma_handle_t *txEdmaHandle`  
*The eDMA TX channel used.*
- `edma_handle_t *rxEdmaHandle`  
*The eDMA RX channel used.*
- `uint8_t nbytes`  
*eDMA minor byte transfer count initially configured.*
- `volatile uint8_t txState`  
*TX transfer state.*
- `volatile uint8_t rxState`  
*RX transfer state.*

## Field Documentation

- (1) `lpuart_edma_transfer_callback_t lpuart_edma_handle_t::callback`
- (2) `void* lpuart_edma_handle_t::userData`
- (3) `size_t lpuart_edma_handle_t::rxDataSizeAll`
- (4) `size_t lpuart_edma_handle_t::txDataSizeAll`
- (5) `edma_handle_t* lpuart_edma_handle_t::txEdmaHandle`
- (6) `edma_handle_t* lpuart_edma_handle_t::rxEdmaHandle`
- (7) `uint8_t lpuart_edma_handle_t::nbytes`
- (8) `volatile uint8_t lpuart_edma_handle_t::txState`

### 32.3.3 Macro Definition Documentation

**32.3.3.1 #define FSL\_LPUART\_EDMA\_DRIVER\_VERSION (MAKE\_VERSION(2, 6, 0))**

### 32.3.4 Typedef Documentation

**32.3.4.1 typedef void(\* lpuart\_edma\_transfer\_callback\_t)(LPUART\_Type \*base,  
lpuart\_edma\_handle\_t \*handle, status\_t status, void \*userData)**

### 32.3.5 Function Documentation

**32.3.5.1 void LPUART\_TransferCreateHandleEDMA ( LPUART\_Type \* *base*,  
lpuart\_edma\_handle\_t \* *handle*, lpuart\_edma\_transfer\_callback\_t *callback*, void  
\* *userData*, edma\_handle\_t \* *txEdmaHandle*, edma\_handle\_t \* *rxEdmaHandle* )**

#### Note

This function disables all LPUART interrupts.

#### Parameters

<i>base</i>	LPUART peripheral base address.
-------------	---------------------------------

<i>handle</i>	Pointer to lpuart_edma_handle_t structure.
<i>callback</i>	Callback function.
<i>userData</i>	User data.
<i>txEdmaHandle</i>	User requested DMA handle for TX DMA transfer.
<i>rxEdmaHandle</i>	User requested DMA handle for RX DMA transfer.

### 32.3.5.2 status\_t LPUART\_SendEDMA ( LPUART\_Type \* *base*, Ipuart\_edma\_handle\_t \* *handle*, Ipuart\_transfer\_t \* *xfer* )

This function sends data using eDMA. This is a non-blocking function, which returns right away. When all data is sent, the send callback function is called.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>xfer</i>	LPUART eDMA transfer structure. See <a href="#">Ipuart_transfer_t</a> .

Return values

<i>kStatus_Success</i>	if succeed, others failed.
<i>kStatus_LPUART_TxBusy</i>	Previous transfer on going.
<i>kStatus_InvalidArgument</i>	Invalid argument.

### 32.3.5.3 status\_t LPUART\_ReceiveEDMA ( LPUART\_Type \* *base*, Ipuart\_edma\_handle\_t \* *handle*, Ipuart\_transfer\_t \* *xfer* )

This function receives data using eDMA. This is non-blocking function, which returns right away. When all data is received, the receive callback function is called.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	Pointer to lpuart_edma_handle_t structure.

<i>xfer</i>	LPUART eDMA transfer structure, see <a href="#">lpuart_transfer_t</a> .
-------------	---

Return values

<i>kStatus_Success</i>	if succeed, others fail.
<i>kStatus_LPUART_Rx-Busy</i>	Previous transfer ongoing.
<i>kStatus_InvalidArgument</i>	Invalid argument.

### 32.3.5.4 void LPUART\_TransferAbortSendEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle* )

This function aborts the sent data using eDMA.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	Pointer to lpuart_edma_handle_t structure.

### 32.3.5.5 void LPUART\_TransferAbortReceiveEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle* )

This function aborts the received data using eDMA.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	Pointer to lpuart_edma_handle_t structure.

### 32.3.5.6 status\_t LPUART\_TransferGetSendCountEDMA ( LPUART\_Type \* *base*, lpuart\_edma\_handle\_t \* *handle*, uint32\_t \* *count* )

This function gets the number of bytes written to the LPUART TX register by DMA.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>count</i>	Send bytes count.

Return values

<i>kStatus_NoTransferIn-Progress</i>	No send in progress.
<i>kStatus_InvalidArgument</i>	Parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter <i>count</i> ;

### 32.3.5.7 **status\_t LPUART\_TransferGetReceiveCountEDMA ( LPUART\_Type \* *base*, Ipuart\_edma\_handle\_t \* *handle*, uint32\_t \* *count* )**

This function gets the number of received bytes.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>count</i>	Receive bytes count.

Return values

<i>kStatus_NoTransferIn-Progress</i>	No receive in progress.
<i>kStatus_InvalidArgument</i>	Parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter <i>count</i> ;

### 32.3.5.8 **void LPUART\_TransferEdmaHandleIRQ ( LPUART\_Type \* *base*, void \* *IpuartEdmaHandle* )**

This function handles the LPUART tx complete IRQ request and invoke user callback. It is not set to static so that it can be used in user application.

Note

This function is used as default IRQ handler by double weak mechanism. If user's specific IRQ handler is implemented, make sure this function is invoked in the handler.

## Parameters

<i>base</i>	LPUART peripheral base address.
<i>lpuartEdma-Handle</i>	LPUART handle pointer.

## 32.4 LPUART FreeRTOS Driver

### 32.4.1 Overview

#### Data Structures

- struct `lpuart_rtos_config_t`  
*LPUART RTOS configuration structure.* [More...](#)

#### Driver version

- #define `FSL_LPUART_FREERTOS_DRIVER_VERSION` (`MAKE_VERSION(2, 6, 0)`)  
*LPUART FreeRTOS driver version.*

#### LPUART RTOS Operation

- int `LPUART_RTOS_Init` (`lpuart_rtos_handle_t *handle, lpuart_handle_t *t_handle, const lpuart_rtos_config_t *cfg`)  
*Initializes an LPUART instance for operation in RTOS.*
- int `LPUART_RTOS_Deinit` (`lpuart_rtos_handle_t *handle`)  
*Deinitializes an LPUART instance for operation.*

#### LPUART transactional Operation

- int `LPUART_RTOS_Send` (`lpuart_rtos_handle_t *handle, uint8_t *buffer, uint32_t length`)  
*Sends data in the background.*
- int `LPUART_RTOS_Receive` (`lpuart_rtos_handle_t *handle, uint8_t *buffer, uint32_t length, size_t *received`)  
*Receives data.*
- int `LPUART_RTOS_SetRxTimeout` (`lpuart_rtos_handle_t *handle, uint32_t rx_timeout_constant_ms, uint32_t rx_timeout_multiplier_ms`)  
*Set RX timeout in runtime.*
- int `LPUART_RTOS_SetTxTimeout` (`lpuart_rtos_handle_t *handle, uint32_t tx_timeout_constant_ms, uint32_t tx_timeout_multiplier_ms`)  
*Set TX timeout in runtime.*

### 32.4.2 Data Structure Documentation

#### 32.4.2.1 struct `lpuart_rtos_config_t`

##### Data Fields

- `LPUART_Type * base`  
*UART base address.*

- `uint32_t srclk`  
*UART source clock in Hz.*
- `uint32_t baudrate`  
*Desired communication speed.*
- `lpuart_parity_mode_t parity`  
*Parity setting.*
- `lpuart_stop_bit_count_t stopbits`  
*Number of stop bits to use.*
- `uint8_t * buffer`  
*Buffer for background reception.*
- `uint32_t buffer_size`  
*Size of buffer for background reception.*
- `uint32_t rx_timeout_constant_ms`  
*RX timeout applied per receive.*
- `uint32_t rx_timeout_multiplier_ms`  
*RX timeout added for each byte of the receive.*
- `uint32_t tx_timeout_constant_ms`  
*TX timeout applied per transmission.*
- `uint32_t tx_timeout_multiplier_ms`  
*TX timeout added for each byte of the transmission.*
- `bool enableRxRTS`  
*RX RTS enable.*
- `bool enableTxCTS`  
*TX CTS enable.*
- `lpuart_transmit_cts_source_t txCtsSource`  
*TX CTS source.*
- `lpuart_transmit_cts_config_t txCtsConfig`  
*TX CTS configure.*

## Field Documentation

- (1) `uint32_t lpuart_rtos_config_t::rx_timeout_multiplier_ms`
- (2) `uint32_t lpuart_rtos_config_t::tx_timeout_multiplier_ms`

### 32.4.3 Macro Definition Documentation

**32.4.3.1 #define FSL\_LPUART\_FREERTOS\_DRIVER\_VERSION (MAKE\_VERSION(2, 6, 0))**

### 32.4.4 Function Documentation

**32.4.4.1 int LPUART\_RTOs\_Init ( `lpuart_rtos_handle_t * handle`, `lpuart_handle_t * t_handle`, `const lpuart_rtos_config_t * cfg` )**

Parameters

<i>handle</i>	The RTOS LPUART handle, the pointer to an allocated space for RTOS context.
<i>t_handle</i>	The pointer to an allocated space to store the transactional layer internal state.
<i>cfg</i>	The pointer to the parameters required to configure the LPUART after initialization.

Returns

0 succeed, others failed

#### 32.4.4.2 int LPUART\_RTOS\_Deinit ( *Ipuart\_rtos\_handle\_t \* handle* )

This function deinitializes the LPUART module, sets all register value to the reset value, and releases the resources.

Parameters

<i>handle</i>	The RTOS LPUART handle.
---------------	-------------------------

#### 32.4.4.3 int LPUART\_RTOS\_Send ( *Ipuart\_rtos\_handle\_t \* handle, uint8\_t \* buffer, uint32\_t length* )

This function sends data. It is an synchronous API. If the hardware buffer is full, the task is in the blocked state.

Parameters

<i>handle</i>	The RTOS LPUART handle.
<i>buffer</i>	The pointer to buffer to send.
<i>length</i>	The number of bytes to send.

#### 32.4.4.4 int LPUART\_RTOS\_Receive ( *Ipuart\_rtos\_handle\_t \* handle, uint8\_t \* buffer, uint32\_t length, size\_t \* received* )

This function receives data from LPUART. It is an synchronous API. If any data is immediately available it is returned immediately and the number of bytes received.

## Parameters

<i>handle</i>	The RTOS LPUART handle.
<i>buffer</i>	The pointer to buffer where to write received data.
<i>length</i>	The number of bytes to receive.
<i>received</i>	The pointer to a variable of size_t where the number of received data is filled.

#### 32.4.4.5 int LPUART\_RTOSETXTIMEOUT ( Ipuart\_rtos\_handle\_t \* *handle*, uint32\_t *rx\_timeout\_constant\_ms*, uint32\_t *rx\_timeout\_multiplier\_ms* )

This function can modify RX timeout between initialization and receive.

param handle The RTOS LPUART handle. param rx\_timeout\_constant\_ms RX timeout applied per receive. param rx\_timeout\_multiplier\_ms RX timeout added for each byte of the receive.

#### 32.4.4.6 int LPUART\_RTOSETXTIMEOUT ( Ipuart\_rtos\_handle\_t \* *handle*, uint32\_t *tx\_timeout\_constant\_ms*, uint32\_t *tx\_timeout\_multiplier\_ms* )

This function can modify TX timeout between initialization and send.

param handle The RTOS LPUART handle. param tx\_timeout\_constant\_ms TX timeout applied per transmission. param tx\_timeout\_multiplier\_ms TX timeout added for each byte of the transmission.

## 32.5 LPUART CMSIS Driver

This section describes the programming interface of the LPUART Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The LPUART driver includes transactional APIs.

Transactional APIs can be used to enable the peripheral quickly and in the application if the code size and performance of transactional APIs can satisfy the requirements. If the code size and performance are critical requirements please write custom code.

### 32.5.1 Function groups

#### 32.5.1.1 LPUART CMSIS GetVersion Operation

This function group will return the LPUART CMSIS Driver version to user.

#### 32.5.1.2 LPUART CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

#### 32.5.1.3 LPUART CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialized the lpuart instance . And this API must be called before you configure a lpuart instance or after you Deinit a lpuart instance.The right steps to start an instance is that you must initialize the instance which been selected firstly,then you can power on the instance.After these all have been done,you can configure the instance by using control operation.If you want to Uninitialize the instance, you must power off the instance first.

#### 32.5.1.4 LPUART CMSIS Transfer Operation

This function group controls the transfer, send/receive data.

#### 32.5.1.5 LPUART CMSIS Status Operation

This function group gets the LPUART transfer status.

### **32.5.1.6 LPUART CMSIS Control Operation**

This function can configure an instance ,set baudrate for lpuart, get current baudrate ,set transfer data bits and other control command.

# Chapter 33

## OCOTP: On Chip One-Time Programmable controller.

### 33.1 Overview

The MCUXpresso SDK provides a peripheral driver for the OCOTP module of MCUXpresso SDK devices.

This section contains information describing the requirements for the on-chip eFuse OTP controller along with details about the block functionality and implementation.

### 33.2 OCOTP function group

The OCOTP driver support operaing API to allow read and write the fuse map.

#### 33.2.1 Initialization and de-initialization

The funciton [OCOTP\\_Init\(\)](#) is to initialize the OCOTP with peripheral base address and source clock frequency.

The function [OCOTP\\_Deinit\(\)](#) is to de-initialize the OCOTP controller with peripheral base address.

#### 33.2.2 Read and Write operation

The function [OCOTP\\_ReloadShadowRegister\(\)](#) is to reload the value from the fuse map. this API should be called firstly before reading the register.

The [OCOTP\\_ReadFuseShadowRegister\(\)](#) is to read the value from a given address, if operation is success, a known value will be return, othwise, a value of 0xBADABADA will be returned.

The function [OCOTP\\_WriteFuseShadowRegister\(\)](#) will write a specific value to a known address. please check the return status o make sure whether the access to register is success.

### 33.3 OCOTP example

This example shows how to get the controller version using API. Due to the eFuse is One-Time programmable, example will only print the information of OCOTP controller version. If more operations are needed, please using the API to implement the write and read operation.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ocotp

### Data Structures

- struct [ocotp\\_timing\\_t](#)  
*OCOTP timing structure.* [More...](#)

## Enumerations

- enum {
   
    kStatus\_OCOTP\_AccessError = MAKE\_STATUS(kStatusGroup\_SDK\_OCOTP, 0),
   
    kStatus\_OCOTP\_CrcFail = MAKE\_STATUS(kStatusGroup\_SDK\_OCOTP, 1),
   
    kStatus\_OCOTP\_ReloadError,
   
    kStatus\_OCOTP\_ProgramFail = MAKE\_STATUS(kStatusGroup\_SDK\_OCOTP, 3),
   
    kStatus\_OCOTP\_Locked = MAKE\_STATUS(kStatusGroup\_SDK\_OCOTP, 4) }
- \_ocotp\_status Error codes for the OCOTP driver.*

## Functions

- void **OCOTP\_Init** (OCOTP\_Type \*base, uint32\_t srcClock\_Hz)
   
*Initializes OCOTP controller.*
- void **OCOTP\_Deinit** (OCOTP\_Type \*base)
   
*De-initializes OCOTP controller.*
- static bool **OCOTP\_CheckBusyStatus** (OCOTP\_Type \*base)
   
*Checking the BUSY bit in CTRL register.*
- static bool **OCOTP\_CheckErrorStatus** (OCOTP\_Type \*base)
   
*Checking the ERROR bit in CTRL register.*
- static void **OCOTP\_ClearErrorStatus** (OCOTP\_Type \*base)
   
*Clear the error bit if this bit is set.*
- status\_t **OCOTP\_ReloadShadowRegister** (OCOTP\_Type \*base)
   
*Reload the shadow register.*
- uint32\_t **OCOTP\_ReadFuseShadowRegister** (OCOTP\_Type \*base, uint32\_t address)
   
*Read the fuse shadow register with the fuse address.*
- status\_t **OCOTP\_ReadFuseShadowRegisterExt** (OCOTP\_Type \*base, uint32\_t address, uint32\_t \*data, uint8\_t fuseWords)
   
*Read the fuse shadow register from the fuse address.*
- status\_t **OCOTP\_WriteFuseShadowRegister** (OCOTP\_Type \*base, uint32\_t address, uint32\_t data)
   
*Write the fuse shadow register with the fuse address and data.*
- status\_t **OCOTP\_WriteFuseShadowRegisterWithLock** (OCOTP\_Type \*base, uint32\_t address, uint32\_t data, bool lock)
   
*Write the fuse shadow register and lock it.*
- static uint32\_t **OCOTP\_GetVersion** (OCOTP\_Type \*base)
   
*Get the OCOTP controller version from the register.*

## Driver version

- #define **FSL\_OCOTP\_DRIVER\_VERSION** (MAKE\_VERSION(2, 1, 3))
   
*OCOTP driver version.*

## 33.4 Data Structure Documentation

### 33.4.1 struct ocotp\_timing\_t

Note that, these value are used for calcalating the read/write timings. And the values should statisfy below rules:

Tsp\_rd=(WAIT+1)/ipg\_clk\_freq should be  $\geq$  150ns; Tsp\_pgm=(RELAX+1)/ipg\_clk\_freq should be  $\geq$  100ns; Trd = ((STROBE\_READ+1)- 2\*(RELAX\_READ+1)) /ipg\_clk\_freq, The Trd is required to be larger than 40 ns. Tpgm = ((STROBE\_PROG+1)- 2\*(RELAX\_PROG+1)) /ipg\_clk\_freq; The Tpgm should be configured within the range of 9000 ns < Tpgm < 11000 ns;

## Data Fields

- `uint32_t wait`  
*Wait time value to fill in the TIMING register.*
- `uint32_t relax`  
*Relax time value to fill in the TIMING register.*
- `uint32_t strobe_prog`  
*Strobe program time value to fill in the TIMING register.*
- `uint32_t strobe_read`  
*Strobe read time value to fill in the TIMING register.*

### Field Documentation

- (1) `uint32_t ocotp_timing_t::wait`
- (2) `uint32_t ocotp_timing_t::relax`
- (3) `uint32_t ocotp_timing_t::strobe_prog`
- (4) `uint32_t ocotp_timing_t::strobe_read`

## 33.5 Macro Definition Documentation

`#define FSL_OCOTP_DRIVER_VERSION (MAKE_VERSION(2, 1, 3))`

## 33.6 Enumeration Type Documentation

### 33.6.1 anonymous enum

Enumerator

`kStatus_OCOTP_AccessError` eFuse and shadow register access error.

`kStatus_OCOTP_CrcFail` CRC check failed.

`kStatus_OCOTP_ReloadError` Error happens during reload shadow register.

`kStatus_OCOTP_ProgramFail` Fuse programming failed.

`kStatus_OCOTP_Locked` Fuse is locked and cannot be programmed.

## 33.7 Function Documentation

`void OCOTP_Init( OCOTP_Type * base, uint32_t srcClock_Hz )`

Parameters

<i>base</i>	OCOTP peripheral base address.
<i>srcClock_Hz</i>	source clock frequency in unit of Hz. When the macro FSL_FEATURE_OCOTP_HAS_TIMING_CTRL is defined as 0, this parameter is not used, application could pass in 0 in this case.

### 33.7.2 void OCOTP\_Deinit( OCOTP\_Type \* *base* )

Return values

<i>kStatus_Success</i>	upon successful execution, error status otherwise.
------------------------	--

### 33.7.3 static bool OCOTP\_CheckBusyStatus( OCOTP\_Type \* *base* ) [inline], [static]

Checking this BUSY bit will help confirm if the OCOTP controller is ready for access.

Parameters

<i>base</i>	OCOTP peripheral base address.
-------------	--------------------------------

Return values

<i>true</i>	for bit set and false for cleared.
-------------	------------------------------------

### 33.7.4 static bool OCOTP\_CheckErrorStatus( OCOTP\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	OCOTP peripheral base address.
-------------	--------------------------------

Return values

<i>true</i>	for bit set and false for cleared.
-------------	------------------------------------

### 33.7.5 static void OCOTP\_ClearErrorStatus ( OCOTP\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	OCOTP peripheral base address.
-------------	--------------------------------

### 33.7.6 status\_t OCOTP\_ReloadShadowRegister ( OCOTP\_Type \* *base* )

This function will help reload the shadow register without resetting the OCOTP module. Please make sure the OCOTP has been initialized before calling this API.

Parameters

<i>base</i>	OCOTP peripheral base addess.
-------------	-------------------------------

Return values

<i>kStatus_Success</i>	Reload success.
<i>kStatus_OCOTP_Reload_Error</i>	Reload failed.

### 33.7.7 uint32\_t OCOTP\_ReadFuseShadowRegister ( OCOTP\_Type \* *base*, uint32\_t *address* )

**Deprecated** Use [OCOTP\\_ReadFuseShadowRegisterExt](#) instead of this function.

Parameters

<i>base</i>	OCOTP peripheral base address.
-------------	--------------------------------

<i>address</i>	the fuse address to be read from.
----------------	-----------------------------------

Returns

The read out data.

### 33.7.8 status\_t OCOTP\_ReadFuseShadowRegisterExt ( OCOTP\_Type \* *base*, uint32\_t *address*, uint32\_t \* *data*, uint8\_t *fuseWords* )

This function reads fuse from *address*, how many words to read is specified by the parameter *fuseWords*. This function could read at most OCOTP\_READ\_FUSE\_DATA\_COUNT fuse word one time.

Parameters

<i>base</i>	OCOTP peripheral base address.
<i>address</i>	the fuse address to be read from.
<i>data</i>	Data array to save the readout fuse value.
<i>fuseWords</i>	How many words to read.

Return values

<i>kStatus_Success</i>	Read success.
<i>kStatus_Fail</i>	Error occurs during read.

### 33.7.9 status\_t OCOTP\_WriteFuseShadowRegister ( OCOTP\_Type \* *base*, uint32\_t *address*, uint32\_t *data* )

Please make sure the write address is not locked while calling this API.

Parameters

<i>base</i>	OCOTP peripheral base address.
<i>address</i>	the fuse address to be written.
<i>data</i>	the value will be written to fuse address.

Return values

<i>write</i>	status, kStatus_Success for success and kStatus_Fail for failed.
--------------	--

### 33.7.10 status\_t OCOTP\_WriteFuseShadowRegisterWithLock ( OCOTP\_Type \* *base*, uint32\_t *address*, uint32\_t *data*, bool *lock* )

Please make sure the write address is not locked while calling this API.

Some OCOTP controller supports ECC mode and redundancy mode (see reference manual for more details). OCOTP controller will auto select ECC or redundancy mode to program the fuse word according to fuse map definition. In ECC mode, the 32 fuse bits in one word can only be written once. In redundancy mode, the word can be written more than once as long as they are different fuse bits. Set parameter *lock* as true to force use ECC mode.

Parameters

<i>base</i>	OCOTP peripheral base address.
<i>address</i>	The fuse address to be written.
<i>data</i>	The value will be written to fuse address.
<i>lock</i>	Lock or unlock write fuse shadow register operation.

Return values

<i>kStatus_Success</i>	Program and reload success.
<i>kStatus_OCOTP_Locked</i>	The eFuse word is locked and cannot be programmed.
<i>kStatus_OCOTP_ProgramFail</i>	eFuse word programming failed.
<i>kStatus_OCOTP_Reload_Error</i>	eFuse word programming success, but error happens during reload the values.
<i>kStatus_OCOTP_Access_Error</i>	Cannot access eFuse word.

### 33.7.11 static uint32\_t OCOTP\_GetVersion ( OCOTP\_Type \* *base* ) [inline], [static]

### Parameters

<i>base</i>	OCOTP peripheral base address.
-------------	--------------------------------

### Return values

<i>return</i>	the version value.
---------------	--------------------

# Chapter 34

## PIT: Periodic Interrupt Timer

### 34.1 Overview

The MCUXpresso SDK provides a driver for the Periodic Interrupt Timer (PIT) of MCUXpresso SDK devices.

### 34.2 Function groups

The PIT driver supports operating the module as a time counter.

#### 34.2.1 Initialization and deinitialization

The function [PIT\\_Init\(\)](#) initializes the PIT with specified configurations. The function [PIT\\_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the PIT operation in debug mode.

The function [PIT\\_SetTimerChainMode\(\)](#) configures the chain mode operation of each PIT channel.

The function [PIT\\_Deinit\(\)](#) disables the PIT timers and disables the module clock.

#### 34.2.2 Timer period Operations

The function [PITR\\_SetTimerPeriod\(\)](#) sets the timer period in units of count. Timers begin counting down from the value set by this function until it reaches 0.

The function [PIT\\_GetCurrentTimerCount\(\)](#) reads the current timer counting value. This function returns the real-time timer counting value, in a range from 0 to a timer period.

The timer period operation functions takes the count value in ticks. Users can call the utility macros provided in `fsl_common.h` to convert to microseconds or milliseconds.

#### 34.2.3 Start and Stop timer operations

The function [PIT\\_StartTimer\(\)](#) starts the timer counting. After calling this function, the timer loads the period value set earlier via the [PIT\\_SetPeriod\(\)](#) function and starts counting down to 0. When the timer reaches 0, it generates a trigger pulse and sets the timeout interrupt flag.

The function [PIT\\_StopTimer\(\)](#) stops the timer counting.

### 34.2.4 Status

Provides functions to get and clear the PIT status.

### 34.2.5 Interrupt

Provides functions to enable/disable PIT interrupts and get current enabled interrupts.

### 34.3 Typical use case

### 34.3.1 PIT tick example

Updates the PIT period and toggles an LED periodically. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pit

# Data Structures

- struct `pit_config_t`  
*PIT configuration structure.* [More...](#)

## Enumerations

- enum pit\_chnl\_t {  
    kPIT\_Chnl\_0 = 0U,  
    kPIT\_Chnl\_1,  
    kPIT\_Chnl\_2,  
    kPIT\_Chnl\_3 }  
    *List of PIT channels.*
  - enum pit\_interrupt\_enable\_t { kPIT\_TimerInterruptEnable = PIT\_TCTRL\_TIE\_MASK }  
    *List of PIT interrupts.*
  - enum pit\_status\_flags\_t { kPIT\_TimerFlag = PIT\_TFLG\_TIF\_MASK }  
    *List of PIT status flags.*

# Functions

- `uint64_t PIT_GetLifetimeTimerCount(PIT_Type *base)`  
*Reads the current lifetime counter value.*

## **Driver version**

- `#define FSL_PIT_DRIVER_VERSION (MAKE_VERSION(2, 0, 4))`  
*PIT Driver Version 2.0.4.*

## Initialization and deinitialization

- void **PIT\_Init** (PIT\_Type \*base, const pit\_config\_t \*config)

- Ungates the PIT clock, enables the PIT module, and configures the peripheral for basic operations.
- void [PIT\\_Deinit](#) (PIT\_Type \*base)  
Gates the PIT clock and disables the PIT module.
- static void [PIT\\_GetDefaultConfig](#) (pit\_config\_t \*config)  
Fills in the PIT configuration structure with the default settings.
- static void [PIT\\_SetTimerChainMode](#) (PIT\_Type \*base, pit\_chnl\_t channel, bool enable)  
Enables or disables chaining a timer with the previous timer.

## Interrupt Interface

- static void [PIT\\_EnableInterrupts](#) (PIT\_Type \*base, pit\_chnl\_t channel, uint32\_t mask)  
Enables the selected PIT interrupts.
- static void [PIT\\_DisableInterrupts](#) (PIT\_Type \*base, pit\_chnl\_t channel, uint32\_t mask)  
Disables the selected PIT interrupts.
- static uint32\_t [PIT\\_GetEnabledInterrupts](#) (PIT\_Type \*base, pit\_chnl\_t channel)  
Gets the enabled PIT interrupts.

## Status Interface

- static uint32\_t [PIT\\_GetStatusFlags](#) (PIT\_Type \*base, pit\_chnl\_t channel)  
Gets the PIT status flags.
- static void [PIT\\_ClearStatusFlags](#) (PIT\_Type \*base, pit\_chnl\_t channel, uint32\_t mask)  
Clears the PIT status flags.

## Read and Write the timer period

- static void [PIT\\_SetTimerPeriod](#) (PIT\_Type \*base, pit\_chnl\_t channel, uint32\_t count)  
Sets the timer period in units of count.
- static uint32\_t [PIT\\_GetCurrentTimerCount](#) (PIT\_Type \*base, pit\_chnl\_t channel)  
Reads the current timer counting value.

## Timer Start and Stop

- static void [PIT\\_StartTimer](#) (PIT\_Type \*base, pit\_chnl\_t channel)  
Starts the timer counting.
- static void [PIT\\_StopTimer](#) (PIT\_Type \*base, pit\_chnl\_t channel)  
Stops the timer counting.

## 34.4 Data Structure Documentation

### 34.4.1 struct pit\_config\_t

This structure holds the configuration settings for the PIT peripheral. To initialize this structure to reasonable defaults, call the [PIT\\_GetDefaultConfig\(\)](#) function and pass a pointer to your config structure instance.

The configuration structure can be made constant so it resides in flash.

## Data Fields

- bool `enableRunInDebug`  
*true: Timers run in debug mode; false: Timers stop in debug mode*

## 34.5 Enumeration Type Documentation

### 34.5.1 enum pit\_chnl\_t

Note

Actual number of available channels is SoC dependent

Enumerator

- kPIT\_Chnl\_0*** PIT channel number 0.  
***kPIT\_Chnl\_1*** PIT channel number 1.  
***kPIT\_Chnl\_2*** PIT channel number 2.  
***kPIT\_Chnl\_3*** PIT channel number 3.

### 34.5.2 enum pit\_interrupt\_enable\_t

Enumerator

- kPIT\_TimerInterruptEnable*** Timer interrupt enable.

### 34.5.3 enum pit\_status\_flags\_t

Enumerator

- kPIT\_TimerFlag*** Timer flag.

## 34.6 Function Documentation

### 34.6.1 void PIT\_Init ( **PIT\_Type** \* *base*, const pit\_config\_t \* *config* )

Note

This API should be called at the beginning of the application using the PIT driver.

Parameters

<i>base</i>	PIT peripheral base address
<i>config</i>	Pointer to the user's PIT config structure

### 34.6.2 void PIT\_Deinit ( PIT\_Type \* *base* )

Parameters

<i>base</i>	PIT peripheral base address
-------------	-----------------------------

### 34.6.3 static void PIT\_GetDefaultConfig ( pit\_config\_t \* *config* ) [inline], [static]

The default values are as follows.

```
*     config->enableRunInDebug = false;
*
```

Parameters

<i>config</i>	Pointer to the configuration structure.
---------------	---

### 34.6.4 static void PIT\_SetTimerChainMode ( PIT\_Type \* *base*, pit\_chnl\_t *channel*, bool *enable* ) [inline], [static]

When a timer has a chain mode enabled, it only counts after the previous timer has expired. If the timer n-1 has counted down to 0, counter n decrements the value by one. Each timer is 32-bits, which allows the developers to chain timers together and form a longer timer (64-bits and larger). The first timer (timer 0) can't be chained to any other timer.

Parameters

<i>base</i>	PIT peripheral base address
-------------	-----------------------------

<i>channel</i>	Timer channel number which is chained with the previous timer
<i>enable</i>	Enable or disable chain. true: Current timer is chained with the previous timer. false: Timer doesn't chain with other timers.

### 34.6.5 static void PIT\_EnableInterrupts ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">pit_interrupt_enable_t</a>

### 34.6.6 static void PIT\_DisableInterrupts ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number
<i>mask</i>	The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">pit_interrupt_enable_t</a>

### 34.6.7 static **uint32\_t** PIT\_GetEnabledInterrupts ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel* ) [inline], [static]

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [pit\\_interrupt\\_enable\\_t](#)

34.6.8 **static uint32\_t PIT\_GetStatusFlags ( PIT\_Type \* *base*, pit\_chnl\_t *channel* )**  
[**inline**], [**static**]

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number

Returns

The status flags. This is the logical OR of members of the enumeration [pit\\_status\\_flags\\_t](#)

### 34.6.9 static void PIT\_ClearStatusFlags ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number
<i>mask</i>	The status flags to clear. This is a logical OR of members of the enumeration <a href="#">pit_status_flags_t</a>

### 34.6.10 static void PIT\_SetTimerPeriod ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel*, **uint32\_t** *count* ) [inline], [static]

Timers begin counting from the value set by this function until it reaches 0, then it generates an interrupt and load this register value again. Writing a new value to this register does not restart the timer. Instead, the value is loaded after the timer expires.

Note

Users can call the utility macros provided in `fsl_common.h` to convert to ticks.

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number

<i>count</i>	Timer period in units of ticks
--------------	--------------------------------

### 34.6.11 static uint32\_t PIT\_GetCurrentTimerCount ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel* ) [inline], [static]

This function returns the real-time timer counting value, in a range from 0 to a timer period.

Note

Users can call the utility macros provided in fsl\_common.h to convert ticks to usec or msec.

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number

Returns

Current timer counting value in ticks

### 34.6.12 static void PIT\_StartTimer ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel* ) [inline], [static]

After calling this function, timers load period value, count down to 0 and then load the respective start value again. Each time a timer reaches 0, it generates a trigger pulse and sets the timeout interrupt flag.

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number.

### 34.6.13 static void PIT\_StopTimer ( **PIT\_Type** \* *base*, **pit\_chnl\_t** *channel* ) [inline], [static]

This function stops every timer counting. Timers reload their periods respectively after the next time they call the PIT\_DRV\_StartTimer.

Parameters

<i>base</i>	PIT peripheral base address
<i>channel</i>	Timer channel number.

### 34.6.14 `uint64_t PIT_GetLifetimeTimerCount ( PIT_Type * base )`

The lifetime timer is a 64-bit timer which chains timer 0 and timer 1 together. Timer 0 and 1 are chained by calling the `PIT_SetTimerChainMode` before using this timer. The period of lifetime timer is equal to the "period of timer 0 \* period of timer 1". For the 64-bit value, the higher 32-bit has the value of timer 1, and the lower 32-bit has the value of timer 0.

Parameters

<i>base</i>	PIT peripheral base address
-------------	-----------------------------

Returns

Current lifetime timer value

# Chapter 35

## PMU: Power Management Unit

### 35.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Power Management Unit (PMU) module of MCUXpresso SDK devices. The power management unit (PMU) is designed to simplify the external power interface. The power system can be split into the input power sources and their characteristics, the integrated power transforming and controlling elements, and the final load interconnection and requirements. By using the internal LDO regulators, the number of external supplies is greatly reduced.

The PMU driver provides the APIs to adjust the work condition of each regulator, and can gate the power of some modules.

### Enumerations

- enum {  
    kPMU\_1P1RegulatorOutputOK = (1U << 0U),  
    kPMU\_1P1BrownoutOnOutput = (1U << 1U),  
    kPMU\_3P0RegulatorOutputOK = (1U << 2U),  
    kPMU\_3P0BrownoutOnOutput = (1U << 3U),  
    kPMU\_2P5RegulatorOutputOK = (1U << 4U),  
    kPMU\_2P5BrownoutOnOutput = (1U << 5U) }  
        *PMU Status flags.*
- enum pmu\_1p1\_weak\_reference\_source\_t {  
    kPMU\_1P1WeakReferenceSourceAlt0 = 0U,  
    kPMU\_1P1WeakReferenceSourceAlt1 = 1U }  
        *The source for the reference voltage of the weak 1P1 regulator.*
- enum pmu\_3p0\_vbus\_voltage\_source\_t {  
    kPMU\_3P0VBusVoltageSourceAlt0 = 0U,  
    kPMU\_3P0VBusVoltageSourceAlt1 = 1U }  
        *Input voltage source for LDO\_3P0 from USB VBus.*
- enum pmu\_core\_reg\_voltage\_ramp\_rate\_t {  
    kPMU\_CoreRegVoltageRampRateFast = 0U,  
    kPMU\_CoreRegVoltageRampRateMediumFast = 1U,  
    kPMU\_CoreRegVoltageRampRateMediumSlow = 2U,  
    kPMU\_CoreRegVoltageRampRateSlow = 0U }  
        *Regulator voltage ramp rate.*
- enum pmu\_power\_bandgap\_t {  
    kPMU\_NormalPowerBandgap = 0U,  
    kPMU\_LowPowerBandgap = 1U }  
        *Bandgap select.*

## Driver version

- #define **FSL\_PMU\_DRIVER\_VERSION** (MAKE\_VERSION(2, 1, 1))  
*PMU driver version.*

## Status.

- uint32\_t **PMU\_GetStatusFlags** (PMU\_Type \*base)  
*Get PMU status flags.*

## 1P1 Regular

- static void **PMU\_1P1SetWeakReferenceSource** (PMU\_Type \*base, pmu\_1p1\_weak\_reference\_source\_t option)  
*Selects the source for the reference voltage of the weak 1P1 regulator.*
- static void **PMU\_1P1EnableWeakRegulator** (PMU\_Type \*base, bool enable)  
*Enables the weak 1P1 regulator.*
- static void **PMU\_1P1SetRegulatorOutputVoltage** (PMU\_Type \*base, uint32\_t value)  
*Adjust the 1P1 regulator output voltage.*
- static void **PMU\_1P1SetBrownoutOffsetVoltage** (PMU\_Type \*base, uint32\_t value)  
*Adjust the 1P1 regulator brownout offset voltage.*
- static void **PMU\_1P1EnablePullDown** (PMU\_Type \*base, bool enable)  
*Enable the pull-down circuitry in the regulator.*
- static void **PMU\_1P1EnableCurrentLimit** (PMU\_Type \*base, bool enable)  
*Enable the current-limit circuitry in the regulator.*
- static void **PMU\_1P1EnableBrownout** (PMU\_Type \*base, bool enable)  
*Enable the brownout circuitry in the regulator.*
- static void **PMU\_1P1EnableOutput** (PMU\_Type \*base, bool enable)  
*Enable the regulator output.*

## 3P0 Regular

- static void **PMU\_3P0SetRegulatorOutputVoltage** (PMU\_Type \*base, uint32\_t value)  
*Adjust the 3P0 regulator output voltage.*
- static void **PMU\_3P0SetVBusVoltageSource** (PMU\_Type \*base, pmu\_3p0\_vbus\_voltage\_source\_t option)  
*Select input voltage source for LDO\_3P0.*
- static void **PMU\_3P0SetBrownoutOffsetVoltage** (PMU\_Type \*base, uint32\_t value)  
*Adjust the 3P0 regulator brownout offset voltage.*
- static void **PMU\_3P0EnableCurrentLimit** (PMU\_Type \*base, bool enable)  
*Enable the current-limit circuitry in the 3P0 regulator.*
- static void **PMU\_3P0EnableBrownout** (PMU\_Type \*base, bool enable)  
*Enable the brownout circuitry in the 3P0 regulator.*
- static void **PMU\_3P0EnableOutput** (PMU\_Type \*base, bool enable)  
*Enable the 3P0 regulator output.*

## 2P5 Regulator

- static void **PMU\_2P5EnableWeakRegulator** (PMU\_Type \*base, bool enable)  
*Enables the weak 2P5 regulator.*
- static void **PMU\_2P5SetRegulatorOutputVoltage** (PMU\_Type \*base, uint32\_t value)

- static void **PMU\_2P5SetBrownoutOffsetVoltage** (PMU\_Type \*base, uint32\_t value)
 

*Adjust the 1P1 regulator output voltage.*
- static void **PMU\_2P5EnablePullDown** (PMU\_Type \*base, bool enable)
 

*Adjust the 2P5 regulator brownout offset voltage.*
- static void **PMU\_2P1EnablePullDown** (PMU\_Type \*base, bool enable)
 

*Enable the pull-down circuitry in the 2P5 regulator.*
- static void **PMU\_2P5EnableCurrentLimit** (PMU\_Type \*base, bool enable)
 

*Enable the pull-down circuitry in the 2P5 regulator.*
- static void **PMU\_2P5nableBrownout** (PMU\_Type \*base, bool enable)
 

*Enable the current-limit circuitry in the 2P5 regulator.*
- static void **PMU\_2P5EnableOutput** (PMU\_Type \*base, bool enable)
 

*Enable the brownout circuitry in the 2P5 regulator.*
- static void **PMU\_2P5EnableOutput** (PMU\_Type \*base, bool enable)
 

*Enable the 2P5 regulator output.*

## Core Regulator

- static void **PMU\_CoreEnableIncreaseGateDrive** (PMU\_Type \*base, bool enable)
 

*Increase the gate drive on power gating FETs.*
- static void **PMU\_CoreSetRegulatorVoltageRampRate** (PMU\_Type \*base, pmu\_core\_reg\_voltage\_ramp\_rate\_t option)
 

*Set the CORE regulator voltage ramp rate.*
- static void **PMU\_CoreSetSOCDomainVoltage** (PMU\_Type \*base, uint32\_t value)
 

*Define the target voltage for the SOC power domain.*
- static void **PMU\_CoreSetARMCoreDomainVoltage** (PMU\_Type \*base, uint32\_t value)
 

*Define the target voltage for the ARM Core power domain.*

## 35.2 Macro Definition Documentation

### 35.2.1 #define FSL\_PMU\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))

Version 2.1.1.

## 35.3 Enumeration Type Documentation

### 35.3.1 anonymous enum

Enumerator

**kPMU\_1P1RegulatorOutputOK** Status bit that signals when the 1p1 regulator output is ok. 1 = regulator output > brownout target.

**kPMU\_1P1BrownoutOnOutput** Status bit that signals when a 1p1 brownout is detected on the regulator output.

**kPMU\_3P0RegulatorOutputOK** Status bit that signals when the 3p0 regulator output is ok. 1 = regulator output > brownout target.

**kPMU\_3P0BrownoutOnOutput** Status bit that signals when a 3p0 brownout is detected on the regulator output.

**kPMU\_2P5RegulatorOutputOK** Status bit that signals when the 2p5 regulator output is ok. 1 = regulator output > brownout target.

***kPMU\_2P5BrownoutOnOutput*** Status bit that signals when a 2p5 brownout is detected on the regulator output.

### 35.3.2 enum pmu\_1p1\_weak\_reference\_source\_t

Enumerator

***kPMU\_1P1WeakReferenceSourceAlt0*** Weak-linreg output tracks low-power-bandgap voltage.

***kPMU\_1P1WeakReferenceSourceAlt1*** Weak-linreg output tracks VDD\_SOC\_CAP voltage.

### 35.3.3 enum pmu\_3p0\_vbus\_voltage\_source\_t

Enumerator

***kPMU\_3P0VBusVoltageSourceAlt0*** USB\_OTG1\_VBUS - Utilize VBUS OTG1 for power.

***kPMU\_3P0VBusVoltageSourceAlt1*** USB\_OTG2\_VBUS - Utilize VBUS OTG2 for power.

### 35.3.4 enum pmu\_core\_reg\_voltage\_ramp\_rate\_t

Enumerator

***kPMU\_CoreRegVoltageRampRateFast*** Fast.

***kPMU\_CoreRegVoltageRampRateMediumFast*** Medium Fast.

***kPMU\_CoreRegVoltageRampRateMediumSlow*** Medium Slow.

***kPMU\_CoreRegVoltageRampRateSlow*** Slow.

### 35.3.5 enum pmu\_power\_bandgap\_t

Enumerator

***kPMU\_NormalPowerBandgap*** Normal power bandgap.

***kPMU\_LowPowerBandgap*** Low power bandgap.

## 35.4 Function Documentation

### 35.4.1 uint32\_t PMU\_GetStatusFlags ( PMU\_Type \* base )

Parameters

<i>base</i>	PMU peripheral base address.
-------------	------------------------------

Returns

PMU status flags. It indicate if regulator output of 1P1,3P0 and 2P5 is ok and brownout output of 1P1,3P0 and 2P5 is detected.

### 35.4.2 static void PMU\_1P1SetWeakReferenceSource ( PMU\_Type \* *base*, pmu\_1p1\_weak\_reference\_source\_t *option* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>option</i>	The option for reference voltage source, see to <a href="#">pmu_1p1_weak_reference_source_t</a> .

### 35.4.3 static void PMU\_1P1EnableWeakRegulator ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

This regulator can be used when the main 1P1 regulator is disabled, under low-power conditions.

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.4 static void PMU\_1P1SetRegulatorOutputVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Each LSB is worth 25mV. Programming examples are detailed below. Other output target voltages may be interpolated from these examples. Choices must be in this range:

- 0x1b(1.375V) >= output\_trg >= 0x04(0.8V)
- 0x04 : 0.8V
- 0x10 : 1.1V (typical)
- 0x1b : 1.375V NOTE: There may be reduced chip functionality or reliability at the extremes of the programming range.

Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for the output.

### 35.4.5 static void PMU\_1P1SetBrownoutOffsetVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Control bits to adjust the regulator brownout offset voltage in 25mV steps. The reset brown-offset is 175mV below the programmed target code. Brownout target = OUTPUT\_TRG - BO\_OFFSET. Some steps may be irrelevant because of input supply limitations or load operation.

Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for the brownout offset. The available range is in 3-bit.

### 35.4.6 static void PMU\_1P1EnablePullDown ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.7 static void PMU\_1P1EnableCurrentLimit ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.8 static void PMU\_1P1EnableBrownout ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.9 static void PMU\_1P1EnableOutput ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.10 static void PMU\_3P0SetRegulatorOutputVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Each LSB is worth 25mV. Programming examples are detailed below. Other output target voltages may be interpolated from these examples. Choices must be in this range:

- 0x00(2.625V) >= output\_trg >= 0x1f(3.4V)
- 0x00 : 2.625V
- 0x0f : 3.0V (typical)
- 0x1f : 3.4V

Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for the output.

### 35.4.11 static void PMU\_3P0SetVBUSVoltageSource ( PMU\_Type \* *base*, pmu\_3p0\_vbus\_voltage\_source\_t *option* ) [inline], [static]

Select input voltage source for LDO\_3P0 from either USB\_OTG1\_VBUS or USB\_OTG2\_VBUS. If only one of the two VBUS voltages is present, it is automatically selected.

Parameters

<i>base</i>	PMU peripheral base address.
<i>option</i>	User-defined input voltage source for LDO_3P0.

### 35.4.12 static void PMU\_3P0SetBrownoutOffsetVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Control bits to adjust the 3P0 regulator brownout offset voltage in 25mV steps. The reset brown-offset is 175mV below the programmed target code. Brownout target = OUTPUT\_TRG - BO\_OFFSET. Some steps may be irrelevant because of input supply limitations or load operation.

Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for the brownout offset. The available range is in 3-bit.

### 35.4.13 static void PMU\_3P0EnableCurrentLimit ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.14 static void PMU\_3P0EnableBrownout ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.15 static void PMU\_3P0EnableOutput ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.16 static void PMU\_2P5EnableWeakRegulator ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]

This low power regulator is used when the main 2P5 regulator is disabled to keep the 2.5V output roughly at 2.5V. Scales directly with the value of VDDHIGH\_IN.

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

### 35.4.17 static void PMU\_2P5SetRegulatorOutputVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Each LSB is worth 25mV. Programming examples are detailed below. Other output target voltages may be interpolated from these examples. Choices must be in this range:

- 0x00(2.1V) >= output\_trg >= 0x1f(2.875V)
- 0x00 : 2.1V
- 0x10 : 2.5V (typical)
- 0x1f : 2.875V NOTE: There may be reduced chip functionality or reliability at the extremes of the programming range.

Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for the output.

### 35.4.18 static void PMU\_2P5SetBrownoutOffsetVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Adjust the regulator brownout offset voltage in 25mV steps. The reset brown-offset is 175mV below the programmed target code. Brownout target = OUTPUT\_TRG - BO\_OFFSET. Some steps may be irrelevant because of input supply limitations or load operation.

Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for the brownout offset. The available range is in 3-bit.

**35.4.19 static void PMU\_2P5EnablePullDown ( PMU\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

**35.4.20 static void PMU\_2P1EnablePullDown ( PMU\_Type \* *base*, bool *enable* )  
[inline], [static]**

**Deprecated** Do not use this function. It has been superceded by [PMU\\_2P5EnablePullDown](#).

**35.4.21 static void PMU\_2P5EnableCurrentLimit ( PMU\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

**35.4.22 static void PMU\_2P5nableBrownout ( PMU\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

---

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

**35.4.23 static void PMU\_2P5EnableOutput ( PMU\_Type \* *base*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

**35.4.24 static void PMU\_CoreEnableIncreaseGateDrive ( PMU\_Type \* *base*, bool *enable* ) [inline], [static]**

If set, increases the gate drive on power gating FETs to reduce leakage in the off state. Care must be taken to apply this bit only when the input supply voltage to the power FET is less than 1.1V. NOTE: This bit should only be used in low-power modes where the external input supply voltage is nominally 0.9V.

Parameters

<i>base</i>	PMU peripheral base address.
<i>enable</i>	Enable the feature or not.

**35.4.25 static void PMU\_CoreSetRegulatorVoltageRampRate ( PMU\_Type \* *base*, pmu\_core\_reg\_voltage\_ramp\_rate\_t *option* ) [inline], [static]**

Parameters

<i>base</i>	PMU peripheral base address.
<i>option</i>	User-defined option for voltage ramp rate, see to <a href="#">pmu_core_reg_voltage_ramp_rate_t</a> .

### 35.4.26 static void PMU\_CoreSetSOCDomainVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Define the target voltage for the SOC power domain. Single-bit increments reflect 25mV core voltage steps. Some steps may not be relevant because of input supply limitations or load operation.

- 0x00 : Power gated off.
- 0x01 : Target core voltage = 0.725V
- 0x02 : Target core voltage = 0.750V
- ...
- 0x10 : Target core voltage = 1.100V
- ...
- 0x1e : Target core voltage = 1.450V
- 0x1F : Power FET switched full on. No regulation. NOTE: This register is capable of programming an over-voltage condition on the device. Consult the datasheet Operating Ranges table for the allowed voltages.

Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for target voltage. 5-bit available

### 35.4.27 static void PMU\_CoreSetARMCoreDomainVoltage ( PMU\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Define the target voltage for the ARM Core power domain. Single-bit increments reflect 25mV core voltage steps. Some steps may not be relevant because of input supply limitations or load operation.

- 0x00 : Power gated off.
- 0x01 : Target core voltage = 0.725V
- 0x02 : Target core voltage = 0.750V
- ...
- 0x10 : Target core voltage = 1.100V
- ...
- 0x1e : Target core voltage = 1.450V
- 0x1F : Power FET switched full on. No regulation. NOTE: This register is capable of programming an over-voltage condition on the device. Consult the datasheet Operating Ranges table for the allowed voltages.

## Parameters

<i>base</i>	PMU peripheral base address.
<i>value</i>	Setting value for target voltage. 5-bit available

# Chapter 36

## PWM: Pulse Width Modulator

### 36.1 Overview

The MCUXpresso SDK provides a driver for the Pulse Width Modulator (PWM) of MCUXpresso SDK devices.

### 36.2 PWM: Pulse Width Modulator

#### 36.2.1 Initialization and deinitialization

The function [PWM\\_Init\(\)](#) initializes the PWM sub module with specified configurations, the function [PWM\\_GetDefaultConfig\(\)](#) could help to get the default configurations. The initialization function configures the sub module for the requested register update mode for registers with buffers. It also sets up the sub module operation in debug and wait modes.

#### 36.2.2 PWM Operations

The function [PWM\\_SetupPwm\(\)](#) sets up PWM channels for PWM output, the function can set up PWM signal properties for multiple channels. The PWM has 2 channels: A and B. Each channel has its own duty cycle and level-mode specified, however the same PWM period and PWM mode is applied to all channels requesting PWM output. The signal duty cycle is provided as a percentage of the PWM period, its value should be between 0 and 100; 0=inactive signal(0% duty cycle) and 100=always active signal (100% duty cycle). The function also sets up the channel dead time value which is used when the user selects complementary mode of operation.

The function [PWM\\_UpdatePwmDutycycle\(\)](#) updates the PWM signal duty cycle of a particular PWM channel.

#### 36.2.3 Input capture operations

The function [PWM\\_SetupInputCapture\(\)](#) sets up a PWM channel for input capture. The user can specify the capture edge and the mode; one-shot capture or free-running capture.

#### 36.2.4 Fault operation

The function [PWM\\_SetupFault\(\)](#) sets up the properties for each fault.

### 36.2.5 PWM Start and Stop operations

The function [PWM\\_StartTimer\(\)](#) can be used to start one or multiple sub modules. The function [PWM\\_StopTimer\(\)](#) can be used to stop one or multiple sub modules.

### 36.2.6 Status

Provide functions to get and clear the PWM status.

### 36.2.7 Interrupt

Provide functions to enable/disable PWM interrupts and get current enabled interrupts.

## 36.3 Register Update

Some of the PWM registers have buffers, the driver support various methods to update these registers with the content of the register buffer. The update mechanism for register with buffers can be specified through the following fields available in the configuration structure. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pwmThe user can select one of the reload options provided in enumeration [pwm\\_register\\_reload\\_t](#). When using immediate reload, the reloadFrequency field is not used.

The driver initialization function sets up the appropriate bits in the PWM module based on the register update options selected.

The below function should be used to initiate a register reload. The example shows register reload initiated on PWM sub modules 0, 1, and 2. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pwm

## 36.4 Typical use case

### 36.4.1 PWM output

Output PWM signal on 3 PWM sub module with different dutycycles. Periodically update the PWM signal duty cycle. Each sub module runs in Complementary output mode with PWM A used to generate the complementary PWM pair. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pwm

## Data Structures

- struct [pwm\\_signal\\_param\\_t](#)  
*Structure for the user to define the PWM signal characteristics. [More...](#)*
- struct [pwm\\_config\\_t](#)  
*PWM config structure. [More...](#)*
- struct [pwm\\_fault\\_input\\_filter\\_param\\_t](#)

*Structure for the user to configure the fault input filter. [More...](#)*

- struct `pwm_fault_param_t`

*Structure is used to hold the parameters to configure a PWM fault. [More...](#)*

- struct `pwm_input_capture_param_t`

*Structure is used to hold parameters to configure the capture capability of a signal pin. [More...](#)*

## Macros

- #define `PWM_SUBMODULE_SWCONTROL_WIDTH` 2

*Number of bits per submodule for software output control.*

- #define `PWM_SUBMODULE_CHANNEL` 2

*Because setting the pwm duty cycle doesn't support PWMX, getting the pwm duty cycle also doesn't support PWMX.*

## Enumerations

- enum `pwm_submodule_t` {

```
kPWM_Module_0 = 0U,
kPWM_Module_1,
kPWM_Module_2,
kPWM_Module_3 }
```

*List of PWM submodules.*

- enum `pwm_channels_t`

*List of PWM channels in each module.*

- enum `pwm_value_register_t` {

```
kPWM_ValueRegister_0 = 0U,
kPWM_ValueRegister_1,
kPWM_ValueRegister_2,
kPWM_ValueRegister_3,
kPWM_ValueRegister_4,
kPWM_ValueRegister_5 }
```

*List of PWM value registers.*

- enum `_pwm_value_register_mask` {

```
kPWM_ValueRegisterMask_0 = (1U << 0),
kPWM_ValueRegisterMask_1 = (1U << 1),
kPWM_ValueRegisterMask_2 = (1U << 2),
kPWM_ValueRegisterMask_3 = (1U << 3),
kPWM_ValueRegisterMask_4 = (1U << 4),
kPWM_ValueRegisterMask_5 = (1U << 5) }
```

*List of PWM value registers mask.*

- enum `pwm_clock_source_t` {

```
kPWM_BusClock = 0U,
kPWM_ExternalClock,
kPWM_Submodule0Clock }
```

*PWM clock source selection.*

- enum `pwm_clock_prescale_t` {

```
kPWM_Prescale_Divide_1 = 0U,  
kPWM_Prescale_Divide_2,  
kPWM_Prescale_Divide_4,  
kPWM_Prescale_Divide_8,  
kPWM_Prescale_Divide_16,  
kPWM_Prescale_Divide_32,  
kPWM_Prescale_Divide_64,  
kPWM_Prescale_Divide_128 }
```

*PWM prescaler factor selection for clock source.*

- enum `pwm_force_output_trigger_t` {  
  kPWM\_Force\_Local = 0U,  
  kPWM\_Force\_Master,  
  kPWM\_Force\_LocalReload,  
  kPWM\_Force\_MasterReload,  
  kPWM\_Force\_LocalSync,  
  kPWM\_Force\_MasterSync,  
  kPWM\_Force\_External,  
  kPWM\_Force\_ExternalSync }

*Options that can trigger a PWM FORCE\_OUT.*

- enum `pwm_output_state_t` {  
  kPWM\_HighState = 0,  
  kPWM\_LowState,  
  kPWM\_NormalState,  
  kPWM\_InvertState,  
  kPWM\_MaskState }

*PWM channel output status.*

- enum `pwm_init_source_t` {  
  kPWM\_Initialize\_LocalSync = 0U,  
  kPWM\_Initialize\_MasterReload,  
  kPWM\_Initialize\_MasterSync,  
  kPWM\_Initialize\_ExtSync }

*PWM counter initialization options.*

- enum `pwm_load_frequency_t` {

```
kPWM_LoadEveryOportunity = 0U,
kPWM_LoadEvery2Oportunity,
kPWM_LoadEvery3Oportunity,
kPWM_LoadEvery4Oportunity,
kPWM_LoadEvery5Oportunity,
kPWM_LoadEvery6Oportunity,
kPWM_LoadEvery7Oportunity,
kPWM_LoadEvery8Oportunity,
kPWM_LoadEvery9Oportunity,
kPWM_LoadEvery10Oportunity,
kPWM_LoadEvery11Oportunity,
kPWM_LoadEvery12Oportunity,
kPWM_LoadEvery13Oportunity,
kPWM_LoadEvery14Oportunity,
kPWM_LoadEvery15Oportunity,
kPWM_LoadEvery16Oportunity }
```

*PWM load frequency selection.*

- enum `pwm_fault_input_t` {
   
kPWM\_Fault\_0 = 0U,
   
kPWM\_Fault\_1,
   
kPWM\_Fault\_2,
   
kPWM\_Fault\_3 }

*List of PWM fault selections.*

- enum `pwm_fault_disable_t` {
   
kPWM\_FaultDisable\_0 = (1U << 0),
   
kPWM\_FaultDisable\_1 = (1U << 1),
   
kPWM\_FaultDisable\_2 = (1U << 2),
   
kPWM\_FaultDisable\_3 = (1U << 3) }

*List of PWM fault disable mapping selections.*

- enum `pwm_fault_channels_t`
  - List of PWM fault channels.*
- enum `pwm_input_capture_edge_t` {
   
kPWM\_Disable = 0U,
   
kPWM\_FallingEdge,
   
kPWM\_RisingEdge,
   
kPWM\_RiseAndFallEdge }

*PWM capture edge select.*

- enum `pwm_force_signal_t` {
   
kPWM\_UsePwm = 0U,
   
kPWM\_InvertedPwm,
   
kPWM\_SoftwareControl,
   
kPWM\_UseExternal }

*PWM output options when a FORCE\_OUT signal is asserted.*

- enum `pwm_chnl_pair_operation_t` {
   
kPWM\_Independent = 0U,
   
kPWM\_ComplementaryPwmA,

`kPWM_ComplementaryPwmB }`

*Options available for the PWM A & B pair operation.*

- enum `pwm_register_reload_t` {
   
`kPWM_ReloadImmediate` = 0U,
   
`kPWM_ReloadPwmHalfCycle`,
   
`kPWM_ReloadPwmFullCycle`,
   
`kPWM_ReloadPwmHalfAndFullCycle` }

*Options available on how to load the buffered-registers with new values.*

- enum `pwm_fault_recovery_mode_t` {
   
`kPWM_NoRecovery` = 0U,
   
`kPWM_RecoverHalfCycle`,
   
`kPWM_RecoverFullCycle`,
   
`kPWM_RecoverHalfAndFullCycle` }

*Options available on how to re-enable the PWM output when recovering from a fault.*

- enum `pwm_interrupt_enable_t` {
   
`kPWM_CompareVal0InterruptEnable` = (1U << 0),
   
`kPWM_CompareVal1InterruptEnable` = (1U << 1),
   
`kPWM_CompareVal2InterruptEnable` = (1U << 2),
   
`kPWM_CompareVal3InterruptEnable` = (1U << 3),
   
`kPWM_CompareVal4InterruptEnable` = (1U << 4),
   
`kPWM_CompareVal5InterruptEnable` = (1U << 5),
   
`kPWM_CaptureX0InterruptEnable` = (1U << 6),
   
`kPWM_CaptureX1InterruptEnable` = (1U << 7),
   
`kPWM_CaptureB0InterruptEnable` = (1U << 8),
   
`kPWM_CaptureB1InterruptEnable` = (1U << 9),
   
`kPWM_CaptureA0InterruptEnable` = (1U << 10),
   
`kPWM_CaptureA1InterruptEnable` = (1U << 11),
   
`kPWM_ReloadInterruptEnable` = (1U << 12),
   
`kPWM_ReloadErrorInterruptEnable` = (1U << 13),
   
`kPWM_Fault0InterruptEnable` = (1U << 16),
   
`kPWM_Fault1InterruptEnable` = (1U << 17),
   
`kPWM_Fault2InterruptEnable` = (1U << 18),
   
`kPWM_Fault3InterruptEnable` = (1U << 19) }

*List of PWM interrupt options.*

- enum `pwm_status_flags_t` {

```

kPWM_CompareVal0Flag = (1U << 0),
kPWM_CompareVal1Flag = (1U << 1),
kPWM_CompareVal2Flag = (1U << 2),
kPWM_CompareVal3Flag = (1U << 3),
kPWM_CompareVal4Flag = (1U << 4),
kPWM_CompareVal5Flag = (1U << 5),
kPWM_CaptureX0Flag = (1U << 6),
kPWM_CaptureX1Flag = (1U << 7),
kPWM_CaptureB0Flag = (1U << 8),
kPWM_CaptureB1Flag = (1U << 9),
kPWM_CaptureA0Flag = (1U << 10),
kPWM_CaptureA1Flag = (1U << 11),
kPWM_ReloadFlag = (1U << 12),
kPWM_ReloadErrorFlag = (1U << 13),
kPWM_RegUpdatedFlag = (1U << 14),
kPWM_Fault0Flag = (1U << 16),
kPWM_Fault1Flag = (1U << 17),
kPWM_Fault2Flag = (1U << 18),
kPWM_Fault3Flag = (1U << 19) }
```

*List of PWM status flags.*

- enum `pwm_dma_enable_t` {
 

```

kPWM_CaptureX0DMAEnable = (1U << 0),
kPWM_CaptureX1DMAEnable = (1U << 1),
kPWM_CaptureB0DMAEnable = (1U << 2),
kPWM_CaptureB1DMAEnable = (1U << 3),
kPWM_CaptureA0DMAEnable = (1U << 4),
kPWM_CaptureA1DMAEnable = (1U << 5) }
```

*List of PWM DMA options.*

- enum `pwm_dma_source_select_t` {
 

```

kPWM_DMAResetDisable = 0U,
kPWM_DMAWatermarksEnable,
kPWM_DMALocalSync,
kPWM_DMALocalReload } }
```

*List of PWM capture DMA enable source select.*

- enum `pwm_watermark_control_t` {
 

```

kPWM_FIFOWatermarksOR = 0U,
kPWM_FIFOWatermarksAND } }
```

*PWM FIFO Watermark AND Control.*

- enum `pwm_mode_t` {
 

```

kPWM_SignedCenterAligned = 0U,
kPWM_CenterAligned,
kPWM_SignedEdgeAligned,
kPWM_EdgeAligned } }
```

*PWM operation mode.*

- enum `pwm_level_select_t` {
 

```

kPWM_HighTrue = 0U,
```

- `kPWM_LowTrue }`  
*PWM output pulse mode, high-true or low-true.*
- enum `pwm_fault_state_t` {
 `kPWM_PwmFaultState0,`  
`kPWM_PwmFaultState1,`  
`kPWM_PwmFaultState2,`  
`kPWM_PwmFaultState3 }`  
*PWM output fault status.*
- enum `pwm_reload_source_select_t` {
 `kPWM_LocalReload = 0U,`  
`kPWM_MasterReload }`  
*PWM reload source select.*
- enum `pwm_fault_clear_t` {
 `kPWM_Automatic = 0U,`  
`kPWM_ManualNormal,`  
`kPWM_ManualSafety }`  
*PWM fault clearing options.*
- enum `pwm_module_control_t` {
 `kPWM_Control_Module_0 = (1U << 0),`  
`kPWM_Control_Module_1 = (1U << 1),`  
`kPWM_Control_Module_2 = (1U << 2),`  
`kPWM_Control_Module_3 = (1U << 3) }`  
*Options for submodule master control operation.*

## Functions

- void `PWM_SetupInputCapture` (`PWM_Type *base, pwm_submodule_t subModule, pwm_channels_t pwmChannel, const pwm_input_capture_param_t *inputCaptureParams)`  
*Sets up the PWM input capture.*
- void `PWM_SetupFaultInputFilter` (`PWM_Type *base, const pwm_fault_input_filter_param_t *faultInputFilterParams)`  
*Sets up the PWM fault input filter.*
- void `PWM_SetupFaults` (`PWM_Type *base, pwm_fault_input_t faultNum, const pwm_fault_param_t *faultParams)`  
*Sets up the PWM fault protection.*
- void `PWM_FaultDefaultConfig` (`pwm_fault_param_t *config)`  
*Fill in the PWM fault config struct with the default settings.*
- void `PWM_SetupForceSignal` (`PWM_Type *base, pwm_submodule_t subModule, pwm_channels_t pwmChannel, pwm_force_signal_t mode)`  
*Selects the signal to output on a PWM pin when a FORCE\_OUT signal is asserted.*
- static void `PWM_SetVALxValue` (`PWM_Type *base, pwm_submodule_t subModule, pwm_value_register_t valueRegister, uint16_t value)`  
*Set the PWM VALx registers.*
- static uint16\_t `PWM_GetVALxValue` (`PWM_Type *base, pwm_submodule_t subModule, pwm_value_register_t valueRegister)`  
*Get the PWM VALx registers.*
- static void `PWM_OutputTriggerEnable` (`PWM_Type *base, pwm_submodule_t subModule, pwm_value_register_t valueRegister, bool activate)`

- static void `PWM_ActivateOutputTrigger` (PWM\_Type \*base, `pwm_submodule_t` subModule, `uint16_t` valueRegisterMask)
  - Enables or disables the PWM output trigger.*
- static void `PWM_DeactivateOutputTrigger` (PWM\_Type \*base, `pwm_submodule_t` subModule, `uint16_t` valueRegisterMask)
  - Enables the PWM output trigger.*
- static void `PWM_SetupSwCtrlOut` (PWM\_Type \*base, `pwm_submodule_t` subModule, `pwm_channels_t` pwmChannel, bool value)
  - Disables the PWM output trigger.*
- static void `PWM_SetPwmLdok` (PWM\_Type \*base, `uint8_t` subModulesToUpdate, bool value)
  - Sets the software control output for a pin to high or low.*
- static void `PWM_SetPwmFaultState` (PWM\_Type \*base, `pwm_submodule_t` subModule, `pwm_channels_t` pwmChannel, `pwm_fault_state_t` faultState)
  - Sets or clears the PWM LDOK bit on a single or multiple submodules.*
- static void `PWM_SetFaultDisableMap` (PWM\_Type \*base, `pwm_submodule_t` subModule, `pwm_channels_t` pwmChannel, `pwm_fault_channels_t` pwm\_fault\_channels, `uint16_t` value)
  - Set PWM fault disable mapping.*
- static void `PWM_OutputEnable` (PWM\_Type \*base, `pwm_channels_t` pwmChannel, `pwm_submodule_t` subModule)
  - Set PWM output enable.*
- static void `PWM_OutputDisable` (PWM\_Type \*base, `pwm_channels_t` pwmChannel, `pwm_submodule_t` subModule)
  - Set PWM output disable.*
- `uint8_t PWM_GetPwmChannelState` (PWM\_Type \*base, `pwm_submodule_t` subModule, `pwm_channels_t` pwmChannel)
  - Get the dutycycle value.*
- `status_t PWM_SetOutputToIdle` (PWM\_Type \*base, `pwm_channels_t` pwmChannel, `pwm_submodule_t` subModule, bool idleStatus)
  - Set PWM output in idle status (high or low).*
- void `PWM_SetClockMode` (PWM\_Type \*base, `pwm_submodule_t` subModule, `pwm_clock_prescale_t` prescaler)
  - Set the pwm submodule prescaler.*
- void `PWM_SetPwmForceOutputToZero` (PWM\_Type \*base, `pwm_submodule_t` subModule, `pwm_channels_t` pwmChannel, bool forcetozero)
  - This function enables-disables the forcing of the output of a given eFlexPwm channel to logic 0.*
- void `PWM_SetChannelOutput` (PWM\_Type \*base, `pwm_submodule_t` subModule, `pwm_channels_t` pwmChannel, `pwm_output_state_t` outputstate)
  - This function set the output state of the PWM pin as requested for the current cycle.*

## Driver version

- #define `FSL_PWM_DRIVER_VERSION` (`MAKE_VERSION(2, 6, 1)`)  
*Version 2.6.1.*

## Initialization and deinitialization

- `status_t PWM_Init` (PWM\_Type \*base, `pwm_submodule_t` subModule, const `pwm_config_t` \*config)

- Ungates the PWM submodule clock and configures the peripheral for basic operation.
- void **PWM\_Deinit** (PWM\_Type \*base, **pwm\_submodule\_t** subModule)  
Gate the PWM submodule clock.
- void **PWM\_GetDefaultConfig** (**pwm\_config\_t** \*config)  
Fill in the PWM config struct with the default settings.

## Module PWM output

- **status\_t PWM\_SetupPwm** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, const **pwm\_signal\_param\_t** \*chnlParams, uint8\_t numOfChnls, **pwm\_mode\_t** mode, uint32\_t pwmFreq\_Hz, uint32\_t srcClock\_Hz)  
Sets up the PWM signals for a PWM submodule.
- **status\_t PWM\_SetupPwmPhaseShift** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, **pwm\_channels\_t** pwmChannel, uint32\_t pwmFreq\_Hz, uint32\_t srcClock\_Hz, uint8\_t shiftvalue, bool doSync)  
Set PWM phase shift for PWM channel running on channel PWM\_A, PWM\_B which with 50% duty cycle.
- void **PWM\_UpdatePwmDutycycle** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, **pwm\_channels\_t** pwmSignal, **pwm\_mode\_t** currPwmMode, uint8\_t dutyCyclePercent)  
Updates the PWM signal's dutycycle.
- void **PWM\_UpdatePwmDutycycleHighAccuracy** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, **pwm\_channels\_t** pwmSignal, **pwm\_mode\_t** currPwmMode, uint16\_t dutyCycle)  
Updates the PWM signal's dutycycle with 16-bit accuracy.

## Interrupts Interface

- void **PWM\_EnableInterrupts** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, uint32\_t mask)  
Enables the selected PWM interrupts.
- void **PWM\_DisableInterrupts** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, uint32\_t mask)  
Disables the selected PWM interrupts.
- uint32\_t **PWM\_GetEnabledInterrupts** (PWM\_Type \*base, **pwm\_submodule\_t** subModule)  
Gets the enabled PWM interrupts.

## DMA Interface

- static void **PWM\_DMAFIFOWatermarkControl** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, **pwm\_watermark\_control\_t** pwm\_watermark\_control)  
Capture DMA Enable Source Select.
- static void **PWM\_DMACaptureSourceSelect** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, **pwm\_dma\_source\_select\_t** pwm\_dma\_source\_select)  
Capture DMA Enable Source Select.
- static void **PWM\_EnableDMACapture** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, uint16\_t mask, bool activate)  
Enables or disables the selected PWM DMA Capture read request.
- static void **PWM\_EnableDMAWrite** (PWM\_Type \*base, **pwm\_submodule\_t** subModule, bool activate)  
Enables or disables the PWM DMA write request.

## Status Interface

- uint32\_t **PWM\_GetStatusFlags** (PWM\_Type \*base, **pwm\_submodule\_t** subModule)

- Gets the PWM status flags.
- void [PWM\\_ClearStatusFlags](#) (PWM\_Type \*base, [pwm\\_submodule\\_t](#) subModule, uint32\_t mask)  
*Clears the PWM status flags.*

## Timer Start and Stop

- static void [PWM\\_StartTimer](#) (PWM\_Type \*base, uint8\_t subModulesToStart)  
*Starts the PWM counter for a single or multiple submodules.*
- static void [PWM\\_StopTimer](#) (PWM\_Type \*base, uint8\_t subModulesToStop)  
*Stops the PWM counter for a single or multiple submodules.*

## 36.5 Data Structure Documentation

### 36.5.1 struct pwm\_signal\_param\_t

#### Data Fields

- [pwm\\_channels\\_t](#) [pwmChannel](#)  
*PWM channel being configured; PWM A or PWM B.*
- uint8\_t [dutyCyclePercent](#)  
*PWM pulse width, value should be between 0 to 100 0=inactive signal(0% duty cycle)...*
- [pwm\\_level\\_select\\_t](#) [level](#)  
*PWM output active level select.*
- uint16\_t [deadtimeValue](#)  
*The deadtime value; only used if channel pair is operating in complementary mode.*
- [pwm\\_fault\\_state\\_t](#) [faultState](#)  
*PWM output fault status.*
- bool [pwmchannelenable](#)  
*Enable PWM output.*

#### Field Documentation

##### (1) uint8\_t [pwm\\_signal\\_param\\_t::dutyCyclePercent](#)

100=always active signal (100% duty cycle)

### 36.5.2 struct pwm\_config\_t

This structure holds the configuration settings for the PWM peripheral. To initialize this structure to reasonable defaults, call the [PWM\\_GetDefaultConfig\(\)](#) function and pass a pointer to your config structure instance.

The config struct can be made const so it resides in flash

#### Data Fields

- bool [enableDebugMode](#)

*true: PWM continues to run in debug mode; false: PWM is paused in debug mode*

- [pwm\\_init\\_source\\_t initializationControl](#)
  - Option to initialize the counter.*
- [pwm\\_clock\\_source\\_t clockSource](#)
  - Clock source for the counter.*
- [pwm\\_clock\\_prescale\\_t prescale](#)
  - Pre-scaler to divide down the clock.*
- [pwm\\_chnl\\_pair\\_operation\\_t pairOperation](#)
  - Channel pair in independent or complementary mode.*
- [pwm\\_register\\_reload\\_t reloadLogic](#)
  - PWM Reload logic setup.*
- [pwm\\_reload\\_source\\_select\\_t reloadSelect](#)
  - Reload source select.*
- [pwm\\_load\\_frequency\\_t reloadFrequency](#)
  - Specifies when to reload, used when user's choice is not immediate reload.*
- [pwm\\_force\\_output\\_trigger\\_t forceTrigger](#)
  - Specify which signal will trigger a FORCE\_OUT.*

### 36.5.3 struct pwm\_fault\_input\_filter\_param\_t

#### Data Fields

- [uint8\\_t faultFilterCount](#)
  - Fault filter count.*
- [uint8\\_t faultFilterPeriod](#)
  - Fault filter period; value of 0 will bypass the filter.*
- [bool faultGlitchStretch](#)
  - Fault Glitch Stretch Enable: A logic 1 means that input fault signals will be stretched to at least 2 IPBus clock cycles.*

### 36.5.4 struct pwm\_fault\_param\_t

#### Data Fields

- [pwm\\_fault\\_clear\\_t faultClearingMode](#)
  - Fault clearing mode to use.*
- [bool faultLevel](#)
  - true: Logic 1 indicates fault; false: Logic 0 indicates fault*
- [bool enableCombinationalPath](#)
  - true: Combinational Path from fault input is enabled; false: No combination path is available*
- [pwm\\_fault\\_recovery\\_mode\\_t recoverMode](#)
  - Specify when to re-enable the PWM output.*

### 36.5.5 struct pwm\_input\_capture\_param\_t

#### Data Fields

- bool `captureInputSel`  
*true: Use the edge counter signal as source false: Use the raw input signal from the pin as source*
- uint8\_t `edgeCompareValue`  
*Compare value, used only if edge counter is used as source.*
- `pwm_input_capture_edge_t edge0`  
*Specify which edge causes a capture for input circuitry 0.*
- `pwm_input_capture_edge_t edge1`  
*Specify which edge causes a capture for input circuitry 1.*
- bool `enableOneShotCapture`  
*true: Use one-shot capture mode; false: Use free-running capture mode*
- uint8\_t `fifoWatermark`  
*Watermark level for capture FIFO.*

#### Field Documentation

##### (1) uint8\_t `pwm_input_capture_param_t::fifoWatermark`

The capture flags in the status register will set if the word count in the FIFO is greater than this watermark level

## 36.6 Macro Definition Documentation

### 36.6.1 #define PWM\_SUBMODULE\_CHANNEL 2

## 36.7 Enumeration Type Documentation

### 36.7.1 enum `pwm_submodule_t`

Enumerator

- kPWM\_Module\_0* Submodule 0.
- kPWM\_Module\_1* Submodule 1.
- kPWM\_Module\_2* Submodule 2.
- kPWM\_Module\_3* Submodule 3.

### 36.7.2 enum `pwm_value_register_t`

Enumerator

- kPWM\_ValueRegister\_0* PWM Value0 register.
- kPWM\_ValueRegister\_1* PWM Value1 register.
- kPWM\_ValueRegister\_2* PWM Value2 register.
- kPWM\_ValueRegister\_3* PWM Value3 register.

*kPWM\_ValueRegister\_4* PWM Value4 register.

*kPWM\_ValueRegister\_5* PWM Value5 register.

### 36.7.3 enum \_pwm\_value\_register\_mask

Enumerator

*kPWM\_ValueRegisterMask\_0* PWM Value0 register mask.

*kPWM\_ValueRegisterMask\_1* PWM Value1 register mask.

*kPWM\_ValueRegisterMask\_2* PWM Value2 register mask.

*kPWM\_ValueRegisterMask\_3* PWM Value3 register mask.

*kPWM\_ValueRegisterMask\_4* PWM Value4 register mask.

*kPWM\_ValueRegisterMask\_5* PWM Value5 register mask.

### 36.7.4 enum pwm\_clock\_source\_t

Enumerator

*kPWM\_BusClock* The IPBus clock is used as the clock.

*kPWM\_ExternalClock* EXT\_CLK is used as the clock.

*kPWM\_Submodule0Clock* Clock of the submodule 0 (AUX\_CLK) is used as the source clock.

### 36.7.5 enum pwm\_clock\_prescale\_t

Enumerator

*kPWM\_Prescale\_Divide\_1* PWM clock frequency = fclk/1.

*kPWM\_Prescale\_Divide\_2* PWM clock frequency = fclk/2.

*kPWM\_Prescale\_Divide\_4* PWM clock frequency = fclk/4.

*kPWM\_Prescale\_Divide\_8* PWM clock frequency = fclk/8.

*kPWM\_Prescale\_Divide\_16* PWM clock frequency = fclk/16.

*kPWM\_Prescale\_Divide\_32* PWM clock frequency = fclk/32.

*kPWM\_Prescale\_Divide\_64* PWM clock frequency = fclk/64.

*kPWM\_Prescale\_Divide\_128* PWM clock frequency = fclk/128.

### 36.7.6 enum pwm\_force\_output\_trigger\_t

Enumerator

*kPWM\_Force\_Local* The local force signal, CTRL2[FORCE], from the submodule is used to force updates.

***kPWM\_Force\_Master*** The master force signal from submodule 0 is used to force updates.

***kPWM\_Force\_LocalReload*** The local reload signal from this submodule is used to force updates without regard to the state of LDOK.

***kPWM\_Force\_MasterReload*** The master reload signal from submodule 0 is used to force updates if LDOK is set.

***kPWM\_Force\_LocalSync*** The local sync signal from this submodule is used to force updates.

***kPWM\_Force\_MasterSync*** The master sync signal from submodule0 is used to force updates.

***kPWM\_Force\_External*** The external force signal, EXT\_FORCE, from outside the PWM module causes updates.

***kPWM\_Force\_ExternalSync*** The external sync signal, EXT\_SYNC, from outside the PWM module causes updates.

### 36.7.7 enum pwm\_output\_state\_t

Enumerator

***kPWM\_HighState*** The output state of PWM channel is high.

***kPWM\_LowState*** The output state of PWM channel is low.

***kPWM\_NormalState*** The output state of PWM channel is normal.

***kPWM\_InvertState*** The output state of PWM channel is invert.

***kPWM\_MaskState*** The output state of PWM channel is mask.

### 36.7.8 enum pwm\_init\_source\_t

Enumerator

***kPWM\_Initialize\_LocalSync*** Local sync causes initialization.

***kPWM\_Initialize\_MasterReload*** Master reload from submodule 0 causes initialization.

***kPWM\_Initialize\_MasterSync*** Master sync from submodule 0 causes initialization.

***kPWM\_Initialize\_ExtSync*** EXT\_SYNC causes initialization.

### 36.7.9 enum pwm\_load\_frequency\_t

Enumerator

***kPWM\_LoadEveryOportunity*** Every PWM opportunity.

***kPWM\_LoadEvery2Oportunity*** Every 2 PWM opportunities.

***kPWM\_LoadEvery3Oportunity*** Every 3 PWM opportunities.

***kPWM\_LoadEvery4Oportunity*** Every 4 PWM opportunities.

***kPWM\_LoadEvery5Oportunity*** Every 5 PWM opportunities.

***kPWM\_LoadEvery6Oportunity*** Every 6 PWM opportunities.

<i>kPWM_LoadEvery7Oportunity</i>	Every 7 PWM opportunities.
<i>kPWM_LoadEvery8Oportunity</i>	Every 8 PWM opportunities.
<i>kPWM_LoadEvery9Oportunity</i>	Every 9 PWM opportunities.
<i>kPWM_LoadEvery10Oportunity</i>	Every 10 PWM opportunities.
<i>kPWM_LoadEvery11Oportunity</i>	Every 11 PWM opportunities.
<i>kPWM_LoadEvery12Oportunity</i>	Every 12 PWM opportunities.
<i>kPWM_LoadEvery13Oportunity</i>	Every 13 PWM opportunities.
<i>kPWM_LoadEvery14Oportunity</i>	Every 14 PWM opportunities.
<i>kPWM_LoadEvery15Oportunity</i>	Every 15 PWM opportunities.
<i>kPWM_LoadEvery16Oportunity</i>	Every 16 PWM opportunities.

### 36.7.10 enum pwm\_fault\_input\_t

Enumerator

<i>kPWM_Fault_0</i>	Fault 0 input pin.
<i>kPWM_Fault_1</i>	Fault 1 input pin.
<i>kPWM_Fault_2</i>	Fault 2 input pin.
<i>kPWM_Fault_3</i>	Fault 3 input pin.

### 36.7.11 enum pwm\_fault\_disable\_t

Enumerator

<i>kPWM_FaultDisable_0</i>	Fault 0 disable mapping.
<i>kPWM_FaultDisable_1</i>	Fault 1 disable mapping.
<i>kPWM_FaultDisable_2</i>	Fault 2 disable mapping.
<i>kPWM_FaultDisable_3</i>	Fault 3 disable mapping.

### 36.7.12 enum pwm\_input\_capture\_edge\_t

Enumerator

<i>kPWM_Disable</i>	Disabled.
<i>kPWM_FallingEdge</i>	Capture on falling edge only.
<i>kPWM_RisingEdge</i>	Capture on rising edge only.
<i>kPWM_RiseAndFallEdge</i>	Capture on rising or falling edge.

### 36.7.13 enum pwm\_force\_signal\_t

Enumerator

***kPWM\_UsePwm*** Generated PWM signal is used by the deadtime logic.

***kPWM\_InvertedPwm*** Inverted PWM signal is used by the deadtime logic.

***kPWM\_SoftwareControl*** Software controlled value is used by the deadtime logic.

***kPWM\_UseExternal*** PWM\_EXTA signal is used by the deadtime logic.

### 36.7.14 enum pwm\_chnl\_pair\_operation\_t

Enumerator

***kPWM\_Independent*** PWM A & PWM B operate as 2 independent channels.

***kPWM\_ComplementaryPwmA*** PWM A & PWM B are complementary channels, PWM A generates the signal.

***kPWM\_ComplementaryPwmB*** PWM A & PWM B are complementary channels, PWM B generates the signal.

### 36.7.15 enum pwm\_register\_reload\_t

Enumerator

***kPWM\_ReloadImmediate*** Buffered-registers get loaded with new values as soon as LDOK bit is set.

***kPWM\_ReloadPwmHalfCycle*** Registers loaded on a PWM half cycle.

***kPWM\_ReloadPwmFullCycle*** Registers loaded on a PWM full cycle.

***kPWM\_ReloadPwmHalfAndFullCycle*** Registers loaded on a PWM half & full cycle.

### 36.7.16 enum pwm\_fault\_recovery\_mode\_t

Enumerator

***kPWM\_NoRecovery*** PWM output will stay inactive.

***kPWM\_RecoverHalfCycle*** PWM output re-enabled at the first half cycle.

***kPWM\_RecoverFullCycle*** PWM output re-enabled at the first full cycle.

***kPWM\_RecoverHalfAndFullCycle*** PWM output re-enabled at the first half or full cycle.

### 36.7.17 enum pwm\_interrupt\_enable\_t

Enumerator

<i>kPWM_CompareVal0InterruptEnable</i>	PWM VAL0 compare interrupt.
<i>kPWM_CompareVal1InterruptEnable</i>	PWM VAL1 compare interrupt.
<i>kPWM_CompareVal2InterruptEnable</i>	PWM VAL2 compare interrupt.
<i>kPWM_CompareVal3InterruptEnable</i>	PWM VAL3 compare interrupt.
<i>kPWM_CompareVal4InterruptEnable</i>	PWM VAL4 compare interrupt.
<i>kPWM_CompareVal5InterruptEnable</i>	PWM VAL5 compare interrupt.
<i>kPWM_CaptureX0InterruptEnable</i>	PWM capture X0 interrupt.
<i>kPWM_CaptureX1InterruptEnable</i>	PWM capture X1 interrupt.
<i>kPWM_CaptureB0InterruptEnable</i>	PWM capture B0 interrupt.
<i>kPWM_CaptureB1InterruptEnable</i>	PWM capture B1 interrupt.
<i>kPWM_CaptureA0InterruptEnable</i>	PWM capture A0 interrupt.
<i>kPWM_CaptureA1InterruptEnable</i>	PWM capture A1 interrupt.
<i>kPWM_ReloadInterruptEnable</i>	PWM reload interrupt.
<i>kPWM_ReloadErrorInterruptEnable</i>	PWM reload error interrupt.
<i>kPWM_Fault0InterruptEnable</i>	PWM fault 0 interrupt.
<i>kPWM_Fault1InterruptEnable</i>	PWM fault 1 interrupt.
<i>kPWM_Fault2InterruptEnable</i>	PWM fault 2 interrupt.
<i>kPWM_Fault3InterruptEnable</i>	PWM fault 3 interrupt.

### 36.7.18 enum pwm\_status\_flags\_t

Enumerator

<i>kPWM_CompareVal0Flag</i>	PWM VAL0 compare flag.
<i>kPWM_CompareVal1Flag</i>	PWM VAL1 compare flag.
<i>kPWM_CompareVal2Flag</i>	PWM VAL2 compare flag.
<i>kPWM_CompareVal3Flag</i>	PWM VAL3 compare flag.
<i>kPWM_CompareVal4Flag</i>	PWM VAL4 compare flag.
<i>kPWM_CompareVal5Flag</i>	PWM VAL5 compare flag.
<i>kPWM_CaptureX0Flag</i>	PWM capture X0 flag.
<i>kPWM_CaptureX1Flag</i>	PWM capture X1 flag.
<i>kPWM_CaptureB0Flag</i>	PWM capture B0 flag.
<i>kPWM_CaptureB1Flag</i>	PWM capture B1 flag.
<i>kPWM_CaptureA0Flag</i>	PWM capture A0 flag.
<i>kPWM_CaptureA1Flag</i>	PWM capture A1 flag.
<i>kPWM_ReloadFlag</i>	PWM reload flag.
<i>kPWM_ReloadErrorFlag</i>	PWM reload error flag.
<i>kPWM_RegUpdatedFlag</i>	PWM registers updated flag.
<i>kPWM_Fault0Flag</i>	PWM fault 0 flag.
<i>kPWM_Fault1Flag</i>	PWM fault 1 flag.

*kPWM\_Fault2Flag* PWM fault 2 flag.

*kPWM\_Fault3Flag* PWM fault 3 flag.

### 36.7.19 enum pwm\_dma\_enable\_t

Enumerator

*kPWM\_CaptureX0DMAEnable* PWM capture X0 DMA.

*kPWM\_CaptureX1DMAEnable* PWM capture X1 DMA.

*kPWM\_CaptureB0DMAEnable* PWM capture B0 DMA.

*kPWM\_CaptureB1DMAEnable* PWM capture B1 DMA.

*kPWM\_CaptureA0DMAEnable* PWM capture A0 DMA.

*kPWM\_CaptureA1DMAEnable* PWM capture A1 DMA.

### 36.7.20 enum pwm\_dma\_source\_select\_t

Enumerator

*kPWM\_DMAResetDisable* Read DMA requests disabled.

*kPWM\_DMAWatermarksEnable* Exceeding a FIFO watermark sets the DMA read request.

*kPWM\_DMALocalSync* A local sync (VAL1 matches counter) sets the read DMA request.

*kPWM\_DMALocalReload* A local reload (STS[RF] being set) sets the read DMA request.

### 36.7.21 enum pwm\_watermark\_control\_t

Enumerator

*kPWM\_FIFOWatermarksOR* Selected FIFO watermarks are OR'ed together.

*kPWM\_FIFOWatermarksAND* Selected FIFO watermarks are AND'ed together.

### 36.7.22 enum pwm\_mode\_t

Enumerator

*kPWM\_SignedCenterAligned* Signed center-aligned.

*kPWM\_CenterAligned* Unsigned center-aligned.

*kPWM\_SignedEdgeAligned* Signed edge-aligned.

*kPWM\_EdgeAligned* Unsigned edge-aligned.

### 36.7.23 enum pwm\_level\_select\_t

Enumerator

***kPWM\_HighTrue*** High level represents "on" or "active" state.

***kPWM\_LowTrue*** Low level represents "on" or "active" state.

### 36.7.24 enum pwm\_fault\_state\_t

Enumerator

***kPWM\_PwmFaultState0*** Output is forced to logic 0 state prior to consideration of output polarity control.

***kPWM\_PwmFaultState1*** Output is forced to logic 1 state prior to consideration of output polarity control.

***kPWM\_PwmFaultState2*** Output is tristated.

***kPWM\_PwmFaultState3*** Output is tristated.

### 36.7.25 enum pwm\_reload\_source\_select\_t

Enumerator

***kPWM\_LocalReload*** The local reload signal is used to reload registers.

***kPWM\_MasterReload*** The master reload signal (from submodule 0) is used to reload.

### 36.7.26 enum pwm\_fault\_clear\_t

Enumerator

***kPWM\_Automatic*** Automatic fault clearing.

***kPWM\_ManualNormal*** Manual fault clearing with no fault safety mode.

***kPWM\_ManualSafety*** Manual fault clearing with fault safety mode.

### 36.7.27 enum pwm\_module\_control\_t

Enumerator

***kPWM\_Control\_Module\_0*** Control submodule 0's start/stop,buffer reload operation.

***kPWM\_Control\_Module\_1*** Control submodule 1's start/stop,buffer reload operation.

***kPWM\_Control\_Module\_2*** Control submodule 2's start/stop,buffer reload operation.

***kPWM\_Control\_Module\_3*** Control submodule 3's start/stop,buffer reload operation.

## 36.8 Function Documentation

### 36.8.1 status\_t PWM\_Init ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **const pwm\_config\_t** \* *config* )

Note

This API should be called at the beginning of the application using the PWM driver.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>config</i>	Pointer to user's PWM config structure.

Returns

kStatus\_Success means success; else failed.

### 36.8.2 void PWM\_Deinit ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule* )

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to deinitialize

### 36.8.3 void PWM\_GetDefaultConfig ( **pwm\_config\_t** \* *config* )

The default values are:

```
* config->enableDebugMode = false;
* config->enableWait = false;
* config->reloadSelect = kPWM_LocalReload;
* config->clockSource = kPWM_BusClock;
* config->prescale = kPWM_Prescale_Divide_1;
* config->initializationControl = kPWM_Initialize_LocalSync;
* config->forceTrigger = kPWM_Force_Local;
* config->reloadFrequency = kPWM_LoadEveryOportunity;
* config->reloadLogic = kPWM_ReloadImmediate;
* config->pairOperation = kPWM_Independent;
*
```

## Parameters

<i>config</i>	Pointer to user's PWM config structure.
---------------	---

**36.8.4 status\_t PWM\_SetupPwm ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, const **pwm\_signal\_param\_t** \* *chnlParams*, **uint8\_t** *numOfChnls*, **pwm\_mode\_t** *mode*, **uint32\_t** *pwmFreq\_Hz*, **uint32\_t** *srcClock\_Hz* )**

The function initializes the submodule according to the parameters passed in by the user. The function also sets up the value compare registers to match the PWM signal requirements. If the dead time insertion logic is enabled, the pulse period is reduced by the dead time period specified by the user.

## Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>chnlParams</i>	Array of PWM channel parameters to configure the channel(s), PWMX submodule is not supported.
<i>numOfChnls</i>	Number of channels to configure, this should be the size of the array passed in. Array size should not be more than 2 as each submodule has 2 pins to output PWM
<i>mode</i>	PWM operation mode, options available in enumeration <a href="#">pwm_mode_t</a>
<i>pwmFreq_Hz</i>	PWM signal frequency in Hz
<i>srcClock_Hz</i>	PWM main counter clock in Hz.

## Returns

Returns kStatus\_Fail if there was error setting up the signal; kStatus\_Success otherwise

**36.8.5 status\_t PWM\_SetupPwmPhaseShift ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_channels\_t** *pwmChannel*, **uint32\_t** *pwmFreq\_Hz*, **uint32\_t** *srcClock\_Hz*, **uint8\_t** *shiftvalue*, **bool** *doSync* )**

## Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	PWM channel to configure
<i>pwmFreq_Hz</i>	PWM signal frequency in Hz
<i>srcClock_Hz</i>	PWM main counter clock in Hz.
<i>shiftvalue</i>	Phase shift value
<i>doSync</i>	true: Set LDOKE bit for the submodule list; false: LDOKE bit don't set, need to call PWM_SetPwmLdok to sync update.

Returns

Returns kStatus\_Fail if there was error setting up the signal; kStatus\_Success otherwise

### 36.8.6 void PWM\_UpdatePwmDutycycle ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_channels\_t** *pwmSignal*, **pwm\_mode\_t** *currPwmMode*, **uint8\_t** *dutyCyclePercent* )

The function updates the PWM dutycycle to the new value that is passed in. If the dead time insertion logic is enabled then the pulse period is reduced by the dead time period specified by the user.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmSignal</i>	Signal (PWM A or PWM B) to update
<i>currPwmMode</i>	The current PWM mode set during PWM setup
<i>dutyCycle-Percent</i>	New PWM pulse width, value should be between 0 to 100 0=inactive signal(0% duty cycle)... 100=active signal (100% duty cycle)

### 36.8.7 void PWM\_UpdatePwmDutycycleHighAccuracy ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_channels\_t** *pwmSignal*, **pwm\_mode\_t** *currPwmMode*, **uint16\_t** *dutyCycle* )

The function updates the PWM dutycycle to the new value that is passed in. If the dead time insertion logic is enabled then the pulse period is reduced by the dead time period specified by the user.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmSignal</i>	Signal (PWM A or PWM B) to update
<i>currPwmMode</i>	The current PWM mode set during PWM setup
<i>dutyCycle</i>	New PWM pulse width, value should be between 0 to 65535 0=inactive signal(0% duty cycle)... 65535=active signal (100% duty cycle)

### 36.8.8 void PWM\_SetupInputCapture ( PWM\_Type \* *base*, pwm\_- submodule\_t *subModule*, pwm\_channels\_t *pwmChannel*, const pwm\_input\_capture\_param\_t \* *inputCaptureParams* )

Each PWM submodule has 3 pins that can be configured for use as input capture pins. This function sets up the capture parameters for each pin and enables the pin for input capture operation.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	Channel in the submodule to setup
<i>inputCapture- Params</i>	Parameters passed in to set up the input pin

### 36.8.9 void PWM\_SetupFaultInputFilter ( PWM\_Type \* *base*, const pwm\_fault\_input\_filter\_param\_t \* *faultInputFilterParams* )

Parameters

<i>base</i>	PWM peripheral base address
<i>faultInput- FilterParams</i>	Parameters passed in to set up the fault input filter.

### 36.8.10 void PWM\_SetupFaults ( PWM\_Type \* *base*, pwm\_fault\_input\_t *faultNum*, const pwm\_fault\_param\_t \* *faultParams* )

PWM has 4 fault inputs.

Parameters

<i>base</i>	PWM peripheral base address
<i>faultNum</i>	PWM fault to configure.
<i>faultParams</i>	Pointer to the PWM fault config structure

### 36.8.11 void PWM\_FaultDefaultConfig ( **pwm\_fault\_param\_t** \* *config* )

The default values are:

```
* config->faultClearingMode = kPWM_Automatic;
* config->faultLevel = false;
* config->enableCombinationalPath = true;
* config->recoverMode = kPWM_NoRecovery;
*
```

Parameters

<i>config</i>	Pointer to user's PWM fault config structure.
---------------	---

### 36.8.12 void PWM\_SetupForceSignal ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_channels\_t** *pwmChannel*, **pwm\_force\_signal\_t** *mode* )

The user specifies which channel to configure by supplying the submodule number and whether to modify PWM A or PWM B within that submodule.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	Channel to configure
<i>mode</i>	Signal to output when a FORCE_OUT is triggered

### 36.8.13 void PWM\_EnableInterrupts ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **uint32\_t** *mask* )

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">pwm_interrupt_enable_t</a>

### 36.8.14 void PWM\_DisableInterrupts ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **uint32\_t** *mask* )

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">pwm_interrupt_enable_t</a>

### 36.8.15 **uint32\_t** PWM\_GetEnabledInterrupts ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule* )

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [pwm\\_interrupt\\_enable\\_t](#)

### 36.8.16 static void PWM\_DMAFIFOWatermarkControl ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_watermark\_control\_t** *pwm\_watermark\_control* ) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwm_watermark_control</i>	PWM FIFO watermark and control

**36.8.17 static void PWM\_DMACaptureSourceSelect ( PWM\_Type \* *base*, pwm\_submodule\_t *subModule*, pwm\_dma\_source\_select\_t *pwm\_dma\_source\_select* ) [inline], [static]**

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwm_dma_source_select</i>	PWM capture DMA enable source select

**36.8.18 static void PWM\_EnableDMACapture ( PWM\_Type \* *base*, pwm\_submodule\_t *subModule*, uint16\_t *mask*, bool *activate* ) [inline], [static]**

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>mask</i>	The DMA to enable or disable. This is a logical OR of members of the enumeration <a href="#">pwm_dma_enable_t</a>
<i>activate</i>	true: Enable DMA read request; false: Disable DMA read request

**36.8.19 static void PWM\_EnableDMAWrite ( PWM\_Type \* *base*, pwm\_submodule\_t *subModule*, bool *activate* ) [inline], [static]**

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>activate</i>	true: Enable DMA write request; false: Disable DMA write request

### 36.8.20 `uint32_t PWM_GetStatusFlags ( PWM_Type * base, pwm_submodule_t subModule )`

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure

Returns

The status flags. This is the logical OR of members of the enumeration [pwm\\_status\\_flags\\_t](#)

### 36.8.21 `void PWM_ClearStatusFlags ( PWM_Type * base, pwm_submodule_t subModule, uint32_t mask )`

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>mask</i>	The status flags to clear. This is a logical OR of members of the enumeration <a href="#">pwm_status_flags_t</a>

### 36.8.22 `static void PWM_StartTimer ( PWM_Type * base, uint8_t subModulesToStart ) [inline], [static]`

Sets the Run bit which enables the clocks to the PWM submodule. This function can start multiple submodules at the same time.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModulesToStart</i>	PWM submodules to start. This is a logical OR of members of the enumeration <a href="#">pwm_module_control_t</a>

### 36.8.23 static void PWM\_StopTimer ( **PWM\_Type** \* *base*, **uint8\_t** *subModulesToStop* ) [inline], [static]

Clears the Run bit which resets the submodule's counter. This function can stop multiple submodules at the same time.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModulesToStop</i>	PWM submodules to stop. This is a logical OR of members of the enumeration <a href="#">pwm_module_control_t</a>

### 36.8.24 static void PWM\_SetVALxValue ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_value\_register\_t** *valueRegister*, **uint16\_t** *value* ) [inline], [static]

This function allows the user to write value into VAL registers directly. And it will destroying the PWM clock period set by the [PWM\\_SetupPwm\(\)](#)/[PWM\\_SetupPwmPhaseShift\(\)](#) functions. Due to VALx registers are buffered, the new value will not active unless call [PWM\\_SetPwmLdok\(\)](#) and the reload point is reached.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>valueRegister</i>	VALx register that will be written new value
<i>value</i>	Value that will be written into VALx register

### 36.8.25 static **uint16\_t** PWM\_GetVALxValue ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_value\_register\_t** *valueRegister* ) [inline], [static]

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>valueRegister</i>	VALx register that will be read value

Returns

The VALx register value

**36.8.26 static void PWM\_OutputTriggerEnable ( PWM\_Type \* *base*,  
pwm\_submodule\_t *subModule*, pwm\_value\_register\_t *valueRegister*, bool  
*activate* ) [inline], [static]**

This function allows the user to enable or disable the PWM trigger. The PWM has 2 triggers. Trigger 0 is activated when the counter matches VAL 0, VAL 2, or VAL 4 register. Trigger 1 is activated when the counter matches VAL 1, VAL 3, or VAL 5 register.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>valueRegister</i>	Value register that will activate the trigger
<i>activate</i>	true: Enable the trigger; false: Disable the trigger

**36.8.27 static void PWM\_ActivateOutputTrigger ( PWM\_Type \* *base*,  
pwm\_submodule\_t *subModule*, uint16\_t *valueRegisterMask* ) [inline],  
[static]**

This function allows the user to enable one or more (VAL0-5) PWM trigger.

Parameters

<i>base</i>	PWM peripheral base address
-------------	-----------------------------

<i>subModule</i>	PWM submodule to configure
<i>valueRegister-Mask</i>	Value register mask that will activate one or more (VAL0-5) trigger enumeration <a href="#">_pwm_value_register_mask</a>

**36.8.28 static void PWM\_DeactivateOutputTrigger ( PWM\_Type \* *base*, pwm\_submodule\_t *subModule*, uint16\_t *valueRegisterMask* ) [inline], [static]**

This function allows the user to disables one or more (VAL0-5) PWM trigger.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>valueRegister-Mask</i>	Value register mask that will Deactivate one or more (VAL0-5) trigger enumeration <a href="#">_pwm_value_register_mask</a>

**36.8.29 static void PWM\_SetupSwCtrlOut ( PWM\_Type \* *base*, pwm\_submodule\_t *subModule*, pwm\_channels\_t *pwmChannel*, bool *value* ) [inline], [static]**

The user specifies which channel to modify by supplying the submodule number and whether to modify PWM A or PWM B within that submodule.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	Channel to configure
<i>value</i>	true: Supply a logic 1, false: Supply a logic 0.

**36.8.30 static void PWM\_SetPwmLdok ( PWM\_Type \* *base*, uint8\_t *subModulesToUpdate*, bool *value* ) [inline], [static]**

Set LDOK bit to load buffered values into CTRL[PRSC] and the INIT, FRACVAL and VAL registers. The values are loaded immediately if kPWM\_ReloadImmediate option was chosen during config. Else the values are loaded at the next PWM reload point. This function can issue the load command to multiple submodules at the same time.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModulesToUpdate</i>	PWM submodules to update with buffered values. This is a logical OR of members of the enumeration <a href="#">pwm_module_control_t</a>
<i>value</i>	true: Set LDOK bit for the submodule list; false: Clear LDOK bit

### 36.8.31 static void PWM\_SetPwmFaultState ( **PWM\_Type** \* *base*, *pwm\_submodule\_t* *subModule*, *pwm\_channels\_t* *pwmChannel*, *pwm\_fault\_state\_t* *faultState* ) [inline], [static]

These bits determine the fault state for the PWM\_A output in fault conditions and STOP mode. It may also define the output state in WAIT and DEBUG modes depending on the settings of CTRL2[WAITEN] and CTRL2[DBGEN]. This function can update PWM output fault status.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	Channel to configure
<i>faultState</i>	PWM output fault status

### 36.8.32 static void PWM\_SetupFaultDisableMap ( **PWM\_Type** \* *base*, *pwm\_submodule\_t* *subModule*, *pwm\_channels\_t* *pwmChannel*, *pwm\_fault\_channels\_t* *pwm\_fault\_channels*, *uint16\_t* *value* ) [inline], [static]

Each of the four bits of this read/write field is one-to-one associated with the four FAULTx inputs of fault channel 0/1. The PWM output will be turned off if there is a logic 1 on an FAULTx input and a 1 in the corresponding bit of this field. A reset sets all bits in this field.

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	PWM channel to configure
<i>pwm_fault_channels</i>	PWM fault channel to configure
<i>value</i>	Fault disable mapping mask value enumeration <a href="#">pwm_fault_disable_t</a>

### 36.8.33 static void PWM\_OutputEnable ( **PWM\_Type** \* *base*, **pwm\_channels\_t** *pwmChannel*, **pwm\_submodule\_t** *subModule* ) [inline], [static]

This feature allows the user to enable the PWM Output.

Parameters

<i>base</i>	PWM peripheral base address
<i>pwmChannel</i>	PWM channel to configure
<i>subModule</i>	PWM submodule to configure

### 36.8.34 static void PWM\_OutputDisable ( **PWM\_Type** \* *base*, **pwm\_channels\_t** *pwmChannel*, **pwm\_submodule\_t** *subModule* ) [inline], [static]

This feature allows the user to disable the PWM output.

Parameters

<i>base</i>	PWM peripheral base address
<i>pwmChannel</i>	PWM channel to configure
<i>subModule</i>	PWM submodule to configure

### 36.8.35 uint8\_t PWM\_GetPwmChannelState ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_channels\_t** *pwmChannel* )

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	PWM channel to configure

Returns

Current channel dutycycle value.

### 36.8.36 status\_t PWM\_SetOutputTidle ( **PWM\_Type** \* *base*, **pwm\_channels\_t** *pwmChannel*, **pwm\_submodule\_t** *subModule*, **bool** *idleStatus* )

Note

This API should call after [PWM\\_SetupPwm\(\)](#) APIs, and PWMX submodule is not supported.

Parameters

<i>base</i>	PWM peripheral base address
<i>pwmChannel</i>	PWM channel to configure
<i>subModule</i>	PWM submodule to configure
<i>idleStatus</i>	True: PWM output is high in idle status; false: PWM output is low in idle status.

Returns

kStatus\_Fail if there was error setting up the signal; kStatus\_Success if set output idle success

### 36.8.37 void PWM\_SetClockMode ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_clock\_prescale\_t** *prescaler* )

Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>prescaler</i>	Set prescaler value

### 36.8.38 void PWM\_SetPwmForceOutputToZero ( **PWM\_Type** \* *base*, **pwm\_submodule\_t** *subModule*, **pwm\_channels\_t** *pwmChannel*, **bool** *forcetozero* )

Parameters

<i>base</i>	PWM peripheral base address
<i>pwmChannel</i>	PWM channel to configure
<i>subModule</i>	PWM submodule to configure
<i>forcetozero</i>	True: Enable the pwm force output to zero; False: Disable the pwm output resumes normal function.

36.8.39 void PWM\_SetChannelOutput ( **PWM\_Type** \* *base*, **pwm\_submodule\_t**  
*subModule*, **pwm\_channels\_t** *pwmChannel*, **pwm\_output\_state\_t**  
*outputstate* )

## Parameters

<i>base</i>	PWM peripheral base address
<i>subModule</i>	PWM submodule to configure
<i>pwmChannel</i>	PWM channel to configure
<i>outputstate</i>	Set pwm output state, see <a href="#">pwm_output_state_t</a> .

# Chapter 37

## PXP: Pixel Pipeline

### 37.1 Overview

The MCUXpresso SDK provides a driver for the Pixel Pipeline (PXP)

The PXP is used to process graphics buffers or composite video and graphics data before sending to an LCD display or TV encoder. The PXP driver only provides functional APIs. It does not maintain software level state, so that the APIs could be involved directly to any upper layer graphics framework easily.

To use the PXP driver, call [PXP\\_Init](#) first to enable and initialize the peripheral. Generally, call the PXP driver APIs the configure input buffer, output buffer, and other setting such as flip, rotate, then call [PXP\\_Start](#), thus the PXP starts the processing. When finished, the flag [kPXP\\_CompleteFlag](#) asserts. PXP also supports operation queuing, it means that a new operation could be submitted to PXP while the current PXP operation is running. When current operation finished, the new operation configurations are loaded to PXP register and new processing starts.

### 37.2 Typical use case

#### 37.2.1 PXP normal operation

This example shows how to perform vertical flip to process surface and save to output buffer. The input and output buffer pixel format are RGB888.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pxp

#### 37.2.2 PXP operation queue

This example shows how to perform vertical flip to process surface using operation queue. The input and output buffer pixel format are RGB888.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pxp

### Data Structures

- struct [pxp\\_output\\_buffer\\_config\\_t](#)  
*PXP output buffer configuration.* [More...](#)
- struct [pxp\\_ps\\_buffer\\_config\\_t](#)  
*PXP process surface buffer configuration.* [More...](#)
- struct [pxp\\_as\\_buffer\\_config\\_t](#)  
*PXP alphas surface buffer configuration.* [More...](#)
- struct [pxp\\_as\\_blend\\_config\\_t](#)  
*PXP alpha surface blending configuration.* [More...](#)
- struct [pxp\\_csc2\\_config\\_t](#)

- struct `pxp_dither_final_lut_data_t`  
*PXP dither final LUT data.* [More...](#)
- struct `pxp_dither_config_t`  
*PXP dither configuration.* [More...](#)
- struct `pxp_porter_duff_config_t`  
*PXP Porter Duff configuration.* [More...](#)
- struct `pxp_pic_copy_config_t`  
*PXP Porter Duff blend mode.* [More...](#)

## Enumerations

- enum `_pxp_interrupt_enable` {
   
`kPXP_CompleteInterruptEnable` = PXP\_CTRL\_IRQ\_ENABLE\_MASK,  
`kPXP_CommandLoadInterruptEnable` = PXP\_CTRL\_NEXT\_IRQ\_ENABLE\_MASK }
- enum `_pxp_flags` {
   
`kPXP_CompleteFlag` = PXP\_STAT\_IRQ0\_MASK,  
`kPXP_Axi0WriteErrorFlag` = PXP\_STAT\_AXI\_WRITE\_ERROR\_0\_MASK,  
`kPXP_Axi0ReadErrorFlag` = PXP\_STAT\_AXI\_READ\_ERROR\_0\_MASK,  
`kPXP_CommandLoadFlag` = PXP\_STAT\_NEXT\_IRQ\_MASK }
- enum `pxp_flip_mode_t` {
   
`kPXP_FlipDisable` = 0U,  
`kPXP_FlipHorizontal` = 0x01U,  
`kPXP_FlipVertical` = 0x02U,  
`kPXP_FlipBoth` = 0x03U }
- enum `pxp_rotate_position_t` {
   
`kPXP_RotateOutputBuffer` = 0U,  
`kPXP_RotateProcessSurface` }
- enum `pxp_rotate_degree_t` {
   
`kPXP_Rotate0` = 0U,  
`kPXP_Rotate90`,  
`kPXP_Rotate180`,  
`kPXP_Rotate270` }
- enum `pxp_interlaced_output_mode_t` {
   
`kPXP_OutputProgressive` = 0U,  
`kPXP_OutputField0`,  
`kPXP_OutputField1`,  
`kPXP_OutputInterlaced` }
- enum `pxp_output_pixel_format_t` {

```

kPXP_OutputPixelFormatARGB888 = 0x0,
kPXP_OutputPixelFormatRGB888 = 0x4,
kPXP_OutputPixelFormatRGB888P = 0x5,
kPXP_OutputPixelFormatARGB1555 = 0x8,
kPXP_OutputPixelFormatARGB4444 = 0x9,
kPXP_OutputPixelFormatRGB555 = 0xC,
kPXP_OutputPixelFormatRGB444 = 0xD,
kPXP_OutputPixelFormatRGB565 = 0xE,
kPXP_OutputPixelFormatYUV1P444 = 0x10,
kPXP_OutputPixelFormatUYVY1P422 = 0x12,
kPXP_OutputPixelFormatVYUY1P422 = 0x13,
kPXP_OutputPixelFormatY8 = 0x14,
kPXP_OutputPixelFormatY4 = 0x15,
kPXP_OutputPixelFormatYUV2P422 = 0x18,
kPXP_OutputPixelFormatYUV2P420 = 0x19,
kPXP_OutputPixelFormatYVU2P422 = 0x1A,
kPXP_OutputPixelFormatYVU2P420 = 0x1B }

```

*PXP output buffer format.*

- enum `pxp_ps_pixel_format_t` {
 

```

kPXP_PsPixelFormatARGB888 = 0x4,
kPXP_PsPixelFormatARGB1555 = 0xC,
kPXP_PsPixelFormatARGB4444 = 0xD,
kPXP_PsPixelFormatRGB565 = 0xE,
kPXP_PsPixelFormatYUV1P444 = 0x10,
kPXP_PsPixelFormatUYVY1P422 = 0x12,
kPXP_PsPixelFormatVYUY1P422 = 0x13,
kPXP_PsPixelFormatY8 = 0x14,
kPXP_PsPixelFormatY4 = 0x15,
kPXP_PsPixelFormatYUV2P422 = 0x18,
kPXP_PsPixelFormatYUV2P420 = 0x19,
kPXP_PsPixelFormatYVU2P422 = 0x1A,
kPXP_PsPixelFormatYVU2P420 = 0x1B,
kPXP_PsPixelFormatYVU422 = 0x1E,
kPXP_PsPixelFormatYVU420 = 0x1F,
kPXP_PsPixelFormatRGBA8888 = 0x24,
kPXP_PsPixelFormatRGBA5551 = 0x2C,
kPXP_PsPixelFormatRGBA4444 = 0x2D }

```

*PXP process surface buffer pixel format.*

- enum `pxp_ps_yuv_format_t` {
 

```

kPXP_PsYUVFormatYUV = 0U,
kPXP_PsYUVFormatYCbCr }

```

*PXP process surface buffer YUV format.*

- enum `pxp_as_pixel_format_t` {

```

kPXP_AsPixelFormatARGB8888 = 0x0,
kPXP_AsPixelFormatRGB888 = 0x4,
kPXP_AsPixelFormatARGB1555 = 0x8,
kPXP_AsPixelFormatARGB4444 = 0x9,
kPXP_AsPixelFormatRGB555 = 0xC,
kPXP_AsPixelFormatRGB444 = 0xD,
kPXP_AsPixelFormatRGB565 = 0xE,
kPXP_AsPixelFormatRGBA8888 = 0x1,
kPXP_AsPixelFormatRGBA5551 = 0xA,
kPXP_AsPixelFormatRGBA4444 = 0xB }

```

*PXP alpha surface buffer pixel format.*

- enum `pxp_alpha_mode_t` {
   
kPXP\_AlphaEmbedded,
   
kPXP\_AlphaOverride,
   
kPXP\_AlphaMultiply,
   
kPXP\_AlphaRop }

*PXP alpha mode during blending.*

- enum `pxp_rop_mode_t` {
   
kPXP\_RopMaskAs = 0x0,
   
kPXP\_RopMaskNotAs = 0x1,
   
kPXP\_RopMaskAsNot = 0x2,
   
kPXP\_RopMergeAs = 0x3,
   
kPXP\_RopMergeNotAs = 0x4,
   
kPXP\_RopMergeAsNot = 0x5,
   
kPXP\_RopNotCopyAs = 0x6,
   
kPXP\_RopNot = 0x7,
   
kPXP\_RopNotMaskAs = 0x8,
   
kPXP\_RopNotMergeAs = 0x9,
   
kPXP\_RopXorAs = 0xA,
   
kPXP\_RopNotXorAs = 0xB }

*PXP ROP mode during blending.*

- enum `pxp_block_size_t` {
   
kPXP\_BlockSize8 = 0U,
   
kPXP\_BlockSize16 }
- enum `pxp_csc1_mode_t` {
   
kPXP\_Csc1YUV2RGB = 0U,
   
kPXP\_Csc1YCbCr2RGB }
- enum `pxp_csc2_mode_t` {
   
kPXP\_Csc2YUV2RGB = 0U,
   
kPXP\_Csc2YCbCr2RGB,
   
kPXP\_Csc2RGB2YUV,
   
kPXP\_Csc2RGB2YCbCr }
- enum `pxp_ram_t` {

- ```

kPXP_RamDither0Lut = 0U,
kPXP_RamDither1Lut = 3U,
kPXP_RamDither2Lut = 4U }

PXP internal memory.
• enum _pxp_dither_mode {
  kPXP_DitherPassThrough = 0U,
  kPXP_DitherFloydSteinberg = 1U,
  kPXP_DitherAtkinson = 2U,
  kPXP_DitherOrdered = 3U,
  kPXP_DitherQuantOnly = 4U,
  kPXP_DitherSierra = 5U }

PXP dither mode.
• enum _pxp_dither_lut_mode {
  kPXP_DitherLutOff = 0U,
  kPXP_DitherLutPreDither,
  kPXP_DitherLutPostDither }

PXP dither LUT mode.
• enum _pxp_dither_matrix_size {
  kPXP_DitherMatrix4 = 0,
  kPXP_DitherMatrix8,
  kPXP_DitherMatrix16 }

PXP dither matrix size.
• enum {
  kPXP_PorterDuffFactorOne = 0U,
  kPXP_PorterDuffFactorZero,
  kPXP_PorterDuffFactorStraight,
  kPXP_PorterDuffFactorInversed }

Porter Duff factor mode.
• enum {
  kPXP_PorterDuffGlobalAlpha = 0U,
  kPXP_PorterDuffLocalAlpha,
  kPXP_PorterDuffScaledAlpha }

Porter Duff global alpha mode.
• enum {
  kPXP_PorterDuffAlphaStraight = 0U,
  kPXP_PorterDuffAlphaInversed }

Porter Duff alpha mode.
• enum {
  kPXP_PorterDuffColorStraight = 0,
  kPXP_PorterDuffColorInversed = 1,
  kPXP_PorterDuffColorNoAlpha = 0,
  kPXP_PorterDuffColorWithAlpha = 1 }

Porter Duff color mode.
• enum pxp_porter_duff_blend_mode_t {

```

```

kPXP_PorterDuffSrc = 0,
kPXP_PorterDuffAtop,
kPXP_PorterDuffOver,
kPXP_PorterDuffIn,
kPXP_PorterDuffOut,
kPXP_PorterDuffDst,
kPXP_PorterDuffDstAtop,
kPXP_PorterDuffDstOver,
kPXP_PorterDuffDstIn,
kPXP_PorterDuffDstOut,
kPXP_PorterDuffXor,
kPXP_PorterDuffClear }

PXP Porter Duff blend mode.

```

## Driver version

- #define **FSL\_PXP\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 6, 0))

## Initialization and deinitialization

- void **PXP\_Init** (PXP\_Type \*base)  
*Initialize the PXP.*
- void **PXP\_Deinit** (PXP\_Type \*base)  
*De-initialize the PXP.*
- void **PXP\_Reset** (PXP\_Type \*base)  
*Reset the PXP.*
- void **PXP\_ResetControl** (PXP\_Type \*base)  
*Reset the PXP and the control register to initialized state.*

## Global operations

- static void **PXP\_Start** (PXP\_Type \*base)  
*Start process.*
- static void **PXP\_EnableLcdHandShake** (PXP\_Type \*base, bool enable)  
*Enable or disable LCD hand shake.*
- static void **PXP\_EnableContinousRun** (PXP\_Type \*base, bool enable)  
*Enable or disable continous run.*
- static void **PXP\_SetProcessBlockSize** (PXP\_Type \*base, **pxp\_block\_size\_t** size)  
*Set the PXP processing block size.*

## Status

- static uint32\_t **PXP\_GetStatusFlags** (PXP\_Type \*base)  
*Gets PXP status flags.*
- static void **PXP\_ClearStatusFlags** (PXP\_Type \*base, uint32\_t statusMask)  
*Clears status flags with the provided mask.*
- static uint8\_t **PXP\_GetAxiErrorId** (PXP\_Type \*base, uint8\_t axiIndex)  
*Gets the AXI ID of the failing bus operation.*

## Interrupts

- static void **PXP\_EnableInterrupts** (PXP\_Type \*base, uint32\_t mask)  
*Enables PXP interrupts according to the provided mask.*
- static void **PXP\_DisableInterrupts** (PXP\_Type \*base, uint32\_t mask)  
*Disables PXP interrupts according to the provided mask.*

## Alpha surface

- void **PXP\_SetAlphaSurfaceBufferConfig** (PXP\_Type \*base, const ppx\_as\_buffer\_config\_t \*config)  
*Set the alpha surface input buffer configuration.*
- void **PXP\_SetAlphaSurfaceBlendConfig** (PXP\_Type \*base, const ppx\_as\_blend\_config\_t \*config)  
*Set the alpha surface blending configuration.*
- void **PXP\_SetAlphaSurfaceOverlayColorKey** (PXP\_Type \*base, uint32\_t colorKeyLow, uint32\_t colorKeyHigh)  
*Set the alpha surface overlay color key.*
- static void **PXP\_EnableAlphaSurfaceOverlayColorKey** (PXP\_Type \*base, bool enable)  
*Enable or disable the alpha surface color key.*
- void **PXP\_SetAlphaSurfacePosition** (PXP\_Type \*base, uint16\_t upperLeftX, uint16\_t upperLeftY, uint16\_t lowerRightX, uint16\_t lowerRightY)  
*Set the alpha surface position in output buffer.*

## Process surface

- static void **PXP\_SetProcessSurfaceBackGroundColor** (PXP\_Type \*base, uint32\_t backGroundColor)  
*Set the back ground color of PS.*
- void **PXP\_SetProcessSurfaceBufferConfig** (PXP\_Type \*base, const ppx\_ps\_buffer\_config\_t \*config)  
*Set the process surface input buffer configuration.*
- void **PXP\_SetProcessSurfaceScaler** (PXP\_Type \*base, uint16\_t inputWidth, uint16\_t inputHeight, uint16\_t outputWidth, uint16\_t outputHeight)  
*Set the process surface scaler configuration.*
- void **PXP\_SetProcessSurfacePosition** (PXP\_Type \*base, uint16\_t upperLeftX, uint16\_t upperLeftY, uint16\_t lowerRightX, uint16\_t lowerRightY)  
*Set the process surface position in output buffer.*
- void **PXP\_SetProcessSurfaceColorKey** (PXP\_Type \*base, uint32\_t colorKeyLow, uint32\_t colorKeyHigh)  
*Set the process surface color key.*
- static void **PXP\_SetProcessSurfaceYUVFormat** (PXP\_Type \*base, ppx\_ps\_yuv\_format\_t format)  
*Set the process surface input pixel format YUV or YCbCr.*

## Output buffer

- void **PXP\_SetOutputBufferConfig** (PXP\_Type \*base, const ppx\_output\_buffer\_config\_t \*config)  
*Set the PXP output buffer configuration.*
- static void **PXP\_SetOverwrittenAlphaValue** (PXP\_Type \*base, uint8\_t alpha)  
*Set the global overwritten alpha value.*
- static void **PXP\_EnableOverWrittenAlpha** (PXP\_Type \*base, bool enable)  
*Enable or disable the global overwritten alpha value.*

- static void [PXP\\_SetRotateConfig](#) (PXP\_Type \*base, ppx\_rotate\_position\_t position, ppx\_rotate\_degree\_t degree, ppx\_flip\_mode\_t flipMode)  
*Set the rotation configuration.*
- void [PXP\\_BuildRect](#) (PXP\_Type \*base, ppx\_output\_pixel\_format\_t outFormat, uint32\_t value, uint16\_t width, uint16\_t height, uint16\_t pitch, uint32\_t outAddr)  
*Build a solid rectangle of given pixel value.*

## Command queue

- void [PXP\\_SetNextCommand](#) (PXP\_Type \*base, void \*commandAddr)  
*Set the next command.*
- static bool [PXP\\_IsNextCommandPending](#) (PXP\_Type \*base)  
*Check whether the next command is pending.*
- static void [PXP\\_CancelNextCommand](#) (PXP\_Type \*base)  
*Cancel command set by [PXP\\_SetNextCommand](#).*

## Color space conversion

- void [PXP\\_SetCsc1Mode](#) (PXP\_Type \*base, ppx\_csc1\_mode\_t mode)  
*Set the CSC1 mode.*
- static void [PXP\\_EnableCsc1](#) (PXP\_Type \*base, bool enable)  
*Enable or disable the CSC1.*

## Porter Duff

- void [PXP\\_SetPorterDuffConfig](#) (PXP\_Type \*base, const ppx\_porter\_duff\_config\_t \*config)  
*Set the Porter Duff configuration.*
- status\_t [PXP\\_GetPorterDuffConfigExt](#) (ppx\_porter\_duff\_blend\_mode\_t mode, ppx\_porter\_duff\_config\_t \*config, uint8\_t dstGlobalAlphaMode, uint8\_t dstAlphaMode, uint8\_t dstColorMode, uint8\_t srcGlobalAlphaMode, uint8\_t srcAlphaMode, uint8\_t srcColorMode, uint8\_t dstGlobalAlpha, uint8\_t srcGlobalAlpha)  
*Get the Porter Duff configuration.*
- static status\_t [PXP\\_GetPorterDuffConfig](#) (ppx\_porter\_duff\_blend\_mode\_t mode, ppx\_porter\_duff\_config\_t \*config)  
*Get the Porter Duff configuration by blend mode.*

## 37.3 Data Structure Documentation

### 37.3.1 struct ppx\_output\_buffer\_config\_t

#### Data Fields

- ppx\_output\_pixel\_format\_t pixelFormat  
*Output buffer pixel format.*
- ppx\_interlaced\_output\_mode\_t interlacedMode  
*Interlaced output mode.*
- uint32\_t buffer0Addr  
*Output buffer 0 address.*
- uint32\_t buffer1Addr

- *Output buffer 1 address, used for UV data in YUV 2-plane mode, or field 1 in output interlaced mode.*
- **uint16\_t pitchBytes**  
*Number of bytes between two vertically adjacent pixels.*
- **uint16\_t width**  
*Pixels per line.*
- **uint16\_t height**  
*How many lines in output buffer.*

## Field Documentation

- (1) **pxp\_output\_pixel\_format\_t ppx\_output\_buffer\_config\_t::pixelFormat**
- (2) **pxp\_interlaced\_output\_mode\_t ppx\_output\_buffer\_config\_t::interlacedMode**
- (3) **uint32\_t ppx\_output\_buffer\_config\_t::buffer0Addr**
- (4) **uint32\_t ppx\_output\_buffer\_config\_t::buffer1Addr**
- (5) **uint16\_t ppx\_output\_buffer\_config\_t::pitchBytes**
- (6) **uint16\_t ppx\_output\_buffer\_config\_t::width**
- (7) **uint16\_t ppx\_output\_buffer\_config\_t::height**

### 37.3.2 struct ppx\_ps\_buffer\_config\_t

## Data Fields

- **pxp\_ps\_pixel\_format\_t pixelFormat**  
*PS buffer pixel format.*
- **bool swapByte**  
*For each 16 bit word, set true to swap the two bytes.*
- **uint32\_t bufferAddr**  
*Input buffer address for the first panel.*
- **uint32\_t bufferAddrU**  
*Input buffer address for the second panel.*
- **uint32\_t bufferAddrV**  
*Input buffer address for the third panel.*
- **uint16\_t pitchBytes**  
*Number of bytes between two vertically adjacent pixels.*

**Field Documentation**

- (1) `pxp_ps_pixel_format_t pxp_ps_buffer_config_t::pixelFormat`
- (2) `bool pxp_ps_buffer_config_t::swapByte`
- (3) `uint32_t pxp_ps_buffer_config_t::bufferAddr`
- (4) `uint32_t pxp_ps_buffer_config_t::bufferAddrU`
- (5) `uint32_t pxp_ps_buffer_config_t::bufferAddrV`
- (6) `uint16_t pxp_ps_buffer_config_t::pitchBytes`

**37.3.3 struct pxp\_as\_buffer\_config\_t****Data Fields**

- `pxp_as_pixel_format_t pixelFormat`  
*AS buffer pixel format.*
- `uint32_t bufferAddr`  
*Input buffer address.*
- `uint16_t pitchBytes`  
*Number of bytes between two vertically adjacent pixels.*

**Field Documentation**

- (1) `pxp_as_pixel_format_t pxp_as_buffer_config_t::pixelFormat`
- (2) `uint32_t pxp_as_buffer_config_t::bufferAddr`
- (3) `uint16_t pxp_as_buffer_config_t::pitchBytes`

**37.3.4 struct pxp\_as\_blend\_config\_t****Data Fields**

- `uint8_t alpha`  
*User defined alpha value, only used when `alphaMode` is `kPXP_AlphaOverride` or `kPXP_AlphaRop`.*
- `bool invertAlpha`  
*Set true to invert the alpha.*
- `pxp_alpha_mode_t alphaMode`  
*Alpha mode.*
- `pxp_rop_mode_t ropMode`  
*ROP mode, only valid when `alphaMode` is `kPXP_AlphaRop`.*

**Field Documentation**

- (1) `uint8_t ppx_as_blend_config_t::alpha`
- (2) `bool ppx_as_blend_config_t::invertAlpha`
- (3) `ppx_alpha_mode_t ppx_as_blend_config_t::alphaMode`
- (4) `ppx_rop_mode_t ppx_as_blend_config_t::ropMode`

**37.3.5 struct ppx\_csc2\_config\_t**

Converting from YUV/YCbCr color spaces to the RGB color space uses the following equation structure:

$$R = A1(Y+D1) + A2(U+D2) + A3(V+D3) \quad G = B1(Y+D1) + B2(U+D2) + B3(V+D3) \quad B = C1(Y+D1) + C2(U+D2) + C3(V+D3)$$

Converting from the RGB color space to YUV/YCbCr color spaces uses the following equation structure:

$$Y = A1*R + A2*G + A3*B + D1 \quad U = B1*R + B2*G + B3*B + D2 \quad V = C1*R + C2*G + C3*B + D3$$

**Data Fields**

- `ppx_csc2_mode_t mode`  
*Conversion mode.*
- float `A1`  
*A1.*
- float `A2`  
*A2.*
- float `A3`  
*A3.*
- float `B1`  
*B1.*
- float `B2`  
*B2.*
- float `B3`  
*B3.*
- float `C1`  
*C1.*
- float `C2`  
*C2.*
- float `C3`  
*C3.*
- int16\_t `D1`  
*D1.*
- int16\_t `D2`  
*D2.*
- int16\_t `D3`  
*D3.*

**Field Documentation**

- (1) `pxp_csc2_mode_t ppx_csc2_config_t::mode`
- (2) `float ppx_csc2_config_t::A1`
- (3) `float ppx_csc2_config_t::A2`
- (4) `float ppx_csc2_config_t::A3`
- (5) `float ppx_csc2_config_t::B1`
- (6) `float ppx_csc2_config_t::B2`
- (7) `float ppx_csc2_config_t::B3`
- (8) `float ppx_csc2_config_t::C1`
- (9) `float ppx_csc2_config_t::C2`
- (10) `float ppx_csc2_config_t::C3`
- (11) `int16_t ppx_csc2_config_t::D1`
- (12) `int16_t ppx_csc2_config_t::D2`
- (13) `int16_t ppx_csc2_config_t::D3`

**37.3.6 struct ppx\_dither\_final\_lut\_data\_t****Data Fields**

- `uint32_t data_3_0`  
*Data 3 to data 0.*
- `uint32_t data_7_4`  
*Data 7 to data 4.*
- `uint32_t data_11_8`  
*Data 11 to data 8.*
- `uint32_t data_15_12`  
*Data 15 to data 12.*

**Field Documentation**

- (1) `uint32_t ppx_dither_final_lut_data_t::data_3_0`

Data 0 is the least significant byte.

- (2) `uint32_t ppx_dither_final_lut_data_t::data_7_4`

Data 4 is the least significant byte.

(3) **uint32\_t ppx\_dither\_final\_lut\_data\_t::data\_11\_8**

Data 8 is the least significant byte.

(4) **uint32\_t ppx\_dither\_final\_lut\_data\_t::data\_15\_12**

Data 12 is the least significant byte.

**37.3.7 struct ppx\_dither\_config\_t****Data Fields**

- **uint32\_t enableDither0:** 1  
*Enable dither engine 0 or not, set 1 to enable, 0 to disable.*
- **uint32\_t enableDither1:** 1  
*Enable dither engine 1 or not, set 1 to enable, 0 to disable.*
- **uint32\_t enableDither2:** 1  
*Enable dither engine 2 or not, set 1 to enable, 0 to disable.*
- **uint32\_t ditherMode0:** 3  
*Dither mode for dither engine 0.*
- **uint32\_t ditherMode1:** 3  
*Dither mode for dither engine 1.*
- **uint32\_t ditherMode2:** 3  
*Dither mode for dither engine 2.*
- **uint32\_t quantBitNum:** 3  
*Number of bits quantize down to, the valid value is 1~7.*
- **uint32\_t lutMode:** 2  
*How to use the memory LUT, see [\\_ppx\\_dither\\_lut\\_mode](#).*
- **uint32\_t idxMatrixSize0:** 2  
*Size of index matrix used for dither for dither engine 0, see [\\_ppx\\_dither\\_matrix\\_size](#).*
- **uint32\_t idxMatrixSize1:** 2  
*Size of index matrix used for dither for dither engine 1, see [\\_ppx\\_dither\\_matrix\\_size](#).*
- **uint32\_t idxMatrixSize2:** 2  
*Size of index matrix used for dither for dither engine 2, see [\\_ppx\\_dither\\_matrix\\_size](#).*
- **uint32\_t enableFinalLut:** 1  
*Enable the final LUT, set 1 to enable, 0 to disable.*

**Field Documentation**(1) **uint32\_t ppx\_dither\_config\_t::enableDither0**(2) **uint32\_t ppx\_dither\_config\_t::enableDither1**(3) **uint32\_t ppx\_dither\_config\_t::enableDither2**(4) **uint32\_t ppx\_dither\_config\_t::ditherMode0**

See [\\_ppx\\_dither\\_mode](#).

(5) `uint32_t ppx_dither_config_t::ditherMode1`

See [\\_ppx\\_dither\\_mode](#).

(6) `uint32_t ppx_dither_config_t::ditherMode2`

See [\\_ppx\\_dither\\_mode](#).

(7) `uint32_t ppx_dither_config_t::quantBitNum`

(8) `uint32_t ppx_dither_config_t::lutMode`

This must be set to `kPXP_DitherLutOff` if any dither engine uses `kPXP_DitherOrdered` mode.

(9) `uint32_t ppx_dither_config_t::idxMatrixSize0`

(10) `uint32_t ppx_dither_config_t::idxMatrixSize1`

(11) `uint32_t ppx_dither_config_t::idxMatrixSize2`

(12) `uint32_t ppx_dither_config_t::enableFinalLut`

### 37.3.8 struct ppx\_porter\_duff\_config\_t

#### Data Fields

- `uint32_t enable`: 1  
*Enable or disable Porter Duff.*
- `uint32_t srcFactorMode`: 2  
*Source layer (or AS, s1) factor mode, see [ppx\\_porter\\_duff\\_factor\\_mode](#).*
- `uint32_t dstGlobalAlphaMode`: 2  
*Destination layer (or PS, s0) global alpha mode, see [ppx\\_porter\\_duff\\_global\\_alpha\\_mode](#).*
- `uint32_t dstAlphaMode`: 1  
*Destination layer (or PS, s0) alpha mode, see [ppx\\_porter\\_duff\\_alpha\\_mode](#).*
- `uint32_t dstColorMode`: 1  
*Destination layer (or PS, s0) color mode, see [ppx\\_porter\\_duff\\_color\\_mode](#).*
- `uint32_t dstFactorMode`: 2  
*Destination layer (or PS, s0) factor mode, see [ppx\\_porter\\_duff\\_factor\\_mode](#).*
- `uint32_t srcGlobalAlphaMode`: 2  
*Source layer (or AS, s1) global alpha mode, see [ppx\\_porter\\_duff\\_global\\_alpha\\_mode](#).*
- `uint32_t srcAlphaMode`: 1  
*Source layer (or AS, s1) alpha mode, see [ppx\\_porter\\_duff\\_alpha\\_mode](#).*
- `uint32_t srcColorMode`: 1  
*Source layer (or AS, s1) color mode, see [ppx\\_porter\\_duff\\_color\\_mode](#).*
- `uint32_t dstGlobalAlpha`: 8  
*Destination layer (or PS, s0) global alpha value, 0~255.*
- `uint32_t srcGlobalAlpha`: 8  
*Source layer (or AS, s1) global alpha value, 0~255.*

## Field Documentation

- (1) `uint32_t ppx_porter_duff_config_t::enable`
- (2) `uint32_t ppx_porter_duff_config_t::srcFactorMode`
- (3) `uint32_t ppx_porter_duff_config_t::dstGlobalAlphaMode`
- (4) `uint32_t ppx_porter_duff_config_t::dstAlphaMode`
- (5) `uint32_t ppx_porter_duff_config_t::dstColorMode`
- (6) `uint32_t ppx_porter_duff_config_t::dstFactorMode`
- (7) `uint32_t ppx_porter_duff_config_t::srcGlobalAlphaMode`
- (8) `uint32_t ppx_porter_duff_config_t::srcAlphaMode`
- (9) `uint32_t ppx_porter_duff_config_t::srcColorMode`
- (10) `uint32_t ppx_porter_duff_config_t::dstGlobalAlpha`
- (11) `uint32_t ppx_porter_duff_config_t::srcGlobalAlpha`

### 37.3.9 struct ppx\_pic\_copy\_config\_t

Note: don't change the enum item value

## Data Fields

- `uint32_t srcPicBaseAddr`  
*Source picture base address.*
- `uint16_t srcPitchBytes`  
*Pitch of the source buffer.*
- `uint16_t srcOffsetX`  
*Copy position in source picture.*
- `uint16_t srcOffsetY`  
*Copy position in source picture.*
- `uint32_t destPicBaseAddr`  
*Destination picture base address.*
- `uint16_t destPitchBytes`  
*Pitch of the destination buffer.*
- `uint16_t destOffsetX`  
*Copy position in destination picture.*
- `uint16_t destOffsetY`  
*Copy position in destination picture.*
- `uint16_t width`  
*Pixel number each line to copy.*
- `uint16_t height`

- *Lines to copy.*
- `pxp_as_pixel_format_t pixelFormat`  
*Buffer pixel format.*

### Field Documentation

- (1) `uint32_t ppx_pic_copy_config_t::srcPicBaseAddr`
- (2) `uint16_t ppx_pic_copy_config_t::srcPitchBytes`
- (3) `uint16_t ppx_pic_copy_config_t::srcOffsetX`
- (4) `uint16_t ppx_pic_copy_config_t::srcOffsetY`
- (5) `uint32_t ppx_pic_copy_config_t::destPicBaseAddr`
- (6) `uint16_t ppx_pic_copy_config_t::destPitchBytes`
- (7) `uint16_t ppx_pic_copy_config_t::destOffsetX`
- (8) `uint16_t ppx_pic_copy_config_t::destOffsetY`
- (9) `uint16_t ppx_pic_copy_config_t::width`
- (10) `uint16_t ppx_pic_copy_config_t::height`
- (11) `pxp_as_pixel_format_t ppx_pic_copy_config_t::pixelFormat`

## 37.4 Enumeration Type Documentation

### 37.4.1 enum \_pxp\_interrupt\_enable

Enumerator

`kPXP_CompleteInterruptEnable` PXP process completed. bit 1

`kPXP_CommandLoadInterruptEnable` Interrupt to show that the command set by [PXP\\_SetNext-Command](#) has been loaded. bit 2

### 37.4.2 enum \_pxp\_flags

Note

These enumerations are meant to be OR'd together to form a bit mask.

Enumerator

`kPXP_CompleteFlag` PXP process completed. bit 0

`kPXP_Axi0WriteErrorFlag` PXP encountered an AXI write error and processing has been terminated. bit 1

***kPXP\_Axi0ReadErrorFlag*** PXP encountered an AXI read error and processing has been terminated. bit 2

***kPXP\_CommandLoadFlag*** The command set by [PXP\\_SetNextCommand](#) has been loaded, could set new command. bit 3

### 37.4.3 enum pxp\_flip\_mode\_t

Enumerator

***kPXP\_FlipDisable*** Flip disable.

***kPXP\_FlipHorizontal*** Horizontal flip.

***kPXP\_FlipVertical*** Vertical flip.

***kPXP\_FlipBoth*** Flip both directions.

### 37.4.4 enum pxp\_rotate\_position\_t

Enumerator

***kPXP\_RotateOutputBuffer*** Rotate the output buffer.

***kPXP\_RotateProcessSurface*** Rotate the process surface.

### 37.4.5 enum pxp\_rotate\_degree\_t

Enumerator

***kPXP\_Rotate0*** Clock wise rotate 0 deg.

***kPXP\_Rotate90*** Clock wise rotate 90 deg.

***kPXP\_Rotate180*** Clock wise rotate 180 deg.

***kPXP\_Rotate270*** Clock wise rotate 270 deg.

### 37.4.6 enum pxp\_interlaced\_output\_mode\_t

Enumerator

***kPXP\_OutputProgressive*** All data written in progressive format to output buffer 0.

***kPXP\_OutputField0*** Only write field 0 data to output buffer 0.

***kPXP\_OutputField1*** Only write field 1 data to output buffer 0.

***kPXP\_OutputInterlaced*** Field 0 write to buffer 0, field 1 write to buffer 1.

### 37.4.7 enum ppx\_output\_pixel\_format\_t

Enumerator

*kPXP\_OutputPixelFormatARGB8888* 32-bit pixels with alpha.  
*kPXP\_OutputPixelFormatRGB888* 32-bit pixels without alpha (unpacked 24-bit format)  
*kPXP\_OutputPixelFormatRGB888P* 24-bit pixels without alpha (packed 24-bit format)  
*kPXP\_OutputPixelFormatARGB1555* 16-bit pixels with alpha.  
*kPXP\_OutputPixelFormatARGB4444* 16-bit pixels with alpha.  
*kPXP\_OutputPixelFormatRGB555* 16-bit pixels without alpha.  
*kPXP\_OutputPixelFormatRGB444* 16-bit pixels without alpha.  
*kPXP\_OutputPixelFormatRGB565* 16-bit pixels without alpha.  
*kPXP\_OutputPixelFormatYUV1P444* 32-bit pixels (1-plane XYUV unpacked).  
*kPXP\_OutputPixelFormatUYVY1P422* 16-bit pixels (1-plane U0,Y0,V0,Y1 interleaved bytes)  
*kPXP\_OutputPixelFormatVYUY1P422* 16-bit pixels (1-plane V0,Y0,U0,Y1 interleaved bytes)  
*kPXP\_OutputPixelFormatY8* 8-bit monochrome pixels (1-plane Y luma output)  
*kPXP\_OutputPixelFormatY4* 4-bit monochrome pixels (1-plane Y luma, 4 bit truncation)  
*kPXP\_OutputPixelFormatYUV2P422* 16-bit pixels (2-plane UV interleaved bytes)  
*kPXP\_OutputPixelFormatYUV2P420* 16-bit pixels (2-plane UV)  
*kPXP\_OutputPixelFormatYVU2P422* 16-bit pixels (2-plane VU interleaved bytes)  
*kPXP\_OutputPixelFormatYVU2P420* 16-bit pixels (2-plane VU)

### 37.4.8 enum ppx\_ps\_pixel\_format\_t

Enumerator

*kPXP\_PsPixelFormatARGB8888* 32-bit pixels with alpha(when participates in blend with alpha surface uses pixel format that has alpha value) or without alpha (unpacked 24-bit format)  
*kPXP\_PsPixelFormatARGB1555* 16-bit pixels with alpha(when participates in blend with alpha surface uses pixel format that has alpha value) or without alpha.  
*kPXP\_PsPixelFormatARGB4444* 16-bit pixels with alpha(when participates in blend with alpha surface uses pixel format that has alpha value) or without alpha.  
*kPXP\_PsPixelFormatRGB565* 16-bit pixels without alpha.  
*kPXP\_PsPixelFormatYUV1P444* 32-bit pixels (1-plane XYUV unpacked).  
*kPXP\_PsPixelFormatUYVY1P422* 16-bit pixels (1-plane U0,Y0,V0,Y1 interleaved bytes)  
*kPXP\_PsPixelFormatVYUY1P422* 16-bit pixels (1-plane V0,Y0,U0,Y1 interleaved bytes)  
*kPXP\_PsPixelFormatY8* 8-bit monochrome pixels (1-plane Y luma output)  
*kPXP\_PsPixelFormatY4* 4-bit monochrome pixels (1-plane Y luma, 4 bit truncation)  
*kPXP\_PsPixelFormatYUV2P422* 16-bit pixels (2-plane UV interleaved bytes)  
*kPXP\_PsPixelFormatYUV2P420* 16-bit pixels (2-plane UV)  
*kPXP\_PsPixelFormatYVU2P422* 16-bit pixels (2-plane VU interleaved bytes)  
*kPXP\_PsPixelFormatYVU2P420* 16-bit pixels (2-plane VU)  
*kPXP\_PsPixelFormatYVU422* 16-bit pixels (3-plane)  
*kPXP\_PsPixelFormatYVU420* 16-bit pixels (3-plane)

***kPXP\_PsPixelFormatRGBA8888*** 32-bit pixels with alpha at low 8-bit  
***kPXP\_PsPixelFormatRGBA5551*** 16-bit pixels with alpha at low 1-bit.  
***kPXP\_PsPixelFormatRGBA4444*** 16-bit pixels with alpha at low 4-bit.

### 37.4.9 enum pxp\_ps\_yuv\_format\_t

Enumerator

***kPXP\_PsYUVFormatYUV*** YUV format.  
***kPXP\_PsYUVFormatYCbCr*** YCbCr format.

### 37.4.10 enum pxp\_as\_pixel\_format\_t

Enumerator

***kPXP\_AsPixelFormatARGB8888*** 32-bit pixels with alpha.  
***kPXP\_AsPixelFormatRGB888*** 32-bit pixels without alpha (unpacked 24-bit format)  
***kPXP\_AsPixelFormatARGB1555*** 16-bit pixels with alpha.  
***kPXP\_AsPixelFormatARGB4444*** 16-bit pixels with alpha.  
***kPXP\_AsPixelFormatRGB555*** 16-bit pixels without alpha.  
***kPXP\_AsPixelFormatRGB444*** 16-bit pixels without alpha.  
***kPXP\_AsPixelFormatRGB565*** 16-bit pixels without alpha.  
***kPXP\_AsPixelFormatRGBA8888*** 32-bit pixels with alpha at low 8-bit.  
***kPXP\_AsPixelFormatRGBA5551*** 16-bit pixels with alpha at low 1-bit.  
***kPXP\_AsPixelFormatRGBA4444*** 16-bit pixels with alpha at low 4-bit.

### 37.4.11 enum pxp\_alpha\_mode\_t

Enumerator

***kPXP\_AlphaEmbedded*** The alpha surface pixel alpha value will be used for blend.  
***kPXP\_AlphaOverride*** The user defined alpha value will be used for blend directly.  
***kPXP\_AlphaMultiply*** The alpha surface pixel alpha value scaled the user defined alpha value will be used for blend, for example, pixel alpha set to 200, user defined alpha set to 100, then the result alpha is  $200 * 100 / 255$ .  
***kPXP\_AlphaRop*** Raster operation.

### 37.4.12 enum pxp\_rop\_mode\_t

Explanation:

- AS: Alpha surface
- PS: Process surface
- nAS: Alpha surface NOT value
- nPS: Process surface NOT value

Enumerator

*kPXP\_RopMaskAs* AS AND PS.  
*kPXP\_RopMaskNotAs* nAS AND PS.  
*kPXP\_RopMaskAsNot* AS AND nPS.  
*kPXP\_RopMergeAs* AS OR PS.  
*kPXP\_RopMergeNotAs* nAS OR PS.  
*kPXP\_RopMergeAsNot* AS OR nPS.  
*kPXP\_RopNotCopyAs* nAS.  
*kPXP\_RopNot* nPS.  
*kPXP\_RopNotMaskAs* AS NAND PS.  
*kPXP\_RopNotMergeAs* AS NOR PS.  
*kPXP\_RopXorAs* AS XOR PS.  
*kPXP\_RopNotXorAs* AS XNOR PS.

### 37.4.13 enum pxp\_block\_size\_t

Enumerator

*kPXP\_BlockSize8* Process 8x8 pixel blocks.  
*kPXP\_BlockSize16* Process 16x16 pixel blocks.

### 37.4.14 enum pxp\_csc1\_mode\_t

Enumerator

*kPXP\_Csc1YUV2RGB* YUV to RGB.  
*kPXP\_Csc1YCbCr2RGB* YCbCr to RGB.

### 37.4.15 enum pxp\_csc2\_mode\_t

Enumerator

*kPXP\_Csc2YUV2RGB* YUV to RGB.  
*kPXP\_Csc2YCbCr2RGB* YCbCr to RGB.  
*kPXP\_Csc2RGB2YUV* RGB to YUV.  
*kPXP\_Csc2RGB2YCbCr* RGB to YCbCr.

### 37.4.16 enum pxp\_ram\_t

Enumerator

*kPXP\_RamDither0Lut* Dither 0 LUT memory.

*kPXP\_RamDither1Lut* Dither 1 LUT memory.

*kPXP\_RamDither2Lut* Dither 2 LUT memory.

### 37.4.17 enum \_pxp\_dither\_mode

Enumerator

*kPXP\_DitherPassThrough* Pass through, no dither.

*kPXP\_DitherFloydSteinberg* Floyd-Steinberg. For dither engine 0 only.

*kPXP\_DitherAtkinson* Atkinson. For dither engine 0 only.

*kPXP\_DitherOrdered* Ordered dither.

*kPXP\_DitherQuantOnly* No dithering, only quantization.

*kPXP\_DitherSierra* Sierra. For dither engine 0 only.

### 37.4.18 enum \_pxp\_dither\_lut\_mode

Enumerator

*kPXP\_DitherLutOff* The LUT memory is not used for LUT, could be used as ordered dither index matrix.

*kPXP\_DitherLutPreDither* Use LUT at the pre-dither stage, The pre-dither LUT could only be used in Floyd mode or Atkinson mode, which are not supported by current PXP module.

*kPXP\_DitherLutPostDither* Use LUT at the post-dither stage.

### 37.4.19 enum \_pxp\_dither\_matrix\_size

Enumerator

*kPXP\_DitherMatrix4* The dither index matrix is 4x4.

*kPXP\_DitherMatrix8* The dither index matrix is 8x8.

*kPXP\_DitherMatrix16* The dither index matrix is 16x16.

### 37.4.20 anonymous enum

Enumerator

*kPXP\_PorterDuffFactorOne* Use 1.

*kPXP\_PorterDuffFactorZero* Use 0.  
*kPXP\_PorterDuffFactorStraight* Use straight alpha.  
*kPXP\_PorterDuffFactorInversed* Use inversed alpha.

### 37.4.21 anonymous enum

Enumerator

*kPXP\_PorterDuffGlobalAlpha* Use global alpha.  
*kPXP\_PorterDuffLocalAlpha* Use local alpha in each pixel.  
*kPXP\_PorterDuffScaledAlpha* Use global alpha \* local alpha.

### 37.4.22 anonymous enum

Enumerator

*kPXP\_PorterDuffAlphaStraight* Use straight alpha,  $s0\_alpha' = s0\_alpha$ .  
*kPXP\_PorterDuffAlphaInversed* Use inversed alpha,  $s0\_alpha' = 0xFF - s0\_alpha$ .

### 37.4.23 anonymous enum

Enumerator

*kPXP\_PorterDuffColorStraight* **Deprecated** Use *kPXP\_PorterDuffColorNoAlpha*.  
*kPXP\_PorterDuffColorInversed* **Deprecated** Use *kPXP\_PorterDuffColorWithAlpha*.  
*kPXP\_PorterDuffColorNoAlpha*  $s0\_pixel' = s0\_pixel$ .  
*kPXP\_PorterDuffColorWithAlpha*  $s0\_pixel' = s0\_pixel * s0\_alpha''$ .

### 37.4.24 enum pxp\_porter\_duff\_blend\_mode\_t

Note: don't change the enum item value

Enumerator

*kPXP\_PorterDuffSrc* Source Only.  
*kPXP\_PorterDuffAtop* Source Atop.  
*kPXP\_PorterDuffOver* Source Over.  
*kPXP\_PorterDuffIn* Source In.  
*kPXP\_PorterDuffOut* Source Out.  
*kPXP\_PorterDuffDst* Destination Only.  
*kPXP\_PorterDuffDstAtop* Destination Atop.  
*kPXP\_PorterDuffDstOver* Destination Over.  
*kPXP\_PorterDuffDstIn* Destination In.

*kPXP\_PorterDuffDstOut* Destination Out.  
*kPXP\_PorterDuffXor* XOR.  
*kPXP\_PorterDuffClear* Clear.

## 37.5 Function Documentation

### 37.5.1 void PXP\_Init ( PXP\_Type \* *base* )

This function enables the PXP peripheral clock, and resets the PXP registers to default status.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
|-------------|------------------------------|

### 37.5.2 void PXP\_Deinit ( PXP\_Type \* *base* )

This function disables the PXP peripheral clock.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
|-------------|------------------------------|

### 37.5.3 void PXP\_Reset ( PXP\_Type \* *base* )

This function resets the PXP peripheral registers to default status.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
|-------------|------------------------------|

### 37.5.4 void PXP\_ResetControl ( PXP\_Type \* *base* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
|-------------|------------------------------|

### 37.5.5 static void PXP\_Start ( PXP\_Type \* *base* ) [inline], [static]

Start PXP process using current configuration.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
|-------------|------------------------------|

### 37.5.6 static void PXP\_EnableLcdHandShake ( PXP\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | PXP peripheral base address.      |
| <i>enable</i> | True to enable, false to disable. |

### 37.5.7 static void PXP\_EnableContinousRun ( PXP\_Type \* *base*, bool *enable* ) [inline], [static]

If continous run not enabled, [PXP\\_Start](#) starts the PXP process. When completed, PXP enters idle mode and flag [kPXP\\_CompleteFlag](#) asserts.

If continous run enabled, the PXP will repeat based on the current configuration register settings.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | PXP peripheral base address.      |
| <i>enable</i> | True to enable, false to disable. |

### 37.5.8 static void PXP\_SetProcessBlockSize ( PXP\_Type \* *base*, pxp\_block\_size\_t *size* ) [inline], [static]

This function chooses the pixel block size that PXP using during process. Larger block size means better performace, but be careful that when PXP is rotating, the output must be divisible by the block size selected.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
|-------------|------------------------------|

|             |                       |
|-------------|-----------------------|
| <i>size</i> | The pixel block size. |
|-------------|-----------------------|

### 37.5.9 static uint32\_t PXP\_GetStatusFlags ( PXP\_Type \* *base* ) [inline], [static]

This function gets all PXP status flags. The flags are returned as the logical OR value of the enumerators [\\_pxp\\_flags](#). To check a specific status, compare the return value with enumerators in [\\_pxp\\_flags](#). For example, to check whether the PXP has completed process, use like this:

```
if (kPXP_CompleteFlag & PXP_GetStatusFlags (PXP))
{
    ...
}
```

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
|-------------|------------------------------|

Returns

PXP status flags which are OR'ed by the enumerators in the [\\_pxp\\_flags](#).

### 37.5.10 static void PXP\_ClearStatusFlags ( PXP\_Type \* *base*, uint32\_t *statusMask* ) [inline], [static]

This function clears PXP status flags with a provided mask.

Parameters

|                   |                                                                                        |
|-------------------|----------------------------------------------------------------------------------------|
| <i>base</i>       | PXP peripheral base address.                                                           |
| <i>statusMask</i> | The status flags to be cleared; it is logical OR value of <a href="#">_pxp_flags</a> . |

### 37.5.11 static uint8\_t PXP\_GetAxiErrorId ( PXP\_Type \* *base*, uint8\_t *axilIndex* ) [inline], [static]

Parameters

|                 |                                                                                                  |
|-----------------|--------------------------------------------------------------------------------------------------|
| <i>base</i>     | PXP peripheral base address.                                                                     |
| <i>axiIndex</i> | Whitch AXI to get <ul style="list-style-type: none"> <li>• 0: AXI0</li> <li>• 1: AXI1</li> </ul> |

Returns

The AXI ID of the failing bus operation.

### 37.5.12 static void PXP\_EnableInterrupts ( **PXP\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

This function enables the PXP interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [\\_pxp\\_interrupt\\_enable](#). For example, to enable PXP process complete interrupt and command loaded interrupt, do the following.

```
PXP_EnableInterrupts(PXP, kPXP_CommandLoadInterruptEnable  
| kPXP_CompleteInterruptEnable);
```

Parameters

|             |                                                                                 |
|-------------|---------------------------------------------------------------------------------|
| <i>base</i> | PXP peripheral base address.                                                    |
| <i>mask</i> | The interrupts to enable. Logical OR of <a href="#">_pxp_interrupt_enable</a> . |

### 37.5.13 static void PXP\_DisableInterrupts ( **PXP\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

This function disables the PXP interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [\\_pxp\\_interrupt\\_enable](#).

Parameters

|             |                                                                                  |
|-------------|----------------------------------------------------------------------------------|
| <i>base</i> | PXP peripheral base address.                                                     |
| <i>mask</i> | The interrupts to disable. Logical OR of <a href="#">_pxp_interrupt_enable</a> . |

### 37.5.14 void PXP\_SetAlphaSurfaceBufferConfig ( **PXP\_Type** \* *base*, **const** **pxp\_as\_buffer\_config\_t** \* *config* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | PXP peripheral base address.  |
| <i>config</i> | Pointer to the configuration. |

### 37.5.15 void PXP\_SetAlphaSurfaceBlendConfig ( PXP\_Type \* *base*, const ppx\_as\_blend\_config\_t \* *config* )

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | PXP peripheral base address.            |
| <i>config</i> | Pointer to the configuration structure. |

### 37.5.16 void PXP\_SetAlphaSurfaceOverlayColorKey ( PXP\_Type \* *base*, uint32\_t *colorKeyLow*, uint32\_t *colorKeyHigh* )

If a pixel in the current overlay image with a color that falls in the range from the *colorKeyLow* to *colorKeyHigh* range, it will use the process surface pixel value for that location. If no PS image is present or if the PS image also matches its colorkey range, the PS background color is used.

Parameters

|                     |                              |
|---------------------|------------------------------|
| <i>base</i>         | PXP peripheral base address. |
| <i>colorKeyLow</i>  | Color key low range.         |
| <i>colorKeyHigh</i> | Color key high range.        |

Note

Colorkey operations are higher priority than alpha or ROP operations

### 37.5.17 static void PXP\_EnableAlphaSurfaceOverlayColorKey ( PXP\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | PXP peripheral base address.      |
| <i>enable</i> | True to enable, false to disable. |

**37.5.18 void PXP\_SetAlphaSurfacePosition ( PXP\_Type \* *base*, uint16\_t *upperLeftX*, uint16\_t *upperLeftY*, uint16\_t *lowerRightX*, uint16\_t *lowerRightY* )**

Parameters

|                    |                              |
|--------------------|------------------------------|
| <i>base</i>        | PXP peripheral base address. |
| <i>upperLeftX</i>  | X of the upper left corner.  |
| <i>upperLeftY</i>  | Y of the upper left corner.  |
| <i>lowerRightX</i> | X of the lower right corner. |
| <i>lowerRightY</i> | Y of the lower right corner. |

**37.5.19 static void PXP\_SetProcessSurfaceBackGroundColor ( PXP\_Type \* *base*, uint32\_t *backGroundColor* ) [inline], [static]**

Parameters

|                         |                                      |
|-------------------------|--------------------------------------|
| <i>base</i>             | PXP peripheral base address.         |
| <i>backGround-Color</i> | Pixel value of the background color. |

**37.5.20 void PXP\_SetProcessSurfaceBufferConfig ( PXP\_Type \* *base*, const ppx\_p\_s\_buffer\_config\_t \* *config* )**

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | PXP peripheral base address.  |
| <i>config</i> | Pointer to the configuration. |

37.5.21 **void PXP\_SetProcessSurfaceScaler ( PXP\_Type \* *base*, uint16\_t *inputWidth*, uint16\_t *inputHeight*, uint16\_t *outputWidth*, uint16\_t *outputHeight* )**

The valid down scale fact is  $1/(2^{12}) \sim 16$ .

Parameters

|                     |                              |
|---------------------|------------------------------|
| <i>base</i>         | PXP peripheral base address. |
| <i>inputWidth</i>   | Input image width.           |
| <i>inputHeight</i>  | Input image height.          |
| <i>outputWidth</i>  | Output image width.          |
| <i>outputHeight</i> | Output image height.         |

**37.5.22 void PXP\_SetProcessSurfacePosition ( PXP\_Type \* *base*, uint16\_t *upperLeftX*, uint16\_t *upperLeftY*, uint16\_t *lowerRightX*, uint16\_t *lowerRightY* )**

Parameters

|                    |                              |
|--------------------|------------------------------|
| <i>base</i>        | PXP peripheral base address. |
| <i>upperLeftX</i>  | X of the upper left corner.  |
| <i>upperLeftY</i>  | Y of the upper left corner.  |
| <i>lowerRightX</i> | X of the lower right corner. |
| <i>lowerRightY</i> | Y of the lower right corner. |

**37.5.23 void PXP\_SetProcessSurfaceColorKey ( PXP\_Type \* *base*, uint32\_t *colorKeyLow*, uint32\_t *colorKeyHigh* )**

If the PS image matches colorkey range, the PS background color is output. Set *colorKeyLow* to 0xFF and *colorKeyHigh* to 0 will disable the colorkeying.

Parameters

|                     |                              |
|---------------------|------------------------------|
| <i>base</i>         | PXP peripheral base address. |
| <i>colorKeyLow</i>  | Color key low range.         |
| <i>colorKeyHigh</i> | Color key high range.        |

### 37.5.24 static void PXP\_SetProcessSurfaceYUVFormat ( **PXP\_Type** \* *base*, **pxp\_ps\_yuv\_format\_t** *format* ) [inline], [static]

If process surface input pixel format is YUV and CSC1 is not enabled, in other words, the process surface output pixel format is also YUV, then this function should be called to set whether input pixel format is YUV or YCbCr.

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | PXP peripheral base address. |
| <i>format</i> | The YUV format.              |

### 37.5.25 void PXP\_SetOutputBufferConfig ( **PXP\_Type** \* *base*, const **pxp\_output\_buffer\_config\_t** \* *config* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | PXP peripheral base address.  |
| <i>config</i> | Pointer to the configuration. |

### 37.5.26 static void PXP\_SetOverwrittenAlphaValue ( **PXP\_Type** \* *base*, **uint8\_t** *alpha* ) [inline], [static]

If global overwritten alpha is enabled, the alpha component in output buffer pixels will be overwritten, otherwise the computed alpha value is used.

Parameters

|              |                              |
|--------------|------------------------------|
| <i>base</i>  | PXP peripheral base address. |
| <i>alpha</i> | The alpha value.             |

### 37.5.27 static void PXP\_EnableOverWrittenAlpha ( **PXP\_Type** \* *base*, **bool** *enable* ) [inline], [static]

If global overwritten alpha is enabled, the alpha component in output buffer pixels will be overwritten, otherwise the computed alpha value is used.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | PXP peripheral base address.      |
| <i>enable</i> | True to enable, false to disable. |

**37.5.28 static void PXP\_SetRotateConfig ( PXP\_Type \* *base*, ppx\_rotate\_position\_t *position*, ppx\_rotate\_degree\_t *degree*, ppx\_flip\_mode\_t *flipMode* ) [inline], [static]**

The PXP could rotate the process surface or the output buffer. There are two PXP versions:

- Version 1: Only has one rotate sub module, the output buffer and process surface share the same rotate sub module, which means the process surface and output buffer could not be rotate at the same time. When pass in [kPXP\\_RotateOutputBuffer](#), the process surface could not use the rotate, Also when pass in [kPXP\\_RotateProcessSurface](#), output buffer could not use the rotate.
- Version 2: Has two separate rotate sub modules, the output buffer and process surface could configure the rotation independently.

Upper layer could use the macro PXP\_SHARE\_ROTATE to check which version is. PXP\_SHARE\_ROTATE=1 means version 1.

Parameters

|                 |                                          |
|-----------------|------------------------------------------|
| <i>base</i>     | PXP peripheral base address.             |
| <i>position</i> | Rotate process surface or output buffer. |
| <i>degree</i>   | Rotate degree.                           |
| <i>flipMode</i> | Flip mode.                               |

Note

This function is different depends on the macro PXP\_SHARE\_ROTATE.

**37.5.29 void PXP\_BuildRect ( PXP\_Type \* *base*, ppx\_output\_pixel\_format\_t *outFormat*, uint32\_t *value*, uint16\_t *width*, uint16\_t *height*, uint16\_t *pitch*, uint32\_t *outAddr* )**

## Parameters

|                  |                                                                          |
|------------------|--------------------------------------------------------------------------|
| <i>base</i>      | PXP peripheral base address.                                             |
| <i>outFormat</i> | output pixel format.                                                     |
| <i>value</i>     | The value of the pixel to be filled in the rectangle in ARGB8888 format. |
| <i>width</i>     | width of the rectangle.                                                  |
| <i>height</i>    | height of the rectangle.                                                 |
| <i>pitch</i>     | output pitch in byte.                                                    |
| <i>outAddr</i>   | address of the memory to store the rectangle.                            |

**37.5.30 void PXP\_SetNextCommand ( PXP\_Type \* *base*, void \* *commandAddr* )**

The PXP supports a primitive ability to queue up one operation while the current operation is running. Workflow:

1. Prepare the PXP register values except STAT, CSCCOEFn, NEXT in the memory in the order they appear in the register map.
2. Call this function sets the new operation to PXP.
3. There are two methods to check whether the PXP has loaded the new operation. The first method is using [PXP\\_IsNextCommandPending](#). If there is new operation not loaded by the PXP, this function returns true. The second method is checking the flag [kPXP\\_CommandLoadFlag](#), if command loaded, this flag asserts. User could enable interrupt [kPXP\\_CommandLoadInterruptEnable](#) to get the loaded signal in interrupt way.
4. When command loaded by PXP, a new command could be set using this function.

```

uint32_t ppx_command1[48];
uint32_t ppx_command2[48];

ppx_command1[0] = ...;
ppx_command1[1] = ...;
...
ppx_command2[0] = ...;
ppx_command2[1] = ...;
...

while (PXP_IsNextCommandPending(PXP))
{
}

PXP_SetNextCommand(PXP, ppx_command1);

while (PXP_IsNextCommandPending(PXP))
{
}

PXP_SetNextCommand(PXP, ppx_command2);

```

Parameters

|                    |                              |
|--------------------|------------------------------|
| <i>base</i>        | PXP peripheral base address. |
| <i>commandAddr</i> | Address of the new command.  |

### 37.5.31 static bool PXP\_IsNextCommandPending ( PXP\_Type \* *base* ) [inline], [static]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

Returns

True is pending, false is not.

### 37.5.32 static void PXP\_CancelNextCommand ( PXP\_Type \* *base* ) [inline], [static]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

### 37.5.33 void PXP\_SetCsc1Mode ( PXP\_Type \* *base*, pxp\_csc1\_mode\_t *mode* )

The CSC1 module receives scaled YUV/YCbCr444 pixels from the scale engine and converts the pixels to the RGB888 color space. It could only be used by process surface.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | PXP peripheral base address. |
| <i>mode</i> | The conversion mode.         |

### 37.5.34 static void PXP\_EnableCsc1 ( PXP\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | PXP peripheral base address.      |
| <i>enable</i> | True to enable, false to disable. |

### 37.5.35 void PXP\_SetPorterDuffConfig ( PXP\_Type \* *base*, const ppx\_porter\_duff\_config\_t \* *config* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | PXP peripheral base address.  |
| <i>config</i> | Pointer to the configuration. |

### 37.5.36 status\_t PXP\_GetPorterDuffConfigExt ( ppx\_porter\_duff\_blend\_mode\_t *mode*, ppx\_porter\_duff\_config\_t \* *config*, uint8\_t *dstGlobalAlphaMode*, uint8\_t *dstAlphaMode*, uint8\_t *dstColorMode*, uint8\_t *srcGlobalAlphaMode*, uint8\_t *srcAlphaMode*, uint8\_t *srcColorMode*, uint8\_t *dstGlobalAlpha*, uint8\_t *srcGlobalAlpha* )

The FactorMode are selected based on blend mode, the other values are set based on input parameters. These values could be modified after calling this function. This function is extened [PXP\\_SetPorterDuffConfig](#).

Parameters

|                           |                                                                                                        |
|---------------------------|--------------------------------------------------------------------------------------------------------|
| <i>mode</i>               | The blend mode.                                                                                        |
| <i>config</i>             | Pointer to the configuration.                                                                          |
| <i>dstGlobalAlphaMode</i> | Destination layer (or PS, s0) global alpha mode, see <a href="#">ppx_porter_duff_global_alpha_mode</a> |
| <i>dstAlphaMode</i>       | Destination layer (or PS, s0) alpha mode, see <a href="#">ppx_porter_duff_alpha_mode</a> .             |
| <i>dstColorMode</i>       | Destination layer (or PS, s0) color mode, see <a href="#">ppx_porter_duff_color_mode</a> .             |
| <i>srcGlobalAlphaMode</i> | Source layer (or AS, s1) global alpha mode, see <a href="#">ppx_porter_duff_global_alpha_mode</a>      |

|                       |                                                                                       |
|-----------------------|---------------------------------------------------------------------------------------|
| <i>srcAlphaMode</i>   | Source layer (or AS, s1) alpha mode, see <a href="#">pxp_porter_duff_alpha_mode</a> . |
| <i>srcColorMode</i>   | Source layer (or AS, s1) color mode, see <a href="#">pxp_porter_duff_color_mode</a> . |
| <i>dstGlobalAlpha</i> | Destination layer (or PS, s0) global alpha value, 0~255                               |
| <i>srcGlobalAlpha</i> | Source layer (or AS, s1) global alpha value, 0~255                                    |

Return values

|                                |                                     |
|--------------------------------|-------------------------------------|
| <i>kStatus_Success</i>         | Successfully get the configuratoin. |
| <i>kStatus_InvalidArgument</i> | The blend mode not supported.       |

### 37.5.37 static status\_t PXP\_GetPorterDuffConfig ( pxp\_porter\_duff\_blend\_mode\_t mode, pxp\_porter\_duff\_config\_t \* config ) [inline], [static]

The FactorMode are selected based on blend mode, the AlphaMode are set to [kPXP\\_PorterDuffAlphaStraight](#), the ColorMode are set to [kPXP\\_PorterDuffColorWithAlpha](#), the GlobalAlphaMode are set to [kPXP\\_PorterDuffLocalAlpha](#). These values could be modified after calling this function.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>mode</i>   | The blend mode.               |
| <i>config</i> | Pointer to the configuration. |

Return values

|                                |                                     |
|--------------------------------|-------------------------------------|
| <i>kStatus_Success</i>         | Successfully get the configuratoin. |
| <i>kStatus_InvalidArgument</i> | The blend mode not supported.       |

# Chapter 38

## QTMR: Quad Timer Driver

### 38.1 Overview

The MCUXpresso SDK provides a driver for the QTMR module of MCUXpresso SDK devices.

### Data Structures

- struct `qtmr_config_t`  
*Quad Timer config structure. [More...](#)*

### Enumerations

- enum `qtmr_primary_count_source_t` {  
  `kQTMR_ClockCounter0InputPin` = 0,  
  `kQTMR_ClockCounter1InputPin`,  
  `kQTMR_ClockCounter2InputPin`,  
  `kQTMR_ClockCounter3InputPin`,  
  `kQTMR_ClockCounter0Output`,  
  `kQTMR_ClockCounter1Output`,  
  `kQTMR_ClockCounter2Output`,  
  `kQTMR_ClockCounter3Output`,  
  `kQTMR_ClockDivide_1`,  
  `kQTMR_ClockDivide_2`,  
  `kQTMR_ClockDivide_4`,  
  `kQTMR_ClockDivide_8`,  
  `kQTMR_ClockDivide_16`,  
  `kQTMR_ClockDivide_32`,  
  `kQTMR_ClockDivide_64`,  
  `kQTMR_ClockDivide_128` }  
*Quad Timer primary clock source selection.*
- enum `qtmr_input_source_t` {  
  `kQTMR_Counter0InputPin` = 0,  
  `kQTMR_Counter1InputPin`,  
  `kQTMR_Counter2InputPin`,  
  `kQTMR_Counter3InputPin` }  
*Quad Timer input sources selection.*
- enum `qtmr_counting_mode_t` {

```
kQTMR_NoOperation = 0,
kQTMR_PriSrcRiseEdge,
kQTMR_PriSrcRiseAndFallEdge,
kQTMR_PriSrcRiseEdgeSecInpHigh,
kQTMR_QuadCountMode,
kQTMR_PriSrcRiseEdgeSecDir,
kQTMR_SecSrcTrigPriCnt,
kQTMR_CascadeCount }
```

*Quad Timer counting mode selection.*

- enum `qtmr_pwm_out_state_t` {
 kQTMR\_PwmLow = 0,
 kQTMR\_PwmHigh }

*Quad Timer PWM output state.*

- enum `qtmr_output_mode_t` {
 kQTMR\_AssertWhenCountActive = 0,
 kQTMR\_ClearOnCompare,
 kQTMR\_SetOnCompare,
 kQTMR\_ToggleOnCompare,
 kQTMR\_ToggleOnAltCompareReg,
 kQTMR\_SetOnCompareClearOnSecSrcInp,
 kQTMR\_SetOnCompareClearOnCountRoll,
 kQTMR\_EnableGateClock }

*Quad Timer output mode selection.*

- enum `qtmr_input_capture_edge_t` {
 kQTMR\_NoCapture = 0,
 kQTMR\_RisingEdge,
 kQTMR\_FallingEdge,
 kQTMR\_RisingAndFallingEdge }

*Quad Timer input capture edge mode, rising edge, or falling edge.*

- enum `qtmr_reload_control_t` {
 kQTMR\_NoPreload = 0,
 kQTMR\_LoadOnComp1,
 kQTMR\_LoadOnComp2 }

*Quad Timer input capture edge mode, rising edge, or falling edge.*

- enum `qtmr_debug_action_t` {
 kQTMR\_RunNormalInDebug = 0U,
 kQTMR\_HaltCounter,
 kQTMR\_ForceOutToZero,
 kQTMR\_HaltCountForceOutZero }

*List of Quad Timer run options when in Debug mode.*

- enum `qtmr_interrupt_enable_t` {
 kQTMR\_CompareInterruptEnable = (1U << 0),
 kQTMR\_Compare1InterruptEnable = (1U << 1),
 kQTMR\_Compare2InterruptEnable = (1U << 2),
 kQTMR\_OverflowInterruptEnable = (1U << 3),
 kQTMR\_EdgeInterruptEnable = (1U << 4) }

- *List of Quad Timer interrupts.*
- enum `qtmr_status_flags_t` {
   
    `kQTMR_CompareFlag` = (1U << 0),
   
    `kQTMR_Compare1Flag` = (1U << 1),
   
    `kQTMR_Compare2Flag` = (1U << 2),
   
    `kQTMR_OverflowFlag` = (1U << 3),
   
    `kQTMR_EdgeFlag` = (1U << 4) }
- List of Quad Timer flags.*
- enum `qtmr_channel_selection_t` {
   
    `kQTMR_Channel_0` = 0U,
   
    `kQTMR_Channel_1`,
   
    `kQTMR_Channel_2`,
   
    `kQTMR_Channel_3` }
- List of channel selection.*
- enum `qtmr_dma_enable_t` {
   
    `kQTMR_InputEdgeFlagDmaEnable` = (1U << 0),
   
    `kQTMR_ComparatorPreload1DmaEnable` = (1U << 1),
   
    `kQTMR_ComparatorPreload2DmaEnable` = (1U << 2) }
- List of Quad Timer DMA enable.*

## Functions

- `status_t QTMR_SetupPwm (TMR_Type *base, qtmr_channel_selection_t channel, uint32_t pwmFreqHz, uint8_t dutyCyclePercent, bool outputPolarity, uint32_t srcClock_Hz)`
  
*Sets up Quad timer module for PWM signal output.*
- void `QTMR_SetupInputCapture (TMR_Type *base, qtmr_channel_selection_t channel, qtmr_input_source_t capturePin, bool inputPolarity, bool reloadOnCapture, qtmr_input_capture_edge_t captureMode)`
  
*Allows the user to count the source clock cycles until a capture event arrives.*

## Driver version

- #define `FSL_QTMR_DRIVER_VERSION (MAKE_VERSION(2, 2, 2))`
  
*Version.*

## Initialization and deinitialization

- void `QTMR_Init (TMR_Type *base, qtmr_channel_selection_t channel, const qtmr_config_t *config)`
  
*Ungates the Quad Timer clock and configures the peripheral for basic operation.*
- void `QTMR_Deinit (TMR_Type *base, qtmr_channel_selection_t channel)`
  
*Stops the counter and gates the Quad Timer clock.*
- void `QTMR_GetDefaultConfig (qtmr_config_t *config)`
  
*Fill in the Quad Timer config struct with the default settings.*

## Interrupt Interface

- void `QTMR_EnableInterrupts (TMR_Type *base, qtmr_channel_selection_t channel, uint32_t mask)`

- void `QTMR_DisableInterrupts` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, uint32\_t mask)  
*Enables the selected Quad Timer interrupts.*
- uint32\_t `QTMR_GetEnabledInterrupts` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel)  
*Disables the selected Quad Timer interrupts.*  
*Gets the enabled Quad Timer interrupts.*

## Status Interface

- uint32\_t `QTMR_GetStatus` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel)  
*Gets the Quad Timer status flags.*
- void `QTMR_ClearStatusFlags` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, uint32\_t mask)  
*Clears the Quad Timer status flags.*

## Read and Write the timer period

- void `QTMR_SetTimerPeriod` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, uint16\_t ticks)  
*Sets the timer period in ticks.*
- void `QTMR_SetCompareValue` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, uint16\_t ticks)  
*Set compare value.*
- static void `QTMR_SetLoadValue` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, uint16\_t value)  
*Set load value.*
- static uint16\_t `QTMR_GetCurrentTimerCount` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel)  
*Reads the current timer counting value.*

## Timer Start and Stop

- static void `QTMR_StartTimer` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, qtmr\_counting\_mode\_t clockSource)  
*Starts the Quad Timer counter.*
- static void `QTMR_StopTimer` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel)  
*Stops the Quad Timer counter.*

## Enable and Disable the Quad Timer DMA

- void `QTMR_EnableDma` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, uint32\_t mask)  
*Enable the Quad Timer DMA.*
- void `QTMR_DisableDma` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, uint32\_t mask)  
*Disable the Quad Timer DMA.*
- void `QTMR_SetPwmOutputToIdle` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel, bool idleStatus)  
*Set PWM output in idle status (high or low).*
- static qtmr\_pwm\_out\_state\_t `QTMR_GetPwmOutputStatus` (TMR\_Type \*base, qtmr\_channel\_selection\_t channel)  
*Get the channel output status.*

- `uint8_t QTMR_GetPwmChannelStatus (TMR_Type *base, qtmr_channel_selection_t channel)`  
*Get the PWM channel dutycycle value.*
- `void QTMR_SetPwmClockMode (TMR_Type *base, qtmr_channel_selection_t channel, qtmr_primary_count_source_t prescaler)`  
*This function set the value of the prescaler on QTimer channels.*

## 38.2 Data Structure Documentation

### 38.2.1 struct qtmr\_config\_t

This structure holds the configuration settings for the Quad Timer peripheral. To initialize this structure to reasonable defaults, call the `QTMR_GetDefaultConfig()` function and pass a pointer to your config structure instance.

The config struct can be made const so it resides in flash

### Data Fields

- `qtmr_primary_count_source_t primarySource`  
*Specify the primary count source.*
- `qtmr_input_source_t secondarySource`  
*Specify the secondary count source.*
- `bool enableMasterMode`  
*true: Broadcast compare function output to other counters; false no broadcast*
- `bool enableExternalForce`  
*true: Compare from another counter force state of OFLAG signal false: OFLAG controlled by local counter*
- `uint8_t faultFilterCount`  
*Fault filter count.*
- `uint8_t faultFilterPeriod`  
*Fault filter period; value of 0 will bypass the filter.*
- `qtmr_debug_action_t debugMode`  
*Operation in Debug mode.*

## 38.3 Enumeration Type Documentation

### 38.3.1 enum qtmr\_primary\_count\_source\_t

Enumerator

- |                                          |                          |
|------------------------------------------|--------------------------|
| <code>kQTMR_ClockCounter0InputPin</code> | Use counter 0 input pin. |
| <code>kQTMR_ClockCounter1InputPin</code> | Use counter 1 input pin. |
| <code>kQTMR_ClockCounter2InputPin</code> | Use counter 2 input pin. |
| <code>kQTMR_ClockCounter3InputPin</code> | Use counter 3 input pin. |
| <code>kQTMR_ClockCounter0Output</code>   | Use counter 0 output.    |
| <code>kQTMR_ClockCounter1Output</code>   | Use counter 1 output.    |
| <code>kQTMR_ClockCounter2Output</code>   | Use counter 2 output.    |
| <code>kQTMR_ClockCounter3Output</code>   | Use counter 3 output.    |

*kQTMR\_ClockDivide\_1* IP bus clock divide by 1 prescaler.  
*kQTMR\_ClockDivide\_2* IP bus clock divide by 2 prescaler.  
*kQTMR\_ClockDivide\_4* IP bus clock divide by 4 prescaler.  
*kQTMR\_ClockDivide\_8* IP bus clock divide by 8 prescaler.  
*kQTMR\_ClockDivide\_16* IP bus clock divide by 16 prescaler.  
*kQTMR\_ClockDivide\_32* IP bus clock divide by 32 prescaler.  
*kQTMR\_ClockDivide\_64* IP bus clock divide by 64 prescaler.  
*kQTMR\_ClockDivide\_128* IP bus clock divide by 128 prescaler.

### 38.3.2 enum qtmr\_input\_source\_t

Enumerator

*kQTMR\_Counter0InputPin* Use counter 0 input pin.  
*kQTMR\_Counter1InputPin* Use counter 1 input pin.  
*kQTMR\_Counter2InputPin* Use counter 2 input pin.  
*kQTMR\_Counter3InputPin* Use counter 3 input pin.

### 38.3.3 enum qtmr\_counting\_mode\_t

Enumerator

*kQTMR\_NoOperation* No operation.  
*kQTMR\_PriSrcRiseEdge* Count rising edges of primary source.  
*kQTMR\_PriSrcRiseAndFallEdge* Count rising and falling edges of primary source.  
*kQTMR\_PriSrcRiseEdgeSecInpHigh* Count rise edges of pri SRC while sec inp high active.  
*kQTMR\_QuadCountMode* Quadrature count mode, uses pri and sec sources.  
*kQTMR\_PriSrcRiseEdgeSecDir* Count rising edges of pri SRC; sec SRC specifies dir.  
*kQTMR\_SecSrcTrigPriCnt* Edge of sec SRC trigger primary count until compare.  
*kQTMR\_CascadeCount* Cascaded count mode (up/down)

### 38.3.4 enum qtmr\_pwm\_out\_state\_t

Enumerator

*kQTMR\_PwmLow* The output state of PWM channel is low.  
*kQTMR\_PwmHigh* The output state of PWM channel is low.

### 38.3.5 enum qtmr\_output\_mode\_t

Enumerator

- kQTMR AssertWhenCountActive* Assert OFLAG while counter is active.
- kQTMR ClearOnCompare* Clear OFLAG on successful compare.
- kQTMR SetOnCompare* Set OFLAG on successful compare.
- kQTMR ToggleOnCompare* Toggle OFLAG on successful compare.
- kQTMR ToggleOnAltCompareReg* Toggle OFLAG using alternating compare registers.
- kQTMR SetOnCompareClearOnSecSrcInp* Set OFLAG on compare, clear on sec SRC input edge.
  
- kQTMR SetOnCompareClearOnCountRoll* Set OFLAG on compare, clear on counter rollover.
- kQTMR EnableGateClock* Enable gated clock output while count is active.

### 38.3.6 enum qtmr\_input\_capture\_edge\_t

Enumerator

- kQTMR NoCapture* Capture is disabled.
- kQTMR RisingEdge* Capture on rising edge (IPS=0) or falling edge (IPS=1)
- kQTMR FallingEdge* Capture on falling edge (IPS=0) or rising edge (IPS=1)
- kQTMR RisingAndFallingEdge* Capture on both edges.

### 38.3.7 enum qtmr\_reload\_control\_t

Enumerator

- kQTMR NoPreload* Never preload.
- kQTMR LoadOnComp1* Load upon successful compare with value in COMP1.
- kQTMR LoadOnComp2* Load upon successful compare with value in COMP2.

### 38.3.8 enum qtmr\_debug\_action\_t

Enumerator

- kQTMR RunNormalInDebug* Continue with normal operation.
- kQTMR HaltCounter* Halt counter.
- kQTMR ForceOutToZero* Force output to logic 0.
- kQTMR HaltCountForceOutZero* Halt counter and force output to logic 0.

### 38.3.9 enum qtmr\_interrupt\_enable\_t

Enumerator

*kQTMR\_CompareInterruptEnable* Compare interrupt.  
*kQTMR\_Compare1InterruptEnable* Compare 1 interrupt.  
*kQTMR\_Compare2InterruptEnable* Compare 2 interrupt.  
*kQTMR\_OverflowInterruptEnable* Timer overflow interrupt.  
*kQTMR\_EdgeInterruptEnable* Input edge interrupt.

### 38.3.10 enum qtmr\_status\_flags\_t

Enumerator

*kQTMR\_CompareFlag* Compare flag.  
*kQTMR\_Compare1Flag* Compare 1 flag.  
*kQTMR\_Compare2Flag* Compare 2 flag.  
*kQTMR\_OverflowFlag* Timer overflow flag.  
*kQTMR\_EdgeFlag* Input edge flag.

### 38.3.11 enum qtmr\_channel\_selection\_t

Enumerator

*kQTMR\_Channel\_0* TMR Channel 0.  
*kQTMR\_Channel\_1* TMR Channel 1.  
*kQTMR\_Channel\_2* TMR Channel 2.  
*kQTMR\_Channel\_3* TMR Channel 3.

### 38.3.12 enum qtmr\_dma\_enable\_t

Enumerator

*kQTMR\_InputEdgeFlagDmaEnable* Input Edge Flag DMA Enable.  
*kQTMR\_ComparatorPreload1DmaEnable* Comparator Preload Register 1 DMA Enable.  
*kQTMR\_ComparatorPreload2DmaEnable* Comparator Preload Register 2 DMA Enable.

## 38.4 Function Documentation

### 38.4.1 void QTMR\_Init ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, const qtmr\_config\_t \* *config* )

## Note

This API should be called at the beginning of the application using the Quad Timer driver.

## Parameters

|                |                                               |
|----------------|-----------------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address            |
| <i>channel</i> | Quad Timer channel number                     |
| <i>config</i>  | Pointer to user's Quad Timer config structure |

**38.4.2 void QTMR\_Deinit ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel* )**

## Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |

**38.4.3 void QTMR\_GetDefaultConfig ( qtmr\_config\_t \* *config* )**

The default values are:

```
* config->debugMode = kQTMR_RunNormalInDebug;
* config->enableExternalForce = false;
* config->enableMasterMode = false;
* config->faultFilterCount = 0;
* config->faultFilterPeriod = 0;
* config->primarySource = kQTMR_ClockDivide_2;
* config->secondarySource = kQTMR_Counter0InputPin;
*
```

## Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>config</i> | Pointer to user's Quad Timer config structure. |
|---------------|------------------------------------------------|

**38.4.4 status\_t QTMR\_SetupPwm ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint32\_t *pwmFreqHz*, uint8\_t *dutyCyclePercent*, bool *outputPolarity*, uint32\_t *srcClock\_Hz* )**

The function initializes the timer module according to the parameters passed in by the user. The function also sets up the value compare registers to match the PWM signal requirements.

Parameters

|                          |                                                                                                                           |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>              | Quad Timer peripheral base address                                                                                        |
| <i>channel</i>           | Quad Timer channel number                                                                                                 |
| <i>pwmFreqHz</i>         | PWM signal frequency in Hz                                                                                                |
| <i>dutyCycle-Percent</i> | PWM pulse width, value should be between 0 to 100 0=inactive signal(0% duty cycle)... 100=active signal (100% duty cycle) |
| <i>outputPolarity</i>    | true: invert polarity of the output signal, false: no inversion                                                           |
| <i>srcClock_Hz</i>       | Main counter clock in Hz.                                                                                                 |

Returns

Returns an error if there was error setting up the signal.

### 38.4.5 void QTMR\_SetupInputCapture ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, qtmr\_input\_source\_t *capturePin*, bool *inputPolarity*, bool *reloadOnCapture*, qtmr\_input\_capture\_edge\_t *captureMode* )

The count is stored in the capture register.

Parameters

|                         |                                                                         |
|-------------------------|-------------------------------------------------------------------------|
| <i>base</i>             | Quad Timer peripheral base address                                      |
| <i>channel</i>          | Quad Timer channel number                                               |
| <i>capturePin</i>       | Pin through which we receive the input signal to trigger the capture    |
| <i>inputPolarity</i>    | true: invert polarity of the input signal, false: no inversion          |
| <i>reloadOn-Capture</i> | true: reload the counter when an input capture occurs, false: no reload |
| <i>captureMode</i>      | Specifies which edge of the input signal triggers a capture             |

### 38.4.6 void QTMR\_EnableInterrupts ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint32\_t *mask* )

Parameters

|                |                                                                                                                      |
|----------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address                                                                                   |
| <i>channel</i> | Quad Timer channel number                                                                                            |
| <i>mask</i>    | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">qtmr_interrupt_enable_t</a> |

### 38.4.7 void QTMR\_DisableInterrupts ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint32\_t *mask* )

Parameters

|                |                                                                                                                      |
|----------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address                                                                                   |
| <i>channel</i> | Quad Timer channel number                                                                                            |
| <i>mask</i>    | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">qtmr_interrupt_enable_t</a> |

### 38.4.8 uint32\_t QTMR\_GetEnabledInterrupts ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel* )

Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [qtmr\\_interrupt\\_enable\\_t](#)

### 38.4.9 uint32\_t QTMR\_GetStatus ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel* )

Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |

Returns

The status flags. This is the logical OR of members of the enumeration [qtmr\\_status\\_flags\\_t](#)

### 38.4.10 void QTMR\_ClearStatusFlags ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint32\_t *mask* )

Parameters

|                |                                                                                                                   |
|----------------|-------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address                                                                                |
| <i>channel</i> | Quad Timer channel number                                                                                         |
| <i>mask</i>    | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">qtmr_status_flags_t</a> |

### 38.4.11 void QTMR\_SetTimerPeriod ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint16\_t *ticks* )

Timers counts from initial value till it equals the count value set here. The counter will then reinitialize to the value specified in the Load register.

Note

1. This function will write the time period in ticks to COMP1 or COMP2 register depending on the count direction
2. User can call the utility macros provided in fsl\_common.h to convert to ticks
3. This function supports cases, providing only primary source clock without secondary source clock.

Parameters

---

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |
| <i>ticks</i>   | Timer period in units of ticks     |

### 38.4.12 void QTMR\_SetCompareValue ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint16\_t *ticks* )

This function sets the value used for comparison with the counter value.

Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |
| <i>ticks</i>   | Timer period in units of ticks.    |

### 38.4.13 static void QTMR\_SetLoadValue ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint16\_t *value* ) [inline], [static]

This function sets the value used to initialize the counter after a counter comparison.

Parameters

|                |                                     |
|----------------|-------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address  |
| <i>channel</i> | Quad Timer channel number           |
| <i>value</i>   | Load register initialization value. |

### 38.4.14 static uint16\_t QTMR\_GetCurrentTimerCount ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel* ) [inline], [static]

This function returns the real-time timer counting value, in a range from 0 to a timer period.

Note

User can call the utility macros provided in fsl\_common.h to convert ticks to usec or msec

Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |

Returns

Current counter value in ticks

**38.4.15 static void QTMR\_StartTimer ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, qtmr\_counting\_mode\_t *clockSource* ) [inline], [static]**

Parameters

|                    |                                    |
|--------------------|------------------------------------|
| <i>base</i>        | Quad Timer peripheral base address |
| <i>channel</i>     | Quad Timer channel number          |
| <i>clockSource</i> | Quad Timer clock source            |

**38.4.16 static void QTMR\_StopTimer ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel* ) [inline], [static]**

Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |

**38.4.17 void QTMR\_EnableDma ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint32\_t *mask* )**

Parameters

---

|                |                                                                                                         |
|----------------|---------------------------------------------------------------------------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address                                                                      |
| <i>channel</i> | Quad Timer channel number                                                                               |
| <i>mask</i>    | The DMA to enable. This is a logical OR of members of the enumeration <a href="#">qtmr_dma_enable_t</a> |

### 38.4.18 void QTMR\_DisableDma ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, uint32\_t *mask* )

Parameters

|                |                                                                                                         |
|----------------|---------------------------------------------------------------------------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address                                                                      |
| <i>channel</i> | Quad Timer channel number                                                                               |
| <i>mask</i>    | The DMA to enable. This is a logical OR of members of the enumeration <a href="#">qtmr_dma_enable_t</a> |

### 38.4.19 void QTMR\_SetPwmOutputToldle ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, bool *idleStatus* )

Note

When the PWM is set again, the counting needs to be restarted.

Parameters

|                   |                                                                                   |
|-------------------|-----------------------------------------------------------------------------------|
| <i>base</i>       | Quad Timer peripheral base address                                                |
| <i>channel</i>    | Quad Timer channel number                                                         |
| <i>idleStatus</i> | True: PWM output is high in idle status; false: PWM output is low in idle status. |

### 38.4.20 static qtmr\_pwm\_out\_state\_t QTMR\_GetPwmOutputStatus ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel* ) [inline], [static]

Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |

Returns

Current channel output status.

### 38.4.21 **uint8\_t QTMR\_GetPwmChannelStatus ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel* )**

Parameters

|                |                                    |
|----------------|------------------------------------|
| <i>base</i>    | Quad Timer peripheral base address |
| <i>channel</i> | Quad Timer channel number          |

Returns

Current channel dutycycle value.

### 38.4.22 **void QTMR\_SetPwmClockMode ( TMR\_Type \* *base*, qtmr\_channel\_selection\_t *channel*, qtmr\_primary\_count\_source\_t *prescaler* )**

Parameters

|                  |                                    |
|------------------|------------------------------------|
| <i>base</i>      | Quad Timer peripheral base address |
| <i>channel</i>   | Quad Timer channel number          |
| <i>prescaler</i> | Set prescaler value                |

# Chapter 39

## RTWDOG: 32-bit Watchdog Timer

### 39.1 Overview

The MCUXpresso SDK provides a peripheral driver for the RTWDOG module of MCUXpresso SDK devices.

### 39.2 Typical use case

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/rtwdog

## Data Structures

- struct `rtwdog_work_mode_t`  
*Defines RTWDOG work mode. [More...](#)*
- struct `rtwdog_config_t`  
*Describes RTWDOG configuration structure. [More...](#)*

## Enumerations

- enum `rtwdog_clock_source_t` {  
  kRTWDOG\_ClockSource0 = 0U,  
  kRTWDOG\_ClockSource1 = 1U,  
  kRTWDOG\_ClockSource2 = 2U,  
  kRTWDOG\_ClockSource3 = 3U }  
*Describes RTWDOG clock source.*
- enum `rtwdog_clock_prescaler_t` {  
  kRTWDOG\_ClockPrescalerDivide1 = 0x0U,  
  kRTWDOG\_ClockPrescalerDivide256 = 0x1U }  
*Describes the selection of the clock prescaler.*
- enum `rtwdog_test_mode_t` {  
  kRTWDOG\_TestModeDisabled = 0U,  
  kRTWDOG\_UserModeEnabled = 1U,  
  kRTWDOG\_LowByteTest = 2U,  
  kRTWDOG\_HighByteTest = 3U }  
*Describes RTWDOG test mode.*
- enum `_rtwdog_interrupt_enable_t` { kRTWDOG\_InterruptEnable = RTWDOG\_CS\_INT\_MASK }  
*RTWDOG interrupt configuration structure.*
- enum `_rtwdog_status_flags_t` {  
  kRTWDOG\_RunningFlag = RTWDOG\_CS\_EN\_MASK,  
  kRTWDOG\_InterruptFlag = RTWDOG\_CS\_FLG\_MASK }  
*RTWDOG status flags.*

## Unlock sequence

- #define **WDOG\_FIRST\_WORD\_OF\_UNLOCK** (RTWDOG\_UPDATE\_KEY & 0xFFFFU)  
*First word of unlock sequence.*
- #define **WDOG\_SECOND\_WORD\_OF\_UNLOCK** ((RTWDOG\_UPDATE\_KEY >> 16U) & 0xFFFFU)  
*Second word of unlock sequence.*

## Refresh sequence

- #define **WDOG\_FIRST\_WORD\_OF\_REFRESH** (RTWDOG\_REFRESH\_KEY & 0xFFFFU)  
*First word of refresh sequence.*
- #define **WDOG\_SECOND\_WORD\_OF\_REFRESH** ((RTWDOG\_REFRESH\_KEY >> 16U) & 0xFFFFU)  
*Second word of refresh sequence.*

## Driver version

- #define **FSL\_RTWDOG\_DRIVER\_VERSION** (MAKE\_VERSION(2, 1, 2))  
*RTWDOG driver version 2.1.2.*

## RTWDOG Initialization and De-initialization

- void **RTWDOG\_GetDefaultConfig** (rtwdog\_config\_t \*config)  
*Initializes the RTWDOG configuration structure.*
- void **RTWDOG\_Init** (RTWDOG\_Type \*base, const rtwdog\_config\_t \*config)  
*Initializes the RTWDOG module.*
- void **RTWDOG\_Deinit** (RTWDOG\_Type \*base)  
*De-initializes the RTWDOG module.*

## RTWDOG functional Operation

- static void **RTWDOG\_Enable** (RTWDOG\_Type \*base)  
*Enables the RTWDOG module.*
- static void **RTWDOG\_Disable** (RTWDOG\_Type \*base)  
*Disables the RTWDOG module.*
- static void **RTWDOG\_EnableInterrupts** (RTWDOG\_Type \*base, uint32\_t mask)  
*Enables the RTWDOG interrupt.*
- static void **RTWDOG\_DisableInterrupts** (RTWDOG\_Type \*base, uint32\_t mask)  
*Disables the RTWDOG interrupt.*
- static uint32\_t **RTWDOG\_GetStatusFlags** (RTWDOG\_Type \*base)  
*Gets the RTWDOG all status flags.*
- static void **RTWDOG\_EnableWindowMode** (RTWDOG\_Type \*base, bool enable)  
*Enables/disables the window mode.*
- static uint32\_t **RTWDOG\_CountToMesec** (RTWDOG\_Type \*base, uint32\_t count, uint32\_t clockFreqInHz)  
*Converts raw count value to millisecond.*
- void **RTWDOG\_ClearStatusFlags** (RTWDOG\_Type \*base, uint32\_t mask)  
*Clears the RTWDOG flag.*
- static void **RTWDOG\_SetTimeoutValue** (RTWDOG\_Type \*base, uint16\_t timeoutCount)

- static void [RTWDOG\\_SetWindowValue](#) (RTWDOG\_Type \*base, uint16\_t windowValue)
 

*Sets the RTWDOG timeout value.*
- [\\_\\_STATIC\\_FORCEINLINE](#) void [RTWDOG\\_Unlock](#) (RTWDOG\_Type \*base)
 

*Unlocks the RTWDOG register written.*
- static void [RTWDOG\\_Refresh](#) (RTWDOG\_Type \*base)
 

*Refreshes the RTWDOG timer.*
- static uint16\_t [RTWDOG\\_GetCounterValue](#) (RTWDOG\_Type \*base)
 

*Gets the RTWDOG counter value.*

## 39.3 Data Structure Documentation

### 39.3.1 struct rtwdog\_work\_mode\_t

#### Data Fields

- bool [enableWait](#)

*Enables or disables RTWDOG in wait mode.*
- bool [enableStop](#)

*Enables or disables RTWDOG in stop mode.*
- bool [enableDebug](#)

*Enables or disables RTWDOG in debug mode.*

### 39.3.2 struct rtwdog\_config\_t

#### Data Fields

- bool [enableRtwdog](#)

*Enables or disables RTWDOG.*
- [rtwdog\\_clock\\_source\\_t](#) [clockSource](#)

*Clock source select.*
- [rtwdog\\_clock\\_prescaler\\_t](#) [prescaler](#)

*Clock prescaler value.*
- [rtwdog\\_work\\_mode\\_t](#) [workMode](#)

*Configures RTWDOG work mode in debug stop and wait mode.*
- [rtwdog\\_test\\_mode\\_t](#) [testMode](#)

*Configures RTWDOG test mode.*
- bool [enableUpdate](#)

*Update write-once register enable.*
- bool [enableInterrupt](#)

*Enables or disables RTWDOG interrupt.*
- bool [enableWindowMode](#)

*Enables or disables RTWDOG window mode.*
- uint16\_t [windowValue](#)

*Window value.*
- uint16\_t [timeoutValue](#)

*Timeout value.*

## 39.4 Macro Definition Documentation

**39.4.1 #define FSL\_RTWDOG\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 2))**

## 39.5 Enumeration Type Documentation

### 39.5.1 enum rtwdog\_clock\_source\_t

Enumerator

*kRTWDOG\_ClockSource0* Clock source 0.

*kRTWDOG\_ClockSource1* Clock source 1.

*kRTWDOG\_ClockSource2* Clock source 2.

*kRTWDOG\_ClockSource3* Clock source 3.

### 39.5.2 enum rtwdog\_clock\_prescaler\_t

Enumerator

*kRTWDOG\_ClockPrescalerDivide1* Divided by 1.

*kRTWDOG\_ClockPrescalerDivide256* Divided by 256.

### 39.5.3 enum rtwdog\_test\_mode\_t

Enumerator

*kRTWDOG\_TestModeDisabled* Test Mode disabled.

*kRTWDOG\_UserModeEnabled* User Mode enabled.

*kRTWDOG\_LowByteTest* Test Mode enabled, only low byte is used.

*kRTWDOG\_HighByteTest* Test Mode enabled, only high byte is used.

### 39.5.4 enum \_rtwdog\_interrupt\_enable\_t

This structure contains the settings for all of the RTWDOG interrupt configurations.

Enumerator

*kRTWDOG\_InterruptEnable* Interrupt is generated before forcing a reset.

### 39.5.5 enum \_rtwdog\_status\_flags\_t

This structure contains the RTWDOG status flags for use in the RTWDOG functions.

Enumerator

- kRTWDOG\_RunningFlag* Running flag, set when RTWDOG is enabled.
- kRTWDOG\_InterruptFlag* Interrupt flag, set when interrupt occurs.

## 39.6 Function Documentation

### 39.6.1 void RTWDOG\_GetDefaultConfig ( rtwdog\_config\_t \* config )

This function initializes the RTWDOG configuration structure to default values. The default values are:

```
* rtwdogConfig->enableRtwdog = true;
* rtwdogConfig->clockSource = kRTWDOG_ClockSource1;
* rtwdogConfig->prescaler = kRTWDOG_ClockPrescalerDivide1;
* rtwdogConfig->workMode.enableWait = true;
* rtwdogConfig->workMode.enableStop = false;
* rtwdogConfig->workMode.enableDebug = false;
* rtwdogConfig->testMode = kRTWDOG_TestModeDisabled;
* rtwdogConfig->enableUpdate = true;
* rtwdogConfig->enableInterrupt = false;
* rtwdogConfig->enableWindowMode = false;
* rtwdogConfig->>windowValue = 0U;
* rtwdogConfig->timeoutValue = 0xFFFFU;
*
```

Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>config</i> | Pointer to the RTWDOG configuration structure. |
|---------------|------------------------------------------------|

See Also

[rtwdog\\_config\\_t](#)

### 39.6.2 void RTWDOG\_Init ( RTWDOG\_Type \* base, const rtwdog\_config\_t \* config )

This function initializes the RTWDOG. To reconfigure the RTWDOG without forcing a reset first, enableUpdate must be set to true in the configuration.

Example:

```
* rtwdog_config_t config;
* RTWDOG_GetDefaultConfig(&config);
* config.timeoutValue = 0x7ffU;
* config.enableUpdate = true;
* RTWDOG_Init(wdog_base,&config);
*
```

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | RTWDOG peripheral base address.  |
| <i>config</i> | The configuration of the RTWDOG. |

### 39.6.3 void RTWDOG\_Deinit ( RTWDOG\_Type \* *base* )

This function shuts down the RTWDOG. Ensure that the WDOG\_CS.UPDATE is 1, which means that the register update is enabled.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | RTWDOG peripheral base address. |
|-------------|---------------------------------|

### 39.6.4 static void RTWDOG\_Enable ( RTWDOG\_Type \* *base* ) [inline], [static]

This function writes a value into the WDOG\_CS register to enable the RTWDOG. The WDOG\_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | RTWDOG peripheral base address. |
|-------------|---------------------------------|

### 39.6.5 static void RTWDOG\_Disable ( RTWDOG\_Type \* *base* ) [inline], [static]

This function writes a value into the WDOG\_CS register to disable the RTWDOG. The WDOG\_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | RTWDOG peripheral base address |
|-------------|--------------------------------|

### 39.6.6 static void RTWDOG\_EnableInterrupts ( RTWDOG\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function writes a value into the WDOG\_CS register to enable the RTWDOG interrupt. The WDOG\_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

|             |                                                                                                                                                                            |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | RTWDOG peripheral base address.                                                                                                                                            |
| <i>mask</i> | The interrupts to enable. The parameter can be a combination of the following source if defined: <ul style="list-style-type: none"><li>• kRTWDOG_InterruptEnable</li></ul> |

### 39.6.7 static void RTWDOG\_DisableInterrupts ( RTWDOG\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function writes a value into the WDOG\_CS register to disable the RTWDOG interrupt. The WDOG\_CS register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

|             |                                                                                                                                                                              |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | RTWDOG peripheral base address.                                                                                                                                              |
| <i>mask</i> | The interrupts to disabled. The parameter can be a combination of the following source if defined: <ul style="list-style-type: none"><li>• kRTWDOG_InterruptEnable</li></ul> |

### 39.6.8 static uint32\_t RTWDOG\_GetStatusFlags ( RTWDOG\_Type \* *base* ) [inline], [static]

This function gets all status flags.

Example to get the running flag:

```
*     uint32_t status;
*     status = RTWDOG_GetStatusFlags(wdog_base) &
*             kRTWDOG_RunningFlag;
*
```

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | RTWDOG peripheral base address |
|-------------|--------------------------------|

Returns

State of the status flag: asserted (true) or not-asserted (false).

See Also

[\\_rtwdog\\_status\\_flags\\_t](#)

- true: related status flag has been set.
- false: related status flag is not set.

### 39.6.9 static void RTWDOG\_EnableWindowMode ( RTWDOG\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                               |
|---------------|-----------------------------------------------|
| <i>base</i>   | RTWDOG peripheral base address.               |
| <i>enable</i> | Enables(true) or disables(false) the feature. |

### 39.6.10 static uint32\_t RTWDOG\_CountToMesec ( RTWDOG\_Type \* *base*, uint32\_t *count*, uint32\_t *clockFreqInHz* ) [inline], [static]

Note that if the clock frequency is too high the timeout period can be less than 1 ms. In this case this api will return 0 value.

Parameters

|                      |                                                |
|----------------------|------------------------------------------------|
| <i>base</i>          | RTWDOG peripheral base address.                |
| <i>count</i>         | Raw count value.                               |
| <i>clockFreqInHz</i> | The frequency of the clock source RTWDOG uses. |

### 39.6.11 void RTWDOG\_ClearStatusFlags ( RTWDOG\_Type \* *base*, uint32\_t *mask* )

This function clears the RTWDOG status flag.

Example to clear an interrupt flag:

```
*     RTWDOG_ClearStatusFlags(wdog_base,
    kRTWDOG_InterruptFlag);
*
```

## Parameters

|             |                                                                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | RTWDOG peripheral base address.                                                                                                                                  |
| <i>mask</i> | The status flags to clear. The parameter can be any combination of the following values: <ul style="list-style-type: none"><li>• kRTWDOG_InterruptFlag</li></ul> |

**39.6.12 static void RTWDOG\_SetTimeoutValue ( RTWDOG\_Type \* *base*, uint16\_t *timeoutCount* ) [inline], [static]**

This function writes a timeout value into the WDOG\_TOVAL register. The WDOG\_TOVAL register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

## Parameters

|                     |                                                    |
|---------------------|----------------------------------------------------|
| <i>base</i>         | RTWDOG peripheral base address                     |
| <i>timeoutCount</i> | RTWDOG timeout value, count of RTWDOG clock ticks. |

**39.6.13 static void RTWDOG\_SetWindowValue ( RTWDOG\_Type \* *base*, uint16\_t *windowValue* ) [inline], [static]**

This function writes a window value into the WDOG\_WIN register. The WDOG\_WIN register is a write-once register. Ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

## Parameters

|                    |                                 |
|--------------------|---------------------------------|
| <i>base</i>        | RTWDOG peripheral base address. |
| <i>windowValue</i> | RTWDOG window value.            |

**39.6.14 \_\_STATIC\_FORCEINLINE void RTWDOG\_Unlock ( RTWDOG\_Type \* *base* )**

This function unlocks the RTWDOG register written.

Before starting the unlock sequence and following the configuration, disable the global interrupts. Otherwise, an interrupt could effectively invalidate the unlock sequence and the WCT may expire. After the configuration finishes, re-enable the global interrupts.

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | RTWDOG peripheral base address |
|-------------|--------------------------------|

### **39.6.15 static void RTWDOG\_Refresh ( RTWDOG\_Type \* *base* ) [inline], [static]**

This function feeds the RTWDOG. This function should be called before the Watchdog timer is in timeout. Otherwise, a reset is asserted.

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | RTWDOG peripheral base address |
|-------------|--------------------------------|

### **39.6.16 static uint16\_t RTWDOG\_GetCounterValue ( RTWDOG\_Type \* *base* ) [inline], [static]**

This function gets the RTWDOG counter value.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | RTWDOG peripheral base address. |
|-------------|---------------------------------|

Returns

Current RTWDOG counter value.

# Chapter 40

## SAI: Serial Audio Interface

### 40.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Serial Audio Interface (SAI) module of MCUXpresso SDK devices.

SAI driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for SAI initialization, configuration and operation, and for optimization and customization purposes. Using the functional API requires the knowledge of the SAI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. SAI functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `sai_handle_t` as the first parameter. Initialize the handle by calling the [SAI\\_TransferTxCreateHandle\(\)](#) or [SAI\\_TransferRxCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [SAI\\_TransferSendNonBlocking\(\)](#) and [SAI\\_TransferReceiveNonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_SAI_TxIdle` and `kStatus_SAI_RxIdle` status.

### 40.2 Typical configurations

#### Bit width configuration

SAI driver support 8/16/24/32bits stereo/mono raw audio data transfer. SAI EDMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI DMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI SDMA driver support 8/16/24/32bits stereo/mono raw audio data transfer.

#### Frame configuration

SAI driver support I2S, DSP, Left justified, Right justified, TDM mode. Application can call the api directly: `SAI_GetClassicI2SConfig` `SAI_GetLeftJustifiedConfig` `SAI_GetRightJustifiedConfig` `SAI_GetTDMConfig` `SAI_GetDSPConfig`

## 40.3 Typical use case

### 40.3.1 SAI Send/receive using an interrupt method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/sai

### 40.3.2 SAI Send/receive using a DMA method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/sai

## Modules

- [SAI Driver](#)
- [SAI EDMA Driver](#)

## 40.4 SAI Driver

### 40.4.1 Overview

#### Data Structures

- struct [sai\\_config\\_t](#)  
*SAI user configuration structure. [More...](#)*
- struct [sai\\_transfer\\_format\\_t](#)  
*sai transfer format [More...](#)*
- struct [sai\\_fifo\\_t](#)  
*sai fifo configurations [More...](#)*
- struct [sai\\_bit\\_clock\\_t](#)  
*sai bit clock configurations [More...](#)*
- struct [sai\\_frame\\_sync\\_t](#)  
*sai frame sync configurations [More...](#)*
- struct [sai\\_serial\\_data\\_t](#)  
*sai serial data configurations [More...](#)*
- struct [sai\\_transceiver\\_t](#)  
*sai transceiver configurations [More...](#)*
- struct [sai\\_transfer\\_t](#)  
*SAI transfer structure. [More...](#)*
- struct [sai\\_handle\\_t](#)  
*SAI handle structure. [More...](#)*

#### Macros

- #define [SAI\\_XFER\\_QUEUE\\_SIZE](#) (4U)  
*SAI transfer queue size, user can refine it according to use case.*
- #define [FSL\\_SAI\\_HAS\\_FIFO\\_EXTEND\\_FEATURE](#) 1  
*sai fifo feature*

#### Typedefs

- typedef void(\* [sai\\_transfer\\_callback\\_t](#) )(I2S\_Type \*base, sai\_handle\_t \*handle, [status\\_t](#) status, void \*userData)  
*SAI transfer callback prototype.*

## Enumerations

- enum {
   
kStatus\_SAI\_TxBusy = MAKE\_STATUS(kStatusGroup\_SAI, 0),
   
kStatus\_SAI\_RxBusy = MAKE\_STATUS(kStatusGroup\_SAI, 1),
   
kStatus\_SAI\_TxError = MAKE\_STATUS(kStatusGroup\_SAI, 2),
   
kStatus\_SAI\_RxError = MAKE\_STATUS(kStatusGroup\_SAI, 3),
   
kStatus\_SAI\_QueueFull = MAKE\_STATUS(kStatusGroup\_SAI, 4),
   
kStatus\_SAI\_TxIdle = MAKE\_STATUS(kStatusGroup\_SAI, 5),
   
kStatus\_SAI\_RxIdle = MAKE\_STATUS(kStatusGroup\_SAI, 6) }
   
*\_sai\_status\_t, SAI return status.*
- enum {
   
kSAI\_Channel0Mask = 1 << 0U,
   
kSAI\_Channel1Mask = 1 << 1U,
   
kSAI\_Channel2Mask = 1 << 2U,
   
kSAI\_Channel3Mask = 1 << 3U,
   
kSAI\_Channel4Mask = 1 << 4U,
   
kSAI\_Channel5Mask = 1 << 5U,
   
kSAI\_Channel6Mask = 1 << 6U,
   
kSAI\_Channel7Mask = 1 << 7U }  
*\_sai\_channel\_mask,.sai channel mask value, actual channel numbers is depend soc specific*
- enum **sai\_protocol\_t** {
   
kSAI\_BusLeftJustified = 0x0U,
   
kSAI\_BusRightJustified,
   
kSAI\_BusI2S,
   
kSAI\_BusPCMA,
   
kSAI\_BusPCMB }
- Define the SAI bus type.*
- enum **sai\_master\_slave\_t** {
   
kSAI\_Master = 0x0U,
   
kSAI\_Slave = 0x1U,
   
kSAI\_Bclk\_Master\_FrameSync\_Slave = 0x2U,
   
kSAI\_Bclk\_Slave\_FrameSync\_Master = 0x3U }  
*Master or slave mode.*
- enum **sai\_mono\_stereo\_t** {
   
kSAI\_Stereo = 0x0U,
   
kSAI\_MonoRight,
   
kSAI\_MonoLeft }
- Mono or stereo audio format.*
- enum **sai\_data\_order\_t** {
   
kSAI\_DataLSB = 0x0U,
   
kSAI\_DataMSB }
- SAI data order, MSB or LSB.*
- enum **sai\_clock\_polarity\_t** {

- ```
kSAI_PolarityActiveHigh = 0x0U,
kSAI_PolarityActiveLow = 0x1U,
kSAI_SampleOnFallingEdge = 0x0U,
kSAI_SampleOnRisingEdge = 0x1U }
```

*SAI clock polarity, active high or low.*
- enum `sai_sync_mode_t` {
 

```
kSAI_ModeAsync = 0x0U,
kSAI_ModeSync }
```

*Synchronous or asynchronous mode.*
- enum `sai_bclk_source_t` {
 

```
kSAI_BclkSourceBusclk = 0x0U,
kSAI_BclkSourceMclkOption1 = 0x1U,
kSAI_BclkSourceMclkOption2 = 0x2U,
kSAI_BclkSourceMclkOption3 = 0x3U,
kSAI_BclkSourceMclkDiv = 0x1U,
kSAI_BclkSourceOtherSai0 = 0x2U,
kSAI_BclkSourceOtherSai1 = 0x3U }
```

*Bit clock source.*
- enum {
 

```
kSAI_WordStartInterruptEnable,
kSAI_SyncErrorInterruptEnable = I2S_TCSR_SEIE_MASK,
kSAI_FIFOWarningInterruptEnable = I2S_TCSR_FWIE_MASK,
kSAI_FIFOErrorInterruptEnable = I2S_TCSR_FEIE_MASK,
kSAI_FIFORequestInterruptEnable = I2S_TCSR_FRIE_MASK }
```

*\_sai\_interrupt\_enable\_t, The SAI interrupt enable flag*
- enum {
 

```
kSAI_FIFOWarningDMAEnable = I2S_TCSR_FWDE_MASK,
kSAI_FIFORequestDMAEnable = I2S_TCSR_FRDE_MASK }
```

*\_sai\_dma\_enable\_t, The DMA request sources*
- enum {
 

```
kSAI_WordStartFlag = I2S_TCSR_WSF_MASK,
kSAI_SyncErrorFlag = I2S_TCSR_SEF_MASK,
kSAI_FIFOErrorFlag = I2S_TCSR_FEF_MASK,
kSAI_FIFORequestFlag = I2S_TCSR_FRF_MASK,
kSAI_FIFOWarningFlag = I2S_TCSR_FWF_MASK }
```

*\_sai\_flags, The SAI status flag*
- enum `sai_reset_type_t` {
 

```
kSAI_ResetTypeSoftware = I2S_TCSR_SR_MASK,
kSAI_ResetTypeFIFO = I2S_TCSR_FR_MASK,
kSAI_ResetAll = I2S_TCSR_SR_MASK | I2S_TCSR_FR_MASK }
```

*The reset type.*
- enum `sai_fifo_packing_t` {
 

```
kSAI_FifoPackingDisabled = 0x0U,
kSAI_FifoPacking8bit = 0x2U,
kSAI_FifoPacking16bit = 0x3U }
```

*The SAI packing mode The mode includes 8 bit and 16 bit packing.*
- enum `sai_sample_rate_t` {

```
kSAI_SampleRate8KHz = 8000U,
kSAI_SampleRate11025Hz = 11025U,
kSAI_SampleRate12KHz = 12000U,
kSAI_SampleRate16KHz = 16000U,
kSAI_SampleRate22050Hz = 22050U,
kSAI_SampleRate24KHz = 24000U,
kSAI_SampleRate32KHz = 32000U,
kSAI_SampleRate44100Hz = 44100U,
kSAI_SampleRate48KHz = 48000U,
kSAI_SampleRate96KHz = 96000U,
kSAI_SampleRate192KHz = 192000U,
kSAI_SampleRate384KHz = 384000U }
```

*Audio sample rate.*

- enum `sai_word_width_t` {
   
kSAI\_WordWidth8bits = 8U,
   
kSAI\_WordWidth16bits = 16U,
   
kSAI\_WordWidth24bits = 24U,
   
kSAI\_WordWidth32bits = 32U }

*Audio word width.*

- enum `sai_data_pin_state_t` {
   
kSAI\_DataPinStateTriState,
   
kSAI\_DataPinStateOutputZero = 1U }
- sai data pin state definition*
- enum `sai_fifo_combine_t` {
   
kSAI\_FifoCombineDisabled = 0U,
   
kSAI\_FifoCombineModeEnabledOnRead,
   
kSAI\_FifoCombineModeEnabledOnWrite,
   
kSAI\_FifoCombineModeEnabledReadWrite }
- sai fifo combine mode definition*

- enum `sai_transceiver_type_t` {
   
kSAI\_Transmitter = 0U,
   
kSAI\_Receiver = 1U }
- sai transceiver type*
- enum `sai_frame_sync_len_t` {
   
kSAI\_FrameSyncLenOneBitClk = 0U,
   
kSAI\_FrameSyncLenPerWordWidth = 1U }
- sai frame sync len*

## Driver version

- #define `FSL_SAI_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 8)`)
- Version 2.3.8.*

## Initialization and deinitialization

- void **SAI\_TxInit** (I2S\_Type \*base, const **sai\_config\_t** \*config)  
*Initializes the SAI Tx peripheral.*
- void **SAI\_RxInit** (I2S\_Type \*base, const **sai\_config\_t** \*config)  
*Initializes the SAI Rx peripheral.*
- void **SAI\_TxGetDefaultConfig** (**sai\_config\_t** \*config)  
*Sets the SAI Tx configuration structure to default values.*
- void **SAI\_RxGetDefaultConfig** (**sai\_config\_t** \*config)  
*Sets the SAI Rx configuration structure to default values.*
- void **SAI\_Init** (I2S\_Type \*base)  
*Initializes the SAI peripheral.*
- void **SAI\_Deinit** (I2S\_Type \*base)  
*De-initializes the SAI peripheral.*
- void **SAI\_TxReset** (I2S\_Type \*base)  
*Resets the SAI Tx.*
- void **SAI\_RxReset** (I2S\_Type \*base)  
*Resets the SAI Rx.*
- void **SAI\_TxEnable** (I2S\_Type \*base, bool enable)  
*Enables/disables the SAI Tx.*
- void **SAI\_RxEnable** (I2S\_Type \*base, bool enable)  
*Enables/disables the SAI Rx.*
- static void **SAI\_TxSetBitClockDirection** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave)  
*Set Rx bit clock direction.*
- static void **SAI\_RxSetBitClockDirection** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave)  
*Set Rx bit clock direction.*
- static void **SAI\_RxSetFrameSyncDirection** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave)  
*Set Rx frame sync direction.*
- static void **SAI\_TxSetFrameSyncDirection** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave)  
*Set Tx frame sync direction.*
- void **SAI\_TxSetBitClockRate** (I2S\_Type \*base, uint32\_t sourceClockHz, uint32\_t sampleRate, uint32\_t bitWidth, uint32\_t channelNumbers)  
*Transmitter bit clock rate configurations.*
- void **SAI\_RxSetBitClockRate** (I2S\_Type \*base, uint32\_t sourceClockHz, uint32\_t sampleRate, uint32\_t bitWidth, uint32\_t channelNumbers)  
*Receiver bit clock rate configurations.*
- void **SAI\_TxSetBitclockConfig** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave, **sai\_bit\_clock\_t** \*config)  
*Transmitter Bit clock configurations.*
- void **SAI\_RxSetBitclockConfig** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave, **sai\_bit\_clock\_t** \*config)  
*Receiver Bit clock configurations.*
- void **SAI\_TxSetFifoConfig** (I2S\_Type \*base, **sai\_fifo\_t** \*config)  
*SAI transmitter fifo configurations.*
- void **SAI\_RxSetFifoConfig** (I2S\_Type \*base, **sai\_fifo\_t** \*config)  
*SAI receiver fifo configurations.*
- void **SAI\_TxSetFrameSyncConfig** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave, **sai\_frame\_sync\_t** \*config)  
*SAI transmitter Frame sync configurations.*
- void **SAI\_RxSetFrameSyncConfig** (I2S\_Type \*base, **sai\_master\_slave\_t** masterSlave, **sai\_frame\_sync\_t** \*config)  
*SAI receiver Frame sync configurations.*

- `sync_t *config`  
*SAI receiver Frame sync configurations.*
- void `SAI_TxSetSerialDataConfig` (I2S\_Type \*base, `sai_serial_data_t` \*config)  
*SAI transmitter Serial data configurations.*
- void `SAI_RxSetSerialDataConfig` (I2S\_Type \*base, `sai_serial_data_t` \*config)  
*SAI receiver Serial data configurations.*
- void `SAI_TxSetConfig` (I2S\_Type \*base, `sai_transceiver_t` \*config)  
*SAI transmitter configurations.*
- void `SAI_RxSetConfig` (I2S\_Type \*base, `sai_transceiver_t` \*config)  
*SAI receiver configurations.*
- void `SAI_GetClassicI2SConfig` (`sai_transceiver_t` \*config, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)  
*Get classic I2S mode configurations.*
- void `SAI_GetLeftJustifiedConfig` (`sai_transceiver_t` \*config, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)  
*Get left justified mode configurations.*
- void `SAI_GetRightJustifiedConfig` (`sai_transceiver_t` \*config, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)  
*Get right justified mode configurations.*
- void `SAI_GetTDMConfig` (`sai_transceiver_t` \*config, `sai_frame_sync_len_t` frameSyncWidth, `sai_word_width_t` bitWidth, `uint32_t` dataWordNum, `uint32_t` saiChannelMask)  
*Get TDM mode configurations.*
- void `SAI_GetDSPConfig` (`sai_transceiver_t` \*config, `sai_frame_sync_len_t` frameSyncWidth, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)  
*Get DSP mode configurations.*

## Status

- static `uint32_t SAI_TxGetStatusFlag` (I2S\_Type \*base)  
*Gets the SAI Tx status flag state.*
- static void `SAI_TxClearStatusFlags` (I2S\_Type \*base, `uint32_t` mask)  
*Clears the SAI Tx status flag state.*
- static `uint32_t SAI_RxGetStatusFlag` (I2S\_Type \*base)  
*Gets the SAI Rx status flag state.*
- static void `SAI_RxClearStatusFlags` (I2S\_Type \*base, `uint32_t` mask)  
*Clears the SAI Rx status flag state.*
- void `SAI_TxSoftwareReset` (I2S\_Type \*base, `sai_reset_type_t` resetType)  
*Do software reset or FIFO reset .*
- void `SAI_RxSoftwareReset` (I2S\_Type \*base, `sai_reset_type_t` resetType)  
*Do software reset or FIFO reset .*
- void `SAI_TxSetChannelFIFOMask` (I2S\_Type \*base, `uint8_t` mask)  
*Set the Tx channel FIFO enable mask.*
- void `SAI_RxSetChannelFIFOMask` (I2S\_Type \*base, `uint8_t` mask)  
*Set the Rx channel FIFO enable mask.*
- void `SAI_TxSetDataOrder` (I2S\_Type \*base, `sai_data_order_t` order)  
*Set the Tx data order.*
- void `SAI_RxSetDataOrder` (I2S\_Type \*base, `sai_data_order_t` order)  
*Set the Rx data order.*
- void `SAI_TxSetBitClockPolarity` (I2S\_Type \*base, `sai_clock_polarity_t` polarity)

- Set the Tx data order.
- void [SAI\\_RxSetBitClockPolarity](#) (I2S\_Type \*base, sai\_clock\_polarity\_t polarity)
  - Set the Rx data order.
- void [SAI\\_TxSetFrameSyncPolarity](#) (I2S\_Type \*base, sai\_clock\_polarity\_t polarity)
  - Set the Tx data order.
- void [SAI\\_RxSetFrameSyncPolarity](#) (I2S\_Type \*base, sai\_clock\_polarity\_t polarity)
  - Set the Rx data order.
- void [SAI\\_TxSetFIFOPacking](#) (I2S\_Type \*base, sai\_fifo\_packing\_t pack)
  - Set Tx FIFO packing feature.
- void [SAI\\_RxSetFIFOPacking](#) (I2S\_Type \*base, sai\_fifo\_packing\_t pack)
  - Set Rx FIFO packing feature.
- static void [SAI\\_TxSetFIFOErrorContinue](#) (I2S\_Type \*base, bool isEnabled)
  - Set Tx FIFO error continue.
- static void [SAI\\_RxSetFIFOErrorContinue](#) (I2S\_Type \*base, bool isEnabled)
  - Set Rx FIFO error continue.

## Interrupts

- static void [SAI\\_TxEnableInterrupts](#) (I2S\_Type \*base, uint32\_t mask)
  - Enables the SAI Tx interrupt requests.
- static void [SAI\\_RxEnableInterrupts](#) (I2S\_Type \*base, uint32\_t mask)
  - Enables the SAI Rx interrupt requests.
- static void [SAI\\_TxDisableInterrupts](#) (I2S\_Type \*base, uint32\_t mask)
  - Disables the SAI Tx interrupt requests.
- static void [SAI\\_RxDisableInterrupts](#) (I2S\_Type \*base, uint32\_t mask)
  - Disables the SAI Rx interrupt requests.

## DMA Control

- static void [SAI\\_TxEnableDMA](#) (I2S\_Type \*base, uint32\_t mask, bool enable)
  - Enables/disables the SAI Tx DMA requests.
- static void [SAI\\_RxEnableDMA](#) (I2S\_Type \*base, uint32\_t mask, bool enable)
  - Enables/disables the SAI Rx DMA requests.
- static uintptr\_t [SAI\\_TxGetDataRegisterAddress](#) (I2S\_Type \*base, uint32\_t channel)
  - Gets the SAI Tx data register address.
- static uintptr\_t [SAI\\_RxGetDataRegisterAddress](#) (I2S\_Type \*base, uint32\_t channel)
  - Gets the SAI Rx data register address.

## Bus Operations

- void [SAI\\_TxSetFormat](#) (I2S\_Type \*base, sai\_transfer\_format\_t \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)
  - Configures the SAI Tx audio format.
- void [SAI\\_RxSetFormat](#) (I2S\_Type \*base, sai\_transfer\_format\_t \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)
  - Configures the SAI Rx audio format.

- void **SAI\_WriteBlocking** (I2S\_Type \*base, uint32\_t channel, uint32\_t bitWidth, uint8\_t \*buffer, uint32\_t size)
 

*Sends data using a blocking method.*
- void **SAI\_WriteMultiChannelBlocking** (I2S\_Type \*base, uint32\_t channel, uint32\_t channelMask, uint32\_t bitWidth, uint8\_t \*buffer, uint32\_t size)
 

*Sends data to multi channel using a blocking method.*
- static void **SAI\_WriteData** (I2S\_Type \*base, uint32\_t channel, uint32\_t data)
 

*Writes data into SAI FIFO.*
- void **SAI\_ReadBlocking** (I2S\_Type \*base, uint32\_t channel, uint32\_t bitWidth, uint8\_t \*buffer, uint32\_t size)
 

*Receives data using a blocking method.*
- void **SAI\_ReadMultiChannelBlocking** (I2S\_Type \*base, uint32\_t channel, uint32\_t channelMask, uint32\_t bitWidth, uint8\_t \*buffer, uint32\_t size)
 

*Receives multi channel data using a blocking method.*
- static uint32\_t **SAI\_ReadData** (I2S\_Type \*base, uint32\_t channel)
 

*Reads data from the SAI FIFO.*

## Transactional

- void **SAI\_TransferTxCreateHandle** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transfer\_callback\_t** callback, void \*userData)
 

*Initializes the SAI Tx handle.*
- void **SAI\_TransferRxCreateHandle** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transfer\_callback\_t** callback, void \*userData)
 

*Initializes the SAI Rx handle.*
- void **SAI\_TransferTxSetConfig** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transceiver\_t** \*config)
 

*SAI transmitter transfer configurations.*
- void **SAI\_TransferRxSetConfig** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transceiver\_t** \*config)
 

*SAI receiver transfer configurations.*
- **status\_t SAI\_TransferTxSetFormat** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transfer\_format\_t** \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)
 

*Configures the SAI Tx audio format.*
- **status\_t SAI\_TransferRxSetFormat** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transfer\_format\_t** \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)
 

*Configures the SAI Rx audio format.*
- **status\_t SAI\_TransferSendNonBlocking** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transfer\_t** \*xfer)
 

*Performs an interrupt non-blocking send transfer on SAI.*
- **status\_t SAI\_TransferReceiveNonBlocking** (I2S\_Type \*base, sai\_handle\_t \*handle, **sai\_transfer\_t** \*xfer)
 

*Performs an interrupt non-blocking receive transfer on SAI.*
- **status\_t SAI\_TransferGetSendCount** (I2S\_Type \*base, sai\_handle\_t \*handle, size\_t \*count)
 

*Gets a set byte count.*
- **status\_t SAI\_TransferGetReceiveCount** (I2S\_Type \*base, sai\_handle\_t \*handle, size\_t \*count)
 

*Gets a received byte count.*
- void **SAI\_TransferAbortSend** (I2S\_Type \*base, sai\_handle\_t \*handle)
 

*Aborts the current send.*
- void **SAI\_TransferAbortReceive** (I2S\_Type \*base, sai\_handle\_t \*handle)

*Aborts the current IRQ receive.*

- void [SAI\\_TransferTerminateSend](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Terminate all SAI send.*
- void [SAI\\_TransferTerminateReceive](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Terminate all SAI receive.*
- void [SAI\\_TransferTxHandleIRQ](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Tx interrupt handler.*
- void [SAI\\_TransferRxHandleIRQ](#) (I2S\_Type \*base, sai\_handle\_t \*handle)  
*Tx interrupt handler.*

## 40.4.2 Data Structure Documentation

### 40.4.2.1 struct sai\_config\_t

#### Data Fields

- sai\_protocol\_t **protocol**  
*Audio bus protocol in SAI.*
- sai\_sync\_mode\_t **syncMode**  
*SAI sync mode, control Tx/Rx clock sync.*
- sai\_bclk\_source\_t **bclkSource**  
*Bit Clock source.*
- sai\_master\_slave\_t **masterSlave**  
*Master or slave.*

### 40.4.2.2 struct sai\_transfer\_format\_t

#### Data Fields

- uint32\_t **sampleRate\_Hz**  
*Sample rate of audio data.*
- uint32\_t **bitWidth**  
*Data length of audio data, usually 8/16/24/32 bits.*
- sai\_mono\_stereo\_t **stereo**  
*Mono or stereo.*
- uint8\_t **watermark**  
*Watermark value.*
- uint8\_t **channel**  
*Transfer start channel.*
- uint8\_t **channelMask**  
*enabled channel mask value, reference \_sai\_channel\_mask*
- uint8\_t **endChannel**  
*end channel number*
- uint8\_t **channelNums**  
*Total enabled channel numbers.*
- sai\_protocol\_t **protocol**  
*Which audio protocol used.*
- bool **isFrameSyncCompact**

*True means Frame sync length is configurable according to bitWidth, false means frame sync length is 64 times of bit clock.*

## Field Documentation

### (1) `bool sai_transfer_format_t::isFrameSyncCompact`

#### 40.4.2.3 `struct sai_fifo_t`

##### Data Fields

- `bool fifoContinueOneError`  
*fifo continues when error occur*
- `sai_fifo_combine_t fifoCombine`  
*fifo combine mode*
- `sai_fifo_packing_t fifoPacking`  
*fifo packing mode*
- `uint8_t fifoWatermark`  
*fifo watermark*

#### 40.4.2.4 `struct sai_bit_clock_t`

##### Data Fields

- `bool bclkSrcSwap`  
*bit clock source swap*
- `bool bclkInputDelay`  
*bit clock actually used by the transmitter is delayed by the pad output delay, this has effect of decreasing the data input setup time, but increasing the data output valid time .*
- `sai_clock_polarity_t bclkPolarity`  
*bit clock polarity*
- `sai_bclk_source_t bclkSource`  
*bit Clock source*

## Field Documentation

### (1) `bool sai_bit_clock_t::bclkInputDelay`

#### 40.4.2.5 `struct sai_frame_sync_t`

##### Data Fields

- `uint8_t frameSyncWidth`  
*frame sync width in number of bit clocks*
- `bool frameSyncEarly`  
*TRUE is frame sync assert one bit before the first bit of frame FALSE is frame sync assert with the first bit of the frame.*
- `bool frameSyncGenerateOnDemand`  
*internal frame sync is generated when FIFO waring flag is clear*
- `sai_clock_polarity_t frameSyncPolarity`

*frame sync polarity*

#### 40.4.2.6 struct sai\_serial\_data\_t

##### Data Fields

- [sai\\_data\\_pin\\_state\\_t dataMode](#)  
*sai data pin state when slots masked or channel disabled*
- [sai\\_data\\_order\\_t dataOrder](#)  
*configure whether the LSB or MSB is transmitted first*
- [uint8\\_t dataWord0Length](#)  
*configure the number of bits in the first word in each frame*
- [uint8\\_t dataWordNLength](#)  
*configure the number of bits in the each word in each frame, except the first word*
- [uint8\\_t dataWordLength](#)  
*used to record the data length for dma transfer*
- [uint8\\_t dataFirstBitShifted](#)  
*Configure the bit index for the first bit transmitted for each word in the frame.*
- [uint8\\_t dataWordNum](#)  
*configure the number of words in each frame*
- [uint32\\_t dataMaskedWord](#)  
*configure whether the transmit word is masked*

#### 40.4.2.7 struct sai\_transceiver\_t

##### Data Fields

- [sai\\_serial\\_data\\_t serialData](#)  
*serial data configurations*
- [sai\\_frame\\_sync\\_t frameSync](#)  
*ws configurations*
- [sai\\_bit\\_clock\\_t bitClock](#)  
*bit clock configurations*
- [sai\\_fifo\\_t fifo](#)  
*fifo configurations*
- [sai\\_master\\_slave\\_t masterSlave](#)  
*transceiver is master or slave*
- [sai\\_sync\\_mode\\_t syncMode](#)  
*transceiver sync mode*
- [uint8\\_t startChannel](#)  
*Transfer start channel.*
- [uint8\\_t channelMask](#)  
*enabled channel mask value, reference \_sai\_channel\_mask*
- [uint8\\_t endChannel](#)  
*end channel number*
- [uint8\\_t channelNums](#)  
*Total enabled channel numbers.*

#### 40.4.2.8 struct sai\_transfer\_t

##### Data Fields

- `uint8_t * data`  
*Data start address to transfer.*
- `size_t dataSize`  
*Transfer size.*

##### Field Documentation

- (1) `uint8_t* sai_transfer_t::data`
- (2) `size_t sai_transfer_t::dataSize`

#### 40.4.2.9 struct \_sai\_handle

##### Data Fields

- `I2S_Type * base`  
*base address*
- `uint32_t state`  
*Transfer status.*
- `sai_transfer_callback_t callback`  
*Callback function called at transfer event.*
- `void * userData`  
*Callback parameter passed to callback function.*
- `uint8_t bitWidth`  
*Bit width for transfer, 8/16/24/32 bits.*
- `uint8_t channel`  
*Transfer start channel.*
- `uint8_t channelMask`  
*enabled channel mask value, refernece \_sai\_channel\_mask*
- `uint8_t endChannel`  
*end channel number*
- `uint8_t channelNums`  
*Total enabled channel numbers.*
- `sai_transfer_t saiQueue [SAI_XFER_QUEUE_SIZE]`  
*Transfer queue storing queued transfer.*
- `size_t transferSize [SAI_XFER_QUEUE_SIZE]`  
*Data bytes need to transfer.*
- `volatile uint8_t queueUser`  
*Index for user to queue transfer.*
- `volatile uint8_t queueDriver`  
*Index for driver to get the transfer data and size.*
- `uint8_t watermark`  
*Watermark value.*

### 40.4.3 Macro Definition Documentation

#### 40.4.3.1 #define SAI\_XFER\_QUEUE\_SIZE (4U)

### 40.4.4 Enumeration Type Documentation

#### 40.4.4.1 anonymous enum

Enumerator

- kStatus\_SAI\_TxBusy* SAI Tx is busy.
- kStatus\_SAI\_RxBusy* SAI Rx is busy.
- kStatus\_SAI\_TxError* SAI Tx FIFO error.
- kStatus\_SAI\_RxError* SAI Rx FIFO error.
- kStatus\_SAI\_QueueFull* SAI transfer queue is full.
- kStatus\_SAI\_TxIdle* SAI Tx is idle.
- kStatus\_SAI\_RxIdle* SAI Rx is idle.

#### 40.4.4.2 anonymous enum

Enumerator

- kSAI\_Channel0Mask* channel 0 mask value
- kSAI\_Channel1Mask* channel 1 mask value
- kSAI\_Channel2Mask* channel 2 mask value
- kSAI\_Channel3Mask* channel 3 mask value
- kSAI\_Channel4Mask* channel 4 mask value
- kSAI\_Channel5Mask* channel 5 mask value
- kSAI\_Channel6Mask* channel 6 mask value
- kSAI\_Channel7Mask* channel 7 mask value

#### 40.4.4.3 enum sai\_protocol\_t

Enumerator

- kSAI\_BusLeftJustified* Uses left justified format.
- kSAI\_BusRightJustified* Uses right justified format.
- kSAI\_BusI2S* Uses I2S format.
- kSAI\_BusPCMA* Uses I2S PCM A format.
- kSAI\_BusPCMB* Uses I2S PCM B format.

#### 40.4.4.4 enum sai\_master\_slave\_t

Enumerator

***kSAI\_Master*** Master mode include bclk and frame sync.

***kSAI\_Slave*** Slave mode include bclk and frame sync.

***kSAI\_Bclk\_Master\_FrameSync\_Slave*** bclk in master mode, frame sync in slave mode

***kSAI\_Bclk\_Slave\_FrameSync\_Master*** bclk in slave mode, frame sync in master mode

#### 40.4.4.5 enum sai\_mono\_stereo\_t

Enumerator

***kSAI\_Stereo*** Stereo sound.

***kSAI\_MonoRight*** Only Right channel have sound.

***kSAI\_MonoLeft*** Only left channel have sound.

#### 40.4.4.6 enum sai\_data\_order\_t

Enumerator

***kSAI\_DataLSB*** LSB bit transferred first.

***kSAI\_DataMSB*** MSB bit transferred first.

#### 40.4.4.7 enum sai\_clock\_polarity\_t

Enumerator

***kSAI\_PolarityActiveHigh*** Drive outputs on rising edge.

***kSAI\_PolarityActiveLow*** Drive outputs on falling edge.

***kSAI\_SampleOnFallingEdge*** Sample inputs on falling edge.

***kSAI\_SampleOnRisingEdge*** Sample inputs on rising edge.

#### 40.4.4.8 enum sai\_sync\_mode\_t

Enumerator

***kSAI\_ModeAsync*** Asynchronous mode.

***kSAI\_ModeSync*** Synchronous mode (with receiver or transmit)

#### 40.4.4.9 enum sai\_bclk\_source\_t

Enumerator

- kSAI\_BclkSourceBusclk* Bit clock using bus clock.
- kSAI\_BclkSourceMclkOption1* Bit clock MCLK option 1.
- kSAI\_BclkSourceMclkOption2* Bit clock MCLK option2.
- kSAI\_BclkSourceMclkOption3* Bit clock MCLK option3.
- kSAI\_BclkSourceMclkDiv* Bit clock using master clock divider.
- kSAI\_BclkSourceOtherSai0* Bit clock from other SAI device.
- kSAI\_BclkSourceOtherSai1* Bit clock from other SAI device.

#### 40.4.4.10 anonymous enum

Enumerator

- kSAI\_WordStartInterruptEnable* Word start flag, means the first word in a frame detected.
- kSAI\_SyncErrorInterruptEnable* Sync error flag, means the sync error is detected.
- kSAI\_FIFOWarningInterruptEnable* FIFO warning flag, means the FIFO is empty.
- kSAI\_FIFOErrorInterruptEnable* FIFO error flag.
- kSAI\_FIFORequestInterruptEnable* FIFO request, means reached watermark.

#### 40.4.4.11 anonymous enum

Enumerator

- kSAI\_FIFOWarningDMAEnable* FIFO warning caused by the DMA request.
- kSAI\_FIFORequestDMAEnable* FIFO request caused by the DMA request.

#### 40.4.4.12 anonymous enum

Enumerator

- kSAI\_WordStartFlag* Word start flag, means the first word in a frame detected.
- kSAI\_SyncErrorFlag* Sync error flag, means the sync error is detected.
- kSAI\_FIFOErrorFlag* FIFO error flag.
- kSAI\_FIFORequestFlag* FIFO request flag.
- kSAI\_FIFOWarningFlag* FIFO warning flag.

#### 40.4.4.13 enum sai\_reset\_type\_t

Enumerator

- kSAI\_ResetTypeSoftware* Software reset, reset the logic state.
- kSAI\_ResetTypeFIFO* FIFO reset, reset the FIFO read and write pointer.

***kSAI\_ResetAll*** All reset.

#### 40.4.4.14 enum sai\_fifo\_packing\_t

Enumerator

***kSAI\_FifoPackingDisabled*** Packing disabled.

***kSAI\_FifoPacking8bit*** 8 bit packing enabled

***kSAI\_FifoPacking16bit*** 16bit packing enabled

#### 40.4.4.15 enum sai\_sample\_rate\_t

Enumerator

***kSAI\_SampleRate8KHz*** Sample rate 8000 Hz.

***kSAI\_SampleRate11025Hz*** Sample rate 11025 Hz.

***kSAI\_SampleRate12KHz*** Sample rate 12000 Hz.

***kSAI\_SampleRate16KHz*** Sample rate 16000 Hz.

***kSAI\_SampleRate22050Hz*** Sample rate 22050 Hz.

***kSAI\_SampleRate24KHz*** Sample rate 24000 Hz.

***kSAI\_SampleRate32KHz*** Sample rate 32000 Hz.

***kSAI\_SampleRate44100Hz*** Sample rate 44100 Hz.

***kSAI\_SampleRate48KHz*** Sample rate 48000 Hz.

***kSAI\_SampleRate96KHz*** Sample rate 96000 Hz.

***kSAI\_SampleRate192KHz*** Sample rate 192000 Hz.

***kSAI\_SampleRate384KHz*** Sample rate 384000 Hz.

#### 40.4.4.16 enum sai\_word\_width\_t

Enumerator

***kSAI\_WordWidth8bits*** Audio data width 8 bits.

***kSAI\_WordWidth16bits*** Audio data width 16 bits.

***kSAI\_WordWidth24bits*** Audio data width 24 bits.

***kSAI\_WordWidth32bits*** Audio data width 32 bits.

#### 40.4.4.17 enum sai\_data\_pin\_state\_t

Enumerator

***kSAI\_DataPinStateTriState*** transmit data pins are tri-stated when slots are masked or channels are disabled

***kSAI\_DataPinStateOutputZero*** transmit data pins are never tri-stated and will output zero when slots are masked or channel disabled

#### 40.4.4.18 enum sai\_fifo\_combine\_t

Enumerator

*kSAI\_FifoCombineDisabled* sai fifo combine mode disabled  
*kSAI\_FifoCombineModeEnabledOnRead* sai fifo combine mode enabled on FIFO reads  
*kSAI\_FifoCombineModeEnabledOnWrite* sai fifo combine mode enabled on FIFO write  
*kSAI\_FifoCombineModeEnabledOnReadWrite* sai fifo combined mode enabled on FIFO read/writes

#### 40.4.4.19 enum sai\_transceiver\_type\_t

Enumerator

*kSAI\_Transmitter* sai transmitter  
*kSAI\_Receiver* sai receiver

#### 40.4.4.20 enum sai\_frame\_sync\_len\_t

Enumerator

*kSAI\_FrameSyncLenOneBitClk* 1 bit clock frame sync len for DSP mode  
*kSAI\_FrameSyncLenPerWordWidth* Frame sync length decided by word width.

### 40.4.5 Function Documentation

#### 40.4.5.1 void SAI\_TxInit ( I2S\_Type \* *base*, const sai\_config\_t \* *config* )

**Deprecated** Do not use this function. It has been superceded by [SAI\\_Init](#)

Ungates the SAI clock, resets the module, and configures SAI Tx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI\\_TxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAIM module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	SAI base pointer
<i>config</i>	SAI configuration structure.

#### 40.4.5.2 void SAI\_RxInit ( I2S\_Type \* *base*, const sai\_config\_t \* *config* )

**Deprecated** Do not use this function. It has been superceded by [SAI\\_Init](#)

Ungates the SAI clock, resets the module, and configures the SAI Rx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI\\_RxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAI module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	SAI base pointer
<i>config</i>	SAI configuration structure.

#### 40.4.5.3 void SAI\_TxGetDefaultConfig ( sai\_config\_t \* *config* )

**Deprecated** Do not use this function. It has been superceded by [SAI\\_GetClassicI2SConfig](#), [SAI\\_GetLeft-JustifiedConfig](#) , [SAI\\_GetRightJustifiedConfig](#), [SAI\\_GetDSPConfig](#), [SAI\\_GetTDMConfig](#)

This API initializes the configuration structure for use in [SAI\\_TxConfig\(\)](#). The initialized structure can remain unchanged in [SAI\\_TxConfig\(\)](#), or it can be modified before calling [SAI\\_TxConfig\(\)](#). This is an example.

```
sai_config_t config;
SAI_TxGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

#### 40.4.5.4 void SAI\_RxGetDefaultConfig ( sai\_config\_t \* *config* )

**Deprecated** Do not use this function. It has been superceded by [SAI\\_GetClassicI2SConfig](#), [SAI\\_GetLeftJustifiedConfig](#), [SAI\\_GetRightJustifiedConfig](#), [SAI\\_GetDSPConfig](#), [SAI\\_GetTDMConfig](#)

This API initializes the configuration structure for use in SAI\_RxConfig(). The initialized structure can remain unchanged in SAI\_RxConfig() or it can be modified before calling SAI\_RxConfig(). This is an example.

```
sai_config_t config;
SAI_RxGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

#### 40.4.5.5 void SAI\_Init ( I2S\_Type \* *base* )

This API gates the SAI clock. The SAI module can't operate unless SAI\_Init is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

#### 40.4.5.6 void SAI\_Deinit ( I2S\_Type \* *base* )

This API gates the SAI clock. The SAI module can't operate unless SAI\_TxInit or SAI\_RxInit is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

#### 40.4.5.7 void SAI\_TxReset ( I2S\_Type \* *base* )

This function enables the software reset and FIFO reset of SAI Tx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

#### 40.4.5.8 void SAI\_RxReset ( I2S\_Type \* *base* )

This function enables the software reset and FIFO reset of SAI Rx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

#### 40.4.5.9 void SAI\_TxEnable ( I2S\_Type \* *base*, bool *enable* )

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Tx, false means disable.

#### 40.4.5.10 void SAI\_RxEnable ( I2S\_Type \* *base*, bool *enable* )

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Rx, false means disable.

#### 40.4.5.11 static void SAI\_TxSetBitClockDirection ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave* ) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>masterSlave</i>	reference sai_master_slave_t.
--------------------	-------------------------------

#### 40.4.5.12 static void SAI\_RxSetBitClockDirection ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave* ) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

#### 40.4.5.13 static void SAI\_RxSetFrameSyncDirection ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave* ) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

#### 40.4.5.14 static void SAI\_TxSetFrameSyncDirection ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave* ) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

#### 40.4.5.15 void SAI\_TxSetBitClockRate ( I2S\_Type \* *base*, uint32\_t *sourceClockHz*, uint32\_t *sampleRate*, uint32\_t *bitWidth*, uint32\_t *channelNumbers* )

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

**40.4.5.16 void SAI\_RxSetBitClockRate ( I2S\_Type \* *base*, uint32\_t *sourceClockHz*, uint32\_t *sampleRate*, uint32\_t *bitWidth*, uint32\_t *channelNumbers* )**

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

**40.4.5.17 void SAI\_TxSetBitclockConfig ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave*, sai\_bit\_clock\_t \* *config* )**

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

**40.4.5.18 void SAI\_RxSetBitclockConfig ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave*, sai\_bit\_clock\_t \* *config* )**

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

#### 40.4.5.19 void SAI\_TxSetFifoConfig ( I2S\_Type \* *base*, sai\_fifo\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

#### 40.4.5.20 void SAI\_RxSetFifoConfig ( I2S\_Type \* *base*, sai\_fifo\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

#### 40.4.5.21 void SAI\_TxSetFrameSyncConfig ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave*, sai\_frame\_sync\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

#### 40.4.5.22 void SAI\_RxSetFrameSyncConfig ( I2S\_Type \* *base*, sai\_master\_slave\_t *masterSlave*, sai\_frame\_sync\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

#### 40.4.5.23 void SAI\_TxSetSerialDataConfig ( I2S\_Type \* *base*, sai\_serial\_data\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

#### 40.4.5.24 void SAI\_RxSetSerialDataConfig ( I2S\_Type \* *base*, sai\_serial\_data\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

#### 40.4.5.25 void SAI\_TxSetConfig ( I2S\_Type \* *base*, sai\_transceiver\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	transmitter configurations.

#### 40.4.5.26 void SAI\_RxSetConfig ( I2S\_Type \* *base*, sai\_transceiver\_t \* *config* )

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>config</i>	receiver configurations.
---------------	--------------------------

**40.4.5.27 void SAI\_GetClassicI2SConfig ( *sai\_transceiver\_t \* config*, *sai\_word\_width\_t bitWidth*, *sai\_mono\_stereo\_t mode*, *uint32\_t saiChannelMask* )**

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

**40.4.5.28 void SAI\_GetLeftJustifiedConfig ( *sai\_transceiver\_t \* config*, *sai\_word\_width\_t bitWidth*, *sai\_mono\_stereo\_t mode*, *uint32\_t saiChannelMask* )**

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

**40.4.5.29 void SAI\_GetRightJustifiedConfig ( *sai\_transceiver\_t \* config*, *sai\_word\_width\_t bitWidth*, *sai\_mono\_stereo\_t mode*, *uint32\_t saiChannelMask* )**

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.

<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

**40.4.5.30 void SAI\_GetTDMConfig ( *sai\_transceiver\_t \* config, sai\_frame\_sync\_len\_t frameSyncWidth, sai\_word\_width\_t bitWidth, uint32\_t dataWordNum, uint32\_t saiChannelMask* )**

Parameters

<i>config</i>	transceiver configurations.
<i>frameSyncWidth</i>	length of frame sync.
<i>bitWidth</i>	audio data word width.
<i>dataWordNum</i>	word number in one frame.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

**40.4.5.31 void SAI\_GetDSPConfig ( *sai\_transceiver\_t \* config, sai\_frame\_sync\_len\_t frameSyncWidth, sai\_word\_width\_t bitWidth, sai\_mono\_stereo\_t mode, uint32\_t saiChannelMask* )**

Note

DSP mode is also called PCM mode which support MODE A and MODE B, DSP/PCM MODE A configuration flow. RX is similiar but uses SAI\_RxSetConfig instead of SAI\_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
                   kSAI_Stereo, channelMask)
* config->frameSync.frameSyncEarly      = true;
* SAI_TxSetConfig(base, config)
*
```

DSP/PCM MODE B configuration flow for TX. RX is similiar but uses SAI\_RxSetConfig instead of SAI\_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
                   kSAI_Stereo, channelMask)
* SAI_TxSetConfig(base, config)
*
```

Parameters

<i>config</i>	transceiver configurations.
<i>frameSyncWidth</i>	length of frame sync.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannelMask</i>	mask value of the channel to enable.

**40.4.5.32 static uint32\_t SAI\_TxGetStatusFlag ( I2S\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Tx status flag value. Use the Status Mask to get the status value needed.

**40.4.5.33 static void SAI\_TxClearStatusFlags ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	State mask. It can be a combination of the following source if defined: <ul style="list-style-type: none"> <li>• kSAI_WordStartFlag</li> <li>• kSAI_SyncErrorFlag</li> <li>• kSAI_FIFOErrorFlag</li> </ul>

**40.4.5.34 static uint32\_t SAI\_RxGetStatusFlag ( I2S\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Rx status flag value. Use the Status Mask to get the status value needed.

#### 40.4.5.35 static void SAI\_RxClearStatusFlags ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>State mask. It can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kSAI_WordStartFlag</li> <li>• kSAI_SyncErrorFlag</li> <li>• kSAI_FIFOErrorFlag</li> </ul>

#### 40.4.5.36 void SAI\_TxSoftwareReset ( I2S\_Type \* *base*, sai\_reset\_type\_t *resetType* )

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Tx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like TCR1~TCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>resetType</i>	Reset type, FIFO reset or software reset

#### 40.4.5.37 void SAI\_RxSoftwareReset ( I2S\_Type \* *base*, sai\_reset\_type\_t *resetType* )

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Rx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like RCR1~RCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>resetType</i>	Reset type, FIFO reset or software reset

#### 40.4.5.38 void SAI\_TxSetChannelFIFOMask ( I2S\_Type \* *base*, uint8\_t *mask* )

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

#### 40.4.5.39 void SAI\_RxSetChannelFIFOMask ( I2S\_Type \* *base*, uint8\_t *mask* )

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

#### 40.4.5.40 void SAI\_TxSetDataOrder ( I2S\_Type \* *base*, sai\_data\_order\_t *order* )

Parameters

<i>base</i>	SAI base pointer
<i>order</i>	Data order MSB or LSB

#### 40.4.5.41 void SAI\_RxSetDataOrder ( I2S\_Type \* *base*, sai\_data\_order\_t *order* )

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

<i>order</i>	Data order MSB or LSB
--------------	-----------------------

**40.4.5.42 void SAI\_TxSetBitClockPolarity ( I2S\_Type \* *base*, sai\_clock\_polarity\_t *polarity* )**

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

**40.4.5.43 void SAI\_RxSetBitClockPolarity ( I2S\_Type \* *base*, sai\_clock\_polarity\_t *polarity* )**

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

**40.4.5.44 void SAI\_TxSetFrameSyncPolarity ( I2S\_Type \* *base*, sai\_clock\_polarity\_t *polarity* )**

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

**40.4.5.45 void SAI\_RxSetFrameSyncPolarity ( I2S\_Type \* *base*, sai\_clock\_polarity\_t *polarity* )**

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

**40.4.5.46 void SAI\_TxSetFIFOPacking ( I2S\_Type \* *base*, sai\_fifo\_packing\_t *pack* )**

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

#### 40.4.5.47 void SAI\_RxSetFIFOPacking ( I2S\_Type \* *base*, sai\_fifo\_packing\_t *pack* )

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

#### 40.4.5.48 static void SAI\_TxSetFIFOErrorContinue ( I2S\_Type \* *base*, bool *isEnabled* ) [inline], [static]

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in TCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

#### 40.4.5.49 static void SAI\_RxSetFIFOErrorContinue ( I2S\_Type \* *base*, bool *isEnabled* ) [inline], [static]

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in RCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

#### 40.4.5.50 static void SAI\_TxEnableInterrupts ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kSAI_WordStartInterruptEnable</li> <li>• kSAI_SyncErrorInterruptEnable</li> <li>• kSAI_FIFOWarningInterruptEnable</li> <li>• kSAI_FIFORequestInterruptEnable</li> <li>• kSAI_FIFOErrorInterruptEnable</li> </ul>

#### 40.4.5.51 static void SAI\_RxEnableInterrupts ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kSAI_WordStartInterruptEnable</li> <li>• kSAI_SyncErrorInterruptEnable</li> <li>• kSAI_FIFOWarningInterruptEnable</li> <li>• kSAI_FIFORequestInterruptEnable</li> <li>• kSAI_FIFOErrorInterruptEnable</li> </ul>

#### 40.4.5.52 static void SAI\_TxDisableInterrupts ( I2S\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kSAI_WordStartInterruptEnable</li> <li>• kSAI_SyncErrorInterruptEnable</li> <li>• kSAI_FIFOWarningInterruptEnable</li> <li>• kSAI_FIFORequestInterruptEnable</li> <li>• kSAI_FIFOErrorInterruptEnable</li> </ul>

**40.4.5.53 static void SAI\_RxDisableInterrupts ( I2S\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kSAI_WordStartInterruptEnable</li> <li>• kSAI_SyncErrorInterruptEnable</li> <li>• kSAI_FIFOWarningInterruptEnable</li> <li>• kSAI_FIFORequestInterruptEnable</li> <li>• kSAI_FIFOErrorInterruptEnable</li> </ul>

**40.4.5.54 static void SAI\_TxEnableDMA ( I2S\_Type \* *base*, uint32\_t *mask*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>DMA source The parameter can be combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kSAI_FIFOWarningDMAEnable</li> <li>• kSAI_FIFORequestDMAEnable</li> </ul>
<i>enable</i>	True means enable DMA, false means disable DMA.

**40.4.5.55 static void SAI\_RxEnableDMA ( I2S\_Type \* *base*, uint32\_t *mask*, bool *enable* )  
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

<i>mask</i>	DMA source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> <li>• kSAI_FIFOWarningDMAEnable</li> <li>• kSAI_FIFORequestDMAEnable</li> </ul>
<i>enable</i>	True means enable DMA, false means disable DMA.

#### 40.4.5.56 static uintptr\_t SAI\_TxGetDataRegisterAddress ( I2S\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

#### 40.4.5.57 static uintptr\_t SAI\_RxGetDataRegisterAddress ( I2S\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

#### 40.4.5.58 void SAI\_TxSetFormat ( I2S\_Type \* *base*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )

**Deprecated** Do not use this function. It has been superceded by [SAI\\_TxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz.

**40.4.5.59 void SAI\_RxSetFormat ( I2S\_Type \* *base*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

**Deprecated** Do not use this function. It has been superceded by [SAI\\_RxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz.

**40.4.5.60 void SAI\_WriteBlocking ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *bitWidth*, uint8\_t \* *buffer*, uint32\_t *size* )**

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

**40.4.5.61 void SAI\_WriteMultiChannelBlocking ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *channelMask*, uint32\_t *bitWidth*, uint8\_t \* *buffer*, uint32\_t *size* )**

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

**40.4.5.62 static void SAI\_WriteData ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *data* ) [inline], [static]**

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>data</i>	Data needs to be written.

**40.4.5.63 void SAI\_ReadBlocking ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *bitWidth*, uint8\_t \* *buffer*, uint32\_t *size* )**

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

**40.4.5.64 void SAI\_ReadMultiChannelBlocking ( I2S\_Type \* *base*, uint32\_t *channel*, uint32\_t *channelMask*, uint32\_t *bitWidth*, uint8\_t \* *buffer*, uint32\_t *size* )**

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

**40.4.5.65 static uint32\_t SAI\_ReadData ( I2S\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.

Returns

Data in SAI FIFO.

**40.4.5.66 void SAI\_TransferTxCreateHandle ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*,  
sai\_transfer\_callback\_t *callback*, void \* *userData* )**

This function initializes the Tx handle for the SAI Tx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function

#### 40.4.5.67 void SAI\_TransferRxCreateHandle ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the Rx handle for the SAI Rx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function.

#### 40.4.5.68 void SAI\_TransferTxSetConfig ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transceiver\_t \* *config* )

This function initializes the Tx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	transmitter configurations.

#### 40.4.5.69 void SAI\_TransferRxSetConfig ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transceiver\_t \* *config* )

This function initializes the Rx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	receiver configurations.

**40.4.5.70 status\_t SAI\_TransferTxSetFormat ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

**Deprecated** Do not use this function. It has been superceded by [SAI\\_TransferTxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the <i>masterClockHz</i> in <i>format</i> .

Returns

Status of this function. Return value is the *status\_t*.

**40.4.5.71 status\_t SAI\_TransferRxSetFormat ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

**Deprecated** Do not use this function. It has been superceded by [SAI\\_TransferRxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

## Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the masterClockHz in format.

## Returns

Status of this function. Return value is one of status\_t.

#### 40.4.5.72 status\_t SAI\_TransferSendNonBlocking ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )

## Note

This API returns immediately after the transfer initiates. Call the SAI\_TxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus\_SAI\_Busy, the transfer is finished.

## Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>xfer</i>	Pointer to the sai_transfer_t structure.

## Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_TxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

#### 40.4.5.73 status\_t SAI\_TransferReceiveNonBlocking ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )

## Note

This API returns immediately after the transfer initiates. Call the SAI\_RxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus\_SAI\_Busy, the transfer is finished.

## Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>xfer</i>	Pointer to the <a href="#">sai_transfer_t</a> structure.

## Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_RxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

**40.4.5.74 status\_t SAI\_TransferGetSendCount ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, size\_t \* *count* )**

## Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count sent.

## Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

**40.4.5.75 status\_t SAI\_TransferGetReceiveCount ( I2S\_Type \* *base*, sai\_handle\_t \* *handle*, size\_t \* *count* )**

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

#### 40.4.5.76 void SAI\_TransferAbortSend ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

Note

This API can be called any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

#### 40.4.5.77 void SAI\_TransferAbortReceive ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

#### 40.4.5.78 void SAI\_TransferTerminateSend ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI\_TransferAbortSend.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

#### 40.4.5.79 void SAI\_TransferTerminateReceive ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI\_TransferAbortReceive.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

#### 40.4.5.80 void SAI\_TransferTxHandleIRQ ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

#### 40.4.5.81 void SAI\_TransferRxHandleIRQ ( I2S\_Type \* *base*, sai\_handle\_t \* *handle* )

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

## 40.5 SAI EDMA Driver

### 40.5.1 Overview

#### Data Structures

- struct `sai_edma_handle_t`  
*SAI DMA transfer handle, users should not touch the content of the handle. [More...](#)*

#### Typedefs

- typedef void(\* `sai_edma_callback_t`)(I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `status_t` status, void \*userData)  
*SAI eDMA transfer callback function for finish and error.*

#### Driver version

- #define `FSL_SAI_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 5, 1)`)  
*Version 2.5.1.*

#### eDMA Transactional

- void `SAI_TransferTxCreateHandleEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_edma_callback_t` callback, void \*userData, `edma_handle_t` \*txDmaHandle)  
*Initializes the SAI eDMA handle.*
- void `SAI_TransferRxCreateHandleEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_edma_callback_t` callback, void \*userData, `edma_handle_t` \*rxDmaHandle)  
*Initializes the SAI Rx eDMA handle.*
- void `SAI_TransferTxSetFormatEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_transfer_format_t` \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Tx audio format.*
- void `SAI_TransferRxSetFormatEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_transfer_format_t` \*format, uint32\_t mclkSourceClockHz, uint32\_t bclkSourceClockHz)  
*Configures the SAI Rx audio format.*
- void `SAI_TransferTxSetConfigEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_transceiver_t` \*saiConfig)  
*Configures the SAI Tx.*
- void `SAI_TransferRxSetConfigEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_transceiver_t` \*saiConfig)  
*Configures the SAI Rx.*
- `status_t SAI_TransferSendEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_transfer_t` \*xfer)  
*Performs a non-blocking SAI transfer using DMA.*
- `status_t SAI_TransferReceiveEDMA` (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, `sai_transfer_t` \*xfer)

- *Performs a non-blocking SAI receive using eDMA.*  
**status\_t SAI\_TransferSendLoopEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, sai\_transfer\_t \*xfer, uint32\_t loopTransferCount)
- *Performs a non-blocking SAI loop transfer using eDMA.*  
**status\_t SAI\_TransferReceiveLoopEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, sai\_transfer\_t \*xfer, uint32\_t loopTransferCount)
- *Performs a non-blocking SAI loop transfer using eDMA.*  
**void SAI\_TransferTerminateSendEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle)  
*Terminate all SAI send.*
- **void SAI\_TransferTerminateReceiveEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle)  
*Terminate all SAI receive.*
- **void SAI\_TransferAbortSendEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle)  
*Aborts a SAI transfer using eDMA.*
- **void SAI\_TransferAbortReceiveEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle)  
*Aborts a SAI receive using eDMA.*
- **status\_t SAI\_TransferGetSendCountEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets byte count sent by SAI.*
- **status\_t SAI\_TransferGetReceiveCountEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle, size\_t \*count)  
*Gets byte count received by SAI.*
- **uint32\_t SAI\_TransferGetValidTransferSlotsEDMA** (I2S\_Type \*base, sai\_edma\_handle\_t \*handle)  
*Gets valid transfer slot.*

## 40.5.2 Data Structure Documentation

### 40.5.2.1 struct sai\_edma\_handle

#### Data Fields

- **edma\_handle\_t \* dmaHandle**  
*DMA handler for SAI send.*
- **uint8\_t nbytes**  
*eDMA minor byte transfer count initially configured.*
- **uint8\_t bytesPerFrame**  
*Bytes in a frame.*
- **uint8\_t channelMask**  
*Enabled channel mask value, reference \_sai\_channel\_mask.*
- **uint8\_t channelNums**  
*total enabled channel nums*
- **uint8\_t channel**  
*Which data channel.*
- **uint8\_t count**  
*The transfer data count in a DMA request.*
- **uint32\_t state**  
*Internal state for SAI eDMA transfer.*
- **sai\_edma\_callback\_t callback**  
*Callback for users while transfer finish or error occurs.*
- **void \* userData**

- *User callback parameter.*
- `uint8_t tcd [ (SAI_XFER_QUEUE_SIZE+1U)*sizeof(edma_tcd_t) ]`  
*TCD pool for eDMA transfer.*
- `sai_transfer_t saiQueue [SAI_XFER_QUEUE_SIZE]`  
*Transfer queue storing queued transfer.*
- `size_t transferSize [SAI_XFER_QUEUE_SIZE]`  
*Data bytes need to transfer.*
- `volatile uint8_t queueUser`  
*Index for user to queue transfer.*
- `volatile uint8_t queueDriver`  
*Index for driver to get the transfer data and size.*

## Field Documentation

- (1) `uint8_t sai_edma_handle_t::nbytes`
- (2) `uint8_t sai_edma_handle_t::tcd[(SAI_XFER_QUEUE_SIZE+1U)*sizeof(edma_tcd_t)]`
- (3) `sai_transfer_t sai_edma_handle_t::saiQueue[SAI_XFER_QUEUE_SIZE]`
- (4) `volatile uint8_t sai_edma_handle_t::queueUser`

## 40.5.3 Function Documentation

**40.5.3.1 void SAI\_TransferTxCreateHandleEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_edma\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *txDmaHandle* )**

This function initializes the SAI master DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>base</i>	SAI peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>txDmaHandle</i>	eDMA handle pointer, this handle shall be static allocated by users.

**40.5.3.2 void SAI\_TransferRxCreateHandleEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_edma\_callback\_t *callback*, void \* *userData*, edma\_handle\_t \* *rxDmaHandle* )**

This function initializes the SAI slave DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>base</i>	SAI peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>rxDmaHandle</i>	eDMA handle pointer, this handle shall be static allocated by users.

**40.5.3.3 void SAI\_TransferTxSetFormatEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

**Deprecated** Do not use this function. It has been superceded by [SAI\\_TransferTxSetConfigEDMA](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to formatting requirements.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>format</i>	Pointer to SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If bit clock source is master clock, this value should equals to masterClockHz in format.

Return values

<i>kStatus_Success</i>	Audio format set successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

**40.5.3.4 void SAI\_TransferRxSetFormatEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_format\_t \* *format*, uint32\_t *mclkSourceClockHz*, uint32\_t *bclkSourceClockHz* )**

**Deprecated** Do not use this function. It has been superceded by [SAI\\_TransferRxSetConfigEDMA](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to formatting requirements.

#### Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>format</i>	Pointer to SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is the master clock, this value should equal to <i>masterClockHz</i> in format.

#### Return values

<i>kStatus_Success</i>	Audio format set successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

### 40.5.3.5 void SAI\_TransferTxSetConfigEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transceiver\_t \* *saiConfig* )

#### Note

SAI eDMA supports data transfer in multiple SAI channels if the FIFO Combine feature is supported. To activate the multi-channel transfer enable SAI channels by filling the channelMask of *sai\_transceiver\_t* with the corresponding values of *\_sai\_channel\_mask* enum, enable the FIFO Combine mode by assigning *kSAI\_FifoCombineModeEnabledOnWrite* to the *fifoCombine* member of *sai\_fifo\_combine\_t* which is a member of *sai\_transceiver\_t*. This is an example of multi-channel data transfer configuration step.

```
*   sai_transceiver_t config;
*   SAI_GetClassicI2SConfig(&config, kSAI_WordWidth16bits,
*                           kSAI_Stereo, kSAI_Channel0Mask|kSAI_Channel1Mask);
*   config fifo fifoCombine = kSAI_FifoCombineModeEnabledOnWrite
*   ;
*   SAI_TransferTxSetConfigEDMA(I2S0, &edmaHandle, &config);
*
```

#### Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>saiConfig</i>	sai configurations.

#### 40.5.3.6 void SAI\_TransferRxSetConfigEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transceiver\_t \* *saiConfig* )

Note

SAI eDMA supports data transfer in a multiple SAI channels if the FIFO Combine feature is supported. To activate the multi-channel transfer enable SAI channels by filling the channelMask of *sai\_transceiver\_t* with the corresponding values of \_sai\_channel\_mask enum, enable the FIFO Combine mode by assigning kSAI\_FifoCombineModeEnabledOnRead to the fifoCombine member of *sai\_fifo\_combine\_t* which is a member of *sai\_transceiver\_t*. This is an example of multi-channel data transfer configuration step.

```
*     sai_transceiver_t config;
*     SAI_GetClassicI2SConfig(&config, kSAI_WordWidth16bits,
*                             kSAI_Stereo, kSAI_Channel0Mask|kSAI_Channel1Mask);
*     config fifo.fifoCombine = kSAI_FifoCombineModeEnabledOnRead
*     ;
*     SAI_TransferRxSetConfigEDMA(I2S0, &edmaHandle, &config);
*
```

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>saiConfig</i>	sai configurations.

#### 40.5.3.7 status\_t SAI\_TransferSendEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )

Note

This interface returns immediately after the transfer initiates. Call SAI\_GetTransferStatus to poll the transfer status and check whether the SAI transfer is finished.

This function support multi channel transfer,

1. for the sai IP support fifo combine mode, application should enable the fifo combine mode, no limitation on channel numbers
2. for the sai IP not support fifo combine mode, sai edma provide another solution which using EDMA modulo feature, but support 2 or 4 channels only.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_TxBusy</i>	SAI is busy sending data.

#### 40.5.3.8 status\_t SAI\_TransferReceiveEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer* )

Note

This interface returns immediately after the transfer initiates. Call the SAI\_GetReceiveRemainingBytes to poll the transfer status and check whether the SAI transfer is finished.

This function support multi channel transfer,

1. for the sai IP support fifo combine mode, application should enable the fifo combine mode, no limitation on channel numbers
2. for the sai IP not support fifo combine mode, sai edma provide another solution which using EDMA modulo feature, but support 2 or 4 channels only.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

<i>kStatus_RxBusy</i>	SAI is busy receiving data.
-----------------------	-----------------------------

#### 40.5.3.9 status\_t SAI\_TransferSendLoopEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer*, uint32\_t *loopTransferCount* )

Note

This function support loop transfer only,such as A->B->...->A, application must be aware of that the more counts of the loop transfer, then more tcd memory required, as the function use the tcd pool in sai\_edma\_handle\_t, so application could redefine the SAI\_XFER\_QUEUE\_SIZE to determine the proper TCD pool size. This function support one sai channel only.

Once the loop transfer start, application can use function SAI\_TransferAbortSendEDMA to stop the loop transfer.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure, should be a array with elements counts $\geq 1$ (loopTransferCount).
<i>loopTransferCount</i>	the counts of xfer array.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

#### 40.5.3.10 status\_t SAI\_TransferReceiveLoopEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, sai\_transfer\_t \* *xfer*, uint32\_t *loopTransferCount* )

Note

This function support loop transfer only,such as A->B->...->A, application must be aware of that the more counts of the loop transfer, then more tcd memory required, as the function use the tcd pool in sai\_edma\_handle\_t, so application could redefine the SAI\_XFER\_QUEUE\_SIZE to determine the proper TCD pool size. This function support one sai channel only.

Once the loop transfer start, application can use function SAI\_TransferAbortReceiveEDMA to stop the loop transfer.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure, should be a array with elements counts $\geq 1$ (loopTransferCount).
<i>loopTransfer-Count</i>	the counts of xfer array.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

#### 40.5.3.11 void SAI\_TransferTerminateSendEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle* )

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI\_TransferAbortSendEDMA.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

#### 40.5.3.12 void SAI\_TransferTerminateReceiveEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle* )

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI\_TransferAbortReceiveEDMA.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

**40.5.3.13 void SAI\_TransferAbortSendEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle* )**

This function only aborts the current transfer slots, the other transfer slots' information still kept in the handler. If users want to terminate all transfer slots, just call SAI\_TransferTerminateSendEDMA.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

#### 40.5.3.14 void SAI\_TransferAbortReceiveEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle* )

This function only aborts the current transfer slots, the other transfer slots' information still kept in the handler. If users want to terminate all transfer slots, just call SAI\_TransferTerminateReceiveEDMA.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.

#### 40.5.3.15 status\_t SAI\_TransferGetSendCountEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, size\_t \* *count* )

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>count</i>	Bytes count sent by SAI.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is no non-blocking transaction in progress.

#### 40.5.3.16 status\_t SAI\_TransferGetReceiveCountEDMA ( I2S\_Type \* *base*, sai\_edma\_handle\_t \* *handle*, size\_t \* *count* )

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.
<i>count</i>	Bytes count received by SAI.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is no non-blocking transaction in progress.

#### 40.5.3.17 `uint32_t SAI_TransferGetValidTransferSlotsEDMA ( I2S_Type * base, sai_edma_handle_t * handle )`

This function can be used to query the valid transfer request slot that the application can submit. It should be called in the critical section, that means the application could call it in the corresponding callback function or disable IRQ before calling it in the application, otherwise, the returned value may not correct.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.

Return values

<i>valid</i>	slot count that application submit.
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# Chapter 41

## SEMC: Smart External DRAM Controller Driver

### 41.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Smart External DRAM Controller block of MCUXpresso SDK devices.

### 41.2 SEMC: Smart External DRAM Controller Driver

#### 41.2.1 SEMC Initialization Operation

The SEMC Initialize is to initialize for common configure: gate the SEMC clock, configure IOMUX, and queue weight setting. The SEMC Deinitialize is to ungate the clock and disable SEMC module.

#### 41.2.2 SEMC Interrupt Operation

The interrupt and disable operation for SEMC.

#### 41.2.3 SEMC Memory access Operation

This group is mainly provide NAND/NOR memory access API which is through IP bus/ IP command access. Since the AXI access is directly read/write is so easy, so the AXI read/write part is not provided in SEMC.

### 41.3 Typical use case

#### Data Structures

- struct `semc_sdram_config_t`  
*SEMC SDRAM configuration structure.* [More...](#)
- struct `semc_nand_timing_config_t`  
*SEMC NAND device timing configuration structure.* [More...](#)
- struct `semc_nand_config_t`  
*SEMC NAND configuration structure.* [More...](#)
- struct `semc_nor_config_t`  
*SEMC NOR configuration structure.* [More...](#)
- struct `semc_sram_config_t`  
*SEMC SRAM configuration structure.* [More...](#)
- struct `semc_dbi_config_t`  
*SEMC DBI configuration structure.* [More...](#)
- struct `semc_queuea_weight_struct_t`

- union `semc_queuea_weight_t`  
*SEMC AXI queue a weight setting structure. [More...](#)*
- struct `semc_queueb_weight_struct_t`  
*SEMC AXI queue b weight setting structure. [More...](#)*
- union `semc_queueb_weight_t`  
*SEMC AXI queue b weight setting union. [More...](#)*
- struct `semc_axi_queueweight_t`  
*SEMC AXI queue weight setting. [More...](#)*
- struct `semc_config_t`  
*SEMC configuration structure. [More...](#)*

## Enumerations

- enum {
   
`kStatus_SEMC_InvalidDeviceType` = MAKE\_STATUS(kStatusGroup\_SEMC, 0),
   
`kStatus_SEMC_IpCommandExecutionError` = MAKE\_STATUS(kStatusGroup\_SEMC, 1),
   
`kStatus_SEMC_AxiCommandExecutionError` = MAKE\_STATUS(kStatusGroup\_SEMC, 2),
   
`kStatus_SEMC_InvalidMemorySize` = MAKE\_STATUS(kStatusGroup\_SEMC, 3),
   
`kStatus_SEMC_InvalidIpCmdDataSize` = MAKE\_STATUS(kStatusGroup\_SEMC, 4),
   
`kStatus_SEMC_InvalidAddressPortWidth` = MAKE\_STATUS(kStatusGroup\_SEMC, 5),
   
`kStatus_SEMC_InvalidDataPortWidth` = MAKE\_STATUS(kStatusGroup\_SEMC, 6),
   
`kStatus_SEMC_InvalidSwPinmuxSelection` = MAKE\_STATUS(kStatusGroup\_SEMC, 7),
   
`kStatus_SEMC_InvalidBurstLength` = MAKE\_STATUS(kStatusGroup\_SEMC, 8),
   
`kStatus_SEMC_InvalidColumnAddressBitWidth` = MAKE\_STATUS(kStatusGroup\_SEMC, 9),
   
`kStatus_SEMC_InvalidBaseAddress` = MAKE\_STATUS(kStatusGroup\_SEMC, 10),
   
`kStatus_SEMC_InvalidTimerSetting` = MAKE\_STATUS(kStatusGroup\_SEMC, 11) }
   
*SEMC status, \_semc\_status.*
- enum `semc_mem_type_t` {
   
`kSEMC_MemType_SDRAM` = 0,
   
`kSEMC_MemType_SRAM`,
   
`kSEMC_MemType_NOR`,
   
`kSEMC_MemType_NAND`,
   
`kSEMC_MemType_8080` }
   
*SEMC memory device type.*
- enum `semc_waitready_polarity_t` {
   
`kSEMC_LowActive` = 0,
   
`kSEMC_HighActive` }
   
*SEMC WAIT/RDY polarity.*
- enum `semc_sdram_cs_t` {
   
`kSEMC_SDRAM_CS0` = 0,
   
`kSEMC_SDRAM_CS1`,
   
`kSEMC_SDRAM_CS2`,
   
`kSEMC_SDRAM_CS3` }
   
*SEMC SDRAM Chip selection .*
- enum `semc_sram_cs_t` { `kSEMC_SRAM_CS0` = 0 }
   
*SEMC SRAM Chip selection .*
- enum `semc_nand_access_type_t` { }

- ```

kSEMC_NAND_ACCESS_BY_AXI = 0,
kSEMC_NAND_ACCESS_BY_IPCMD }

    SEMC NAND device type.
• enum semc_interrupt_enable_t {
    kSEMC_IPCmdDoneInterrupt = SEMC_INTEN_IPCMDDONEEN_MASK,
    kSEMC_IPCmdErrInterrupt = SEMC_INTEN_IPCMDERREN_MASK,
    kSEMC_AXICmdErrInterrupt = SEMC_INTEN_AXICMDERREN_MASK,
    kSEMC_AXIBusErrInterrupt = SEMC_INTEN_AXIBUSERREN_MASK }

    SEMC interrupts.
• enum semc_ipcmd_datasize_t {
    kSEMC_IPcmdDataSize_1bytes = 1,
    kSEMC_IPcmdDataSize_2bytes,
    kSEMC_IPcmdDataSize_3bytes,
    kSEMC_IPcmdDataSize_4bytes }

    SEMC IP command data size in bytes.
• enum semc_refresh_time_t {
    kSEMC_RefreshThreeClocks = 0x0U,
    kSEMC_RefreshSixClocks,
    kSEMC_RefreshNineClocks }

    SEMC auto-refresh timing.
• enum semc_caslatency_t {
    kSEMC_LatencyOne = 1,
    kSEMC_LatencyTwo,
    kSEMC_LatencyThree }

    CAS latency.
• enum semc_sdram_column_bit_num_t {
    kSEMC_SdramColumn_12bit = 0x0U,
    kSEMC_SdramColumn_11bit,
    kSEMC_SdramColumn_10bit,
    kSEMC_SdramColumn_9bit,
    kSEMC_SdramColumn_8bit }

    SEMC sdram column address bit number.
• enum sem_sdram_burst_len_t {
    kSEMC_Sdram_BurstLen1 = 0,
    kSEMC_Sdram_BurstLen2,
    kSEMC_Sdram_BurstLen4,
    kSEMC_Sdram_BurstLen8 }

    SEMC sdram burst length.
• enum semc_nand_column_bit_num_t {
    kSEMC_NandColum_16bit = 0x0U,
    kSEMC_NandColum_15bit,
    kSEMC_NandColum_14bit,
    kSEMC_NandColum_13bit,
    kSEMC_NandColum_12bit,
    kSEMC_NandColum_11bit,
    kSEMC_NandColum_10bit,

```

- ```

kSEMC_NandColum_9bit }
    SEMC nand column address bit number.
• enum sem_nand_burst_len_t {
    kSEMC_Nand_BurstLen1 = 0,
    kSEMC_Nand_BurstLen2,
    kSEMC_Nand_BurstLen4,
    kSEMC_Nand_BurstLen8,
    kSEMC_Nand_BurstLen16,
    kSEMC_Nand_BurstLen32,
    kSEMC_Nand_BurstLen64 }

    SEMC nand burst length.
• enum semc_norsram_column_bit_num_t {
    kSEMC_NorColum_12bit = 0x0U,
    kSEMC_NorColum_11bit,
    kSEMC_NorColum_10bit,
    kSEMC_NorColum_9bit,
    kSEMC_NorColum_8bit,
    kSEMC_NorColum_7bit,
    kSEMC_NorColum_6bit,
    kSEMC_NorColum_5bit,
    kSEMC_NorColum_4bit,
    kSEMC_NorColum_3bit,
    kSEMC_NorColum_2bit }

    SEMC nor/sram column address bit number.
• enum sem_norsram_burst_len_t {
    kSEMC_Nor_BurstLen1 = 0,
    kSEMC_Nor_BurstLen2,
    kSEMC_Nor_BurstLen4,
    kSEMC_Nor_BurstLen8,
    kSEMC_Nor_BurstLen16,
    kSEMC_Nor_BurstLen32,
    kSEMC_Nor_BurstLen64 }

    SEMC nor/sram burst length.
• enum semc_dbi_column_bit_num_t {
    kSEMC_Dbi_Colum_12bit = 0x0U,
    kSEMC_Dbi_Colum_11bit,
    kSEMC_Dbi_Colum_10bit,
    kSEMC_Dbi_Colum_9bit,
    kSEMC_Dbi_Colum_8bit,
    kSEMC_Dbi_Colum_7bit,
    kSEMC_Dbi_Colum_6bit,
    kSEMC_Dbi_Colum_5bit,
    kSEMC_Dbi_Colum_4bit,
    kSEMC_Dbi_Colum_3bit,
    kSEMC_Dbi_Colum_2bit }

    SEMC dbi column address bit number.

```

- enum `sem_dbi_burst_len_t` {
   
  `kSEMC_Dbi_BurstLen1` = 0,
   
  `kSEMC_Dbi_BurstLen2`,
   
  `kSEMC_Dbi_Dbi_BurstLen4`,
   
  `kSEMC_Dbi_BurstLen8`,
   
  `kSEMC_Dbi_BurstLen16`,
   
  `kSEMC_Dbi_BurstLen32`,
   
  `kSEMC_Dbi_BurstLen64` }
   
    *SEMC dbi burst length.*
- enum `semc_iomux_pin` {
   
  `kSEMC_MUXA8` = `SEMC_IOCR_MUX_A8_SHIFT`,
   
  `kSEMC_MUXCSX0` = `SEMC_IOCR_MUX_CSX0_SHIFT`,
   
  `kSEMC_MUXCSX1` = `SEMC_IOCR_MUX_CSX1_SHIFT`,
   
  `kSEMC_MUXCSX2` = `SEMC_IOCR_MUX_CSX2_SHIFT`,
   
  `kSEMC_MUXCSX3` = `SEMC_IOCR_MUX_CSX3_SHIFT`,
   
  `kSEMC_MUXRDY` = `SEMC_IOCR_MUX_RDY_SHIFT` }
   
    *SEMC IOMUXC.*
- enum `semc_iomux_nora27_pin` {
   
  `kSEMC_MORA27_NONE` = 0,
   
  `kSEMC_NORA27_MUXCSX3` = `SEMC_IOCR_MUX_CSX3_SHIFT`,
   
  `kSEMC_NORA27_MUXRDY` = `SEMC_IOCR_MUX_RDY_SHIFT` }
   
    *SEMC NOR/PSRAM Address bit 27 A27.*
- enum `smec_port_size_t` {
   
  `kSEMC_PortSize8Bit` = 0,
   
  `kSEMC_PortSize16Bit` }
   
    *SEMC port size.*
- enum `semc_addr_mode_t` {
   
  `kSEMC_AddrDataMux` = 0,
   
  `kSEMC_AdvAddrdataMux`,
   
  `kSEMC_AddrDataNonMux` }
   
    *SEMC address mode.*
- enum `semc_dqs_mode_t` {
   
  `kSEMC_Loopbackinternal` = 0,
   
  `kSEMC_Loopbackdqspad` }
   
    *SEMC DQS read strobe mode.*
- enum `semc_adv_polarity_t` {
   
  `kSEMC_AdvActiveLow` = 0,
   
  `kSEMC_AdvActiveHigh` }
   
    *SEMC ADV signal active polarity.*
- enum `semc_sync_mode_t` {
   
  `kSEMC_AsyncMode` = 0,
   
  `kSEMC_SyncMode` }
   
    *SEMC sync mode.*
- enum `semc_adv_level_control_t` {
   
  `kSEMC_AdvHigh` = 0,
   
  `kSEMC_AdvLow` }
   
    *SEMC ADV signal level control.*

- enum `semc_rdy_polarity_t` {
   
  `kSEMC_RdyActiveLow` = 0,
   
  `kSEMC_RdyActivehigh` }
   
    *SEMC RDY signal active polarity.*
- enum `semc_ipcmd_nand_addrmode_t` {
   
  `kSEMC_NANDAM_ColumnRow` = 0x0U,
   
  `kSEMC_NANDAM_ColumnCA0`,
   
  `kSEMC_NANDAM_ColumnCA0CA1`,
   
  `kSEMC_NANDAM_RawRA0`,
   
  `kSEMC_NANDAM_RawRA0RA1`,
   
  `kSEMC_NANDAM_RawRA0RA1RA2` }
   
    *SEMC IP command for NAND: address mode.*
- enum `semc_ipcmd_nand_cmdmode_t` {
   
  `kSEMC_NANDCM_Command` = 0x2U,
   
  `kSEMC_NANDCM_CommandHold`,
   
  `kSEMC_NANDCM_CommandAddress`,
   
  `kSEMC_NANDCM_CommandAddressHold`,
   
  `kSEMC_NANDCM_CommandAddressRead`,
   
  `kSEMC_NANDCM_CommandAddressWrite`,
   
  `kSEMC_NANDCM_CommandRead`,
   
  `kSEMC_NANDCM_CommandWrite`,
   
  `kSEMC_NANDCM_Read`,
   
  `kSEMC_NANDCM_Write` }
   
    *SEMC IP command for NAND command mode.*
- enum `semc_nand_address_option_t` {
   
  `kSEMC_NandAddrOption_5byte_CA2RA3` = 0U,
   
  `kSEMC_NandAddrOption_4byte_CA2RA2` = 2U,
   
  `kSEMC_NandAddrOption_3byte_CA2RA1` = 4U,
   
  `kSEMC_NandAddrOption_4byte_CA1RA3` = 1U,
   
  `kSEMC_NandAddrOption_3byte_CA1RA2` = 3U,
   
  `kSEMC_NandAddrOption_2byte_CA1RA1` = 7U } }
   
    *SEMC NAND address option.*
- enum `semc_ipcmd_nor_dbi_t` {
   
  `kSEMC_NORDBICM_Read` = 0x2U,
   
  `kSEMC_NORDBICM_Write` }
   
    *SEMC IP command for NOR.*
- enum `semc_ipcmd_sram_t` {
   
  `kSEMC_SRAMCM_ArrayRead` = 0x2U,
   
  `kSEMC_SRAMCM_ArrayWrite`,
   
  `kSEMC_SRAMCM_RegRead`,
   
  `kSEMC_SRAMCM_RegWrite` }
   
    *SEMC IP command for SRAM.*
- enum `semc_ipcmd_sdram_t` {

```
kSEMC_SDRAMCM_Read = 0x8U,
kSEMC_SDRAMCM_Write,
kSEMC_SDRAMCM_Modeset,
kSEMC_SDRAMCM_Active,
kSEMC_SDRAMCM_AutoRefresh,
kSEMC_SDRAMCM_SelfRefresh,
kSEMC_SDRAMCM_Prefetch,
kSEMC_SDRAMCM_Prefetchall }
```

*SEMC IP command for SDARM.*

## Driver version

- #define **FSL\_SEMC\_DRIVER\_VERSION** (MAKE\_VERSION(2, 6, 0))  
*SEMC driver version.*

## SEMC Initialization and De-initialization

- void **SEMC\_GetDefaultConfig** (semc\_config\_t \*config)  
*Gets the SEMC default basic configuration structure.*
- void **SEMC\_Init** (SEMC\_Type \*base, semc\_config\_t \*configure)  
*Initializes SEMC.*
- void **SEMC\_Deinit** (SEMC\_Type \*base)  
*Deinitializes the SEMC module and gates the clock.*

## SEMC Configuration Operation For Each Memory Type

- status\_t **SEMC\_ConfigureSDRAM** (SEMC\_Type \*base, semc\_sdram\_cs\_t cs, semc\_sdram\_config\_t \*config, uint32\_t clkSrc\_Hz)  
*Configures SDRAM controller in SEMC.*
- status\_t **SEMC\_ConfigureNAND** (SEMC\_Type \*base, semc\_nand\_config\_t \*config, uint32\_t clkSrc\_Hz)  
*Configures NAND controller in SEMC.*
- status\_t **SEMC\_ConfigureNOR** (SEMC\_Type \*base, semc\_nor\_config\_t \*config, uint32\_t clkSrc\_Hz)  
*Configures NOR controller in SEMC.*
- status\_t **SEMC\_ConfigureSRAMWithChipSelection** (SEMC\_Type \*base, semc\_sram\_cs\_t cs, semc\_sram\_config\_t \*config, uint32\_t clkSrc\_Hz)  
*Configures SRAM controller in SEMC.*
- status\_t **SEMC\_ConfigureSRAM** (SEMC\_Type \*base, semc\_sram\_config\_t \*config, uint32\_t clkSrc\_Hz)  
*Configures SRAM controller in SEMC.*
- status\_t **SEMC\_ConfigureDBI** (SEMC\_Type \*base, semc\_dbi\_config\_t \*config, uint32\_t clkSrc\_Hz)  
*Configures DBI controller in SEMC.*

## SEMC Interrupt Operation

- static void **SEMC\_EnableInterrupts** (SEMC\_Type \*base, uint32\_t mask)  
*Enables the SEMC interrupt.*

- static void **SEMC\_DisableInterrupts** (SEMC\_Type \*base, uint32\_t mask)  
*Disables the SEMC interrupt.*
- static bool **SEMC\_GetStatusFlag** (SEMC\_Type \*base)  
*Gets the SEMC status.*
- static void **SEMC\_ClearStatusFlags** (SEMC\_Type \*base, uint32\_t mask)  
*Clears the SEMC status flag state.*

## SEMC Memory Access Operation

- static bool **SEMC\_IsInIdle** (SEMC\_Type \*base)  
*Check if SEMC is in idle.*
- **status\_t SEMC\_SendIPCommand** (SEMC\_Type \*base, **semc\_mem\_type\_t** memType, uint32\_t address, uint32\_t command, uint32\_t write, uint32\_t \*read)  
*SEMC IP command access.*
- static uint16\_t **SEMC\_BuildNandIPCommand** (uint8\_t userCommand, **semc\_ipcmd\_nand\_addrmode\_t** addrMode, **semc\_ipcmd\_nand\_cmdmode\_t** cmdMode)  
*Build SEMC IP command for NAND.*
- static bool **SEMC\_IsNandReady** (SEMC\_Type \*base)  
*Check if the NAND device is ready.*
- **status\_t SEMC\_IPCommandNandWrite** (SEMC\_Type \*base, uint32\_t address, uint8\_t \*data, uint32\_t size\_bytes)  
*SEMC NAND device memory write through IP command.*
- **status\_t SEMC\_IPCommandNandRead** (SEMC\_Type \*base, uint32\_t address, uint8\_t \*data, uint32\_t size\_bytes)  
*SEMC NAND device memory read through IP command.*
- **status\_t SEMC\_IPCommandNorWrite** (SEMC\_Type \*base, uint32\_t address, uint8\_t \*data, uint32\_t size\_bytes)  
*SEMC NOR device memory write through IP command.*
- **status\_t SEMC\_IPCommandNorRead** (SEMC\_Type \*base, uint32\_t address, uint8\_t \*data, uint32\_t size\_bytes)  
*SEMC NOR device memory read through IP command.*

## 41.4 Data Structure Documentation

### 41.4.1 struct semc\_sdram\_config\_t

1. The memory size in the configuration is in the unit of KB. So memsize\_kbytes should be set as  $2^{^2}$ ,  $2^{^3}$ ,  $2^{^4}$  .etc which is base 2KB exponential function. Take refer to BR0~BR3 register in RM for details.
2. The prescalePeriod\_N16Cycle is in unit of 16 clock cycle. It is a exception for prescaleTimer\_n16cycle = 0, it means the prescaler timer period is  $256 * 16$  clock cycles. For prescalerIf prescaleTimer\_n16cycle not equal to 0, The prescaler timer period is prescalePeriod\_N16Cycle \* 16 clock cycles. idleTimeout\_NprescalePeriod, refreshUrgThreshold\_NprescalePeriod, refreshPeriod\_NprescalePeriod are similar to prescalePeriod\_N16Cycle.

### Data Fields

- **semc\_iomux\_pin** csxPinMux

- *CS pin mux.*
- `uint32_t address`  
*The base address.*
- `uint32_t memsize_kbytes`  
*The memory size in unit of kbytes.*
- `smec_port_size_t portSize`  
*Port size.*
- `sem_sdram_burst_len_t burstLen`  
*Burst length.*
- `semc_sdram_column_bit_num_t columnAddrBitNum`  
*Column address bit number.*
- `semc_caslatency_t casLatency`  
*CAS latency.*
- `uint8_t tPrecharge2Act_Ns`  
*Precharge to active wait time in unit of nanosecond.*
- `uint8_t tAct2ReadWrite_Ns`  
*Act to read/write wait time in unit of nanosecond.*
- `uint8_t tRefreshRecovery_Ns`  
*Refresh recovery time in unit of nanosecond.*
- `uint8_t tWriteRecovery_Ns`  
*write recovery time in unit of nanosecond.*
- `uint8_t tCkeOff_Ns`  
*CKE off minimum time in unit of nanosecond.*
- `uint8_t tAct2Precharge_Ns`  
*Active to precharge in unit of nanosecond.*
- `uint8_t tSelfRefRecovery_Ns`  
*Self refresh recovery time in unit of nanosecond.*
- `uint8_t tRefresh2Refresh_Ns`  
*Refresh to refresh wait time in unit of nanosecond.*
- `uint8_t tAct2Act_Ns`  
*Active to active wait time in unit of nanosecond.*
- `uint32_t tPrescalePeriod_Ns`  
*Prescaler timer period should not be larger than  $256 * 16 * \text{clock cycle}$ .*
- `uint32_t tIdleTimeout_Ns`  
*Idle timeout in unit of prescale time period.*
- `uint32_t refreshPeriod_nsPerRow`  
*Refresh timer period like  $64\text{ms} * 1000000 / 8192$ .*
- `uint32_t refreshUrgThreshold`  
*Refresh urgent threshold.*
- `uint8_t refreshBurstLen`  
*Refresh burst length.*

## Field Documentation

### (1) `semc_iomux_pin semc_sdram_config_t::csxPinMux`

The kSEMC\_MUXA8 is not valid in sdram pin mux setting.

- (2) `uint32_t semc_sdrdram_config_t::address`
- (3) `uint32_t semc_sdrdram_config_t::memsize_kbytes`
- (4) `smec_port_size_t semc_sdrdram_config_t::portSize`
- (5) `sem_sdrdram_burst_len_t semc_sdrdram_config_t::burstLen`
- (6) `semc_sdrdram_column_bit_num_t semc_sdrdram_config_t::columnAddrBitNum`
- (7) `semc_caslatency_t semc_sdrdram_config_t::casLatency`
- (8) `uint8_t semc_sdrdram_config_t::tPrecharge2Act_Ns`
- (9) `uint8_t semc_sdrdram_config_t::tAct2ReadWrite_Ns`
- (10) `uint8_t semc_sdrdram_config_t::tRefreshRecovery_Ns`
- (11) `uint8_t semc_sdrdram_config_t::tWriteRecovery_Ns`
- (12) `uint8_t semc_sdrdram_config_t::tCkeOff_Ns`
- (13) `uint8_t semc_sdrdram_config_t::tAct2Prechage_Ns`
- (14) `uint8_t semc_sdrdram_config_t::tSelfRefRecovery_Ns`
- (15) `uint8_t semc_sdrdram_config_t::tRefresh2Refresh_Ns`
- (16) `uint8_t semc_sdrdram_config_t::tAct2Act_Ns`
- (17) `uint32_t semc_sdrdram_config_t::tPrescalePeriod_Ns`
- (18) `uint32_t semc_sdrdram_config_t::tIdleTimeout_Ns`
- (19) `uint32_t semc_sdrdram_config_t::refreshPeriod_nsPerRow`
- (20) `uint32_t semc_sdrdram_config_t::refreshUrgThreshold`
- (21) `uint8_t semc_sdrdram_config_t::refreshBurstLen`

#### 41.4.2 struct semc\_nand\_timing\_config\_t

##### Data Fields

- `uint8_t tCeSetup_Ns`  
*CE setup time: tCS.*
- `uint8_t tCeHold_Ns`  
*CE hold time: tCH.*
- `uint8_t tCeInterval_Ns`  
*CE interval time:tCEITV.*

- `uint8_t tWeLow_Ns`  
*WE low time: tWP.*
- `uint8_t tWeHigh_Ns`  
*WE high time: tWH.*
- `uint8_t tReLow_Ns`  
*RE low time: tRP.*
- `uint8_t tReHigh_Ns`  
*RE high time: tREH.*
- `uint8_t tTurnAround_Ns`  
*Turnaround time for async mode: tTA.*
- `uint8_t tWehigh2Relow_Ns`  
*WE# high to RE# wait time: tWHR.*
- `uint8_t tRehigh2Welow_Ns`  
*RE# high to WE# low wait time: tRHW.*
- `uint8_t tAle2WriteStart_Ns`  
*ALE to write start wait time: tADL.*
- `uint8_t tReady2Relow_Ns`  
*Ready to RE# low min wait time: tRR.*
- `uint8_t tWehigh2Busy_Ns`  
*WE# high to busy wait time: tWB.*

## Field Documentation

- (1) `uint8_t semc_nand_timing_config_t::tCeSetup_Ns`
- (2) `uint8_t semc_nand_timing_config_t::tCeHold_Ns`
- (3) `uint8_t semc_nand_timing_config_t::tCeInterval_Ns`
- (4) `uint8_t semc_nand_timing_config_t::tWeLow_Ns`
- (5) `uint8_t semc_nand_timing_config_t::tWeHigh_Ns`
- (6) `uint8_t semc_nand_timing_config_t::tReLow_Ns`
- (7) `uint8_t semc_nand_timing_config_t::tReHigh_Ns`
- (8) `uint8_t semc_nand_timing_config_t::tTurnAround_Ns`
- (9) `uint8_t semc_nand_timing_config_t::tWehigh2Below_Ns`
- (10) `uint8_t semc_nand_timing_config_t::tRehigh2Below_Ns`
- (11) `uint8_t semc_nand_timing_config_t::tAle2WriteStart_Ns`
- (12) `uint8_t semc_nand_timing_config_t::tReady2Below_Ns`
- (13) `uint8_t semc_nand_timing_config_t::tWehigh2Busy_Ns`

### 41.4.3 struct semc\_nand\_config\_t

## Data Fields

- `semc_iomux_pin cePinMux`  
*The CE pin mux setting.*
- `uint32_t axiAddress`  
*The base address for AXI nand.*
- `uint32_t axiMemsize_kbytes`  
*The memory size in unit of kbytes for AXI nand.*
- `uint32_t ipgAddress`  
*The base address for IPG nand .*
- `uint32_t ipgMemsize_kbytes`  
*The memory size in unit of kbytes for IPG nand.*
- `semc_rdy_polarity_t rdyactivePolarity`  
*Wait ready polarity.*
- `bool edoModeEnabled`  
*EDO mode enabled.*
- `semc_nand_column_bit_num_t columnAddrBitNum`  
*Column address bit number.*
- `semc_nand_address_option_t arrayAddrOption`  
*Address option.*

- `sem_nand_burst_len_t burstLen`  
*Burst length.*
- `smec_port_size_t portSize`  
*Port size.*
- `semc_nand_timing_config_t * timingConfig`  
*SEMC nand timing configuration.*

## Field Documentation

(1) `semc_iomux_pin semc_nand_config_t::cePinMux`

The kSEMCMUXRDY is not valid for CE pin setting.

(2) `uint32_t semc_nand_config_t::axiAddress`

(3) `uint32_t semc_nand_config_t::axiMemsize_kbytes`

(4) `uint32_t semc_nand_config_t::ipgAddress`

(5) `uint32_t semc_nand_config_t::ipgMemsize_kbytes`

(6) `semc_rdy_polarity_t semc_nand_config_t::rdyactivePolarity`

(7) `bool semc_nand_config_t::edoModeEnabled`

(8) `semc_nand_column_bit_num_t semc_nand_config_t::columnAddrBitNum`

(9) `semc_nand_address_option_t semc_nand_config_t::arrayAddrOption`

(10) `sem_nand_burst_len_t semc_nand_config_t::burstLen`

(11) `smec_port_size_t semc_nand_config_t::portSize`

(12) `semc_nand_timing_config_t* semc_nand_config_t::timingConfig`

### 41.4.4 struct semc\_nor\_config\_t

## Data Fields

- `semc_iomux_pin cePinMux`  
*The CE# pin mux setting.*
- `semc_iomux_nora27_pin addr27`  
*The Addr bit 27 pin mux setting.*
- `uint32_t address`  
*The base address.*
- `uint32_t memsize_kbytes`  
*The memory size in unit of kbytes.*
- `uint8_t addrPortWidth`  
*The address port width.*
- `semc_rdy_polarity_t rdyactivePolarity`

- **semc\_adv\_polarity\_t advActivePolarity**  
*ADV# polarity.*
- **semc\_norsram\_column\_bit\_num\_t columnAddrBitNum**  
*Column address bit number.*
- **semc\_addr\_mode\_t addrMode**  
*Address mode.*
- **sem\_norsram\_burst\_len\_t burstLen**  
*Burst length.*
- **smec\_port\_size\_t portSize**  
*Port size.*
- **uint8\_t tCeSetup\_Ns**  
*The CE setup time.*
- **uint8\_t tCeHold\_Ns**  
*The CE hold time.*
- **uint8\_t tCeInterval\_Ns**  
*CE interval minimum time.*
- **uint8\_t tAddrSetup\_Ns**  
*The address setup time.*
- **uint8\_t tAddrHold\_Ns**  
*The address hold time.*
- **uint8\_t tWeLow\_Ns**  
*WE low time for async mode.*
- **uint8\_t tWeHigh\_Ns**  
*WE high time for async mode.*
- **uint8\_t tReLow\_Ns**  
*RE low time for async mode.*
- **uint8\_t tReHigh\_Ns**  
*RE high time for async mode.*
- **uint8\_t tTurnAround\_Ns**  
*Turnaround time for async mode.*
- **uint8\_t tAddr2WriteHold\_Ns**  
*Address to write data hold time for async mode.*
- **uint8\_t latencyCount**  
*Latency count for sync mode.*
- **uint8\_t readCycle**  
*Read cycle time for sync mode.*



**Field Documentation**

- (1) `semc_iomux_pin semc_nor_config_t::cePinMux`
- (2) `semc_iomux_nora27_pin semc_nor_config_t::addr27`
- (3) `uint32_t semc_nor_config_t::address`
- (4) `uint32_t semc_nor_config_t::memsize_kbytes`
- (5) `uint8_t semc_nor_config_t::addrPortWidth`
- (6) `semc_rdy_polarity_t semc_nor_config_t::rdyactivePolarity`
- (7) `semc_adv_polarity_t semc_nor_config_t::advActivePolarity`
- (8) `semc_norsram_column_bit_num_t semc_nor_config_t::columnAddrBitNum`
- (9) `semc_addr_mode_t semc_nor_config_t::addrMode`
- (10) `sem_norsram_burst_len_t semc_nor_config_t::burstLen`
- (11) `smec_port_size_t semc_nor_config_t::portSize`
- (12) `uint8_t semc_nor_config_t::tCeSetup_Ns`
- (13) `uint8_t semc_nor_config_t::tCeHold_Ns`
- (14) `uint8_t semc_nor_config_t::tCeInterval_Ns`
- (15) `uint8_t semc_nor_config_t::tAddrSetup_Ns`
- (16) `uint8_t semc_nor_config_t::tAddrHold_Ns`
- (17) `uint8_t semc_nor_config_t::tWeLow_Ns`
- (18) `uint8_t semc_nor_config_t::tWeHigh_Ns`
- (19) `uint8_t semc_nor_config_t::tReLow_Ns`
- (20) `uint8_t semc_nor_config_t::tReHigh_Ns`
- (21) `uint8_t semc_nor_config_t::tTurnAround_Ns`
- (22) `uint8_t semc_nor_config_t::tAddr2WriteHold_Ns`
- (23) `uint8_t semc_nor_config_t::latencyCount`
- (24) `uint8_t semc_nor_config_t::readCycle`

**41.4.5 struct semc\_sram\_config\_t****Data Fields**

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- `semc_iomux_pin cePinMux`

- **The CE# pin mux setting.**
- **semc\_iomux\_nora27\_pin addr27**  
The Addr bit 27 pin mux setting.
- **uint32\_t address**  
The base address.
- **uint32\_t memsize\_kbytes**  
The memory size in unit of kbytes.
- **uint8\_t addrPortWidth**  
The address port width.
- **semc\_adv\_polarity\_t advActivePolarity**  
ADV# polarity 1: active high, 0: active low.
- **semc\_addr\_mode\_t addrMode**  
Address mode.
- **sem\_norsram\_burst\_len\_t burstLen**  
Burst length.
- **smec\_port\_size\_t portSize**  
Port size.
- **semc\_sync\_mode\_t syncMode**  
Sync mode.
- **semc\_adv\_level\_control\_t advLevelCtrl**  
ADV# level control during address hold state, 1: low, 0: high.
- **uint8\_t tCeSetup\_Ns**  
The CE setup time.
- **uint8\_t tCeHold\_Ns**  
The CE hold time.
- **uint8\_t tCeInterval\_Ns**  
CE interval minimum time.
- **uint8\_t readHoldTime\_Ns**  
read hold time.
- **uint8\_t tAddrSetup\_Ns**  
The address setup time.
- **uint8\_t tAddrHold\_Ns**  
The address hold time.
- **uint8\_t tWeLow\_Ns**  
WE low time for async mode.
- **uint8\_t tWeHigh\_Ns**  
WE high time for async mode.
- **uint8\_t tReLow\_Ns**  
RE low time for async mode.
- **uint8\_t tReHigh\_Ns**  
RE high time for async mode.
- **uint8\_t tTurnAround\_Ns**  
Turnaround time for async mode.
- **uint8\_t tAddr2WriteHold\_Ns**  
Address to write data hold time for async mode.
- **uint8\_t tWriteSetup\_Ns**  
Write data setup time for sync mode.
- **uint8\_t tWriteHold\_Ns**  
Write hold time for sync mode.
- **uint8\_t latencyCount**  
Latency count for sync mode.

- `uint8_t readCycle`  
*Read cycle time for sync mode.*



## Field Documentation

- (1) `semc_iomux_pin semc_sram_config_t::cePinMux`
- (2) `semc_iomux_nora27_pin semc_sram_config_t::addr27`
- (3) `uint32_t semc_sram_config_t::address`
- (4) `uint32_t semc_sram_config_t::memsize_kbytes`
- (5) `uint8_t semc_sram_config_t::addrPortWidth`
- (6) `semc_adv_polarity_t semc_sram_config_t::advActivePolarity`
- (7) `semc_addr_mode_t semc_sram_config_t::addrMode`
- (8) `sem_norsram_burst_len_t semc_sram_config_t::burstLen`
- (9) `smec_port_size_t semc_sram_config_t::portSize`
- (10) `semc_sync_mode_t semc_sram_config_t::syncMode`
- (11) `semc_adv_level_control_t semc_sram_config_t::advLevelCtrl`
- (12) `uint8_t semc_sram_config_t::tCeSetup_Ns`
- (13) `uint8_t semc_sram_config_t::tCeHold_Ns`
- (14) `uint8_t semc_sram_config_t::tCeInterval_Ns`
- (15) `uint8_t semc_sram_config_t::readHoldTime_Ns`
- (16) `uint8_t semc_sram_config_t::tAddrSetup_Ns`
- (17) `uint8_t semc_sram_config_t::tAddrHold_Ns`
- (18) `uint8_t semc_sram_config_t::tWeLow_Ns`
- (19) `uint8_t semc_sram_config_t::tWeHigh_Ns`
- (20) `uint8_t semc_sram_config_t::tReLow_Ns`
- (21) `uint8_t semc_sram_config_t::tReHigh_Ns`
- (22) `uint8_t semc_sram_config_t::tTurnAround_Ns`
- (23) `uint8_t semc_sram_config_t::tAddr2WriteHold_Ns`
- (24) `uint8_t semc_sram_config_t::tWriteSetup_Ns`
- (25) `uint8_t semc_sram_config_t::tWriteHold_Ns`
- (26) `uint8_t semc_sram_config_t::latencyCount`
- (27) `uint8_t semc_sram_config_t::readCycle`

*The CE# pin mux.*

- `uint32_t address`

*The base address.*

- `uint32_t memsize_kbytes`

*The memory size in unit of 4kbytes.*

- `semc_db_i_column_bit_num_t columnAddrBitNum`

*Column address bit number.*

- `sem_db_i_burst_len_t burstLen`

*Burst length.*

- `smec_port_size_t portSize`

*Port size.*

- `uint8_t tCsxSetup_Ns`

*The CSX setup time.*

- `uint8_t tCsxHold_Ns`

*The CSX hold time.*

- `uint8_t tWexLow_Ns`

*WEX low time.*

- `uint8_t tWexHigh_Ns`

*WEX high time.*

- `uint8_t tRdxLow_Ns`

*RDX low time.*

- `uint8_t tRdxHigh_Ns`

*RDX high time.*

- `uint8_t tCsxInterval_Ns`

*Write data setup time.*

**Field Documentation**

- (1) `semc_iomux_pin semc_dbi_config_t::csxPinMux`
- (2) `uint32_t semc_dbi_config_t::address`
- (3) `uint32_t semc_dbi_config_t::memsize_kbytes`
- (4) `semc_dbi_column_bit_num_t semc_dbi_config_t::columnAddrBitNum`
- (5) `sem_dbi_burst_len_t semc_dbi_config_t::burstLen`
- (6) `smec_port_size_t semc_dbi_config_t::portSize`
- (7) `uint8_t semc_dbi_config_t::tCsxSetup_Ns`
- (8) `uint8_t semc_dbi_config_t::tCsxHold_Ns`
- (9) `uint8_t semc_dbi_config_t::tWexLow_Ns`
- (10) `uint8_t semc_dbi_config_t::tWexHigh_Ns`
- (11) `uint8_t semc_dbi_config_t::tRdxLow_Ns`
- (12) `uint8_t semc_dbi_config_t::tRdxHigh_Ns`
- (13) `uint8_t semc_dbi_config_t::tCsxInterval_Ns`

**41.4.7 struct semc\_queuea\_weight\_struct\_t****Data Fields**

- `uint32_t qos`: 4  
*weight of qos for queue 0 .*
- `uint32_t aging`: 4  
*weight of aging for queue 0.*
- `uint32_t slaveHitNoswitch`: 8  
*weight of read/write no switch for queue 0 .*
- `uint32_t slaveHitSwitch`: 8  
*weight of read/write switch for queue 0.*

**Field Documentation**

- (1) `uint32_t semc_queuea_weight_struct_t::qos`
- (2) `uint32_t semc_queuea_weight_struct_t::aging`
- (3) `uint32_t semc_queuea_weight_struct_t::slaveHitNoswitch`
- (4) `uint32_t semc_queuea_weight_struct_t::slaveHitSwitch`

**41.4.8 union semc\_queuea\_weight\_t****Data Fields**

- `semc_queuea_weight_struct_t queueaConfig`  
*Structure configuration for queueA.*
- `uint32_t queueaValue`  
*Configuration value for queueA which could directly write to the reg.*

**Field Documentation**

- (1) `semc_queuea_weight_struct_t semc_queuea_weight_t::queueaConfig`
- (2) `uint32_t semc_queuea_weight_t::queueaValue`

**41.4.9 struct semc\_queueb\_weight\_struct\_t****Data Fields**

- `uint32_t qos: 4`  
*weight of qos for queue 1.*
- `uint32_t aging: 4`  
*weight of aging for queue 1.*
- `uint32_t weightPagehit: 8`  
*weight of page hit for queue 1 only .*
- `uint32_t slaveHitNoswitch: 8`  
*weight of read/write no switch for queue 1.*
- `uint32_t bankRotation: 8`  
*weight of bank rotation for queue 1 only .*

**Field Documentation**

- (1) `uint32_t semc_queueb_weight_struct_t::qos`
- (2) `uint32_t semc_queueb_weight_struct_t::aging`
- (3) `uint32_t semc_queueb_weight_struct_t::weightPagehit`
- (4) `uint32_t semc_queueb_weight_struct_t::slaveHitNoswitch`
- (5) `uint32_t semc_queueb_weight_struct_t::bankRotation`

**41.4.10 union semc\_queueb\_weight\_t****Data Fields**

- `semc_queueb_weight_struct_t queuebConfig`  
*Structure configuration for queueB.*
- `uint32_t queuebValue`  
*Configuration value for queueB which could directly write to the reg.*

**Field Documentation**

- (1) `semc_queueb_weight_struct_t semc_queueb_weight_t::queuebConfig`
- (2) `uint32_t semc_queueb_weight_t::queuebValue`

**41.4.11 struct semc\_axi\_queueweight\_t****Data Fields**

- `bool queueaEnable`  
*Enable queue a.*
- `semc_queuea_weight_t queueaWeight`  
*Weight settings for queue a.*
- `bool queuebEnable`  
*Enable queue b.*
- `semc_queueb_weight_t queuebWeight`  
*Weight settings for queue b.*

**Field Documentation**

- (1) **bool semc\_axi\_queueweight\_t::queueaEnable**
- (2) **semc\_queuea\_weight\_t semc\_axi\_queueweight\_t::queueaWeight**
- (3) **bool semc\_axi\_queueweight\_t::queuebEnable**
- (4) **semc\_queueb\_weight\_t semc\_axi\_queueweight\_t::queuebWeight**

**41.4.12 struct semc\_config\_t**

**busTimeoutCycles:** when busTimeoutCycles is zero, the bus timeout cycle is 255\*1024. otherwise the bus timeout cycles is busTimeoutCycles\*1024. **cmdTimeoutCycles:** is used for command execution timeout cycles. it's similar to the busTimeoutCycles.

**Data Fields**

- **semc\_dqs\_mode\_t dqsMode**  
*Dummy read strobe mode: use enum in "semc\_dqs\_mode\_t".*
- **uint8\_t cmdTimeoutCycles**  
*Command execution timeout cycles.*
- **uint8\_t busTimeoutCycles**  
*Bus timeout cycles.*
- **semc\_axi\_queueweight\_t queueWeight**  
*AXI queue weight.*

**Field Documentation**

- (1) **semc\_dqs\_mode\_t semc\_config\_t::dqsMode**
- (2) **uint8\_t semc\_config\_t::cmdTimeoutCycles**
- (3) **uint8\_t semc\_config\_t::busTimeoutCycles**
- (4) **semc\_axi\_queueweight\_t semc\_config\_t::queueWeight**

**41.5 Macro Definition Documentation****41.5.1 #define FSL\_SEMC\_DRIVER\_VERSION (MAKE\_VERSION(2, 6, 0))****41.6 Enumeration Type Documentation****41.6.1 anonymous enum**

Enumerator

**kStatus\_SEMC\_InvalidDeviceType** Invalid device type.

**kStatus\_SEMC\_IpCommandExecutionError** IP command execution error.

*kStatus\_SEMC\_AxiCommandExecutionError* AXI command execution error.  
*kStatus\_SEMC\_InvalidMemorySize* Invalid memory sie.  
*kStatus\_SEMC\_InvalidIpCmdDataSize* Invalid IP command data size.  
*kStatus\_SEMC\_InvalidAddressPortWidth* Invalid address port width.  
*kStatus\_SEMC\_InvalidDataPortWidth* Invalid data port width.  
*kStatus\_SEMC\_InvalidSwPinmuxSelection* Invalid SW pinmux selection.  
*kStatus\_SEMC\_InvalidBurstLength* Invalid burst length.  
*kStatus\_SEMC\_InvalidColumnAddressBitWidth* Invalid column address bit width.  
*kStatus\_SEMC\_InvalidBaseAddress* Invalid base address.  
*kStatus\_SEMC\_InvalidTimerSetting* Invalid timer setting.

#### 41.6.2 enum semc\_mem\_type\_t

Enumerator

*kSEMC\_MemType\_SDRAM* SDRAM.  
*kSEMC\_MemType\_SRAM* SRAM.  
*kSEMC\_MemType\_NOR* NOR.  
*kSEMC\_MemType\_NAND* NAND.  
*kSEMC\_MemType\_8080* 1.

#### 41.6.3 enum semc\_waitready\_polarity\_t

Enumerator

*kSEMC\_LowActive* Low active.  
*kSEMC\_HighActive* High active.

#### 41.6.4 enum semc\_sdram\_cs\_t

Enumerator

*kSEMC\_SDRAM\_CS0* SEMC SDRAM CS0.  
*kSEMC\_SDRAM\_CS1* SEMC SDRAM CS1.  
*kSEMC\_SDRAM\_CS2* SEMC SDRAM CS2.  
*kSEMC\_SDRAM\_CS3* SEMC SDRAM CS3.

#### 41.6.5 enum semc\_sram\_cs\_t

Enumerator

*kSEMC\_SRAM\_CS0* SEMC SRAM CS0.

#### 41.6.6 enum semc\_nand\_access\_type\_t

Enumerator

*kSEMC\_NAND\_ACCESS\_BY\_AXI* Access to NAND flash by AXI bus.

*kSEMC\_NAND\_ACCESS\_BY\_IPCMD* Access to NAND flash by IP bus.

#### 41.6.7 enum semc\_interrupt\_enable\_t

Enumerator

*kSEMC\_IPCmdDoneInterrupt* Ip command done interrupt.

*kSEMC\_IPCmdErrInterrupt* Ip command error interrupt.

*kSEMC\_AXICmdErrInterrupt* AXI command error interrupt.

*kSEMC\_AXIBusErrInterrupt* AXI bus error interrupt.

#### 41.6.8 enum semc\_ipcmd\_datasize\_t

Enumerator

*kSEMC\_IPcmdDataSize\_1bytes* The IP command data size 1 byte.

*kSEMC\_IPcmdDataSize\_2bytes* The IP command data size 2 byte.

*kSEMC\_IPcmdDataSize\_3bytes* The IP command data size 3 byte.

*kSEMC\_IPcmdDataSize\_4bytes* The IP command data size 4 byte.

#### 41.6.9 enum semc\_refresh\_time\_t

Enumerator

*kSEMC\_RefreshThreeClocks* The refresh timing with three bus clocks.

*kSEMC\_RefreshSixClocks* The refresh timing with six bus clocks.

*kSEMC\_RefreshNineClocks* The refresh timing with nine bus clocks.

#### 41.6.10 enum semc\_caslatency\_t

Enumerator

*kSEMC\_LatencyOne* Latency 1.

*kSEMC\_LatencyTwo* Latency 2.

*kSEMC\_LatencyThree* Latency 3.

**41.6.11 enum semc\_sdrdram\_column\_bit\_num\_t**

Enumerator

*kSEMC\_SdramColumn\_12bit* 12 bit.  
*kSEMC\_SdramColumn\_11bit* 11 bit.  
*kSEMC\_SdramColumn\_10bit* 10 bit.  
*kSEMC\_SdramColumn\_9bit* 9 bit.  
*kSEMC\_SdramColumn\_8bit* 8 bit.

**41.6.12 enum sem\_sdrdram\_burst\_len\_t**

Enumerator

*kSEMC\_Sdram\_BurstLen1* According to ERR050577, Auto-refresh command may possibly fail to be triggered during long time back-to-back write (or read) when SDRAM controller's burst length is greater than 1. Burst length 1  
*kSEMC\_Sdram\_BurstLen2* Burst length 2.  
*kSEMC\_Sdram\_BurstLen4* Burst length 4.  
*kSEMC\_Sdram\_BurstLen8* Burst length 8.

**41.6.13 enum semc\_nand\_column\_bit\_num\_t**

Enumerator

*kSEMC\_NandColum\_16bit* 16 bit.  
*kSEMC\_NandColum\_15bit* 15 bit.  
*kSEMC\_NandColum\_14bit* 14 bit.  
*kSEMC\_NandColum\_13bit* 13 bit.  
*kSEMC\_NandColum\_12bit* 12 bit.  
*kSEMC\_NandColum\_11bit* 11 bit.  
*kSEMC\_NandColum\_10bit* 10 bit.  
*kSEMC\_NandColum\_9bit* 9 bit.

**41.6.14 enum sem\_nand\_burst\_len\_t**

Enumerator

*kSEMC\_Nand\_BurstLen1* Burst length 1.  
*kSEMC\_Nand\_BurstLen2* Burst length 2.  
*kSEMC\_Nand\_BurstLen4* Burst length 4.  
*kSEMC\_Nand\_BurstLen8* Burst length 8.

*kSEMC\_Nand\_BurstLen16* Burst length 16.  
*kSEMC\_Nand\_BurstLen32* Burst length 32.  
*kSEMC\_Nand\_BurstLen64* Burst length 64.

#### 41.6.15 enum semc\_norsram\_column\_bit\_num\_t

Enumerator

*kSEMC\_NorColum\_12bit* 12 bit.  
*kSEMC\_NorColum\_11bit* 11 bit.  
*kSEMC\_NorColum\_10bit* 10 bit.  
*kSEMC\_NorColum\_9bit* 9 bit.  
*kSEMC\_NorColum\_8bit* 8 bit.  
*kSEMC\_NorColum\_7bit* 7 bit.  
*kSEMC\_NorColum\_6bit* 6 bit.  
*kSEMC\_NorColum\_5bit* 5 bit.  
*kSEMC\_NorColum\_4bit* 4 bit.  
*kSEMC\_NorColum\_3bit* 3 bit.  
*kSEMC\_NorColum\_2bit* 2 bit.

#### 41.6.16 enum sem\_norsram\_burst\_len\_t

Enumerator

*kSEMC\_Nor\_BurstLen1* Burst length 1.  
*kSEMC\_Nor\_BurstLen2* Burst length 2.  
*kSEMC\_Nor\_BurstLen4* Burst length 4.  
*kSEMC\_Nor\_BurstLen8* Burst length 8.  
*kSEMC\_Nor\_BurstLen16* Burst length 16.  
*kSEMC\_Nor\_BurstLen32* Burst length 32.  
*kSEMC\_Nor\_BurstLen64* Burst length 64.

#### 41.6.17 enum semc\_dbm\_column\_bit\_num\_t

Enumerator

*kSEMC\_DbI\_Colum\_12bit* 12 bit.  
*kSEMC\_DbI\_Colum\_11bit* 11 bit.  
*kSEMC\_DbI\_Colum\_10bit* 10 bit.  
*kSEMC\_DbI\_Colum\_9bit* 9 bit.  
*kSEMC\_DbI\_Colum\_8bit* 8 bit.

*kSEMC\_Dbi\_Colum\_7bit* 7 bit.  
*kSEMC\_Dbi\_Colum\_6bit* 6 bit.  
*kSEMC\_Dbi\_Colum\_5bit* 5 bit.  
*kSEMC\_Dbi\_Colum\_4bit* 4 bit.  
*kSEMC\_Dbi\_Colum\_3bit* 3 bit.  
*kSEMC\_Dbi\_Colum\_2bit* 2 bit.

#### 41.6.18 enum sem\_dbi\_burst\_len\_t

Enumerator

*kSEMC\_Dbi\_BurstLen1* Burst length 1.  
*kSEMC\_Dbi\_BurstLen2* Burst length 2.  
*kSEMC\_Dbi\_Dbi\_BurstLen4* Burst length 4.  
*kSEMC\_Dbi\_BurstLen8* Burst length 8.  
*kSEMC\_Dbi\_BurstLen16* Burst length 16.  
*kSEMC\_Dbi\_BurstLen32* Burst length 32.  
*kSEMC\_Dbi\_BurstLen64* Burst length 64.

#### 41.6.19 enum semc\_iomux\_pin

Enumerator

*kSEMC\_MUXA8* MUX A8 pin.  
*kSEMC\_MUXCSX0* MUX CSX0 pin.  
*kSEMC\_MUXCSX1* MUX CSX1 Pin.  
*kSEMC\_MUXCSX2* MUX CSX2 Pin.  
*kSEMC\_MUXCSX3* MUX CSX3 Pin.  
*kSEMC\_MUXRDY* MUX RDY pin.

#### 41.6.20 enum semc\_iomux\_nora27\_pin

Enumerator

*kSEMC\_MORA27\_NONE* No NOR/SRAM A27 pin.  
*kSEMC\_NORA27\_MUXCSX3* MUX CSX3 Pin.  
*kSEMC\_NORA27\_MUXRDY* MUX RDY pin.

#### 41.6.21 enum smec\_port\_size\_t

Enumerator

*kSEMC\_PortSize8Bit* 8-Bit port size.

*kSEMC\_PortSize16Bit* 16-Bit port size.

#### 41.6.22 enum semc\_addr\_mode\_t

Enumerator

*kSEMC\_AddrDataMux* SEMC address/data mux mode.

*kSEMC\_AdvAddrdataMux* Advanced address/data mux mode.

*kSEMC\_AddrDataNonMux* Address/data non-mux mode.

#### 41.6.23 enum semc\_dqs\_mode\_t

Enumerator

*kSEMC\_Loopbackinternal* Dummy read strobe loopbacked internally.

*kSEMC\_Loopbackdqspad* Dummy read strobe loopbacked from DQS pad.

#### 41.6.24 enum semc\_adv\_polarity\_t

Enumerator

*kSEMC\_AdvActiveLow* Adv active low.

*kSEMC\_AdvActiveHigh* Adv active high.

#### 41.6.25 enum semc\_sync\_mode\_t

Enumerator

*kSEMC\_AsyncMode* Async mode.

*kSEMC\_SyncMode* Sync mode.

**41.6.26 enum semc\_adv\_level\_control\_t**

Enumerator

*kSEMC\_AdvHigh* Adv is high during address hold state.*kSEMC\_AdvLow* Adv is low during address hold state.**41.6.27 enum semc\_rdy\_polarity\_t**

Enumerator

*kSEMC\_RdyActiveLow* Adv active low.*kSEMC\_RdyActivehigh* Adv active low.**41.6.28 enum semc\_ipcmd\_nand\_addrmode\_t**

Enumerator

*kSEMC\_NANDAM\_ColumnRow* Address mode: column and row address(5Byte-CA0/CA1/RA0/-RA1/RA2).*kSEMC\_NANDAM\_ColumnCA0* Address mode: column address only(1 Byte-CA0).*kSEMC\_NANDAM\_ColumnCA0CA1* Address mode: column address only(2 Byte-CA0/CA1).*kSEMC\_NANDAM\_RawRA0* Address mode: row address only(1 Byte-RA0).*kSEMC\_NANDAM\_RawRA0RA1* Address mode: row address only(2 Byte-RA0/RA1).*kSEMC\_NANDAM\_RawRA0RA1RA2* Address mode: row address only(3 Byte-RA0).**41.6.29 enum semc\_ipcmd\_nand\_cmdmode\_t**

Enumerator

*kSEMC\_NANDCM\_Command* command.*kSEMC\_NANDCM\_CommandHold* Command hold.*kSEMC\_NANDCM\_CommandAddress* Command address.*kSEMC\_NANDCM\_CommandAddressHold* Command address hold.*kSEMC\_NANDCM\_CommandAddressRead* Command address read.*kSEMC\_NANDCM\_CommandAddressWrite* Command address write.*kSEMC\_NANDCM\_CommandRead* Command read.*kSEMC\_NANDCM\_CommandWrite* Command write.*kSEMC\_NANDCM\_Read* Read.*kSEMC\_NANDCM\_Write* Write.

**41.6.30 enum semc\_nand\_address\_option\_t**

Enumerator

<i>kSEMC_NandAddrOption_5byte_CA2RA3</i>	CA0+CA1+RA0+RA1+RA2.
<i>kSEMC_NandAddrOption_4byte_CA2RA2</i>	CA0+CA1+RA0+RA1.
<i>kSEMC_NandAddrOption_3byte_CA2RA1</i>	CA0+CA1+RA0.
<i>kSEMC_NandAddrOption_4byte_CA1RA3</i>	CA0+RA0+RA1+RA2.
<i>kSEMC_NandAddrOption_3byte_CA1RA2</i>	CA0+RA0+RA1.
<i>kSEMC_NandAddrOption_2byte_CA1RA1</i>	CA0+RA0.

**41.6.31 enum semc\_ipcmd\_nor\_dbi\_t**

Enumerator

<i>kSEMC_NORDBICM_Read</i>	NOR read.
<i>kSEMC_NORDBICM_Write</i>	NOR write.

**41.6.32 enum semc\_ipcmd\_sram\_t**

Enumerator

<i>kSEMC_SRAMCM_ArrayRead</i>	SRAM memory array read.
<i>kSEMC_SRAMCM_ArrayWrite</i>	SRAM memory array write.
<i>kSEMC_SRAMCM_RegRead</i>	SRAM memory register read.
<i>kSEMC_SRAMCM_RegWrite</i>	SRAM memory register write.

**41.6.33 enum semc\_ipcmd\_sdram\_t**

Enumerator

<i>kSEMC_SDRAMCM_Read</i>	SDRAM memory read.
<i>kSEMC_SDRAMCM_Write</i>	SDRAM memory write.
<i>kSEMC_SDRAMCM_Modeset</i>	SDRAM MODE SET.
<i>kSEMC_SDRAMCM_Active</i>	SDRAM active.
<i>kSEMC_SDRAMCM_AutoRefresh</i>	SDRAM auto-refresh.
<i>kSEMC_SDRAMCM_SelfRefresh</i>	SDRAM self-refresh.
<i>kSEMC_SDRAMCM_Prefetch</i>	SDRAM prefetch.
<i>kSEMC_SDRAMCM_Prefetchall</i>	SDRAM prefetch all.

## 41.7 Function Documentation

### 41.7.1 void SEMC\_GetDefaultConfig ( semc\_config\_t \* *config* )

The purpose of this API is to get the default SEMC configure structure for [SEMC\\_Init\(\)](#). User may use the initialized structure unchanged in [SEMC\\_Init\(\)](#), or modify some fields of the structure before calling [SEMC\\_Init\(\)](#). Example:

```
semc_config_t config;
SEMC_GetDefaultConfig(&config);
```

Parameters

<i>config</i>	The SEMC configuration structure pointer.
---------------	---

### 41.7.2 void SEMC\_Init ( SEMC\_Type \* *base*, semc\_config\_t \* *configure* )

This function ungates the SEMC clock and initializes SEMC. This function must be called before calling any other SEMC driver functions.

Parameters

<i>base</i>	SEMC peripheral base address.
<i>configure</i>	The SEMC configuration structure pointer.

### 41.7.3 void SEMC\_Deinit ( SEMC\_Type \* *base* )

This function gates the SEMC clock. As a result, the SEMC module doesn't work after calling this function, for some IDE, calling this API may cause the next downloading operation failed. so, please call this API cautiously. Additional, users can using "#define FSL\_SDK\_DISABLE\_DRIVER\_CLOCK\_CONTROL (1)" to disable the clock control operation in drivers.

Parameters

<i>base</i>	SEMC peripheral base address.
-------------	-------------------------------

### 41.7.4 status\_t SEMC\_ConfigureSDRAM ( SEMC\_Type \* *base*, semc\_sram\_cs\_t *cs*, semc\_sram\_config\_t \* *config*, uint32\_t *clkSrc\_Hz* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>cs</i>	The chip selection.
<i>config</i>	The sdram configuration.
<i>clkSrc_Hz</i>	The SEMC clock frequency.

#### 41.7.5 status\_t SEMC\_ConfigureNAND ( **SEMC\_Type** \* *base*, **semc\_nand\_config\_t** \* *config*, **uint32\_t** *clkSrc\_Hz* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>config</i>	The nand configuration.
<i>clkSrc_Hz</i>	The SEMC clock frequency.

#### 41.7.6 status\_t SEMC\_ConfigureNOR ( **SEMC\_Type** \* *base*, **semc\_nor\_config\_t** \* *config*, **uint32\_t** *clkSrc\_Hz* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>config</i>	The nor configuration.
<i>clkSrc_Hz</i>	The SEMC clock frequency.

#### 41.7.7 status\_t SEMC\_ConfigureSRAMWithChipSelection ( **SEMC\_Type** \* *base*, **semc\_sram\_cs\_t** *cs*, **semc\_sram\_config\_t** \* *config*, **uint32\_t** *clkSrc\_Hz* )

Parameters

<i>base</i>	SEMC peripheral base address.
-------------	-------------------------------

<i>cs</i>	The chip selection.
<i>config</i>	The sram configuration.
<i>clkSrc_Hz</i>	The SEMC clock frequency.

#### 41.7.8 status\_t SEMC\_ConfigureSRAM ( **SEMC\_Type** \* *base*, **semc\_sram\_config\_t** \* *config*, **uint32\_t** *clkSrc\_Hz* )

**Deprecated** Do not use this function. It has been superceded by [SEMC\\_ConfigureSRAMWithChip-Selection](#).

Parameters

<i>base</i>	SEMC peripheral base address.
<i>config</i>	The sram configuration.
<i>clkSrc_Hz</i>	The SEMC clock frequency.

#### 41.7.9 status\_t SEMC\_ConfigureDBI ( **SEMC\_Type** \* *base*, **semc\_dbi\_config\_t** \* *config*, **uint32\_t** *clkSrc\_Hz* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>config</i>	The dbi configuration.
<i>clkSrc_Hz</i>	The SEMC clock frequency.

#### 41.7.10 static void SEMC\_EnableInterrupts ( **SEMC\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

This function enables the SEMC interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [semc\\_interrupt\\_enable\\_t](#). For example, to enable the IP command done and error interrupt, do the following.

```
*     SEMC_EnableInterrupts(ENET, kSEMC_IPCmdDoneInterrupt |
    kSEMC_IPCmdErrInterrupt);
*
```

Parameters

<i>base</i>	SEMC peripheral base address.
<i>mask</i>	SEMC interrupts to enable. This is a logical OR of the enumeration :: semc_interrupt_enable_t.

#### 41.7.11 static void SEMC\_DisableInterrupts ( SEMC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function disables the SEMC interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [semc\\_interrupt\\_enable\\_t](#). For example, to disable the IP command done and error interrupt, do the following.

```
*     SEMC_DisableInterrupts(ENET,
    kSEMC_IPCmdDoneInterrupt | kSEMC_IPCmdErrInterrupt);
*
```

Parameters

<i>base</i>	SEMC peripheral base address.
<i>mask</i>	SEMC interrupts to disable. This is a logical OR of the enumeration :: semc_interrupt_enable_t.

#### 41.7.12 static bool SEMC\_GetStatusFlag ( SEMC\_Type \* *base* ) [inline], [static]

This function gets the SEMC interrupts event status. User can use the a logical OR of enumeration member as a mask. See [semc\\_interrupt\\_enable\\_t](#).

Parameters

<i>base</i>	SEMC peripheral base address.
-------------	-------------------------------

Returns

status flag, use status flag in [semc\\_interrupt\\_enable\\_t](#) to get the related status.

#### 41.7.13 static void SEMC\_ClearStatusFlags ( SEMC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

The following status register flags can be cleared SEMC interrupt status.

Parameters

<i>base</i>	SEMC base pointer
<i>mask</i>	The status flag mask, a logical OR of enumeration member <a href="#">semc_interrupt_enable_t</a> .

#### 41.7.14 static bool SEMC\_IsIdle ( SEMC\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	SEMC peripheral base address.
-------------	-------------------------------

Returns

True SEMC is in idle, false is not in idle.

#### 41.7.15 status\_t SEMC\_SendIPCommand ( SEMC\_Type \* *base*, semc\_mem\_type\_t *memType*, uint32\_t *address*, uint32\_t *command*, uint32\_t *write*, uint32\_t \* *read* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>memType</i>	SEMC memory type. refer to "semc_mem_type_t"
<i>address</i>	SEMC device address.
<i>command</i>	SEMC IP command. For NAND device, we should use the SEMC_BuildNandIPCommand to get the right nand command. For NOR/DBI device, take refer to "semc_ipcmd_nor_db_t". For SRAM device, take refer to "semc_ipcmd_sram_t". For SDRAM device, take refer to "semc_ipcmd_sdram_t".
<i>write</i>	Data for write access.
<i>read</i>	Data pointer for read data out.

#### 41.7.16 static uint16\_t SEMC\_BuildNandIPCommand ( uint8\_t *userCommand*, semc\_ipcmd\_nand\_addrmode\_t *addrMode*, semc\_ipcmd\_nand\_cmdmode\_t *cmdMode* ) [inline], [static]

This function build SEMC NAND IP command. The command is build of user command code, SEMC address mode and SEMC command mode.

Parameters

<i>userCommand</i>	NAND device normal command.
<i>addrMode</i>	NAND address mode. Refer to "semc_ipcmd_nand_addrmode_t".
<i>cmdMode</i>	NAND command mode. Refer to "semc_ipcmd_nand_cmdmode_t".

#### 41.7.17 static bool SEMC\_IsNandReady ( SEMC\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	SEMC peripheral base address.
-------------	-------------------------------

Returns

True NAND is ready, false NAND is not ready.

#### 41.7.18 status\_t SEMC\_IPCommandNandWrite ( SEMC\_Type \* *base*, uint32\_t *address*, uint8\_t \* *data*, uint32\_t *size\_bytes* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>address</i>	SEMC NAND device address.
<i>data</i>	Data for write access.
<i>size_bytes</i>	Data length.

#### 41.7.19 status\_t SEMC\_IPCommandNandRead ( SEMC\_Type \* *base*, uint32\_t *address*, uint8\_t \* *data*, uint32\_t *size\_bytes* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>address</i>	SEMC NAND device address.
<i>data</i>	Data pointer for data read out.
<i>size_bytes</i>	Data length.

#### 41.7.20 status\_t SEMC\_IPCommandNorWrite ( **SEMC\_Type** \* *base*, **uint32\_t** *address*, **uint8\_t** \* *data*, **uint32\_t** *size\_bytes* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>address</i>	SEMC NOR device address.
<i>data</i>	Data for write access.
<i>size_bytes</i>	Data length.

#### 41.7.21 status\_t SEMC\_IPCommandNorRead ( **SEMC\_Type** \* *base*, **uint32\_t** *address*, **uint8\_t** \* *data*, **uint32\_t** *size\_bytes* )

Parameters

<i>base</i>	SEMC peripheral base address.
<i>address</i>	SEMC NOR device address.
<i>data</i>	Data pointer for data read out.
<i>size_bytes</i>	Data length.

# Chapter 42

## SNVS: Secure Non-Volatile Storage

### 42.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Secure Non-Volatile Storage (SNVS) module.

The SNVS module is designed to safely hold security-related data such as cryptographic key, time counter, monotonic counter, and general purpose security information. The SNVS includes a low power section, namely SNVS\_LP, that is battery backed by the SVNS (or VBAT) power domain. This enables it to keep this data valid and continue to increment the time counter when the power goes down in the rest of the SoC. The always-powered-up part of the module is isolated from the rest of the logic to ensure that it does not get corrupted when the SoC is powered down. The SNVS is designed to comply with Digital Rights Management (DRM) and other security application rules and requirements. This trusted hardware provides features that allow the system software designer to ensure that the data kept by the device is certifiable. Specially, it incorporates a security monitor that checks for various security conditions. If a security violation is indicated then it invalidates access to its sensitive data, and the secret data, for instance, Zeroizable Secret Key, is zeroized. the SNVS can be also configured to bypass its security features and protection mechanism. In this case it can be used by systems that do not require security.

### Modules

- [Secure Non-Volatile Storage High-Power](#)
- [Secure Non-Volatile Storage Low-Power](#)

## 42.2 Secure Non-Volatile Storage High-Power

### 42.2.1 Overview

The MCUXpresso SDK provides a Peripheral driver for the Secure Non-Volatile Storage High-Power(S-NVS-HP) module.

The SNVS\_HP is in the chip's power-supply domain and thus receives the power along with the rest of the chip. The SNVS\_HP provides an interface between the SNVS\_LP and the rest of the system; there is no way to access the SNVS\_LP registers except through the SNVS\_HP. For access to the SNVS\_LP registers, the SNVS\_HP must be powered up. It uses a register access permission policy to determine whether the access to the particular registers is permitted.

## Data Structures

- struct `snvs_hp_rtc_datetime_t`  
*Structure is used to hold the date and time. [More...](#)*
- struct `snvs_hp_rtc_config_t`  
*SNVS config structure. [More...](#)*

## Macros

- #define `SNVS_MAKE_HP_SV_FLAG(x)` (1U << (SNVS\_HPSVR\_SV0\_SHIFT + (x)))  
*Macro to make security violation flag.*

## Enumerations

- enum `snvs_hp_interrupts_t` {
   
`kSNVS_RTC_AlarmInterrupt` = SNVS\_HPCR\_HPTA\_EN\_MASK,  
`kSNVS_RTC_PeriodicInterrupt` = SNVS\_HPCR\_PI\_EN\_MASK }
   
*List of SNVS interrupts.*
- enum `snvs_hp_status_flags_t` {
   
`kSNVS_RTC_AlarmInterruptFlag` = SNVS\_HPSR\_HPTA\_MASK,  
`kSNVS_RTC_PeriodicInterruptFlag` = SNVS\_HPSR\_PI\_MASK,  
`kSNVS_ZMK_ZeroFlag` = (int)SNVS\_HPSR\_ZMK\_ZERO\_MASK,  
`kSNVS_OTPMK_ZeroFlag` = SNVS\_HPSR\_OTPMK\_ZERO\_MASK }
   
*List of SNVS flags.*
- enum `snvs_hp_sv_status_flags_t` {

```

kSNVS_LP_ViolationFlag = SNVS_HPSVSR_SW_LPSV_MASK,
kSNVS_ZMK_EccFailFlag = SNVS_HPSVSR_ZMK_ECC_FAIL_MASK,
kSNVS_LP_SoftwareViolationFlag = SNVS_HPSVSR_SW_LPSV_MASK,
kSNVS_FatalSoftwareViolationFlag = SNVS_HPSVSR_SW_FSV_MASK,
kSNVS_SoftwareViolationFlag = SNVS_HPSVSR_SW_SV_MASK,
kSNVS_Violation0Flag = SNVS_HPSVSR_SV0_MASK,
kSNVS_Violation1Flag = SNVS_HPSVSR_SV1_MASK,
kSNVS_Violation2Flag = SNVS_HPSVSR_SV2_MASK,
kSNVS_Violation4Flag = SNVS_HPSVSR_SV4_MASK,
kSNVS_Violation5Flag = SNVS_HPSVSR_SV5_MASK }

```

*List of SNVS security violation flags.*

- enum `snvs_hp_ssm_state_t` {
   
kSNVS\_SSMInit = 0x00,  
 kSNVS\_SSMHardFail = 0x01,  
 kSNVS\_SSMSoftFail = 0x03,  
 kSNVS\_SSMInitInter = 0x08,  
 kSNVS\_SSMCheck = 0x09,  
 kSNVS\_SSMNonSecure = 0x0B,  
 kSNVS\_SSMTrusted = 0x0D,  
 kSNVS\_SSMSecure = 0x0F }

*List of SNVS Security State Machine State.*

## Functions

- static void `SNVS_HP_EnableMasterKeySelection` (SNVS\_Type \*base, bool enable)  
*Enable or disable master key selection.*
- static void `SNVS_HP_ProgramZeroizableMasterKey` (SNVS\_Type \*base)  
*Trigger to program Zeroizable Master Key.*
- static void `SNVS_HP_ChangeSSMState` (SNVS\_Type \*base)  
*Trigger SSM State Transition.*
- static void `SNVS_HP_SetSoftwareFatalSecurityViolation` (SNVS\_Type \*base)  
*Trigger Software Fatal Security Violation.*
- static void `SNVS_HP_SetSoftwareSecurityViolation` (SNVS\_Type \*base)  
*Trigger Software Security Violation.*
- static `snvs_hp_ssm_state_t` `SNVS_HP_GetSSMState` (SNVS\_Type \*base)  
*Get current SSM State.*
- static void `SNVS_HP_ResetLP` (SNVS\_Type \*base)  
*Reset the SNVS LP section.*
- static uint32\_t `SNVS_HP_GetStatusFlags` (SNVS\_Type \*base)  
*Get the SNVS HP status flags.*
- static void `SNVS_HP_ClearStatusFlags` (SNVS\_Type \*base, uint32\_t mask)  
*Clear the SNVS HP status flags.*
- static uint32\_t `SNVS_HP_GetSecurityViolationStatusFlags` (SNVS\_Type \*base)  
*Get the SNVS HP security violation status flags.*
- static void `SNVS_HP_ClearSecurityViolationStatusFlags` (SNVS\_Type \*base, uint32\_t mask)  
*Clear the SNVS HP security violation status flags.*

## Driver version

- #define **FSL\_SNVS\_HP\_DRIVER\_VERSION** (MAKE\_VERSION(2, 3, 2))  
*Version 2.3.2.*

## Initialization and deinitialization

- void **SNVS\_HP\_Init** (SNVS\_Type \*base)  
*Initialize the SNVS.*
- void **SNVS\_HP\_Deinit** (SNVS\_Type \*base)  
*Deinitialize the SNVS.*
- void **SNVS\_HP\_RTC\_Init** (SNVS\_Type \*base, const **snvs\_hp\_rtc\_config\_t** \*config)  
*Ungates the SNVS clock and configures the peripheral for basic operation.*
- void **SNVS\_HP\_RTC\_Deinit** (SNVS\_Type \*base)  
*Stops the RTC and SRTC timers.*
- void **SNVS\_HP\_RTC\_GetDefaultConfig** (**snvs\_hp\_rtc\_config\_t** \*config)  
*Fills in the SNVS config struct with the default settings.*

## Non secure RTC current Time & Alarm

- **status\_t SNVS\_HP\_RTC\_SetDatetime** (SNVS\_Type \*base, const **snvs\_hp\_rtc\_datetime\_t** \*datetime)  
*Sets the SNVS RTC date and time according to the given time structure.*
- void **SNVS\_HP\_RTC\_GetDatetime** (SNVS\_Type \*base, **snvs\_hp\_rtc\_datetime\_t** \*datetime)  
*Gets the SNVS RTC time and stores it in the given time structure.*
- **status\_t SNVS\_HP\_RTC\_SetAlarm** (SNVS\_Type \*base, const **snvs\_hp\_rtc\_datetime\_t** \*alarmTime)  
*Sets the SNVS RTC alarm time.*
- void **SNVS\_HP\_RTC\_GetAlarm** (SNVS\_Type \*base, **snvs\_hp\_rtc\_datetime\_t** \*datetime)  
*Returns the SNVS RTC alarm time.*
- void **SNVS\_HP\_RTC\_TimeSynchronize** (SNVS\_Type \*base)  
*The function synchronizes RTC counter value with SRTC.*

## Interrupt Interface

- static void **SNVS\_HP\_RTC\_EnableInterrupts** (SNVS\_Type \*base, uint32\_t mask)  
*Enables the selected SNVS interrupts.*
- static void **SNVS\_HP\_RTC\_DisableInterrupts** (SNVS\_Type \*base, uint32\_t mask)  
*Disables the selected SNVS interrupts.*
- uint32\_t **SNVS\_HP\_RTC\_GetEnabledInterrupts** (SNVS\_Type \*base)  
*Gets the enabled SNVS interrupts.*

## Status Interface

- uint32\_t **SNVS\_HP\_RTC\_GetStatusFlags** (SNVS\_Type \*base)

*Gets the SNVS status flags.*

- static void [SNVS\\_HP\\_RTC\\_ClearStatusFlags](#) (SNVS\_Type \*base, uint32\_t mask)  
*Clears the SNVS status flags.*

## Timer Start and Stop

- static void [SNVS\\_HP\\_RTC\\_StartTimer](#) (SNVS\_Type \*base)  
*Starts the SNVS RTC time counter.*
- static void [SNVS\\_HP\\_RTC\\_StopTimer](#) (SNVS\_Type \*base)  
*Stops the SNVS RTC time counter.*

## High Assurance Counter (HAC)

- static void [SNVS\\_HP\\_EnableHighAssuranceCounter](#) (SNVS\_Type \*base, bool enable)  
*Enable or disable the High Assurance Counter (HAC)*
- static void [SNVS\\_HP\\_StartHighAssuranceCounter](#) (SNVS\_Type \*base, bool start)  
*Start or stop the High Assurance Counter (HAC)*
- static void [SNVS\\_HP\\_SetHighAssuranceCounterInitialValue](#) (SNVS\_Type \*base, uint32\_t value)  
*Set the High Assurance Counter (HAC) initialize value.*
- static void [SNVS\\_HP\\_LoadHighAssuranceCounter](#) (SNVS\_Type \*base)  
*Load the High Assurance Counter (HAC)*
- static uint32\_t [SNVS\\_HP\\_GetHighAssuranceCounter](#) (SNVS\_Type \*base)  
*Get the current High Assurance Counter (HAC) value.*
- static void [SNVS\\_HP\\_ClearHighAssuranceCounter](#) (SNVS\_Type \*base)  
*Clear the High Assurance Counter (HAC)*
- static void [SNVS\\_HP\\_LockHighAssuranceCounter](#) (SNVS\_Type \*base)  
*Lock the High Assurance Counter (HAC)*

### 42.2.2 Data Structure Documentation

#### 42.2.2.1 struct snvs\_hp\_rtc\_datetime\_t

##### Data Fields

- uint16\_t [year](#)  
*Range from 1970 to 2099.*
- uint8\_t [month](#)  
*Range from 1 to 12.*
- uint8\_t [day](#)  
*Range from 1 to 31 (depending on month).*
- uint8\_t [hour](#)  
*Range from 0 to 23.*
- uint8\_t [minute](#)  
*Range from 0 to 59.*
- uint8\_t [second](#)  
*Range from 0 to 59.*

## Field Documentation

- (1) `uint16_t snvs_hp_rtc_datetime_t::year`
- (2) `uint8_t snvs_hp_rtc_datetime_t::month`
- (3) `uint8_t snvs_hp_rtc_datetime_t::day`
- (4) `uint8_t snvs_hp_rtc_datetime_t::hour`
- (5) `uint8_t snvs_hp_rtc_datetime_t::minute`
- (6) `uint8_t snvs_hp_rtc_datetime_t::second`

### 42.2.2.2 struct snvs\_hp\_rtc\_config\_t

This structure holds the configuration settings for the SNVS peripheral. To initialize this structure to reasonable defaults, call the SNVS\_GetDefaultConfig() function and pass a pointer to your config structure instance.

The config struct can be made const so it resides in flash

## Data Fields

- bool `rtcCalEnable`  
*true: RTC calibration mechanism is enabled; false: No calibration is used*
- uint32\_t `rtcCalValue`  
*Defines signed calibration value for nonsecure RTC; This is a 5-bit 2's complement value, range from -16 to +15.*
- uint32\_t `periodicInterruptFreq`  
*Defines frequency of the periodic interrupt; Range from 0 to 15.*

### 42.2.3 Macro Definition Documentation

#### 42.2.3.1 #define SNVS\_MAKE\_HP\_SV\_FLAG( x ) (1U << (SNVS\_HPSVSR\_SV0\_SHIFT + (x)))

Macro help to make security violation flag kSNVS\_Violation0Flag to kSNVS\_Violation5Flag, For example, `SNVS_MAKE_HP_SV_FLAG(0)` is kSNVS\_Violation0Flag.

## 42.2.4 Enumeration Type Documentation

### 42.2.4.1 enum snvs\_hp\_interrupts\_t

Enumerator

*kSNVS\_RTC\_AlarmInterrupt* RTC time alarm.

*kSNVS\_RTC\_PeriodicInterrupt* RTC periodic interrupt.

### 42.2.4.2 enum snvs\_hp\_status\_flags\_t

Enumerator

*kSNVS\_RTC\_AlarmInterruptFlag* RTC time alarm flag.

*kSNVS\_RTC\_PeriodicInterruptFlag* RTC periodic interrupt flag.

*kSNVS\_ZMK\_ZeroFlag* The ZMK is zero.

*kSNVS OTPMK\_ZeroFlag* The OTPMK is zero.

### 42.2.4.3 enum snvs\_hp\_sv\_status\_flags\_t

Enumerator

*kSNVS\_LP\_ViolationFlag* Low Power section Security Violation.

*kSNVS\_ZMK\_EccFailFlag* Zeroizable Master Key Error Correcting Code Check Failure.

*kSNVS\_LP\_SoftwareViolationFlag* LP Software Security Violation.

*kSNVS\_FatalSoftwareViolationFlag* Software Fatal Security Violation.

*kSNVS\_SoftwareViolationFlag* Software Security Violation.

*kSNVS\_Violation0Flag* Security Violation 0.

*kSNVS\_Violation1Flag* Security Violation 1.

*kSNVS\_Violation2Flag* Security Violation 2.

*kSNVS\_Violation4Flag* Security Violation 4.

*kSNVS\_Violation5Flag* Security Violation 5.

### 42.2.4.4 enum snvs\_hp\_ssm\_state\_t

Enumerator

*kSNVS\_SSMInit* Init.

*kSNVS\_SSMHardFail* Hard Fail.

*kSNVS\_SSSoftFail* Soft Fail.

*kSNVS\_SSMInitInter* Init Intermediate (transition state between Init and Check)

*kSNVS\_SSMCheck* Check.

*kSNVS\_SSMNonSecure* Non-Secure.

*kSNVS\_SSMTrusted* Trusted.

*kSNVS\_SSMSecure* Secure.

## 42.2.5 Function Documentation

### 42.2.5.1 void SNVS\_HP\_Init ( SNVS\_Type \* *base* )

Note

This API should be called at the beginning of the application using the SNVS driver.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

### 42.2.5.2 void SNVS\_HP\_Deinit ( SNVS\_Type \* *base* )

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

### 42.2.5.3 void SNVS\_HP\_RTC\_Init ( SNVS\_Type \* *base*, const snvs\_hp\_rtc\_config\_t \* *config* )

Note

This API should be called at the beginning of the application using the SNVS driver.

Parameters

<i>base</i>	SNVS peripheral base address
<i>config</i>	Pointer to the user's SNVS configuration structure.

### 42.2.5.4 void SNVS\_HP\_RTC\_Deinit ( SNVS\_Type \* *base* )

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

### 42.2.5.5 void SNVS\_HP\_RTC\_GetDefaultConfig ( snvs\_hp\_rtc\_config\_t \* *config* )

The default values are as follows.

```
*     config->rtccalenable = false;
*     config->rtccalvalue = 0U;
*     config->PIFreq = 0U;
*
```

## Parameters

<i>config</i>	Pointer to the user's SNVS configuration structure.
---------------	---

**42.2.5.6 status\_t SNVS\_HP\_RTC\_SetDatetime ( SNVS\_Type \* *base*, const snvs\_hp\_rtc\_datetime\_t \* *datetime* )**

## Parameters

<i>base</i>	SNVS peripheral base address
<i>datetime</i>	Pointer to the structure where the date and time details are stored.

## Returns

kStatus\_Success: Success in setting the time and starting the SNVS RTC  
kStatus\_InvalidArgument: Error because the datetime format is incorrect

**42.2.5.7 void SNVS\_HP\_RTC\_GetDatetime ( SNVS\_Type \* *base*, snvs\_hp\_rtc\_datetime\_t \* *datetime* )**

## Parameters

<i>base</i>	SNVS peripheral base address
<i>datetime</i>	Pointer to the structure where the date and time details are stored.

**42.2.5.8 status\_t SNVS\_HP\_RTC\_SetAlarm ( SNVS\_Type \* *base*, const snvs\_hp\_rtc\_datetime\_t \* *alarmTime* )**

The function sets the RTC alarm. It also checks whether the specified alarm time is greater than the present time. If not, the function does not set the alarm and returns an error.

Parameters

<i>base</i>	SNVS peripheral base address
<i>alarmTime</i>	Pointer to the structure where the alarm time is stored.

Returns

kStatus\_Success: success in setting the SNVS RTC alarm  
kStatus\_InvalidArgument: Error because the alarm datetime format is incorrect  
kStatus\_Fail: Error because the alarm time has already passed

#### 42.2.5.9 void SNVS\_HP\_RTC\_GetAlarm ( SNVS\_Type \* *base*, snvs\_hp\_RTC\_datetime\_t \* *datetime* )

Parameters

<i>base</i>	SNVS peripheral base address
<i>datetime</i>	Pointer to the structure where the alarm date and time details are stored.

#### 42.2.5.10 void SNVS\_HP\_RTC\_TimeSynchronize ( SNVS\_Type \* *base* )

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.2.5.11 static void SNVS\_HP\_RTC\_EnableInterrupts ( SNVS\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration :: _snvs_hp_interrupts_t

#### 42.2.5.12 static void SNVS\_HP\_RTC\_DisableInterrupts ( SNVS\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	The interrupts to disable. This is a logical OR of members of the enumeration :: _snvs_hp_interrupts_t

#### 42.2.5.13 `uint32_t SNVS_HP_RTC_GetEnabledInterrupts ( SNVS_Type * base )`

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration :: \_snvs\_hp\_interrupts\_t

#### 42.2.5.14 `uint32_t SNVS_HP_RTC_GetStatusFlags ( SNVS_Type * base )`

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

The status flags. This is the logical OR of members of the enumeration :: \_snvs\_hp\_status\_flags\_t

#### 42.2.5.15 `static void SNVS_HP_RTC_ClearStatusFlags ( SNVS_Type * base, uint32_t mask ) [inline], [static]`

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	The status flags to clear. This is a logical OR of members of the enumeration :: _snvs_hp_status_flags_t

#### 42.2.5.16 `static void SNVS_HP_RTC_StartTimer ( SNVS_Type * base ) [inline], [static]`

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.2.5.17 static void SNVS\_HP\_RTC\_StopTimer ( SNVS\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.2.5.18 static void SNVS\_HP\_EnableMasterKeySelection ( SNVS\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>enable</i>	Pass true to enable, false to disable.

**42.2.5.19 static void SNVS\_HP\_ProgramZeroizableMasterKey ( SNVS\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.2.5.20 static void SNVS\_HP\_ChangeSSMState ( SNVS\_Type \* *base* ) [inline], [static]**

Trigger state transition of the system security monitor (SSM). It results only the following transitions of the SSM:

- Check State -> Non-Secure (when Non-Secure Boot and not in Fab Configuration)
- Check State -> Trusted (when Secure Boot or in Fab Configuration )
- Trusted State -> Secure
- Secure State -> Trusted
- Soft Fail -> Non-Secure

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.2.5.21 static void SNVS\_HP\_SetSoftwareFatalSecurityViolation ( SNVS\_Type \* *base* ) [inline], [static]

The result SSM state transition is:

- Check State -> Soft Fail
- Non-Secure State -> Soft Fail
- Trusted State -> Soft Fail
- Secure State -> Soft Fail

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.2.5.22 static void SNVS\_HP\_SetSoftwareSecurityViolation ( SNVS\_Type \* *base* ) [inline], [static]

The result SSM state transition is:

- Check -> Non-Secure
- Trusted -> Soft Fail
- Secure -> Soft Fail

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.2.5.23 static snvs\_hp\_ssm\_state\_t SNVS\_HP\_GetSSMState ( SNVS\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

Current SSM state

**42.2.5.24 static void SNVS\_HP\_ResetLP ( SNVS\_Type \* *base* ) [inline], [static]**

Reset the LP section except SRTC and Time alarm.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.2.5.25 static void SNVS\_HP\_EnableHighAssuranceCounter ( SNVS\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>enable</i>	Pass true to enable, false to disable.

**42.2.5.26 static void SNVS\_HP\_StartHighAssuranceCounter ( SNVS\_Type \* *base*, bool *start* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>start</i>	Pass true to start, false to stop.

**42.2.5.27 static void SNVS\_HP\_SetHighAssuranceCounterInitialValue ( SNVS\_Type \* *base*, uint32\_t *value* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>value</i>	The initial value to set.

**42.2.5.28 static void SNVS\_HP\_LoadHighAssuranceCounter ( SNVS\_Type \* *base* ) [inline], [static]**

This function loads the HAC initialize value to counter register.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.2.5.29 static uint32\_t SNVS\_HP\_GetHighAssuranceCounter ( SNVS\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

HAC currnet value.

**42.2.5.30 static void SNVS\_HP\_ClearHighAssuranceCounter ( SNVS\_Type \* *base* ) [inline], [static]**

This function can be called in a functional or soft fail state. When the HAC is enabled:

- If the HAC is cleared in the soft fail state, the SSM transitions to the hard fail state immediately;
- If the HAC is cleared in functional state, the SSM will transition to hard fail immediately after transitioning to soft fail.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.2.5.31 static void SNVS\_HP\_LockHighAssuranceCounter ( SNVS\_Type \* *base* ) [inline], [static]**

Once locked, the HAC initialize value could not be changed, the HAC enable status could not be changed. This could only be unlocked by system reset.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.2.5.32 static uint32\_t SNVS\_HP\_GetStatusFlags ( SNVS\_Type \* *base* ) [inline], [static]**

The flags are returned as the OR'ed value f the enumeration :: \_snvs\_hp\_status\_flags\_t.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

The OR'ed value of status flags.

#### 42.2.5.33 static void SNVS\_HP\_ClearStatusFlags ( **SNVS\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

The flags to clear are passed in as the OR'ed value of the enumeration :: \_snvs\_hp\_status\_flags\_t. Only these flags could be cleared using this API.

- [kSNVS\\_RTC\\_PeriodicInterruptFlag](#)
- [kSNVS\\_RTC\\_AlarmInterruptFlag](#)

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	OR'ed value of the flags to clear.

#### 42.2.5.34 static **uint32\_t** SNVS\_HP\_GetSecurityViolationStatusFlags ( **SNVS\_Type** \* *base* ) [inline], [static]

The flags are returned as the OR'ed value of the enumeration :: \_snvs\_hp\_sv\_status\_flags\_t.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

The OR'ed value of security violation status flags.

#### 42.2.5.35 static void SNVS\_HP\_ClearSecurityViolationStatusFlags ( **SNVS\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

The flags to clear are passed in as the OR'ed value of the enumeration :: \_snvs\_hp\_sv\_status\_flags\_t. Only these flags could be cleared using this API.

- [kSNVS\\_ZMK\\_EccFailFlag](#)
- [kSNVS\\_Violation0Flag](#)

- [kSNVS\\_Violation1Flag](#)
- [kSNVS\\_Violation2Flag](#)
- [kSNVS\\_Violation3Flag](#)
- [kSNVS\\_Violation4Flag](#)
- [kSNVS\\_Violation5Flag](#)

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	OR'ed value of the flags to clear.

## 42.3 Secure Non-Volatile Storage Low-Power

### 42.3.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Secure Non-Volatile Storage Low-Power (S-NVS-LP) module.

The SNVS\_LP is a data storage subsystem. Its purpose is to store and protect system data, regardless of the main system power state. The SNVS\_LP is in the always-powered-up domain, which is a separate power domain with its own power supply.

## Data Structures

- struct `snvs_lp_passive_tamper_t`  
*Structure is used to configure SNVS LP passive tamper pins. [More...](#)*
- struct `snvs_lp_srtc_datetime_t`  
*Structure is used to hold the date and time. [More...](#)*
- struct `snvs_lp_srtc_config_t`  
*SNVS\_LP config structure. [More...](#)*

## Macros

- #define `SNVS_ZMK_REG_COUNT` 8U /\* 8 Zeroizable Master Key registers. \*/  
*Define of SNVS\_LP Zeroizable Master Key registers.*
- #define `SNVS_LP_MAX_TAMPER` kSNVS\_ExternalTamper1  
*Define of SNVS\_LP Max possible tamper.*

## Enumerations

- enum `snvs_lp_srtc_interrupts_t` { `kSNVS_SRTC_AlarmInterrupt` = SNVS\_LPCR\_LPTA\_EN\_M-ASK }  
*List of SNVS\_LP interrupts.*
- enum `snvs_lp_srtc_status_flags_t` { `kSNVS_SRTC_AlarmInterruptFlag` = SNVS\_LPSR\_LPTA-MASK }  
*List of SNVS\_LP flags.*
- enum `snvs_lp_external_tamper_status_t`  
*List of SNVS\_LP external tampers status.*
- enum `snvs_lp_external_tamper_polarity_t`  
*SNVS\_LP external tamper polarity.*
- enum `snvs_lp_zmk_program_mode_t` {  
`kSNVS_ZMKSoftwareProgram`,  
`kSNVS_ZMKHardwareProgram` }  
*SNVS\_LP Zeroizable Master Key programming mode.*
- enum `snvs_lp_master_key_mode_t` {  
`kSNVS OTPMK` = 0,  
`kSNVS_ZMK` = 2,

```
kSNVS_CMK = 3 }

SNVS_LP Master Key mode.
```

## Functions

- void **SNVS\_LP\_SRTC\_Init** (SNVS\_Type \*base, const **snvs\_lp\_srtc\_config\_t** \*config)  
*Ungates the SNVS clock and configures the peripheral for basic operation.*
- void **SNVS\_LP\_SRTC\_Deinit** (SNVS\_Type \*base)  
*Stops the SRTC timer.*
- void **SNVS\_LP\_SRTC\_GetDefaultConfig** (**snvs\_lp\_srtc\_config\_t** \*config)  
*Fills in the SNVS\_LP config struct with the default settings.*

## Driver version

- #define **FSL\_SNVS\_LP\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 4, 5))  
*Version 2.4.5.*

## Initialization and deinitialization

- void **SNVS\_LP\_Init** (SNVS\_Type \*base)  
*Ungates the SNVS clock and configures the peripheral for basic operation.*
- void **SNVS\_LP\_Deinit** (SNVS\_Type \*base)  
*Deinit the SNVS LP section.*

## Secure RTC (SRTC) current Time & Alarm

- **status\_t SNVS\_LP\_SRTC\_SetDatetime** (SNVS\_Type \*base, const **snvs\_lp\_srtc\_datetime\_t** \*datetime)  
*Sets the SNVS SRTC date and time according to the given time structure.*
- void **SNVS\_LP\_SRTC\_GetDatetime** (SNVS\_Type \*base, **snvs\_lp\_srtc\_datetime\_t** \*datetime)  
*Gets the SNVS SRTC time and stores it in the given time structure.*
- **status\_t SNVS\_LP\_SRTC\_SetAlarm** (SNVS\_Type \*base, const **snvs\_lp\_srtc\_datetime\_t** \*alarmTime)  
*Sets the SNVS SRTC alarm time.*
- void **SNVS\_LP\_SRTC\_GetAlarm** (SNVS\_Type \*base, **snvs\_lp\_srtc\_datetime\_t** \*datetime)  
*Returns the SNVS SRTC alarm time.*

## Interrupt Interface

- static void **SNVS\_LP\_SRTC\_EnableInterrupts** (SNVS\_Type \*base, uint32\_t mask)  
*Enables the selected SNVS interrupts.*
- static void **SNVS\_LP\_SRTC\_DisableInterrupts** (SNVS\_Type \*base, uint32\_t mask)  
*Disables the selected SNVS interrupts.*
- uint32\_t **SNVS\_LP\_SRTC\_GetEnabledInterrupts** (SNVS\_Type \*base)

*Gets the enabled SNVS interrupts.*

## Status Interface

- `uint32_t SNVS_LP_SRTC_GetStatusFlags (SNVS_Type *base)`  
*Gets the SNVS status flags.*
- `static void SNVS_LP_SRTC_ClearStatusFlags (SNVS_Type *base, uint32_t mask)`  
*Clears the SNVS status flags.*

## Timer Start and Stop

- `static void SNVS_LP_SRTC_StartTimer (SNVS_Type *base)`  
*Starts the SNVS SRTC time counter.*
- `static void SNVS_LP_SRTC_StopTimer (SNVS_Type *base)`  
*Stops the SNVS SRTC time counter.*

## External tampering

- `void SNVS_LP_PassiveTamperPin_GetDefaultConfig (snvs_lp_passive_tamper_t *config)`  
*Fills in the SNVS tamper pin config struct with the default settings.*

## Monotonic Counter (MC)

- `static void SNVS_LP_EnableMonotonicCounter (SNVS_Type *base, bool enable)`  
*Enable or disable the Monotonic Counter.*
- `uint64_t SNVS_LP_GetMonotonicCounter (SNVS_Type *base)`  
*Get the current Monotonic Counter.*
- `static void SNVS_LP_IncreaseMonotonicCounter (SNVS_Type *base)`  
*Increase the Monotonic Counter.*

## Zeroizable Master Key (ZMK)

- `void SNVS_LP_WriteZeroizableMasterKey (SNVS_Type *base, uint32_t ZMKey[SNVS_ZMK_REG_COUNT])`  
*Write Zeroizable Master Key (ZMK) to the SNVS registers.*
- `static void SNVS_LP_SetZeroizableMasterKeyValid (SNVS_Type *base, bool valid)`  
*Set Zeroizable Master Key valid.*
- `static bool SNVS_LP_GetZeroizableMasterKeyValid (SNVS_Type *base)`  
*Get Zeroizable Master Key valid status.*
- `static void SNVS_LP_SetZeroizableMasterKeyProgramMode (SNVS_Type *base, snvs_lp_zmk_program_mode_t mode)`  
*Set Zeroizable Master Key programming mode.*
- `static void SNVS_LP_EnableZeroizableMasterKeyECC (SNVS_Type *base, bool enable)`  
*Enable or disable Zeroizable Master Key ECC.*

- static void `SNVS_LP_SetMasterKeyMode` (SNVS\_Type \*base, `snvs_lp_master_key_mode_t mode`)  
*Set SNVS Master Key mode.*

## 42.3.2 Data Structure Documentation

### 42.3.2.1 `struct snvs_lp_passive_tamper_t`

### 42.3.2.2 `struct snvs_lp_srtc_datetime_t`

#### Data Fields

- `uint16_t year`  
*Range from 1970 to 2099.*
- `uint8_t month`  
*Range from 1 to 12.*
- `uint8_t day`  
*Range from 1 to 31 (depending on month).*
- `uint8_t hour`  
*Range from 0 to 23.*
- `uint8_t minute`  
*Range from 0 to 59.*
- `uint8_t second`  
*Range from 0 to 59.*

#### Field Documentation

- (1) `uint16_t snvs_lp_srtc_datetime_t::year`
- (2) `uint8_t snvs_lp_srtc_datetime_t::month`
- (3) `uint8_t snvs_lp_srtc_datetime_t::day`
- (4) `uint8_t snvs_lp_srtc_datetime_t::hour`
- (5) `uint8_t snvs_lp_srtc_datetime_t::minute`
- (6) `uint8_t snvs_lp_srtc_datetime_t::second`

### 42.3.2.3 `struct snvs_lp_srtc_config_t`

This structure holds the configuration settings for the SNVS\_LP peripheral. To initialize this structure to reasonable defaults, call the `SNVS_LP_GetDefaultConfig()` function and pass a pointer to your config structure instance.

The config struct can be made const so it resides in flash

## Data Fields

- bool `srtcCalEnable`  
*true: SRTC calibration mechanism is enabled; false: No calibration is used*
- uint32\_t `srtcCalValue`  
*Defines signed calibration value for SRTC; This is a 5-bit 2's complement value, range from -16 to +15.*

### 42.3.3 Enumeration Type Documentation

#### 42.3.3.1 enum snvs\_lp\_srtc\_interrupts\_t

Enumerator

***kSNVS\_SRTC\_AlarmInterrupt*** SRTC time alarm.

#### 42.3.3.2 enum snvs\_lp\_srtc\_status\_flags\_t

Enumerator

***kSNVS\_SRTC\_AlarmInterruptFlag*** SRTC time alarm flag.

#### 42.3.3.3 enum snvs\_lp\_zmk\_program\_mode\_t

Enumerator

***kSNVS\_ZMKSoftwareProgram*** Software programming mode.

***kSNVS\_ZMKHardwareProgram*** Hardware programming mode.

#### 42.3.3.4 enum snvs\_lp\_master\_key\_mode\_t

Enumerator

***kSNVS\_OTPMK*** One Time Programmable Master Key.

***kSNVS\_ZMK*** Zeroizable Master Key.

***kSNVS\_CMK*** Combined Master Key, it is XOR of OTPMK and ZMK.

### 42.3.4 Function Documentation

#### 42.3.4.1 void SNVS\_LP\_Init( SNVS\_Type \* *base* )

Note

This API should be called at the beginning of the application using the SNVS driver.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.3.4.2 void SNVS\_LP\_Deinit ( SNVS\_Type \* *base* )

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.3.4.3 void SNVS\_LP\_SRTC\_Init ( SNVS\_Type \* *base*, const snvs\_lp\_srtc\_config\_t \* *config* )

Note

This API should be called at the beginning of the application using the SNVS driver.

Parameters

<i>base</i>	SNVS peripheral base address
<i>config</i>	Pointer to the user's SNVS configuration structure.

#### 42.3.4.4 void SNVS\_LP\_SRTC\_Deinit ( SNVS\_Type \* *base* )

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.3.4.5 void SNVS\_LP\_SRTC\_GetDefaultConfig ( snvs\_lp\_srtc\_config\_t \* *config* )

The default values are as follows.

```
*     config->srtccalenable = false;
*     config->srtccalvalue = 0U;
*
```

Parameters

<i>config</i>	Pointer to the user's SNVS configuration structure.
---------------	---

#### 42.3.4.6 **status\_t SNVS\_LP\_SRTC\_SetDatetime ( SNVS\_Type \* *base*, const snvs\_lp\_srtc\_datetime\_t \* *datetime* )**

Parameters

<i>base</i>	SNVS peripheral base address
<i>datetime</i>	Pointer to the structure where the date and time details are stored.

Returns

kStatus\_Success: Success in setting the time and starting the SNVS SRTC  
kStatus\_InvalidArgument: Error because the datetime format is incorrect

#### 42.3.4.7 **void SNVS\_LP\_SRTC\_GetDatetime ( SNVS\_Type \* *base*, snvs\_lp\_srtc\_datetime\_t \* *datetime* )**

Parameters

<i>base</i>	SNVS peripheral base address
<i>datetime</i>	Pointer to the structure where the date and time details are stored.

#### 42.3.4.8 **status\_t SNVS\_LP\_SRTC\_SetAlarm ( SNVS\_Type \* *base*, const snvs\_lp\_srtc\_datetime\_t \* *alarmTime* )**

The function sets the SRTC alarm. It also checks whether the specified alarm time is greater than the present time. If not, the function does not set the alarm and returns an error. Please note, that SRTC alarm has limited resolution because only 32 most significant bits of SRTC counter are compared to SRTC Alarm register. If the alarm time is beyond SRTC resolution, the function does not set the alarm and returns an error.

Parameters

<i>base</i>	SNVS peripheral base address
<i>alarmTime</i>	Pointer to the structure where the alarm time is stored.

Returns

kStatus\_Success: success in setting the SNVS SRTC alarm  
kStatus\_InvalidArgument: Error because the alarm datetime format is incorrect  
kStatus\_Fail: Error because the alarm time has already passed or is beyond resolution

#### 42.3.4.9 void SNVS\_LP\_SRTC\_GetAlarm ( SNVS\_Type \* *base*, snvs\_lp\_srtc\_datetime\_t \* *datetime* )

Parameters

<i>base</i>	SNVS peripheral base address
<i>datetime</i>	Pointer to the structure where the alarm date and time details are stored.

#### 42.3.4.10 static void SNVS\_LP\_SRTC\_EnableInterrupts ( SNVS\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration :: _-snvs_lp_srtc_interrupts

#### 42.3.4.11 static void SNVS\_LP\_SRTC\_DisableInterrupts ( SNVS\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration :: _-snvs_lp_srtc_interrupts

#### 42.3.4.12 uint32\_t SNVS\_LP\_SRTC\_GetEnabledInterrupts ( SNVS\_Type \* *base* )

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration :: \_snvs\_lp\_srtc\_-interrupts

#### 42.3.4.13 **uint32\_t SNVS\_LP\_SRTC\_GetStatusFlags ( SNVS\_Type \* *base* )**

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

The status flags. This is the logical OR of members of the enumeration :: \_snvs\_lp\_srtc\_status\_flags

#### 42.3.4.14 **static void SNVS\_LP\_SRTC\_ClearStatusFlags ( SNVS\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>mask</i>	The status flags to clear. This is a logical OR of members of the enumeration :: _-snvs_lp_srtc_status_flags

#### 42.3.4.15 **static void SNVS\_LP\_SRTC\_StartTimer ( SNVS\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.3.4.16 **static void SNVS\_LP\_SRTC\_StopTimer ( SNVS\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

#### 42.3.4.17 void SNVS\_LP\_PassiveTamperPin\_GetDefaultConfig ( **snvs\_lp\_passive\_tamper\_t** \* *config* )

The default values are as follows. code config->polarity = 0U; config->filterenable = 0U; if available on SoC config->filter = 0U; if available on SoC endcode

Parameters

<i>config</i>	Pointer to the user's SNVS configuration structure.
---------------	---

#### 42.3.4.18 static void SNVS\_LP\_EnableMonotonicCounter ( **SNVS\_Type** \* *base*, **bool enable** ) [inline], [static]

Parameters

<i>base</i>	SNVS peripheral base address
<i>enable</i>	Pass true to enable, false to disable.

#### 42.3.4.19 uint64\_t SNVS\_LP\_GetMonotonicCounter ( **SNVS\_Type** \* *base* )

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

Current Monotonic Counter value.

#### 42.3.4.20 static void SNVS\_LP\_IncreaseMonotonicCounter ( **SNVS\_Type** \* *base* ) [inline], [static]

Increase the Monotonic Counter by 1.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

**42.3.4.21 void SNVS\_LP\_WriteZeroizableMasterKey ( SNVS\_Type \* *base*, uint32\_t *ZMKey*[SNVS\_ZMK\_REG\_COUNT] )**

Parameters

<i>base</i>	SNVS peripheral base address
<i>ZMKey</i>	The ZMK write to the SNVS register.

**42.3.4.22 static void SNVS\_LP\_SetZeroizableMasterKeyValid ( SNVS\_Type \* *base*, bool *valid* ) [inline], [static]**

This API could only be called when using software programming mode. After writing ZMK using [SNVS\\_LP\\_WriteZeroizableMasterKey](#), call this API to make the ZMK valid.

Parameters

<i>base</i>	SNVS peripheral base address
<i>valid</i>	Pass true to set valid, false to set invalid.

**42.3.4.23 static bool SNVS\_LP\_GetZeroizableMasterKeyValid ( SNVS\_Type \* *base* ) [inline], [static]**

In hardware programming mode, call this API to check whether the ZMK is valid.

Parameters

<i>base</i>	SNVS peripheral base address
-------------	------------------------------

Returns

true if valid, false if invalid.

**42.3.4.24 static void SNVS\_LP\_SetZeroizableMasterKeyProgramMode ( SNVS\_Type \* *base*, snvs\_lp\_zmk\_program\_mode\_t *mode* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>mode</i>	ZMK programming mode.

**42.3.4.25 static void SNVS\_LP\_EnableZeroizableMasterKeyECC ( SNVS\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>enable</i>	Pass true to enable, false to disable.

**42.3.4.26 static void SNVS\_LP\_SetMasterKeyMode ( SNVS\_Type \* *base*, snvs\_lp\_master\_key\_mode\_t *mode* ) [inline], [static]**

Parameters

<i>base</i>	SNVS peripheral base address
<i>mode</i>	Master Key mode.

Note

When [kSNVS\\_ZMK](#) or [kSNVS\\_CMK](#) used, the SNVS\_HP must be configured to enable the master key selection.

# Chapter 43

## SPDIF: Sony/Philips Digital Interface

### 43.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Sony/Philips Digital Interface (SPDIF) module of MCUXpresso SDK devices.

SPDIF driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for SPDIF initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the SPDIF peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. SPDIF functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `spdif_handle_t` as the first parameter. Initialize the handle by calling the [SPDIF\\_TransferTxCreateHandle\(\)](#) or [SPDIF\\_TransferRxCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [SPDIF\\_TransferSendNonBlocking\(\)](#) and [SPDIF\\_TransferReceiveNonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_SPDIF_TxIdle` and `kStatus_SPDIF_RxIdle` status.

### 43.2 Typical use case

#### 43.2.1 SPDIF Send/receive using an interrupt method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/spdif

#### 43.2.2 SPDIF Send/receive using a DMA method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/spdif

### Modules

- [SPDIF eDMA Driver](#)

### Data Structures

- struct [spdif\\_config\\_t](#)

- *SPDIF user configuration structure. More...*
- struct `spdif_transfer_t`  
*SPDIF transfer structure. More...*
- struct `spdif_handle_t`  
*SPDIF handle structure. More...*

## Macros

- `#define SPDIF_XFER_QUEUE_SIZE (4U)`  
*SPDIF transfer queue size, user can refine it according to use case.*

## Typedefs

- `typedef void(* spdif_transfer_callback_t )(SPDIF_Type *base, spdif_handle_t *handle, status_t status, void *userData)`  
*SPDIF transfer callback prototype.*

## Enumerations

- enum {
   
`kStatus_SPDIF_RxDPLLLocked` = MAKE\_STATUS(kStatusGroup\_SPDIF, 0),
   
`kStatus_SPDIF_TxFIFOError` = MAKE\_STATUS(kStatusGroup\_SPDIF, 1),
   
`kStatus_SPDIF_TxFIFOResync` = MAKE\_STATUS(kStatusGroup\_SPDIF, 2),
   
`kStatus_SPDIF_RxCnew` = MAKE\_STATUS(kStatusGroup\_SPDIF, 3),
   
`kStatus_SPDIF_ValidateNoGood` = MAKE\_STATUS(kStatusGroup\_SPDIF, 4),
   
`kStatus_SPDIF_RxIllegalSymbol` = MAKE\_STATUS(kStatusGroup\_SPDIF, 5),
   
`kStatus_SPDIF_RxParityBitError` = MAKE\_STATUS(kStatusGroup\_SPDIF, 6),
   
`kStatus_SPDIF_UChannelOverrun` = MAKE\_STATUS(kStatusGroup\_SPDIF, 7),
   
`kStatus_SPDIF_QChannelOverrun` = MAKE\_STATUS(kStatusGroup\_SPDIF, 8),
   
`kStatus_SPDIF_UQChannelSync` = MAKE\_STATUS(kStatusGroup\_SPDIF, 9),
   
`kStatus_SPDIF_UQChannelFrameError` = MAKE\_STATUS(kStatusGroup\_SPDIF, 10),
   
`kStatus_SPDIF_RxFIFOError` = MAKE\_STATUS(kStatusGroup\_SPDIF, 11),
   
`kStatus_SPDIF_RxFIFOResync` = MAKE\_STATUS(kStatusGroup\_SPDIF, 12),
   
`kStatus_SPDIF_LockLoss` = MAKE\_STATUS(kStatusGroup\_SPDIF, 13),
   
`kStatus_SPDIF_TxIdle` = MAKE\_STATUS(kStatusGroup\_SPDIF, 14),
   
`kStatus_SPDIF_RxIdle` = MAKE\_STATUS(kStatusGroup\_SPDIF, 15),
   
`kStatus_SPDIF_QueueFull` = MAKE\_STATUS(kStatusGroup\_SPDIF, 16) }
   
*SPDIF return status.*

- enum `spdif_rxfull_select_t` {
   
`kSPDIF_RxFull1Sample` = 0x0u,
   
`kSPDIF_RxFull4Samples`,
   
`kSPDIF_RxFull8Samples`,
   
`kSPDIF_RxFull16Samples` }
   
*SPDIF Rx FIFO full flag select, it decides when assert the rx full flag.*
- enum `spdif_txempty_select_t` {
   
`kSPDIF_TxEmpty0Sample` = 0x0u,
   
`kSPDIF_TxEmpty4Samples`,
   
`kSPDIF_TxEmpty8Samples`,

- `kSPDIF_TxEmpty12Samples }`

*SPDIF tx FIFO EMPTY flag select, it decides when assert the tx empty flag.*
- enum `spdif_uchannel_source_t` {
 `kSPDIF_NoUChannel` = 0x0U,
 `kSPDIF_UChannelFromRx` = 0x1U,
 `kSPDIF_UChannelFromTx` = 0x3U }
 

*SPDIF U channel source.*
- enum `spdif_gain_select_t` {
 `kSPDIF_GAIN_24` = 0x0U,
 `kSPDIF_GAIN_16`,
 `kSPDIF_GAIN_12`,
 `kSPDIF_GAIN_8`,
 `kSPDIF_GAIN_6`,
 `kSPDIF_GAIN_4`,
 `kSPDIF_GAIN_3` }
 

*SPDIF clock gain.*
- enum `spdif_tx_source_t` {
 `kSPDIF_txFromReceiver` = 0x1U,
 `kSPDIF_txNormal` = 0x5U }
 

*SPDIF tx data source.*
- enum `spdif_validity_config_t` {
 `kSPDIF_validityFlagAlwaysSet` = 0x0U,
 `kSPDIF_validityFlagAlwaysClear` }
 

*SPDIF tx data source.*
- enum {
 `kSPDIF_RxDPLLocked` = SPDIF\_SIE\_LOCK\_MASK,
 `kSPDIF_TxFIFOError` = SPDIF\_SIE\_TXUNOV\_MASK,
 `kSPDIF_TxFIFOResync` = SPDIF\_SIE\_TXRESYN\_MASK,
 `kSPDIF_RxControlChannelChange` = SPDIF\_SIE\_CNEW\_MASK,
 `kSPDIF_ValidityFlagNoGood` = SPDIF\_SIE\_VALNOGOOD\_MASK,
 `kSPDIF_RxIllegalSymbol` = SPDIF\_SIE\_SYMERR\_MASK,
 `kSPDIF_RxParityBitError` = SPDIF\_SIE\_BITERR\_MASK,
 `kSPDIF_UChannelReceiveRegisterFull` = SPDIF\_SIE\_URXFUL\_MASK,
 `kSPDIF_UChannelReceiveRegisterOverrun` = SPDIF\_SIE\_URXOV\_MASK,
 `kSPDIF_QChannelReceiveRegisterFull` = SPDIF\_SIE\_QRXFUL\_MASK,
 `kSPDIF_QChannelReceiveRegisterOverrun` = SPDIF\_SIE\_QRXOV\_MASK,
 `kSPDIF_UQChannelSync` = SPDIF\_SIE\_UQSYNC\_MASK,
 `kSPDIF_UQChannelFrameError` = SPDIF\_SIE\_UQERR\_MASK,
 `kSPDIF_RxFIFOError` = SPDIF\_SIE\_RXFIFOUnOV\_MASK,
 `kSPDIF_RxFIFOResync` = SPDIF\_SIE\_RXFIFOResYN\_MASK,
 `kSPDIF_LockLoss` = SPDIF\_SIE\_LOCKLOSS\_MASK,
 `kSPDIF_TxFIFOEmpty` = SPDIF\_SIE\_TXEM\_MASK,
 `kSPDIF_RxFIFOFull` = SPDIF\_SIE\_RXFIFOFUL\_MASK,
 `kSPDIF_AllInterrupt` }
 

*The SPDIF interrupt enable flag.*
- enum {

```
kSPDIF_RxDMAEnable = SPDIF_SCR_DMA_RX_EN_MASK,
kSPDIF_TxDMAEnable = SPDIF_SCR_DMA_TX_EN_MASK }
```

*The DMA request sources.*

## Driver version

- #define **FSL\_SPDIF\_DRIVER\_VERSION** (MAKE\_VERSION(2, 0, 6))  
*Version 2.0.6.*

## Initialization and deinitialization

- void **SPDIF\_Init** (SPDIF\_Type \*base, const **spdif\_config\_t** \*config)  
*Initializes the SPDIF peripheral.*
- void **SPDIF\_GetDefaultConfig** (**spdif\_config\_t** \*config)  
*Sets the SPDIF configuration structure to default values.*
- void **SPDIF\_Deinit** (SPDIF\_Type \*base)  
*De-initializes the SPDIF peripheral.*
- uint32\_t **SPDIFGetInstance** (SPDIF\_Type \*base)  
*Get the instance number for SPDIF.*
- static void **SPDIF\_TxFIFOReset** (SPDIF\_Type \*base)  
*Resets the SPDIF Tx.*
- static void **SPDIF\_RxFIFOReset** (SPDIF\_Type \*base)  
*Resets the SPDIF Rx.*
- void **SPDIF\_TxEnable** (SPDIF\_Type \*base, bool enable)  
*Enables/disables the SPDIF Tx.*
- static void **SPDIF\_RxEnable** (SPDIF\_Type \*base, bool enable)  
*Enables/disables the SPDIF Rx.*

## Status

- static uint32\_t **SPDIF\_GetStatusFlag** (SPDIF\_Type \*base)  
*Gets the SPDIF status flag state.*
- static void **SPDIF\_ClearStatusFlags** (SPDIF\_Type \*base, uint32\_t mask)  
*Clears the SPDIF status flag state.*

## Interrupts

- static void **SPDIF\_EnableInterrupts** (SPDIF\_Type \*base, uint32\_t mask)  
*Enables the SPDIF Tx interrupt requests.*
- static void **SPDIF\_DisableInterrupts** (SPDIF\_Type \*base, uint32\_t mask)  
*Disables the SPDIF Tx interrupt requests.*

## DMA Control

- static void **SPDIF\_EnableDMA** (SPDIF\_Type \*base, uint32\_t mask, bool enable)  
*Enables/disables the SPDIF DMA requests.*
- static uint32\_t **SPDIF\_TxGetLeftDataRegisterAddress** (SPDIF\_Type \*base)  
*Gets the SPDIF Tx left data register address.*
- static uint32\_t **SPDIF\_TxGetRightDataRegisterAddress** (SPDIF\_Type \*base)  
*Gets the SPDIF Tx right data register address.*

- static uint32\_t **SPDIF\_RxGetLeftDataRegisterAddress** (SPDIF\_Type \*base)  
*Gets the SPDIF Rx left data register address.*
- static uint32\_t **SPDIF\_RxGetRightDataRegisterAddress** (SPDIF\_Type \*base)  
*Gets the SPDIF Rx right data register address.*

## Bus Operations

- void **SPDIF\_TxSetSampleRate** (SPDIF\_Type \*base, uint32\_t sampleRate\_Hz, uint32\_t sourceClockFreq\_Hz)  
*Configures the SPDIF Tx sample rate.*
- uint32\_t **SPDIF\_GetRxSampleRate** (SPDIF\_Type \*base, uint32\_t clockSourceFreq\_Hz)  
*Configures the SPDIF Rx audio format.*
- void **SPDIF\_WriteBlocking** (SPDIF\_Type \*base, uint8\_t \*buffer, uint32\_t size)  
*Sends data using a blocking method.*
- static void **SPDIF\_WriteLeftData** (SPDIF\_Type \*base, uint32\_t data)  
*Writes data into SPDIF FIFO.*
- static void **SPDIF\_WriteRightData** (SPDIF\_Type \*base, uint32\_t data)  
*Writes data into SPDIF FIFO.*
- static void **SPDIF\_WriteChannelStatusHigh** (SPDIF\_Type \*base, uint32\_t data)  
*Writes data into SPDIF FIFO.*
- static void **SPDIF\_WriteChannelStatusLow** (SPDIF\_Type \*base, uint32\_t data)  
*Writes data into SPDIF FIFO.*
- void **SPDIF\_ReadBlocking** (SPDIF\_Type \*base, uint8\_t \*buffer, uint32\_t size)  
*Receives data using a blocking method.*
- static uint32\_t **SPDIF\_ReadLeftData** (SPDIF\_Type \*base)  
*Reads data from the SPDIF FIFO.*
- static uint32\_t **SPDIF\_ReadRightData** (SPDIF\_Type \*base)  
*Reads data from the SPDIF FIFO.*
- static uint32\_t **SPDIF\_ReadChannelStatusHigh** (SPDIF\_Type \*base)  
*Reads data from the SPDIF FIFO.*
- static uint32\_t **SPDIF\_ReadChannelStatusLow** (SPDIF\_Type \*base)  
*Reads data from the SPDIF FIFO.*
- static uint32\_t **SPDIF\_ReadQChannel** (SPDIF\_Type \*base)  
*Reads data from the SPDIF FIFO.*
- static uint32\_t **SPDIF\_ReadUChannel** (SPDIF\_Type \*base)  
*Reads data from the SPDIF FIFO.*

## Transactional

- void **SPDIF\_TransferTxCreateHandle** (SPDIF\_Type \*base, spdif\_handle\_t \*handle, **spdif\_transfer\_callback\_t** callback, void \*userData)  
*Initializes the SPDIF Tx handle.*
- void **SPDIF\_TransferRxCreateHandle** (SPDIF\_Type \*base, spdif\_handle\_t \*handle, **spdif\_transfer\_callback\_t** callback, void \*userData)  
*Initializes the SPDIF Rx handle.*
- status\_t **SPDIF\_TransferSendNonBlocking** (SPDIF\_Type \*base, spdif\_handle\_t \*handle, **spdif\_transfer\_t** \*xfer)  
*Performs an interrupt non-blocking send transfer on SPDIF.*
- status\_t **SPDIF\_TransferReceiveNonBlocking** (SPDIF\_Type \*base, spdif\_handle\_t \*handle, **spdif\_transfer\_t** \*xfer)

*Performs an interrupt non-blocking receive transfer on SPDIF.*

- **status\_t SPDIF\_TransferGetSendCount** (SPDIF\_Type \*base, spdif\_handle\_t \*handle, size\_t \*count)  
*Gets a set byte count.*
- **status\_t SPDIF\_TransferGetReceiveCount** (SPDIF\_Type \*base, spdif\_handle\_t \*handle, size\_t \*count)  
*Gets a received byte count.*
- **void SPDIF\_TransferAbortSend** (SPDIF\_Type \*base, spdif\_handle\_t \*handle)  
*Aborts the current send.*
- **void SPDIF\_TransferAbortReceive** (SPDIF\_Type \*base, spdif\_handle\_t \*handle)  
*Aborts the current IRQ receive.*
- **void SPDIF\_TransferTxHandleIRQ** (SPDIF\_Type \*base, spdif\_handle\_t \*handle)  
*Tx interrupt handler.*
- **void SPDIF\_TransferRxHandleIRQ** (SPDIF\_Type \*base, spdif\_handle\_t \*handle)  
*Rx interrupt handler.*

## 43.3 Data Structure Documentation

### 43.3.1 struct spdif\_config\_t

#### Data Fields

- bool **isTxAutoSync**  
*If auto sync mechanism open.*
- bool **isRxAutoSync**  
*If auto sync mechanism open.*
- uint8\_t **DPLLClkSource**  
*SPDIF DPLL clock source, range from 0~15, meaning is chip-specific.*
- uint8\_t **txClkSource**  
*SPDIF tx clock source, range from 0~7, meaning is chip-specific.*
- **spdif\_rxfull\_select\_t rxFullSelect**  
*SPDIF rx buffer full select.*
- **spdif\_txempty\_select\_t txFullSelect**  
*SPDIF tx buffer empty select.*
- **spdif\_uchannel\_source\_t uChannelSrc**  
*U channel source.*
- **spdif\_tx\_source\_t txSource**  
*SPDIF tx data source.*
- **spdif\_validity\_config\_t validityConfig**  
*Validity flag config.*
- **spdif\_gain\_select\_t gain**  
*Rx receive clock measure gain parameter.*

**Field Documentation**(1) `spdif_gain_select_t` `spdif_config_t::gain`**43.3.2 struct `spdif_transfer_t`****Data Fields**

- `uint8_t * data`  
*Data start address to transfer.*
- `uint8_t * qdata`  
*Data buffer for Q channel.*
- `uint8_t * udata`  
*Data buffer for C channel.*
- `size_t dataSize`  
*Transfer size.*

**Field Documentation**(1) `uint8_t*` `spdif_transfer_t::data`(2) `size_t` `spdif_transfer_t::dataSize`**43.3.3 struct `_spdif_handle`****Data Fields**

- `uint32_t state`  
*Transfer status.*
- `spdif_transfer_callback_t callback`  
*Callback function called at transfer event.*
- `void * userData`  
*Callback parameter passed to callback function.*
- `spdif_transfer_t` `spdifQueue [SPDIF_XFER_QUEUE_SIZE]`  
*Transfer queue storing queued transfer.*
- `size_t transferSize [SPDIF_XFER_QUEUE_SIZE]`  
*Data bytes need to transfer.*
- `volatile uint8_t queueUser`  
*Index for user to queue transfer.*
- `volatile uint8_t queueDriver`  
*Index for driver to get the transfer data and size.*
- `uint8_t watermark`  
*Watermark value.*

**43.4 Macro Definition Documentation****43.4.1 #define `SPDIF_XFER_QUEUE_SIZE (4U)`**

## 43.5 Enumeration Type Documentation

### 43.5.1 anonymous enum

Enumerator

- kStatus\_SPDIF\_RxPLLLocked* SPDIF Rx PLL locked.
- kStatus\_SPDIF\_TxFIFOError* SPDIF Tx FIFO error.
- kStatus\_SPDIF\_TxFIFOResync* SPDIF Tx left and right FIFO resync.
- kStatus\_SPDIF\_RxCnew* SPDIF Rx status channel value updated.
- kStatus\_SPDIF\_ValidateNoGood* SPDIF validate flag not good.
- kStatus\_SPDIF\_RxIllegalSymbol* SPDIF Rx receive illegal symbol.
- kStatus\_SPDIF\_RxParityBitError* SPDIF Rx parity bit error.
- kStatus\_SPDIF\_UChannelOverrun* SPDIF receive U channel overrun.
- kStatus\_SPDIF\_QChannelOverrun* SPDIF receive Q channel overrun.
- kStatus\_SPDIF\_UQChannelSync* SPDIF U/Q channel sync found.
- kStatus\_SPDIF\_UQChannelFrameError* SPDIF U/Q channel frame error.
- kStatus\_SPDIF\_RxFIFOError* SPDIF Rx FIFO error.
- kStatus\_SPDIF\_RxFIFOResync* SPDIF Rx left and right FIFO resync.
- kStatus\_SPDIF\_LockLoss* SPDIF Rx PLL clock lock loss.
- kStatus\_SPDIF\_TxIdle* SPDIF Tx is idle.
- kStatus\_SPDIF\_RxIdle* SPDIF Rx is idle.
- kStatus\_SPDIF\_QueueFull* SPDIF queue full.

### 43.5.2 enum spdif\_rxfull\_select\_t

Enumerator

- kSPDIF\_RxFull1Sample* Rx full at least 1 sample in left and right FIFO.
- kSPDIF\_RxFull4Samples* Rx full at least 4 sample in left and right FIFO.
- kSPDIF\_RxFull8Samples* Rx full at least 8 sample in left and right FIFO.
- kSPDIF\_RxFull16Samples* Rx full at least 16 sample in left and right FIFO.

### 43.5.3 enum spdif\_txempty\_select\_t

Enumerator

- kSPDIF\_TxEmpty0Sample* Tx empty at most 0 sample in left and right FIFO.
- kSPDIF\_TxEmpty4Samples* Tx empty at most 4 sample in left and right FIFO.
- kSPDIF\_TxEmpty8Samples* Tx empty at most 8 sample in left and right FIFO.
- kSPDIF\_TxEmpty12Samples* Tx empty at most 12 sample in left and right FIFO.

**43.5.4 enum spdif\_uchannel\_source\_t**

Enumerator

- kSPDIF\_NoUChannel* No embedded U channel.
- kSPDIF\_UChannelFromRx* U channel from receiver, it is CD mode.
- kSPDIF\_UChannelFromTx* U channel from on chip tx.

**43.5.5 enum spdif\_gain\_select\_t**

Enumerator

- kSPDIF\_GAIN\_24* Gain select is 24.
- kSPDIF\_GAIN\_16* Gain select is 16.
- kSPDIF\_GAIN\_12* Gain select is 12.
- kSPDIF\_GAIN\_8* Gain select is 8.
- kSPDIF\_GAIN\_6* Gain select is 6.
- kSPDIF\_GAIN\_4* Gain select is 4.
- kSPDIF\_GAIN\_3* Gain select is 3.

**43.5.6 enum spdif\_tx\_source\_t**

Enumerator

- kSPDIF\_txFromReceiver* Tx data directly through SPDIF receiver.
- kSPDIF\_txNormal* Normal operation, data from processor.

**43.5.7 enum spdif\_validity\_config\_t**

Enumerator

- kSPDIF\_validityFlagAlwaysSet* Outgoing validity flags always set.
- kSPDIF\_validityFlagAlwaysClear* Outgoing validity flags always clear.

**43.5.8 anonymous enum**

Enumerator

- kSPDIF\_RxDPLLLocked* SPDIF DPLL locked.
- kSPDIF\_TxFIFOError* Tx FIFO underrun or overrun.
- kSPDIF\_TxFIFOResync* Tx FIFO left and right channel resync.

*kSPDIF\_RxControlChannelChange* SPDIF Rx control channel value changed.  
*kSPDIF\_ValidityFlagNoGood* SPDIF validity flag no good.  
*kSPDIF\_RxIllegalSymbol* SPDIF receiver found illegal symbol.  
*kSPDIF\_RxParityBitError* SPDIF receiver found parity bit error.  
*kSPDIF\_UChannelReceiveRegisterFull* SPDIF U channel receive register full.  
*kSPDIF\_UChannelReceiveRegisterOverrun* SPDIF U channel receive register overrun.  
*kSPDIF\_QChannelReceiveRegisterFull* SPDIF Q channel receive register full.  
*kSPDIF\_QChannelReceiveRegisterOverrun* SPDIF Q channel receive register overrun.  
*kSPDIF\_UQChannelSync* SPDIF U/Q channel sync found.  
*kSPDIF\_UQChannelFrameError* SPDIF U/Q channel frame error.  
*kSPDIF\_RxFIFOError* SPDIF Rx FIFO underrun/overrun.  
*kSPDIF\_RxFIFOResync* SPDIF Rx left and right FIFO resync.  
*kSPDIF\_LockLoss* SPDIF receiver loss of lock.  
*kSPDIF\_TxFIFOEmpty* SPDIF Tx FIFO empty.  
*kSPDIF\_RxFIFOFull* SPDIF Rx FIFO full.  
*kSPDIF\_AllInterrupt* all interrupt

### 43.5.9 anonymous enum

Enumerator

*kSPDIF\_RxDMAEnable* Rx FIFO full.  
*kSPDIF\_TxDMAEnable* Tx FIFO empty.

## 43.6 Function Documentation

### 43.6.1 void SPDIF\_Init ( **SPDIF\_Type** \* *base*, **const spdif\_config\_t** \* *config* )

Ungates the SPDIF clock, resets the module, and configures SPDIF with a configuration structure. The configuration structure can be custom filled or set with default values by [SPDIF\\_GetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SPDIF driver. Otherwise, accessing the SPDIF module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	SPDIF base pointer
-------------	--------------------

<i>config</i>	SPDIF configuration structure.
---------------	--------------------------------

### 43.6.2 void SPDIF\_GetDefaultConfig ( *spdif\_config\_t* \* *config* )

This API initializes the configuration structure for use in SPDIF\_Init. The initialized structure can remain unchanged in SPDIF\_Init, or it can be modified before calling SPDIF\_Init. This is an example.

```
spdif_config_t config;
SPDIF_GetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

### 43.6.3 void SPDIF\_Deinit ( *SPDIF\_Type* \* *base* )

This API gates the SPDIF clock. The SPDIF module can't operate unless SPDIF\_Init is called to enable the clock.

Parameters

<i>base</i>	SPDIF base pointer
-------------	--------------------

### 43.6.4 uint32\_t SPDIFGetInstance ( *SPDIF\_Type* \* *base* )

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

### 43.6.5 static void SPDIF\_TxFIFOReset ( *SPDIF\_Type* \* *base* ) [inline], [static]

This function makes Tx FIFO in reset mode.

Parameters

<i>base</i>	SPDIF base pointer
-------------	--------------------

#### 43.6.6 static void SPDIF\_RxFIFOReset ( **SPDIF\_Type** \* *base* ) [inline], [static]

This function enables the software reset and FIFO reset of SPDIF Rx. After reset, clear the reset bit.

Parameters

<i>base</i>	SPDIF base pointer
-------------	--------------------

#### 43.6.7 void SPDIF\_TxEnable ( **SPDIF\_Type** \* *base*, **bool** *enable* )

Parameters

<i>base</i>	SPDIF base pointer
<i>enable</i>	True means enable SPDIF Tx, false means disable.

#### 43.6.8 static void SPDIF\_RxEnable ( **SPDIF\_Type** \* *base*, **bool** *enable* ) [inline], [static]

Parameters

<i>base</i>	SPDIF base pointer
<i>enable</i>	True means enable SPDIF Rx, false means disable.

#### 43.6.9 static uint32\_t SPDIF\_GetStatusFlag ( **SPDIF\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	SPDIF base pointer
-------------	--------------------

Returns

SPDIF status flag value. Use the `_spdif_interrupt_enable_t` to get the status value needed.

#### 43.6.10 static void SPDIF\_ClearStatusFlags ( **SPDIF\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	SPDIF base pointer
<i>mask</i>	<p>State mask. It can be a combination of the <code>_spdif_interrupt_enable_t</code> member. Notice these members cannot be included, as these flags cannot be cleared by writing 1 to these bits:</p> <ul style="list-style-type: none"> <li>• <code>kSPDIF_UChannelReceiveRegisterFull</code></li> <li>• <code>kSPDIF_QChannelReceiveRegisterFull</code></li> <li>• <code>kSPDIF_TxFIFOEmpty</code></li> <li>• <code>kSPDIF_RxFIFOFull</code></li> </ul>

#### 43.6.11 static void SPDIF\_EnableInterrupts ( **SPDIF\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	SPDIF base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• <code>kSPDIF_WordStartInterruptEnable</code></li> <li>• <code>kSPDIF_SyncErrorInterruptEnable</code></li> <li>• <code>kSPDIF_FIFOWarningInterruptEnable</code></li> <li>• <code>kSPDIF_FIFORequestInterruptEnable</code></li> <li>• <code>kSPDIF_FIFOErrorInterruptEnable</code></li> </ul>

#### 43.6.12 static void SPDIF\_DisableInterrupts ( **SPDIF\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	SPDIF base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kSPDIF_WordStartInterruptEnable</li> <li>• kSPDIF_SyncErrorInterruptEnable</li> <li>• kSPDIF_FIFOWarningInterruptEnable</li> <li>• kSPDIF_FIFOREquestInterruptEnable</li> <li>• kSPDIF_FIFOErrorInterruptEnable</li> </ul>

#### 43.6.13 static void SPDIF\_EnableDMA ( **SPDIF\_Type** \* *base*, **uint32\_t** *mask*, **bool enable** ) [inline], [static]

Parameters

<i>base</i>	SPDIF base pointer
<i>mask</i>	<p>SPDIF DMA enable mask, The parameter can be a combination of the following sources if defined</p> <ul style="list-style-type: none"> <li>• kSPDIF_RxDMAEnable</li> <li>• kSPDIF_TxDMAEnable</li> </ul>
<i>enable</i>	True means enable DMA, false means disable DMA.

#### 43.6.14 static **uint32\_t** SPDIF\_TxGetLeftDataRegisterAddress ( **SPDIF\_Type** \* *base* ) [inline], [static]

This API is used to provide a transfer address for the SPDIF DMA transfer configuration.

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

data register address.

**43.6.15 static uint32\_t SPDIF\_TxGetRightDataRegisterAddress ( SPDIF\_Type \*  
base ) [inline], [static]**

This API is used to provide a transfer address for the SPDIF DMA transfer configuration.

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

data register address.

#### 43.6.16 static uint32\_t SPDIF\_RxGetLeftDataRegisterAddress ( **SPDIF\_Type** \* *base* ) [inline], [static]

This API is used to provide a transfer address for the SPDIF DMA transfer configuration.

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

data register address.

#### 43.6.17 static uint32\_t SPDIF\_RxGetRightDataRegisterAddress ( **SPDIF\_Type** \* *base* ) [inline], [static]

This API is used to provide a transfer address for the SPDIF DMA transfer configuration.

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

data register address.

#### 43.6.18 void SPDIF\_TxSetSampleRate ( **SPDIF\_Type** \* *base*, **uint32\_t** *sampleRate\_Hz*, **uint32\_t** *sourceClockFreq\_Hz* )

The audio format can be changed at run-time. This function configures the sample rate.

Parameters

<i>base</i>	SPDIF base pointer.
<i>sampleRate_Hz</i>	SPDIF sample rate frequency in Hz.
<i>sourceClock-Freq_Hz</i>	SPDIF tx clock source frequency in Hz.

#### 43.6.19 **uint32\_t SPDIF\_GetRxSampleRate ( SPDIF\_Type \* *base*, uint32\_t *clockSourceFreq\_Hz* )**

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SPDIF base pointer.
<i>clockSource-Freq_Hz</i>	SPDIF system clock frequency in hz.

#### 43.6.20 **void SPDIF\_WriteBlocking ( SPDIF\_Type \* *base*, uint8\_t \* *buffer*, uint32\_t *size* )**

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SPDIF base pointer.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

#### 43.6.21 **static void SPDIF\_WriteLeftData ( SPDIF\_Type \* *base*, uint32\_t *data* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
<i>data</i>	Data needs to be written.

**43.6.22 static void SPDIF\_WriteRightData ( *SPDIF\_Type* \* *base*, *uint32\_t* *data* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
<i>data</i>	Data needs to be written.

**43.6.23 static void SPDIF\_WriteChannelStatusHigh ( *SPDIF\_Type* \* *base*, *uint32\_t* *data* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
<i>data</i>	Data needs to be written.

**43.6.24 static void SPDIF\_WriteChannelStatusLow ( *SPDIF\_Type* \* *base*, *uint32\_t* *data* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
<i>data</i>	Data needs to be written.

**43.6.25 void SPDIF\_ReadBlocking ( *SPDIF\_Type* \* *base*, *uint8\_t* \* *buffer*, *uint32\_t* *size* )**

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SPDIF base pointer.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

**43.6.26 static uint32\_t SPDIF\_ReadLeftData ( SPDIF\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

Data in SPDIF FIFO.

**43.6.27 static uint32\_t SPDIF\_ReadRightData ( SPDIF\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

Data in SPDIF FIFO.

**43.6.28 static uint32\_t SPDIF\_ReadChannelStatusHigh ( SPDIF\_Type \* *base* ) [inline], [static]**

Parameters

---

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

Data in SPDIF FIFO.

**43.6.29 static uint32\_t SPDIF\_ReadChannelStatusLow ( SPDIF\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

Data in SPDIF FIFO.

**43.6.30 static uint32\_t SPDIF\_ReadQChannel ( SPDIF\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

Data in SPDIF FIFO.

**43.6.31 static uint32\_t SPDIF\_ReadUChannel ( SPDIF\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

Returns

Data in SPDIF FIFO.

**43.6.32 void SPDIF\_TransferTxCreateHandle ( *SPDIF\_Type* \* *base*, *spdif\_handle\_t* \* *handle*, *spdif\_transfer\_callback\_t* *callback*, *void* \* *userData* )**

This function initializes the Tx handle for the SPDIF Tx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SPDIF base pointer
<i>handle</i>	SPDIF handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function

#### 43.6.33 void SPDIF\_TransferRxCreateHandle ( **SPDIF\_Type** \* *base*, **spdif\_handle\_t** \* *handle*, **spdif\_transfer\_callback\_t** *callback*, **void** \* *userData* )

This function initializes the Rx handle for the SPDIF Rx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	SPDIF handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function.

#### 43.6.34 status\_t SPDIF\_TransferSendNonBlocking ( **SPDIF\_Type** \* *base*, **spdif\_handle\_t** \* *handle*, **spdif\_transfer\_t** \* *xfer* )

Note

This API returns immediately after the transfer initiates. Call the SPDIF\_TxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus\_SPDIF\_Busy, the transfer is finished.

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	Pointer to the <b>spdif_handle_t</b> structure which stores the transfer state.
<i>xfer</i>	Pointer to the <b>spdif_transfer_t</b> structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SPDIF_TxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

#### 43.6.35 status\_t SPDIF\_TransferReceiveNonBlocking ( **SPDIF\_Type** \* *base*, **spdif\_handle\_t** \* *handle*, **spdif\_transfer\_t** \* *xfer* )

Note

This API returns immediately after the transfer initiates. Call the SPDIF\_RxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not *kStatus\_SPDIF\_Busy*, the transfer is finished.

Parameters

<i>base</i>	SPDIF base pointer
<i>handle</i>	Pointer to the <b>spdif_handle_t</b> structure which stores the transfer state.
<i>xfer</i>	Pointer to the <b>spdif_transfer_t</b> structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SPDIF_RxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

#### 43.6.36 status\_t SPDIF\_TransferGetSendCount ( **SPDIF\_Type** \* *base*, **spdif\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	SPDIF base pointer.
-------------	---------------------

<i>handle</i>	Pointer to the spdif_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

#### 43.6.37 status\_t SPDIF\_TransferGetReceiveCount ( **SPDIF\_Type** \* *base*, **spdif\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	Pointer to the spdif_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

#### 43.6.38 void SPDIF\_TransferAbortSend ( **SPDIF\_Type** \* *base*, **spdif\_handle\_t** \* *handle* )

Note

This API can be called any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	Pointer to the spdif_handle_t structure which stores the transfer state.

**43.6.39 void SPDIF\_TransferAbortReceive ( *SPDIF\_Type* \* *base*, *spdif\_handle\_t* \* *handle* )**

Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SPDIF base pointer
<i>handle</i>	Pointer to the <i>spdif_handle_t</i> structure which stores the transfer state.

**43.6.40 void SPDIF\_TransferTxHandleIRQ ( *SPDIF\_Type* \* *base*, *spdif\_handle\_t* \* *handle* )**

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	Pointer to the <i>spdif_handle_t</i> structure.

**43.6.41 void SPDIF\_TransferRxHandleIRQ ( *SPDIF\_Type* \* *base*, *spdif\_handle\_t* \* *handle* )**

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	Pointer to the <i>spdif_handle_t</i> structure.

## 43.7 SPDIF eDMA Driver

### 43.7.1 Overview

#### Data Structures

- struct [spdif\\_edma\\_transfer\\_t](#)  
*SPDIF transfer structure. [More...](#)*
- struct [spdif\\_edma\\_handle\\_t](#)  
*SPDIF DMA transfer handle, users should not touch the content of the handle. [More...](#)*

#### Typedefs

- [typedef void\(\\* spdif\\_edma\\_callback\\_t \)](#)(SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle, [status\\_t](#) status, void \*userData)  
*SPDIF eDMA transfer callback function for finish and error.*

#### Driver version

- #define [FSL\\_SPDIF\\_EDMA\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 0, 5))  
*Version 2.0.5.*

#### eDMA Transactional

- void [SPDIF\\_TransferTxCreateHandleEDMA](#) (SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle, [spdif\\_edma\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*dmaLeftHandle, [edma\\_handle\\_t](#) \*dmaRightHandle)  
*Initializes the SPDIF eDMA handle.*
- void [SPDIF\\_TransferRxCreateHandleEDMA](#) (SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle, [spdif\\_edma\\_callback\\_t](#) callback, void \*userData, [edma\\_handle\\_t](#) \*dmaLeftHandle, [edma\\_handle\\_t](#) \*dmaRightHandle)  
*Initializes the SPDIF Rx eDMA handle.*
- [status\\_t SPDIF\\_TransferSendEDMA](#) (SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle, [spdif\\_edma\\_transfer\\_t](#) \*xfer)  
*Performs a non-blocking SPDIF transfer using DMA.*
- [status\\_t SPDIF\\_TransferReceiveEDMA](#) (SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle, [spdif\\_edma\\_transfer\\_t](#) \*xfer)  
*Performs a non-blocking SPDIF receive using eDMA.*
- void [SPDIF\\_TransferAbortSendEDMA](#) (SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle)  
*Aborts a SPDIF transfer using eDMA.*
- void [SPDIF\\_TransferAbortReceiveEDMA](#) (SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle)  
*Aborts a SPDIF receive using eDMA.*
- [status\\_t SPDIF\\_TransferGetSendCountEDMA](#) (SPDIF\_Type \*base, spdif\_edma\_handle\_t \*handle, [size\\_t](#) \*count)  
*Gets byte count sent by SPDIF.*

- `status_t SPDIF_TransferGetReceiveCountEDMA (SPDIF_Type *base, spdif_edma_handle_t *handle, size_t *count)`  
*Gets byte count received by SPDIF.*

## 43.7.2 Data Structure Documentation

### 43.7.2.1 struct spdif\_edma\_transfer\_t

#### Data Fields

- `uint8_t * leftData`  
*Data start address to transfer.*
- `uint8_t * rightData`  
*Data start address to transfer.*
- `size_t dataSize`  
*Transfer size.*

#### Field Documentation

- (1) `uint8_t* spdif_edma_transfer_t::leftData`
- (2) `uint8_t* spdif_edma_transfer_t::rightData`
- (3) `size_t spdif_edma_transfer_t::dataSize`

### 43.7.2.2 struct \_spdif\_edma\_handle

#### Data Fields

- `edma_handle_t * dmaLeftHandle`  
*DMA handler for SPDIF left channel.*
- `edma_handle_t * dmaRightHandle`  
*DMA handler for SPDIF right channel.*
- `uint8_t nbytes`  
*eDMA minor byte transfer count initially configured.*
- `uint8_t count`  
*The transfer data count in a DMA request.*
- `uint32_t state`  
*Internal state for SPDIF eDMA transfer.*
- `spdif_edma_callback_t callback`  
*Callback for users while transfer finish or error occurs.*
- `void * userData`  
*User callback parameter.*
- `edma_tcd_t leftTcd [SPDIF_XFER_QUEUE_SIZE+1U]`  
*TCD pool for eDMA transfer.*
- `edma_tcd_t rightTcd [SPDIF_XFER_QUEUE_SIZE+1U]`  
*TCD pool for eDMA transfer.*
- `spdif_edma_transfer_t spdifQueue [SPDIF_XFER_QUEUE_SIZE]`  
*Transfer queue storing queued transfer.*

- size\_t `transferSize` [SPDIF\_XFER\_QUEUE\_SIZE]  
*Data bytes need to transfer, left and right are the same, so use one.*
- volatile uint8\_t `queueUser`  
*Index for user to queue transfer.*
- volatile uint8\_t `queueDriver`  
*Index for driver to get the transfer data and size.*

## Field Documentation

- (1) `uint8_t spdif_edma_handle_t::nbytes`
- (2) `edma_tcd_t spdif_edma_handle_t::leftTcd[SPDIF_XFER_QUEUE_SIZE+1U]`
- (3) `edma_tcd_t spdif_edma_handle_t::rightTcd[SPDIF_XFER_QUEUE_SIZE+1U]`
- (4) `spdif_edma_transfer_t spdif_edma_handle_t::spdifQueue[SPDIF_XFER_QUEUE_SIZE]`
- (5) `volatile uint8_t spdif_edma_handle_t::queueUser`

## 43.7.3 Function Documentation

**43.7.3.1 void SPDIF\_TransferTxCreateHandleEDMA ( `SPDIF_Type * base,`  
`spdif_edma_handle_t * handle, spdif_edma_callback_t callback, void *`  
`userData, edma_handle_t * dmaLeftHandle, edma_handle_t * dmaRightHandle` )**

This function initializes the SPDIF master DMA handle, which can be used for other SPDIF master transactional APIs. Usually, for a specified SPDIF instance, call this API once to get the initialized handle.

### Parameters

<code>base</code>	SPDIF base pointer.
<code>handle</code>	SPDIF eDMA handle pointer.
<code>base</code>	SPDIF peripheral base address.
<code>callback</code>	Pointer to user callback function.
<code>userData</code>	User parameter passed to the callback function.
<code>dmaLeftHandle</code>	eDMA handle pointer for left channel, this handle shall be static allocated by users.
<code>dmaRightHandle</code>	eDMA handle pointer for right channel, this handle shall be static allocated by users.

```
43.7.3.2 void SPDIF_TransferRxCreateHandleEDMA ( SPDIF_Type * base,  
          spdif_edma_handle_t * handle, spdif_edma_callback_t callback, void *  
          userData, edma_handle_t * dmaLeftHandle, edma_handle_t * dmaRightHandle )
```

This function initializes the SPDIF slave DMA handle, which can be used for other SPDIF master transactional APIs. Usually, for a specified SPDIF instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	SPDIF eDMA handle pointer.
<i>base</i>	SPDIF peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>dmaLeftHandle</i>	eDMA handle pointer for left channel, this handle shall be static allocated by users.
<i>dmaRightHandle</i>	eDMA handle pointer for right channel, this handle shall be static allocated by users.

#### 43.7.3.3 status\_t SPDIF\_TransferSendEDMA ( **SPDIF\_Type** \* *base*, **spdif\_edma\_handle\_t** \* *handle*, **spdif\_edma\_transfer\_t** \* *xfer* )

Note

This interface returns immediately after the transfer initiates. Call SPDIF\_GetTransferStatus to poll the transfer status and check whether the SPDIF transfer is finished.

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	SPDIF eDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SPDIF eDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_TxBusy</i>	SPDIF is busy sending data.

#### 43.7.3.4 status\_t SPDIF\_TransferReceiveEDMA ( **SPDIF\_Type** \* *base*, **spdif\_edma\_handle\_t** \* *handle*, **spdif\_edma\_transfer\_t** \* *xfer* )

Note

This interface returns immediately after the transfer initiates. Call the SPDIF\_GetReceiveRemainingBytes to poll the transfer status and check whether the SPDIF transfer is finished.

Parameters

<i>base</i>	SPDIF base pointer
<i>handle</i>	SPDIF eDMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SPDIF eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_RxBusy</i>	SPDIF is busy receiving data.

#### 43.7.3.5 void SPDIF\_TransferAbortSendEDMA ( **SPDIF\_Type** \* *base*, **spdif\_edma\_handle\_t** \* *handle* )

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	SPDIF eDMA handle pointer.

#### 43.7.3.6 void SPDIF\_TransferAbortReceiveEDMA ( **SPDIF\_Type** \* *base*, **spdif\_edma\_handle\_t** \* *handle* )

Parameters

<i>base</i>	SPDIF base pointer
<i>handle</i>	SPDIF eDMA handle pointer.

#### 43.7.3.7 **status\_t** SPDIF\_TransferGetSendCountEDMA ( **SPDIF\_Type** \* *base*, **spdif\_edma\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

<i>base</i>	SPDIF base pointer.
<i>handle</i>	SPDIF eDMA handle pointer.
<i>count</i>	Bytes count sent by SPDIF.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is no non-blocking transaction in progress.

#### 43.7.3.8 **status\_t SPDIF\_TransferGetReceiveCountEDMA ( *SPDIF\_Type \* base, spdif\_edma\_handle\_t \* handle, size\_t \* count* )**

Parameters

<i>base</i>	SPDIF base pointer
<i>handle</i>	SPDIF eDMA handle pointer.
<i>count</i>	Bytes count received by SPDIF.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is no non-blocking transaction in progress.

# Chapter 44

## SRC: System Reset Controller Driver

### 44.1 Overview

The MCUXpresso SDK provides a peripheral driver for the System Reset Controller (SRC) module.

The System Reset Controller (SRC) controls the reset and boot operation of the SoC. It is responsible for the generation of all reset signals and boot decoding. The reset controller determines the source and the type of reset, such as POR, WARM, COLD, and performs the necessary reset qualification and stretching sequences. Based on the type of reset, the reset logic generates the reset sequence for the entire IC.

### Enumerations

- enum `_src_reset_status_flags` {  
    `kSRC_TemperatureSensorResetFlag` = SRC\_SRSR\_TS\_R\_MASK,  
    `kSRC_Wdog3ResetFlag` = SRC\_SRSR\_WDOG3\_RST\_B\_MASK,  
    `kSRC_JTAGSystemResetFlag`,  
    `kSRC_JTAGSoftwareResetFlag` = SRC\_SRSR\_SJC\_MASK,  
    `kSRC_JTAGGeneratedResetFlag` = SRC\_SRSR\_JTAG\_MASK,  
    `kSRC_WatchdogResetFlag` = SRC\_SRSR\_WDOG\_MASK,  
    `kSRC_IppUserResetFlag` = SRC\_SRSR\_IPP\_USER\_RESET\_B\_MASK,  
    `kSRC_CsuResetFlag` = SRC\_SRSR\_CSU\_RESET\_B\_MASK,  
    `kSRC_LockupSysResetFlag`,  
    `kSRC_IppResetPinFlag` = SRC\_SRSR\_IPP\_RESET\_B\_MASK }  
        *SRC reset status flags.*
- enum `src_warm_reset_bypass_count_t` {  
    `kSRC_WarmResetWaitAlways` = 0U,  
    `kSRC_WarmResetWaitClk16` = 1U,  
    `kSRC_WarmResetWaitClk32` = 2U,  
    `kSRC_WarmResetWaitClk64` = 3U }  
        *Selection of WARM reset bypass count.*

### Functions

- static void `SRC_EnableWDOG3Reset` (SRC\_Type \*base, bool enable)  
        *Enable the WDOG3 reset.*
- static void `SRC_EnableCoreDebugResetAfterPowerGate` (SRC\_Type \*base, bool enable)  
        *Debug reset would be asserted after power gating event.*
- static void `SRC_DoSoftwareResetARMCore0` (SRC\_Type \*base)  
        *Do software reset the ARM core0 only.*
- static bool `SRC_GetSoftwareResetARMCore0Done` (SRC\_Type \*base)  
        *Check if the software for ARM core0 is done.*
- static void `SRC_EnableWDOGReset` (SRC\_Type \*base, bool enable)  
        *Enable the WDOG Reset in SRC.*

- static uint32\_t [SRC\\_GetBootModeWord1](#) (SRC\_Type \*base)  
*Get the boot mode register 1 value.*
- static uint32\_t [SRC\\_GetBootModeWord2](#) (SRC\_Type \*base)  
*Get the boot mode register 2 value.*
- static uint32\_t [SRC\\_GetResetStatusFlags](#) (SRC\_Type \*base)  
*Get the status flags of SRC.*
- void [SRC\\_ClearResetStatusFlags](#) (SRC\_Type \*base, uint32\_t flags)  
*Clear the status flags of SRC.*
- static void [SRC\\_SetGeneralPurposeRegister](#) (SRC\_Type \*base, uint32\_t index, uint32\_t value)  
*Set value to general purpose registers.*
- static uint32\_t [SRC\\_GetGeneralPurposeRegister](#) (SRC\_Type \*base, uint32\_t index)  
*Get the value from general purpose registers.*

## Driver version

- #define [FSL\\_SRC\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 0, 1))  
*SRC driver version 2.0.1.*

## 44.2 Macro Definition Documentation

### 44.2.1 #define FSL\_SRC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 1))

## 44.3 Enumeration Type Documentation

### 44.3.1 enum \_src\_reset\_status\_flags

Enumerator

**kSRC\_TemperatureSensorResetFlag** Indicates whether the reset was the result of software reset from on-chip Temperature Sensor. Temperature Sensor Interrupt needs to be served before this bit can be cleaned.

**kSRC\_Wdog3ResetFlag** IC Watchdog3 Time-out reset. Indicates whether the reset was the result of the watchdog3 time-out event.

**kSRC\_JTAGSystemResetFlag** Indicates whether the reset was the result of software reset form JTAG.

**kSRC\_JTAGSoftwareResetFlag** Indicates whether the reset was the result of setting SJC\_GPCCR bit 31.

**kSRC\_JTAGGeneratedResetFlag** Indicates a reset has been caused by JTAG selection of certain IR codes: EXTEST or HIGHZ.

**kSRC\_WatchdogResetFlag** Indicates a reset has been caused by the watchdog timer timing out. This reset source can be blocked by disabling the watchdog.

**kSRC\_IppUserResetFlag** Indicates whether the reset was the result of the ipp\_user\_reset\_b qualified reset.

**kSRC\_CsuResetFlag** Indicates whether the reset was the result of the csu\_reset\_b input.

**kSRC\_LockupSysResetFlag** Indicates a reset has been caused by CPU lockup or software setting of SYSRESETREQ bit in Application Interrupt and Reset Control Register of the ARM core.

**kSRC\_IppResetPinFlag** Indicates whether reset was the result of ipp\_reset\_b pin (Power-up sequence).

### 44.3.2 enum src\_warm\_reset\_bypass\_count\_t

This type defines the 32KHz clock cycles to count before bypassing the MMDC acknowledge for WARM reset. If the MMDC acknowledge is not asserted before this counter is elapsed, a COLD reset will be initiated.

Enumerator

*kSRC\_WarmResetWaitAlways* System will wait until MMDC acknowledge is asserted.

*kSRC\_WarmResetWaitClk16* Wait 16 32KHz clock cycles before switching the reset.

*kSRC\_WarmResetWaitClk32* Wait 32 32KHz clock cycles before switching the reset.

*kSRC\_WarmResetWaitClk64* Wait 64 32KHz clock cycles before switching the reset.

## 44.4 Function Documentation

### 44.4.1 static void SRC\_EnableWDOG3Reset ( *SRC\_Type* \* *base*, *bool enable* ) [inline], [static]

The WDOG3 reset is enabled by default.

Parameters

<i>base</i>	SRC peripheral base address.
<i>enable</i>	Enable the reset or not.

### 44.4.2 static void SRC\_EnableCoreDebugResetAfterPowerGate ( *SRC\_Type* \* *base*, *bool enable* ) [inline], [static]

Parameters

<i>base</i>	SRC peripheral base address.
<i>enable</i>	Enable the reset or not.

### 44.4.3 static void SRC\_DoSoftwareResetARMCore0 ( *SRC\_Type* \* *base* ) [inline], [static]

Parameters

<i>base</i>	SRC peripheral base address.
-------------	------------------------------

#### 44.4.4 static bool SRC\_GetSoftwareResetARMCore0Done ( SRC\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	SRC peripheral base address.
-------------	------------------------------

Returns

If the reset is done.

#### 44.4.5 static void SRC\_EnableWDOGReset ( SRC\_Type \* *base*, bool *enable* ) [inline], [static]

WDOG Reset is enabled in SRC by default. If the WDOG event to SRC is masked, it would not create a reset to the chip. During the time the WDOG event is masked, when the WDOG event flag is asserted, it would remain asserted regardless of servicing the WDOG module. The only way to clear that bit is the hardware reset.

Parameters

<i>base</i>	SRC peripheral base address.
<i>enable</i>	Enable the reset or not.

#### 44.4.6 static uint32\_t SRC\_GetBootModeWord1 ( SRC\_Type \* *base* ) [inline], [static]

The Boot Mode register contains bits that reflect the status of BOOT\_CFGx pins of the chip. See to chip-specific document for detail information about value.

Parameters

<i>base</i>	SRC peripheral base address.
-------------	------------------------------

Returns

status of BOOT\_CFGx pins of the chip.

#### 44.4.7 static uint32\_t SRC\_GetBootModeWord2( SRC\_Type \* *base* ) [inline], [static]

The Boot Mode register contains bits that reflect the status of BOOT\_MODEx Pins and fuse values that controls boot of the chip. See to chip-specific document for detail information about value.

Parameters

<i>base</i>	SRC peripheral base address.
-------------	------------------------------

Returns

status of BOOT\_MODEx Pins and fuse values that controls boot of the chip.

#### 44.4.8 static uint32\_t SRC\_GetResetStatusFlags( SRC\_Type \* *base* ) [inline], [static]

Parameters

<i>base</i>	SRC peripheral base address.
-------------	------------------------------

Returns

Mask value of status flags, see to [\\_src\\_reset\\_status\\_flags](#).

#### 44.4.9 void SRC\_ClearResetStatusFlags( SRC\_Type \* *base*, uint32\_t *flags* )

Parameters

<i>base</i>	SRC peripheral base address.
<i>flags</i>	value of status flags to be cleared, see to <a href="#">_src_reset_status_flags</a> .

#### 44.4.10 static void SRC\_SetGeneralPurposeRegister ( **SRC\_Type** \* *base*, **uint32\_t** *index*, **uint32\_t** *value* ) [inline], [static]

General purpose registers (GPRx) would hold the value during reset process. Wakeup function could be kept in these register. For example, the GPR1 holds the entry function for waking-up from Partial SLEEP mode while the GPR2 holds the argument. Other GPRx register would store the arbitray values.

Parameters

<i>base</i>	SRC peripheral base address.
<i>index</i>	The index of GPRx register array. Note index 0 reponses the GPR1 register.
<i>value</i>	Setting value for GPRx register.

#### 44.4.11 static **uint32\_t** SRC\_GetGeneralPurposeRegister ( **SRC\_Type** \* *base*, **uint32\_t** *index* ) [inline], [static]

Parameters

<i>base</i>	SRC peripheral base address.
<i>index</i>	The index of GPRx register array. Note index 0 reponses the GPR1 register.

Returns

The setting value for GPRx register.

# Chapter 45

## TEMPMON: Temperature Monitor Module

### 45.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Temperature Monitor Module (TEMPMON) module of MCUXpresso SDK devices.

### 45.2 TEMP MON: Temperature Monitor Module

#### 45.2.1 TEMP MON Operations

The function `TEMPMON_Init()` will initialize the TEMP MON peripheral operation.

The function `TEMPMON_Deinit()` will deinitialize the TEMP MON peripheral operation.

The function `TEMPMON_GetDefaultConfig()` will get default configuration.

The function `TEMPMON_StartMeasure()` will start the temperature measurement process.

The function `TEMPMON_StopMeasure()` will stop the temperature measurement process.

The function `TEMPMON_GetCurrentTemp()` will get the current temperature.

The function `TEMPMON_SetTempAlarm()` will set the temperature count that will generate an alarm interrupt.

#### Files

- file `fsl_tempmon.h`

#### Data Structures

- struct `tempmon_config_t`  
*TEMP MON temperature structure. More...*

#### Enumerations

- enum `tempmon_alarm_mode` {  
  `kTEMPMON_HighAlarmMode` = 0U,  
  `kTEMPMON_PanicAlarmMode` = 1U,  
  `kTEMPMON_LowAlarmMode` = 2U }  
*TEMP MON alarm mode.*

#### Functions

- void `TEMPMON_Init` (TEMPMON\_Type \*base, const `tempmon_config_t` \*config)

- `void TEMPMON_Deinit (TEMPMON_Type *base)`  
*Deinitializes the TEMPMON module.*
- `void TEMPMON_GetDefaultConfig (tempmon_config_t *config)`  
*Gets the default configuration structure.*
- `static void TEMPMON_StartMeasure (TEMPMON_Type *base)`  
*start the temperature measurement process.*
- `static void TEMPMON_StopMeasure (TEMPMON_Type *base)`  
*stop the measurement process.*
- `float TEMPMON_GetCurrentTemperature (TEMPMON_Type *base)`  
*Get current temperature with the fused temperature calibration data.*
- `void TEMPMON_SetTempAlarm (TEMPMON_Type *base, int8_t tempVal, tempmon_alarm_mode alarmMode)`  
*Set the temperature count (raw sensor output) that will generate an alarm interrupt.*

## Driver version

- `#define FSL_TEMPMON_DRIVER_VERSION (MAKE_VERSION(2, 1, 1))`  
*TEMPMON driver version.*

## 45.3 Data Structure Documentation

### 45.3.1 struct tempmon\_config\_t

#### Data Fields

- `uint16_t frequency`  
*The temperature measure frequency.*
- `int8_t highAlarmTemp`  
*The high alarm temperature.*
- `int8_t panicAlarmTemp`  
*The panic alarm temperature.*
- `int8_t lowAlarmTemp`  
*The low alarm temperature.*

#### Field Documentation

- (1) `uint16_t tempmon_config_t::frequency`
- (2) `int8_t tempmon_config_t::highAlarmTemp`
- (3) `int8_t tempmon_config_t::panicAlarmTemp`
- (4) `int8_t tempmon_config_t::lowAlarmTemp`

## 45.4 Macro Definition Documentation

### 45.4.1 #define FSL\_TEMPMON\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))

## 45.5 Enumeration Type Documentation

### 45.5.1 enum tempmon\_alarm\_mode

Enumerator

***kTEMPMON\_HighAlarmMode*** The high alarm temperature interrupt mode.

***kTEMPMON\_PanicAlarmMode*** The panic alarm temperature interrupt mode.

***kTEMPMON\_LowAlarmMode*** The low alarm temperature interrupt mode.

## 45.6 Function Documentation

### 45.6.1 void TEMPMON\_Init ( **TEMPMON\_Type** \* *base*, **const tempmon\_config\_t** \* *config* )

Parameters

<i>base</i>	TEMPMON base pointer
<i>config</i>	Pointer to configuration structure.

### 45.6.2 void TEMPMON\_Deinit ( **TEMPMON\_Type** \* *base* )

Parameters

<i>base</i>	TEMPMON base pointer
-------------	----------------------

### 45.6.3 void TEMPMON\_GetDefaultConfig ( **tempmon\_config\_t** \* *config* )

This function initializes the TEMPMON configuration structure to a default value. The default values are: tempmonConfig->frequency = 0x02U; tempmonConfig->highAlarmTemp = 44U; tempmonConfig->panicAlarmTemp = 90U; tempmonConfig->lowAlarmTemp = 39U;

Parameters

<i>config</i>	Pointer to a configuration structure.
---------------	---------------------------------------

### 45.6.4 static void TEMPMON\_StartMeasure ( **TEMPMON\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	TEMPMON base pointer.
-------------	-----------------------

**45.6.5 static void TEMPMON\_StopMeasure ( TEMPMON\_Type \* *base* )  
[inline], [static]**

Parameters

<i>base</i>	TEMPMON base pointer
-------------	----------------------

**45.6.6 float TEMPMON\_GetCurrentTemperature ( TEMPMON\_Type \* *base* )**

Parameters

<i>base</i>	TEMPMON base pointer
-------------	----------------------

Returns

current temperature with degrees Celsius.

**45.6.7 void TEMPMON\_SetTempAlarm ( TEMPMON\_Type \* *base*, int8\_t *tempVal*, tempmon\_alarm\_mode *alarmMode* )**

Parameters

<i>base</i>	TEMPMON base pointer
<i>tempVal</i>	The alarm temperature with degrees Celsius
<i>alarmMode</i>	The alarm mode.

# Chapter 46

## TRNG: True Random Number Generator

### 46.1 Overview

The MCUXpresso SDK provides a peripheral driver for the True Random Number Generator (TRNG) module of MCUXpresso SDK devices.

The True Random Number Generator is a hardware accelerator module that generates a 512-bit entropy as needed by an entropy consuming module or by other post processing functions. A typical entropy consumer is a pseudo random number generator (PRNG) which can be implemented to achieve both true randomness and cryptographic strength random numbers using the TRNG output as its entropy seed. The entropy generated by a TRNG is intended for direct use by functions that generate secret keys, per-message secrets, random challenges, and other similar quantities used in cryptographic algorithms.

### 46.2 TRNG Initialization

1. Define the TRNG user configuration structure. Use `TRNG_InitUserConfigDefault()` function to set it to default TRNG configuration values.
2. Initialize the TRNG module, call the `TRNG_Init()` function, and pass the user configuration structure. This function automatically enables the TRNG module and its clock. After that, the TRNG is enabled and the entropy generation starts working.
3. To disable the TRNG module, call the `TRNG_Deinit()` function.

### 46.3 Get random data from TRNG

1. `TRNG_GetRandomData()` function gets random data from the TRNG module.

This example code shows how to initialize and get random data from the TRNG driver.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/trng

## Data Structures

- struct `trng_statistical_check_limit_t`  
*Data structure for definition of statistical check limits. [More...](#)*
- struct `trng_config_t`  
*Data structure for the TRNG initialization. [More...](#)*

## Enumerations

- enum `trng_sample_mode_t` {  
  `kTRNG_SampleModeVonNeumann` = 0U,  
  `kTRNG_SampleModeRaw` = 1U,  
  `kTRNG_SampleModeVonNeumannRaw` }  
*TRNG sample mode.*

- enum `trng_clock_mode_t` {
   
    `kTRNG_ClockModeRingOscillator` = 0U,
   
    `kTRNG_ClockModeSystem` = 1U }
   
*TRNG clock mode.*
- enum `trng_ring_osc_div_t` {
   
    `kTRNG_RingOscDiv0` = 0U,
   
    `kTRNG_RingOscDiv2` = 1U,
   
    `kTRNG_RingOscDiv4` = 2U,
   
    `kTRNG_RingOscDiv8` = 3U }
   
*TRNG ring oscillator divide.*

## Functions

- `status_t TRNG_GetDefaultConfig (trng_config_t *userConfig)`
  
*Initializes the user configuration structure to default values.*
- `status_t TRNG_Init (TRNG_Type *base, const trng_config_t *userConfig)`
  
*Initializes the TRNG.*
- `void TRNG_Deinit (TRNG_Type *base)`
  
*Shuts down the TRNG.*
- `status_t TRNG_GetRandomData (TRNG_Type *base, void *data, size_t dataSize)`
  
*Gets random data.*

## Driver version

- `#define FSL_TRNG_DRIVER_VERSION (MAKE_VERSION(2, 0, 16))`
  
*TRNG driver version 2.0.16.*

## 46.4 Data Structure Documentation

### 46.4.1 struct `trng_statistical_check_limit_t`

Used by `trng_config_t`.

#### Data Fields

- `uint32_t maximum`
  
*Maximum limit.*
- `uint32_t minimum`
  
*Minimum limit.*

**Field Documentation**

- (1) `uint32_t trng_statistical_check_limit_t::maximum`
- (2) `uint32_t trng_statistical_check_limit_t::minimum`

**46.4.2 struct trng\_config\_t**

This structure initializes the TRNG by calling the `TRNG_Init()` function. It contains all TRNG configurations.

**Data Fields**

- `bool lock`  
*Disable programmability of TRNG registers.*
- `trng_clock_mode_t clockMode`  
*Clock mode used to operate TRNG.*
- `trng_ring_osc_div_t ringOscDiv`  
*Ring oscillator divide used by TRNG.*
- `trng_sample_mode_t sampleMode`  
*Sample mode of the TRNG ring oscillator.*
- `uint16_t entropyDelay`  
*Entropy Delay.*
- `uint16_t sampleSize`  
*Sample Size.*
- `uint16_t sparseBitLimit`  
*Sparse Bit Limit which defines the maximum number of consecutive samples that may be discarded before an error is generated.*
- `uint8_t retryCount`  
*Retry count.*
- `uint8_t longRunMaxLimit`  
*Largest allowable number of consecutive samples of all 1, or all 0, that is allowed during the Entropy generation.*
- `trng_statistical_check_limit_t monobitLimit`  
*Maximum and minimum limits for statistical check of number of ones/zero detected during entropy generation.*
- `trng_statistical_check_limit_t runBit1Limit`  
*Maximum and minimum limits for statistical check of number of runs of length 1 detected during entropy generation.*
- `trng_statistical_check_limit_t runBit2Limit`  
*Maximum and minimum limits for statistical check of number of runs of length 2 detected during entropy generation.*
- `trng_statistical_check_limit_t runBit3Limit`  
*Maximum and minimum limits for statistical check of number of runs of length 3 detected during entropy generation.*
- `trng_statistical_check_limit_t runBit4Limit`  
*Maximum and minimum limits for statistical check of number of runs of length 4 detected during entropy generation.*
- `trng_statistical_check_limit_t runBit5Limit`

*Maximum and minimum limits for statistical check of number of runs of length 5 detected during entropy generation.*

- [\*\*trng\\_statistical\\_check\\_limit\\_t runBit6PlusLimit\*\*](#)

*Maximum and minimum limits for statistical check of number of runs of length 6 or more detected during entropy generation.*

- [\*\*trng\\_statistical\\_check\\_limit\\_t pokerLimit\*\*](#)

*Maximum and minimum limits for statistical check of "Poker Test".*

- [\*\*trng\\_statistical\\_check\\_limit\\_t frequencyCountLimit\*\*](#)

*Maximum and minimum limits for statistical check of entropy sample frequency count.*

## Field Documentation

(1) **bool trng\_config\_t::lock**

(2) **trng\_clock\_mode\_t trng\_config\_t::clockMode**

(3) **trng\_ring\_osc\_div\_t trng\_config\_t::ringOscDiv**

(4) **trng\_sample\_mode\_t trng\_config\_t::sampleMode**

(5) **uint16\_t trng\_config\_t::entropyDelay**

Defines the length (in system clocks) of each Entropy sample taken.

(6) **uint16\_t trng\_config\_t::sampleSize**

Defines the total number of Entropy samples that will be taken during Entropy generation.

(7) **uint16\_t trng\_config\_t::sparseBitLimit**

This limit is used only for during von Neumann sampling (enabled by TRNG\_HAL\_SetSampleMode()). Samples are discarded if two consecutive raw samples are both 0 or both 1. If this discarding occurs for a long period of time, it indicates that there is insufficient Entropy.

(8) **uint8\_t trng\_config\_t::retryCount**

It defines the number of times a statistical check may fail during the TRNG Entropy Generation before generating an error.

- (9) `uint8_t trng_config_t::longRunMaxLimit`
- (10) `trng_statistical_check_limit_t trng_config_t::monobitLimit`
- (11) `trng_statistical_check_limit_t trng_config_t::runBit1Limit`
- (12) `trng_statistical_check_limit_t trng_config_t::runBit2Limit`
- (13) `trng_statistical_check_limit_t trng_config_t::runBit3Limit`
- (14) `trng_statistical_check_limit_t trng_config_t::runBit4Limit`
- (15) `trng_statistical_check_limit_t trng_config_t::runBit5Limit`
- (16) `trng_statistical_check_limit_t trng_config_t::runBit6PlusLimit`
- (17) `trng_statistical_check_limit_t trng_config_t::pokerLimit`
- (18) `trng_statistical_check_limit_t trng_config_t::frequencyCountLimit`

## 46.5 Macro Definition Documentation

### 46.5.1 #define FSL\_TRNG\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 16))

Current version: 2.0.16

Change log:

- version 2.0.16
  - Added support for Dual oscillator mode.
- version 2.0.15
  - Changed TRNG\_USER\_CONFIG\_DEFAULT\_XXX values according to latest recommended by design team.
- version 2.0.14
  - add support for RW610 and RW612
- version 2.0.13
  - After deepsleep it might return error, added clearing bits in [TRNG\\_GetRandomData\(\)](#) and generating new entropy.
  - Modified reloading entropy in [TRNG\\_GetRandomData\(\)](#), for some data length it doesn't reloading entropy correctly.
- version 2.0.12
  - For KW34A4\_SERIES, KW35A4\_SERIES, KW36A4\_SERIES set TRNG\_USER\_CONFIG\_DEFAULT\_OSC\_DIV to kTRNG\_RingOscDiv8.
- version 2.0.11
  - Add clearing pending errors in [TRNG\\_Init\(\)](#).
- version 2.0.10
  - Fixed doxygen issues.
- version 2.0.9
  - Fix HIS\_CCM metrics issues.

- version 2.0.8
  - For K32L2A41A\_SERIES set TRNG\_USER\_CONFIG\_DEFAULT\_OSC\_DIV to kTRNG\_RingOscDiv4.
- version 2.0.7
  - Fix MISRA 2004 issue rule 12.5.
- version 2.0.6
  - For KW35Z4\_SERIES set TRNG\_USER\_CONFIG\_DEFAULT\_OSC\_DIV to kTRNG\_RingOscDiv8.
- version 2.0.5
  - Add possibility to define default TRNG configuration by device specific preprocessor macros for FRQMIN, FRQMAX and OSCDIV.
- version 2.0.4
  - Fix MISRA-2012 issues.
- Version 2.0.3
  - update TRNG\_Init to restart entropy generation
- Version 2.0.2
  - fix MISRA issues
- Version 2.0.1
  - add support for KL8x and KL28Z
  - update default OSCDIV for K81 to divide by 2

## 46.6 Enumeration Type Documentation

### 46.6.1 enum trng\_sample\_mode\_t

Used by [trng\\_config\\_t](#).

Enumerator

***kTRNG\_SampleModeVonNeumann*** Use von Neumann data in both Entropy shifter and Statistical Checker.

***kTRNG\_SampleModeRaw*** Use raw data into both Entropy shifter and Statistical Checker.

***kTRNG\_SampleModeVonNeumannRaw*** Use von Neumann data in Entropy shifter. Use raw data into Statistical Checker.

### 46.6.2 enum trng\_clock\_mode\_t

Used by [trng\\_config\\_t](#).

Enumerator

***kTRNG\_ClockModeRingOscillator*** Ring oscillator is used to operate the TRNG (default).

***kTRNG\_ClockModeSystem*** System clock is used to operate the TRNG. This is for test use only, and indeterminate results may occur.

### 46.6.3 enum trng\_ring\_osc\_div\_t

Used by [trng\\_config\\_t](#).

Enumerator

- kTRNG\_RingOscDiv0*** Ring oscillator with no divide.
- kTRNG\_RingOscDiv2*** Ring oscillator divided-by-2.
- kTRNG\_RingOscDiv4*** Ring oscillator divided-by-4.
- kTRNG\_RingOscDiv8*** Ring oscillator divided-by-8.

## 46.7 Function Documentation

### 46.7.1 status\_t TRNG\_GetDefaultConfig ( [trng\\_config\\_t](#) \* *userConfig* )

This function initializes the configuration structure to default values. The default values are as follows.

```
*      userConfig->lock = 0;
*      userConfig->clockMode = kTRNG\_ClockModeRingOscillator;
*      userConfig->ringOscDiv = kTRNG\_RingOscDiv0; Or to other kTRNG_RingOscDiv[2|8]
*      depending on the platform.
*      userConfig->sampleMode = kTRNG\_SampleModeRaw;
*      userConfig->entropyDelay = 3200;
*      userConfig->sampleSize = 2500;
*      userConfig->sparseBitLimit = 63;
*      userConfig->retryCount = 1;
*      userConfig->longRunMaxLimit = 32;
*      userConfig->monobitLimit.maximum = 317;
*      userConfig->monobitLimit.minimum = 195;
*      userConfig->runBit1Limit.maximum = 107;
*      userConfig->runBit1Limit.minimum = 27;
*      userConfig->runBit2Limit.maximum = 62;
*      userConfig->runBit2Limit.minimum = 7;
*      userConfig->runBit3Limit.maximum = 39;
*      userConfig->runBit3Limit.minimum = 0;
*      userConfig->runBit4Limit.maximum = 26;
*      userConfig->runBit4Limit.minimum = 0;
*      userConfig->runBit5Limit.maximum = 18;
*      userConfig->runBit5Limit.minimum = 0;
*      userConfig->runBit6PlusLimit.maximum = 17;
*      userConfig->runBit6PlusLimit.minimum = 0;
*      userConfig->pokerLimit.maximum = 1600;
*      userConfig->pokerLimit.minimum = 1030;
*      userConfig->frequencyCountLimit.maximum = 30000;
*      userConfig->frequencyCountLimit.minimum = 1600;
*
```

Parameters

---

<i>userConfig</i>	User configuration structure.
-------------------	-------------------------------

Returns

If successful, returns the kStatus\_TRNG\_Success. Otherwise, it returns an error.

#### 46.7.2 status\_t TRNG\_Init ( TRNG\_Type \* *base*, const trng\_config\_t \* *userConfig* )

This function initializes the TRNG. When called, the TRNG entropy generation starts immediately.

Parameters

<i>base</i>	TRNG base address
<i>userConfig</i>	Pointer to the initialization configuration structure.

Returns

If successful, returns the kStatus\_TRNG\_Success. Otherwise, it returns an error.

#### 46.7.3 void TRNG\_Deinit ( TRNG\_Type \* *base* )

This function shuts down the TRNG.

Parameters

<i>base</i>	TRNG base address.
-------------	--------------------

#### 46.7.4 status\_t TRNG\_GetRandomData ( TRNG\_Type \* *base*, void \* *data*, size\_t *dataSize* )

This function gets random data from the TRNG.

Parameters

<i>base</i>	TRNG base address.
-------------	--------------------

<i>data</i>	Pointer address used to store random data.
<i>dataSize</i>	Size of the buffer pointed by the data parameter.

Returns

random data

# Chapter 47

## USDHC: Ultra Secured Digital Host Controller Driver

### 47.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Ultra Secured Digital Host Controller (USDHC) module of MCUXpresso SDK/i.MX devices.

### 47.2 Typical use case

#### 47.2.1 USDHC Operation

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/usdhc`.

#### Cache maintain capability

The uSDHC host controller is intergrated with ADMA to have better transfer performance, so to maintain data integrity during DMA operations on the platform that has cache, USDHC driver provide a cache maintain functionality by define: `FSL_SDK_ENABLE_DRIVER_CACHE_CONTROL = 1` It is suggest that the address of buffer used for read/write is align with cache line size.

#### Scatter gather transfer capability

The USDHC driver implement scatter gather transfer functionality, so application can submit uncontinuous data buffer in one transfer request by the scatter gather api, to have this feature, USDHC driver has below api `USDHC_TransferScatterGatherADMANonBlocking` This function suppprt scatter gather transfer and cover the functionality of `USDHC_TransferNonBlocking` also, but if application would like to use the function, please enable function macro firstly, since the scatter gather functionality is disabled by default.  
`#define FSL_USDHC_ENABLE_SCATTER_GATHER_TRANSFER 1`

Please note that once the macro is defined, the `USDHC_TransferNonBlocking` will be removed automatically.

### Data Structures

- struct `usdhc_adma2_descriptor_t`  
    *Defines the ADMA2 descriptor structure. [More...](#)*
- struct `usdhc_capability_t`  
    *USDHC capability information. [More...](#)*
- struct `usdhc_boot_config_t`  
    *Data structure to configure the MMC boot feature. [More...](#)*
- struct `usdhc_config_t`  
    *Data structure to initialize the USDHC. [More...](#)*
- struct `usdhc_command_t`  
    *Card command descriptor. [More...](#)*

- struct `usdhc_adma_config_t`  
*ADMA configuration.* [More...](#)
- struct `usdhc_scatter_gather_data_list_t`  
*Card scatter gather data list.* [More...](#)
- struct `usdhc_scatter_gather_data_t`  
*Card scatter gather data descriptor.* [More...](#)
- struct `usdhc_scatter_gather_transfer_t`  
*usdhc scatter gather transfer.* [More...](#)
- struct `usdhc_data_t`  
*Card data descriptor.* [More...](#)
- struct `usdhc_transfer_t`  
*Transfer state.* [More...](#)
- struct `usdhc_transfer_callback_t`  
*USDHC callback functions.* [More...](#)
- struct `usdhc_handle_t`  
*USDHC handle.* [More...](#)
- struct `usdhc_host_t`  
*USDHC host descriptor.* [More...](#)

## Macros

- #define `USDHC_MAX_BLOCK_COUNT` (`USDHC_BLK_ATT_BLKCNT_MASK >> USDHC_BLK_ATT_BLKCNT_SHIFT`)  
*Maximum block count can be set one time.*
- #define `FSL_USDHC_ENABLE_SCATTER_GATHER_TRANSFER_0U`  
*USDHC scatter gather feature control macro.*
- #define `USDHC_ADMA1_ADDRESS_ALIGN` (4096U)  
*The alignment size for ADDRESS filed in ADMA1's descriptor.*
- #define `USDHC_ADMA1_LENGTH_ALIGN` (4096U)  
*The alignment size for LENGTH field in ADMA1's descriptor.*
- #define `USDHC_ADMA2_ADDRESS_ALIGN` (4U)  
*The alignment size for ADDRESS field in ADMA2's descriptor.*
- #define `USDHC_ADMA2_LENGTH_ALIGN` (4U)  
*The alignment size for LENGTH filed in ADMA2's descriptor.*
- #define `USDHC_ADMA1_DESCRIPTOR_ADDRESS_SHIFT` (12U)  
*The bit shift for ADDRESS filed in ADMA1's descriptor.*
- #define `USDHC_ADMA1_DESCRIPTOR_ADDRESS_MASK` (0xFFFFFU)  
*The bit mask for ADDRESS field in ADMA1's descriptor.*
- #define `USDHC_ADMA1_DESCRIPTOR_LENGTH_SHIFT` (12U)  
*The bit shift for LENGTH filed in ADMA1's descriptor.*
- #define `USDHC_ADMA1_DESCRIPTOR_LENGTH_MASK` (0xFFFFU)  
*The mask for LENGTH field in ADMA1's descriptor.*
- #define `USDHC_ADMA1_DESCRIPTOR_MAX_LENGTH_PER_ENTRY` (`USDHC_ADMA1_DESCRIPTOR_LENGTH_MASK + 1U - 4096U`)  
*The maximum value of LENGTH filed in ADMA1's descriptor.*
- #define `USDHC_ADMA2_DESCRIPTOR_LENGTH_SHIFT` (16U)  
*The bit shift for LENGTH field in ADMA2's descriptor.*
- #define `USDHC_ADMA2_DESCRIPTOR_LENGTH_MASK` (0xFFFFU)  
*The bit mask for LENGTH field in ADMA2's descriptor.*
- #define `USDHC_ADMA2_DESCRIPTOR_MAX_LENGTH_PER_ENTRY` (`USDHC_ADMA2_DESCRIPTOR_LENGTH_MASK - 3U`)

*The maximum value of LENGTH field in ADMA2's descriptor.*

## Typedefs

- `typedef uint32_t usdhc_adma1_descriptor_t`  
*Defines the ADMA1 descriptor structure.*
- `typedef status_t(* usdhc_transfer_function_t )(USDHC_Type *base, usdhc_transfer_t *content)`  
*USDHC transfer function.*

## Enumerations

- `enum {`
  - `kStatus_USDHC_BusyTransferring = MAKE_STATUS(kStatusGroup_USDHC, 0U),`
  - `kStatus_USDHC_PrepareAdmaDescriptorFailed = MAKE_STATUS(kStatusGroup_USDHC, 1U),`
  - `kStatus_USDHC_SendCommandFailed = MAKE_STATUS(kStatusGroup_USDHC, 2U),`
  - `kStatus_USDHC_TransferDataFailed = MAKE_STATUS(kStatusGroup_USDHC, 3U),`
  - `kStatus_USDHC_DMADataAddrNotAlign = MAKE_STATUS(kStatusGroup_USDHC, 4U),`
  - `kStatus_USDHC_ReTuningRequest = MAKE_STATUS(kStatusGroup_USDHC, 5U),`
  - `kStatus_USDHC_TuningError = MAKE_STATUS(kStatusGroup_USDHC, 6U),`
  - `kStatus_USDHC_NotSupport = MAKE_STATUS(kStatusGroup_USDHC, 7U),`
  - `kStatus_USDHC_TransferDataComplete = MAKE_STATUS(kStatusGroup_USDHC, 8U),`
  - `kStatus_USDHC_SendCommandSuccess = MAKE_STATUS(kStatusGroup_USDHC, 9U),`
  - `kStatus_USDHC_TransferDMAComplete = MAKE_STATUS(kStatusGroup_USDHC, 10U) }`

*Enum \_usdhc\_status.*
- `enum {`
  - `kUSDHC_SupportAdmaFlag = USDHC_HOST_CTRL_CAP_ADMAS_MASK,`
  - `kUSDHC_SupportHighSpeedFlag = USDHC_HOST_CTRL_CAP_HSS_MASK,`
  - `kUSDHC_SupportDmaFlag = USDHC_HOST_CTRL_CAP_DMAS_MASK,`
  - `kUSDHC_SupportSuspendResumeFlag = USDHC_HOST_CTRL_CAP_SRS_MASK,`
  - `kUSDHC_SupportV330Flag = USDHC_HOST_CTRL_CAP_VS33_MASK,`
  - `kUSDHC_SupportV300Flag = USDHC_HOST_CTRL_CAP_VS30_MASK,`
  - `kUSDHC_SupportV180Flag = USDHC_HOST_CTRL_CAP_VS18_MASK,`
  - `kUSDHC_Support4BitFlag = (USDHC_HOST_CTRL_CAP_MBL_SHIFT << 0U),`
  - `kUSDHC_Support8BitFlag = (USDHC_HOST_CTRL_CAP_MBL_SHIFT << 1U),`
  - `kUSDHC_SupportDDR50Flag = USDHC_HOST_CTRL_CAP_DDR50_SUPPORT_MASK,`
  - `kUSDHC_SupportSDR104Flag = USDHC_HOST_CTRL_CAP_SDR104_SUPPORT_MASK,`
  - `kUSDHC_SupportSDR50Flag = USDHC_HOST_CTRL_CAP_SDR50_SUPPORT_MASK }`

*Enum \_usdhc\_capability\_flag.*
- `enum {`
  - `kUSDHC_WakeupEventOnCardInt = USDHC_PROT_CTRL_WECINT_MASK,`
  - `kUSDHC_WakeupEventOnCardInsert = USDHC_PROT_CTRL_WECINS_MASK,`
  - `kUSDHC_WakeupEventOnCardRemove = USDHC_PROT_CTRL_WECRM_MASK,`
  - `kUSDHC_WakeupEventsAll }`

*Enum \_usdhc\_wakeup\_event.*
- `enum {`

```

kUSDHC_ResetAll = USDHC_SYS_CTRL_RSTA_MASK,
kUSDHC_ResetCommand = USDHC_SYS_CTRL_RSTC_MASK,
kUSDHC_ResetData = USDHC_SYS_CTRL_RSTD_MASK,
kUSDHC_ResetTuning = USDHC_SYS_CTRL_RSTT_MASK,
kUSDHC_ResetsAll = (kUSDHC_ResetAll | kUSDHC_ResetCommand | kUSDHC_ResetData |
kUSDHC_ResetTuning) }

Enum usdhc_reset.
• enum {
    kUSDHC_EnableDmaFlag = USDHC_MIX_CTRL_DMAEN_MASK,
    kUSDHC_CommandTypeSuspendFlag = USDHC_CMD_XFR_TYP_CMDTYP(1U),
    kUSDHC_CommandTypeResumeFlag = USDHC_CMD_XFR_TYP_CMDTYP(2U),
    kUSDHC_CommandTypeAbortFlag = USDHC_CMD_XFR_TYP_CMDTYP(3U),
    kUSDHC_EnableBlockCountFlag = USDHC_MIX_CTRL_BCEN_MASK,
    kUSDHC_EnableAutoCommand12Flag = USDHC_MIX_CTRL_AC12EN_MASK,
    kUSDHC_DataReadFlag = USDHC_MIX_CTRL_DTDSEL_MASK,
    kUSDHC_MultipleBlockFlag = USDHC_MIX_CTRL_MSBSEL_MASK,
    kUSDHC_EnableAutoCommand23Flag = USDHC_MIX_CTRL_AC23EN_MASK,
    kUSDHC_ResponseLength136Flag = USDHC_CMD_XFR_TYP_RSPTYP(1U),
    kUSDHC_ResponseLength48Flag = USDHC_CMD_XFR_TYP_RSPTYP(2U),
    kUSDHC_ResponseLength48BusyFlag = USDHC_CMD_XFR_TYP_RSPTYP(3U),
    kUSDHC_EnableCrcCheckFlag = USDHC_CMD_XFR_TYP_CCCEN_MASK,
    kUSDHC_EnableIndexCheckFlag = USDHC_CMD_XFR_TYP_CICEN_MASK,
    kUSDHC_DataPresentFlag = USDHC_CMD_XFR_TYP_DPSEL_MASK }

Enum usdhc_transfer_flag.
• enum {
    kUSDHC_CommandInhibitFlag = USDHC_PRES_STATE_CIHB_MASK,
    kUSDHC_DataInhibitFlag = USDHC_PRES_STATE_CDIHB_MASK,
    kUSDHC_DataLineActiveFlag = USDHC_PRES_STATE_DLAI_MASK,
    kUSDHC_SdClockStableFlag = USDHC_PRES_STATE_SDSTB_MASK,
    kUSDHC_WriteTransferActiveFlag = USDHC_PRES_STATE_WTA_MASK,
    kUSDHC_ReadTransferActiveFlag = USDHC_PRES_STATE_RTA_MASK,
    kUSDHC_BufferWriteEnableFlag = USDHC_PRES_STATE_BWEN_MASK,
    kUSDHC_BufferReadEnableFlag = USDHC_PRES_STATE_BREN_MASK,
    kUSDHC_ReTuningRequestFlag = USDHC_PRES_STATE_RTR_MASK,
    kUSDHC_DelaySettingFinishedFlag = USDHC_PRES_STATE_TSCD_MASK,
    kUSDHC_CardInsertedFlag = USDHC_PRES_STATE_CINST_MASK,
    kUSDHC_CommandLineLevelFlag = USDHC_PRES_STATE_CLSL_MASK,
    kUSDHC_Data0LineLevelFlag = 1U << USDHC_PRES_STATE_DLSL_SHIFT,
    kUSDHC_Data1LineLevelFlag = 1U << (USDHC_PRES_STATE_DLSL_SHIFT + 1U),
    kUSDHC_Data2LineLevelFlag = 1U << (USDHC_PRES_STATE_DLSL_SHIFT + 2U),
    kUSDHC_Data3LineLevelFlag = 1U << (USDHC_PRES_STATE_DLSL_SHIFT + 3U),
    kUSDHC_Data4LineLevelFlag = 1U << (USDHC_PRES_STATE_DLSL_SHIFT + 4U),
    kUSDHC_Data5LineLevelFlag = 1U << (USDHC_PRES_STATE_DLSL_SHIFT + 5U),
    kUSDHC_Data6LineLevelFlag = 1U << (USDHC_PRES_STATE_DLSL_SHIFT + 6U),
    kUSDHC_Data7LineLevelFlag = (int)(1U << (USDHC_PRES_STATE_DLSL_SHIFT + 7U)) }

```

- *Enum \_usdhc\_present\_status\_flag.*
- enum {
   
kUSDHC\_CommandCompleteFlag = USDHC\_INT\_STATUS\_CC\_MASK,  
 kUSDHC\_DataCompleteFlag = USDHC\_INT\_STATUS\_TC\_MASK,  
 kUSDHC\_BlockGapEventFlag = USDHC\_INT\_STATUS\_BGE\_MASK,  
 kUSDHC\_DmaCompleteFlag = USDHC\_INT\_STATUS\_DINT\_MASK,  
 kUSDHC\_BufferWriteReadyFlag = USDHC\_INT\_STATUS\_BWR\_MASK,  
 kUSDHC\_BufferReadReadyFlag = USDHC\_INT\_STATUS\_BRR\_MASK,  
 kUSDHC\_CardInsertionFlag = USDHC\_INT\_STATUS\_CINS\_MASK,  
 kUSDHC\_CardRemovalFlag = USDHC\_INT\_STATUS\_CRM\_MASK,  
 kUSDHC\_CardInterruptFlag = USDHC\_INT\_STATUS\_CINT\_MASK,  
 kUSDHC\_ReTuningEventFlag = USDHC\_INT\_STATUS RTE\_MASK,  
 kUSDHC\_TuningPassFlag = USDHC\_INT\_STATUS\_TP\_MASK,  
 kUSDHC\_TuningErrorFlag = USDHC\_INT\_STATUS\_TNE\_MASK,  
 kUSDHC\_CommandTimeoutFlag = USDHC\_INT\_STATUS\_CTOE\_MASK,  
 kUSDHC\_CommandCrcErrorFlag = USDHC\_INT\_STATUS\_CCE\_MASK,  
 kUSDHC\_CommandEndBitErrorFlag = USDHC\_INT\_STATUS\_CEBE\_MASK,  
 kUSDHC\_CommandIndexErrorFlag = USDHC\_INT\_STATUS\_CIE\_MASK,  
 kUSDHC\_DataTimeoutFlag = USDHC\_INT\_STATUS\_DTOE\_MASK,  
 kUSDHC\_DataCrcErrorFlag = USDHC\_INT\_STATUS\_DCE\_MASK,  
 kUSDHC\_DataEndBitErrorFlag = USDHC\_INT\_STATUS\_DEBE\_MASK,  
 kUSDHC\_AutoCommand12ErrorFlag = USDHC\_INT\_STATUS\_AC12E\_MASK,  
 kUSDHC\_DmaErrorFlag = USDHC\_INT\_STATUS\_DMAE\_MASK,  
 kUSDHC\_CommandErrorFlag,  
 kUSDHC\_DataErrorFlag,  
 kUSDHC\_ErrorFlag = (kUSDHC\_CommandErrorFlag | kUSDHC\_DataErrorFlag | kUSDHC\_DmaErrorFlag),  
 kUSDHC\_DataFlag,  
 kUSDHC\_DataDMAFlag = (kUSDHC\_DataCompleteFlag | kUSDHC\_DataErrorFlag | kUSDHC\_DmaErrorFlag),  
 kUSDHC\_CommandFlag = (kUSDHC\_CommandErrorFlag | kUSDHC\_CommandCompleteFlag),  
 kUSDHC\_CardDetectFlag = (kUSDHC\_CardInsertionFlag | kUSDHC\_CardRemovalFlag),  
 kUSDHC\_SDR104TuningFlag = (kUSDHC\_TuningErrorFlag | kUSDHC\_TuningPassFlag | kUSDHC\_ReTuningEventFlag),  
 kUSDHC\_AllInterruptFlags }
- *Enum \_usdhc\_interrupt\_status\_flag.*
- enum {
   
kUSDHC\_AutoCommand12NotExecutedFlag = USDHC\_AUTOCMD12\_ERR\_STATUS\_AC12NE\_MASK,  
 kUSDHC\_AutoCommand12TimeoutFlag = USDHC\_AUTOCMD12\_ERR\_STATUS\_AC12TOE\_MASK,  
 kUSDHC\_AutoCommand12EndBitErrorFlag = USDHC\_AUTOCMD12\_ERR\_STATUS\_AC12EBE\_MASK,  
 kUSDHC\_AutoCommand12CrcErrorFlag = USDHC\_AUTOCMD12\_ERR\_STATUS\_AC12CE\_

```

MASK,
kUSDHC_AutoCommand12IndexErrorFlag = USDHC_AUTOCMD12_ERR_STATUS_AC12IE-
_MASK,
kUSDHC_AutoCommand12NotIssuedFlag = USDHC_AUTOCMD12_ERR_STATUS_CNIBA-
C12E_MASK }

Enum_usdhc_auto_command12_error_status_flag.
• enum {
  kUSDHC_ExecuteTuning = USDHC_AUTOCMD12_ERR_STATUS_EXECUTE_TUNING_M-
ASK,
  kUSDHC_TuningSampleClockSel }

Enum_usdhc_standard_tuning.
• enum {
  kUSDHC_AdmaLengMismatchFlag = USDHC_ADMA_ERR_STATUSADMALME_MASK,
  kUSDHC_AdmaDescriptorErrorFlag = USDHC_ADMA_ERR_STATUSADMADCE_MASK }

Enum_usdhc_adma_error_status_flag.
• enum {
  kUSDHC_AdmaErrorStateStopDma = 0x00U,
  kUSDHC_AdmaErrorStateFetchDescriptor = 0x01U,
  kUSDHC_AdmaErrorStateChangeAddress = 0x02U,
  kUSDHC_AdmaErrorStateTransferData = 0x03U,
  kUSDHC_AdmaErrorStateInvalidLength = 0x04U,
  kUSDHC_AdmaErrorStateInvalidDescriptor = 0x08U,
  kUSDHC_AdmaErrorState }

Enum_usdhc_adma_error_state.
• enum {
  kUSDHC_ForceEventAutoCommand12NotExecuted,
  kUSDHC_ForceEventAutoCommand12Timeout = USDHC_FORCE_EVENT_FEVTAC12TOE-
MASK,
  kUSDHC_ForceEventAutoCommand12CrcError = USDHC_FORCE_EVENT_FEVTAC12CE-
MASK,
  kUSDHC_ForceEventEndBitError = USDHC_FORCE_EVENT_FEVTAC12EBE_MASK,
  kUSDHC_ForceEventAutoCommand12IndexError = USDHC_FORCE_EVENT_FEVTAC12IE-
MASK,
  kUSDHC_ForceEventAutoCommand12NotIssued = USDHC_FORCE_EVENT_FEVTCNIBA-
C12E_MASK,
  kUSDHC_ForceEventCommandTimeout = USDHC_FORCE_EVENT_FEVTCTOE_MASK,
  kUSDHC_ForceEventCommandCrcError = USDHC_FORCE_EVENT_FEVTCCE_MASK,
  kUSDHC_ForceEventCommandEndBitError = USDHC_FORCE_EVENT_FEVTCCEBE_MASK,
  kUSDHC_ForceEventCommandIndexError = USDHC_FORCE_EVENT_FEVTCIE_MASK,
  kUSDHC_ForceEventDataTimeout = USDHC_FORCE_EVENT_FEVTDTOE_MASK,
  kUSDHC_ForceEventDataCrcError = USDHC_FORCE_EVENT_FEVTDCE_MASK,
  kUSDHC_ForceEventDataEndBitError = USDHC_FORCE_EVENT_FEVTDEBE_MASK,
  kUSDHC_ForceEventAutoCommand12Error = USDHC_FORCE_EVENT_FEVTAC12E_MAS-
}

```

- K,
- `kUSDHC_ForceEventCardInt` = (int)USDHC\_FORCE\_EVENT\_FEVTCINT\_MASK,
  - `kUSDHC_ForceEventDmaError` = USDHC\_FORCE\_EVENT\_FEVTDMAE\_MASK,
  - `kUSDHC_ForceEventTuningError` = USDHC\_FORCE\_EVENT\_FEVTTNE\_MASK,
  - `kUSDHC_ForceEventsAll` }
- Enum usdhc\_force\_event.*
- enum `usdhc_transfer_direction_t` {
    - `kUSDHC_TransferDirectionReceive` = 1U,
    - `kUSDHC_TransferDirectionSend` = 0U }
- Data transfer direction.*
- enum `usdhc_data_bus_width_t` {
    - `kUSDHC_DataBusWidth1Bit` = 0U,
    - `kUSDHC_DataBusWidth4Bit` = 1U,
    - `kUSDHC_DataBusWidth8Bit` = 2U }
- Data transfer width.*
- enum `usdhc_endian_mode_t` {
    - `kUSDHC_EndianModeBig` = 0U,
    - `kUSDHC_EndianModeHalfWordBig` = 1U,
    - `kUSDHC_EndianModeLittle` = 2U }
- Endian mode.*
- enum `usdhc_dma_mode_t` {
    - `kUSDHC_DmaModeSimple` = 0U,
    - `kUSDHC_DmaModeAdma1` = 1U,
    - `kUSDHC_DmaModeAdma2` = 2U,
    - `kUSDHC_ExternalDMA` = 3U }
- DMA mode.*
- enum {
    - `kUSDHC_StopAtBlockGapFlag` = USDHC\_PROT\_CTRL\_SABGREQ\_MASK,
    - `kUSDHC_ReadWaitControlFlag` = USDHC\_PROT\_CTRL\_RWCTL\_MASK,
    - `kUSDHC InterruptAtBlockGapFlag` = USDHC\_PROT\_CTRL\_IABG\_MASK,
    - `kUSDHC_ReadDoneNo8CLK` = USDHC\_PROT\_CTRL\_RD\_DONE\_NO\_8CLK\_MASK,
    - `kUSDHC_ExactBlockNumberReadFlag` = USDHC\_PROT\_CTRL\_NON\_EXACT\_BLK\_RD\_M-ASK }
- Enum usdhc\_sdio\_control\_flag.*
- enum `usdhc_boot_mode_t` {
    - `kUSDHC_BootModeNormal` = 0U,
    - `kUSDHC_BootModeAlternative` = 1U }
- MMC card boot mode.*
- enum `usdhc_card_command_type_t` {
    - `kCARD_CommandTypeNormal` = 0U,
    - `kCARD_CommandTypeSuspend` = 1U,
    - `kCARD_CommandTypeResume` = 2U,
    - `kCARD_CommandTypeAbort` = 3U,
    - `kCARD_CommandTypeEmpty` = 4U }
- The command type.*
- enum `usdhc_card_response_type_t` {

```
kCARD_ResponseNone = 0U,
kCARD_ResponseTypeR1 = 1U,
kCARD_ResponseTypeR1b = 2U,
kCARD_ResponseTypeR2 = 3U,
kCARD_ResponseTypeR3 = 4U,
kCARD_ResponseTypeR4 = 5U,
kCARD_ResponseTypeR5 = 6U,
kCARD_ResponseTypeR5b = 7U,
kCARD_ResponseTypeR6 = 8U,
kCARD_ResponseTypeR7 = 9U }
```

*The command response type.*

- enum {
 

```
kUSDHC_Adma1DescriptorValidFlag = (1U << 0U),
kUSDHC_Adma1DescriptorEndFlag = (1U << 1U),
kUSDHC_Adma1DescriptorInterruptFlag = (1U << 2U),
kUSDHC_Adma1DescriptorActivity1Flag = (1U << 4U),
kUSDHC_Adma1DescriptorActivity2Flag = (1U << 5U),
kUSDHC_Adma1DescriptorTypeNop = (kUSDHC_Adma1DescriptorValidFlag),
kUSDHC_Adma1DescriptorTypeTransfer = (kUSDHC_Adma1DescriptorActivity2Flag | kUSDHC_Adma1DescriptorValidFlag),
kUSDHC_Adma1DescriptorTypeLink,
kUSDHC_Adma1DescriptorTypeSetLength = (kUSDHC_Adma1DescriptorActivity1Flag | kUSDHC_Adma1DescriptorValidFlag) }
```

*Enum\_usdhc\_adma1\_descriptor\_flag.*

- enum {
 

```
kUSDHC_Adma2DescriptorValidFlag = (1U << 0U),
kUSDHC_Adma2DescriptorEndFlag = (1U << 1U),
kUSDHC_Adma2DescriptorInterruptFlag = (1U << 2U),
kUSDHC_Adma2DescriptorActivity1Flag = (1U << 4U),
kUSDHC_Adma2DescriptorActivity2Flag = (1U << 5U),
kUSDHC_Adma2DescriptorTypeNop = (kUSDHC_Adma2DescriptorValidFlag),
kUSDHC_Adma2DescriptorTypeReserved = (kUSDHC_Adma2DescriptorActivity1Flag | kUSDHC_Adma2DescriptorValidFlag),
kUSDHC_Adma2DescriptorTypeTransfer = (kUSDHC_Adma2DescriptorActivity2Flag | kUSDHC_Adma2DescriptorValidFlag),
kUSDHC_Adma2DescriptorTypeLink }
```

*Enum\_usdhc\_adma2\_descriptor\_flag.*

- enum {
 

```
kUSDHC_AdmaDescriptorSingleFlag = 0U,
kUSDHC_AdmaDescriptorMultipleFlag }
```

*Enum\_usdhc\_adma\_flag.*

- enum usdhc\_burst\_len\_t {
 

```
kUSDHC_EnBurstLenForINCR = 0x01U,
kUSDHC_EnBurstLenForINCR4816 = 0x02U,
kUSDHC_EnBurstLenForINCR4816WRAP = 0x04U }
```

*DMA transfer burst len config.*

- enum {
   
    kUSDHC\_TransferDataNormal = 0U,  
 kUSDHC\_TransferDataTuning = 1U,  
 kUSDHC\_TransferDataBoot = 2U,  
 kUSDHC\_TransferDataBootcontinuous = 3U }
- Enum usdhc\_transfer\_data\_type.*

## Driver version

- #define **FSL\_USDHC\_DRIVER\_VERSION** (**MAKE\_VERSION**(2U, 8U, 2U))  
*Driver version 2.8.2.*

## Initialization and deinitialization

- void **USDHC\_Init** (USDHC\_Type \*base, const **usdhc\_config\_t** \*config)  
*USDHC module initialization function.*
- void **USDHC\_Deinit** (USDHC\_Type \*base)  
*Deinitializes the USDHC.*
- bool **USDHC\_Reset** (USDHC\_Type \*base, uint32\_t mask, uint32\_t timeout)  
*Resets the USDHC.*

## DMA Control

- status\_t **USDHC\_SetAdmaTableConfig** (USDHC\_Type \*base, **usdhc\_adma\_config\_t** \*dmaConfig, **usdhc\_data\_t** \*dataConfig, uint32\_t flags)  
*Sets the DMA descriptor table configuration.*
- status\_t **USDHC\_SetInternalDmaConfig** (USDHC\_Type \*base, **usdhc\_adma\_config\_t** \*dmaConfig, const uint32\_t \*dataAddr, bool enAutoCmd23)  
*Internal DMA configuration.*
- status\_t **USDHC\_SetADMA2Descriptor** (uint32\_t \*admaTable, uint32\_t admaTableWords, const uint32\_t \*dataBufferAddr, uint32\_t dataBytes, uint32\_t flags)  
*Sets the ADMA2 descriptor table configuration.*
- status\_t **USDHC\_SetADMA1Descriptor** (uint32\_t \*admaTable, uint32\_t admaTableWords, const uint32\_t \*dataBufferAddr, uint32\_t dataBytes, uint32\_t flags)  
*Sets the ADMA1 descriptor table configuration.*
- static void **USDHC\_EnableInternalDMA** (USDHC\_Type \*base, bool enable)  
*Enables internal DMA.*

## Interrupts

- static void **USDHC\_EnableInterruptStatus** (USDHC\_Type \*base, uint32\_t mask)  
*Enables the interrupt status.*
- static void **USDHC\_DisableInterruptStatus** (USDHC\_Type \*base, uint32\_t mask)  
*Disables the interrupt status.*
- static void **USDHC\_EnableInterruptSignal** (USDHC\_Type \*base, uint32\_t mask)  
*Enables the interrupt signal corresponding to the interrupt status flag.*
- static void **USDHC\_DisableInterruptSignal** (USDHC\_Type \*base, uint32\_t mask)  
*Disables the interrupt signal corresponding to the interrupt status flag.*

## Status

- static uint32\_t **USDHC\_GetEnabledInterruptStatusFlags** (USDHC\_Type \*base)  
*Gets the enabled interrupt status.*
- static uint32\_t **USDHC\_GetInterruptStatusFlags** (USDHC\_Type \*base)  
*Gets the current interrupt status.*
- static void **USDHC\_ClearInterruptStatusFlags** (USDHC\_Type \*base, uint32\_t mask)  
*Clears a specified interrupt status.*
- static uint32\_t **USDHC\_GetAutoCommand12ErrorStatusFlags** (USDHC\_Type \*base)  
*Gets the status of auto command 12 error.*
- static uint32\_t **USDHC\_GetAdmaErrorStatusFlags** (USDHC\_Type \*base)  
*Gets the status of the ADMA error.*
- static uint32\_t **USDHC\_GetPresentStatusFlags** (USDHC\_Type \*base)  
*Gets a present status.*

## Bus Operations

- void **USDHC\_GetCapability** (USDHC\_Type \*base, usdhc\_capability\_t \*capability)  
*Gets the capability information.*
- static void **USDHC\_ForceClockOn** (USDHC\_Type \*base, bool enable)  
*Forces the card clock on.*
- uint32\_t **USDHC\_SetSdClock** (USDHC\_Type \*base, uint32\_t srcClock\_Hz, uint32\_t busClock\_Hz)  
*Sets the SD bus clock frequency.*
- bool **USDHC\_SetCardActive** (USDHC\_Type \*base, uint32\_t timeout)  
*Sends 80 clocks to the card to set it to the active state.*
- static void **USDHC\_AssertHardwareReset** (USDHC\_Type \*base, bool high)  
*Triggers a hardware reset.*
- static void **USDHC\_SetDataBusWidth** (USDHC\_Type \*base, usdhc\_data\_bus\_width\_t width)  
*Sets the data transfer width.*
- static void **USDHC\_WriteData** (USDHC\_Type \*base, uint32\_t data)  
*Fills the data port.*
- static uint32\_t **USDHC\_ReadData** (USDHC\_Type \*base)  
*Retrieves the data from the data port.*
- void **USDHC\_SendCommand** (USDHC\_Type \*base, usdhc\_command\_t \*command)  
*Sends command function.*
- static void **USDHC\_EnableWakeupEvent** (USDHC\_Type \*base, uint32\_t mask, bool enable)  
*Enables or disables a wakeup event in low-power mode.*
- static void **USDHC\_CardDetectByData3** (USDHC\_Type \*base, bool enable)  
*Detects card insert status.*
- static bool **USDHC\_DetectCardInsert** (USDHC\_Type \*base)  
*Detects card insert status.*
- static void **USDHC\_EnableSdioControl** (USDHC\_Type \*base, uint32\_t mask, bool enable)  
*Enables or disables the SDIO card control.*
- static void **USDHC\_SetContinueRequest** (USDHC\_Type \*base)  
*Restarts a transaction which has stopped at the block GAP for the SDIO card.*
- static void **USDHC\_RequestStopAtBlockGap** (USDHC\_Type \*base, bool enable)  
*Request stop at block gap function.*
- void **USDHC\_SetMmcBootConfig** (USDHC\_Type \*base, const usdhc\_boot\_config\_t \*config)  
*Configures the MMC boot feature.*
- static void **USDHC\_EnableMmcBoot** (USDHC\_Type \*base, bool enable)  
*Enables or disables the mmc boot mode.*

- static void **USDHC\_SetForceEvent** (USDHC\_Type \*base, uint32\_t mask)
 

*Forces generating events according to the given mask.*
- static void **USDHC\_SelectVoltage** (USDHC\_Type \*base, bool en18v)
 

*Selects the USDHC output voltage.*
- static bool **USDHC\_RequestTuningForSDR50** (USDHC\_Type \*base)
 

*Checks the SDR50 mode request tuning bit.*
- static bool **USDHC\_RequestReTuning** (USDHC\_Type \*base)
 

*Checks the request re-tuning bit.*
- static void **USDHC\_EnableAutoTuning** (USDHC\_Type \*base, bool enable)
 

*The SDR104 mode auto tuning enable and disable.*
- void **USDHC\_EnableAutoTuningForCmdAndData** (USDHC\_Type \*base)
 

*The auto tuning enable for CMD/DATA line.*
- void **USDHC\_EnableManualTuning** (USDHC\_Type \*base, bool enable)
 

*Manual tuning trigger or abort.*
- static uint32\_t **USDHC\_GetTuningDelayStatus** (USDHC\_Type \*base)
 

*Get the tuning delay cell setting.*
- status\_t **USDHC\_SetTuningDelay** (USDHC\_Type \*base, uint32\_t preDelay, uint32\_t outDelay, uint32\_t postDelay)
 

*The tuning delay cell setting.*
- status\_t **USDHC\_AdjustDelayForManualTuning** (USDHC\_Type \*base, uint32\_t delay)
 

*Adjusts delay for manual tuning.*
- static void **USDHC\_SetStandardTuningCounter** (USDHC\_Type \*base, uint8\_t counter)
 

*set tuning counter tuning.*
- void **USDHC\_EnableStandardTuning** (USDHC\_Type \*base, uint32\_t tuningStartTap, uint32\_t step, bool enable)
 

*The enable standard tuning function.*
- static uint32\_t **USDHC\_GetExecuteStdTuningStatus** (USDHC\_Type \*base)
 

*Gets execute STD tuning status.*
- static uint32\_t **USDHC\_CheckStdTuningResult** (USDHC\_Type \*base)
 

*Checks STD tuning result.*
- static uint32\_t **USDHC\_CheckTuningError** (USDHC\_Type \*base)
 

*Checks tuning error.*
- void **USDHC\_EnableDDRMode** (USDHC\_Type \*base, bool enable, uint32\_t nibblePos)
 

*The enable/disable DDR mode.*
- void **USDHC\_SetDataConfig** (USDHC\_Type \*base, usdhc\_transfer\_direction\_t dataDirection, uint32\_t blockCount, uint32\_t blockSize)
 

*USDHC data configuration.*

## Transactional functions

- void **USDHC\_TransferCreateHandle** (USDHC\_Type \*base, usdhc\_handle\_t \*handle, const usdhc\_transfer\_callback\_t \*callback, void \*userData)
 

*Creates the USDHC handle.*
- status\_t **USDHC\_TransferNonBlocking** (USDHC\_Type \*base, usdhc\_handle\_t \*handle, usdhc\_adma\_config\_t \*dmaConfig, usdhc\_transfer\_t \*transfer)
 

*Transfers the command/data using an interrupt and an asynchronous method.*
- status\_t **USDHC\_TransferBlocking** (USDHC\_Type \*base, usdhc\_adma\_config\_t \*dmaConfig, usdhc\_transfer\_t \*transfer)
 

*Transfers the command/data using a blocking method.*
- void **USDHC\_TransferHandleIRQ** (USDHC\_Type \*base, usdhc\_handle\_t \*handle)

*IRQ handler for the USDHC.*

## 47.3 Data Structure Documentation

### 47.3.1 struct usdhc\_adma2\_descriptor\_t

#### Data Fields

- `uint32_t attribute`  
*The control and status field.*
- `const uint32_t * address`  
*The address field.*

#### Field Documentation

- (1) `uint32_t usdhc_adma2_descriptor_t::attribute`
- (2) `const uint32_t* usdhc_adma2_descriptor_t::address`

### 47.3.2 struct usdhc\_capability\_t

Defines a structure to save the capability information of USDHC.

#### Data Fields

- `uint32_t sdVersion`  
*Support SD card/sdio version.*
- `uint32_t mmcVersion`  
*Support EMMC card version.*
- `uint32_t maxBlockLength`  
*Maximum block length unitized as byte.*
- `uint32_t maxBlockCount`  
*Maximum block count can be set one time.*
- `uint32_t flags`  
*Capability flags to indicate the support information([\\_usdhc\\_capability\\_flag](#)).*

**Field Documentation**

- (1) `uint32_t usdhc_capability_t::sdVersion`
- (2) `uint32_t usdhc_capability_t::mmcVersion`
- (3) `uint32_t usdhc_capability_t::maxBlockLength`
- (4) `uint32_t usdhc_capability_t::maxBlockCount`
- (5) `uint32_t usdhc_capability_t::flags`

**47.3.3 struct usdhc\_boot\_config\_t****Data Fields**

- `uint32_t ackTimeoutCount`  
*Timeout value for the boot ACK.*
- `usdhc_boot_mode_t bootMode`  
*Boot mode selection.*
- `uint32_t blockCount`  
*Stop at block gap value of automatic mode.*
- `size_t blockSize`  
*Block size.*
- `bool enableBootAck`  
*Enable or disable boot ACK.*
- `bool enableAutoStopAtBlockGap`  
*Enable or disable auto stop at block gap function in boot period.*

**Field Documentation**

- (1) `uint32_t usdhc_boot_config_t::ackTimeoutCount`

The available range is 0 ~ 15.

- (2) `usdhc_boot_mode_t usdhc_boot_config_t::bootMode`

- (3) `uint32_t usdhc_boot_config_t::blockCount`

Available range is 0 ~ 65535.

- (4) `size_t usdhc_boot_config_t::blockSize`
- (5) `bool usdhc_boot_config_t::enableBootAck`
- (6) `bool usdhc_boot_config_t::enableAutoStopAtBlockGap`

#### 47.3.4 struct usdhc\_config\_t

##### Data Fields

- `uint32_t dataTimeout`  
*Data timeout value.*
- `usdhc_endian_mode_t endianMode`  
*Endian mode.*
- `uint8_t readWatermarkLevel`  
*Watermark level for DMA read operation.*
- `uint8_t writeWatermarkLevel`  
*Watermark level for DMA write operation.*
- `uint8_t readBurstLen`  
*Read burst len.*
- `uint8_t writeBurstLen`  
*Write burst len.*

##### Field Documentation

- (1) `uint32_t usdhc_config_t::dataTimeout`
- (2) `usdhc_endian_mode_t usdhc_config_t::endianMode`
- (3) `uint8_t usdhc_config_t::readWatermarkLevel`

Available range is 1 ~ 128.

- (4) `uint8_t usdhc_config_t::writeWatermarkLevel`

Available range is 1 ~ 128.

- (5) `uint8_t usdhc_config_t::readBurstLen`
- (6) `uint8_t usdhc_config_t::writeBurstLen`

#### 47.3.5 struct usdhc\_command\_t

Defines card command-related attribute.

##### Data Fields

- `uint32_t index`

- *Command index.*
- `uint32_t argument`  
*Command argument.*
- `usdhc_card_command_type_t type`  
*Command type.*
- `usdhc_card_response_type_t responseType`  
*Command response type.*
- `uint32_t response [4U]`  
*Response for this command.*
- `uint32_t responseErrorFlags`  
*Response error flag, which need to check the command reponse.*
- `uint32_t flags`  
*Cmd flags.*

## Field Documentation

- (1) `uint32_t usdhc_command_t::index`
- (2) `uint32_t usdhc_command_t::argument`
- (3) `usdhc_card_command_type_t usdhc_command_t::type`
- (4) `usdhc_card_response_type_t usdhc_command_t::responseType`
- (5) `uint32_t usdhc_command_t::response[4U]`
- (6) `uint32_t usdhc_command_t::responseErrorFlags`
- (7) `uint32_t usdhc_command_t::flags`

## 47.3.6 struct usdhc\_adma\_config\_t

### Data Fields

- `usdhc_dma_mode_t dmaMode`  
*DMA mode.*
- `usdhc_burst_len_t burstLen`  
*Burst len config.*
- `uint32_t * admaTable`  
*ADMA table address, can't be null if transfer way is ADMA1/ADMA2.*
- `uint32_t admaTableWords`  
*ADMA table length united as words, can't be 0 if transfer way is ADMA1/ADMA2.*

**Field Documentation**

- (1) `usdhc_dma_mode_t usdhc_adma_config_t::dmaMode`
- (2) `usdhc_burst_len_t usdhc_adma_config_t::burstLen`
- (3) `uint32_t* usdhc_adma_config_t::admaTable`
- (4) `uint32_t usdhc_adma_config_t::admaTableWords`

**47.3.7 struct usdhc\_scatter\_gather\_data\_list\_t**

Allow application register uncontinuous data buffer for data transfer.

**47.3.8 struct usdhc\_scatter\_gather\_data\_t**

Defines a structure to contain data-related attribute. The 'enableIgnoreError' is used when upper card driver wants to ignore the error event to read/write all the data and not to stop read/write immediately when an error event happens. For example, bus testing procedure for MMC card.

**Data Fields**

- bool `enableAutoCommand12`  
*Enable auto CMD12.*
- bool `enableAutoCommand23`  
*Enable auto CMD23.*
- bool `enableIgnoreError`  
*Enable to ignore error event to read/write all the data.*
- `usdhc_transfer_direction_t dataDirection`  
*data direction*
- `uint8_t dataType`  
*this is used to distinguish the normal/tuning/boot data.*
- `size_t blockSize`  
*Block size.*
- `usdhc_scatter_gather_data_list_t sgData`  
*scatter gather data*

**Field Documentation**

- (1) **bool usdhc\_scatter\_gather\_data\_t::enableAutoCommand12**
- (2) **bool usdhc\_scatter\_gather\_data\_t::enableAutoCommand23**
- (3) **bool usdhc\_scatter\_gather\_data\_t::enableIgnoreError**
- (4) **uint8\_t usdhc\_scatter\_gather\_data\_t::dataType**
- (5) **size\_t usdhc\_scatter\_gather\_data\_t::blockSize**

**47.3.9 struct usdhc\_scatter\_gather\_transfer\_t****Data Fields**

- **usdhc\_scatter\_gather\_data\_t \* data**  
*Data to transfer.*
- **usdhc\_command\_t \* command**  
*Command to send.*

**Field Documentation**

- (1) **usdhc\_scatter\_gather\_data\_t\* usdhc\_scatter\_gather\_transfer\_t::data**
- (2) **usdhc\_command\_t\* usdhc\_scatter\_gather\_transfer\_t::command**

**47.3.10 struct usdhc\_data\_t**

Defines a structure to contain data-related attribute. The 'enableIgnoreError' is used when upper card driver wants to ignore the error event to read/write all the data and not to stop read/write immediately when an error event happens. For example, bus testing procedure for MMC card.

**Data Fields**

- **bool enableAutoCommand12**  
*Enable auto CMD12.*
- **bool enableAutoCommand23**  
*Enable auto CMD23.*
- **bool enableIgnoreError**  
*Enable to ignore error event to read/write all the data.*
- **uint8\_t dataType**  
*this is used to distinguish the normal/tuning/boot data.*
- **size\_t blockSize**  
*Block size.*
- **uint32\_t blockCount**  
*Block count.*
- **uint32\_t \* rxData**

- `const uint32_t * txData`  
*Buffer to save data read.*
- `const uint32_t * txData`  
*Data buffer to write.*

### Field Documentation

- (1) `bool usdhc_data_t::enableAutoCommand12`
- (2) `bool usdhc_data_t::enableAutoCommand23`
- (3) `bool usdhc_data_t::enableIgnoreError`
- (4) `uint8_t usdhc_data_t::dataType`
- (5) `size_t usdhc_data_t::blockSize`
- (6) `uint32_t usdhc_data_t::blockCount`
- (7) `uint32_t* usdhc_data_t::rxData`
- (8) `const uint32_t* usdhc_data_t::txData`

### 47.3.11 struct usdhc\_transfer\_t

#### Data Fields

- `usdhc_data_t * data`  
*Data to transfer.*
- `usdhc_command_t * command`  
*Command to send.*

### Field Documentation

- (1) `usdhc_data_t* usdhc_transfer_t::data`
- (2) `usdhc_command_t* usdhc_transfer_t::command`

### 47.3.12 struct usdhc\_transfer\_callback\_t

#### Data Fields

- `void(* CardInserted )(USDHC_Type *base, void *userData)`  
*Card inserted occurs when DAT3/CD pin is for card detect.*
- `void(* CardRemoved )(USDHC_Type *base, void *userData)`  
*Card removed occurs.*
- `void(* SdioInterrupt )(USDHC_Type *base, void *userData)`  
*SDIO card interrupt occurs.*
- `void(* BlockGap )(USDHC_Type *base, void *userData)`  
*stopped at block gap event*

- void(\* **TransferComplete** )(USDHC\_Type \*base, usdhc\_handle\_t \*handle, **status\_t** status, void \*userData)
 

*Transfer complete callback.*
- void(\* **ReTuning** )(USDHC\_Type \*base, void \*userData)
 

*Handle the re-tuning.*

### Field Documentation

- (1) void(\* **usdhc\_transfer\_callback\_t**::**TransferComplete**)(USDHC\_Type \*base, usdhc\_handle\_t \*handle, **status\_t** status, void \*userData)
- (2) void(\* **usdhc\_transfer\_callback\_t**::**ReTuning**)(USDHC\_Type \*base, void \*userData)

### 47.3.13 struct \_usdhc\_handle

USDHC handle typedef.

Defines the structure to save the USDHC state information and callback function.

#### Note

All the fields except interruptFlags and transferredWords must be allocated by the user.

### Data Fields

- **usdhc\_data\_t** \*volatile **data**

*Transfer parameter.*
- **usdhc\_command\_t** \*volatile **command**

*Transfer parameter.*
- volatile uint32\_t **transferredWords**

*Transfer status.*
- **usdhc\_transfer\_callback\_t** **callback**

*Callback function.*
- void \* **userData**

*Parameter for transfer complete callback.*

### Field Documentation

- (1) **usdhc\_data\_t\*** **volatile usdhc\_handle\_t**::**data**

Data to transfer.
- (2) **usdhc\_command\_t\*** **volatile usdhc\_handle\_t**::**command**

Command to send.
- (3) **volatile uint32\_t usdhc\_handle\_t**::**transferredWords**

Words transferred by DATAPORT way.

- (4) `usdhc_transfer_callback_t usdhc_handle_t::callback`
- (5) `void* usdhc_handle_t::userData`

#### 47.3.14 struct usdhc\_host\_t

##### Data Fields

- `USDHC_Type * base`  
*USDHC peripheral base address.*
- `uint32_t sourceClock_Hz`  
*USDHC source clock frequency united in Hz.*
- `usdhc_config_t config`  
*USDHC configuration.*
- `usdhc_capability_t capability`  
*USDHC capability information.*
- `usdhc_transfer_function_t transfer`  
*USDHC transfer function.*

##### Field Documentation

- (1) `USDHC_Type* usdhc_host_t::base`
- (2) `uint32_t usdhc_host_t::sourceClock_Hz`
- (3) `usdhc_config_t usdhc_host_t::config`
- (4) `usdhc_capability_t usdhc_host_t::capability`
- (5) `usdhc_transfer_function_t usdhc_host_t::transfer`

#### 47.4 Macro Definition Documentation

47.4.1 `#define FSL_USDHC_DRIVER_VERSION (MAKE_VERSION(2U, 8U, 2U))`

47.4.2 `#define USDHC_ADMA1_ADDRESS_ALIGN (4096U)`

47.4.3 `#define USDHC_ADMA1_LENGTH_ALIGN (4096U)`

47.4.4 `#define USDHC_ADMA2_ADDRESS_ALIGN (4U)`

47.4.5 `#define USDHC_ADMA2_LENGTH_ALIGN (4U)`

47.4.6 `#define USDHC_ADMA1_DESCRIPTOR_ADDRESS_SHIFT (12U)`

Address/page field	Reserved	6p(*8-*3)*6/8 lightgrayAttribute	04	03	02	01
31 12	11 6	05				
address or data length	000000	Act2	Act1	0	Int	E

**ADMA1 descriptor table**

Act2	Act1	Comment	31-28	27-12
0	0	No op	Don't care	
0	1	Set data length	0000	Data Length
1	0	Transfer data	Data address	
1	1	Link descriptor	Descriptor address	

**ADMA2 action**

**47.4.7 #define USDHC\_ADMA1\_DESCRIPTOR\_ADDRESS\_MASK (0xFFFFFU)**

**47.4.8 #define USDHC\_ADMA1\_DESCRIPTOR\_LENGTH\_SHIFT (12U)**

**47.4.9 #define USDHC\_ADMA1\_DESCRIPTOR\_LENGTH\_MASK (0xFFFFU)**

**47.4.10 #define USDHC\_ADMA1\_DESCRIPTOR\_MAX\_LENGTH\_PER\_ENTRY (USDHC\_ADMA1\_DESCRIPTOR\_LENGTH\_MASK + 1U - 4096U)**

Since the max transfer size ADMA1 support is 65535 which is indivisible by 4096, so to make sure a large data load transfer (>64KB) continuously (require the data address be always align with 4096), software will set the maximum data length for ADMA1 to (64 - 4)KB.

**47.4.11 #define USDHC\_ADMA2\_DESCRIPTOR\_LENGTH\_SHIFT (16U)**

Address field	Length	Reserved	6p(*9-*4)*6/9 lightgrayAttribute	04	03	02	01
63 32	31 16	15 06	05				
32-bit address	16-bit length	0000000000	Act2	Act1	0	Int	E

**ADMA2 descriptor table**

<b>Act2</b>	<b>Act1</b>	<b>Comment</b>	<b>Operation</b>
0	0	No op	Don't care
0	1	Reserved	Read this line and go to next one
1	0	Transfer data	Transfer data with address and length set in this descriptor line
1	1	Link descriptor	Link to another descriptor

**ADMA2 action****47.6 Enumeration Type Documentation****47.6.1 anonymous enum**

USDHC status.

Enumerator

- kStatus\_USDHC\_BusyTransferring* Transfer is on-going.
- kStatus\_USDHC\_PrepAdmaDescriptorFailed* Set DMA descriptor failed.
- kStatus\_USDHC\_SendCommandFailed* Send command failed.
- kStatus\_USDHC\_TransferDataFailed* Transfer data failed.
- kStatus\_USDHC\_DMADataAddrNotAlign* Data address not aligned.
- kStatus\_USDHC\_ReTuningRequest* Re-tuning request.
- kStatus\_USDHC\_TuningError* Tuning error.
- kStatus\_USDHC\_NotSupport* Not support.
- kStatus\_USDHC\_TransferDataComplete* Transfer data complete.
- kStatus\_USDHC\_SendCommandSuccess* Transfer command complete.
- kStatus\_USDHC\_TransferDMAComplete* Transfer DMA complete.

**47.6.2 anonymous enum**

Host controller capabilities flag mask.

Enumerator

- kUSDHC\_SupportAdmaFlag* Support ADMA.
- kUSDHC\_SupportHighSpeedFlag* Support high-speed.
- kUSDHC\_SupportDmaFlag* Support DMA.
- kUSDHC\_SupportSuspendResumeFlag* Support suspend/resume.
- kUSDHC\_SupportV330Flag* Support voltage 3.3V.

- kUSDHC\_SupportV300Flag* Support voltage 3.0V.
- kUSDHC\_SupportV180Flag* Support voltage 1.8V.
- kUSDHC\_Support4BitFlag* Flag in HTCAPBLT\_MBL's position, supporting 4-bit mode.
- kUSDHC\_Support8BitFlag* Flag in HTCAPBLT\_MBL's position, supporting 8-bit mode.
- kUSDHC\_SupportDDR50Flag* SD version 3.0 new feature, supporting DDR50 mode.
- kUSDHC\_SupportSDR104Flag* Support SDR104 mode.
- kUSDHC\_SupportSDR50Flag* Support SDR50 mode.

#### 47.6.3 anonymous enum

Wakeup event mask.

Enumerator

- kUSDHC\_WakeupEventOnCardInt* Wakeup on card interrupt.
- kUSDHC\_WakeupEventOnCardInsert* Wakeup on card insertion.
- kUSDHC\_WakeupEventOnCardRemove* Wakeup on card removal.
- kUSDHC\_WakeupEventsAll* All wakeup events.

#### 47.6.4 anonymous enum

Reset type mask.

Enumerator

- kUSDHC\_ResetAll* Reset all except card detection.
- kUSDHC\_ResetCommand* Reset command line.
- kUSDHC\_ResetData* Reset data line.
- kUSDHC\_ResetTuning* Reset tuning circuit.
- kUSDHC\_ResetsAll* All reset types.

#### 47.6.5 anonymous enum

Transfer flag mask.

Enumerator

- kUSDHC\_EnableDmaFlag* Enable DMA.
- kUSDHC\_CommandTypeSuspendFlag* Suspend command.
- kUSDHC\_CommandTypeResumeFlag* Resume command.
- kUSDHC\_CommandTypeAbortFlag* Abort command.
- kUSDHC\_EnableBlockCountFlag* Enable block count.
- kUSDHC\_EnableAutoCommand12Flag* Enable auto CMD12.
- kUSDHC\_DataReadFlag* Enable data read.

*kUSDHC\_MultipleBlockFlag* Multiple block data read/write.  
*kUSDHC\_EnableAutoCommand23Flag* Enable auto CMD23.  
*kUSDHC\_ResponseLength136Flag* 136-bit response length.  
*kUSDHC\_ResponseLength48Flag* 48-bit response length.  
*kUSDHC\_ResponseLength48BusyFlag* 48-bit response length with busy status.  
*kUSDHC\_EnableCrcCheckFlag* Enable CRC check.  
*kUSDHC\_EnableIndexCheckFlag* Enable index check.  
*kUSDHC\_DataPresentFlag* Data present flag.

#### 47.6.6 anonymous enum

Present status flag mask.

Enumerator

*kUSDHC\_CommandInhibitFlag* Command inhibit.  
*kUSDHC\_DataInhibitFlag* Data inhibit.  
*kUSDHC\_DataLineActiveFlag* Data line active.  
*kUSDHC\_SdClockStableFlag* SD bus clock stable.  
*kUSDHC\_WriteTransferActiveFlag* Write transfer active.  
*kUSDHC\_ReadTransferActiveFlag* Read transfer active.  
*kUSDHC\_BufferWriteEnableFlag* Buffer write enable.  
*kUSDHC\_BufferReadEnableFlag* Buffer read enable.  
*kUSDHC\_ReTuningRequestFlag* Re-tuning request flag, only used for SDR104 mode.  
*kUSDHC\_DelaySettingFinishedFlag* Delay setting finished flag.  
*kUSDHC\_CardInsertedFlag* Card inserted.  
*kUSDHC\_CommandLineLevelFlag* Command line signal level.  
*kUSDHC\_Data0LineLevelFlag* Data0 line signal level.  
*kUSDHC\_Data1LineLevelFlag* Data1 line signal level.  
*kUSDHC\_Data2LineLevelFlag* Data2 line signal level.  
*kUSDHC\_Data3LineLevelFlag* Data3 line signal level.  
*kUSDHC\_Data4LineLevelFlag* Data4 line signal level.  
*kUSDHC\_Data5LineLevelFlag* Data5 line signal level.  
*kUSDHC\_Data6LineLevelFlag* Data6 line signal level.  
*kUSDHC\_Data7LineLevelFlag* Data7 line signal level.

#### 47.6.7 anonymous enum

Interrupt status flag mask.

Enumerator

*kUSDHC\_CommandCompleteFlag* Command complete.  
*kUSDHC\_DataCompleteFlag* Data complete.

*kUSDHC\_BlockGapEventFlag* Block gap event.  
*kUSDHC\_DmaCompleteFlag* DMA interrupt.  
*kUSDHC\_BufferWriteReadyFlag* Buffer write ready.  
*kUSDHC\_BufferReadReadyFlag* Buffer read ready.  
*kUSDHC\_CardInsertionFlag* Card inserted.  
*kUSDHC\_CardRemovalFlag* Card removed.  
*kUSDHC\_CardInterruptFlag* Card interrupt.  
*kUSDHC\_ReTuningEventFlag* Re-Tuning event, only for SD3.0 SDR104 mode.  
*kUSDHC\_TuningPassFlag* SDR104 mode tuning pass flag.  
*kUSDHC\_TuningErrorFlag* SDR104 tuning error flag.  
*kUSDHC\_CommandTimeoutFlag* Command timeout error.  
*kUSDHC\_CommandCrcErrorFlag* Command CRC error.  
*kUSDHC\_CommandEndBitErrorFlag* Command end bit error.  
*kUSDHC\_CommandIndexErrorFlag* Command index error.  
*kUSDHC\_DataTimeoutFlag* Data timeout error.  
*kUSDHC\_DataCrcErrorFlag* Data CRC error.  
*kUSDHC\_DataEndBitErrorFlag* Data end bit error.  
*kUSDHC\_AutoCommand12ErrorFlag* Auto CMD12 error.  
*kUSDHC\_DmaErrorFlag* DMA error.  
*kUSDHC\_CommandErrorFlag* Command error.  
*kUSDHC\_DataErrorFlag* Data error.  
*kUSDHC\_ErrorFlag* All error.  
*kUSDHC\_DataFlag* Data interrupts.  
*kUSDHC\_DataDMAFlag* Data interrupts.  
*kUSDHC\_CommandFlag* Command interrupts.  
*kUSDHC\_CardDetectFlag* Card detection interrupts.  
*kUSDHC\_SDR104TuningFlag* SDR104 tuning flag.  
*kUSDHC\_AllInterruptFlags* All flags mask.

#### 47.6.8 anonymous enum

Auto CMD12 error status flag mask.

Enumerator

*kUSDHC\_AutoCommand12NotExecutedFlag* Not executed error.  
*kUSDHC\_AutoCommand12TimeoutFlag* Timeout error.  
*kUSDHC\_AutoCommand12EndBitErrorFlag* End bit error.  
*kUSDHC\_AutoCommand12CrcErrorFlag* CRC error.  
*kUSDHC\_AutoCommand12IndexErrorFlag* Index error.  
*kUSDHC\_AutoCommand12NotIssuedFlag* Not issued error.

### 47.6.9 anonymous enum

Standard tuning flag.

Enumerator

***kUSDHC\_ExecuteTuning*** Used to start tuning procedure.

***kUSDHC\_TuningSampleClockSel*** When `std_tuning_en` bit is set, this bit is used to select sampleing clock.

### 47.6.10 anonymous enum

ADMA error status flag mask.

Enumerator

***kUSDHC\_AdmaLengthMismatchFlag*** Length mismatch error.

***kUSDHC\_AdmaDescriptorErrorFlag*** Descriptor error.

### 47.6.11 anonymous enum

ADMA error state.

This state is the detail state when ADMA error has occurred.

Enumerator

***kUSDHC\_AdmaErrorStateStopDma*** Stop DMA, previous location set in the ADMA system address is errored address.

***kUSDHC\_AdmaErrorStateFetchDescriptor*** Fetch descriptor, current location set in the ADMA system address is errored address.

***kUSDHC\_AdmaErrorStateChangeAddress*** Change address, no DMA error has occurred.

***kUSDHC\_AdmaErrorStateTransferData*** Transfer data, previous location set in the ADMA system address is errored address.

***kUSDHC\_AdmaErrorStateInvalidLength*** Invalid length in ADMA descriptor.

***kUSDHC\_AdmaErrorStateInvalidDescriptor*** Invalid descriptor fetched by ADMA.

***kUSDHC\_AdmaErrorState*** ADMA error state.

### 47.6.12 anonymous enum

Force event bit position.

Enumerator

***kUSDHC\_ForceEventAutoCommand12NotExecuted*** Auto CMD12 not executed error.

*kUSDHC\_ForceEventAutoCommand12Timeout* Auto CMD12 timeout error.  
*kUSDHC\_ForceEventAutoCommand12CrcError* Auto CMD12 CRC error.  
*kUSDHC\_ForceEventEndBitError* Auto CMD12 end bit error.  
*kUSDHC\_ForceEventAutoCommand12IndexError* Auto CMD12 index error.  
*kUSDHC\_ForceEventAutoCommand12NotIssued* Auto CMD12 not issued error.  
*kUSDHC\_ForceEventCommandTimeout* Command timeout error.  
*kUSDHC\_ForceEventCommandCrcError* Command CRC error.  
*kUSDHC\_ForceEventCommandEndBitError* Command end bit error.  
*kUSDHC\_ForceEventCommandIndexError* Command index error.  
*kUSDHC\_ForceEventDataTimeout* Data timeout error.  
*kUSDHC\_ForceEventDataCrcError* Data CRC error.  
*kUSDHC\_ForceEventDataEndBitError* Data end bit error.  
*kUSDHC\_ForceEventAutoCommand12Error* Auto CMD12 error.  
*kUSDHC\_ForceEventCardInt* Card interrupt.  
*kUSDHC\_ForceEventDmaError* Dma error.  
*kUSDHC\_ForceEventTuningError* Tuning error.  
*kUSDHC\_ForceEventsAll* All force event flags mask.

#### 47.6.13 enum usdhc\_transfer\_direction\_t

Enumerator

*kUSDHC\_TransferDirectionReceive* USDHC transfer direction receive.  
*kUSDHC\_TransferDirectionSend* USDHC transfer direction send.

#### 47.6.14 enum usdhc\_data\_bus\_width\_t

Enumerator

*kUSDHC\_DataBusWidth1Bit* 1-bit mode  
*kUSDHC\_DataBusWidth4Bit* 4-bit mode  
*kUSDHC\_DataBusWidth8Bit* 8-bit mode

#### 47.6.15 enum usdhc\_endian\_mode\_t

Enumerator

*kUSDHC\_EndianModeBig* Big endian mode.  
*kUSDHC\_EndianModeHalfWordBig* Half word big endian mode.  
*kUSDHC\_EndianModeLittle* Little endian mode.

**47.6.16 enum usdhc\_dma\_mode\_t**

Enumerator

- kUSDHC\_DmaModeSimple* External DMA.
- kUSDHC\_DmaModeAdma1* ADMA1 is selected.
- kUSDHC\_DmaModeAdma2* ADMA2 is selected.
- kUSDHC\_ExternalDMA* External DMA mode selected.

**47.6.17 anonymous enum**

SDIO control flag mask.

Enumerator

- kUSDHC\_StopAtBlockGapFlag* Stop at block gap.
- kUSDHC\_ReadWaitControlFlag* Read wait control.
- kUSDHC\_InterruptAtBlockGapFlag* Interrupt at block gap.
- kUSDHC\_ReadDoneNo8CLK* Read done without 8 clk for block gap.
- kUSDHC\_ExactBlockNumberReadFlag* Exact block number read.

**47.6.18 enum usdhc\_boot\_mode\_t**

Enumerator

- kUSDHC\_BootModeNormal* Normal boot.
- kUSDHC\_BootModeAlternative* Alternative boot.

**47.6.19 enum usdhc\_card\_command\_type\_t**

Enumerator

- kCARD\_CommandTypeNormal* Normal command.
- kCARD\_CommandTypeSuspend* Suspend command.
- kCARD\_CommandTypeResume* Resume command.
- kCARD\_CommandTypeAbort* Abort command.
- kCARD\_CommandTypeEmpty* Empty command.

**47.6.20 enum usdhc\_card\_response\_type\_t**

Defines the command response type from card to host controller.

Enumerator

- kCARD\_ResponseNone* Response type: none.
- kCARD\_ResponseR1* Response type: R1.
- kCARD\_ResponseR1b* Response type: R1b.
- kCARD\_ResponseR2* Response type: R2.
- kCARD\_ResponseR3* Response type: R3.
- kCARD\_ResponseR4* Response type: R4.
- kCARD\_ResponseR5* Response type: R5.
- kCARD\_ResponseR5b* Response type: R5b.
- kCARD\_ResponseR6* Response type: R6.
- kCARD\_ResponseR7* Response type: R7.

#### 47.6.21 anonymous enum

The mask for the control/status field in ADMA1 descriptor.

Enumerator

- kUSDHC\_Adma1DescriptorValidFlag* Valid flag.
- kUSDHC\_Adma1DescriptorEndFlag* End flag.
- kUSDHC\_Adma1DescriptorInterruptFlag* Interrupt flag.
- kUSDHC\_Adma1DescriptorActivity1Flag* Activity 1 flag.
- kUSDHC\_Adma1DescriptorActivity2Flag* Activity 2 flag.
- kUSDHC\_Adma1DescriptorTypeNop* No operation.
- kUSDHC\_Adma1DescriptorTypeTransfer* Transfer data.
- kUSDHC\_Adma1DescriptorTypeLink* Link descriptor.
- kUSDHC\_Adma1DescriptorTypeSetLength* Set data length.

#### 47.6.22 anonymous enum

ADMA1 descriptor control and status mask.

Enumerator

- kUSDHC\_Adma2DescriptorValidFlag* Valid flag.
- kUSDHC\_Adma2DescriptorEndFlag* End flag.
- kUSDHC\_Adma2DescriptorInterruptFlag* Interrupt flag.
- kUSDHC\_Adma2DescriptorActivity1Flag* Activity 1 mask.
- kUSDHC\_Adma2DescriptorActivity2Flag* Activity 2 mask.
- kUSDHC\_Adma2DescriptorTypeNop* No operation.
- kUSDHC\_Adma2DescriptorTypeReserved* Reserved.
- kUSDHC\_Adma2DescriptorTypeTransfer* Transfer type.
- kUSDHC\_Adma2DescriptorTypeLink* Link type.

### 47.6.23 anonymous enum

ADMA descriptor configuration flag.

Enumerator

***kUSDHC\_AdmaDescriptorSingleFlag*** Try to finish the transfer in a single ADMA descriptor. If transfer size is bigger than one ADMA descriptor's ability, new another descriptor for data transfer.

***kUSDHC\_AdmaDescriptorMultipleFlag*** Create multiple ADMA descriptors within the ADMA table, this is used for mmc boot mode specifically, which need to modify the ADMA descriptor on the fly, so the flag should be used combining with stop at block gap feature.

### 47.6.24 enum usdhc\_burst\_len\_t

Enumerator

***kUSDHC\_EnBurstLenForINCR*** Enable burst len for INCR.

***kUSDHC\_EnBurstLenForINCR4816*** Enable burst len for INCR4/INCR8/INCR16.

***kUSDHC\_EnBurstLenForINCR4816WRAP*** Enable burst len for INCR4/8/16 WRAP.

### 47.6.25 anonymous enum

Transfer data type definition.

Enumerator

***kUSDHC\_TransferDataNormal*** Transfer normal read/write data.

***kUSDHC\_TransferDataTuning*** Transfer tuning data.

***kUSDHC\_TransferDataBoot*** Transfer boot data.

***kUSDHC\_TransferDataBootcontinuous*** Transfer boot data continuously.

## 47.7 Function Documentation

### 47.7.1 void USDHC\_Init ( ***USDHC\_Type \* base***, ***const usdhc\_config\_t \* config*** )

Configures the USDHC according to the user configuration.

Example:

```
usdhc_config_t config;
config.cardDetectDat3 = false;
config.endianMode = kUSDHC_EndianModeLittle;
config.dmaMode = kUSDHC_DmaModeAdma2;
config.readWatermarkLevel = 128U;
config.writeWatermarkLevel = 128U;
USDHC_Init(USDHC, &config);
```

Parameters

<i>base</i>	USDHC peripheral base address.
<i>config</i>	USDHC configuration information.

Return values

<i>kStatus_Success</i>	Operate successfully.
------------------------	-----------------------

#### 47.7.2 void USDHC\_Deinit ( **USDHC\_Type** \* *base* )

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

#### 47.7.3 bool USDHC\_Reset ( **USDHC\_Type** \* *base*, **uint32\_t** *mask*, **uint32\_t** *timeout* )

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	The reset type mask( <a href="#">_usdhc_reset</a> ).
<i>timeout</i>	Timeout for reset.

Return values

<i>true</i>	Reset successfully.
<i>false</i>	Reset failed.

#### 47.7.4 status\_t USDHC\_SetAdmaTableConfig ( **USDHC\_Type** \* *base*, **usdhc\_adma\_config\_t** \* *dmaConfig*, **usdhc\_data\_t** \* *dataConfig*, **uint32\_t** *flags* )

A high level DMA descriptor configuration function.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>dmaConfig</i>	ADMA configuration
<i>dataConfig</i>	Data descriptor
<i>flags</i>	ADAM descriptor flag, used to indicate to create multiple or single descriptor, please refer to enum <a href="#">_usdhc_adma_flag</a> .

Return values

<a href="#">kStatus_OutOfRange</a>	ADMA descriptor table length isn't enough to describe data.
<a href="#">kStatus_Success</a>	Operate successfully.

**47.7.5 status\_t USDHC\_SetInternalDmaConfig ( **USDHC\_Type** \* *base*, **usdhc\_adma\_config\_t** \* *dmaConfig*, const **uint32\_t** \* *dataAddr*, **bool enAutoCmd23** )**

This function is used to config the USDHC DMA related registers.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>dmaConfig</i>	ADMA configuration.
<i>dataAddr</i>	Transfer data address, a simple DMA parameter, if ADMA is used, leave it to NULL.
<i>enAutoCmd23</i>	Flag to indicate Auto CMD23 is enable or not, a simple DMA parameter, if ADMA is used, leave it to false.

Return values

<a href="#">kStatus_OutOfRange</a>	ADMA descriptor table length isn't enough to describe data.
<a href="#">kStatus_Success</a>	Operate successfully.

**47.7.6 status\_t USDHC\_SetADMA2Descriptor ( **uint32\_t** \* *admaTable*, **uint32\_t admaTableWords**, const **uint32\_t** \* *dataBufferAddr*, **uint32\_t dataBytes**, **uint32\_t flags** )**

Parameters

<i>admaTable</i>	ADMA table address.
<i>admaTableWords</i>	ADMA table length.
<i>dataBufferAddr</i>	Data buffer address.
<i>dataBytes</i>	Data Data length.
<i>flags</i>	ADAM descriptor flag, used to indicate to create multiple or single descriptor, please refer to enum <a href="#">_usdhc_adma_flag</a> .

Return values

<a href="#">kStatus_OutOfRange</a>	ADMA descriptor table length isn't enough to describe data.
<a href="#">kStatus_Success</a>	Operate successfully.

#### 47.7.7 **status\_t USDHC\_SetADMA1Descriptor ( uint32\_t \* *admaTable*, uint32\_t *admaTableWords*, const uint32\_t \* *dataBufferAddr*, uint32\_t *dataBytes*, uint32\_t *flags* )**

Parameters

<i>admaTable</i>	ADMA table address.
<i>admaTableWords</i>	ADMA table length.
<i>dataBufferAddr</i>	Data buffer address.
<i>dataBytes</i>	Data length.
<i>flags</i>	ADAM descriptor flag, used to indicate to create multiple or single descriptor, please refer to enum <a href="#">_usdhc_adma_flag</a> .

Return values

<a href="#">kStatus_OutOfRange</a>	ADMA descriptor table length isn't enough to describe data.
<a href="#">kStatus_Success</a>	Operate successfully.

#### 47.7.8 **static void USDHC\_EnableInternalDMA ( USDHC\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	enable or disable flag

#### 47.7.9 static void USDHC\_EnableInterruptStatus ( **USDHC\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	Interrupt status flags mask( <a href="#">_usdhc_interrupt_status_flag</a> ).

#### 47.7.10 static void USDHC\_DisableInterruptStatus ( **USDHC\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	The interrupt status flags mask( <a href="#">_usdhc_interrupt_status_flag</a> ).

#### 47.7.11 static void USDHC\_EnableInterruptSignal ( **USDHC\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	The interrupt status flags mask( <a href="#">_usdhc_interrupt_status_flag</a> ).

#### 47.7.12 static void USDHC\_DisableInterruptSignal ( **USDHC\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	The interrupt status flags mask( <a href="#">_usdhc_interrupt_status_flag</a> ).

#### 47.7.13 static uint32\_t USDHC\_GetEnabledInterruptStatusFlags ( **USDHC\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

Returns

Current interrupt status flags mask([\\_usdhc\\_interrupt\\_status\\_flag](#)).

#### 47.7.14 static uint32\_t USDHC\_GetInterruptStatusFlags ( **USDHC\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

Returns

Current interrupt status flags mask([\\_usdhc\\_interrupt\\_status\\_flag](#)).

#### 47.7.15 static void USDHC\_ClearInterruptStatusFlags ( **USDHC\_Type** \* *base*, uint32\_t *mask* ) [inline], [static]

write 1 clears

Parameters

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<i>base</i>	USDHC peripheral base address.
<i>mask</i>	The interrupt status flags mask( <a href="#">_usdhc_interrupt_status_flag</a> ).

#### 47.7.16 static uint32\_t USDHC\_GetAutoCommand12ErrorStatusFlags ( **USDHC\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

Returns

Auto command 12 error status flags mask([\\_usdhc\\_auto\\_command12\\_error\\_status\\_flag](#)).

#### 47.7.17 static uint32\_t USDHC\_GetAdmaErrorStatusFlags ( **USDHC\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

Returns

ADMA error status flags mask([\\_usdhc\\_adma\\_error\\_status\\_flag](#)).

#### 47.7.18 static uint32\_t USDHC\_GetPresentStatusFlags ( **USDHC\_Type** \* *base* ) [inline], [static]

This function gets the present USDHC's status except for an interrupt status and an error status.

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

Returns

Present USDHC's status flags mask([\\_usdhc\\_present\\_status\\_flag](#)).

47.7.19 **void USDHC\_GetCapability ( **USDHC\_Type** \* *base*, **usdhc\_capability\_t** \* *capability* )**

Parameters

<i>base</i>	USDHC peripheral base address.
<i>capability</i>	Structure to save capability information.

**47.7.20 static void USDHC\_ForceClockOn ( **USDHC\_Type** \* *base*, **bool** *enable* )  
[inline], [static]**

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	enable/disable flag

**47.7.21 **uint32\_t** USDHC\_SetSdClock ( **USDHC\_Type** \* *base*, **uint32\_t** *srcClock\_Hz*,  
**uint32\_t** *busClock\_Hz* )**

Parameters

<i>base</i>	USDHC peripheral base address.
<i>srcClock_Hz</i>	USDHC source clock frequency united in Hz.
<i>busClock_Hz</i>	SD bus clock frequency united in Hz.

Returns

The nearest frequency of busClock\_Hz configured for SD bus.

**47.7.22 **bool** USDHC\_SetCardActive ( **USDHC\_Type** \* *base*, **uint32\_t** *timeout* )**

This function must be called each time the card is inserted to ensure that the card can receive the command correctly.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>timeout</i>	Timeout to initialize card.

Return values

<i>true</i>	Set card active successfully.
<i>false</i>	Set card active failed.

#### 47.7.23 static void USDHC\_AassertHardwareReset ( **USDHC\_Type** \* *base*, **bool** *high* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>high</i>	1 or 0 level

#### 47.7.24 static void USDHC\_SetDataBusWidth ( **USDHC\_Type** \* *base*, **usdhc\_data\_bus\_width\_t** *width* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>width</i>	Data transfer width.

#### 47.7.25 static void USDHC\_WriteData ( **USDHC\_Type** \* *base*, **uint32\_t** *data* ) [inline], [static]

This function is used to implement the data transfer by Data Port instead of DMA.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>data</i>	The data about to be sent.

**47.7.26 static uint32\_t USDHC\_ReadData ( USDHC\_Type \* *base* ) [inline],  
[static]**

This function is used to implement the data transfer by Data Port instead of DMA.

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

Returns

The data has been read.

#### 47.7.27 void USDHC\_SendCommand ( **USDHC\_Type** \* *base*, **usdhc\_command\_t** \* *command* )

Parameters

<i>base</i>	USDHC peripheral base address.
<i>command</i>	configuration

#### 47.7.28 static void USDHC\_EnableWakeupEvent ( **USDHC\_Type** \* *base*, **uint32\_t** *mask*, **bool** *enable* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	Wakeup events mask( <a href="#">_usdhc_wakeup_event</a> ).
<i>enable</i>	True to enable, false to disable.

#### 47.7.29 static void USDHC\_CardDetectByData3 ( **USDHC\_Type** \* *base*, **bool** *enable* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	enable/disable flag

#### 47.7.30 static bool USDHC\_DetectCardInsert ( **USDHC\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

#### 47.7.31 static void USDHC\_EnableSdioControl ( **USDHC\_Type** \* *base*, **uint32\_t** *mask*, **bool** *enable* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	SDIO card control flags mask( <a href="#">_usdhc_sdio_control_flag</a> ).
<i>enable</i>	True to enable, false to disable.

#### 47.7.32 static void USDHC\_SetContinueRequest ( **USDHC\_Type** \* *base* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
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#### 47.7.33 static void USDHC\_RequestStopAtBlockGap ( **USDHC\_Type** \* *base*, **bool** *enable* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	True to stop at block gap, false to normal transfer.

#### 47.7.34 void USDHC\_SetMmcBootConfig ( **USDHC\_Type** \* *base*, **const** **usdhc\_boot\_config\_t** \* *config* )

Example:

```
usdhc_boot_config_t config;
config.ackTimeoutCount = 4;
config.bootMode = kUSDHC_BootModeNormal;
config.blockCount = 5;
config.enableBootAck = true;
```

```
config.enableBoot = true;
config.enableAutoStopAtBlockGap = true;
USDHC_SetMmcBootConfig(USDHC, &config);
```

Parameters

<i>base</i>	USDHC peripheral base address.
<i>config</i>	The MMC boot configuration information.

#### 47.7.35 static void USDHC\_EnableMmcBoot ( **USDHC\_Type** \* *base*, **bool** *enable* ) [**inline**], [**static**]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	True to enable, false to disable.

#### 47.7.36 static void USDHC\_SetForceEvent ( **USDHC\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>mask</i>	The force events bit position (_usdhc_force_event).

#### 47.7.37 static void UDSHC\_SelectVoltage ( **USDHC\_Type** \* *base*, **bool** *en18v* ) [**inline**], [**static**]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>en18v</i>	True means 1.8V, false means 3.0V.

#### 47.7.38 static bool USDHC\_RequestTuningForSDR50 ( **USDHC\_Type** \* *base* ) [**inline**], [**static**]

When this bit set, application shall perform tuning for SDR50 mode.

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

#### 47.7.39 static bool USDHC\_RequestReTuning ( **USDHC\_Type** \* *base* ) [inline], [static]

When this bit is set, user should do manual tuning or standard tuning function.

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

#### 47.7.40 static void USDHC\_EnableAutoTuning ( **USDHC\_Type** \* *base*, **bool** *enable* ) [inline], [static]

This function should be called after tuning function execute pass, auto tuning will handle by hardware.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	enable/disable flag

#### 47.7.41 void USDHC\_EnableAutoTuningForCmdAndData ( **USDHC\_Type** \* *base* )

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

#### 47.7.42 void USDHC\_EnableManualTuning ( **USDHC\_Type** \* *base*, **bool** *enable* )

User should handle the tuning cmd and find the boundary of the delay then calculate a average value which will be configured to the **CLK\_TUNE\_CTRL\_STATUS** This function should be called before function [USDHC\\_AdjustDelayForManualTuning](#).

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	tuning enable flag

**47.7.43 static uint32\_t USDHC\_GetTuningDelayStatus ( **USDHC\_Type** \* *base* )  
[inline], [static]**

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

Return values

<i>CLK</i>	Tuning Control and Status register value.
------------	---

**47.7.44 status\_t USDHC\_SetTuningDelay ( **USDHC\_Type** \* *base*, uint32\_t *preDelay*,  
uint32\_t *outDelay*, uint32\_t *postDelay* )**

Parameters

<i>base</i>	USDHC peripheral base address.
<i>preDelay</i>	Set the number of delay cells on the feedback clock between the feedback clock and CLK_PRE.
<i>outDelay</i>	Set the number of delay cells on the feedback clock between CLK_PRE and CLK_OUT.
<i>postDelay</i>	Set the number of delay cells on the feedback clock between CLK_OUT and CLK_POST.

Return values

<i>kStatus_Fail</i>	config the delay setting fail
<i>kStatus_Success</i>	config the delay setting success

**47.7.45 status\_t USDHC\_AdjustDelayForManualTuning ( **USDHC\_Type** \* *base*,  
uint32\_t *delay* )**

**Deprecated** Do not use this function. It has been superceded by USDHC\_SetTuingDelay

Parameters

<i>base</i>	USDHC peripheral base address.
<i>delay</i>	setting configuration

Return values

<i>kStatus_Fail</i>	config the delay setting fail
<i>kStatus_Success</i>	config the delay setting success

#### 47.7.46 static void USDHC\_SetStandardTuningCounter ( **USDHC\_Type** \* *base*, **uint8\_t** *counter* ) [inline], [static]

Parameters

<i>base</i>	USDHC peripheral base address.
<i>counter</i>	tuning counter

Return values

<i>kStatus_Fail</i>	config the delay setting fail
<i>kStatus_Success</i>	config the delay setting success

#### 47.7.47 void USDHC\_EnableStandardTuning ( **USDHC\_Type** \* *base*, **uint32\_t** *tuningStartTap*, **uint32\_t** *step*, **bool** *enable* )

The standard tuning window and tuning counter using the default config tuning cmd is sent by the software, user need to check whether the tuning result can be used for SDR50, SDR104, and HS200 mode tuning.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>tuningStartTap</i>	start tap
<i>step</i>	tuning step

<i>enable</i>	enable/disable flag
---------------	---------------------

**47.7.48 static uint32\_t USDHC\_GetExecuteStdTuningStatus ( USDHC\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

**47.7.49 static uint32\_t USDHC\_CheckStdTuningResult ( USDHC\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

**47.7.50 static uint32\_t USDHC\_CheckTuningError ( USDHC\_Type \* *base* ) [inline], [static]**

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

**47.7.51 void USDHC\_EnableDDRMode ( USDHC\_Type \* *base*, bool *enable*, uint32\_t *nibblePos* )**

Parameters

<i>base</i>	USDHC peripheral base address.
<i>enable</i>	enable/disable flag
<i>nibblePos</i>	nibble position

47.7.52 **void USDHC\_SetDataConfig ( **USDHC\_Type** \* *base*, **usdhc\_transfer-direction\_t** *dataDirection*, **uint32\_t** *blockCount*, **uint32\_t** *blockSize* )**

Parameters

<i>base</i>	USDHC peripheral base address.
<i>dataDirection</i>	Data direction, tx or rx.
<i>blockCount</i>	Data block count.
<i>blockSize</i>	Data block size.

**47.7.53 void USDHC\_TransferCreateHandle ( ***USDHC\_Type \* base,***  
***usdhc\_handle\_t \* handle,*** ***const usdhc\_transfer\_callback\_t \* callback,***  
***void \* userData )*****

Parameters

<i>base</i>	USDHC peripheral base address.
<i>handle</i>	USDHC handle pointer.
<i>callback</i>	Structure pointer to contain all callback functions.
<i>userData</i>	Callback function parameter.

**47.7.54 status\_t USDHC\_TransferNonBlocking ( ***USDHC\_Type \* base,***  
***usdhc\_handle\_t \* handle,*** ***usdhc\_adma\_config\_t \* dmaConfig,***  
***usdhc\_transfer\_t \* transfer )*****

This function sends a command and data and returns immediately. It doesn't wait for the transfer to complete or to encounter an error. The application must not call this API in multiple threads at the same time. Because of that this API doesn't support the re-entry mechanism.

Note

Call API [USDHC\\_TransferCreateHandle](#) when calling this API.

Parameters

<i>base</i>	USDHC peripheral base address.
-------------	--------------------------------

<i>handle</i>	USDHC handle.
<i>dmaConfig</i>	ADMA configuration.
<i>transfer</i>	Transfer content.

Return values

<i>kStatus_InvalidArgument</i>	Argument is invalid.
<i>kStatus_USDHC_Busy-Transferring</i>	Busy transferring.
<i>kStatus_USDHC_-PrepareAdmaDescriptor-Failed</i>	Prepare ADMA descriptor failed.
<i>kStatus_Success</i>	Operate successfully.

#### 47.7.55 status\_t USDHC\_TransferBlocking ( **USDHC\_Type** \* *base*, **usdhc\_adma\_config\_t** \* *dmaConfig*, **usdhc\_transfer\_t** \* *transfer* )

This function waits until the command response/data is received or the USDHC encounters an error by polling the status flag.

The application must not call this API in multiple threads at the same time. Because this API doesn't support the re-entry mechanism.

Note

There is no need to call API [USDHC\\_TransferCreateHandle](#) when calling this API.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>dmaConfig</i>	adma configuration
<i>transfer</i>	Transfer content.

Return values

<i>kStatus_InvalidArgument</i>	Argument is invalid.
--------------------------------	----------------------

<i>kStatus_USDHC_PrepAdmaDescriptorFailed</i>	Prepare ADMA descriptor failed.
<i>kStatus_USDHC_SendCommandFailed</i>	Send command failed.
<i>kStatus_USDHC_TransferDataFailed</i>	Transfer data failed.
<i>kStatus_Success</i>	Operate successfully.

#### 47.7.56 void USDHC\_TransferHandleIRQ ( **USDHC\_Type** \* *base*, **usdhc\_handle\_t** \* *handle* )

This function deals with the IRQs on the given host controller.

Parameters

<i>base</i>	USDHC peripheral base address.
<i>handle</i>	USDHC handle.

# Chapter 48

## WDOG: Watchdog Timer Driver

### 48.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Watchdog module (WDOG) of MCUXpresso SDK devices.

### 48.2 Typical use case

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/wdog

## Data Structures

- struct `wdog_work_mode_t`  
*Defines WDOG work mode. [More...](#)*
- struct `wdog_config_t`  
*Describes WDOG configuration structure. [More...](#)*

## Enumerations

- enum `_wdog_interrupt_enable` { `kWDOG_InterruptEnable` = `WDOG_WICR_WIE_MASK` }  
*WDOG interrupt configuration structure, default settings all disabled.*
- enum `_wdog_status_flags` {  
  `kWDOG_RunningFlag` = `WDOG_WCR_WDE_MASK`,  
  `kWDOG_PowerOnResetFlag` = `WDOG_WRSR_POR_MASK`,  
  `kWDOG_TimeoutResetFlag` = `WDOG_WRSR_TOUT_MASK`,  
  `kWDOG_SoftwareResetFlag` = `WDOG_WRSR_SFTW_MASK`,  
  `kWDOG InterruptFlag` = `WDOG_WICR_WTIS_MASK` }  
*WDOG status flags.*

## Driver version

- #define `FSL_WDOG_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 1)`)  
*Defines WDOG driver version.*

## Refresh sequence

- #define `WDOG_REFRESH_KEY` (0xAAAA5555U)

## WDOG Initialization and De-initialization.

- void `WDOG_GetDefaultConfig` (`wdog_config_t *config`)  
*Initializes the WDOG configuration structure.*
- void `WDOG_Init` (`WDOG_Type *base, const wdog_config_t *config`)

- `void WDOG_Deinit (WDOG_Type *base)`  
*Initializes the WDOG.*
- `static void WDOG_Enable (WDOG_Type *base)`  
*Shuts down the WDOG.*
- `static void WDOG_Disable (WDOG_Type *base)`  
*Enables the WDOG module.*
- `static void WDOG_Disable (WDOG_Type *base)`  
*Disables the WDOG module.*
- `static void WDOG_TriggerSystemSoftwareReset (WDOG_Type *base)`  
*Trigger the system software reset.*
- `static void WDOG_TriggerSoftwareSignal (WDOG_Type *base)`  
*Trigger an output assertion.*
- `static void WDOG_EnableInterrupts (WDOG_Type *base, uint16_t mask)`  
*Enables the WDOG interrupt.*
- `uint16_t WDOG_GetStatusFlags (WDOG_Type *base)`  
*Gets the WDOG all reset status flags.*
- `void WDOG_ClearInterruptStatus (WDOG_Type *base, uint16_t mask)`  
*Clears the WDOG flag.*
- `static void WDOG_SetTimeoutValue (WDOG_Type *base, uint16_t timeoutCount)`  
*Sets the WDOG timeout value.*
- `static void WDOG_SetInterruptTimeoutValue (WDOG_Type *base, uint16_t timeoutCount)`  
*Sets the WDOG interrupt count timeout value.*
- `static void WDOG_DisablePowerDownEnable (WDOG_Type *base)`  
*Disable the WDOG power down enable bit.*
- `void WDOG_Refesh (WDOG_Type *base)`  
*Refreshes the WDOG timer.*

## 48.3 Data Structure Documentation

### 48.3.1 struct wdog\_work\_mode\_t

#### Data Fields

- `bool enableWait`  
*continue or suspend WDOG in wait mode*
- `bool enableStop`  
*continue or suspend WDOG in stop mode*
- `bool enableDebug`  
*continue or suspend WDOG in debug mode*

### 48.3.2 struct wdog\_config\_t

#### Data Fields

- `bool enableWdog`  
*Enables or disables WDOG.*
- `wdog_work_mode_t workMode`  
*Configures WDOG work mode in debug stop and wait mode.*
- `bool enableInterrupt`

- `uint16_t timeoutValue`  
*Timeout value.*
- `uint16_t interruptTimeValue`  
*Interrupt count timeout value.*
- `bool softwareResetExtension`  
*software reset extension*
- `bool enablePowerDown`  
*power down enable bit*
- `bool enableTimeOutAssert`  
*Enable WDOG\_B timeout assertion.*

## Field Documentation

(1) `bool wdog_config_t::enableTimeOutAssert`

## 48.4 Enumeration Type Documentation

### 48.4.1 enum \_wdog\_interrupt\_enable

This structure contains the settings for all of the WDOG interrupt configurations.

Enumerator

`kWDOG_InterruptEnable` WDOG timeout generates an interrupt before reset.

### 48.4.2 enum \_wdog\_status\_flags

This structure contains the WDOG status flags for use in the WDOG functions.

Enumerator

`kWDOG_RunningFlag` Running flag, set when WDOG is enabled.

`kWDOG_PowerOnResetFlag` Power On flag, set when reset is the result of a powerOnReset.

`kWDOG_TimeoutResetFlag` Timeout flag, set when reset is the result of a timeout.

`kWDOG_SoftwareResetFlag` Software flag, set when reset is the result of a software.

`kWDOG InterruptFlag` interrupt flag, whether interrupt has occurred or not

## 48.5 Function Documentation

### 48.5.1 void WDOG\_GetDefaultConfig ( `wdog_config_t * config` )

This function initializes the WDOG configuration structure to default values. The default values are as follows.

```
*   wdogConfig->enableWdog = true;
*   wdogConfig->workMode.enableWait = true;
*   wdogConfig->workMode.enableStop = false;
```

```
* wdogConfig->workMode.enableDebug = false;
* wdogConfig->enableInterrupt = false;
* wdogConfig->enablePowerdown = false;
* wdogConfig->resetExtension = flase;
* wdogConfig->timeoutValue = 0xFFU;
* wdogConfig->interruptTimeValue = 0x04u;
*
```

## Parameters

<i>config</i>	Pointer to the WDOG configuration structure.
---------------	--

## See Also

[wdog\\_config\\_t](#)

**48.5.2 void WDOG\_Init ( WDOG\_Type \* *base*, const wdog\_config\_t \* *config* )**

This function initializes the WDOG. When called, the WDOG runs according to the configuration.

This is an example.

```
* wdog_config_t config;
* WDOG_GetDefaultConfig(&config);
* config.timeoutValue = 0xffU;
* config->interruptTimeValue = 0x04u;
* WDOG_Init(wdog_base,&config);
*
```

## Parameters

<i>base</i>	WDOG peripheral base address
<i>config</i>	The configuration of WDOG

**48.5.3 void WDOG\_Deinit ( WDOG\_Type \* *base* )**

This function shuts down the WDOG. Watchdog Enable bit is a write one once only bit. It is not possible to clear this bit by a software write, once the bit is set. This bit(WDE) can be set/reset only in debug mode(exception).

**48.5.4 static void WDOG\_Enable ( WDOG\_Type \* *base* ) [inline], [static]**

This function writes a value into the WDOG\_WCR register to enable the WDOG. This is a write one once only bit. It is not possible to clear this bit by a software write, once the bit is set. only debug mode exception.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

#### 48.5.5 static void WDOG\_Disable ( WDOG\_Type \* *base* ) [inline], [static]

This function writes a value into the WDOG\_WCR register to disable the WDOG. This is a write one once only bit. It is not possible to clear this bit by a software write,once the bit is set. only debug mode exception

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

#### 48.5.6 static void WDOG\_TriggerSystemSoftwareReset ( WDOG\_Type \* *base* ) [inline], [static]

This function will write to the WCR[SRS] bit to trigger a software system reset. This bit will automatically resets to "1" after it has been asserted to "0". Note: Calling this API will reset the system right now, please using it with more attention.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

#### 48.5.7 static void WDOG\_TriggerSoftwareSignal ( WDOG\_Type \* *base* ) [inline], [static]

This function will write to the WCR[WDA] bit to trigger WDOG\_B signal assertion. The WDOG\_B signal can be routed to external pin of the chip, the output pin will turn to assertion along with WDOG\_B signal. Note: The WDOG\_B signal will remain assert until a power on reset occurred, so, please take more attention while calling it.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

**48.5.8 static void WDOG\_EnableInterrupts ( WDOG\_Type \* *base*, uint16\_t *mask* )  
[inline], [static]**

This bit is a write once only bit. Once the software does a write access to this bit, it will get locked and cannot be reprogrammed until the next system reset assertion

Parameters

<i>base</i>	WDOG peripheral base address
<i>mask</i>	The interrupts to enable The parameter can be combination of the following source if defined. <ul style="list-style-type: none"> <li>• kWDOG_InterruptEnable</li> </ul>

#### 48.5.9 `uint16_t WDOG_GetStatusFlags ( WDOG_Type * base )`

This function gets all reset status flags.

```
* uint16_t status;
* status = WDOG_GetStatusFlags (wdog_base);
*
```

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

Returns

State of the status flag: asserted (true) or not-asserted (false).

See Also

##### [\\_wdog\\_status\\_flags](#)

- true: a related status flag has been set.
- false: a related status flag is not set.

#### 48.5.10 `void WDOG_ClearInterruptStatus ( WDOG_Type * base, uint16_t mask )`

This function clears the WDOG status flag.

This is an example for clearing the interrupt flag.

```
*   WDOG_ClearStatusFlags (wdog_base, KWDOG_InterruptFlag);
*
```

Parameters

<i>base</i>	WDOG peripheral base address
<i>mask</i>	The status flags to clear. The parameter could be any combination of the following values. kWDOG_TimeoutFlag

#### 48.5.11 static void WDOG\_SetTimeoutValue ( WDOG\_Type \* *base*, uint16\_t *timeoutCount* ) [inline], [static]

This function sets the timeout value. This function writes a value into WCR registers. The time-out value can be written at any point of time but it is loaded to the counter at the time when WDOG is enabled or after the service routine has been performed.

Parameters

<i>base</i>	WDOG peripheral base address
<i>timeoutCount</i>	WDOG timeout value; count of WDOG clock tick.

#### 48.5.12 static void WDOG\_SetInterruptTimeoutValue ( WDOG\_Type \* *base*, uint16\_t *timeoutCount* ) [inline], [static]

This function sets the interrupt count timeout value. This function writes a value into WIC registers which are write-once. This field is write once only. Once the software does a write access to this field, it will get locked and cannot be reprogrammed until the next system reset assertion.

Parameters

<i>base</i>	WDOG peripheral base address
<i>timeoutCount</i>	WDOG timeout value; count of WDOG clock tick.

#### 48.5.13 static void WDOG\_DisablePowerDownEnable ( WDOG\_Type \* *base* ) [inline], [static]

This function disable the WDOG power down enable(PDE). This function writes a value into WMCR registers which are write-once. This field is write once only. Once software sets this bit it cannot be reset until the next system reset.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

#### 48.5.14 void WDOG\_Refresh ( **WDOG\_Type** \* *base* )

This function feeds the WDOG. This function should be called before the WDOG timer is in timeout. Otherwise, a reset is asserted.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

# Chapter 49

## XBARA: Inter-Peripheral Crossbar Switch

### 49.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Inter-Peripheral Crossbar Switch (XBARA) block of MCUXpresso SDK devices.

The XBARA peripheral driver configures the XBARA (Inter-Peripheral Crossbar Switch) and handles initialization and configuration of the XBARA module.

XBARA driver has two parts:

- Signal connection interconnects input and output signals.
- Active edge feature - Some of the outputs provide an active edge detection. If an active edge occurs, an interrupt or a DMA request can be called. APIs handle user callbacks for the interrupts. The driver also includes API for clearing and reading status bits.

### 49.2 Function

#### 49.2.1 XBARA Initialization

To initialize the XBARA driver, a state structure has to be passed into the initialization function. This block of memory keeps pointers to user's callback functions and parameters to these functions. The XBARA module is initialized by calling the [XBARA\\_Init\(\)](#) function.

#### 49.2.2 Call diagram

1. Call the "XBARA\_Init()" function to initialize the XBARA module.
2. Optionally, call the "XBARA\_SetSignalsConnection()" function to Set connection between the selected XBARA\_IN[\*] input and the XBARA\_OUT[\*] output signal. It connects the XBARA input to the selected XBARA output. A configuration structure of the "xbara\_input\_signal\_t" type and "xbara\_output\_signal\_t" type is required.
3. Call the "XBARA\_SetOutputSignalConfig" function to set the active edge features, such interrupts or DMA requests. A configuration structure of the "xbara\_control\_config\_t" type is required to point to structure that keeps configuration of control register.
4. Finally, the XBARA works properly.

### 49.3 Typical use case

#### Data Structures

- struct [xbara\\_control\\_config\\_t](#)  
*Defines the configuration structure of the XBARA control register.* [More...](#)

## Enumerations

- enum `xbara_active_edge_t` {
   
  `kXBARA_EdgeNone` = 0U,
   
  `kXBARA_EdgeRising` = 1U,
   
  `kXBARA_EdgeFalling` = 2U,
   
  `kXBARA_EdgeRisingAndFalling` = 3U }
   
*XBARA active edge for detection.*
- enum `xbara_request_t` {
   
  `kXBARA_RequestDisable` = 0U,
   
  `kXBARA_RequestDMAEnable` = 1U,
   
  `kXBARA_RequestInterruptEnable` = 2U }
   
*Defines the XBARA DMA and interrupt configurations.*
- enum `xbara_status_flag_t` {
   
  `kXBARA_EdgeDetectionOut0`,
   
  `kXBARA_EdgeDetectionOut1`,
   
  `kXBARA_EdgeDetectionOut2`,
   
  `kXBARA_EdgeDetectionOut3` }
   
*XBARA status flags.*

## XBARA functional Operation.

- void `XBARA_Init` (XBARA\_Type \*base)
   
*Initializes the XBARA module.*
- void `XBARA_Deinit` (XBARA\_Type \*base)
   
*Shuts down the XBARA module.*
- void `XBARA_SetSignalsConnection` (XBARA\_Type \*base, xbar\_input\_signal\_t input, xbar\_output\_signal\_t output)
   
*Sets a connection between the selected XBARA\_IN[\*] input and the XBARA\_OUT[\*] output signal.*
- uint32\_t `XBARA_GetStatusFlags` (XBARA\_Type \*base)
   
*Gets the active edge detection status.*
- void `XBARA_ClearStatusFlags` (XBARA\_Type \*base, uint32\_t mask)
   
*Clears the edge detection status flags of relative mask.*
- void `XBARA_SetOutputSignalConfig` (XBARA\_Type \*base, xbar\_output\_signal\_t output, const `xbara_control_config_t` \*controlConfig)
   
*Configures the XBARA control register.*

## 49.4 Data Structure Documentation

### 49.4.1 struct xbara\_control\_config\_t

This structure keeps the configuration of XBARA control register for one output. Control registers are available only for a few outputs. Not every XBARA module has control registers.

#### Data Fields

- `xbara_active_edge_t activeEdge`

- **xbara\_request\_t requestType**  
*Selects DMA/Interrupt request.*

**Field Documentation**

- (1) **xbara\_active\_edge\_t xbara\_control\_config\_t::activeEdge**
- (2) **xbara\_request\_t xbara\_control\_config\_t::requestType**

**49.5 Enumeration Type Documentation****49.5.1 enum xbara\_active\_edge\_t**

Enumerator

***kXBARA\_EdgeNone*** Edge detection status bit never asserts.

***kXBARA\_EdgeRising*** Edge detection status bit asserts on rising edges.

***kXBARA\_EdgeFalling*** Edge detection status bit asserts on falling edges.

***kXBARA\_EdgeRisingAndFalling*** Edge detection status bit asserts on rising and falling edges.

**49.5.2 enum xbara\_request\_t**

Enumerator

***kXBARA\_RequestDisable*** Interrupt and DMA are disabled.

***kXBARA\_RequestDMAEnable*** DMA enabled, interrupt disabled.

***kXBARA\_RequestInterruptEnable*** Interrupt enabled, DMA disabled.

**49.5.3 enum xbara\_status\_flag\_t**

This provides constants for the XBARA status flags for use in the XBARA functions.

Enumerator

***kXBARA\_EdgeDetectionOut0*** XBAR\_OUT0 active edge interrupt flag, sets when active edge detected.

***kXBARA\_EdgeDetectionOut1*** XBAR\_OUT1 active edge interrupt flag, sets when active edge detected.

***kXBARA\_EdgeDetectionOut2*** XBAR\_OUT2 active edge interrupt flag, sets when active edge detected.

***kXBARA\_EdgeDetectionOut3*** XBAR\_OUT3 active edge interrupt flag, sets when active edge detected.

## 49.6 Function Documentation

### 49.6.1 void XBARA\_Init ( XBARA\_Type \* *base* )

This function un-gates the XBARA clock.

Parameters

<i>base</i>	XBARA peripheral address.
-------------	---------------------------

#### 49.6.2 void XBARA\_Deinit ( XBARA\_Type \* *base* )

This function disables XBARA clock.

Parameters

<i>base</i>	XBARA peripheral address.
-------------	---------------------------

#### 49.6.3 void XBARA\_SetSignalsConnection ( XBARA\_Type \* *base*, xbar\_input\_signal\_t *input*, xbar\_output\_signal\_t *output* )

This function connects the XBARA input to the selected XBARA output. If more than one XBARA module is available, only the inputs and outputs from the same module can be connected.

Example:

```
XBARA_SetSignalsConnection(XBARA, kXBARA_InputPIT_TRG0, kXBARA_OutputDMAMUX18);
```

Parameters

<i>base</i>	XBARA peripheral address.
<i>input</i>	XBARA input signal.
<i>output</i>	XBARA output signal.

#### 49.6.4 uint32\_t XBARA\_GetStatusFlags ( XBARA\_Type \* *base* )

This function gets the active edge detect status of all XBARA\_OUTs. If the active edge occurs, the return value is asserted. When the interrupt or the DMA functionality is enabled for the XBARA\_OUTx, this field is 1 when the interrupt or DMA request is asserted and 0 when the interrupt or DMA request has been cleared.

Parameters

<i>base</i>	XBARA peripheral address.
-------------	---------------------------

Returns

the mask of these status flag bits.

#### 49.6.5 void XBARA\_ClearStatusFlags ( XBARA\_Type \* *base*, uint32\_t *mask* )

Parameters

<i>base</i>	XBARA peripheral address.
<i>mask</i>	the status flags to clear.

#### 49.6.6 void XBARA\_SetOutputSignalConfig ( XBARA\_Type \* *base*, xbar\_output\_signal\_t *output*, const xbara\_control\_config\_t \* *controlConfig* )

This function configures an XBARA control register. The active edge detection and the DMA/IRQ function on the corresponding XBARA output can be set.

Example:

```
xbara_control_config_t userConfig;
userConfig.activeEdge = kXBARA_EdgeRising;
userConfig.requestType = kXBARA_RequestInterruptEnable;
XBARA_SetOutputSignalConfig(XBARA, kXBARA_OutputDMAMUX18, &userConfig);
```

Parameters

<i>base</i>	XBARA peripheral address.
<i>output</i>	XBARA output number.
<i>controlConfig</i>	Pointer to structure that keeps configuration of control register.

# Chapter 50

## XBARB: Inter-Peripheral Crossbar Switch

### 50.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Inter-Peripheral Crossbar Switch (XBARB) block of MCUXpresso SDK devices.

The XBARB peripheral driver configures the XBARB (Inter-Peripheral Crossbar Switch) and handles initialization and configuration of the XBARB module.

XBARB driver has two parts:

- Signal connection interconnects input and output signals.

### 50.2 Function groups

#### 50.2.1 XBARB Initialization

To initialize the XBARB driver, a state structure has to be passed into the initialization function. This block of memory keeps pointers to user's callback functions and parameters to these functions. The XBARB module is initialized by calling the [XBARB\\_Init\(\)](#) function.

#### 50.2.2 Call diagram

1. Call the "XBARB\_Init()" function to initialize the XBARB module.
2. Optionally, call the "XBARB\_SetSignalsConnection()" function to Set connection between the selected XBARB\_IN[\*] input and the XBARB\_OUT[\*] output signal. It connects the XBARB input to the selected XBARB output. A configuration structure of the "xbarb\_input\_signal\_t" type and "xbarb\_output\_signal\_t" type is required.
3. Finally, the XBARB works properly.

### 50.3 Typical use case

#### XBARB functional Operation.

- void [XBARB\\_Init](#) (XBARB\_Type \*base)  
*Initializes the XBARB module.*
- void [XBARB\\_Deinit](#) (XBARB\_Type \*base)  
*Shuts down the XBARB module.*
- void [XBARB\\_SetSignalsConnection](#) (XBARB\_Type \*base, xbar\_input\_signal\_t input, xbar\_output\_signal\_t output)  
*Configures a connection between the selected XBARB\_IN[\*] input and the XBARB\_OUT[\*] output signal.*

## 50.4 Function Documentation

### 50.4.1 void XBARB\_Init ( XBARB\_Type \* *base* )

This function un-gates the XBARB clock.

Parameters

<i>base</i>	XBARB peripheral address.
-------------	---------------------------

#### 50.4.2 void XBARB\_Deinit ( XBARB\_Type \* *base* )

This function disables XBARB clock.

Parameters

<i>base</i>	XBARB peripheral address.
-------------	---------------------------

#### 50.4.3 void XBARB\_SetSignalsConnection ( XBARB\_Type \* *base*, xbar\_input\_signal\_t *input*, xbar\_output\_signal\_t *output* )

This function configures which XBARB input is connected to the selected XBARB output. If more than one XBARB module is available, only the inputs and outputs from the same module can be connected.

Parameters

<i>base</i>	XBARB peripheral address.
<i>input</i>	XBARB input signal.
<i>output</i>	XBARB output signal.

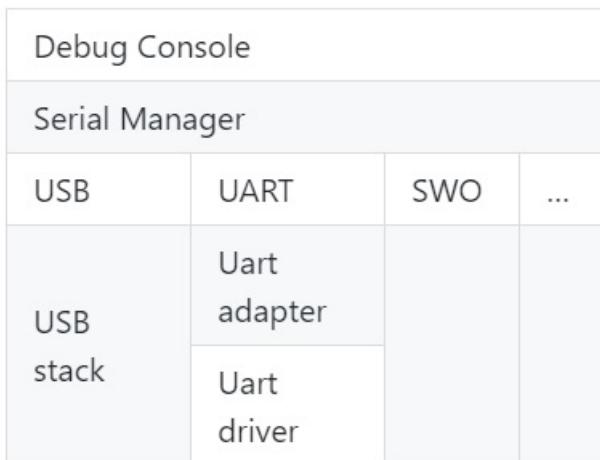
# Chapter 51

## Debug Console

### 51.1 Overview

This chapter describes the programming interface of the debug console driver.

The debug console enables debug log messages to be output via the specified peripheral with frequency of the peripheral source clock and base address at the specified baud rate. Additionally, it provides input and output functions to scan and print formatted data. The below picture shows the layout of debug console.



**Debug console overview**

### 51.2 Function groups

#### 51.2.1 Initialization

To initialize the debug console, call the [DbgConsole\\_Init\(\)](#) function with these parameters. This function automatically enables the module and the clock.

```
status_t DbgConsole_Init(uint8_t instance, uint32_t baudRate,  
                         serial_port_type_t device, uint32_t clkSrcFreq);
```

Select the supported debug console hardware device type, such as

```
typedef enum _serial_port_type  
{  
    kSerialPort_Uart = 1U,  
    kSerialPort_UsbCdc,  
    kSerialPort_Swo,  
} serial_port_type_t;
```

After the initialization is successful, stdout and stdin are connected to the selected peripheral. This example shows how to call the [DbgConsole\\_Init\(\)](#) given the user configuration structure.

```
DbgConsole_Init(BOARD_DEBUG_UART_INSTANCE, BOARD_DEBUG_UART_BAUDRATE, BOARD_DEBUG_UART_TYPE,
                 BOARD_DEBUG_UART_CLK_FREQ);
```

### 51.2.2 Advanced Feature

The debug console provides input and output functions to scan and print formatted data.

- Support a format specifier for PRINTF following this prototype " %[flags][width][.precision][length]specifier", which is explained below

flags	Description
-	Left-justified within the given field width. Right-justified is the default.
+	Forces to precede the result with a plus or minus sign (+ or -) even for positive numbers. By default, only negative numbers are preceded with a - sign.
(space)	If no sign is written, a blank space is inserted before the value.
#	Used with o, x, or X specifiers the value is preceded with 0, 0x, or 0X respectively for values other than zero. Used with e, E and f, it forces the written output to contain a decimal point even if no digits would follow. By default, if no digits follow, no decimal point is written. Used with g or G the result is the same as with e or E but trailing zeros are not removed.
0	Left-pads the number with zeroes (0) instead of spaces, where padding is specified (see width sub-specifier).

Width	Description
(number)	A minimum number of characters to be printed. If the value to be printed is shorter than this number, the result is padded with blank spaces. The value is not truncated even if the result is larger.
*	The width is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

.precision	Description
.number	For integer specifiers (d, i, o, u, x, X) precision specifies the minimum number of digits to be written. If the value to be written is shorter than this number, the result is padded with leading zeros. The value is not truncated even if the result is longer. A precision of 0 means that no character is written for the value 0. For e, E, and f specifiers this is the number of digits to be printed after the decimal point. For g and G specifiers This is the maximum number of significant digits to be printed. For s this is the maximum number of characters to be printed. By default, all characters are printed until the ending null character is encountered. For c type it has no effect. When no precision is specified, the default is 1. If the period is specified without an explicit value for precision, 0 is assumed.
.*	The precision is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

length	Description
Do not support	

specifier	Description
d or i	Signed decimal integer
f	Decimal floating point
F	Decimal floating point capital letters
x	Unsigned hexadecimal integer
X	Unsigned hexadecimal integer capital letters
o	Signed octal
b	Binary value
p	Pointer address
u	Unsigned decimal integer
c	Character
s	String of characters
n	Nothing printed

specifier	Description
-----------	-------------

- Support a format specifier for SCANF following this prototype " %[\*][width][length]specifier", which is explained below

*	Description
	An optional starting asterisk indicates that the data is to be read from the stream but ignored. In other words, it is not stored in the corresponding argument.

width	Description
	This specifies the maximum number of characters to be read in the current reading operation.

length	Description
hh	The argument is interpreted as a signed character or unsigned character (only applies to integer specifiers: i, d, o, u, x, and X).
h	The argument is interpreted as a short integer or unsigned short integer (only applies to integer specifiers: i, d, o, u, x, and X).
l	The argument is interpreted as a long integer or unsigned long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
ll	The argument is interpreted as a long long integer or unsigned long long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
L	The argument is interpreted as a long double (only applies to floating point specifiers: e, E, f, g, and G).
j or z or t	Not supported

specifier	Qualifying Input	Type of argument
c	Single character: Reads the next character. If a width different from 1 is specified, the function reads width characters and stores them in the successive locations of the array passed as argument. No null character is appended at the end.	char *
i	Integer: : Number optionally preceded with a + or - sign	int *
d	Decimal integer: Number optionally preceded with a + or - sign	int *
a, A, e, E, f, F, g, G	Floating point: Decimal number containing a decimal point, optionally preceded by a + or - sign and optionally followed by the e or E character and a decimal number. Two examples of valid entries are -732.103 and 7.12e4	float *
o	Octal Integer:	int *
s	String of characters. This reads subsequent characters until a white space is found (white space characters are considered to be blank, newline, and tab).	char *
u	Unsigned decimal integer.	unsigned int *

The debug console has its own printf/scanf/putchar/getchar functions which are defined in the header file.

```
int DbgConsole_Printf(const char *fmt_s, ...);
int DbgConsole_Putchar(int ch);
int DbgConsole_Scanf(char *fmt_ptr, ...);
int DbgConsole_Getchar(void);
```

This utility supports selecting toolchain's printf/scanf or the MCUXpresso SDK printf/scanf.

```
#if SDK_DEBUGCONSOLE == DEBUGCONSOLE_DISABLE /* Disable debug console */
#define PRINTF
#define SCANF
#define PUTCHAR
#define GETCHAR
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_SDK /* Select printf, scanf, putchar, getchar of SDK
```

```

version. */
#define PRINTF DbgConsole_Printf
#define SCANF DbgConsole_Scanf
#define PUTCHAR DbgConsole_Putchar
#define GETCHAR DbgConsole_Getchar
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN /* Select printf, scanf, putchar, getchar of
toolchain. */
#define PRINTF printf
#define SCANF scanf
#define PUTCHAR putchar
#define GETCHAR getchar
#endif /* SDK_DEBUGCONSOLE */

```

### 51.2.3 SDK\_DEBUGCONSOLE and SDK\_DEBUGCONSOLE\_UART

There are two macros `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` added to configure `PRINTF` and low level output peripheral.

- The macro `SDK_DEBUGCONSOLE` is used for frontend. Whether debug console redirect to toolchain or SDK or disabled, it decides which is the frontend of the debug console, Tool chain or SDK. The function can be set by the macro `SDK_DEBUGCONSOLE`.
- The macro `SDK_DEBUGCONSOLE_UART` is used for backend. It is used to decide whether provide low level IO implementation to toolchain printf and scanf. For example, within MCUXpresso, if the macro `SDK_DEBUGCONSOLE_UART` is defined, `_sys_write` and `_sys_read` will be used when `_REDLIB_` is defined; `_write` and `_read` will be used in other cases. The macro does not specifically refer to the peripheral "UART". It refers to the external peripheral similar to UART, like as USB CDC, UART, SWO, etc. So if the macro `SDK_DEBUGCONSOLE_UART` is not defined when tool-chain printf is calling, the semihosting will be used.

The following matrix show the effects of `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` on `PRINTF` and `printf`. The green mark is the default setting of the debug console.

<code>SDK_DEBUGCONSOLE</code>	<code>SDK_DEBUGCONSOLE_UART</code>	<code>PRINTF</code>	<code>printf</code>
<code>DEBUGCONSOLE_- REDIRECT_TO_SDK</code>	defined	Low level peripheral*	Low level peripheral
<code>DEBUGCONSOLE_- REDIRECT_TO_SDK</code>	undefined	Low level peripheral*	semihost
<code>DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN</code>	defined	Low level peripheral*	Low level peripheral
<code>DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN</code>	undefined	semihost	semihost
<code>DEBUGCONSOLE_- DISABLE</code>	defined	No output	Low level peripheral
<code>DEBUGCONSOLE_- DISABLE</code>	undefined	No output	semihost

<b>SDK_DEBUGCONSOLE</b>	<b>SDK_DEBUGCONSOLE_UART</b>	<b>PRINTF</b>	<b>printf</b>
-------------------------	------------------------------	---------------	---------------

\* the **low level peripheral** could be USB CDC, UART, or SWO, and so on.

### 51.3 Typical use case

#### Some examples use the PUTCHAR & GETCHAR function

```
ch = GETCHAR();
PUTCHAR(ch);
```

#### Some examples use the PRINTF function

Statement prints the string format.

```
PRINTF("%s %s\r\n", "Hello", "world!");
```

Statement prints the hexadecimal format/

```
PRINTF("0x%02X hexadecimal number equivalents 255", 255);
```

Statement prints the decimal floating point and unsigned decimal.

```
PRINTF("Execution timer: %s\n\rTime: %u ticks %2.5f milliseconds\n\rDONE\n\r", "1 day", 86400, 86.4);
```

#### Some examples use the SCANF function

```
PRINTF("Enter a decimal number: ");
SCANF("%d", &i);
PRINTF("\r\nYou have entered %d.\r\n", i, i);
PRINTF("Enter a hexadecimal number: ");
SCANF("%x", &i);
PRINTF("\r\nYou have entered 0x%X (%d).\r\n", i, i);
```

#### Print out failure messages using MCUXpresso SDK \_\_assert\_func:

```
void __assert_func(const char *file, int line, const char *func, const char *failedExpr)
{
    PRINTF("ASSERT ERROR \" %s \": file \"%s\" Line \"%d\" function name \"%s\" \n", failedExpr, file
           , line, func);
    for (;;) {
    }
}
```

**Note:**

To use 'printf' and 'scanf' for GNUMC Base, add file '**fsl\_sbrk.c**' in path: ..\{package}\devices\{subset}\utilities\fsl\\_sbrk.c to your project.

**Modules**

- [SWO](#)
- [Semihosting](#)
- [debug console configuration](#)

*The configuration is used for debug console only.*

**Macros**

- #define [DEBUGCONSOLE\\_REDIRECT\\_TO\\_TOOLCHAIN](#) 0U  
*Definition select redirect toolchain printf, scanf to uart or not.*
- #define [DEBUGCONSOLE\\_REDIRECT\\_TO\\_SDK](#) 1U  
*Select SDK version printf, scanf.*
- #define [DEBUGCONSOLE\\_DISABLE](#) 2U  
*Disable debugconsole function.*
- #define [SDK\\_DEBUGCONSOLE DEBUGCONSOLE\\_REDIRECT\\_TO\\_SDK](#)  
*Definition to select sdk or toolchain printf, scanf.*
- #define [PRINTF DbgConsole\\_Printf](#)  
*Definition to select redirect toolchain printf, scanf to uart or not.*

**Variables**

- [serial\\_handle\\_t g\\_serialHandle](#)  
*serial manager handle*

**Initialization**

- [status\\_t DbgConsole\\_Init](#) (uint8\_t instance, uint32\_t baudRate, [serial\\_port\\_type\\_t](#) device, uint32\_t clkSrcFreq)  
*Initializes the peripheral used for debug messages.*
- [status\\_t DbgConsole\\_Deinit](#) (void)  
*De-initializes the peripheral used for debug messages.*
- [status\\_t DbgConsole\\_EnterLowpower](#) (void)  
*Prepares to enter low power consumption.*
- [status\\_t DbgConsole\\_ExitLowpower](#) (void)  
*Restores from low power consumption.*
- int [DbgConsole\\_Printf](#) (const char \*fmt\_s,...)  
*Writes formatted output to the standard output stream.*
- int [DbgConsole\\_Vprintf](#) (const char \*fmt\_s, va\_list formatStringArg)  
*Writes formatted output to the standard output stream.*
- int [DbgConsole\\_Putchar](#) (int ch)  
*Writes a character to stdout.*
- int [DbgConsole\\_Scanf](#) (char \*fmt\_s,...)  
*Reads formatted data from the standard input stream.*
- int [DbgConsole\\_Getchar](#) (void)

- *Reads a character from standard input.*  
• int [DbgConsole\\_BlockingPrintf](#) (const char \*fmt\_s,...)  
*Writes formatted output to the standard output stream with the blocking mode.*
- int [DbgConsole\\_BlockingVprintf](#) (const char \*fmt\_s, va\_list formatStringArg)  
*Writes formatted output to the standard output stream with the blocking mode.*
- status\_t [DbgConsole\\_Flush](#) (void)  
*Debug console flush.*
- status\_t [DbgConsole\\_TryGetchar](#) (char \*ch)  
*Debug console try to get char This function provides a API which will not block current task, if character is available return it, otherwise return fail.*

## 51.4 Macro Definition Documentation

### 51.4.1 #define DEBUGCONSOLE\_REDIRECT\_TO\_TOOLCHAIN 0U

Select toolchain printf and scanf.

### 51.4.2 #define DEBUGCONSOLE\_REDIRECT\_TO\_SDK 1U

### 51.4.3 #define DEBUGCONSOLE\_DISABLE 2U

### 51.4.4 #define SDK\_DEBUGCONSOLE DEBUGCONSOLE\_REDIRECT\_TO\_SDK

The macro only support to be redefined in project setting.

### 51.4.5 #define PRINTF DbgConsole\_Printf

if SDK\_DEBUGCONSOLE defined to 0,it represents select toolchain printf, scanf. if SDK\_DEBUGCONSOLE defined to 1,it represents select SDK version printf, scanf. if SDK\_DEBUGCONSOLE defined to 2,it represents disable debugconsole function.

## 51.5 Function Documentation

### 51.5.1 status\_t DbgConsole\_Init ( uint8\_t instance, uint32\_t baudRate, serial\_port\_type\_t device, uint32\_t clkSrcFreq )

Call this function to enable debug log messages to be output via the specified peripheral initialized by the serial manager module. After this function has returned, stdout and stdin are connected to the selected peripheral.

## Parameters

<i>instance</i>	The instance of the module. If the device is kSerialPort_Uart, the instance is UART peripheral instance. The UART hardware peripheral type is determined by UART adapter. For example, if the instance is 1, if the lpuart_adapter.c is added to the current project, the UART peripheral is LPUART1. If the uart_adapter.c is added to the current project, the UART peripheral is UART1.
<i>baudRate</i>	The desired baud rate in bits per second.
<i>device</i>	Low level device type for the debug console, can be one of the following. <ul style="list-style-type: none"> <li>• kSerialPort_Uart,</li> <li>• kSerialPort_UsbCdc</li> </ul>
<i>clkSrcFreq</i>	Frequency of peripheral source clock.

## Returns

Indicates whether initialization was successful or not.

## Return values

<i>kStatus_Success</i>	Execution successfully
------------------------	------------------------

**51.5.2 status\_t DbgConsole\_Deinit ( void )**

Call this function to disable debug log messages to be output via the specified peripheral initialized by the serial manager module.

## Returns

Indicates whether de-initialization was successful or not.

**51.5.3 status\_t DbgConsole\_EnterLowpower ( void )**

This function is used to prepare to enter low power consumption.

## Returns

Indicates whether de-initialization was successful or not.

**51.5.4 status\_t DbgConsole\_ExitLowpower ( void )**

This function is used to restore from low power consumption.

Returns

Indicates whether de-initialization was successful or not.

**51.5.5 int DbgConsole\_Printf ( const char \* *fmt\_s*, ... )**

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

**51.5.6 int DbgConsole\_Vprintf ( const char \* *fmt\_s*, va\_list *formatStringArg* )**

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatString-Arg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

**51.5.7 int DbgConsole\_Putchar ( int *ch* )**

Call this function to write a character to stdout.

Parameters

<i>ch</i>	Character to be written.
-----------	--------------------------

Returns

Returns the character written.

### 51.5.8 int DbgConsole\_Scanf ( char \* *fmt\_s*, ... )

Call this function to read formatted data from the standard input stream.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the DEBUG\_CONSOLE\_TRANSFER\_NON\_B-LOCKING is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function DbgConsole\_TryGetchar to get the input char.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of fields successfully converted and assigned.

### 51.5.9 int DbgConsole\_Getchar ( void )

Call this function to read a character from standard input.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the DEBUG\_CONSOLE\_TRANSFER\_NON\_B-LOCKING is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function DbgConsole\_TryGetchar to get the input char.

Returns

Returns the character read.

**51.5.10 int DbgConsole\_BlockingPrintf ( const char \* *fmt\_s*, ... )**

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG\_CONSOLE\_TRANSFER\_NON\_BLOCKING set or not. The function could be used in system ISR mode with DEBUG\_CONSOLE\_TRANSFER\_NON\_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

**51.5.11 int DbgConsole\_BlockingVprintf ( const char \* *fmt\_s*, va\_list *formatStringArg* )**

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG\_CONSOLE\_TRANSFER\_NON\_BLOCKING set or not. The function could be used in system ISR mode with DEBUG\_CONSOLE\_TRANSFER\_NON\_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatString-Arg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

**51.5.12 status\_t DbgConsole\_Flush ( void )**

Call this function to wait the tx buffer empty. If interrupt transfer is using, make sure the global IRQ is enable before call this function This function should be called when 1, before enter power down mode 2, log is required to print to terminal immediately

Returns

Indicates whether wait idle was successful or not.

51.5.13 **status\_t DbgConsole\_TryGetchar ( char \* *ch* )**

### Parameters

<i>ch</i>	the address of char to receive
-----------	--------------------------------

### Returns

Indicates get char was successful or not.

## 51.6 debug console configuration

The configuration is used for debug console only.

### 51.6.1 Overview

Please note, it is not sued for debug console lite.

#### Macros

- `#define DEBUG_CONSOLE_TRANSMIT_BUFFER_LEN (512U)`  
*If Non-blocking mode is needed, please define it at project setting, otherwise blocking mode is the default transfer mode.*
- `#define DEBUG_CONSOLE_RECEIVE_BUFFER_LEN (1024U)`  
*define the receive buffer length which is used to store the user input, buffer is enabled automatically when non-blocking transfer is using, This value will affect the RAM's ultilization, should be set per paltform's capability and software requirement.*
- `#define DEBUG_CONSOLE_TX_RELIABLE_ENABLE (1U)`  
*Whether enable the reliable TX function If the macro is zero, the reliable TX function of the debug console is disabled.*
- `#define DEBUG_CONSOLE_RX_ENABLE (1U)`  
*Whether enable the RX function If the macro is zero, the receive function of the debug console is disabled.*
- `#define DEBUG_CONSOLE_PRINTF_MAX_LOG_LEN (128U)`  
*define the MAX log length debug console support , that is when you call printf("log", x);, the log length can not bigger than this value.*
- `#define DEBUG_CONSOLE_SCANF_MAX_LOG_LEN (20U)`  
*define the buffer support buffer scanf log length, that is when you call scanf("log", &x);, the log length can not bigger than this value.*
- `#define DEBUG_CONSOLE_SYNCHRONIZATION_BM 0`  
*Debug console synchronization User should not change these macro for synchronization mode, but add the corresponding synchronization mechanism per different software environment.*
- `#define DEBUG_CONSOLE_SYNCHRONIZATION_FREERTOS 1`  
*synchronization for freertos software*
- `#define DEBUG_CONSOLE_SYNCHRONIZATION_MODE DEBUG_CONSOLE_SYNCHRONIZATION_BM`  
*RTOS synchronization mechanism disable If not defined, default is enable, to avoid multitask log print mess.*
- `#define DEBUG_CONSOLE_ENABLE_ECHO_FUNCTION 0`  
*echo function support If you want to use the echo function,please define DEBUG\_CONSOLE\_ENABLE\_ECHO at your project setting.*
- `#define BOARD_USE_VIRTUALCOM 0U`  
*Definition to select virtual com(USB CDC) as the debug console.*

## 51.6.2 Macro Definition Documentation

### 51.6.2.1 #define DEBUG\_CONSOLE\_TRANSMIT\_BUFFER\_LEN (512U)

Warning: If you want to use non-blocking transfer, please make sure the corresponding IO interrupt is enable, otherwise there is no output. And non-blocking is combine with buffer, no matter bare-metal or rtos. Below shows how to configure in your project if you want to use non-blocking mode. For IAR, right click project and select "Options", define it in "C/C++ Compiler->Preprocessor->Defined symbols". For KEIL, click "Options for Target...", define it in "C/C++->Preprocessor Symbols->Define". For ARM-GCC, open CmakeLists.txt and add the following lines, "SET(CMAKE\_C\_FLAGS\_DEBUG "\${CMAKE\_C\_FLAGS\_DEBUG} -DDEBUG\_CONSOLE\_TRANSFER\_NON\_BLOCKING")" for debug target. "SET(CMAKE\_C\_FLAGS\_RELEASE "\${CMAKE\_C\_FLAGS\_RELEASE} -DDEBUG\_CONSOLE\_TRANSFER\_NON\_BLOCKING")" for release target. For MCUXpresso, right click project and select "Properties", define it in "C/C++ Build->Settings->MCU C Complier->Preprocessor".

define the transmit buffer length which is used to store the multi task log, buffer is enabled automatically when non-blocking transfer is using, This value will affect the RAM's utilization, should be set per platform's capability and software requirement. If it is configured too small, log maybe missed , because the log will not be buffered if the buffer is full, and the print will return immediately with -1. And this value should be multiple of 4 to meet memory alignment.

### 51.6.2.2 #define DEBUG\_CONSOLE\_RECEIVE\_BUFFER\_LEN (1024U)

If it is configured too small, log maybe missed, because buffer will be overwritten if buffer is too small. And this value should be multiple of 4 to meet memory alignment.

### 51.6.2.3 #define DEBUG\_CONSOLE\_TX\_RELIABLE\_ENABLE (1U)

When the macro is zero, the string of PRINTF will be thrown away after the transmit buffer is full.

### 51.6.2.4 #define DEBUG\_CONSOLE\_PRINTF\_MAX\_LOG\_LEN (128U)

This macro decide the local log buffer length, the buffer locate at stack, the stack maybe overflow if the buffer is too big and current task stack size not big enough.

### 51.6.2.5 #define DEBUG\_CONSOLE\_SCANF\_MAX\_LOG\_LEN (20U)

As same as the DEBUG\_CONSOLE\_BUFFER\_PRINTF\_MAX\_LOG\_LEN.

#### 51.6.2.6 #define DEBUG\_CONSOLE\_SYNCHRONIZATION\_BM 0

Such as, if another RTOS is used, add: #define DEBUG\_CONSOLE\_SYNCHRONIZATION\_XXXX 3 in this configuration file and implement the synchronization in fsl.log.c.

synchronization for baremetal software

#### 51.6.2.7 #define DEBUG\_CONSOLE\_SYNCHRONIZATION\_MODE DEBUG\_CONSOLE\_SYNCHRONIZATION\_BM

If other RTOS is used, you can implement the RTOS's specific synchronization mechanism in fsl.log.c If synchronization is disabled, log maybe messed on terminal.

#### 51.6.2.8 #define BOARD\_USE\_VIRTUALCOM 0U

## 51.7 Semihosting

Semihosting is a mechanism for ARM targets to communicate input/output requests from application code to a host computer running a debugger. This mechanism can be used, for example, to enable functions in the C library, such as `printf()` and `scanf()`, to use the screen and keyboard of the host rather than having a screen and keyboard on the target system.

### 51.7.1 Guide Semihosting for IAR

**NOTE:** After the setting both "printf" and "scanf" are available for debugging, if you want use PRINTF with semihosting, please make sure the `SDK_DEBUGCONSOLE` is `DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN`.

#### Step 1: Setting up the environment

1. To set debugger options, choose Project>Options. In the Debugger category, click the Setup tab.
2. Select Run to main and click OK. This ensures that the debug session starts by running the main function.
3. The project is now ready to be built.

#### Step 2: Building the project

1. Compile and link the project by choosing Project>Make or F7.
2. Alternatively, click the Make button on the tool bar. The Make command compiles and links those files that have been modified.

#### Step 3: Starting semihosting

1. Choose "Semihosting\_IAR" project -> "Options" -> "Debugger" -> "J-Link/J-Trace".
2. Choose tab "J-Link/J-Trace" -> "Connection" tab -> "SWD".
3. Choose tab "General Options" -> "Library Configurations", select Semihosted, select Via semihosting. Please Make sure the `SDK_DEBUGCONSOLE_UART` is not defined in project settings.
4. Start the project by choosing Project>Download and Debug.
5. Choose View>Terminal I/O to display the output from the I/O operations.

### 51.7.2 Guide Semihosting for Keil µVision

**NOTE:** Semihosting is not support by MDK-ARM, use the retargeting functionality of MDK-ARM instead.

### 51.7.3 Guide Semihosting for MCUXpresso IDE

#### Step 1: Setting up the environment

1. To set debugger options, choose Project>Properties. select the setting category.
2. Select Tool Settings, unfold MCU C Compile.
3. Select Preprocessor item.
4. Set SDK\_DEBUGCONSOLE=0, if set SDK\_DEBUGCONSOLE=1, the log will be redirect to the UART.

#### Step 2: Building the project

1. Compile and link the project.

#### Step 3: Starting semihosting

1. Download and debug the project.
2. When the project runs successfully, the result can be seen in the Console window.

Semihosting can also be selected through the "Quick settings" menu in the left bottom window, Quick settings->SDK Debug Console->Semihost console.

### 51.7.4 Guide Semihosting for ARMGCC

#### Step 1: Setting up the environment

1. Turn on "J-LINK GDB Server" -> Select suitable "Target device" -> "OK".
2. Turn on "PuTTY". Set up as follows.
  - "Host Name (or IP address)" : localhost
  - "Port" :2333
  - "Connection type" : Telet.
  - Click "Open".
3. Increase "Heap/Stack" for GCC to 0x2000:

#### Add to "CMakeLists.txt"

```
SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} --defsym=__stack_size__=0x2000")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --defsym=__stack_size__=0x2000")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --defsym=__heap_size__=0x2000")
SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} --defsym=__heap_size__=0x2000")
```

## Step 2: Building the project

1. Change "CMakeLists.txt":

```
Change "SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} -specs=nano.specs")"
to "SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} -specs=rdimon.specs")"
```

### Replace paragraph

```
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fno-common")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -ffunction-sections")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fdata-sections")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -ffreestanding")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fno-builtin")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -mthumb")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -mapcs")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --gc-sections")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -static")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -z")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} muldefs")
```

### To

```
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --specs=rdimon.specs ")
```

### Remove

```
target_link_libraries(semihosting_ARMGCC.elf debug nosys)
```

2. Run "build\_debug.bat" to build project

### Step 3: Starting semihosting

1. Download the image and set as follows.

```
cd D:\mcu-sdk-2.0-origin\boards\twrk64f120m\driver_examples\semihosting\armgcc\debug
d:
C:\PROGRA~2\GNUTOO~1\4BD65~1.920\bin\arm-none-eabi-gdb.exe
target remote localhost:2331
monitor reset
monitor semihosting enable
monitor semihosting thumbSWI 0xAB
monitor semihosting IOClient 1
monitor flash device = MK64FN1M0xxxx12
load semihosting_ARMGCC.elf
monitor reg pc = (0x00000004)
monitor reg sp = (0x00000000)
continue
```

2. After the setting, press "enter". The PuTTY window now shows the printf() output.

## 51.8 SWO

Serial wire output is a mechanism for ARM targets to output signal from core through a single pin. Some IDEs also support SWO, such IAR and KEIL, both input and output are supported, see below for details.

### 51.8.1 Guide SWO for SDK

**NOTE:** After the setting both "printf" and "PRINTF" are available for debugging, JlinkSWOViewer can be used to capture the output log.

#### Step 1: Setting up the environment

1. Define SERIAL\_PORT\_TYPE\_SWO in your project settings.
2. Prepare code, the port and baudrate can be decided by application, clkSrcFreq should be mcu core clock frequency:

```
DbgConsole_Init(instance, baudRate, kSerialPort_Swo, clkSrcFreq);
```

3. Use PRINTF or printf to print some thing in application.

#### Step 2: Building the project

#### Step 3: Download and run project

### 51.8.1.1 Guide SWO for IAR

**NOTE:** After the setting both "printf" and "scanf" are available for debugging.

#### Step 1: Setting up the environment

1. Choose project -> "Options" -> "Debugger" -> "J-Link/J-Trace".
2. Choose tab "J-Link/J-Trace" -> "Connection" tab -> "SWD".
3. Choose tab "General Options" -> "Library Configurations", select Semihosted, select Via SWO.
4. To configure the hardware's generation of trace data, click the SWO Configuration button available in the SWO Configuration dialog box. The value of the CPU clock option must reflect the frequency of the CPU clock speed at which the application executes. Note also that the settings you make are preserved between debug sessions. To decrease the amount of transmissions on the communication channel, you can disable the Timestamp option. Alternatively, set a lower rate for PC Sampling or use a higher SWO clock frequency.
5. Open the SWO Trace window from J-LINK, and click the Activate button to enable trace data collection.
6. There are three cases for this SDK\_DEBUGCONSOLE\_UART whether or not defined. a: if use uppercase PRINTF to output log, The SDK\_DEBUGCONSOLE\_UART defined or not defined will not effect debug function. b: if use lowercase printf to output log and defined SDK\_DEBUGCONSOLE\_UART to zero, then debug function ok. c: if use lowercase printf to output log and defined SDK\_DEBUGCONSOLE\_UART to one, then debug function ok.

**NOTE:** Case a or c only apply at example which enable swo function, the SDK\_DEBUGCONSOLE\_UART definition in fsl\_debug\_console.h. For case a and c, Do and not do the above third step will be not affect function.

1. Start the project by choosing Project>Download and Debug.

### **Step 2: Building the project**

### **Step 3: Starting swo**

1. Download and debug application.
2. Choose View -> Terminal I/O to display the output from the I/O operations.
3. Run application.

## **51.8.2 Guide SWO for Keil µVision**

**NOTE:** After the setting both "printf" and "scanf" are available for debugging.

### **Step 1: Setting up the environment**

1. There are three cases for this SDK\_DEBUGCONSOLE\_UART whether or not defined. a: if use uppercase PRINTF to output log, the SDK\_DEBUGCONSOLE\_UART definition does not affect the functionality and skip the second step directly. b: if use lowercase printf to output log and defined SDK\_DEBUGCONSOLE\_UART to zero, then start the second step. c: if use lowercase printf to output log and defined SDK\_DEBUGCONSOLE\_UART to one, then skip the second step directly.

**NOTE:** Case a or c only apply at example which enable swo function, the SDK\_DEBUGCONSOLE\_UART definition in fsl\_debug\_console.h.

1. In menu bar, click Management Run-Time Environment icon, select Compiler, unfold I/O, enable STDERR/STDIN/STDOUT and set the variant to ITM.
2. Open Project>Options for target or using Alt+F7 or click.
3. Select “Debug” tab, select “J-Link/J-Trace Cortex” and click “Setting button”.
4. Select “Debug” tab and choose Port:SW, then select “Trace” tab, choose “Enable” and click OK, please make sure the Core clock is set correctly, enable autodetect max SWO clk, enable ITM Stimulus Ports 0.

### **Step 3: Building the project**

1. Compile and link the project by choosing Project>Build Target or using F7.

### **Step 4: Run the project**

1. Choose “Debug” on menu bar or Ctrl F5.
2. In menu bar, choose “Serial Window” and click to “Debug (printf) Viewer”.
3. Run line by line to see result in Console Window.

### 51.8.3 Guide SWO for MCUXpresso IDE

**NOTE:** MCUX support SWO for LPC-Link2 debug probe only.

### 51.8.4 Guide SWO for ARMGCC

**NOTE:** ARMGCC has no library support SWO.

# Chapter 52

## Notification Framework

### 52.1 Overview

This section describes the programming interface of the Notifier driver.

### 52.2 Notifier Overview

The Notifier provides a configuration dynamic change service. Based on this service, applications can switch between pre-defined configurations. The Notifier enables drivers and applications to register callback functions to this framework. Each time that the configuration is changed, drivers and applications receive a notification and change their settings. To simplify, the Notifier only supports the static callback registration. This means that, for applications, all callback functions are collected into a static table and passed to the Notifier.

These are the steps for the configuration transition.

1. Before configuration transition, the Notifier sends a "BEFORE" message to the callback table. When this message is received, IP drivers should check whether any current processes can be stopped and stop them. If the processes cannot be stopped, the callback function returns an error.  
The Notifier supports two types of transition policies, a graceful policy and a forceful policy. When the graceful policy is used, if some callbacks return an error while sending a "BEFORE" message, the configuration transition stops and the Notifier sends a "RECOVER" message to all drivers that have stopped. Then, these drivers can recover the previous status and continue to work. When the forceful policy is used, drivers are stopped forcefully.
2. After the "BEFORE" message is processed successfully, the system switches to the new configuration.
3. After the configuration changes, the Notifier sends an "AFTER" message to the callback table to notify drivers that the configuration transition is finished.

This example shows how to use the Notifier in the Power Manager application.

```
#include "fsl_notifier.h"

// Definition of the Power Manager callback.
status_t callback0(notifier_notification_block_t *notify, void *data)
{
    status_t ret = kStatus_Success;

    ...
    ...

    return ret;
}
// Definition of the Power Manager user function.
status_t APP_PowerModeSwitch(notifier_user_config_t *targetConfig, void *
    userData)
```

```

{
    ...
    ...
    ...
}

...
...
...
...
...
...
// Main function.
int main(void)
{
    // Define a notifier handle.
    notifier_handle_t powerModeHandle;

    // Callback configuration.
    user_callback_data_t callbackData0;

    notifier_callback_config_t callbackCfg0 = {callback0,
        kNOTIFIER_CallbackBeforeAfter,
        (void *)&callbackData0};

    notifier_callback_config_t callbacks[] = {callbackCfg0};

    // Power mode configurations.
    power_user_config_t vlprConfig;
    power_user_config_t stopConfig;

    notifier_user_config_t *powerConfigs[] = {&vlprConfig, &stopConfig};

    // Definition of a transition to and out the power modes.
    vlprConfig.mode = kAPP_PowerModeVlpr;
    vlprConfig.enableLowPowerWakeUpOnInterrupt = false;

    stopConfig = vlprConfig;
    stopConfig.mode = kAPP_PowerModeStop;

    // Create Notifier handle.
    NOTIFIER_CreateHandle(&powerModeHandle, powerConfigs, 2U, callbacks, 1U,
        APP_PowerModeSwitch, NULL);
    ...

    ...
    // Power mode switch.
    NOTIFIER_switchConfig(&powerModeHandle, targetConfigIndex,
        kNOTIFIER_PolicyAgreement);
}

```

## Data Structures

- struct [notifier\\_notification\\_block\\_t](#)  
*notification block passed to the registered callback function.* [More...](#)
- struct [notifier\\_callback\\_config\\_t](#)  
*Callback configuration structure.* [More...](#)
- struct [notifier\\_handle\\_t](#)  
*Notifier handle structure.* [More...](#)

## Typedefs

- [typedef void notifier\\_user\\_config\\_t](#)  
*Notifier user configuration type.*
- [typedef status\\_t\(\\* notifier\\_user\\_function\\_t \)\(notifier\\_user\\_config\\_t \\*targetConfig, void \\*userData\)](#)

- *Notifier user function prototype Use this function to execute specific operations in configuration switch.*  
**typedef status\_t(\* notifier\_callback\_t )(notifier\_notification\_block\_t \*notify, void \*data)**  
*Callback prototype.*

## Enumerations

- **enum \_notifier\_status {**  
**kStatus\_NOTIFIER\_ErrorNotificationBefore,**  
**kStatus\_NOTIFIER\_ErrorNotificationAfter }**  
*Notifier error codes.*
- **enum notifier\_policy\_t {**  
**kNOTIFIER\_PolicyAgreement,**  
**kNOTIFIER\_PolicyForcible }**  
*Notifier policies.*
- **enum notifier\_notification\_type\_t {**  
**kNOTIFIER\_NotifyRecover = 0x00U,**  
**kNOTIFIER\_NotifyBefore = 0x01U,**  
**kNOTIFIER\_NotifyAfter = 0x02U }**  
*Notification type.*
- **enum notifier\_callback\_type\_t {**  
**kNOTIFIER\_CallbackBefore = 0x01U,**  
**kNOTIFIER\_CallbackAfter = 0x02U,**  
**kNOTIFIER\_CallbackBeforeAfter = 0x03U }**  
*The callback type, which indicates kinds of notification the callback handles.*

## Functions

- **status\_t NOTIFIER\_CreateHandle (notifier\_handle\_t \*notifierHandle, notifier\_user\_config\_t \*\*configs, uint8\_t configsNumber, notifier\_callback\_config\_t \*callbacks, uint8\_t callbacksNumber, notifier\_user\_function\_t userFunction, void \*userData)**  
*Creates a Notifier handle.*
- **status\_t NOTIFIER\_SwitchConfig (notifier\_handle\_t \*notifierHandle, uint8\_t configIndex, notifier\_policy\_t policy)**  
*Switches the configuration according to a pre-defined structure.*
- **uint8\_t NOTIFIER\_GetErrorCallbackIndex (notifier\_handle\_t \*notifierHandle)**  
*This function returns the last failed notification callback.*

## 52.3 Data Structure Documentation

### 52.3.1 struct notifier\_notification\_block\_t

#### Data Fields

- **notifier\_user\_config\_t \* targetConfig**  
*Pointer to target configuration.*
- **notifier\_policy\_t policy**  
*Configure transition policy.*
- **notifier\_notification\_type\_t notifyType**

*Configure notification type.*

#### Field Documentation

- (1) **notifier\_user\_config\_t\* notifier\_notification\_block\_t::targetConfig**
- (2) **notifier\_policy\_t notifier\_notification\_block\_t::policy**
- (3) **notifier\_notification\_type\_t notifier\_notification\_block\_t::notifyType**

### 52.3.2 struct notifier\_callback\_config\_t

This structure holds the configuration of callbacks. Callbacks of this type are expected to be statically allocated. This structure contains the following application-defined data. callback - pointer to the callback function callbackType - specifies when the callback is called callbackData - pointer to the data passed to the callback.

#### Data Fields

- **notifier\_callback\_t callback**  
*Pointer to the callback function.*
- **notifier\_callback\_type\_t callbackType**  
*Callback type.*
- **void \*callbackData**  
*Pointer to the data passed to the callback.*

#### Field Documentation

- (1) **notifier\_callback\_t notifier\_callback\_config\_t::callback**
- (2) **notifier\_callback\_type\_t notifier\_callback\_config\_t::callbackType**
- (3) **void\* notifier\_callback\_config\_t::callbackData**

### 52.3.3 struct notifier\_handle\_t

Notifier handle structure. Contains data necessary for the Notifier proper function. Stores references to registered configurations, callbacks, information about their numbers, user function, user data, and other internal data. [NOTIFIER\\_CreateHandle\(\)](#) must be called to initialize this handle.

#### Data Fields

- **notifier\_user\_config\_t \*\* configsTable**  
*Pointer to configure table.*
- **uint8\_t configsNumber**  
*Number of configurations.*

- `notifier_callback_config_t * callbacksTable`  
*Pointer to callback table.*
- `uint8_t callbacksNumber`  
*Maximum number of callback configurations.*
- `uint8_t errorCallbackIndex`  
*Index of callback returns error.*
- `uint8_t currentConfigIndex`  
*Index of current configuration.*
- `notifier_user_function_t userFunction`  
*User function.*
- `void * userData`  
*User data passed to user function.*

## Field Documentation

- (1) `notifier_user_config_t** notifier_handle_t::configsTable`
- (2) `uint8_t notifier_handle_t::configsNumber`
- (3) `notifier_callback_config_t* notifier_handle_t::callbacksTable`
- (4) `uint8_t notifier_handle_t::callbacksNumber`
- (5) `uint8_t notifier_handle_t::errorCallbackIndex`
- (6) `uint8_t notifier_handle_t::currentConfigIndex`
- (7) `notifier_user_function_t notifier_handle_t::userFunction`
- (8) `void* notifier_handle_t::userData`

## 52.4 Typedef Documentation

### 52.4.1 `typedef void notifier_user_config_t`

Reference of the user defined configuration is stored in an array; the notifier switches between these configurations based on this array.

### 52.4.2 `typedef status_t(* notifier_user_function_t)(notifier_user_config_t *targetConfig, void *userData)`

Before and after this function execution, different notification is sent to registered callbacks. If this function returns any error code, `NOTIFIER_SwitchConfig()` exits.

Parameters

<i>targetConfig</i>	target Configuration.
<i>userData</i>	Refers to other specific data passed to user function.

Returns

An error code or kStatus\_Success.

### 52.4.3 **typedef status\_t(\* notifier\_callback\_t)(notifier\_notification\_block\_t \*notify, void \*data)**

Declaration of a callback. It is common for registered callbacks. Reference to function of this type is part of the [notifier\\_callback\\_config\\_t](#) callback configuration structure. Depending on callback type, function of this prototype is called (see [NOTIFIER\\_SwitchConfig\(\)](#)) before configuration switch, after it or in both use cases to notify about the switch progress (see [notifier\\_callback\\_type\\_t](#)). When called, the type of the notification is passed as a parameter along with the reference to the target configuration structure (see [notifier\\_notification\\_block\\_t](#)) and any data passed during the callback registration. When notified before the configuration switch, depending on the configuration switch policy (see [notifier\\_policy\\_t](#)), the callback may deny the execution of the user function by returning an error code different than kStatus\_Success (see [NOTIFIER\\_SwitchConfig\(\)](#)).

Parameters

<i>notify</i>	Notification block.
<i>data</i>	Callback data. Refers to the data passed during callback registration. Intended to pass any driver or application data such as internal state information.

Returns

An error code or kStatus\_Success.

## 52.5 Enumeration Type Documentation

### 52.5.1 enum \_notifier\_status

Used as return value of Notifier functions.

Enumerator

***kStatus\_NOTIFIER\_ErrorNotificationBefore*** An error occurs during send "BEFORE" notification.

***kStatus\_NOTIFIER\_ErrorNotificationAfter*** An error occurs during send "AFTER" notification.

### 52.5.2 enum notifier\_policy\_t

Defines whether the user function execution is forced or not. For `kNOTIFIER_PolicyForcible`, the user function is executed regardless of the callback results, while `kNOTIFIER_PolicyAgreement` policy is used to exit `NOTIFIER_SwitchConfig()` when any of the callbacks returns error code. See also `NOTIFIER_SwitchConfig()` description.

Enumerator

***kNOTIFIER\_PolicyAgreement*** `NOTIFIER_SwitchConfig()` method is exited when any of the callbacks returns error code.

***kNOTIFIER\_PolicyForcible*** The user function is executed regardless of the results.

### 52.5.3 enum notifier\_notification\_type\_t

Used to notify registered callbacks

Enumerator

***kNOTIFIER\_NotifyRecover*** Notify IP to recover to previous work state.

***kNOTIFIER\_NotifyBefore*** Notify IP that configuration setting is going to change.

***kNOTIFIER\_NotifyAfter*** Notify IP that configuration setting has been changed.

### 52.5.4 enum notifier\_callback\_type\_t

Used in the callback configuration structure (`notifier_callback_config_t`) to specify when the registered callback is called during configuration switch initiated by the `NOTIFIER_SwitchConfig()`. Callback can be invoked in following situations.

- Before the configuration switch (Callback return value can affect `NOTIFIER_SwitchConfig()` execution. See the `NOTIFIER_SwitchConfig()` and `notifier_policy_t` documentation).
- After an unsuccessful attempt to switch configuration
- After a successful configuration switch

Enumerator

***kNOTIFIER\_CallbackBefore*** Callback handles BEFORE notification.

***kNOTIFIER\_CallbackAfter*** Callback handles AFTER notification.

***kNOTIFIER\_CallbackBeforeAfter*** Callback handles BEFORE and AFTER notification.

## 52.6 Function Documentation

52.6.1 `status_t NOTIFIER_CreateHandle ( notifier_handle_t * notifierHandle,  
notifier_user_config_t ** configs, uint8_t configsNumber, notifier_callback-  
_config_t * callbacks, uint8_t callbacksNumber, notifier_user_function_t  
userFunction, void * userData )`

## Parameters

<i>notifierHandle</i>	A pointer to the notifier handle.
<i>configs</i>	A pointer to an array with references to all configurations which is handled by the Notifier.
<i>configsNumber</i>	Number of configurations. Size of the configuration array.
<i>callbacks</i>	A pointer to an array of callback configurations. If there are no callbacks to register during Notifier initialization, use NULL value.
<i>callbacks-Number</i>	Number of registered callbacks. Size of the callbacks array.
<i>userFunction</i>	User function.
<i>userData</i>	User data passed to user function.

## Returns

An error Code or kStatus\_Success.

### 52.6.2 **status\_t NOTIFIER\_SwitchConfig ( notifier\_handle\_t \* *notifierHandle*, uint8\_t *configIndex*, notifier\_policy\_t *policy* )**

This function sets the system to the target configuration. Before transition, the Notifier sends notifications to all callbacks registered to the callback table. Callbacks are invoked in the following order: All registered callbacks are notified ordered by index in the callbacks array. The same order is used for before and after switch notifications. The notifications before the configuration switch can be used to obtain confirmation about the change from registered callbacks. If any registered callback denies the configuration change, further execution of this function depends on the notifier policy: the configuration change is either forced (kNOTIFIER\_PolicyForcible) or exited (kNOTIFIER\_PolicyAgreement). When configuration change is forced, the result of the before switch notifications are ignored. If an agreement is required, if any callback returns an error code, further notifications before switch notifications are cancelled and all already notified callbacks are re-invoked. The index of the callback which returned error code during pre-switch notifications is stored (any error codes during callbacks re-invocation are ignored) and NOTIFIER\_GetErrorCallback() can be used to get it. Regardless of the policies, if any callback returns an error code, an error code indicating in which phase the error occurred is returned when NOTIFIER\_SwitchConfig() exits.

## Parameters

<i>notifierHandle</i>	pointer to notifier handle
<i>configIndex</i>	Index of the target configuration.
<i>policy</i>	Transaction policy, kNOTIFIER_PolicyAgreement or kNOTIFIER_PolicyForcible.

Returns

An error code or kStatus\_Success.

### 52.6.3 uint8\_t NOTIFIER\_GetErrorCallbackIndex ( *notifier\_handle\_t \*notifierHandle* )

This function returns an index of the last callback that failed during the configuration switch while the last [NOTIFIER\\_SwitchConfig\(\)](#) was called. If the last [NOTIFIER\\_SwitchConfig\(\)](#) call ended successfully value equal to callbacks number is returned. The returned value represents an index in the array of static call-backs.

Parameters

<i>notifierHandle</i>	Pointer to the notifier handle
-----------------------	--------------------------------

Returns

Callback Index of the last failed callback or value equal to callbacks count.

# Chapter 53

## Shell

### 53.1 Overview

This section describes the programming interface of the Shell middleware.

Shell controls MCUs by commands via the specified communication peripheral based on the debug console driver.

### 53.2 Function groups

#### 53.2.1 Initialization

To initialize the Shell middleware, call the `SHELL_Init()` function with these parameters. This function automatically enables the middleware.

```
shell_status_t SHELL_Init(shell_handle_t shellHandle,  
    serial_handle_t serialHandle, char *prompt);
```

Then, after the initialization was successful, call a command to control MCUs.

This example shows how to call the `SHELL_Init()` given the user configuration structure.

```
SHELL_Init(s_shellHandle, s_serialHandle, "Test@SHELL>");
```

#### 53.2.2 Advanced Feature

- Support to get a character from standard input devices.

```
static shell_status_t SHELL_GetChar(shell_context_handle_t *shellContextHandle, uint8_t *ch);
```

Commands	Description
help	List all the registered commands.
exit	Exit program.

#### 53.2.3 Shell Operation

```
SHELL_Init(s_shellHandle, s_serialHandle, "Test@SHELL>");  
SHELL_Task(s_shellHandle);
```

## Data Structures

- struct `shell_command_t`  
*User command data configuration structure. More...*

## Macros

- #define `SHELL_NON_BLOCKING_MODE` SERIAL\_MANAGER\_NON\_BLOCKING\_MODE  
*Whether use non-blocking mode.*
- #define `SHELL_AUTO_COMPLETE` (1U)  
*Macro to set on/off auto-complete feature.*
- #define `SHELL_BUFFER_SIZE` (64U)  
*Macro to set console buffer size.*
- #define `SHELL_MAX_ARGS` (8U)  
*Macro to set maximum arguments in command.*
- #define `SHELL_HISTORY_COUNT` (3U)  
*Macro to set maximum count of history commands.*
- #define `SHELL_IGNORE_PARAMETER_COUNT` (0xFF)  
*Macro to bypass arguments check.*
- #define `SHELL_HANDLE_SIZE`  
*The handle size of the shell module.*
- #define `SHELL_USE_COMMON_TASK` (0U)  
*Macro to determine whether use common task.*
- #define `SHELL_TASK_PRIORITY` (2U)  
*Macro to set shell task priority.*
- #define `SHELL_TASK_STACK_SIZE` (1000U)  
*Macro to set shell task stack size.*
- #define `SHELL_HANDLE_DEFINE`(name) uint32\_t name[((`SHELL_HANDLE_SIZE` + sizeof(uint32\_t) - 1U) / sizeof(uint32\_t))]  
*Defines the shell handle.*
- #define `SHELL_COMMAND_DEFINE`(command, descriptor, callback, paramInt)  
*Defines the shell command structure.*
- #define `SHELL_COMMAND`(command) &g\_shellCommand##command  
*Gets the shell command pointer.*

## Typedefs

- typedef void \* `shell_handle_t`  
*The handle of the shell module.*
- typedef `shell_status_t`(\* `cmd_function_t` )(`shell_handle_t` shellHandle, int32\_t argc, char \*\*argv)  
*User command function prototype.*

## Enumerations

- enum `shell_status_t` {
   
`kStatus_SHELL_Success` = kStatus\_Success,
   
`kStatus_SHELL_Error` = MAKE\_STATUS(kStatusGroup\_SHELL, 1),
   
`kStatus_SHELL_OpenWriteHandleFailed` = MAKE\_STATUS(kStatusGroup\_SHELL, 2),
   
`kStatus_SHELL_OpenReadHandleFailed` = MAKE\_STATUS(kStatusGroup\_SHELL, 3),
   
`kStatus_SHELL_RetUsage` = MAKE\_STATUS(kStatusGroup\_SHELL, 4) }
   
*Shell status.*

## Shell functional operation

- `shell_status_t SHELL_Init (shell_handle_t shellHandle, serial_handle_t serialHandle, char *prompt)`  
*Initializes the shell module.*
- `shell_status_t SHELL_RegisterCommand (shell_handle_t shellHandle, shell_command_t *shellCommand)`  
*Registers the shell command.*
- `shell_status_t SHELL_UnregisterCommand (shell_command_t *shellCommand)`  
*Unregisters the shell command.*
- `shell_status_t SHELL_Write (shell_handle_t shellHandle, const char *buffer, uint32_t length)`  
*Sends data to the shell output stream.*
- `int SHELL_Printf (shell_handle_t shellHandle, const char *formatString,...)`  
*Writes formatted output to the shell output stream.*
- `shell_status_t SHELL_WriteSynchronization (shell_handle_t shellHandle, const char *buffer, uint32_t length)`  
*Sends data to the shell output stream with OS synchronization.*
- `int SHELL_PrintfSynchronization (shell_handle_t shellHandle, const char *formatString,...)`  
*Writes formatted output to the shell output stream with OS synchronization.*
- `void SHELL_ChangePrompt (shell_handle_t shellHandle, char *prompt)`  
*Change shell prompt.*
- `void SHELL_PrintPrompt (shell_handle_t shellHandle)`  
*Print shell prompt.*
- `void SHELL_Task (shell_handle_t shellHandle)`  
*The task function for Shell.*
- `static bool SHELL_checkRunningInIsr (void)`  
*Check if code is running in ISR.*

## 53.3 Data Structure Documentation

### 53.3.1 struct shell\_command\_t

#### Data Fields

- `const char * pcCommand`  
*The command that is executed.*
- `char * pcHelpString`  
*String that describes how to use the command.*
- `const cmd_function_t pFuncCallBack`  
*A pointer to the callback function that returns the output generated by the command.*
- `uint8_t cExpectedNumberOfParameters`  
*Commands expect a fixed number of parameters, which may be zero.*
- `list_element_t link`  
*link of the element*

#### Field Documentation

##### (1) `const char* shell_command_t::pcCommand`

For example "help". It must be all lower case.

**(2) `char* shell_command_t::pcHelpString`**

It should start with the command itself, and end with "\r\n". For example "help: Returns a list of all the commands\r\n".

**(3) `const cmd_function_t shell_command_t::pFuncCallBack`****(4) `uint8_t shell_command_t::cExpectedNumberOfParameters`**

## 53.4 Macro Definition Documentation

### 53.4.1 `#define SHELL_NON_BLOCKING_MODE SERIAL_MANAGER_NON_BLOCKING_MODE`

### 53.4.2 `#define SHELL_AUTO_COMPLETE (1U)`

### 53.4.3 `#define SHELL_BUFFER_SIZE (64U)`

### 53.4.4 `#define SHELL_MAX_ARGS (8U)`

### 53.4.5 `#define SHELL_HISTORY_COUNT (3U)`

### 53.4.6 `#define SHELL_HANDLE_SIZE`

**Value:**

```
(160U + SHELL_HISTORY_COUNT * SHELL_BUFFER_SIZE +
    SHELL_BUFFER_SIZE + SERIAL_MANAGER_READ_HANDLE_SIZE + \
    SERIAL_MANAGER_WRITE_HANDLE_SIZE)
```

It is the sum of the SHELL\_HISTORY\_COUNT \* SHELL\_BUFFER\_SIZE + SHELL\_BUFFER\_SIZE + SERIAL\_MANAGER\_READ\_HANDLE\_SIZE + SERIAL\_MANAGER\_WRITE\_HANDLE\_SIZE

**53.4.7 #define SHELL\_USE\_COMMON\_TASK (0U)****53.4.8 #define SHELL\_TASK\_PRIORITY (2U)****53.4.9 #define SHELL\_TASK\_STACK\_SIZE (1000U)****53.4.10 #define SHELL\_HANDLE\_DEFINE( *name* ) uint32\_t  
                  *name*[((SHELL\_HANDLE\_SIZE + sizeof(uint32\_t) - 1U) / sizeof(uint32\_t))]**

This macro is used to define a 4 byte aligned shell handle. Then use "(shell\_handle\_t)*name*" to get the shell handle.

The macro should be global and could be optional. You could also define shell handle by yourself.

This is an example,

```
* SHELL_HANDLE_DEFINE(shellHandle);
*
```

Parameters

<i>name</i>	The name string of the shell handle.
-------------	--------------------------------------

**53.4.11 #define SHELL\_COMMAND\_DEFINE( *command*, *descriptor*, *callback*,  
*paramCount* )**

**Value:**

```
\shell_command_t g_shellCommand##command = {
    (#command), (descriptor), (callback), (paramCount), {0},      \
}
```

This macro is used to define the shell command structure [shell\\_command\\_t](#). And then uses the macro SHELL\_COMMAND to get the command structure pointer. The macro should not be used in any function.

This is a example,

```
* SHELL_COMMAND_DEFINE(exit, "\r\n\"exit\": Exit program\r\n", SHELL_ExitCommand, 0);
* SHELL_RegisterCommand(s_shellHandle, SHELL_COMMAND(exit));
*
```

Parameters

<i>command</i>	The command string of the command. The double quotes do not need. Such as exit for "exit", help for "Help", read for "read".
<i>descriptor</i>	The description of the command is used for showing the command usage when "help" is typing.
<i>callback</i>	The callback of the command is used to handle the command line when the input command is matched.
<i>paramCount</i>	The max parameter count of the current command.

### 53.4.12 #define SHELL\_COMMAND( *command* ) &g\_shellCommand##*command*

This macro is used to get the shell command pointer. The macro should not be used before the macro SHELL\_COMMAND\_DEFINE is used.

Parameters

<i>command</i>	The command string of the command. The double quotes do not need. Such as exit for "exit", help for "Help", read for "read".
----------------	--

## 53.5 Typedef Documentation

### 53.5.1 **typedef shell\_status\_t(\* cmd\_function\_t)(shell\_handle\_t shellHandle, int32\_t argc, char \*\*argv)**

## 53.6 Enumeration Type Documentation

### 53.6.1 enum shell\_status\_t

Enumerator

*kStatus\_SHELL\_Success* Success.

*kStatus\_SHELL\_Error* Failed.

*kStatus\_SHELL\_OpenWriteHandleFailed* Open write handle failed.

*kStatus\_SHELL\_OpenReadHandleFailed* Open read handle failed.

*kStatus\_SHELL\_RetUsage* RetUsage for print cmd usage.

## 53.7 Function Documentation

### 53.7.1 **shell\_status\_t SHELL\_Init ( shell\_handle\_t shellHandle, serial\_handle\_t serialHandle, char \* prompt )**

This function must be called before calling all other Shell functions. Call operation the Shell commands with user-defined settings. The example below shows how to set up the Shell and how to call the SHELL-

\_Init function by passing in these parameters. This is an example.

```
* static SHELL_HANDLE_DEFINE(s_shellHandle);
* SHELL_Init((shell_handle_t)s_shellHandle,
*             serial_handle_t)s_serialHandle, "Test@SHELL>");
```

#### Parameters

<i>shellHandle</i>	Pointer to point to a memory space of size <b>SHELL_HANDLE_SIZE</b> allocated by the caller. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: <b>SHELL_HANDLE_DEFINE(shellHandle)</b> ; or <code>uint32_t shellHandle[((SHELL_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>
<i>serialHandle</i>	The serial manager module handle pointer.
<i>prompt</i>	The string prompt pointer of Shell. Only the global variable can be passed.

#### Return values

<i>kStatus_SHELL_Success</i>	The shell initialization succeed.
<i>kStatus_SHELL_Error</i>	An error occurred when the shell is initialized.
<i>kStatus_SHELL_Open-WriteHandleFailed</i>	Open the write handle failed.
<i>kStatus_SHELL_Open-ReadHandleFailed</i>	Open the read handle failed.

### 53.7.2 shell\_status\_t **SHELL\_RegisterCommand** ( shell\_handle\_t **shellHandle**, shell\_command\_t \* **shellCommand** )

This function is used to register the shell command by using the command configuration `shell_command_config_t`. This is a example,

```
* SHELL_COMMAND_DEFINE(exit, "\r\n\"exit\": Exit program\r\n", SHELL_ExitCommand, 0);
* SHELL_RegisterCommand(s_shellHandle, SHELL_COMMAND(exit));
*
```

#### Parameters

---

<i>shellHandle</i>	The shell module handle pointer.
<i>shellCommand</i>	The command element.

Return values

<i>kStatus_SHELL_Success</i>	Successfully register the command.
<i>kStatus_SHELL_Error</i>	An error occurred.

### 53.7.3 shell\_status\_t SHELL\_UnregisterCommand ( shell\_command\_t \* *shellCommand* )

This function is used to unregister the shell command.

Parameters

<i>shellCommand</i>	The command element.
---------------------	----------------------

Return values

<i>kStatus_SHELL_Success</i>	Successfully unregister the command.
------------------------------	--------------------------------------

### 53.7.4 shell\_status\_t SHELL\_Write ( shell\_handle\_t *shellHandle*, const char \* *buffer*, uint32\_t *length* )

This function is used to send data to the shell output stream.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>buffer</i>	Start address of the data to write.
<i>length</i>	Length of the data to write.

Return values

<i>kStatus_SHELL_Success</i>	Successfully send data.
------------------------------	-------------------------

<i>kStatus_SHELL_Error</i>	An error occurred.
----------------------------	--------------------

### 53.7.5 int SHELL\_Printf ( shell\_handle\_t *shellHandle*, const char \* *formatString*, ... )

Call this function to write a formatted output to the shell output stream.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>formatString</i>	Format string.

Returns

Returns the number of characters printed or a negative value if an error occurs.

### 53.7.6 shell\_status\_t SHELL\_WriteSynchronization ( shell\_handle\_t *shellHandle*, const char \* *buffer*, uint32\_t *length* )

This function is used to send data to the shell output stream with OS synchronization, note the function could not be called in ISR.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>buffer</i>	Start address of the data to write.
<i>length</i>	Length of the data to write.

Return values

<i>kStatus_SHELL_Success</i>	Successfully send data.
<i>kStatus_SHELL_Error</i>	An error occurred.

### 53.7.7 int SHELL\_PrintfSynchronization ( shell\_handle\_t *shellHandle*, const char \* *formatString*, ... )

Call this function to write a formatted output to the shell output stream with OS synchronization, note the function could not be called in ISR.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>formatString</i>	Format string.

Returns

Returns the number of characters printed or a negative value if an error occurs.

### 53.7.8 void SHELL\_ChangePrompt ( shell\_handle\_t *shellHandle*, char \* *prompt* )

Call this function to change shell prompt.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>prompt</i>	The string which will be used for command prompt

Returns

NULL.

### 53.7.9 void SHELL\_PrintPrompt ( shell\_handle\_t *shellHandle* )

Call this function to print shell prompt.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
--------------------	----------------------------------

Returns

NULL.

### 53.7.10 void SHELL\_Task ( shell\_handle\_t *shellHandle* )

The task function for Shell; The function should be polled by upper layer. This function does not return until Shell command exit was called.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
--------------------	----------------------------------

### 53.7.11 static bool SHELL\_checkRunningInIsr( void ) [inline], [static]

This function is used to check if code running in ISR.

Return values

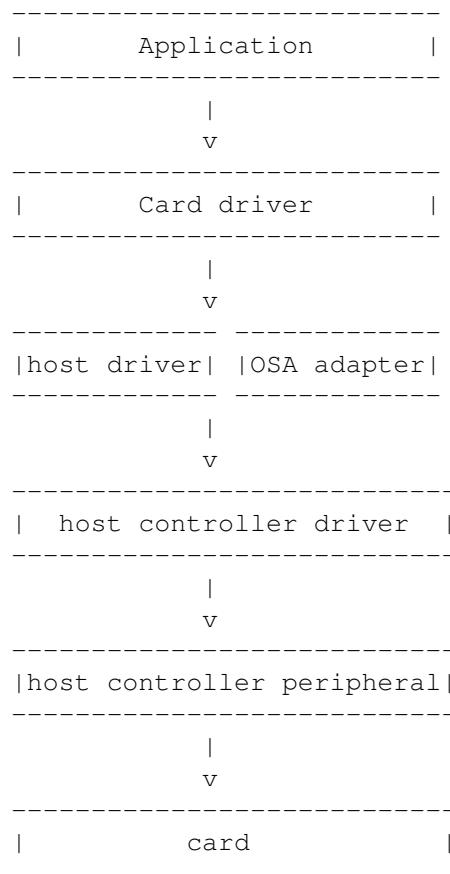
<i>TRUE</i>	if code runing in ISR.
-------------	------------------------

# Chapter 54

## Cards: Secure Digital Card/Embedded MultiMedia Card/SD-IO Card

### 54.1 Overview

The MCUXpresso SDK provides drivers to access the Secure Digital Card(up to v3.0), Embedded Multi-Media Card(up to v5.0) and sdio card(up to v3.0) based on the SDHC/USDHC/SDIF driver. Here is a simple block diagram about the drivers:



### Modules

- [MMC Card Driver](#)
- [SD Card Driver](#)
- [SDIO Card Driver](#)
- [SDMMC Common](#)
- [SDMMC HOST Driver](#)
- [SDMMC OSA](#)

## 54.2 SDIO Card Driver

### 54.2.1 Overview

The SDIO card driver provide card initialization/IO direct and extend command interface.

### 54.2.2 SDIO CARD Operation

#### error log support

Not supported yet.

#### User configurable

#### Board dependency

#### Mutual exclusive access support for RTOS

SDIO driver has added mutual exclusive access support for init/deinit/write/read/erase function. Please note that the card init function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization

```
SDIO_Deinit(card); /* This function will destroy the created mutex */
SDIO_Init(card);
```

#### Typical use case

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/sdmmc\_examples/

## Data Structures

- struct [sdio\\_card\\_t](#)  
*SDIO card state. [More...](#)*

## Macros

- #define [FSL\\_SDIO\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2U, 4U, 1U)) /\*2.4.1\*/
*Middleware version.*
- #define [FSL\\_SDIO\\_MAX\\_IO\\_NUMS](#) (7U)
*sdio device support maximum IO number*

## Typedefs

- `typedef void(* sdio_io_irq_handler_t )(sdio_card_t *card, uint32_t func)`  
*sdio io handler*

## Enumerations

- `enum sdio_io_direction_t {  
 kSDIO_IORead = 0U,  
 kSDIO_IOWrite = 1U }`  
*sdio io read/write direction*

## Initialization and deinitialization

- `status_t SDIO_Init (sdio_card_t *card)`  
*SDIO card init function.*
- `void SDIO_Deinit (sdio_card_t *card)`  
*SDIO card\_deinit, include card and host\_deinit.*
- `status_t SDIO_CardInit (sdio_card_t *card)`  
*Initializes the card.*
- `void SDIO_CardDeinit (sdio_card_t *card)`  
*Deinitializes the card.*
- `status_t SDIO_HostInit (sdio_card_t *card)`  
*initialize the host.*
- `void SDIO_HostDeinit (sdio_card_t *card)`  
*Deinitializes the host.*
- `void SDIO_HostDoReset (sdio_card_t *card)`  
*reset the host.*
- `void SDIO_SetCardPower (sdio_card_t *card, bool enable)`  
*set card power.*
- `status_t SDIO_CardInActive (sdio_card_t *card)`  
*set SDIO card to inactive state*
- `status_t SDIO_GetCardCapability (sdio_card_t *card, sdio_func_num_t func)`  
*get SDIO card capability*
- `status_t SDIO_SetBlockSize (sdio_card_t *card, sdio_func_num_t func, uint32_t blockSize)`  
*set SDIO card block size*
- `status_t SDIO_CardReset (sdio_card_t *card)`  
*set SDIO card reset*
- `status_t SDIO_SetDataBusWidth (sdio_card_t *card, sdio_bus_width_t busWidth)`  
*set SDIO card data bus width*
- `status_t SDIO_SwitchToHighSpeed (sdio_card_t *card)`  
*switch the card to high speed*
- `status_t SDIO_ReadCIS (sdio_card_t *card, sdio_func_num_t func, const uint32_t *tupleList, uint32_t tupleNum)`  
*read SDIO card CIS for each function*
- `status_t SDIO_PollingCardInsert (sdio_card_t *card, uint32_t status)`  
*sdio wait card detect function.*
- `bool SDIO_IsCardPresent (sdio_card_t *card)`

*sdio card present check function.*

## IO operations

- `status_t SDIO_IO_Write_Direct` (`sdio_card_t *card`, `sdio_func_num_t func`, `uint32_t regAddr`, `uint8_t *data`, `bool raw`)
 

*IO direct write transfer function.*
- `status_t SDIO_IO_Read_Direct` (`sdio_card_t *card`, `sdio_func_num_t func`, `uint32_t regAddr`, `uint8_t *data`)
 

*IO direct read transfer function.*
- `status_t SDIO_IO_RW_Direct` (`sdio_card_t *card`, `sdio_io_direction_t direction`, `sdio_func_num_t func`, `uint32_t regAddr`, `uint8_t dataIn`, `uint8_t *dataOut`)
 

*IO direct read/write transfer function.*
- `status_t SDIO_IO_Write_Extended` (`sdio_card_t *card`, `sdio_func_num_t func`, `uint32_t regAddr`, `uint8_t *buffer`, `uint32_t count`, `uint32_t flags`)
 

*IO extended write transfer function.*
- `status_t SDIO_IO_Read_Extended` (`sdio_card_t *card`, `sdio_func_num_t func`, `uint32_t regAddr`, `uint8_t *buffer`, `uint32_t count`, `uint32_t flags`)
 

*IO extended read transfer function.*
- `status_t SDIO_EnableIOInterrupt` (`sdio_card_t *card`, `sdio_func_num_t func`, `bool enable`)
 

*enable IO interrupt*
- `status_t SDIO_EnableIO` (`sdio_card_t *card`, `sdio_func_num_t func`, `bool enable`)
 

*enable IO and wait IO ready*
- `status_t SDIO_SelectIO` (`sdio_card_t *card`, `sdio_func_num_t func`)
 

*select IO*
- `status_t SDIO_AbortIO` (`sdio_card_t *card`, `sdio_func_num_t func`)
 

*Abort IO transfer.*
- `status_t SDIO_SetDriverStrength` (`sdio_card_t *card`, `sd_driver_strength_t driverStrength`)
 

*Set driver strength.*
- `status_t SDIO_EnableAsyncInterrupt` (`sdio_card_t *card`, `bool enable`)
 

*Enable/Disable Async interrupt.*
- `status_t SDIO_GetPendingInterrupt` (`sdio_card_t *card`, `uint8_t *pendingInt`)
 

*Get pending interrupt.*
- `status_t SDIO_IO_Transfer` (`sdio_card_t *card`, `sdio_command_t cmd`, `uint32_t argument`, `uint32_t blockSize`, `uint8_t *txData`, `uint8_t *rxData`, `uint16_t dataSize`, `uint32_t *response`)
 

*sdio card io transfer function.*
- `void SDIO_SetIOIRQHandler` (`sdio_card_t *card`, `sdio_func_num_t func`, `sdio_io_irq_handler_t handler`)
 

*sdio set io IRQ handler.*
- `status_t SDIO_HandlePendingIOInterrupt` (`sdio_card_t *card`)
 

*sdio card io pending interrupt handle function.*

### 54.2.3 Data Structure Documentation

#### 54.2.3.1 struct \_sdio\_card

sdio card descriptor

Define the card structure including the necessary fields to identify and describe the card.

## Data Fields

- `sdmmchost_t * host`  
*Host information.*
- `sdio_usr_param_t usrParam`  
*user parameter*
- `bool noInternalAlign`  
*use this flag to disable sdmmc align.*
- `uint8_t internalBuffer [FSL_SDMMC_CARD_INTERNAL_BUFFER_SIZE]`  
*internal buffer*
- `bool isHostReady`  
*use this flag to indicate if need host re-init or not*
- `bool memPresentFlag`  
*indicate if memory present*
- `uint32_t busClock_Hz`  
*SD bus clock frequency united in Hz.*
- `uint32_t relativeAddress`  
*Relative address of the card.*
- `uint8_t sdVersion`  
*SD version.*
- `sd_timing_mode_t currentTiming`  
*current timing mode*
- `sd_driver_strength_t driverStrength`  
*driver strength*
- `sd_max_current_t maxCurrent`  
*card current limit*
- `sdmmc_operation_voltage_t operationVoltage`  
*card operation voltage*
- `uint8_t sdioVersion`  
*SDIO version.*
- `uint8_t cccrVersioin`  
*CCCR version.*
- `uint8_t ioTotalNumber`  
*total number of IO function*
- `uint32_t cccrflags`  
*Flags in \_sd\_card\_flag.*
- `uint32_t io0blockSize`  
*record the io0 block size*
- `uint32_t ocr`  
*Raw OCR content, only 24bit available for SDIO card.*
- `uint32_t commonCISPointer`  
*point to common CIS*
- `sdio_common_cis_t commonCIS`  
*CIS table.*
- `sdio_fbr_t ioFBR [FSL_SDIO_MAX_IO_NUMS]`  
*FBR table.*
- `sdio_func_cis_t funcCIS [FSL_SDIO_MAX_IO_NUMS]`  
*function CIS table*
- `sdio_io_irq_handler_t ioIRQHandler [FSL_SDIO_MAX_IO_NUMS]`

- *io IRQ handler*
- `uint8_t ioIntIndex`  
*used to record current enabled io interrupt index*
- `uint8_t ioIntNums`  
*used to record total enabled io interrupt numbers*
- `sdmmc_osa_mutex_t lock`  
*card access lock*

## Field Documentation

### (1) `bool sdio_card_t::noInternalAlign`

If disable, sdmmc will not make sure the data buffer address is word align, otherwise all the transfer are align to low level driver

## 54.2.4 Macro Definition Documentation

### 54.2.4.1 `#define FSL_SDIO_DRIVER_VERSION (MAKE_VERSION(2U, 4U, 1U)) /*2.4.1*/`

## 54.2.5 Enumeration Type Documentation

### 54.2.5.1 `enum sdio_io_direction_t`

Enumerator

- `kSDIO_IORead` io read
- `kSDIO_IOWrite` io write

## 54.2.6 Function Documentation

### 54.2.6.1 `status_t SDIO_Init( sdio_card_t * card )`

Thread safe function, please note that the function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization

```
* SDIO_Deinit(card);
* SDIO_Init(card);
*
```

Parameters

---

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_Go-IdleFailed</i>	
<i>kStatus_SDMMC_Hand-ShakeOperation-ConditionFailed</i>	
<i>kStatus_SDMMC_SDIO-InvalidCard</i>	
<i>kStatus_SDMMC_SDIO-InvalidVoltage</i>	
<i>kStatus_SDMMC_Send-RelativeAddressFailed</i>	
<i>kStatus_SDMMC_Select-CardFailed</i>	
<i>kStatus_SDMMC_SDIO-SwitchHighSpeedFail</i>	
<i>kStatus_SDMMC_SDIO-ReadCISFail</i>	
<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.2 void SDIO\_Deinit ( **sdio\_card\_t** \* *card* )

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.2.6.3 status\_t SDIO\_CardInit ( **sdio\_card\_t** \* *card* )

This function initializes the card only, make sure the host is ready when call this function, otherwise it will return *kStatus\_SDMMC\_HostNotReady*.

Thread safe function, please note that the function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization

```
* SDIO_CardDeinit(card);
* SDIO_CardInit(card);
*
```

## Parameters

<i>card</i>	Card descriptor.
-------------	------------------

## Return values

<i>kStatus_SDMMC_Host-NotReady</i>	host is not ready.
<i>kStatus_SDMMC_Go-IdleFailed</i>	Go idle failed.
<i>kStatus_SDMMC_Not-SupportYet</i>	Card not support.
<i>kStatus_SDMMC_Send-OperationCondition-Failed</i>	Send operation condition failed.
<i>kStatus_SDMMC_All-SendCidFailed</i>	Send CID failed.
<i>kStatus_SDMMC_Send-RelativeAddressFailed</i>	Send relative address failed.
<i>kStatus_SDMMC_Send-CsdFailed</i>	Send CSD failed.
<i>kStatus_SDMMC_Select-CardFailed</i>	Send SELECT_CARD command failed.
<i>kStatus_SDMMC_Send-ScrFailed</i>	Send SCR failed.
<i>kStatus_SDMMC_SetBus-WidthFailed</i>	Set bus width failed.
<i>kStatus_SDMMC_Switch-HighSpeedFailed</i>	Switch high speed failed.

<i>kStatus_SDMMC_SetCardBlockSizeFailed</i>	Set card block size failed.
<i>kStatus_Success</i>	Operate successfully.

#### 54.2.6.4 void SDIO\_CardDeinit ( *sdio\_card\_t* \* *card* )

This function deinitializes the specific card.

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.2.6.5 status\_t SDIO\_HostInit ( *sdio\_card\_t* \* *card* )

This function deinitializes the specific host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.2.6.6 void SDIO\_HostDeinit ( *sdio\_card\_t* \* *card* )

This function deinitializes the host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.2.6.7 void SDIO\_HostDoReset ( *sdio\_card\_t* \* *card* )

This function reset the specific host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.2.6.8 void SDIO\_SetCardPower ( *sdio\_card\_t* \* *card*, *bool enable* )

The power off operation depend on host or the user define power on function.

Parameters

<i>card</i>	card descriptor.
<i>enable</i>	true is power on, false is power off.

#### 54.2.6.9 status\_t SDIO\_CardInActive ( **sdio\_card\_t \* card** )

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.10 status\_t SDIO\_GetCardCapability ( **sdio\_card\_t \* card, sdio\_func\_num\_t func** )

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.11 status\_t SDIO\_SetBlockSize ( **sdio\_card\_t \* card, sdio\_func\_num\_t func, uint32\_t blockSize** )

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	io number
<i>blockSize</i>	block size

Return values

<i>kStatus_SDMMC_SetCardBlockSizeFailed</i>	
<i>kStatus_SDMMC_SDIO_InvalidArgument</i>	
<i>kStatus_Success</i>	

#### 54.2.6.12 status\_t SDIO\_CardReset ( *sdio\_card\_t \* card* )

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.13 status\_t SDIO\_SetDataBusWidth ( *sdio\_card\_t \* card, sdio\_bus\_width\_t busWidth* )

Parameters

<i>card</i>	Card descriptor.
<i>busWidth</i>	bus width

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

54.2.6.14 status\_t SDIO\_SwitchToHighSpeed ( *sdio\_card\_t \* card* )

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_-TransferFailed</i>	
<i>kStatus_SDMMC_SDIO_-SwitchHighSpeedFail</i>	
<i>kStatus_Success</i>	

#### 54.2.6.15 status\_t SDIO\_ReadCIS ( *sdio\_card\_t \* card*, *sdio\_func\_num\_t func*, *const uint32\_t \* tupleList*, *uint32\_t tupleNum* )

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	io number
<i>tupleList</i>	code list
<i>tupleNum</i>	code number

Return values

<i>kStatus_SDMMC_SDIO_-ReadCISFail</i>	
<i>kStatus_SDMMC_-TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.16 status\_t SDIO\_PollingCardInsert ( *sdio\_card\_t \* card*, *uint32\_t status* )

Detect card through GPIO, CD, DATA3.

Parameters

<i>card</i>	card descriptor.
<i>status</i>	detect status, kSD_Inserted or kSD_Removed.

#### 54.2.6.17 bool SDIO\_IsCardPresent ( *sdio\_card\_t \* card* )

Parameters

<i>card</i>	card descriptor.
-------------	------------------

#### 54.2.6.18 status\_t SDIO\_IO\_Write\_Direct ( *sdio\_card\_t \* card*, *sdio\_func\_num\_t func*, *uint32\_t regAddr*, *uint8\_t \* data*, *bool raw* )

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number
<i>regAddr</i>	register address
<i>data</i>	the data pointer to write
<i>raw</i>	flag, indicate read after write or write only

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.19 status\_t SDIO\_IO\_Read\_Direct ( *sdio\_card\_t \* card*, *sdio\_func\_num\_t func*, *uint32\_t regAddr*, *uint8\_t \* data* )

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number
<i>regAddr</i>	register address
<i>data</i>	pointer to read

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.20 status\_t SDIO\_IO\_RW\_Direct ( *sdio\_card\_t \* card*, *sdio\_io\_direction\_t direction*, *sdio\_func\_num\_t func*, *uint32\_t regAddr*, *uint8\_t dataIn*, *uint8\_t \* dataOut* )

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>direction</i>	io access direction, please reference <i>sdio_io_direction_t</i> .
<i>func</i>	IO number
<i>regAddr</i>	register address
<i>dataIn</i>	data to write
<i>dataOut</i>	data pointer for readback data, support both for read and write, when application want readback the data after write command, <i>dataOut</i> should not be NULL.

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.21 status\_t SDIO\_IO\_Write\_Extended ( *sdio\_card\_t \* card*, *sdio\_func\_num\_t func*, *uint32\_t regAddr*, *uint8\_t \* buffer*, *uint32\_t count*, *uint32\_t flags* )

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number
<i>regAddr</i>	register address
<i>buffer</i>	data buffer to write
<i>count</i>	data count
<i>flags</i>	write flags

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_SDMMC_SDIO_InvalidArgument</i>	
<i>kStatus_Success</i>	

#### 54.2.6.22 **status\_t SDIO\_IO\_Read\_Extended ( *sdio\_card\_t \* card, sdio\_func\_num\_t func, uint32\_t regAddr, uint8\_t \* buffer, uint32\_t count, uint32\_t flags* )**

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number
<i>regAddr</i>	register address
<i>buffer</i>	data buffer to read
<i>count</i>	data count
<i>flags</i>	write flags

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_SDMMC_SDIO_InvalidArgument</i>	
<i>kStatus_Success</i>	

#### 54.2.6.23 **status\_t SDIO\_EnableOIInterrupt ( *sdio\_card\_t \* card, sdio\_func\_num\_t func, bool enable* )**

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number
<i>enable</i>	enable/disable flag

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.24 status\_t SDIO\_EnableIO ( ***sdio\_card\_t \* card, sdio\_func\_num\_t func, bool enable*** )

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number
<i>enable</i>	enable/disable flag

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.25 status\_t SDIO\_SelectIO ( ***sdio\_card\_t \* card, sdio\_func\_num\_t func*** )

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

54.2.6.26 status\_t SDIO\_AbortIO ( *sdio\_card\_t \* card, sdio\_func\_num\_t func* )

Parameters

<i>card</i>	Card descriptor.
<i>func</i>	IO number

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.27 status\_t SDIO\_SetDriverStrength ( *sdio\_card\_t \* card, sd\_driver\_strength\_t driverStrength* )

Parameters

<i>card</i>	Card descriptor.
<i>driverStrength</i>	target driver strength.

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.28 status\_t SDIO\_EnableAsyncInterrupt ( *sdio\_card\_t \* card, bool enable* )

Parameters

<i>card</i>	Card descriptor.
<i>enable</i>	true is enable, false is disable.

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
-------------------------------------	--

<i>kStatus_Success</i>
------------------------

#### 54.2.6.29 status\_t SDIO\_GetPendingInterrupt ( *sdio\_card\_t \* card, uint8\_t \* pendingInt* )

Parameters

<i>card</i>	Card descriptor.
<i>pendingInt</i>	pointer store pending interrupt

Return values

<i>kStatus_SDMMC_TransferFailed</i>	
<i>kStatus_Success</i>	

#### 54.2.6.30 status\_t SDIO\_IO\_Transfer ( *sdio\_card\_t \* card, sdio\_command\_t cmd, uint32\_t argument, uint32\_t blockSize, uint8\_t \* txData, uint8\_t \* rxData, uint16\_t dataSize, uint32\_t \* response* )

This function can be used for transfer direct/extend command. Please pay attention to the non-align data buffer address transfer, if data buffer address can not meet host controller internal DMA requirement, sdio driver will try to use internal align buffer if data size is not bigger than internal buffer size, Align address transfer always can get a better performance, so if application want sdio driver make sure buffer address align,

Please note it is a thread safe function.

Parameters

<i>card</i>	card descriptor.
<i>cmd</i>	command to transfer
<i>argument</i>	argument to transfer
<i>blockSize</i>	used for block mode.
<i>txData</i>	tx buffer pointer or NULL

<i>rxData</i>	rx buffer pointer or NULL
<i>dataSize</i>	transfer data size
<i>response</i>	reponse pointer, if application want read response back, please set it to a NON-NULL pointer.

#### 54.2.6.31 void SDIO\_SetIOIRQHandler ( *sdio\_card\_t* \* *card*, *sdio\_func\_num\_t* *func*, *sdio\_io\_irq\_handler\_t* *handler* )

Parameters

<i>card</i>	card descriptor.
<i>func</i>	function io number.
<i>handler</i>	io IRQ handler.

#### 54.2.6.32 status\_t SDIO\_HandlePendingIOInterrupt ( *sdio\_card\_t* \* *card* )

This function is used to handle the pending io interrupt. To reigster a IO IRQ handler,

```
* SDIO_EnableIOInterrupt(card, 0, true);
* SDIO_SetIOIRQHandler(card, 0, func0_handler);
*
```

call it in interrupt callback

```
* SDIO_HandlePendingIOInterrupt(card);
*
```

To releae a IO IRQ handler,

```
* SDIO_EnableIOInterrupt(card, 0, false);
* SDIO_SetIOIRQHandler(card, 0, NULL);
*
```

Parameters

<i>card</i>	card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_-TransferFailed</i>	
<i>kStatus_Success</i>	

## 54.3 SD Card Driver

### 54.3.1 Overview

The SDCARD driver provide card initialization/read/write/erase interface.

### 54.3.2 SD CARD Operation

#### error log support

Lots of error log has been added to sd relate functions, if error occurs during initial/read/write, please enable the error log print functionality with `#define SDMMC_ENABLE_LOG_PRINT 1` And rerun the project then user can check what kind of error happened.

#### User configurable

```
typedef struct _sd_card
{
    sdmmchost_t *host;
    sd_usr_param_t usrParam;
    bool isHostReady;
    bool noInternalAlign;
    uint32_t busClock_Hz;
    uint32_t relativeAddress;
    uint32_t version;
    uint32_t flags;
    uint8_t internalBuffer[FSL_SDMMC_CARD_INTERNAL_BUFFER_SIZE];
    uint32_t ocr;
    sd_cid_t cid;
    sd_csd_t csd;
    sd_scr_t scr;
    sd_status_t stat;
    uint32_t blockCount;
    uint32_t blockSize;
    sd_timing_mode_t currentTiming;
    sd_driver_strength_t driverStrength;
    sd_max_current_t maxCurrent;
    sdmmc_operation_voltage_t operationVoltage;
    sdmmc_osa_mutex_t lock;
} sd_card_t;
```

Part of The variables above is user configurable,

##### 1. host

Application need to provide host controller base address and the host's source clock frequency, etc.  
For example:

```
/* allocate dma descriptor buffer for host controller */
s_host.dmaDesBuffer
s_host.dmaDesBufferWordsNum
/* */
((sd_card_t *)card)->host
((sd_card_t *)card)->host->hostController.base
((sd_card_t *)card)->host->hostController.sourceClock_Hz = BOARD_USDHC1ClockConfiguration();

/* allocate resource for sdmmc osa layer */
((sd_card_t *)card)->host->hostEvent = &s_event;
```

## 2. sdcard\_usr\_param\_t usrParam

```
/* board layer configuration register */
((sd_card_t *)card)->usrParam.cd      = &s_cd;
((sd_card_t *)card)->usrParam.pwr      = BOARD_SDCardPowerControl;
((sd_card_t *)card)->usrParam.ioStrength = BOARD_SD_Pin_Config;
((sd_card_t *)card)->usrParam.ioVoltage  = &s_ioVoltage;
((sd_card_t *)card)->usrParam.maxFreq    = BOARD_SDMMC_SD_HOST_SUPPORT_SDR104_FREQ;

a. cd-which allow application define the card insert/remove callback function, redefine the card detect
   timeout ms and also allow application determine how to detect card.
b. pwr-which allow application redefine the card power on/off function.
c. ioStrength-which is used to switch the signal pin configurations include driver strength/speed mode
   dynamically for different timing(SDR/HS timing) mode, reference the function defined sdmmc_config.c
d. ioVoltage-which allow application register io voltage switch function instead of using the function host
   driver provided for SDR/HS200/HS400 timing.
e. maxFreq-which allow application set the maximum bus clock that the board support.
```

### 1. bool noInternalAlign

Sdmmc include an address align internal buffer(to use host controller internal DMA), to improve read/write performance while application cannot make sure the data address used to read/write is align, set it to true will achieve a better performance.

### 2. sd\_timing\_mode\_t currentTiming

It is used to indicate the currentTiming the card is working on, however sdmmc also support preset timing mode, then sdmmc will try to switch to this timing first, if failed, a valid timing will switch to automatically. Generally, user may not set this variable if you don't know what kind of timing the card support, sdmmc will switch to the highest timing which the card support.

### 3. sd\_driver\_strength\_t driverStrength

Choose a valid card driver strength if application required and call SD\_SetDriverStrength in application.

### 4. sd\_max\_current\_t maxCurrent

Choose a valid card current if application required and call SD\_SetMaxCurrent in application.

## Mutual exclusive access support for RTOS

SDCARD driver has added mutual exclusive access support for init/deinit/write/read/erase function. Please note that the card init function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization

```
SD_Deinit(card); /* This function will destroy the created mutex */
SD_Init(card);
```

## Typical use case

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/sdmmc\_examples/

## Data Structures

- struct `sd_card_t`  
*SD card state.* [More...](#)

## Macros

- #define **FSL\_SD\_DRIVER\_VERSION** (MAKE\_VERSION(2U, 4U, 2U)) /\*2.4.2\*/
 *Driver version.*

## Enumerations

- enum {
 **kSD\_SupportHighCapacityFlag** = (1U << 1U),
 **kSD\_Support4BitWidthFlag** = (1U << 2U),
 **kSD\_SupportSdhcFlag** = (1U << 3U),
 **kSD\_SupportSdxcFlag** = (1U << 4U),
 **kSD\_SupportVoltage180v** = (1U << 5U),
 **kSD\_SupportSetBlockCountCmd** = (1U << 6U),
 **kSD\_SupportSpeedClassControlCmd** = (1U << 7U) }
- SD card flags.*

## SDCARD Function

- **status\_t SD\_Init (sd\_card\_t \*card)**  
*Initializes the card on a specific host controller.*
- **void SD\_Deinit (sd\_card\_t \*card)**  
*Deinitializes the card.*
- **status\_t SD\_CardInit (sd\_card\_t \*card)**  
*Initializes the card.*
- **void SD\_CardDeinit (sd\_card\_t \*card)**  
*Deinitializes the card.*
- **status\_t SD\_HostInit (sd\_card\_t \*card)**  
*initialize the host.*
- **void SD\_HostDeinit (sd\_card\_t \*card)**  
*Deinitializes the host.*
- **void SD\_HostDoReset (sd\_card\_t \*card)**  
*reset the host.*
- **void SD\_SetCardPower (sd\_card\_t \*card, bool enable)**  
*set card power.*
- **status\_t SD\_PollingCardInsert (sd\_card\_t \*card, uint32\_t status)**  
*sd wait card detect function.*
- **bool SD\_IsCardPresent (sd\_card\_t \*card)**  
*sd card present check function.*
- **bool SD\_CheckReadOnly (sd\_card\_t \*card)**  
*Checks whether the card is write-protected.*
- **status\_t SD\_SelectCard (sd\_card\_t \*card, bool isSelected)**  
*Send SELECT\_CARD command to set the card to be transfer state or not.*
- **status\_t SD\_ReadStatus (sd\_card\_t \*card)**  
*Send ACMD13 to get the card current status.*
- **status\_t SD\_ReadBlocks (sd\_card\_t \*card, uint8\_t \*buffer, uint32\_t startBlock, uint32\_t blockCount)**

- *Reads blocks from the specific card.*  
**status\_t SD\_WriteBlocks** (*sd\_card\_t* \*card, const *uint8\_t* \*buffer, *uint32\_t* startBlock, *uint32\_t* blockCount)
- *Writes blocks of data to the specific card.*  
**status\_t SD\_EraseBlocks** (*sd\_card\_t* \*card, *uint32\_t* startBlock, *uint32\_t* blockCount)
- *Erases blocks of the specific card.*  
**status\_t SD\_SetDriverStrength** (*sd\_card\_t* \*card, *sd\_driver\_strength\_t* driverStrength)
- select card driver strength select card driver strength*
- *select max current select max operation current*  
**status\_t SD\_SetMaxCurrent** (*sd\_card\_t* \*card, *sd\_max\_current\_t* maxCurrent)
- *Polling card idle status.*  
**status\_t SD\_PollingCardStatusBusy** (*sd\_card\_t* \*card, *uint32\_t* timeoutMs)

### 54.3.3 Data Structure Documentation

#### 54.3.3.1 struct *sd\_card\_t*

Define the card structure including the necessary fields to identify and describe the card.

#### Data Fields

- **sdmmchost\_t \* host**  
*Host configuration.*
- **sd\_usr\_param\_t usrParam**  
*user parameter*
- **bool isHostReady**  
*use this flag to indicate if need host re-init or not*
- **bool noInternalAlign**  
*used to enable/disable the functionality of the exchange buffer*
- **uint32\_t busClock\_Hz**  
*SD bus clock frequency unitized in Hz.*
- **uint32\_t relativeAddress**  
*Relative address of the card.*
- **uint32\_t version**  
*Card version.*
- **uint32\_t flags**  
*Flags in \_sd\_card\_flag.*
- **uint8\_t internalBuffer [FSL\_SDMMC\_CARD\_INTERNAL\_BUFFER\_SIZE]**  
*internal buffer*
- **uint32\_t ocr**  
*Raw OCR content.*
- **sd\_cid\_t cid**  
*CID.*
- **sd\_csd\_t csd**  
*CSD.*
- **sd\_scr\_t scr**  
*SCR.*
- **sd\_status\_t stat**

- *sd 512 bit status*
- **uint32\_t blockCount**  
*Card total block number.*
- **uint32\_t blockSize**  
*Card block size.*
- **sd\_timing\_mode\_t currentTiming**  
*current timing mode*
- **sd\_driver\_strength\_t driverStrength**  
*driver strength*
- **sd\_max\_current\_t maxCurrent**  
*card current limit*
- **sdmmc\_operation\_voltage\_t operationVoltage**  
*card operation voltage*
- **sdmmc\_osa\_mutex\_t lock**  
*card access lock*

#### 54.3.4 Macro Definition Documentation

54.3.4.1 **#define FSL\_SD\_DRIVER\_VERSION (MAKE\_VERSION(2U, 4U, 2U)) /\*2.4.2\*/**

#### 54.3.5 Enumeration Type Documentation

##### 54.3.5.1 anonymous enum

Enumerator

**kSD\_SupportHighCapacityFlag** Support high capacity.

**kSD\_Support4BitWidthFlag** Support 4-bit data width.

**kSD\_SupportSdhcFlag** Card is SDHC.

**kSD\_SupportSdxcFlag** Card is SDXC.

**kSD\_SupportVoltage180v** card support 1.8v voltage

**kSD\_SupportSetBlockCountCmd** card support cmd23 flag

**kSD\_SupportSpeedClassControlCmd** card support speed class control flag

#### 54.3.6 Function Documentation

##### 54.3.6.1 **status\_t SD\_Init ( sd\_card\_t \* card )**

This function initializes the card on a specific host controller, it is consist of host init, card detect, card init function, however user can ignore this high level function, instead of use the low level function, such as SD\_CardInit, SD\_HostInit, SD\_CardDetect.

Thread safe function, please note that the function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization

\* `SD_Deinit(card);`

```
* SD_Init(card);
*
```

## Parameters

<i>card</i>	Card descriptor.
-------------	------------------

## Return values

<i>kStatus_SDMMC_HostNotReady</i>	host is not ready.
<i>kStatus_SDMMC_GoIdleFailed</i>	Go idle failed.
<i>kStatus_SDMMC_NotSupportYet</i>	Card not support.
<i>kStatus_SDMMC_HandShakeOperationConditionFailed</i>	Send operation condition failed.
<i>kStatus_SDMMC_AllSendCidFailed</i>	Send CID failed.
<i>kStatus_SDMMC_SendRelativeAddressFailed</i>	Send relative address failed.
<i>kStatus_SDMMC_SendCsdFailed</i>	Send CSD failed.
<i>kStatus_SDMMC_SelectCardFailed</i>	Send SELECT_CARD command failed.
<i>kStatus_SDMMC_SendScrFailed</i>	Send SCR failed.
<i>kStatus_SDMMC_SetDataBusWidthFailed</i>	Set bus width failed.
<i>kStatus_SDMMC_SwitchBusTimingFailed</i>	Switch high speed failed.
<i>kStatus_SDMMC_SetCardBlockSizeFailed</i>	Set card block size failed.

<i>kStatus_Success</i>	Operate successfully.
------------------------	-----------------------

#### 54.3.6.2 void SD\_Deinit ( *sd\_card\_t* \* *card* )

This function deinitializes the specific card and host. Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.3.6.3 *status\_t* SD\_CardInit ( *sd\_card\_t* \* *card* )

This function initializes the card only, make sure the host is ready when call this function, otherwise it will return *kStatus\_SDMMC\_HostNotReady*.

Thread safe function, please note that the function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization

```
* SD_CardDeinit(card);
* SD_CardInit(card);
*
```

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_Host-NotReady</i>	host is not ready.
<i>kStatus_SDMMC_Go-IdleFailed</i>	Go idle failed.
<i>kStatus_SDMMC_Not-SupportYet</i>	Card not support.
<i>kStatus_SDMMC_Hand-ShakeOperation-ConditionFailed</i>	Send operation condition failed.

<i>kStatus_SDMMC_AllSendCidFailed</i>	Send CID failed.
<i>kStatus_SDMMC_SendRelativeAddressFailed</i>	Send relative address failed.
<i>kStatus_SDMMC_SendCsdFailed</i>	Send CSD failed.
<i>kStatus_SDMMC_SelectCardFailed</i>	Send SELECT_CARD command failed.
<i>kStatus_SDMMC_SendScrFailed</i>	Send SCR failed.
<i>kStatus_SDMMC_SetDataBusWidthFailed</i>	Set bus width failed.
<i>kStatus_SDMMC_SwitchBusTimingFailed</i>	Switch high speed failed.
<i>kStatus_SDMMC_SetCardBlockSizeFailed</i>	Set card block size failed.
<i>kStatus_Success</i>	Operate successfully.

#### 54.3.6.4 void SD\_CardDeinit( *sd\_card\_t* \* *card* )

This function deinitializes the specific card. Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.3.6.5 status\_t SD\_HostInit( *sd\_card\_t* \* *card* )

This function deinitializes the specific host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.3.6.6 void SD\_HostDeinit( *sd\_card\_t* \* *card* )

This function deinitializes the host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.3.6.7 void SD\_HostDoReset ( *sd\_card\_t* \* *card* )

This function reset the specific host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.3.6.8 void SD\_SetCardPower ( *sd\_card\_t* \* *card*, *bool* *enable* )

The power off operation depend on host or the user define power on function.

Parameters

<i>card</i>	card descriptor.
<i>enable</i>	true is power on, false is power off.

#### 54.3.6.9 *status\_t* SD\_PollingCardInsert ( *sd\_card\_t* \* *card*, *uint32\_t* *status* )

Detect card through GPIO, CD, DATA3.

Parameters

<i>card</i>	card descriptor.
<i>status</i>	detect status, kSD_Inserted or kSD_Removed.

#### 54.3.6.10 *bool* SD\_IsCardPresent ( *sd\_card\_t* \* *card* )

Parameters

<i>card</i>	card descriptor.
-------------	------------------

#### 54.3.6.11 *bool* SD\_CheckReadOnly ( *sd\_card\_t* \* *card* )

This function checks if the card is write-protected via the CSD register.

Parameters

<i>card</i>	The specific card.
-------------	--------------------

Return values

<i>true</i>	Card is read only.
<i>false</i>	Card isn't read only.

#### 54.3.6.12 status\_t SD\_SelectCard ( *sd\_card\_t \* card, bool isSelected* )

Parameters

<i>card</i>	Card descriptor.
<i>isSelected</i>	True to set the card into transfer state, false to disselect.

Return values

<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_Success</i>	Operate successfully.

#### 54.3.6.13 status\_t SD\_ReadStatus ( *sd\_card\_t \* card* )

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_SDMMC_SendApplicationCommandFailed</i>	send application command failed.

<i>kStatus_Success</i>	Operate successfully.
------------------------	-----------------------

#### 54.3.6.14 status\_t SD\_ReadBlocks ( *sd\_card\_t \* card*, *uint8\_t \* buffer*, *uint32\_t startBlock*, *uint32\_t blockCount* )

This function reads blocks from the specific card with default block size defined by the SDHC\_CARD\_DEFAULT\_BLOCK\_SIZE.

Please note it is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>buffer</i>	The buffer to save the data read from card.
<i>startBlock</i>	The start block index.
<i>blockCount</i>	The number of blocks to read.

Return values

<i>kStatus_InvalidArgument</i>	Invalid argument.
<i>kStatus_SDMMC_Card-NotSupport</i>	Card not support.
<i>kStatus_SDMMC_Not-SupportYet</i>	Not support now.
<i>kStatus_SDMMC_Wait-WriteCompleteFailed</i>	Send status failed.
<i>kStatus_SDMMC_-TransferFailed</i>	Transfer failed.
<i>kStatus_SDMMC_Stop-TransmissionFailed</i>	Stop transmission failed.
<i>kStatus_Success</i>	Operate successfully.

#### 54.3.6.15 status\_t SD\_WriteBlocks ( *sd\_card\_t \* card*, *const uint8\_t \* buffer*, *uint32\_t startBlock*, *uint32\_t blockCount* )

This function writes blocks to the specific card with default block size 512 bytes.

Please note,

1. It is a thread safe function.
2. It is a async write function which means that the card status may still busy after the function return.

Application can call function SD\_PollingCardStatusBusy to wait card status idle after the write operation.

Parameters

<i>card</i>	Card descriptor.
<i>buffer</i>	The buffer holding the data to be written to the card.
<i>startBlock</i>	The start block index.
<i>blockCount</i>	The number of blocks to write.

Return values

<i>kStatus_InvalidArgument</i>	Invalid argument.
<i>kStatus_SDMMC_Not-SupportYet</i>	Not support now.
<i>kStatus_SDMMC_Card-NotSupport</i>	Card not support.
<i>kStatus_SDMMC_Wait-WriteCompleteFailed</i>	Send status failed.
<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_SDMMC_Stop-TransmissionFailed</i>	Stop transmission failed.
<i>kStatus_Success</i>	Operate successfully.

#### 54.3.6.16 **status\_t SD\_EraseBlocks ( sd\_card\_t \* card, uint32\_t startBlock, uint32\_t blockCount )**

This function erases blocks of the specific card with default block size 512 bytes.

Please note,

1. It is a thread safe function.
2. It is a async erase function which means that the card status may still busy after the function return.  
Application can call function SD\_PollingCardStatusBusy to wait card status idle after the erase operation.

Parameters

<i>card</i>	Card descriptor.
<i>startBlock</i>	The start block index.
<i>blockCount</i>	The number of blocks to erase.

Return values

<i>kStatus_InvalidArgument</i>	Invalid argument.
<i>kStatus_SDMMC_Wait-WriteCompleteFailed</i>	Send status failed.
<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_SDMMC_Wait-WriteCompleteFailed</i>	Send status failed.
<i>kStatus_Success</i>	Operate successfully.

#### 54.3.6.17 **status\_t SD\_SetDriverStrength ( sd\_card\_t \* *card*, sd\_driver\_strength\_t *driverStrength* )**

Parameters

<i>card</i>	Card descriptor.
<i>driverStrength</i>	Driver strength

#### 54.3.6.18 **status\_t SD\_SetMaxCurrent ( sd\_card\_t \* *card*, sd\_max\_current\_t *maxCurrent* )**

Parameters

<i>card</i>	Card descriptor.
<i>maxCurrent</i>	Max current

#### 54.3.6.19 **status\_t SD\_PollingCardStatusBusy ( sd\_card\_t \* *card*, uint32\_t *timeoutMs* )**

This function can be used to polling the status from busy to Idle, the function will return if the card status idle or timeout.

## Parameters

<i>card</i>	Card descriptor.
<i>timeoutMs</i>	polling card status timeout value.

## Return values

<i>kStatus_Success</i>	Operate successfully.
<i>kStatus_SDMMC_Wait-WriteCompleteFailed</i>	CMD13 transfer failed.
<i>kStatus_SDMMC_-PollingCardIdle-Failed,polling</i>	card DAT0 idle failed.

## 54.4 MMC Card Driver

### 54.4.1 Overview

The MMCCARD driver provide card initialization/read/write/erase interface.

### 54.4.2 MMC CARD Operation

#### error log support

Not support yet

#### User configurable

#### Board dependency

#### Mutual exclusive access support for RTOS

MMCCARD driver has added mutual exclusive access support for init/deinit/write/read/erase function. Please note that the card init function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization.

```
MMC_Deinit(card); /* This function will destroy the created mutex */
MMC_Init(card);
```

#### Typical use case

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/sdmmc\_examples/

## Data Structures

- struct [mmc\\_usr\\_param\\_t](#)  
*card user parameter [More...](#)*
- struct [mmc\\_card\\_t](#)  
*mmc card state [More...](#)*

## Macros

- #define [FSL\\_MMC\\_DRIVER\\_VERSION](#)([MAKE\\_VERSION](#)(2U, 5U, 0U)) /\*2.5.0\*/
*Middleware mmc version.*

## Typedefs

- `typedef void(* mmc_io_strength_t )(uint32_t busFreq)`  
*card io strength control*

## Enumerations

- `enum {`  
 `kMMC_SupportHighSpeed26MHZFlag = (1U << 0U),`  
 `kMMC_SupportHighSpeed52MHZFlag = (1U << 1U),`  
 `kMMC_SupportHighSpeedDDR52MHZ180V300VFlag = (1 << 2U),`  
 `kMMC_SupportHighSpeedDDR52MHZ120VFlag = (1 << 3U),`  
 `kMMC_SupportHS200200MHZ180VFlag = (1 << 4U),`  
 `kMMC_SupportHS200200MHZ120VFlag = (1 << 5U),`  
 `kMMC_SupportHS400DDR200MHZ180VFlag = (1 << 6U),`  
 `kMMC_SupportHS400DDR200MHZ120VFlag = (1 << 7U),`  
 `kMMC_SupportHighCapacityFlag = (1U << 8U),`  
 `kMMC_SupportAlternateBootFlag = (1U << 9U),`  
 `kMMC_SupportDDRBootFlag = (1U << 10U),`  
 `kMMC_SupportHighSpeedBootFlag = (1U << 11U),`  
 `kMMC_SupportEnhanceHS400StrobeFlag = (1U << 12U) }`  
*MMC card flags.*  
`}`
- `enum mmc_sleep_awake_t {`  
 `kMMC_Sleep = 1U,`  
 `kMMC_Awake = 0U }`  
*mmccard sleep/awake state*

## MMCCARD Function

- `status_t MMC_Init (mmc_card_t *card)`  
*Initializes the MMC card and host.*
- `void MMC_Deinit (mmc_card_t *card)`  
*Deinitializes the card and host.*
- `status_t MMC_CardInit (mmc_card_t *card)`  
*Initializes the card.*
- `void MMC_CardDeinit (mmc_card_t *card)`  
*Deinitializes the card.*
- `status_t MMC_HostInit (mmc_card_t *card)`  
*initialize the host.*
- `void MMC_HostDeinit (mmc_card_t *card)`  
*Deinitializes the host.*
- `void MMC_HostDoReset (mmc_card_t *card)`  
*Resets the host.*
- `void MMC_HostReset (SDMMCHOST_CONFIG *host)`  
*Resets the host.*
- `void MMC_SetCardPower (mmc_card_t *card, bool enable)`

- **bool MMC\_CheckReadOnly (mmc\_card\_t \*card)**  
*Checks if the card is read-only.*
- **status\_t MMC\_ReadBlocks (mmc\_card\_t \*card, uint8\_t \*buffer, uint32\_t startBlock, uint32\_t blockCount)**  
*Reads data blocks from the card.*
- **status\_t MMC\_WriteBlocks (mmc\_card\_t \*card, const uint8\_t \*buffer, uint32\_t startBlock, uint32\_t blockCount)**  
*Writes data blocks to the card.*
- **status\_t MMC\_EraseGroups (mmc\_card\_t \*card, uint32\_t startGroup, uint32\_t endGroup)**  
*Erases groups of the card.*
- **status\_t MMC\_SelectPartition (mmc\_card\_t \*card, mmc\_access\_partition\_t partitionNumber)**  
*Selects the partition to access.*
- **status\_t MMC\_SetBootConfig (mmc\_card\_t \*card, const mmc\_boot\_config\_t \*config)**  
*Configures the boot activity of the card.*
- **status\_t MMC\_StartBoot (mmc\_card\_t \*card, const mmc\_boot\_config\_t \*mmcConfig, uint8\_t \*buffer, sdmmchost\_boot\_config\_t \*hostConfig)**  
*MMC card start boot.*
- **status\_t MMC\_SetBootConfigWP (mmc\_card\_t \*card, uint8\_t wp)**  
*MMC card set boot configuration write protect.*
- **status\_t MMC\_ReadBootData (mmc\_card\_t \*card, uint8\_t \*buffer, sdmmchost\_boot\_config\_t \*hostConfig)**  
*MMC card continuous read boot data.*
- **status\_t MMC\_StopBoot (mmc\_card\_t \*card, uint32\_t bootMode)**  
*MMC card stop boot mode.*
- **status\_t MMC\_SetBootPartitionWP (mmc\_card\_t \*card, mmc\_boot\_partition\_wp\_t bootPartitionWP)**  
*MMC card set boot partition write protect.*
- **status\_t MMC\_EnableCacheControl (mmc\_card\_t \*card, bool enable)**  
*MMC card cache control function.*
- **status\_t MMC\_FlushCache (mmc\_card\_t \*card)**  
*MMC card cache flush function.*
- **status\_t MMC\_SetSleepAwake (mmc\_card\_t \*card, mmc\_sleep\_awake\_t state)**  
*MMC sets card sleep awake state.*
- **status\_t MMC\_PollingCardStatusBusy (mmc\_card\_t \*card, bool checkStatus, uint32\_t timeoutMs)**  
*Polling card idle status.*

#### 54.4.3 Data Structure Documentation

##### 54.4.3.1 struct mmc\_usr\_param\_t

###### Data Fields

- **mmc\_io\_strength\_t ioStrength**  
*switch sd io strength*
- **uint32\_t maxFreq**  
*board support maximum frequency*
- **uint32\_t capability**  
*board capability flag*

#### 54.4.3.2 struct mmc\_card\_t

Defines the card structure including the necessary fields to identify and describe the card.

#### Data Fields

- `sdmmchost_t * host`  
*Host information.*
- `mmc_usr_param_t usrParam`  
*user parameter*
- `bool isHostReady`  
*Use this flag to indicate if host re-init needed or not.*
- `bool noInternalAlign`  
*Use this flag to disable sdmmc align.*
- `uint32_t busClock_Hz`  
*MMC bus clock united in Hz.*
- `uint32_t relativeAddress`  
*Relative address of the card.*
- `bool enablePreDefinedBlockCount`  
*Enable PRE-DEFINED block count when read/write.*
- `uint32_t flags`  
*Capability flag in `_mmc_card_flag`.*
- `uint8_t internalBuffer [FSL_SDMMC_CARD_INTERNAL_BUFFER_SIZE]`  
*raw buffer used for mmc driver internal*
- `uint32_t ocr`  
*Raw OCR content.*
- `mmc_cid_t cid`  
*CID.*
- `mmc_csd_t csd`  
*CSD.*
- `mmc_extended_csd_t extendedCsd`  
*Extended CSD.*
- `uint32_t blockSize`  
*Card block size.*
- `uint32_t userPartitionBlocks`  
*Card total block number in user partition.*
- `uint32_t bootPartitionBlocks`  
*Boot partition size united as block size.*
- `uint32_t eraseGroupBlocks`  
*Erase group size united as block size.*
- `mmc_access_partition_t currentPartition`  
*Current access partition.*
- `mmc_voltage_window_t hostVoltageWindowVCCQ`  
*application must set this value according to board specific*
- `mmc_voltage_window_t hostVoltageWindowVCC`  
*application must set this value according to board specific*
- `mmc_high_speed_timing_t busTiming`  
*indicates the current work timing mode*
- `mmc_data_bus_width_t busWidth`  
*indicates the current work bus width*

- `sdmmc_osa_mutex_t lock`  
*card access lock*

## Field Documentation

### (1) `bool mmc_card_t::noInternalAlign`

If disabled, sdmmc will not make sure the data buffer address is word align, otherwise all the transfer are aligned to low level driver.

## 54.4.4 Macro Definition Documentation

### 54.4.4.1 `#define FSL_MMC_DRIVER_VERSION (MAKE_VERSION(2U, 5U, 0U)) /*2.5.0*/`

## 54.4.5 Enumeration Type Documentation

### 54.4.5.1 anonymous enum

Enumerator

*kMMC\_SupportHighSpeed26MHZFlag* Support high speed 26MHZ.  
*kMMC\_SupportHighSpeed52MHZFlag* Support high speed 52MHZ.  
*kMMC\_SupportHighSpeedDDR52MHZ180V300VFlag* ddr 52MHZ 1.8V or 3.0V  
*kMMC\_SupportHighSpeedDDR52MHZ120VFlag* DDR 52MHZ 1.2V.  
*kMMC\_SupportHS200200MHZ180VFlag* HS200 ,200MHZ,1.8V.  
*kMMC\_SupportHS200200MHZ120VFlag* HS200, 200MHZ, 1.2V.  
*kMMC\_SupportHS400DDR200MHZ180VFlag* HS400, DDR, 200MHZ,1.8V.  
*kMMC\_SupportHS400DDR200MHZ120VFlag* HS400, DDR, 200MHZ,1.2V.  
*kMMC\_SupportHighCapacityFlag* Support high capacity.  
*kMMC\_SupportAlternateBootFlag* Support alternate boot.  
*kMMC\_SupportDDRBootFlag* support DDR boot flag  
*kMMC\_SupportHighSpeedBootFlag* support high speed boot flag  
*kMMC\_SupportEnhanceHS400StrobeFlag* support enhance HS400 strobe

### 54.4.5.2 `enum mmc_sleep_awake_t`

Enumerator

*kMMC\_Sleep* MMC card sleep.  
*kMMC\_Awake* MMC card awake.

## 54.4.6 Function Documentation

54.4.6.1 `status_t MMC_Init( mmc_card_t * card )`

## Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Thread safe function, please note that the function will create the mutex lock dynamically by default, so to avoid the mutex to be created redundantly, application must follow bellow sequence for card re-initialization:

```
MMC_Deinit(card);
MMC_Init(card);
*
```

## Return values

<i>kStatus_SDMMC_HostNotReady</i>	Host is not ready.
<i>kStatus_SDMMC_GoIdleFailed</i>	Going idle failed.
<i>kStatus_SDMMC_HandShakeOperationConditionFailed</i>	Sending operation condition failed.
<i>kStatus_SDMMC_AllSendCidFailed</i>	Sending CID failed.
<i>kStatus_SDMMC_SetRelativeAddressFailed</i>	Setgng relative address failed.
<i>kStatus_SDMMC_SendCsdFailed</i>	Sending CSD failed.
<i>kStatus_SDMMC_CardNotSupport</i>	Card not support.
<i>kStatus_SDMMC_SelectCardFailed</i>	Sending SELECT_CARD command failed.
<i>kStatus_SDMMC_SendExtendedCsdFailed</i>	Sending EXT_CSD failed.
<i>kStatus_SDMMC_SetDataBusWidthFailed</i>	Setting bus width failed.

<i>kStatus_SDMMC_Switch-BusTimingFailed</i>	Switching high speed failed.
<i>kStatus_SDMMC_Set-CardBlockSizeFailed</i>	Setting card block size failed.
<i>kStatus_SDMMC_Set-PowerClassFail</i>	Setting card power class failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.2 void MMC\_Deinit ( mmc\_card\_t \* *card* )

Note

It is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.4.6.3 status\_t MMC\_CardInit ( mmc\_card\_t \* *card* )

Thread safe function, please note that the function will create the mutex lock dynamically by default, so to avoid the mutex to be created redundantly, application must follow bellow sequence for card re-initialization:

```
MMC_CardDeinit(card);
MMC_CardInit(card);
*
```

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>kStatus_SDMMC_Host-NotReady</i>	Host is not ready.
------------------------------------	--------------------

<i>kStatus_SDMMC_Go-IdleFailed</i>	Going idle failed.
<i>kStatus_SDMMC_Hand-ShakeOperation-ConditionFailed</i>	Sending operation condition failed.
<i>kStatus_SDMMC_All-SendCidFailed</i>	Sending CID failed.
<i>kStatus_SDMMC_Set-RelativeAddressFailed</i>	Setting relative address failed.
<i>kStatus_SDMMC_Send-CsdFailed</i>	Sending CSD failed.
<i>kStatus_SDMMC_Card-NotSupport</i>	Card not support.
<i>kStatus_SDMMC_Select-CardFailed</i>	Sending SELECT_CARD command failed.
<i>kStatus_SDMMC_Send-ExtendedCsdFailed</i>	Sending EXT_CSD failed.
<i>kStatus_SDMMC_Set-DataBusWidthFailed</i>	Setting bus width failed.
<i>kStatus_SDMMC_Switch-BusTimingFailed</i>	Switching high speed failed.
<i>kStatus_SDMMC_Set-CardBlockSizeFailed</i>	Setting card block size failed.
<i>kStatus_SDMMC_Set-PowerClassFail</i>	Setting card power class failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.4 void MMC\_CardDeinit ( mmc\_card\_t \* **card** )

Note

It is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.4.6.5 status\_t MMC\_HostInit ( mmc\_card\_t \* *card* )

This function deinitializes the specific host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.4.6.6 void MMC\_HostDeinit ( mmc\_card\_t \* *card* )

This function deinitializes the host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.4.6.7 void MMC\_HostDoReset ( mmc\_card\_t \* *card* )

This function resets the specific host.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.4.6.8 void MMC\_HostReset ( SDMMCHOST\_CONFIG \* *host* )

**Deprecated** Do not use this function. It has been superceded by [MMC\\_HostDoReset](#). This function resets the specific host.

Parameters

<i>host</i>	Host descriptor.
-------------	------------------

#### 54.4.6.9 void MMC\_SetCardPower ( mmc\_card\_t \* *card*, bool *enable* )

Parameters

<i>card</i>	Card descriptor.
<i>enable</i>	True is powering on, false is powering off.

#### 54.4.6.10 bool MMC\_CheckReadOnly ( mmc\_card\_t \* *card* )

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

Return values

<i>true</i>	Card is read only.
<i>false</i>	Card isn't read only.

#### 54.4.6.11 status\_t MMC\_ReadBlocks ( mmc\_card\_t \* *card*, uint8\_t \* *buffer*, uint32\_t *startBlock*, uint32\_t *blockCount* )

Note

It is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>buffer</i>	The buffer to save data.
<i>startBlock</i>	The start block index.
<i>blockCount</i>	The number of blocks to read.

Return values

<i>kStatus_InvalidArgument</i>	Invalid argument.
<i>kStatus_SDMMC_Card-NotSupport</i>	Card not support.

<i>kStatus_SDMMC_SetBlockCountFailed</i>	Setting block count failed.
<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_SDMMC_StopTransmissionFailed</i>	Stopping transmission failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.12 **status\_t MMC\_WriteBlocks ( mmc\_card\_t \* card, const uint8\_t \* buffer, uint32\_t startBlock, uint32\_t blockCount )**

Note

1. It is a thread safe function.
2. It is an async write function which means that the card status may still be busy after the function returns. Application can call function MMC\_PollingCardStatusBusy to wait for the card status to be idle after the write operation.

Parameters

<i>card</i>	Card descriptor.
<i>buffer</i>	The buffer to save data blocks.
<i>startBlock</i>	Start block number to write.
<i>blockCount</i>	Block count.

Return values

<i>kStatus_InvalidArgument</i>	Invalid argument.
<i>kStatus_SDMMC_NotSupportYet</i>	Not support now.
<i>kStatus_SDMMC_SetBlockCountFailed</i>	Setting block count failed.
<i>kStatus_SDMMC_WaitWriteCompleteFailed</i>	Sending status failed.

<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_SDMMC_StopTransmissionFailed</i>	Stop transmission failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.13 status\_t MMC\_EraseGroups ( *mmc\_card\_t \* card*, *uint32\_t startGroup*, *uint32\_t endGroup* )

The erase command is best used to erase the entire device or a partition. Erase group is the smallest erase unit in MMC card. The erase range is [startGroup, endGroup].

Note

1. It is a thread safe function.
2. This function always polls card busy status according to the timeout value defined in the card register after all the erase command sent out.

Parameters

<i>card</i>	Card descriptor.
<i>startGroup</i>	Start group number.
<i>endGroup</i>	End group number.

Return values

<i>kStatus_InvalidArgument</i>	Invalid argument.
<i>kStatus_SDMMC_WaitWriteCompleteFailed</i>	Send status failed.
<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.14 status\_t MMC\_SelectPartition ( *mmc\_card\_t \* card*, *mmc\_access\_partition\_t partitionNumber* )

Note

It is a thread safe function.

Parameters

<i>card</i>	Card descriptor.
<i>partition-Number</i>	The partition number.

Return values

<i>kStatus_SDMMC_ConfigureExtendedCsdFailed</i>	Configuring EXT_CSD failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.15 status\_t MMC\_SetBootConfig ( mmc\_card\_t \* *card*, const mmc\_boot\_config\_t \* *config* )

Parameters

<i>card</i>	Card descriptor.
<i>config</i>	Boot configuration structure.

Return values

<i>kStatus_SDMMC_NotSupportYet</i>	Not support now.
<i>kStatus_SDMMC_ConfigureExtendedCsdFailed</i>	Configuring EXT_CSD failed.
<i>kStatus_SDMMC_ConfigureBootFailed</i>	Configuring boot failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.16 status\_t MMC\_StartBoot ( mmc\_card\_t \* *card*, const mmc\_boot\_config\_t \* *mmcConfig*, uint8\_t \* *buffer*, sdmmchost\_boot\_config\_t \* *hostConfig* )

Parameters

<i>card</i>	Card descriptor.
<i>mmcConfig</i>	The mmc Boot configuration structure.
<i>buffer</i>	Address to receive data.
<i>hostConfig</i>	Host boot configurations.

Return values

<i>kStatus_Fail</i>	Failed.
<i>kStatus_SDMMC_TransferFailed</i>	Transfer failed.
<i>kStatus_SDMMC_Go_IdleFailed</i>	Resetting card failed.
<i>kStatus_Success</i>	Operation succeeded.

#### 54.4.6.17 status\_t MMC\_SetBootConfigWP ( *mmc\_card\_t \* card, uint8\_t wp* )

Parameters

<i>card</i>	Card descriptor.
<i>wp</i>	Write protect value.

#### 54.4.6.18 status\_t MMC\_ReadBootData ( *mmc\_card\_t \* card, uint8\_t \* buffer, sdmmchost\_boot\_config\_t \* hostConfig* )

Parameters

<i>card</i>	Card descriptor.
<i>buffer</i>	Buffer address.
<i>hostConfig</i>	Host boot configurations.

#### 54.4.6.19 status\_t MMC\_StopBoot ( *mmc\_card\_t \* card, uint32\_t bootMode* )

Parameters

<i>card</i>	Card descriptor.
<i>bootMode</i>	Boot mode.

#### 54.4.6.20 status\_t MMC\_SetBootPartitionWP ( *mmc\_card\_t \* card*, *mmc\_boot\_partition\_wp\_t bootPartitionWP* )

Parameters

<i>card</i>	Card descriptor.
<i>bootPartition-WP</i>	Boot partition write protect value.

#### 54.4.6.21 status\_t MMC\_EnableCacheControl ( *mmc\_card\_t \* card*, *bool enable* )

The mmc device's cache is enabled by the driver by default. The cache should in typical case reduce the access time (compared to an access to the main nonvolatile storage) for both write and read.

Parameters

<i>card</i>	Card descriptor.
<i>enable</i>	True is enabling the cache, false is disabling the cache.

#### 54.4.6.22 status\_t MMC\_FlushCache ( *mmc\_card\_t \* card* )

A Flush operation refers to the requirement, from the host to the device, to write the cached data to the nonvolatile memory. Prior to a flush, the device may autonomously write data to the nonvolatile memory, but after the flush operation all data in the volatile area must be written to nonvolatile memory. There is no requirement for flush due to switching between the partitions. (Note: This also implies that the cache data shall not be lost when switching between partitions). Cached data may be lost in SLEEP state, so host should flush the cache before placing the device into SLEEP state.

Parameters

<i>card</i>	Card descriptor.
-------------	------------------

#### 54.4.6.23 status\_t MMC\_SetSleepAwake ( mmc\_card\_t \* card, mmc\_sleep\_awake\_t state )

The Sleep/Awake command is used to initiate the state transition between Standby state and Sleep state. The memory device indicates the transition phase busy by pulling down the DAT0 line. The Sleep/Standby state is reached when the memory device stops pulling down the DAT0 line, then the function returns.

Parameters

<i>card</i>	Card descriptor.
<i>state</i>	The sleep/awake command argument, refer to <a href="#">mmc_sleep_awake_t</a> .

Return values

<i>kStatus_SDMMC_NotSupportYet</i>	Indicates the memory device doesn't support the Sleep/Awake command.
<i>kStatus_SDMMC_TransferFailed</i>	Indicates command transferred fail.
<i>kStatus_SDMMC_PollingCardIdleFailed</i>	Indicates polling DAT0 busy timeout.
<i>kStatus_SDMMC_DeselectCardFailed</i>	Indicates deselect card command failed.
<i>kStatus_SDMMC_SelectCardFailed</i>	Indicates select card command failed.
<i>kStatus_Success</i>	Indicates the card state switched successfully.

#### 54.4.6.24 status\_t MMC\_PollingCardStatusBusy ( mmc\_card\_t \* card, bool checkStatus, uint32\_t timeoutMs )

This function can be used to poll the status from busy to idle, the function will return with the card status being idle or timeout or command failed.

Parameters

<i>card</i>	Card descriptor.
<i>checkStatus</i>	True is send CMD and read DAT0 status to check card status, false is read DAT0 status only.
<i>timeoutMs</i>	Polling card status timeout value.

Return values

<i>kStatus_SDMMC_Card-StatusIdle</i>	Card is idle.
<i>kStatus_SDMMC_Card-StatusBusy</i>	Card is busy.
<i>kStatus_SDMMC_TransferFailed</i>	Command transfer failed.
<i>kStatus_SDMMC_SwitchFailed</i>	Status command reports switch error.

## 54.5 SDMMC HOST Driver

### 54.5.1 Overview

The host adapter driver provide adapter for blocking/non\_blocking mode.

### Modules

- [USDHC HOST adapter Driver](#)

## 54.6 SDMMC OSA

### 54.6.1 Overview

The sdmmc osa adapter provide interface of os adapter.

### Data Structures

- struct `sdmmc_osa_event_t`  
*sdmmc osa event* [More...](#)
- struct `sdmmc_osa_mutex_t`  
*sdmmc osa mutex* [More...](#)

### Macros

- #define `SDMMC_OSA_EVENT_TRANSFER_CMD_SUCCESS` (1UL << 0U)  
*transfer event*
- #define `SDMMC_OSA_EVENT_CARD_INSERTED` (1UL << 8U)  
*card detect event, start from index 8*
- #define `SDMMC_OSA_POLLING_EVENT_BY_SEMPHORE` 1  
*enable semaphore by default*

### sdmmc osa Function

- void `SDMMC_OSAInit` (void)  
*Initialize OSA.*
- `status_t SDMMC_OSAEventCreate` (void \*eventHandle)  
*OSA Create event.*
- `status_t SDMMC_OSAEventWait` (void \*eventHandle, uint32\_t eventType, uint32\_t timeoutMilliseconds, uint32\_t \*event)  
*Wait event.*
- `status_t SDMMC_OSAEventSet` (void \*eventHandle, uint32\_t eventType)  
*set event.*
- `status_t SDMMC_OSAEventGet` (void \*eventHandle, uint32\_t eventType, uint32\_t \*flag)  
*Get event flag.*
- `status_t SDMMC_OSAEventClear` (void \*eventHandle, uint32\_t eventType)  
*clear event flag.*
- `status_t SDMMC_OSAEventDestroy` (void \*eventHandle)  
*Delete event.*
- `status_t SDMMC_OSAMutexCreate` (void \*mutexHandle)  
*Create a mutex.*
- `status_t SDMMC_OSAMutexLock` (void \*mutexHandle, uint32\_t millisec)  
*set event.*
- `status_t SDMMC_OSAMutexUnlock` (void \*mutexHandle)  
*Get event flag.*
- `status_t SDMMC_OSAMutexDestroy` (void \*mutexHandle)  
*Delete mutex.*

- void **SDMMC\_OSA****Delay** (uint32\_t milliseconds)  
*sdmmc delay.*
- uint32\_t **SDMMC\_OSA****DelayUs** (uint32\_t microseconds)  
*sdmmc delay us.*

## 54.6.2 Data Structure Documentation

### 54.6.2.1 struct **sdmmc\_osa\_event\_t**

### 54.6.2.2 struct **sdmmc\_osa\_mutex\_t**

## 54.6.3 Function Documentation

### 54.6.3.1 status\_t **SDMMC\_OSAEventCreate** ( void \* *eventHandle* )

Parameters

<i>eventHandle</i>	event handle.
--------------------	---------------

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

### 54.6.3.2 status\_t **SDMMC\_OSAEventWait** ( void \* *eventHandle*, uint32\_t *eventType*, uint32\_t *timeoutMilliseconds*, uint32\_t \* *event* )

Parameters

<i>eventHandle</i>	The event type
<i>eventType</i>	Timeout time in milliseconds.
<i>timeout-Milliseconds</i>	timeout value in ms.
<i>event</i>	event flags.

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

#### 54.6.3.3 status\_t SDMMC\_OSAEventSet ( void \* *eventHandle*, uint32\_t *eventType* )

Parameters

<i>eventHandle</i>	event handle.
<i>eventType</i>	The event type

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

#### 54.6.3.4 status\_t SDMMC\_OSAEventGet ( void \* *eventHandle*, uint32\_t *eventType*, uint32\_t \* *flag* )

Parameters

<i>eventHandle</i>	event handle.
<i>eventType</i>	event type.
<i>flag</i>	pointer to store event value.

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

#### 54.6.3.5 status\_t SDMMC\_OSAEventClear ( void \* *eventHandle*, uint32\_t *eventType* )

Parameters

<i>eventHandle</i>	event handle.
<i>eventType</i>	The event type

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

#### 54.6.3.6 status\_t SDMMC\_OSAEventDestroy ( void \* *eventHandle* )

Parameters

<i>eventHandle</i>	The event handle.
--------------------	-------------------

#### 54.6.3.7 status\_t SDMMC\_OSAMutexCreate ( void \* *mutexHandle* )

Parameters

<i>mutexHandle</i>	mutex handle.
--------------------	---------------

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

#### 54.6.3.8 status\_t SDMMC\_OSAMutexLock ( void \* *mutexHandle*, uint32\_t *millisec* )

Parameters

<i>mutexHandle</i>	mutex handle.
<i>millisec</i>	The maximum number of milliseconds to wait for the mutex. If the mutex is locked, Pass the value <i>osaWaitForever_c</i> will wait indefinitely, pass 0 will return <i>KOSA_StatusTimeout</i> immediately.

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

#### 54.6.3.9 status\_t SDMMC\_OSAMutexUnlock ( void \* *mutexHandle* )

Parameters

<i>mutexHandle</i>	mutex handle.
--------------------	---------------

Return values

<i>kStatus_Fail</i>	or <i>kStatus_Success</i> .
---------------------	-----------------------------

#### 54.6.3.10 **status\_t SDMMC\_OSAMutexDestroy( void \* *mutexHandle* )**

Parameters

<i>mutexHandle</i>	The mutex handle.
--------------------	-------------------

#### 54.6.3.11 **void SDMMC\_OSADelay( uint32\_t *milliseconds* )**

Parameters

<i>milliseconds</i>	time to delay
---------------------	---------------

#### 54.6.3.12 **uint32\_t SDMMC\_OSADelayUs( uint32\_t *microseconds* )**

Parameters

<i>microseconds</i>	time to delay
---------------------	---------------

Returns

actual delayed microseconds

## 54.6.4 USDHC HOST adapter Driver

### 54.6.4.1 Overview

The USDHC host adapter driver provide adapter for blocking/non\_blocking mode.

#### Cache maintain capability

To maintain data integrity during DMA operations on the platform that has cache, host driver provide a cache maintain functionality by set: host.enableCacheControl = kSDMMCHOST\_CacheControlRW-Buffer This is used for only when the low level driver cache maintain functionality is disabled. It is suggest that the address of buffer used for read/write is align with cache line size.

#### Cache line alignment maintain capability

when application submit a transfer request that the data buffer address is not align with cache line size, the potential data loss may happen during driver maintain the data cache, to avoid such issue happens, sdmmc usdhc host driver provides support on convert the unalign data transfer into align data transfer, if application would like to use the feature, please enable this functionality by define below macro firstly, #define SDMMCHOST\_ENABLE\_CACHE\_LINE\_ALIGN\_TRANSFER 1 And then call SDMMCHOST\_InstallCacheAlignBuffer to install a cache line size align buffer, please note the installed buffer size must not small than 2 \* cache line size. Please note that this functionality is support by the non blocking adapter only.

### Data Structures

- struct `sdmmchost_t`  
*sdmmc host handler* [More...](#)

### Macros

- #define `FSL_SDMMC_HOST_ADAPTER_VERSION` (`MAKE_VERSION(2U, 6U, 3U)`) /\*2.6.-3\*/  
*Middleware adapter version.*
- #define `SDMMCHOST_SUPPORT_HIGH_SPEED` (1U)  
*sdmmc host misc capability*
- #define `SDMMCHOST_SUPPORT_DDR50` (`SDMMCHOST_SUPPORT_DDR_MODE`)  
*sdmmc host sdcard DDR50 mode capability*
- #define `SDMMCHOST_SUPPORT_SDR104` (1U)  
*sdmmc host sdcard SDR50 mode capability*
- #define `SDMMCHOST_SUPPORT_SDR50` (1U)  
*sdmmc host sdcard SDR104/mmccard HS200 mode capability*
- #define `SDMMCHOST_SUPPORT_HS400` (0U)  
*sdmmc host mmccard HS400 mode capability*

- #define **SDMMCHOST\_INSTANCE\_SUPPORT\_8\_BIT\_WIDTH**(host) FSL\_FEATURE\_USDH-C\_INSTANCE\_SUPPORT\_8\_BIT\_WIDTHn(host->hostController.base)  
*sdmmc host instance capability*
- #define **SDMMCHOST\_DATA3\_DETECT\_CARD\_DELAY** (10U)  
*sdmmchost delay for DAT3 detect card*
- #define **SDMMCHOST\_DMA\_DESCRIPTOR\_BUFFER\_ALIGN\_SIZE** (4U)  
*SDMMC host dma descriptor buffer address align size.*
- #define **SDMMCHOST\_STANDARD\_TUNING\_START** (10U)  
*tuning configuration*
- #define **SDMMCHOST\_TUINIG\_STEP** (2U)  
*standard tuning stBep*

## Typedefs

- typedef **usdhc\_transfer\_t** **sdmmchost\_transfer\_t**  
*sdmmc host transfer function*

## Enumerations

- enum {
 **kSDMMCHOST\_SupportHighSpeed** = 1U << 0U,
 **kSDMMCHOST\_SupportSuspendResume** = 1U << 1U,
 **kSDMMCHOST\_SupportVoltage3v3** = 1U << 2U,
 **kSDMMCHOST\_SupportVoltage3v0** = 1U << 3U,
 **kSDMMCHOST\_SupportVoltage1v8** = 1U << 4U,
 **kSDMMCHOST\_SupportVoltage1v2** = 1U << 5U,
 **kSDMMCHOST\_Support4BitDataWidth** = 1U << 6U,
 **kSDMMCHOST\_Support8BitDataWidth** = 1U << 7U,
 **kSDMMCHOST\_SupportDDRMode** = 1U << 8U,
 **kSDMMCHOST\_SupportDetectCardByData3** = 1U << 9U,
 **kSDMMCHOST\_SupportDetectCardByCD** = 1U << 10U,
 **kSDMMCHOST\_SupportAutoCmd12** = 1U << 11U,
 **kSDMMCHOST\_SupportSDR104** = 1U << 12U,
 **kSDMMCHOST\_SupportSDR50** = 1U << 13U,
 **kSDMMCHOST\_SupportHS200** = 1U << 14U,
 **kSDMMCHOST\_SupportHS400** = 1U << 15U }
   
*sdmmc host capability*
- enum {
 **kSDMMCHOST\_EndianModeBig** = 0U,
 **kSDMMCHOST\_EndianModeHalfWordBig** = 1U,
 **kSDMMCHOST\_EndianModeLittle** = 2U }
   
*host Endian mode corresponding to driver define*
- enum {
 **kSDMMCHOST\_StandardTuning** = 0U,
 **kSDMMCHOST\_ManualTuning** = 1U }
   
*sdmmc host tuning type*

- enum {
   
kSDMMCHOST\_NoCacheControl = 0U,  
 kSDMMCHOST\_CacheControlRWBuffer = 1U }  
*sdmmc host maintain cache flag*

## USDHC host controller function

- void **SDMMCHOST\_SetCardBusWidth** (sdmmhost\_t \*host, uint32\_t dataBusWidth)  
*set data bus width.*
- static void **SDMMCHOST\_SendCardActive** (sdmmhost\_t \*host)  
*Send initialization active 80 clocks to card.*
- static uint32\_t **SDMMCHOST\_SetCardClock** (sdmmhost\_t \*host, uint32\_t targetClock)  
*Set card bus clock.*
- static bool **SDMMCHOST\_IsCardBusy** (sdmmhost\_t \*host)  
*check card status by DATA0.*
- static uint32\_t **SDMMCHOST\_GetSignalLineStatus** (sdmmhost\_t \*host, uint32\_t signalLine)  
*Get signal line status.*
- static void **SDMMCHOST\_EnableCardInt** (sdmmhost\_t \*host, bool enable)  
*enable card interrupt.*
- static void **SDMMCHOST\_EnableDDRMode** (sdmmhost\_t \*host, bool enable, uint32\_t nibblePos)  
*enable DDR mode.*
- static void **SDMMCHOST\_EnableHS400Mode** (sdmmhost\_t \*host, bool enable)  
*enable HS400 mode.*
- static void **SDMMCHOST\_EnableStrobeDll** (sdmmhost\_t \*host, bool enable)  
*enable STROBE DLL.*
- status\_t **SDMMCHOST\_StartBoot** (sdmmhost\_t \*host, sdmmhost\_boot\_config\_t \*hostConfig, sdmmhost\_cmd\_t \*cmd, uint8\_t \*buffer)  
*start read boot data.*
- status\_t **SDMMCHOST\_ReadBootData** (sdmmhost\_t \*host, sdmmhost\_boot\_config\_t \*hostConfig, uint8\_t \*buffer)  
*read boot data.*
- static void **SDMMCHOST\_EnableBoot** (sdmmhost\_t \*host, bool enable)  
*enable boot mode.*
- status\_t **SDMMCHOST\_CardIntInit** (sdmmhost\_t \*host, void \*sdioInt)  
*card interrupt function.*
- static void **SDMMCHOST\_ForceClockOn** (sdmmhost\_t \*host, bool enable)  
*force card clock on.*
- void **SDMMCHOST\_SwitchToVoltage** (sdmmhost\_t \*host, uint32\_t voltage)  
*switch to voltage.*
- status\_t **SDMMCHOST\_CardDetectInit** (sdmmhost\_t \*host, void \*cd)  
*card detect init function.*
- status\_t **SDMMCHOST\_PollingCardDetectStatus** (sdmmhost\_t \*host, uint32\_t waitCardStatus, uint32\_t timeout)  
*Detect card insert, only need for SD cases.*
- uint32\_t **SDMMCHOST\_CardDetectStatus** (sdmmhost\_t \*host)  
*card detect status.*
- status\_t **SDMMCHOST\_Init** (sdmmhost\_t \*host)  
*Init host controller.*
- void **SDMMCHOST\_Deinit** (sdmmhost\_t \*host)

- *Deinit host controller.*
- void **SDMMCHOST\_SetCardPower** (**sdmmchost\_t** \*host, bool enable)  
*host power off card function.*
- **status\_t SDMMCHOST\_TransferFunction** (**sdmmchost\_t** \*host, **sdmmchost\_transfer\_t** \*content)  
*host transfer function.*
- **status\_t SDMMCHOST\_ExecuteTuning** (**sdmmchost\_t** \*host, uint32\_t tuningCmd, uint32\_t \*revBuf, uint32\_t blockSize)  
*sdmmc host execute tuning.*
- void **SDMMCHOST\_Reset** (**sdmmchost\_t** \*host)  
*host reset function.*
- void **SDMMCHOST\_ConvertDataToLittleEndian** (**sdmmchost\_t** \*host, uint32\_t \*data, uint32\_t wordSize, uint32\_t format)  
*sdmmc host convert data sequence to little endian sequence*

#### 54.6.4.2 Data Structure Documentation

##### 54.6.4.2.1 struct **sdmmchost\_t**

###### Data Fields

- **usdhc\_host\_t hostController**  
*host configuration*
- void \* **dmaDesBuffer**  
*DMA descriptor buffer address.*
- uint32\_t **dmaDesBufferWordsNum**  
*DMA descriptor buffer size in byte.*
- usdhc\_handle\_t **handle**  
*host controller handler*
- uint32\_t **capability**  
*host controller capability*
- uint32\_t **maxBlockCount**  
*host controller maximum block count*
- uint32\_t **maxBlockSize**  
*host controller maximum block size*
- uint8\_t **tuningType**  
*host tuning type*
- **sdmmc\_osa\_event\_t hostEvent**  
*host event handler*
- void \* **cd**  
*card detect*
- void \* **cardInt**  
*call back function for card interrupt*
- **sdmmc\_osa\_mutex\_t lock**  
*host access lock*

#### 54.6.4.3 Macro Definition Documentation

**54.6.4.3.1 #define FSL\_SDMMC\_HOST\_ADAPTER\_VERSION (MAKE\_VERSION(2U, 6U, 3U))  
/\*2.6.3\*/**

**54.6.4.3.2 #define SDMMCHOST\_STANDARD\_TUNING\_START (10U)**

standard tuning start point

#### 54.6.4 Enumeration Type Documentation

##### 54.6.4.4.1 anonymous enum

Enumerator

*kSDMMCHOST\_SupportHighSpeed* high speed capability  
*kSDMMCHOST\_SupportSuspendResume* suspend resume capability  
*kSDMMCHOST\_SupportVoltage3v3* 3V3 capability  
*kSDMMCHOST\_SupportVoltage3v0* 3V0 capability  
*kSDMMCHOST\_SupportVoltage1v8* 1V8 capability  
*kSDMMCHOST\_SupportVoltage1v2* 1V2 capability  
*kSDMMCHOST\_Support4BitDataWidth* 4 bit data width capability  
*kSDMMCHOST\_Support8BitDataWidth* 8 bit data width capability  
*kSDMMCHOST\_SupportDDRMode* DDR mode capability.  
*kSDMMCHOST\_SupportDetectCardByData3* data3 detect card capability  
*kSDMMCHOST\_SupportDetectCardByCD* CD detect card capability.  
*kSDMMCHOST\_SupportAutoCmd12* auto command 12 capability  
*kSDMMCHOST\_SupportSDR104* SDR104 capability.  
*kSDMMCHOST\_SupportSDR50* SDR50 capability.  
*kSDMMCHOST\_SupportHS200* HS200 capability.  
*kSDMMCHOST\_SupportHS400* HS400 capability.

##### 54.6.4.4.2 anonymous enum

Enumerator

*kSDMMCHOST\_EndianModeBig* Big endian mode.  
*kSDMMCHOST\_EndianModeHalfWordBig* Half word big endian mode.  
*kSDMMCHOST\_EndianModeLittle* Little endian mode.

##### 54.6.4.4.3 anonymous enum

Enumerator

*kSDMMCHOST\_StandardTuning* standard tuning type  
*kSDMMCHOST\_ManualTuning* manual tuning type

#### 54.6.4.4 anonymous enum

Enumerator

***kSDMMCHOST\_NoCacheControl*** sdmmc host cache control disabled

***kSDMMCHOST\_CacheControlRWBuffer*** sdmmc host cache control read/write buffer

#### 54.6.4.5 Function Documentation

##### 54.6.4.5.1 void SDMMCHOST\_SetCardBusWidth ( *sdmmchost\_t \* host*, *uint32\_t dataBusWidth* )

Parameters

<i>host</i>	host handler
<i>dataBusWidth</i>	data bus width

##### 54.6.4.5.2 static void SDMMCHOST\_SendCardActive ( *sdmmchost\_t \* host* ) [inline], [static]

Parameters

<i>host</i>	host handler
-------------	--------------

##### 54.6.4.5.3 static uint32\_t SDMMCHOST\_SetCardClock ( *sdmmchost\_t \* host*, *uint32\_t targetClock* ) [inline], [static]

Parameters

<i>host</i>	host handler
<i>targetClock</i>	target clock frequency

Return values

<i>actual</i>	clock frequency can be reach.
---------------	-------------------------------

##### 54.6.4.5.4 static bool SDMMCHOST\_IsCardBusy ( *sdmmchost\_t \* host* ) [inline], [static]

Parameters

<i>host</i>	host handler
-------------	--------------

Return values

<i>true</i>	is busy, false is idle.
-------------	-------------------------

**54.6.4.5.5 static uint32\_t SDMMCHOST\_GetSignalLineStatus ( sdmmchost\_t \* *host*, uint32\_t *signalLine* ) [inline], [static]**

Parameters

<i>host</i>	host handler
<i>signalLine</i>	signal line type, reference _sdmmc_signal_line

**54.6.4.5.6 static void SDMMCHOST\_EnableCardInt ( sdmmchost\_t \* *host*, bool *enable* ) [inline], [static]**

Parameters

<i>host</i>	host handler
<i>enable</i>	true is enable, false is disable.

**54.6.4.5.7 static void SDMMCHOST\_EnableDDRMode ( sdmmchost\_t \* *host*, bool *enable*, uint32\_t *nibblePos* ) [inline], [static]**

Parameters

<i>host</i>	host handler
<i>enable</i>	true is enable, false is disable.
<i>nibblePos</i>	nibble position indication. 0- the sequence is 'odd high nibble -> even high nibble -> odd low nibble -> even low nibble'; 1- the sequence is 'odd high nibble -> odd low nibble -> even high nibble -> even low nibble'.

**54.6.4.5.8 static void SDMMCHOST\_EnableHS400Mode ( sdmmchost\_t \* *host*, bool *enable* ) [inline], [static]**

Parameters

<i>host</i>	host handler
<i>enable</i>	true is enable, false is disable.

**54.6.4.5.9 static void SDMMCHOST\_EnableStrobeDII ( *sdmmchost\_t \* host, bool enable* )  
[inline], [static]**

Parameters

<i>host</i>	host handler
<i>enable</i>	true is enable, false is disable.

**54.6.4.5.10 status\_t SDMMCHOST\_StartBoot ( *sdmmchost\_t \* host, sdmmchost\_boot\_config\_t \* hostConfig, sdmmchost\_cmd\_t \* cmd, uint8\_t \* buffer* )**

Parameters

<i>host</i>	host handler
<i>hostConfig</i>	boot configuration
<i>cmd</i>	boot command
<i>buffer</i>	buffer address

**54.6.4.5.11 status\_t SDMMCHOST\_ReadBootData ( *sdmmchost\_t \* host, sdmmchost\_boot\_config\_t \* hostConfig, uint8\_t \* buffer* )**

Parameters

<i>host</i>	host handler
<i>hostConfig</i>	boot configuration
<i>buffer</i>	buffer address

**54.6.4.5.12 static void SDMMCHOST\_EnableBoot ( *sdmmchost\_t \* host, bool enable* )  
[inline], [static]**

Parameters

<i>host</i>	host handler
<i>enable</i>	true is enable, false is disable

#### 54.6.4.5.13 status\_t SDMMCHOST\_CardIntInit ( *sdmmchost\_t \* host, void \* sdioInt* )

Parameters

<i>host</i>	host handler
<i>sdioInt</i>	card interrupt configuration

#### 54.6.4.5.14 static void SDMMCHOST\_ForceClockOn ( *sdmmchost\_t \* host, bool enable* ) [inline], [static]

Parameters

<i>host</i>	host handler
<i>enable</i>	true is enable, false is disable.

#### 54.6.4.5.15 void SDMMCHOST\_SwitchToVoltage ( *sdmmchost\_t \* host, uint32\_t voltage* )

Parameters

<i>host</i>	host handler
<i>voltage</i>	switch to voltage level.

#### 54.6.4.5.16 status\_t SDMMCHOST\_CardDetectInit ( *sdmmchost\_t \* host, void \* cd* )

Parameters

<i>host</i>	host handler
-------------	--------------

<i>cd</i>	card detect configuration
-----------	---------------------------

#### 54.6.4.5.17 status\_t SDMMCHOST\_PollingCardDetectStatus ( *sdmmchost\_t \* host, uint32\_t waitCardStatus, uint32\_t timeout* )

Parameters

<i>host</i>	host handler
<i>waitCardStatus</i>	status which user want to wait
<i>timeout</i>	wait time out.

Return values

<i>kStatus_Success</i>	detect card insert
<i>kStatus_Fail</i>	card insert event fail

#### 54.6.4.5.18 uint32\_t SDMMCHOST\_CardDetectStatus ( *sdmmchost\_t \* host* )

Parameters

<i>host</i>	host handler
-------------	--------------

Return values

<i>kSD_Inserted,kSD_Removed</i>	
---------------------------------	--

#### 54.6.4.5.19 status\_t SDMMCHOST\_Init ( *sdmmchost\_t \* host* )

Thread safe function, please note that the function will create the mutex lock dynamically by default, so to avoid the mutex create redundantly, application must follow bellow sequence for card re-initialization

```
* SDMMCHOST_Deinit(host);
* SDMMCHOST_Init(host);
*
```

Parameters

<i>host</i>	host handler
-------------	--------------

Return values

<i>kStatus_Success</i>	host init success
<i>kStatus_Fail</i>	event fail

#### 54.6.4.5.20 void SDMMCHOST\_Deinit ( *sdmmchost\_t \* host* )

Please note it is a thread safe function.

Parameters

<i>host</i>	host handler
-------------	--------------

#### 54.6.4.5.21 void SDMMCHOST\_SetCardPower ( *sdmmchost\_t \* host, bool enable* )

Parameters

<i>host</i>	host handler
<i>enable</i>	true is power on, false is power down.

#### 54.6.4.5.22 *status\_t SDMMCHOST\_TransferFunction ( *sdmmchost\_t \* host, sdmmchost\_transfer\_t \* content* )*

Please note it is a thread safe function.

Note

the host transfer function support below functionality,

1. Non-cache line size alignment check on the data buffer, it is means that no matter the data buffer used for data transfer is align with cache line size or not, sdmmc host driver will use the address directly.
2. Cache line size alignment check on the data buffer, sdmmc host driver will check the data buffer address, if the buffer is not align with cache line size, sdmmc host driver will convert it to cache line size align buffer, the functionality is enabled by #define SDMMCHOST\_ENABLE\_CACHE\_LINE\_ALIGN\_TRANSFER 1 #define FSL\_USDHC\_ENABLE\_SCATTER\_GATHER\_TRANSFER 1U If application would like to enable the cache line size align functionality, please make sure the SDMMCHOST\_InstallCacheAlignBuffer is called before

submit data transfer request and make sure the installing buffer size is not smaller than  $2 * \text{cache line size}$ .

Parameters

<i>host</i>	host handler
<i>content</i>	transfer content.

#### 54.6.4.5.23 **status\_t SDMMCHOST\_ExecuteTuning ( *sdmmchost\_t \* host, uint32\_t tuningCmd, uint32\_t \* revBuf, uint32\_t blockSize* )**

Parameters

<i>host</i>	host handler
<i>tuningCmd</i>	tuning command.
<i>revBuf</i>	receive buffer pointer
<i>blockSize</i>	tuning data block size.

#### 54.6.4.5.24 **void SDMMCHOST\_Reset ( *sdmmchost\_t \* host* )**

Parameters

<i>host</i>	host handler
-------------	--------------

#### 54.6.4.5.25 **void SDMMCHOST\_ConvertDataToLittleEndian ( *sdmmchost\_t \* host, uint32\_t \* data, uint32\_t wordSize, uint32\_t format* )**

Parameters

<i>host</i>	host handler.
<i>data</i>	data buffer address.
<i>wordSize</i>	data buffer size in word.
<i>format</i>	data packet format.

## 54.7 SDMMC Common

### 54.7.1 Overview

The sdmmc common function and definition.

## Data Structures

- struct `sd_detect_card_t`  
`sd card detect` [More...](#)
- struct `sd_io_voltage_t`  
`io voltage control configuration` [More...](#)
- struct `sd_usr_param_t`  
`sdcard user parameter` [More...](#)
- struct `sdio_card_int_t`  
`card interrupt application callback` [More...](#)
- struct `sdio_usr_param_t`  
`sdio user parameter` [More...](#)
- struct `sdio_fbr_t`  
`sdio card FBR register` [More...](#)
- struct `sdio_common_cis_t`  
`sdio card common CIS` [More...](#)
- struct `sdio_func_cis_t`  
`sdio card function CIS` [More...](#)
- struct `sd_status_t`  
`SD card status.` [More...](#)
- struct `sd_cid_t`  
`SD card CID register.` [More...](#)
- struct `sd_csd_t`  
`SD card CSD register.` [More...](#)
- struct `sd_scr_t`  
`SD card SCR register.` [More...](#)
- struct `mmc_cid_t`  
`MMC card CID register.` [More...](#)
- struct `mmc_csd_t`  
`MMC card CSD register.` [More...](#)
- struct `mmc_extended_csd_t`  
`MMC card Extended CSD register (unit: byte).` [More...](#)
- struct `mmc_extended_csd_config_t`  
`MMC Extended CSD configuration.` [More...](#)
- struct `mmc_boot_config_t`  
`MMC card boot configuration definition.` [More...](#)

## Macros

- #define `SWAP_WORD_BYTSEQUENCE(x)` (`__REV(x)`)  
`Reverse byte sequence in uint32_t.`
- #define `SWAP_HALF_WROD_BYTSEQUENCE(x)` (`__REV16(x)`)

- Reverse byte sequence for each half word in `uint32_t`.
- `#define FSL_SDMMC_MAX_VOLTAGE_RETRIES` (1000U)  
Maximum loop count to check the card operation voltage range.
- `#define FSL_SDMMC_MAX_CMD_RETRIES` (10U)  
Maximum loop count to send the cmd.
- `#define FSL_SDMMC_DEFAULT_BLOCK_SIZE` (512U)  
Default block size.
- `#define SDMMC_DATA_BUFFER_ALIGN_CACHE` `FSL_FEATURE_L1DCACHE_LINESIZE_BYT`  
make sure the internal buffer address is cache align
- `#define FSL_SDMMC_CARD_INTERNAL_BUFFER_SIZE` (`FSL_SDMMC_DEFAULT_BLOCK_SIZE + SDMMC_DATA_BUFFER_ALIGN_CACHE`)  
sdmmc card internal buffer size
- `#define FSL_SDMMC_CARD_MAX_BUS_FREQ`(max, target) ((max) == 0U ? (target) : ((max) > (target) ? (target) : (max)))  
get maximum freq
- `#define SDMMC_LOG`(format,...)  
SD/MMC error log.
- `#define SDMMC_CLOCK_400KHZ` (4000000U)  
SD/MMC card initialization clock frequency.
- `#define SD_CLOCK_25MHZ` (25000000U)  
SD card bus frequency 1 in high-speed mode.
- `#define SD_CLOCK_50MHZ` (50000000U)  
SD card bus frequency 2 in high-speed mode.
- `#define SD_CLOCK_100MHZ` (100000000U)  
SD card bus frequency in SDR50 mode.
- `#define SD_CLOCK_208MHZ` (208000000U)  
SD card bus frequency in SDR104 mode.
- `#define MMC_CLOCK_26MHZ` (26000000U)  
MMC card bus frequency 1 in high-speed mode.
- `#define MMC_CLOCK_52MHZ` (52000000U)  
MMC card bus frequency 2 in high-speed mode.
- `#define MMC_CLOCK_DDR52` (52000000U)  
MMC card bus frequency in high-speed DDR52 mode.
- `#define MMC_CLOCK_HS200` (200000000U)  
MMC card bus frequency in high-speed HS200 mode.
- `#define MMC_CLOCK_HS400` (400000000U)  
MMC card bus frequency in high-speed HS400 mode.
- `#define SDMMC_MASK`(bit) (1UL << (bit))  
mask convert
- `#define SDMMC_R1_ALL_ERROR_FLAG`  
*R1 all the error flag.*
- `#define SDMMC_R1_CURRENT_STATE`(x) (((x)&0x00001E00U) >> 9U)  
*R1: current state.*
- `#define SDSPI_R7_VERSION_SHIFT` (28U)  
The bit mask for COMMAND VERSION field in R7.
- `#define SDSPI_R7_VERSION_MASK` (0xFU)  
The bit mask for COMMAND VERSION field in R7.
- `#define SDSPI_R7_VOLTAGE_SHIFT` (8U)  
The bit shift for VOLTAGE ACCEPTED field in R7.
- `#define SDSPI_R7_VOLTAGE_MASK` (0xFU)

- `#define SDSPI_R7_VOLTAGE_27_36_MASK (0x1U << SDSPI_R7_VOLTAGE_SHIFT)`  
*The bit mask for VOLTAGE ACCEPTED field in R7.*
- `#define SDSPI_R7_VOLTAGE_2.7V_to_3.6V_MASK (0x1U << SDSPI_R7_VOLTAGE_SHIFT)`  
*The bit mask for VOLTAGE 2.7V to 3.6V field in R7.*
- `#define SDSPI_R7_ECHO_SHIFT (0U)`  
*The bit shift for ECHO field in R7.*
- `#define SDSPI_R7_ECHO_MASK (0xFFU)`  
*The bit mask for ECHO field in R7.*
- `#define SDSPI_DATA_ERROR_TOKEN_MASK (0xFU)`  
*Data error token mask.*
- `#define SDSPI_DATA_RESPONSE_TOKEN_MASK (0x1FU)`  
*Mask for data response bits.*
- `#define SDIO_CCCR_REG_NUMBER (0x16U)`  
*sdio card cccr register number*
- `#define SDIO_IO_READY_TIMEOUT_UNIT (10U)`  
*sdio IO ready timeout steps*
- `#define SDIO_CMD_ARGUMENT_RW_POS (31U)`  
*read/write flag position*
- `#define SDIO_CMD_ARGUMENT_FUNC_NUM_POS (28U)`  
*function number position*
- `#define SDIO_DIRECT_CMD_ARGUMENT_RAW_POS (27U)`  
*direct raw flag position*
- `#define SDIO_CMD_ARGUMENT_REG_ADDR_POS (9U)`  
*direct reg addr position*
- `#define SDIO_CMD_ARGUMENT_REG_ADDR_MASK (0x1FFFFU)`  
*direct reg addr mask*
- `#define SDIO_DIRECT_CMD_DATA_MASK (0xFFU)`  
*data mask*
- `#define SDIO_EXTEND_CMD_ARGUMENT_BLOCK_MODE_POS (27U)`  
*extended command argument block mode bit position*
- `#define SDIO_EXTEND_CMD_ARGUMENT_OP_CODE_POS (26U)`  
*extended command argument OP Code bit position*
- `#define SDIO_EXTEND_CMD_BLOCK_MODE_MASK (0x08000000U)`  
*block mode mask*
- `#define SDIO_EXTEND_CMD_OP_CODE_MASK (0x04000000U)`  
*op code mask*
- `#define SDIO_EXTEND_CMD_COUNT_MASK (0x1FFU)`  
*byte/block count mask*
- `#define SDIO_MAX_BLOCK_SIZE (2048U)`  
*max block size*
- `#define SDIO_FBR_BASE(x) ((x)*0x100U)`  
*function basic register*
- `#define SDIO_TPL_CODE_END (0xFFU)`  
*tuple end*
- `#define SDIO_TPL_CODE_MANIFID (0x20U)`  
*manufacturer ID*
- `#define SDIO_TPL_CODE_FUNCID (0x21U)`  
*function ID*
- `#define SDIO_TPL_CODE_FUNCE (0x22U)`  
*function extension tuple*
- `#define SDIO_OCR_VOLTAGE_WINDOW_MASK (0xFFFFU << 8U)`  
*sdio ocr voltage window mask*

- #define **SDIO\_OCR\_IO\_NUM\_MASK** (7U << kSDIO\_OcrIONumber)
 

*sdio ocr register IO NUMBER mask*
- #define **SDIO\_CCCR\_SUPPORT\_HIGHSPEED** (1UL << 9U)
 

*UHS timing mode flag.*
- #define **SDIO\_CCCR\_DRIVER\_TYPE\_MASK** (3U << 4U)
 

*Driver type flag.*
- #define **SDIO\_CCCR\_ASYNC\_INT\_MASK** (1U)
 

*async interrupt flag*
- #define **SDIO\_CCCR\_SUPPORT\_8BIT\_BUS** (1UL << 18U)
 

*8 bit data bus flag*
- #define **MMC\_OCR\_V170TO195\_SHIFT** (7U)
 

*The bit mask for VOLTAGE WINDOW 1.70V to 1.95V field in OCR.*
- #define **MMC\_OCR\_V170TO195\_MASK** (0x00000080U)
 

*The bit mask for VOLTAGE WINDOW 1.70V to 1.95V field in OCR.*
- #define **MMC\_OCR\_V200TO260\_SHIFT** (8U)
 

*The bit shift for VOLTAGE WINDOW 2.00V to 2.60V field in OCR.*
- #define **MMC\_OCR\_V200TO260\_MASK** (0x00007F00U)
 

*The bit mask for VOLTAGE WINDOW 2.00V to 2.60V field in OCR.*
- #define **MMC\_OCR\_V270TO360\_SHIFT** (15U)
 

*The bit shift for VOLTAGE WINDOW 2.70V to 3.60V field in OCR.*
- #define **MMC\_OCR\_V270TO360\_MASK** (0x00FF8000U)
 

*The bit mask for VOLTAGE WINDOW 2.70V to 3.60V field in OCR.*
- #define **MMC\_OCR\_ACCESS\_MODE\_SHIFT** (29U)
 

*The bit shift for ACCESS MODE field in OCR.*
- #define **MMC\_OCR\_ACCESS\_MODE\_MASK** (0x60000000U)
 

*The bit mask for ACCESS MODE field in OCR.*
- #define **MMC\_OCR\_BUSY\_SHIFT** (31U)
 

*The bit shift for BUSY field in OCR.*
- #define **MMC\_OCR\_BUSY\_MASK** (1U << MMC\_OCR\_BUSY\_SHIFT)
 

*The bit mask for BUSY field in OCR.*
- #define **MMC\_TRANSFER\_SPEED\_FREQUENCY\_UNIT\_SHIFT** (0U)
 

*The bit shift for FREQUENCY UNIT field in TRANSFER SPEED(TRAN-SPEED in Extended CSD)*
- #define **MMC\_TRANSFER\_SPEED\_FREQUENCY\_UNIT\_MASK** (0x07U)
 

*The bit mask for FREQUENCY UNIT in TRANSFER SPEED.*
- #define **MMC\_TRANSFER\_SPEED\_MULTIPLIER\_SHIFT** (3U)
 

*The bit shift for MULTIPLIER field in TRANSFER SPEED.*
- #define **MMC\_TRANSFER\_SPEED\_MULTIPLIER\_MASK** (0x78U)
 

*The bit mask for MULTIPLIER field in TRANSFER SPEED.*
- #define **READ\_MMC\_TRANSFER\_SPEED\_FREQUENCY\_UNIT(CSD)** (((CSD).transferSpeed) & **MMC\_TRANSFER\_SPEED\_FREQUENCY\_UNIT\_MASK**) >> **MMC\_TRANSFER\_SPEED\_FREQUENCY\_UNIT\_SHIFT**)
 

*Read the value of FREQUENCY UNIT in TRANSFER SPEED.*
- #define **READ\_MMC\_TRANSFER\_SPEED\_MULTIPLIER(CSD)** (((CSD).transferSpeed) & **MMC\_TRANSFER\_SPEED\_MULTIPLIER\_MASK**) >> **MMC\_TRANSFER\_SPEED\_MULTIPLIER\_SHIFT**)
 

*Read the value of MULTIPLIER filed in TRANSFER SPEED.*
- #define **MMC\_POWER\_CLASS\_4BIT\_MASK** (0x0FU)
 

*The power class value bit mask when bus in 4 bit mode.*
- #define **MMC\_POWER\_CLASS\_8BIT\_MASK** (0xF0U)
 

*The power class current value bit mask when bus in 8 bit mode.*
- #define **MMC\_CACHE\_CONTROL\_ENABLE** (1U)

- `mmc cache control enable`
- `#define MMC_CACHE_TRIGGER_FLUSH (1U)`
- mmc cache flush*
- `#define MMC_DATA_BUS_WIDTH_TYPE_NUMBER (3U)`  
*The number of data bus width type.*
- `#define MMC_PARTITION_CONFIG_PARTITION_ACCESS_SHIFT (0U)`  
*The bit shift for PARTITION ACCESS filed in BOOT CONFIG (BOOT\_CONFIG in Extend CSD).*
- `#define MMC_PARTITION_CONFIG_PARTITION_ACCESS_MASK (0x00000007U)`  
*The bit mask for PARTITION ACCESS field in BOOT CONFIG.*
- `#define MMC_PARTITION_CONFIG_PARTITION_ENABLE_SHIFT (3U)`  
*The bit shift for PARTITION ENABLE field in BOOT CONFIG.*
- `#define MMC_PARTITION_CONFIG_PARTITION_ENABLE_MASK (0x00000038U)`  
*The bit mask for PARTITION ENABLE field in BOOT CONFIG.*
- `#define MMC_PARTITION_CONFIG_BOOT_ACK_SHIFT (6U)`  
*The bit shift for ACK field in BOOT CONFIG.*
- `#define MMC_PARTITION_CONFIG_BOOT_ACK_MASK (0x00000040U)`  
*The bit mask for ACK field in BOOT CONFIG.*
- `#define MMC_BOOT_BUS_CONDITION_BUS_WIDTH_SHIFT (0U)`  
*The bit shift for BOOT BUS WIDTH field in BOOT CONFIG.*
- `#define MMC_BOOT_BUS_CONDITION_BUS_WIDTH_MASK (3U)`  
*The bit mask for BOOT BUS WIDTH field in BOOT CONFIG.*
- `#define MMC_BOOT_BUS_CONDITION_RESET_BUS_CONDITION_SHIFT (2U)`  
*The bit shift for BOOT BUS WIDTH RESET field in BOOT CONFIG.*
- `#define MMC_BOOT_BUS_CONDITION_RESET_BUS_CONDITION_MASK (4U)`  
*The bit mask for BOOT BUS WIDTH RESET field in BOOT CONFIG.*
- `#define MMC_BOOT_BUS_CONDITION_BOOT_MODE_SHIFT (3U)`  
*The bit shift for BOOT MODE field in BOOT CONFIG.*
- `#define MMC_BOOT_BUS_CONDITION_BOOT_MODE_MASK (0x18U)`  
*The bit mask for BOOT MODE field in BOOT CONFIG.*
- `#define MMC_EXTENDED_CSD_BYTES (512U)`  
*The length of Extended CSD register, unit as bytes.*
- `#define MMC_DEFAULT_RELATIVE_ADDRESS (2UL)`  
*MMC card default relative address.*
- `#define SD_PRODUCT_NAME_BYTES (5U)`  
*SD card product name length united as bytes.*
- `#define SD_AU_START_VALUE (1U)`  
*SD AU start value.*
- `#define SD_UHS_AU_START_VALUE (7U)`  
*SD UHS AU start value.*
- `#define SD_TRANSFER_SPEED_RATE_UNIT_SHIFT (0U)`  
*The bit shift for RATE UNIT field in TRANSFER SPEED.*
- `#define SD_TRANSFER_SPEED_RATE_UNIT_MASK (0x07U)`  
*The bit mask for RATE UNIT field in TRANSFER SPEED.*
- `#define SD_TRANSFER_SPEED_TIME_VALUE_SHIFT (2U)`  
*The bit shift for TIME VALUE field in TRANSFER SPEED.*
- `#define SD_TRANSFER_SPEED_TIME_VALUE_MASK (0x78U)`  
*The bit mask for TIME VALUE field in TRANSFER SPEED.*
- `#define SD_RD_TRANSFER_SPEED_RATE_UNIT(x) (((x.transferSpeed) & SD_TRANSFER_SPEED_RATE_UNIT_MASK) >> SD_TRANSFER_SPEED_RATE_UNIT_SHIFT)`  
*Read the value of FREQUENCY UNIT in TRANSFER SPEED field.*
- `#define SD_RD_TRANSFER_SPEED_TIME_VALUE(x) (((x.transferSpeed) & SD_TRANSFER-`

`_SPEED_TIME_VALUE_MASK) >> SD_TRANSFER_SPEED_TIME_VALUE_SHIFT)`

*Read the value of TIME VALUE in TRANSFER SPEED field.*

- `#define MMC_PRODUCT_NAME_BYTES (6U)`  
*MMC card product name length united as bytes.*
- `#define MMC_SWITCH_COMMAND_SET_SHIFT (0U)`  
*The bit shift for COMMAND SET field in SWITCH command.*
- `#define MMC_SWITCH_COMMAND_SET_MASK (0x00000007U)`  
*The bit mask for COMMAND set field in SWITCH command.*
- `#define MMC_SWITCH_VALUE_SHIFT (8U)`  
*The bit shift for VALUE field in SWITCH command.*
- `#define MMC_SWITCH_VALUE_MASK (0x0000FF00U)`  
*The bit mask for VALUE field in SWITCH command.*
- `#define MMC_SWITCH_BYTE_INDEX_SHIFT (16U)`  
*The bit shift for BYTE INDEX field in SWITCH command.*
- `#define MMC_SWITCH_BYTE_INDEX_MASK (0x00FF0000U)`  
*The bit mask for BYTE INDEX field in SWITCH command.*
- `#define MMC_SWITCH_ACCESS_MODE_SHIFT (24U)`  
*The bit shift for ACCESS MODE field in SWITCH command.*
- `#define MMC_SWITCH_ACCESS_MODE_MASK (0x03000000U)`  
*The bit mask for ACCESS MODE field in SWITCH command.*

## Typedefs

- `typedef void(* sd_cd_t )(bool isInserted, void *userData)`  
*card detect application callback definition*
- `typedef bool(* sd_cd_status_t )(void)`  
*card detect status*
- `typedef void(* sd_io_voltage_func_t )(sdmmc_operation_voltage_t voltage)`  
*card switch voltage function pointer*
- `typedef void(* sd_pwr_t )(bool enable)`  
*card power control function pointer*
- `typedef void(* sd_io_strength_t )(uint32_t busFreq)`  
*card io strength control*
- `typedef void(* sdio_int_t )(void *userData)`  
*card interrupt function pointer*

## Enumerations

- enum {
   
kStatus\_SDMMC\_NotSupportYet = MAKE\_STATUS(kStatusGroup\_SDMMC, 0U),
   
kStatus\_SDMMC\_TransferFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 1U),
   
kStatus\_SDMMC\_SetCardBlockSizeFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 2U),
   
kStatus\_SDMMC\_HostNotSupport = MAKE\_STATUS(kStatusGroup\_SDMMC, 3U),
   
kStatus\_SDMMC\_CardNotSupport = MAKE\_STATUS(kStatusGroup\_SDMMC, 4U),
   
kStatus\_SDMMC\_AllSendCidFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 5U),
   
kStatus\_SDMMC\_SendRelativeAddressFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 6U),
   
kStatus\_SDMMC\_SendCsdFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 7U),
   
kStatus\_SDMMC\_SelectCardFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 8U),
   
kStatus\_SDMMC\_SendScrFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 9U),
   
kStatus\_SDMMC\_SetDataBusWidthFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 10U),
   
kStatus\_SDMMC\_GoIdleFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 11U),
   
kStatus\_SDMMC\_HandShakeOperationConditionFailed,
   
kStatus\_SDMMC\_SendApplicationCommandFailed,
   
kStatus\_SDMMC\_SwitchFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 14U),
   
kStatus\_SDMMC\_StopTransmissionFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 15U),
   
kStatus\_SDMMC\_WaitWriteCompleteFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 16U),
   
kStatus\_SDMMC\_SetBlockCountFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 17U),
   
kStatus\_SDMMC\_SetRelativeAddressFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 18U),
   
kStatus\_SDMMC\_SwitchBusTimingFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 19U),
   
kStatus\_SDMMC\_SendExtendedCsdFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 20U),
   
kStatus\_SDMMC\_ConfigureBootFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 21U),
   
kStatus\_SDMMC\_ConfigureExtendedCsdFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 22-U),
   
kStatus\_SDMMC\_EnableHighCapacityEraseFailed,
   
kStatus\_SDMMC\_SendTestPatternFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 24U),
   
kStatus\_SDMMC\_ReceiveTestPatternFailed = MAKE\_STATUS(kStatusGroup\_SDMMC, 25U),
   
kStatus\_SDMMC\_SDIO\_ResponseError = MAKE\_STATUS(kStatusGroup\_SDMMC, 26U),
   
kStatus\_SDMMC\_SDIO\_InvalidArgument,
   
kStatus\_SDMMC\_SDIO\_SendOperationConditionFail,
   
kStatus\_SDMMC\_InvalidVoltage = MAKE\_STATUS(kStatusGroup\_SDMMC, 29U),
   
kStatus\_SDMMC\_SDIO\_SwitchHighSpeedFail = MAKE\_STATUS(kStatusGroup\_SDMMC, 30-U),
   
kStatus\_SDMMC\_SDIO\_ReadCISFail = MAKE\_STATUS(kStatusGroup\_SDMMC, 31U),
   
kStatus\_SDMMC\_SDIO\_InvalidCard = MAKE\_STATUS(kStatusGroup\_SDMMC, 32U),
   
kStatus\_SDMMC\_TuningFail = MAKE\_STATUS(kStatusGroup\_SDMMC, 33U),
   
kStatus\_SDMMC\_SwitchVoltageFail = MAKE\_STATUS(kStatusGroup\_SDMMC, 34U),
   
kStatus\_SDMMC\_SwitchVoltage18VFail33VSuccess = MAKE\_STATUS(kStatusGroup\_SDMM-

C, 35U),

```
kStatus_SDMMC_ReTuningRequest = MAKE_STATUS(kStatusGroup_SDMMC, 36U),
kStatus_SDMMC_SetDriverStrengthFail = MAKE_STATUS(kStatusGroup_SDMMC, 37U),
kStatus_SDMMC_SetPowerClassFail = MAKE_STATUS(kStatusGroup_SDMMC, 38U),
kStatus_SDMMC_HostNotReady = MAKE_STATUS(kStatusGroup_SDMMC, 39U),
kStatus_SDMMC_CardDetectFailed = MAKE_STATUS(kStatusGroup_SDMMC, 40U),
kStatus_SDMMC_AuSizeNotSetProperly = MAKE_STATUS(kStatusGroup_SDMMC, 41U),
kStatus_SDMMC_PollingCardIdleFailed = MAKE_STATUS(kStatusGroup_SDMMC, 42U),
kStatus_SDMMC_DeselectCardFailed = MAKE_STATUS(kStatusGroup_SDMMC, 43U),
kStatus_SDMMC_CardStatusIdle = MAKE_STATUS(kStatusGroup_SDMMC, 44U),
kStatus_SDMMC_CardStatusBusy = MAKE_STATUS(kStatusGroup_SDMMC, 45U),
kStatus_SDMMC_CardInitFailed = MAKE_STATUS(kStatusGroup_SDMMC, 46U) }
```

*SD/MMC card API's running status.*

- enum {
   
kSDMMC\_SignalLineCmd = 1U,
   
kSDMMC\_SignalLineData0 = 2U,
   
kSDMMC\_SignalLineData1 = 4U,
   
kSDMMC\_SignalLineData2 = 8U,
   
kSDMMC\_SignalLineData3 = 16U,
   
kSDMMC\_SignalLineData4 = 32U,
   
kSDMMC\_SignalLineData5 = 64U,
   
kSDMMC\_SignalLineData6 = 128U,
   
kSDMMC\_SignalLineData7 = 256U }

*sdmmc signal line*

- enum **sdmmc\_operation\_voltage\_t** {
   
kSDMMC\_OperationVoltageNone = 0U,
   
kSDMMC\_OperationVoltage330V = 1U,
   
kSDMMC\_OperationVoltage300V = 2U,
   
kSDMMC\_OperationVoltage180V = 3U }

*card operation voltage*

- enum {
   
kSDMMC\_BusWidth1Bit = 0U,
   
kSDMMC\_BusWidth4Bit = 1U,
   
kSDMMC\_BusWidth8Bit = 2U }

*card bus width*

- enum { **kSDMMC\_Support8BitWidth** = 1U }

*sdmmc capability flag*

- enum {
   
kSDMMC\_DataPacketFormatLSBFirst,
   
kSDMMC\_DataPacketFormatMSBFirst }

*@ brief sdmmc data packet format*

- enum **sd\_detect\_card\_type\_t** {
   
kSD\_DetectCardByGpioCD,
   
kSD\_DetectCardByHostCD,
   
kSD\_DetectCardByHostDATA3 }

*sd card detect type*

- enum {
   
  kSD\_Inserted = 1U,
   
  kSD\_Removed = 0U }
   
    *@ brief SD card detect status*
- enum {
   
  kSD\_DAT3PullDown = 0U,
   
  kSD\_DAT3PullUp = 1U }
   
    *@ brief SD card detect status*
- enum **sd\_io\_voltage\_ctrl\_type\_t** {
   
  kSD\_IOVoltageCtrlNotSupport = 0U,
   
  kSD\_IOVoltageCtrlByGpio = 2U }
   
    *io voltage control type*
- enum {
   
  kSDMMC\_R1OutOfRangeFlag = 31,
   
  kSDMMC\_R1AddressErrorFlag = 30,
   
  kSDMMC\_R1BlockLengthErrorFlag = 29,
   
  kSDMMC\_R1EraseSequenceErrorFlag = 28,
   
  kSDMMC\_R1EraseParameterErrorFlag = 27,
   
  kSDMMC\_R1WriteProtectViolationFlag = 26,
   
  kSDMMC\_R1CardIsLockedFlag = 25,
   
  kSDMMC\_R1LockUnlockFailedFlag = 24,
   
  kSDMMC\_R1CommandCrcErrorFlag = 23,
   
  kSDMMC\_R1IllegalCommandFlag = 22,
   
  kSDMMC\_R1CardEccFailedFlag = 21,
   
  kSDMMC\_R1CardControllerErrorFlag = 20,
   
  kSDMMC\_R1ErrorFlag = 19,
   
  kSDMMC\_R1CidCsdOverwriteFlag = 16,
   
  kSDMMC\_R1WriteProtectEraseSkipFlag = 15,
   
  kSDMMC\_R1CardEccDisabledFlag = 14,
   
  kSDMMC\_R1EraseResetFlag = 13,
   
  kSDMMC\_R1ReadyForDataFlag = 8,
   
  kSDMMC\_R1SwitchErrorFlag = 7,
   
  kSDMMC\_R1ApplicationCommandFlag = 5,
   
  kSDMMC\_R1AuthenticationSequenceErrorFlag = 3 }
   
    *Card status bit in R1.*
- enum **sdmmc\_r1\_current\_state\_t** {
   
  kSDMMC\_R1StateIdle = 0U,
   
  kSDMMC\_R1StateReady = 1U,
   
  kSDMMC\_R1StateIdentify = 2U,
   
  kSDMMC\_R1StateStandby = 3U,
   
  kSDMMC\_R1StateTransfer = 4U,
   
  kSDMMC\_R1StateSendData = 5U,
   
  kSDMMC\_R1StateReceiveData = 6U,
   
  kSDMMC\_R1StateProgram = 7U,
   
  kSDMMC\_R1StateDisconnect = 8U }
   
    *CURRENT\_STATE filed in R1.*

- enum {
   
  kSDSPI\_R1InIdleStateFlag = (1U << 0U),
   
  kSDSPI\_R1EraseResetFlag = (1U << 1U),
   
  kSDSPI\_R1IllegalCommandFlag = (1U << 2U),
   
  kSDSPI\_R1CommandCrcErrorFlag = (1U << 3U),
   
  kSDSPI\_R1EraseSequenceErrorFlag = (1U << 4U),
   
  kSDSPI\_R1AddressErrorFlag = (1U << 5U),
   
  kSDSPI\_R1ParameterErrorFlag = (1U << 6U) }

*Error bit in SPI mode R1.*

- enum {
   
  kSDSPI\_R2CardLockedFlag = (1U << 0U),
   
  kSDSPI\_R2WriteProtectEraseSkip = (1U << 1U),
   
  kSDSPI\_R2LockUnlockFailed = (1U << 1U),
   
  kSDSPI\_R2ErrorFlag = (1U << 2U),
   
  kSDSPI\_R2CardControllerErrorFlag = (1U << 3U),
   
  kSDSPI\_R2CardEccFailedFlag = (1U << 4U),
   
  kSDSPI\_R2WriteProtectViolationFlag = (1U << 5U),
   
  kSDSPI\_R2EraseParameterErrorFlag = (1U << 6U),
   
  kSDSPI\_R2OutOfRangeFlag = (1U << 7U),
   
  kSDSPI\_R2CsdOverwriteFlag = (1U << 7U) }

*Error bit in SPI mode R2.*

- enum {
   
  kSDSPI\_DataErrorTokenError = (1U << 0U),
   
  kSDSPI\_DataErrorTokenCardControllerError = (1U << 1U),
   
  kSDSPI\_DataErrorTokenCardEccFailed = (1U << 2U),
   
  kSDSPI\_DataErrorTokenOutOfRange = (1U << 3U) }

*Data Error Token mask bit.*

- enum **sdspi\_data\_token\_t** {
   
  kSDSPI\_DataTokenBlockRead = 0xFEU,
   
  kSDSPI\_DataTokenSingleBlockWrite = 0xFEU,
   
  kSDSPI\_DataTokenMultipleBlockWrite = 0xFCU,
   
  kSDSPI\_DataTokenStopTransfer = 0xFDU }

*Data Token.*

- enum **sdspi\_data\_response\_token\_t** {
   
  kSDSPI\_DataResponseTokenAccepted = 0x05U,
   
  kSDSPI\_DataResponseTokenCrcError = 0x0BU,
   
  kSDSPI\_DataResponseTokenWriteError = 0x0DU }

*Data Response Token.*

- enum **sd\_command\_t** {
   
  kSD\_SendRelativeAddress = 3U,
   
  kSD\_Switch = 6U,
   
  kSD\_SendInterfaceCondition = 8U,
   
  kSD\_VoltageSwitch = 11U,
   
  kSD\_SpeedClassControl = 20U,
   
  kSD\_EraseWriteBlockStart = 32U,
   
  kSD\_EraseWriteBlockEnd = 33U,

- ```
kSD_SendTuningBlock = 19U }
    SD card individual commands.
```
- enum `sdspi_command_t` { `kSDSPI_CommandCrc` = 59U }
 SDSPI individual commands.
  - enum `sd_application_command_t` {
 `kSD_ApplicationSetBusWidth` = 6U,
 `kSD_ApplicationStatus` = 13U,
 `kSD_ApplicationSendNumberWriteBlocks` = 22U,
 `kSD_ApplicationSetWriteBlockEraseCount` = 23U,
 `kSD_ApplicationSendOperationCondition` = 41U,
 `kSD_ApplicationSetClearCardDetect` = 42U,
 `kSD_ApplicationSendScr` = 51U }

 SD card individual application commands.
  - enum {
 `kSDMMC_CommandClassBasic` = (1U << 0U),
 `kSDMMC_CommandClassBlockRead` = (1U << 2U),
 `kSDMMC_CommandClassBlockWrite` = (1U << 4U),
 `kSDMMC_CommandClassErase` = (1U << 5U),
 `kSDMMC_CommandClassWriteProtect` = (1U << 6U),
 `kSDMMC_CommandClassLockCard` = (1U << 7U),
 `kSDMMC_CommandClassApplicationSpecific` = (1U << 8U),
 `kSDMMC_CommandClassInputOutputMode` = (1U << 9U),
 `kSDMMC_CommandClassSwitch` = (1U << 10U) }

 SD card command class.
  - enum {
 `kSD_OcrPowerUpBusyFlag` = 31,
 `kSD_OcrHostCapacitySupportFlag` = 30,
 `kSD_OcrCardCapacitySupportFlag` = `kSD_OcrHostCapacitySupportFlag`,
 `kSD_OcrSwitch18RequestFlag` = 24,
 `kSD_OcrSwitch18AcceptFlag` = `kSD_OcrSwitch18RequestFlag`,
 `kSD_OcrVdd27_28Flag` = 15,
 `kSD_OcrVdd28_29Flag` = 16,
 `kSD_OcrVdd29_30Flag` = 17,
 `kSD_OcrVdd30_31Flag` = 18,
 `kSD_OcrVdd31_32Flag` = 19,
 `kSD_OcrVdd32_33Flag` = 20,
 `kSD_OcrVdd33_34Flag` = 21,
 `kSD_OcrVdd34_35Flag` = 22,
 `kSD_OcrVdd35_36Flag` = 23 }

 OCR register in SD card.
  - enum {
 `kSD_SpecificationVersion1_0` = (1U << 0U),
 `kSD_SpecificationVersion1_1` = (1U << 1U),
 `kSD_SpecificationVersion2_0` = (1U << 2U),
 `kSD_SpecificationVersion3_0` = (1U << 3U) }

 SD card specification version number.

- enum `sd_switch_mode_t` {
   
  `kSD_SwitchCheck` = 0U,
   
  `kSD_SwitchSet` = 1U }
   
    *SD card switch mode.*
- enum {
   
  `kSD_CsdReadBlockPartialFlag` = (1U << 0U),
   
  `kSD_CsdWriteBlockMisalignFlag` = (1U << 1U),
   
  `kSD_CsdReadBlockMisalignFlag` = (1U << 2U),
   
  `kSD_CsdDsrImplementedFlag` = (1U << 3U),
   
  `kSD_CsdEraseBlockEnabledFlag` = (1U << 4U),
   
  `kSD_CsdWriteProtectGroupEnabledFlag` = (1U << 5U),
   
  `kSD_CsdWriteBlockPartialFlag` = (1U << 6U),
   
  `kSD_CsdFileFormatGroupFlag` = (1U << 7U),
   
  `kSD_CsdCopyFlag` = (1U << 8U),
   
  `kSD_CsdPermanentWriteProtectFlag` = (1U << 9U),
   
  `kSD_CsdTemporaryWriteProtectFlag` = (1U << 10U) }
   
    *SD card CSD register flags.*
- enum {
   
  `kSD_ScrDataStatusAfterErase` = (1U << 0U),
   
  `kSD_ScrSdSpecification3` = (1U << 1U) }
   
    *SD card SCR register flags.*
- enum {
   
  `kSD_FunctionSDR12Deafult` = 0U,
   
  `kSD_FunctionSDR25HighSpeed` = 1U,
   
  `kSD_FunctionSDR50` = 2U,
   
  `kSD_FunctionSDR104` = 3U,
   
  `kSD_FunctionDDR50` = 4U }
   
    *SD timing function number.*
- enum {
   
  `kSD_GroupTimingMode` = 0U,
   
  `kSD_GroupCommandSystem` = 1U,
   
  `kSD_GroupDriverStrength` = 2U,
   
  `kSD_GroupCurrentLimit` = 3U }  
*SD group number.*
- enum `sd_timing_mode_t` {
   
  `kSD_TimingSDR12DefaultMode` = 0U,
   
  `kSD_TimingSDR25HighSpeedMode` = 1U,
   
  `kSD_TimingSDR50Mode` = 2U,
   
  `kSD_TimingSDR104Mode` = 3U,
   
  `kSD_TimingDDR50Mode` = 4U }  
*SD card timing mode flags.*
- enum `sd_driver_strength_t` {
   
  `kSD_DriverStrengthTypeB` = 0U,
   
  `kSD_DriverStrengthTypeA` = 1U,
   
  `kSD_DriverStrengthTypeC` = 2U,
   
  `kSD_DriverStrengthTypeD` = 3U }

- SD card driver strength.*
- enum `sd_max_current_t` {  
  `kSD_CurrentLimit200MA` = 0U,  
  `kSD_CurrentLimit400MA` = 1U,  
  `kSD_CurrentLimit600MA` = 2U,  
  `kSD_CurrentLimit800MA` = 3U }
- SD card current limit.*
- enum `sdmmc_command_t` {  
  `kSDMMC_GoIdleState` = 0U,  
  `kSDMMC_AllSendCid` = 2U,  
  `kSDMMC_SetDsr` = 4U,  
  `kSDMMC_SelectCard` = 7U,  
  `kSDMMC_SendCsd` = 9U,  
  `kSDMMC_SendCid` = 10U,  
  `kSDMMC_StopTransmission` = 12U,  
  `kSDMMC_SendStatus` = 13U,  
  `kSDMMC_GoInactiveState` = 15U,  
  `kSDMMC_SetBlockLength` = 16U,  
  `kSDMMC_ReadSingleBlock` = 17U,  
  `kSDMMC_ReadMultipleBlock` = 18U,  
  `kSDMMC_SetBlockCount` = 23U,  
  `kSDMMC_WriteSingleBlock` = 24U,  
  `kSDMMC_WriteMultipleBlock` = 25U,  
  `kSDMMC_ProgramCsd` = 27U,  
  `kSDMMC_SetWriteProtect` = 28U,  
  `kSDMMC_ClearWriteProtect` = 29U,  
  `kSDMMC_SendWriteProtect` = 30U,  
  `kSDMMC_Erase` = 38U,  
  `kSDMMC_LockUnlock` = 42U,  
  `kSDMMC_ApplicationCommand` = 55U,  
  `kSDMMC_GeneralCommand` = 56U,  
  `kSDMMC_ReadOcr` = 58U }
- SD/MMC card common commands.*
- enum {

```

kSDIO_RegCCCRSdioVer = 0x00U,
kSDIO_RegSDVersion = 0x01U,
kSDIO_RegIOEnable = 0x02U,
kSDIO_RegIOReady = 0x03U,
kSDIO_RegIOIntEnable = 0x04U,
kSDIO_RegIOIntPending = 0x05U,
kSDIO_RegIOAbort = 0x06U,
kSDIO_RegBusInterface = 0x07U,
kSDIO_RegCardCapability = 0x08U,
kSDIO_RegCommonCISPointer = 0x09U,
kSDIO_RegBusSuspend = 0x0C,
kSDIO_RegFunctionSelect = 0x0DU,
kSDIO_RegExecutionFlag = 0x0EU,
kSDIO_RegReadyFlag = 0x0FU,
kSDIO_RegFN0BlockSizeLow = 0x10U,
kSDIO_RegFN0BlockSizeHigh = 0x11U,
kSDIO_RegPowerControl = 0x12U,
kSDIO_RegBusSpeed = 0x13U,
kSDIO_RegUHSITimingSupport = 0x14U,
kSDIO_RegDriverStrength = 0x15U,
kSDIO_RegInterruptExtension = 0x16U }

    sdio card cccr register addr
• enum sdio_command_t {
    kSDIO_SendRelativeAddress = 3U,
    kSDIO_SendOperationCondition = 5U,
    kSDIO_SendInterfaceCondition = 8U,
    kSDIO_RWIODirect = 52U,
    kSDIO_RWIOExtended = 53U }

    sdio card individual commands
• enum sdio_func_num_t {
    kSDIO_FunctionNum0,
    kSDIO_FunctionNum1,
    kSDIO_FunctionNum2,
    kSDIO_FunctionNum3,
    kSDIO_FunctionNum4,
    kSDIO_FunctionNum5,
    kSDIO_FunctionNum6,
    kSDIO_FunctionNum7,
    kSDIO_FunctionMemory }

    sdio card individual commands
• enum {

```

- ```

kSDIO_StatusCmdCRCError = 0x8000U,
kSDIO_StatusIllegalCmd = 0x4000U,
kSDIO_StatusR6Error = 0x2000U,
kSDIO_StatusError = 0x0800U,
kSDIO_StatusFunctionNumError = 0x0200U,
kSDIO_StatusOutOfRange = 0x0100U }
    
```

*sdio command response flag*
- enum {
 

```

kSDIO_OcrPowerUpBusyFlag = 31,
kSDIO_OcrIONumber = 28,
kSDIO_OcrMemPresent = 27,
kSDIO_OcrVdd20_21Flag = 8,
kSDIO_OcrVdd21_22Flag = 9,
kSDIO_OcrVdd22_23Flag = 10,
kSDIO_OcrVdd23_24Flag = 11,
kSDIO_OcrVdd24_25Flag = 12,
kSDIO_OcrVdd25_26Flag = 13,
kSDIO_OcrVdd26_27Flag = 14,
kSDIO_OcrVdd27_28Flag = 15,
kSDIO_OcrVdd28_29Flag = 16,
kSDIO_OcrVdd29_30Flag = 17,
kSDIO_OcrVdd30_31Flag = 18,
kSDIO_OcrVdd31_32Flag = 19,
kSDIO_OcrVdd32_33Flag = 20,
kSDIO_OcrVdd33_34Flag = 21,
kSDIO_OcrVdd34_35Flag = 22,
kSDIO_OcrVdd35_36Flag = 23 }
    
```

*sdio operation condition flag*
- enum {
 

```

kSDIO_CCCRSupportDirectCmdDuringDataTrans = (1UL << 0U),
kSDIO_CCCRSupportMultiBlock = (1UL << 1U),
kSDIO_CCCRSupportReadWait = (1UL << 2U),
kSDIO_CCCRSupportSuspendResume = (1UL << 3U),
kSDIO_CCCRSupportIntDuring4BitDataTrans = (1UL << 4U),
kSDIO_CCCRSupportLowSpeed1Bit = (1UL << 6U),
kSDIO_CCCRSupportLowSpeed4Bit = (1UL << 7U),
kSDIO_CCCRSupportMasterPowerControl = (1UL << 8U),
kSDIO_CCCRSupportHighSpeed = (1UL << 9U),
kSDIO_CCCRSupportContinuousSPIInt = (1UL << 10U) }
    
```

*sdio capability flag*
- enum {
 

```

kSDIO_FBRSupportCSA = (1U << 0U),
kSDIO_FBRSupportPowerSelection = (1U << 1U) }
    
```

*sdio fbr flag*
- enum **sdio\_bus\_width\_t** {

- ```

kSDIO_DataBus1Bit = 0x00U,
kSDIO_DataBus4Bit = 0X02U,
kSDIO_DataBus8Bit = 0X03U }
    
```

*sdio bus width*
- enum `mmc_command_t` {
 

```

kMMC_SendOperationCondition = 1U,
kMMC_SetRelativeAddress = 3U,
kMMC_SleepAwake = 5U,
kMMC_Switch = 6U,
kMMC_SendExtendedCsd = 8U,
kMMC_ReadDataUntilStop = 11U,
kMMC_BusTestRead = 14U,
kMMC_SendingBusTest = 19U,
kMMC_WriteDataUntilStop = 20U,
kMMC_SendTuningBlock = 21U,
kMMC_ProgramCid = 26U,
kMMC_EraseGroupStart = 35U,
kMMC_EraseGroupEnd = 36U,
kMMC_FastInputOutput = 39U,
kMMC_GoInterruptState = 40U }
    
```

*MMC card individual commands.*
- enum `mmc_classified_voltage_t` {
 

```

kMMC_ClassifiedVoltageHigh = 0U,
kMMC_ClassifiedVoltageDual = 1U }
    
```

*MMC card classified as voltage range.*
- enum `mmc_classified_density_t` { `kMMC_ClassifiedDensityWithin2GB` = 0U }
- enum `mmc_access_mode_t` {
 

```

kMMC_AccessModeByte = 0U,
kMMC_AccessModeSector = 2U }
    
```

*MMC card access mode(Access mode in OCR).*
- enum `mmc_voltage_window_t` {
 

```

kMMC_VoltageWindowNone = 0U,
kMMC_VoltageWindow120 = 0x01U,
kMMC_VoltageWindow170to195 = 0x02U,
kMMC_VoltageWindows270to360 = 0x1FFU }
    
```

*MMC card voltage window(VDD voltage window in OCR).*
- enum `mmc_csd_structure_version_t` {
 

```

kMMC_CsdStrucureVersion10 = 0U,
kMMC_CsdStrucureVersion11 = 1U,
kMMC_CsdStrucureVersion12 = 2U,
kMMC_CsdStrucureVersionInExtcsd = 3U }
    
```

*CSD structure version(CSD\_STRUCTURE in CSD).*
- enum `mmc_specification_version_t` {

```
kMMC_SpecificationVersion0 = 0U,
kMMC_SpecificationVersion1 = 1U,
kMMC_SpecificationVersion2 = 2U,
kMMC_SpecificationVersion3 = 3U,
kMMC_SpecificationVersion4 = 4U }
```

*MMC card specification version(SPEC\_VERS in CSD).*

- enum {
   
kMMC\_ExtendedCsdRevision10 = 0U,
 kMMC\_ExtendedCsdRevision11 = 1U,
 kMMC\_ExtendedCsdRevision12 = 2U,
 kMMC\_ExtendedCsdRevision13 = 3U,
 kMMC\_ExtendedCsdRevision14 = 4U,
 kMMC\_ExtendedCsdRevision15 = 5U,
 kMMC\_ExtendedCsdRevision16 = 6U,
 kMMC\_ExtendedCsdRevision17 = 7U }

*MMC card Extended CSD fix version(EXT\_CSD\_REV in Extended CSD)*

- enum **mmc\_command\_set\_t** {
   
kMMC\_CommandSetStandard = 0U,
 kMMC\_CommandSet1 = 1U,
 kMMC\_CommandSet2 = 2U,
 kMMC\_CommandSet3 = 3U,
 kMMC\_CommandSet4 = 4U }

*MMC card command set(COMMAND\_SET in Extended CSD)*

- enum {
   
kMMC\_SupportAlternateBoot = 1U,
 kMMC\_SupportDDRBoot = 2U,
 kMMC\_SupportHighSpeedBoot = 4U }

*boot support(BOOT\_INFO in Extended CSD)*

- enum **mmc\_high\_speed\_timing\_t** {
   
kMMC\_HighSpeedTimingNone = 0U,
 kMMC\_HighSpeedTiming = 1U,
 kMMC\_HighSpeed200Timing = 2U,
 kMMC\_HighSpeed400Timing = 3U,
 kMMC\_EnhanceHighSpeed400Timing = 4U }

*MMC card high-speed timing(HS\_TIMING in Extended CSD)*

- enum **mmc\_data\_bus\_width\_t** {
   
kMMC\_DataBusWidth1bit = 0U,
 kMMC\_DataBusWidth4bit = 1U,
 kMMC\_DataBusWidth8bit = 2U,
 kMMC\_DataBusWidth4bitDDR = 5U,
 kMMC\_DataBusWidth8bitDDR = 6U,
 kMMC\_DataBusWidth8bitDDRSTROBE = 0x86U }

*MMC card data bus width(BUS\_WIDTH in Extended CSD)*

- enum **mmc\_boot\_partition\_enable\_t** {

```
kMMC_BootPartitionEnableNot = 0U,
kMMC_BootPartitionEnablePartition1 = 1U,
kMMC_BootPartitionEnablePartition2 = 2U,
kMMC_BootPartitionEnableUserAera = 7U }
```

*MMC card boot partition enabled(BOOT\_PARTITION\_ENABLE in Extended CSD)*

- enum `mmc_boot_timing_mode_t` {
   
kMMC\_BootModeSDRWithDefaultTiming = 0U,
   
kMMC\_BootModeSDRWithHighSpeedTiming = 1U,
   
kMMC\_BootModeDDRTiming = 2U }

*boot mode configuration Note: HS200 & HS400 is not support during BOOT operation.*

- enum `mmc_boot_partition_wp_t` {
   
kMMC\_BootPartitionWPDisable = 0x50U,
   
kMMC\_BootPartitionPwrWPToBothPartition,
   
kMMC\_BootPartitionPermWPToBothPartition = 0x04U,
   
kMMC\_BootPartitionPwrWPToPartition1 = (1U << 7U) | 1U,
   
kMMC\_BootPartitionPwrWPToPartition2 = (1U << 7U) | 3U,
   
kMMC\_BootPartitionPermWPToPartition1,
   
kMMC\_BootPartitionPermWPToPartition2,
   
kMMC\_BootPartitionPermWPToPartition1PwrWPToPartition2,
   
kMMC\_BootPartitionPermWPToPartition2PwrWPToPartition1 }

*MMC card boot partition write protect configurations All the bits in BOOT\_WP register, except the two R/W bits B\_PERM\_WP\_DIS and B\_PERM\_WP\_EN, shall only be written once per power cycle. The protection mode intended for both boot areas will be set with a single write.*

- enum {
   
kMMC\_BootPartitionNotProtected = 0U,
   
kMMC\_BootPartitionPwrProtected = 1U,
   
kMMC\_BootPartitionPermProtected = 2U }

*MMC card boot partition write protect status.*

- enum `mmc_access_partition_t` {
   
kMMC\_AccessPartitionUserAera = 0U,
   
kMMC\_AccessPartitionBoot1 = 1U,
   
kMMC\_AccessPartitionBoot2 = 2U,
   
kMMC\_AccessRPMB = 3U,
   
kMMC\_AccessGeneralPurposePartition1 = 4U,
   
kMMC\_AccessGeneralPurposePartition2 = 5U,
   
kMMC\_AccessGeneralPurposePartition3 = 6U,
   
kMMC\_AccessGeneralPurposePartition4 = 7U }

*MMC card partition to be accessed(BOOT\_PARTITION\_ACCESS in Extended CSD)*

- enum {

```

kMMC_CsdReadBlockPartialFlag = (1U << 0U),
kMMC_CsdWriteBlockMisalignFlag = (1U << 1U),
kMMC_CsdReadBlockMisalignFlag = (1U << 2U),
kMMC_CsdDsrImplementedFlag = (1U << 3U),
kMMC_CsdWriteProtectGroupEnabledFlag = (1U << 4U),
kMMC_CsdWriteBlockPartialFlag = (1U << 5U),
kMMC_ContentProtectApplicationFlag = (1U << 6U),
kMMC_CsdFileFormatGroupFlag = (1U << 7U),
kMMC_CsdCopyFlag = (1U << 8U),
kMMC_CsdPermanentWriteProtectFlag = (1U << 9U),
kMMC_CsdTemporaryWriteProtectFlag = (1U << 10U) }

```

*MMC card CSD register flags.*

- enum `mmc_extended_csd_access_mode_t` {
   
kMMC\_ExtendedCsdAccessModeCommandSet = 0U,
   
kMMC\_ExtendedCsdAccessModeSetBits = 1U,
   
kMMC\_ExtendedCsdAccessModeClearBits = 2U,
   
kMMC\_ExtendedCsdAccessModeWriteBits = 3U }

*Extended CSD register access mode(Access mode in CMD6).*

- enum `mmc_extended_csd_index_t` {
   
kMMC\_ExtendedCsdIndexFlushCache = 32U,
   
kMMC\_ExtendedCsdIndexCacheControl = 33U,
   
kMMC\_ExtendedCsdIndexBootPartitionWP = 173U,
   
kMMC\_ExtendedCsdIndexEraseGroupDefinition = 175U,
   
kMMC\_ExtendedCsdIndexBootBusConditions = 177U,
   
kMMC\_ExtendedCsdIndexBootConfigWP = 178U,
   
kMMC\_ExtendedCsdIndexPartitionConfig = 179U,
   
kMMC\_ExtendedCsdIndexBusWidth = 183U,
   
kMMC\_ExtendedCsdIndexHighSpeedTiming = 185U,
   
kMMC\_ExtendedCsdIndexPowerClass = 187U,
   
kMMC\_ExtendedCsdIndexCommandSet = 191U }

*EXT CSD byte index.*

- enum {
   
kMMC\_DriverStrength0 = 0U,
   
kMMC\_DriverStrength1 = 1U,
   
kMMC\_DriverStrength2 = 2U,
   
kMMC\_DriverStrength3 = 3U,
   
kMMC\_DriverStrength4 = 4U }
- mmc driver strength*
- enum `mmc_extended_csd_flags_t` {
   
kMMC\_ExtCsdExtPartitionSupport = (1 << 0U),
   
kMMC\_ExtCsdEnhancePartitionSupport = (1 << 1U),
   
kMMC\_ExtCsdPartitioningSupport = (1 << 2U),
   
kMMC\_ExtCsdPrgCIDCSDInDDRModeSupport = (1 << 3U),
   
kMMC\_ExtCsdBKOpsSupport = (1 << 4U),
   
kMMC\_ExtCsdDataTagSupport = (1 << 5U),
   
kMMC\_ExtCsdModeOperationCodeSupport = (1 << 6U) }

- enum `mmc_boot_mode_t` {
   
    `kMMC_BootModeNormal` = 0U,
   
    `kMMC_BootModeAlternative` = 1U }
   
    *MMC card boot mode.*

## common function

tuning pattern

- `status_t SDMMC_SelectCard (sdmmchost_t *host, uint32_t relativeAddress, bool isSelected)`
  
    *Selects the card to put it into transfer state.*
- `status_t SDMMC_SendApplicationCommand (sdmmchost_t *host, uint32_t relativeAddress)`
  
    *Sends an application command.*
- `status_t SDMMC_SetBlockCount (sdmmchost_t *host, uint32_t blockCount)`
  
    *Sets the block count.*
- `status_t SDMMC_GoIdle (sdmmchost_t *host)`
  
    *Sets the card to be idle state.*
- `status_t SDMMC_SetBlockSize (sdmmchost_t *host, uint32_t blockSize)`
  
    *Sets data block size.*
- `status_t SDMMC_SetCardInactive (sdmmchost_t *host)`
  
    *Sets card to inactive status.*

### 54.7.2 Data Structure Documentation

#### 54.7.2.1 struct sd\_detect\_card\_t

##### Data Fields

- `sd_detect_card_type_t type`
  
    *card detect type*
- `uint32_t cdDebounce_ms`
  
    *card detect debounce delay ms*
- `sd_cd_t callback`
  
    *card inserted callback which is meaningful for interrupt case*
- `sd_cd_status_t cardDetected`
  
    *used to check sd cd status when card detect through GPIO*
- `sd_dat3_pull_t dat3PullFunc`
  
    *function pointer of DATA3 pull up/down*
- `void * userData`
  
    *user data*

#### 54.7.2.2 struct sd\_io\_voltage\_t

##### Data Fields

- `sd_io_voltage_ctrl_type_t type`

- **sd\_io\_voltage\_func\_t func**  
*io voltage switch function*

#### 54.7.2.3 struct sd\_usr\_param\_t

##### Data Fields

- **sd\_pwr\_t pwr**  
*power control configuration pointer*
- **uint32\_t powerOnDelayMS**  
*power on delay time*
- **uint32\_t powerOffDelayMS**  
*power off delay time*
- **sd\_io\_strength\_t ioStrength**  
*switch sd io strength*
- **sd\_io\_voltage\_t \* ioVoltage**  
*switch io voltage*
- **sd\_detect\_card\_t \* cd**  
*card detect*
- **uint32\_t maxFreq**  
*board support maximum frequency*
- **uint32\_t capability**  
*board capability flag*

#### 54.7.2.4 struct sdio\_card\_int\_t

##### Data Fields

- **void \* userData**  
*user data*
- **sdio\_int\_t cardInterrupt**  
*card int call back*

#### 54.7.2.5 struct sdio\_usr\_param\_t

##### Data Fields

- **sd\_pwr\_t pwr**  
*power control configuration pointer*
- **uint32\_t powerOnDelayMS**  
*power on delay time*
- **uint32\_t powerOffDelayMS**  
*power off delay time*
- **sd\_io\_strength\_t ioStrength**  
*switch sd io strength*
- **sd\_io\_voltage\_t \* ioVoltage**  
*switch io voltage*

- `sd_detect_card_t * cd`  
*card detect*
- `sdio_card_int_t * sdioInt`  
*card int*
- `uint32_t maxFreq`  
*board support maximum frequency*
- `uint32_t capability`  
*board capability flag*

#### 54.7.2.6 struct `sdio_fbr_t`

##### Data Fields

- `uint8_t flags`  
*current io flags*
- `uint8_t ioStdFunctionCode`  
*current io standard function code*
- `uint8_t ioExtFunctionCode`  
*current io extended function code*
- `uint32_t ioPointerToCIS`  
*current io pointer to CIS*
- `uint32_t ioPointerToCSA`  
*current io pointer to CSA*
- `uint16_t ioBlockSize`  
*current io block size*

#### 54.7.2.7 struct `sdio_common_cis_t`

##### Data Fields

- `uint16_t mID`  
*manufacturer code*
- `uint16_t mInfo`  
*manufacturer information*
- `uint8_t funcID`  
*function ID*
- `uint16_t fn0MaxBlkSize`  
*function 0 max block size*
- `uint8_t maxTransSpeed`  
*max data transfer speed for all function*

#### 54.7.2.8 struct `sdio_func_cis_t`

##### Data Fields

- `uint8_t funcID`  
*function ID*
- `uint8_t funcInfo`

- *function info*
- **uint8\_t ioVersion**  
*level of application specification this io support*
- **uint32\_t cardPSN**  
*product serial number*
- **uint32\_t ioCSASize**  
*available CSA size for io*
- **uint8\_t ioCSAProperty**  
*CSA property.*
- **uint16\_t ioMaxBlockSize**  
*io max transfer data size*
- **uint32\_t ioOCR**  
*io ioeration condition*
- **uint8\_t ioOPMinPwr**  
*min current in operation mode*
- **uint8\_t ioOPAvgPwr**  
*average current in operation mode*
- **uint8\_t ioOPMaxPwr**  
*max current in operation mode*
- **uint8\_t ioSBMinPwr**  
*min current in standby mode*
- **uint8\_t ioSBAvgPwr**  
*average current in standby mode*
- **uint8\_t ioSBMaxPwr**  
*max current in standby mode*
- **uint16\_t ioMinBandWidth**  
*io min transfer bandwidth*
- **uint16\_t ioOptimumBandWidth**  
*io optimum transfer bandwidth*
- **uint16\_t ioReadyTimeout**  
*timeout value from enalbe to ready*
- **uint16\_t ioHighCurrentAvgCurrent**  
*the average peak current (mA)  
when IO operating in high current mode*
- **uint16\_t ioHighCurrentMaxCurrent**  
*the max peak current (mA)  
when IO operating in high current mode*
- **uint16\_t ioLowCurrentAvgCurrent**  
*the average peak current (mA)  
when IO operating in lower current mode*
- **uint16\_t ioLowCurrentMaxCurrent**  
*the max peak current (mA)  
when IO operating in lower current mode*

#### 54.7.2.9 struct sd\_status\_t

##### Data Fields

- **uint8\_t busWidth**  
*current buswidth*

- `uint8_t secureMode`  
*secured mode*
- `uint16_t cardType`  
*sdcard type*
- `uint32_t protectedSize`  
*size of protected area*
- `uint8_t speedClass`  
*speed class of card*
- `uint8_t performanceMove`  
*Performance of move indicated by 1[MB/S]step.*
- `uint8_t auSize`  
*size of AU*
- `uint16_t eraseSize`  
*number of AUs to be erased at a time*
- `uint8_t eraseTimeout`  
*timeout value for erasing areas specified by UNIT OF ERASE AU*
- `uint8_t eraseOffset`  
*fixed offset value added to erase time*
- `uint8_t uhsSpeedGrade`  
*speed grade for UHS mode*
- `uint8_t uhsAuSize`  
*size of AU for UHS mode*

#### 54.7.2.10 struct sd\_cid\_t

##### Data Fields

- `uint8_t manufacturerID`  
*Manufacturer ID [127:120].*
- `uint16_t applicationID`  
*OEM/Application ID [119:104].*
- `uint8_t productName [SD_PRODUCT_NAME_BYTES]`  
*Product name [103:64].*
- `uint8_t productVersion`  
*Product revision [63:56].*
- `uint32_t productSerialNumber`  
*Product serial number [55:24].*
- `uint16_t manufacturerData`  
*Manufacturing date [19:8].*

#### 54.7.2.11 struct sd\_csd\_t

##### Data Fields

- `uint8_t csdStructure`  
*CSD structure [127:126].*
- `uint8_t dataReadAccessTime1`  
*Data read access-time-1 [119:112].*
- `uint8_t dataReadAccessTime2`

- **uint8\_t transferSpeed**  
*Maximum data transfer rate [103:96].*
- **uint16\_t cardCommandClass**  
*Card command classes [95:84].*
- **uint8\_t readBlockLength**  
*Maximum read data block length [83:80].*
- **uint16\_t flags**  
*Flags in \_sd\_csd\_flag.*
- **uint32\_t deviceSize**  
*Device size [73:62].*
- **uint8\_t readCurrentVddMin**  
*Maximum read current at VDD min [61:59].*
- **uint8\_t readCurrentVddMax**  
*Maximum read current at VDD max [58:56].*
- **uint8\_t writeCurrentVddMin**  
*Maximum write current at VDD min [55:53].*
- **uint8\_t writeCurrentVddMax**  
*Maximum write current at VDD max [52:50].*
- **uint8\_t deviceSizeMultiplier**  
*Device size multiplier [49:47].*
- **uint8\_t eraseSectorSize**  
*Erase sector size [45:39].*
- **uint8\_t writeProtectGroupSize**  
*Write protect group size [38:32].*
- **uint8\_t writeSpeedFactor**  
*Write speed factor [28:26].*
- **uint8\_t writeBlockLength**  
*Maximum write data block length [25:22].*
- **uint8\_t fileFormat**  
*File format [11:10].*

#### 54.7.2.12 struct sd\_scr\_t

##### Data Fields

- **uint8\_t scrStructure**  
*SCR Structure [63:60].*
- **uint8\_t sdSpecification**  
*SD memory card specification version [59:56].*
- **uint16\_t flags**  
*SCR flags in \_sd\_scr\_flag.*
- **uint8\_t sdSecurity**  
*Security specification supported [54:52].*
- **uint8\_t sdBusWidths**  
*Data bus widths supported [51:48].*
- **uint8\_t extendedSecurity**  
*Extended security support [46:43].*
- **uint8\_t commandSupport**  
*Command support bits [33:32] 33-support CMD23, 32-support cmd20.*

- `uint32_t reservedForManufacturer`  
*reserved for manufacturer usage [31:0]*

#### 54.7.2.13 struct mmc\_cid\_t

##### Data Fields

- `uint8_t manufacturerID`  
*Manufacturer ID.*
- `uint16_t applicationID`  
*OEM/Application ID.*
- `uint8_t productName [MMC_PRODUCT_NAME_BYTES]`  
*Product name.*
- `uint8_t productVersion`  
*Product revision.*
- `uint32_t productSerialNumber`  
*Product serial number.*
- `uint8_t manufacturerData`  
*Manufacturing date.*

#### 54.7.2.14 struct mmc\_csd\_t

##### Data Fields

- `uint8_t csdStructureVersion`  
*CSD structure [127:126].*
- `uint8_t systemSpecificationVersion`  
*System specification version [125:122].*
- `uint8_t dataReadAccessTime1`  
*Data read access-time 1 [119:112].*
- `uint8_t dataReadAccessTime2`  
*Data read access-time 2 in CLOCK cycles (NSAC\*100) [111:104].*
- `uint8_t transferSpeed`  
*Max.*
- `uint16_t cardCommandClass`  
*card command classes [95:84]*
- `uint8_t readBlockLength`  
*Max.*
- `uint16_t flags`  
*Contain flags in \_mmc\_csd\_flag.*
- `uint16_t deviceSize`  
*Device size [73:62].*
- `uint8_t readCurrentVddMin`  
*Max.*
- `uint8_t readCurrentVddMax`  
*Max.*
- `uint8_t writeCurrentVddMin`  
*Max.*
- `uint8_t writeCurrentVddMax`

- `uint8_t deviceSizeMultiplier`  
*Device size multiplier [49:47].*
- `uint8_t eraseGroupSize`  
*Erase group size [46:42].*
- `uint8_t eraseGroupSizeMultiplier`  
*Erase group size multiplier [41:37].*
- `uint8_t writeProtectGroupSize`  
*Write protect group size [36:32].*
- `uint8_t defaultEcc`  
*Manufacturer default ECC [30:29].*
- `uint8_t writeSpeedFactor`  
*Write speed factor [28:26].*
- `uint8_t maxWriteBlockLength`  
*Max.*
- `uint8_t fileFormat`  
*File format [11:10].*
- `uint8_t eccCode`  
*ECC code [9:8].*

## Field Documentation

(1) `uint8_t mmc_csd_t::transferSpeed`

bus clock frequency [103:96]

(2) `uint8_t mmc_csd_t::readBlockLength`

read data block length [83:80]

(3) `uint8_t mmc_csd_t::readCurrentVddMin`

read current @ VDD min [61:59]

(4) `uint8_t mmc_csd_t::readCurrentVddMax`

read current @ VDD max [58:56]

(5) `uint8_t mmc_csd_t::writeCurrentVddMin`

write current @ VDD min [55:53]

(6) `uint8_t mmc_csd_t::writeCurrentVddMax`

write current @ VDD max [52:50]

(7) `uint8_t mmc_csd_t::maxWriteBlockLength`

write data block length [25:22]

### 54.7.2.15 struct mmc\_extended\_csd\_t

#### Data Fields

- `uint8_t cacheCtrl`  
 $<$  secure removal type[16]
- `uint8_t partitionAttribute`  
 $<$  power off notification[34]
- `uint8_t userWP`  
 $<$  max enhance area size [159-157]
- `uint8_t bootPartitionWP`  
boot write protect register[173]
- `uint8_t bootWPStatus`  
boot write protect status register[174]
- `uint8_t highDensityEraseGroupDefinition`  
High-density erase group definition [175].
- `uint8_t bootDataBusConditions`  
Boot bus conditions [177].
- `uint8_t bootConfigProtect`  
Boot config protection [178].
- `uint8_t partitionConfig`  
Boot configuration [179].
- `uint8_t eraseMemoryContent`  
Erased memory content [181].
- `uint8_t dataBusWidth`  
Data bus width mode [183].
- `uint8_t highSpeedTiming`  
High-speed interface timing [185].
- `uint8_t powerClass`  
Power class [187].
- `uint8_t commandSetRevision`  
Command set revision [189].
- `uint8_t commandSet`  
Command set [191].
- `uint8_t extendecCsdVersion`  
Extended CSD revision [192].
- `uint8_t csdStructureVersion`  
CSD structure version [194].
- `uint8_t cardType`  
Card Type [196].
- `uint8_t ioDriverStrength`  
IO driver strength [197].
- `uint8_t partitionSwitchTimeout`  
 $<$  out of interrupt busy timing [198]
- `uint8_t powerClass52MHz195V`  
Power Class for 52MHz @ 1.95V [200].
- `uint8_t powerClass26MHz195V`  
Power Class for 26MHz @ 1.95V [201].
- `uint8_t powerClass52MHz360V`  
Power Class for 52MHz @ 3.6V [202].
- `uint8_t powerClass26MHz360V`

- **Power Class for 26MHz @ 3.6V [203].**
- **uint8\_t minimumReadPerformance4Bit26MHz**  
*Minimum Read Performance for 4bit at 26MHz [205].*
- **uint8\_t minimumWritePerformance4Bit26MHz**  
*Minimum Write Performance for 4bit at 26MHz [206].*
- **uint8\_t minimumReadPerformance8Bit26MHz4Bit52MHz**  
*Minimum read Performance for 8bit at 26MHz/4bit @ 52MHz [207].*
- **uint8\_t minimumWritePerformance8Bit26MHz4Bit52MHz**  
*Minimum Write Performance for 8bit at 26MHz/4bit @ 52MHz [208].*
- **uint8\_t minimumReadPerformance8Bit52MHz**  
*Minimum Read Performance for 8bit at 52MHz [209].*
- **uint8\_t minimumWritePerformance8Bit52MHz**  
*Minimum Write Performance for 8bit at 52MHz [210].*
- **uint32\_t sectorCount**  
*Sector Count [215:212].*
- **uint8\_t sleepAwakeTimeout**  
*< sleep notification timeout [216]*
- **uint8\_t sleepCurrentVCCQ**  
*< Production state awareness timeout [218]*
- **uint8\_t sleepCurrentVCC**  
*Sleep current (VCC) [220].*
- **uint8\_t highCapacityWriteProtectGroupSize**  
*High-capacity write protect group size [221].*
- **uint8\_t reliableWriteSectorCount**  
*Reliable write sector count [222].*
- **uint8\_t highCapacityEraseTimeout**  
*High-capacity erase timeout [223].*
- **uint8\_t highCapacityEraseUnitSize**  
*High-capacity erase unit size [224].*
- **uint8\_t accessSize**  
*Access size [225].*
- **uint8\_t minReadPerformance8bitAt52MHZDDR**  
*< secure trim multiplier[229]*
- **uint8\_t minWritePerformance8bitAt52MHZDDR**  
*Minimum write performance for 8bit at DDR 52MHZ[235].*
- **uint8\_t powerClass200MHZVCCQ130VVCC360V**  
*power class for 200MHZ, at VCCQ= 1.3V,VCC=3.6V[236]*
- **uint8\_t powerClass200MHZVCCQ195VVCC360V**  
*power class for 200MHZ, at VCCQ= 1.95V,VCC=3.6V[237]*
- **uint8\_t powerClass52MHZDDR195V**  
*power class for 52MHZ,DDR at Vcc 1.95V[238]*
- **uint8\_t powerClass52MHZDDR360V**  
*power class for 52MHZ,DDR at Vcc 3.6V[239]*
- **uint32\_t genericCMD6Timeout**  
*< 1st initialization time after partitioning[241]*
- **uint32\_t cacheSize**  
*cache size[252-249]*
- **uint8\_t powerClass200MHZDDR360V**  
*power class for 200MHZ, DDR at VCC=2.6V[253]*
- **uint8\_t extPartitionSupport**  
*< fw VERSION [261-254]*

- `uint8_t supportedCommandSet`  
*< large unit size[495]*

### Field Documentation

#### (1) `uint8_t mmc_extended_csd_t::cacheCtrl`

*< product state awareness enablement[17]  
< max preload data size[21-18]  
< pre-load data size[25-22]  
< FFU status [26]  
< mode operation code[29]  
< mode config [30] control to turn on/off cache[33]*

#### (2) `uint8_t mmc_extended_csd_t::partitionAttribute`

*< packed cmd fail index [35]  
< packed cmd status[36]  
< context configuration[51-37]  
< extended partitions attribut[53-52]  
< exception events status[55-54]  
< exception events control[57-56]  
< number of group to be released[58]  
< class 6 command control[59]  
< 1st initialization after disabling sector size emu[60]  
< sector size[61]  
< sector size emulation[62]  
< native sector size[63]  
< period wakeup [131]  
< package case temperature is controlled[132]  
< production state awareness[133]  
< enhanced user data start addr [139-136]  
< enhanced user data area size[142-140]  
< general purpose partition size[154-143] partition attribute [156]*

#### (3) `uint8_t mmc_extended_csd_t::userWP`

*< HPI management [161]*

< write reliability parameter register[166]  
< write reliability setting register[167]  
< RPMB size multi [168]  
< FW configuration[169] user write protect register[171]

**(4) uint8\_t mmc\_extended\_csd\_t::partitionSwitchTimeout**

partition switch timing [199]

**(5) uint8\_t mmc\_extended\_csd\_t::sleepAwakeTimeout**

Sleep/awake timeout [217]

**(6) uint8\_t mmc\_extended\_csd\_t::sleepCurrentVCCQ**

Sleep current (VCCQ) [219]

**(7) uint8\_t mmc\_extended\_csd\_t::minReadPerformance8bitAt52MHZDDR**

< secure erase multiplier[230]  
< secure feature support[231]  
< trim multiplier[232] Minimum read performance for 8bit at DDR 52MHZ[234]

**(8) uint32\_t mmc\_extended\_csd\_t::genericCMD6Timeout**

< correct prg sectors number[245-242]  
< background operations status[246]  
< power off notification timeout[247] generic CMD6 timeout[248]

**(9) uint8\_t mmc\_extended\_csd\_t::extPartitionSupport**

< device version[263-262]  
< optimal trim size[264]  
< optimal write size[265]  
< optimal read size[266]  
< pre EOL information[267]  
< device life time estimation typeA[268]  
< device life time estimation typeB[269]  
< number of FW sectors correctly programmed[305-302]  
< FFU argument[490-487]  
< operation code timeout[491]

< support mode [493] extended partition attribute support[494]

**(10) uint8\_t mmc\_extended\_csd\_t::supportedCommandSet**

< context management capability[496]

< tag resource size[497]

< tag unit size[498]

< max packed write cmd[500]

< max packed read cmd[501]

< HPI feature[503] Supported Command Sets [504]

#### 54.7.2.16 struct mmc\_extended\_csd\_config\_t

##### Data Fields

- **mmc\_command\_set\_t commandSet**  
*Command set.*
- **uint8\_t ByteValue**  
*The value to set.*
- **uint8\_t ByteIndex**  
*The byte index in Extended CSD(mmc\_extended\_csd\_index\_t)*
- **mmc\_extended\_csd\_access\_mode\_t accessMode**  
*Access mode.*

#### 54.7.2.17 struct mmc\_boot\_config\_t

##### Data Fields

- **mmc\_boot\_mode\_t bootMode**  
*mmc boot mode*
- **bool enableBootAck**  
*Enable boot ACK.*
- **mmc\_boot\_partition\_enable\_t bootPartition**  
*Boot partition.*
- **mmc\_boot\_timing\_mode\_t bootTimingMode**  
*boot mode*
- **mmc\_data\_bus\_width\_t bootDataBusWidth**  
*Boot data bus width.*
- **bool retainBootbusCondition**  
*If retain boot bus width and boot mode conditions.*
- **bool pwrBootConfigProtection**  
*Disable the change of boot configuration register bits from at this point until next power cycle or next H/W reset operation*
- **bool premBootConfigProtection**  
*Disable the change of boot configuration register bits permanently.*
- **mmc\_boot\_partition\_wp\_t bootPartitionWP**

*boot partition write protect configurations*

### 54.7.3 Macro Definition Documentation

54.7.3.1 `#define SDMMC_LOG( format, ... )`

54.7.3.2 `#define READ_MMC_TRANSFER_SPEED_FREQUENCY_UNIT( CSD ) (((CSD).transferSpeed) & MMC_TRANSFER_SPEED_FREQUENCY_UNIT_MASK) >> MMC_TRANSFER_SPEED_FREQUENCY_UNIT_SHIFT)`

54.7.3.3 `#define READ_MMC_TRANSFER_SPEED_MULTIPLIER( CSD ) (((CSD).transferSpeed) & MMC_TRANSFER_SPEED_MULTIPLIER_MASK) >> MMC_TRANSFER_SPEED_MULTIPLIER_SHIFT)`

54.7.3.4 `#define MMC_EXTENDED_CSD_BYTES (512U)`

54.7.3.5 `#define SD_PRODUCT_NAME_BYTES (5U)`

54.7.3.6 `#define MMC_PRODUCT_NAME_BYTES (6U)`

54.7.3.7 `#define MMC_SWITCH_COMMAND_SET_SHIFT (0U)`

54.7.3.8 `#define MMC_SWITCH_COMMAND_SET_MASK (0x00000007U)`

### 54.7.4 Enumeration Type Documentation

54.7.4.1 anonymous enum

Enumerator

`kStatus_SDMMC_NotSupportYet` Haven't supported.

`kStatus_SDMMC_TransferFailed` Send command failed.

`kStatus_SDMMC_SetCardBlockSizeFailed` Set block size failed.

`kStatus_SDMMC_HostNotSupport` Host doesn't support.

`kStatus_SDMMC_CardNotSupport` Card doesn't support.

`kStatus_SDMMC_AllSendCidFailed` Send CID failed.

`kStatus_SDMMC_SendRelativeAddressFailed` Send relative address failed.

`kStatus_SDMMC_SendCsdFailed` Send CSD failed.

`kStatus_SDMMC_SelectCardFailed` Select card failed.

`kStatus_SDMMC_SendScrFailed` Send SCR failed.

`kStatus_SDMMC_SetDataBusWidthFailed` Set bus width failed.

`kStatus_SDMMC_GoIdleFailed` Go idle failed.

`kStatus_SDMMC_HandShakeOperationConditionFailed` Send Operation Condition failed.

`kStatus_SDMMC_SendApplicationCommandFailed` Send application command failed.

*kStatus\_SDMMC\_SwitchFailed* Switch command failed.  
*kStatus\_SDMMC\_StopTransmissionFailed* Stop transmission failed.  
*kStatus\_SDMMC\_WaitWriteCompleteFailed* Wait write complete failed.  
*kStatus\_SDMMC\_SetBlockCountFailed* Set block count failed.  
*kStatus\_SDMMC\_SetRelativeAddressFailed* Set relative address failed.  
*kStatus\_SDMMC\_SwitchBusTimingFailed* Switch high speed failed.  
*kStatus\_SDMMC\_SendExtendedCsdFailed* Send EXT\_CSD failed.  
*kStatus\_SDMMC\_ConfigureBootFailed* Configure boot failed.  
*kStatus\_SDMMC\_ConfigureExtendedCsdFailed* Configure EXT\_CSD failed.  
*kStatus\_SDMMC\_EnableHighCapacityEraseFailed* Enable high capacity erase failed.  
*kStatus\_SDMMC\_SendTestPatternFailed* Send test pattern failed.  
*kStatus\_SDMMC\_ReceiveTestPatternFailed* Receive test pattern failed.  
*kStatus\_SDMMC\_SDIO\_ResponseError* sdio response error  
*kStatus\_SDMMC\_SDIO\_InvalidArgument* sdio invalid argument response error  
*kStatus\_SDMMC\_SDIO\_SendOperationConditionFail* sdio send operation condition fail  
*kStatus\_SDMMC\_InvalidVoltage* invalid voltage  
*kStatus\_SDMMC\_SDIO\_SwitchHighSpeedFail* switch to high speed fail  
*kStatus\_SDMMC\_SDIO\_ReadCISFail* read CIS fail  
*kStatus\_SDMMC\_SDIO\_InvalidCard* invalid SDIO card  
*kStatus\_SDMMC\_TuningFail* tuning fail  
*kStatus\_SDMMC\_SwitchVoltageFail* switch voltage fail  
*kStatus\_SDMMC\_SwitchVoltage18VFail33VSuccess* switch voltage fail  
*kStatus\_SDMMC\_ReTuningRequest* retuning request  
*kStatus\_SDMMC\_SetDriverStrengthFail* set driver strength fail  
*kStatus\_SDMMC\_SetPowerClassFail* set power class fail  
*kStatus\_SDMMC\_HostNotReady* host controller not ready  
*kStatus\_SDMMC\_CardDetectFailed* card detect failed  
*kStatus\_SDMMC\_AuSizeNotSetProperly* AU size not set properly.  
*kStatus\_SDMMC\_PollingCardIdleFailed* polling card idle status failed  
*kStatus\_SDMMC\_DeselectCardFailed* deselect card failed  
*kStatus\_SDMMC\_CardStatusIdle* card idle  
*kStatus\_SDMMC\_CardStatusBusy* card busy  
*kStatus\_SDMMC\_CardInitFailed* card init failed

#### 54.7.4.2 anonymous enum

Enumerator

|                               |           |
|-------------------------------|-----------|
| <i>kSDMMC_SignalLineCmd</i>   | cmd line  |
| <i>kSDMMC_SignalLineData0</i> | data line |
| <i>kSDMMC_SignalLineData1</i> | data line |
| <i>kSDMMC_SignalLineData2</i> | data line |
| <i>kSDMMC_SignalLineData3</i> | data line |
| <i>kSDMMC_SignalLineData4</i> | data line |
| <i>kSDMMC_SignalLineData5</i> | data line |

*kSDMMC\_SignalLineData6* data line  
*kSDMMC\_SignalLineData7* data line

#### 54.7.4.3 enum sdmmc\_operation\_voltage\_t

Enumerator

*kSDMMC\_OperationVoltageNone* indicate current voltage setting is not setting by suser  
*kSDMMC\_OperationVoltage330V* card operation voltage around 3.3v  
*kSDMMC\_OperationVoltage300V* card operation voltage around 3.0v  
*kSDMMC\_OperationVoltage180V* card operation voltage around 1.8v

#### 54.7.4.4 anonymous enum

Enumerator

*kSDMMC\_BusWidth1Bit* card bus 1 width  
*kSDMMC\_BusWidth4Bit* card bus 4 width  
*kSDMMC\_BusWidth8Bit* card bus 8 width

#### 54.7.4.5 anonymous enum

Enumerator

*kSDMMC\_Support8BitWidth* 8 bit data width capability

#### 54.7.4.6 anonymous enum

Enumerator

*kSDMMC\_DataPacketFormatLSBFirst* usual data packet format LSB first, MSB last  
*kSDMMC\_DataPacketFormatMSBFirst* Wide width data packet format MSB first, LSB last.

#### 54.7.4.7 enum sd\_detect\_card\_type\_t

Enumerator

*kSD\_DetectCardByGpioCD* sd card detect by CD pin through GPIO  
*kSD\_DetectCardByHostCD* sd card detect by CD pin through host  
*kSD\_DetectCardByHostDATA3* sd card detect by DAT3 pin through host

#### 54.7.4.8 anonymous enum

Enumerator

*kSD\_Inserted* card is inserted

*kSD\_Removed* card is removed

#### 54.7.4.9 anonymous enum

Enumerator

*kSD\_DAT3PullDown* data3 pull down

*kSD\_DAT3PullUp* data3 pull up

#### 54.7.4.10 enum sd\_io\_voltage\_ctrl\_type\_t

Enumerator

*kSD\_IOVoltageCtrlNotSupport* io voltage control not support

*kSD\_IOVoltageCtrlByGpio* io voltage control by gpio

#### 54.7.4.11 anonymous enum

Enumerator

*kSDMMC\_R1OutOfRangeFlag* Out of range status bit.

*kSDMMC\_R1AddressErrorFlag* Address error status bit.

*kSDMMC\_R1BlockLengthErrorFlag* Block length error status bit.

*kSDMMC\_R1EraseSequenceErrorFlag* Erase sequence error status bit.

*kSDMMC\_R1EraseParameterErrorFlag* Erase parameter error status bit.

*kSDMMC\_R1WriteProtectViolationFlag* Write protection violation status bit.

*kSDMMC\_R1CardIsLockedFlag* Card locked status bit.

*kSDMMC\_R1LockUnlockFailedFlag* lock/unlock error status bit

*kSDMMC\_R1CommandCrcErrorFlag* CRC error status bit.

*kSDMMC\_R1IllegalCommandFlag* Illegal command status bit.

*kSDMMC\_R1CardEccFailedFlag* Card ecc error status bit.

*kSDMMC\_R1CardControllerErrorFlag* Internal card controller error status bit.

*kSDMMC\_R1ErrorFlag* A general or an unknown error status bit.

*kSDMMC\_R1CidCsdOverwriteFlag* Cid/csd overwrite status bit.

*kSDMMC\_R1WriteProtectEraseSkipFlag* Write protection erase skip status bit.

*kSDMMC\_R1CardEccDisabledFlag* Card ecc disabled status bit.

*kSDMMC\_R1EraseResetFlag* Erase reset status bit.

*kSDMMC\_R1ReadyForDataFlag* Ready for data status bit.

*kSDMMC\_R1SwitchErrorFlag* Switch error status bit.

*kSDMMC\_R1ApplicationCommandFlag* Application command enabled status bit.

*kSDMMC\_R1AuthenticationSequenceErrorFlag* error in the sequence of authentication process

#### 54.7.4.12 enum sdmmc\_r1\_current\_state\_t

Enumerator

*kSDMMC\_R1StateIdle* R1: current state: idle.  
*kSDMMC\_R1StateReady* R1: current state: ready.  
*kSDMMC\_R1StateIdentify* R1: current state: identification.  
*kSDMMC\_R1StateStandby* R1: current state: standby.  
*kSDMMC\_R1StateTransfer* R1: current state: transfer.  
*kSDMMC\_R1StateSendData* R1: current state: sending data.  
*kSDMMC\_R1StateReceiveData* R1: current state: receiving data.  
*kSDMMC\_R1StateProgram* R1: current state: programming.  
*kSDMMC\_R1StateDisconnect* R1: current state: disconnect.

#### 54.7.4.13 anonymous enum

Enumerator

*kSDSPI\_R1InIdleStateFlag* In idle state.  
*kSDSPI\_R1EraseResetFlag* Erase reset.  
*kSDSPI\_R1IllegalCommandFlag* Illegal command.  
*kSDSPI\_R1CommandCrcErrorFlag* Com crc error.  
*kSDSPI\_R1EraseSequenceErrorFlag* Erase sequence error.  
*kSDSPI\_R1AddressErrorFlag* Address error.  
*kSDSPI\_R1ParameterErrorFlag* Parameter error.

#### 54.7.4.14 anonymous enum

Enumerator

*kSDSPI\_R2CardLockedFlag* Card is locked.  
*kSDSPI\_R2WriteProtectEraseSkip* Write protect erase skip.  
*kSDSPI\_R2LockUnlockFailed* Lock/unlock command failed.  
*kSDSPI\_R2ErrorFlag* Unknown error.  
*kSDSPI\_R2CardControllerErrorFlag* Card controller error.  
*kSDSPI\_R2CardEccFailedFlag* Card ecc failed.  
*kSDSPI\_R2WriteProtectViolationFlag* Write protect violation.  
*kSDSPI\_R2EraseParameterErrorFlag* Erase parameter error.  
*kSDSPI\_R2OutOfRangeFlag* Out of range.  
*kSDSPI\_R2CsdOverwriteFlag* CSD overwrite.

#### 54.7.4.15 anonymous enum

Enumerator

*kSDSPI\_DataErrorTokenError* Data error.  
*kSDSPI\_DataErrorTokenCardControllerError* Card controller error.  
*kSDSPI\_DataErrorTokenCardEccFailed* Card ecc error.  
*kSDSPI\_DataErrorTokenOutOfRange* Out of range.

#### 54.7.4.16 enum sdspi\_data\_token\_t

Enumerator

*kSDSPI\_DataTokenBlockRead* Single block read, multiple block read.  
*kSDSPI\_DataTokenSingleBlockWrite* Single block write.  
*kSDSPI\_DataTokenMultipleBlockWrite* Multiple block write.  
*kSDSPI\_DataTokenStopTransfer* Stop transmission.

#### 54.7.4.17 enum sdspi\_data\_response\_token\_t

Enumerator

*kSDSPI\_DataResponseTokenAccepted* Data accepted.  
*kSDSPI\_DataResponseTokenCrcError* Data rejected due to CRC error.  
*kSDSPI\_DataResponseTokenWriteError* Data rejected due to write error.

#### 54.7.4.18 enum sd\_command\_t

Enumerator

*kSD\_SendRelativeAddress* Send Relative Address.  
*kSD\_Switch* Switch Function.  
*kSD\_SendInterfaceCondition* Send Interface Condition.  
*kSD\_VoltageSwitch* Voltage Switch.  
*kSD\_SpeedClassControl* Speed Class control.  
*kSD\_EraseWriteBlockStart* Write Block Start.  
*kSD\_EraseWriteBlockEnd* Write Block End.  
*kSD\_SendTuningBlock* Send Tuning Block.

#### 54.7.4.19 enum sdspi\_command\_t

Enumerator

*kSDSPI\_CommandCrc* Command crc protection on/off.

#### 54.7.4.20 enum sd\_application\_command\_t

Enumerator

*kSD\_ApplicationSetBusWidth* Set Bus Width.  
*kSD\_ApplicationStatus* Send SD status.  
*kSD\_ApplicationSendNumberWriteBlocks* Send Number Of Written Blocks.  
*kSD\_ApplicationSetWriteBlockEraseCount* Set Write Block Erase Count.  
*kSD\_ApplicationSendOperationCondition* Send Operation Condition.  
*kSD\_ApplicationSetClearCardDetect* Set Connnect/Disconnect pull up on detect pin.  
*kSD\_ApplicationSendScr* Send Scr.

#### 54.7.4.21 anonymous enum

Enumerator

*kSDMMC\_CommandClassBasic* Card command class 0.  
*kSDMMC\_CommandClassBlockRead* Card command class 2.  
*kSDMMC\_CommandClassBlockWrite* Card command class 4.  
*kSDMMC\_CommandClassErase* Card command class 5.  
*kSDMMC\_CommandClassWriteProtect* Card command class 6.  
*kSDMMC\_CommandClassLockCard* Card command class 7.  
*kSDMMC\_CommandClassApplicationSpecific* Card command class 8.  
*kSDMMC\_CommandClassInputOutputMode* Card command class 9.  
*kSDMMC\_CommandClassSwitch* Card command class 10.

#### 54.7.4.22 anonymous enum

Enumerator

*kSD\_OcrPowerUpBusyFlag* Power up busy status.  
*kSD\_OcrHostCapacitySupportFlag* Card capacity status.  
*kSD\_OcrCardCapacitySupportFlag* Card capacity status.  
*kSD\_OcrSwitch18RequestFlag* Switch to 1.8V request.  
*kSD\_OcrSwitch18AcceptFlag* Switch to 1.8V accepted.  
*kSD\_OcrVdd27\_28Flag* VDD 2.7-2.8.  
*kSD\_OcrVdd28\_29Flag* VDD 2.8-2.9.  
*kSD\_OcrVdd29\_30Flag* VDD 2.9-3.0.  
*kSD\_OcrVdd30\_31Flag* VDD 2.9-3.0.  
*kSD\_OcrVdd31\_32Flag* VDD 3.0-3.1.  
*kSD\_OcrVdd32\_33Flag* VDD 3.1-3.2.  
*kSD\_OcrVdd33\_34Flag* VDD 3.2-3.3.  
*kSD\_OcrVdd34\_35Flag* VDD 3.3-3.4.  
*kSD\_OcrVdd35\_36Flag* VDD 3.4-3.5.

#### 54.7.4.23 anonymous enum

Enumerator

*kSD\_SpecificationVersion1\_0* SD card version 1.0-1.01.

*kSD\_SpecificationVersion1\_1* SD card version 1.10.

*kSD\_SpecificationVersion2\_0* SD card version 2.00.

*kSD\_SpecificationVersion3\_0* SD card version 3.0.

#### 54.7.4.24 enum sd\_switch\_mode\_t

Enumerator

*kSD\_SwitchCheck* SD switch mode 0: check function.

*kSD\_SwitchSet* SD switch mode 1: set function.

#### 54.7.4.25 anonymous enum

Enumerator

*kSD\_CsdReadBlockPartialFlag* Partial blocks for read allowed [79:79].

*kSD\_CsdWriteBlockMisalignFlag* Write block misalignment [78:78].

*kSD\_CsdReadBlockMisalignFlag* Read block misalignment [77:77].

*kSD\_CsdDsrImplementedFlag* DSR implemented [76:76].

*kSD\_CsdEraseBlockEnabledFlag* Erase single block enabled [46:46].

*kSD\_CsdWriteProtectGroupEnabledFlag* Write protect group enabled [31:31].

*kSD\_CsdWriteBlockPartialFlag* Partial blocks for write allowed [21:21].

*kSD\_CsdFileFormatGroupFlag* File format group [15:15].

*kSD\_CsdCopyFlag* Copy flag [14:14].

*kSD\_CsdPermanentWriteProtectFlag* Permanent write protection [13:13].

*kSD\_CsdTemporaryWriteProtectFlag* Temporary write protection [12:12].

#### 54.7.4.26 anonymous enum

Enumerator

*kSD\_ScrDataStatusAfterErase* Data status after erases [55:55].

*kSD\_ScrSdSpecification3* Specification version 3.00 or higher [47:47].

#### 54.7.4.27 anonymous enum

Enumerator

*kSD\_FunctionSDR12Default* SDR12 mode & default.

*kSD\_FunctionSDR25HighSpeed* SDR25 & high speed.

*kSD\_FunctionSDR50* SDR50 mode.  
*kSD\_FunctionSDR104* SDR104 mode.  
*kSD\_FunctionDDR50* DDR50 mode.

#### 54.7.4.28 anonymous enum

Enumerator

*kSD\_GroupTimingMode* access mode group  
*kSD\_GroupCommandSystem* command system group  
*kSD\_GroupDriverStrength* driver strength group  
*kSD\_GroupCurrentLimit* current limit group

#### 54.7.4.29 enum sd\_timing\_mode\_t

Enumerator

*kSD\_TimingSDR12DefaultMode* Identification mode & SDR12.  
*kSD\_TimingSDR25HighSpeedMode* High speed mode & SDR25.  
*kSD\_TimingSDR50Mode* SDR50 mode.  
*kSD\_TimingSDR104Mode* SDR104 mode.  
*kSD\_TimingDDR50Mode* DDR50 mode.

#### 54.7.4.30 enum sd\_driver\_strength\_t

Enumerator

*kSD\_DriverStrengthTypeB* default driver strength  
*kSD\_DriverStrengthTypeA* driver strength TYPE A  
*kSD\_DriverStrengthTypeC* driver strength TYPE C  
*kSD\_DriverStrengthTypeD* driver strength TYPE D

#### 54.7.4.31 enum sd\_max\_current\_t

Enumerator

*kSD\_CurrentLimit200MA* default current limit  
*kSD\_CurrentLimit400MA* current limit to 400MA  
*kSD\_CurrentLimit600MA* current limit to 600MA  
*kSD\_CurrentLimit800MA* current limit to 800MA

#### 54.7.4.32 enum sdmmc\_command\_t

Enumerator

*kSDMMC\_GoIdleState* Go Idle State.  
*kSDMMC\_AllSendCid* All Send CID.  
*kSDMMC\_SetDsr* Set DSR.  
*kSDMMC\_SelectCard* Select Card.  
*kSDMMC\_SendCsd* Send CSD.  
*kSDMMC\_SendCid* Send CID.  
*kSDMMC\_StopTransmission* Stop Transmission.  
*kSDMMC\_SendStatus* Send Status.  
*kSDMMC\_GoInactiveState* Go Inactive State.  
*kSDMMC\_SetBlockLength* Set Block Length.  
*kSDMMC\_ReadSingleBlock* Read Single Block.  
*kSDMMC\_ReadMultipleBlock* Read Multiple Block.  
*kSDMMC\_SetBlockCount* Set Block Count.  
*kSDMMC\_WriteSingleBlock* Write Single Block.  
*kSDMMC\_WriteMultipleBlock* Write Multiple Block.  
*kSDMMC\_ProgramCsd* Program CSD.  
*kSDMMC\_SetWriteProtect* Set Write Protect.  
*kSDMMC\_ClearWriteProtect* Clear Write Protect.  
*kSDMMC\_SendWriteProtect* Send Write Protect.  
*kSDMMC\_Erase* Erase.  
*kSDMMC\_LockUnlock* Lock Unlock.  
*kSDMMC\_ApplicationCommand* Send Application Command.  
*kSDMMC\_GeneralCommand* General Purpose Command.  
*kSDMMC\_ReadOcr* Read OCR.

#### 54.7.4.33 anonymous enum

Enumerator

*kSDIO\_RegCCCRSdioVer* CCCR & SDIO version.  
*kSDIO\_RegSDVersion* SD version.  
*kSDIO\_RegIOEnable* io enable register  
*kSDIO\_RegIOReady* io ready register  
*kSDIO\_RegIOIntEnable* io interrupt enable register  
*kSDIO\_RegIOIntPending* io interrupt pending register  
*kSDIO\_RegIOAbort* io abort register  
*kSDIO\_RegBusInterface* bus interface register  
*kSDIO\_RegCardCapability* card capability register  
*kSDIO\_RegCommonCISPointer* common CIS pointer register  
*kSDIO\_RegBusSuspend* bus suspend register  
*kSDIO\_RegFunctionSelect* function select register  
*kSDIO\_RegExecutionFlag* execution flag register

*kSDIO\_RegReadyFlag* ready flag register  
*kSDIO\_RegFN0BlockSizeLow* FN0 block size register.  
*kSDIO\_RegFN0BlockSizeHigh* FN0 block size register.  
*kSDIO\_RegPowerControl* power control register  
*kSDIO\_RegBusSpeed* bus speed register  
*kSDIO\_RegUHSITimingSupport* UHS-I timing support register.  
*kSDIO\_RegDriverStrength* Driver strength register.  
*kSDIO\_RegInterruptExtension* Interrupt extension register.

#### 54.7.4.34 enum sdio\_command\_t

Enumerator

*kSDIO\_SendRelativeAddress* send relative address  
*kSDIO\_SendOperationCondition* send operation condition  
*kSDIO\_SendInterfaceCondition* send interface condition  
*kSDIO\_RWIODirect* read/write IO direct command  
*kSDIO\_RWIOExtended* read/write IO extended command

#### 54.7.4.35 enum sdio\_func\_num\_t

Enumerator

*kSDIO\_FunctionNum0* sdio function0  
*kSDIO\_FunctionNum1* sdio function1  
*kSDIO\_FunctionNum2* sdio function2  
*kSDIO\_FunctionNum3* sdio function3  
*kSDIO\_FunctionNum4* sdio function4  
*kSDIO\_FunctionNum5* sdio function5  
*kSDIO\_FunctionNum6* sdio function6  
*kSDIO\_FunctionNum7* sdio function7  
*kSDIO\_FunctionMemory* for combo card

#### 54.7.4.36 anonymous enum

Enumerator

*kSDIO\_StatusCmdCRCError* the CRC check of the previous cmd fail  
*kSDIO\_StatusIllegalCmd* cmd illegal for the card state  
*kSDIO\_StatusR6Error* special for R6 error status  
*kSDIO\_StatusError* A general or an unknown error occurred.  
*kSDIO\_StatusFunctionNumError* invalid function error  
*kSDIO\_StatusOutOfRange* cmd argument was out of the allowed range

#### 54.7.4.37 anonymous enum

Enumerator

|                                 |                       |
|---------------------------------|-----------------------|
| <i>kSDIO_OcrPowerUpBusyFlag</i> | Power up busy status. |
| <i>kSDIO_OcrIONumber</i>        | number of IO function |
| <i>kSDIO_OcrMemPresent</i>      | memory present flag   |
| <i>kSDIO_OcrVdd20_21Flag</i>    | VDD 2.0-2.1.          |
| <i>kSDIO_OcrVdd21_22Flag</i>    | VDD 2.1-2.2.          |
| <i>kSDIO_OcrVdd22_23Flag</i>    | VDD 2.2-2.3.          |
| <i>kSDIO_OcrVdd23_24Flag</i>    | VDD 2.3-2.4.          |
| <i>kSDIO_OcrVdd24_25Flag</i>    | VDD 2.4-2.5.          |
| <i>kSDIO_OcrVdd25_26Flag</i>    | VDD 2.5-2.6.          |
| <i>kSDIO_OcrVdd26_27Flag</i>    | VDD 2.6-2.7.          |
| <i>kSDIO_OcrVdd27_28Flag</i>    | VDD 2.7-2.8.          |
| <i>kSDIO_OcrVdd28_29Flag</i>    | VDD 2.8-2.9.          |
| <i>kSDIO_OcrVdd29_30Flag</i>    | VDD 2.9-3.0.          |
| <i>kSDIO_OcrVdd30_31Flag</i>    | VDD 2.9-3.0.          |
| <i>kSDIO_OcrVdd31_32Flag</i>    | VDD 3.0-3.1.          |
| <i>kSDIO_OcrVdd32_33Flag</i>    | VDD 3.1-3.2.          |
| <i>kSDIO_OcrVdd33_34Flag</i>    | VDD 3.2-3.3.          |
| <i>kSDIO_OcrVdd34_35Flag</i>    | VDD 3.3-3.4.          |
| <i>kSDIO_OcrVdd35_36Flag</i>    | VDD 3.4-3.5.          |

#### 54.7.4.38 anonymous enum

Enumerator

|                                                  |                                              |
|--------------------------------------------------|----------------------------------------------|
| <i>kSDIO_CCCRSupportDirectCmdDuringDataTrans</i> | support direct cmd during data transfer      |
| <i>kSDIO_CCCRSupportMultiBlock</i>               | support multi block mode                     |
| <i>kSDIO_CCCRSupportReadWait</i>                 | support read wait                            |
| <i>kSDIO_CCCRSupportSuspendResume</i>            | support suspend resume                       |
| <i>kSDIO_CCCRSupportIntDuring4BitDataTrans</i>   | support interrupt during 4-bit data transfer |
| <i>kSDIO_CCCRSupportLowSpeed1Bit</i>             | support low speed 1bit mode                  |
| <i>kSDIO_CCCRSupportLowSpeed4Bit</i>             | support low speed 4bit mode                  |
| <i>kSDIO_CCCRSupportMasterPowerControl</i>       | support master power control                 |
| <i>kSDIO_CCCRSupportHighSpeed</i>                | support high speed                           |
| <i>kSDIO_CCCRSupportContinuousSPIInt</i>         | support continuous SPI interrupt             |

#### 54.7.4.39 anonymous enum

Enumerator

|                                       |                                  |
|---------------------------------------|----------------------------------|
| <i>kSDIO_FBRSupportCSA</i>            | function support CSA             |
| <i>kSDIO_FBRSupportPowerSelection</i> | function support power selection |

**54.7.4.40 enum sdio\_bus\_width\_t**

Enumerator

*kSDIO\_DataBus1Bit* 1 bit bus mode  
*kSDIO\_DataBus4Bit* 4 bit bus mode  
*kSDIO\_DataBus8Bit* 8 bit bus mode

**54.7.4.41 enum mmc\_command\_t**

Enumerator

*kMMC\_SendOperationCondition* Send Operation Condition.  
*kMMC\_SetRelativeAddress* Set Relative Address.  
*kMMC\_SleepAwake* Sleep Awake.  
*kMMC\_Switch* Switch.  
*kMMC\_SendExtendedCsd* Send EXT\_CSD.  
*kMMC\_ReadDataUntilStop* Read Data Until Stop.  
*kMMC\_BusTestRead* Test Read.  
*kMMC\_SendingBusTest* test bus width cmd  
*kMMC\_WriteDataUntilStop* Write Data Until Stop.  
*kMMC\_SendTuningBlock* MMC sending tuning block.  
*kMMC\_ProgramCid* Program CID.  
*kMMC\_EraseGroupStart* Erase Group Start.  
*kMMC\_EraseGroupEnd* Erase Group End.  
*kMMC\_FastInputOutput* Fast IO.  
*kMMC\_GoInterruptState* Go interrupt State.

**54.7.4.42 enum mmc\_classified\_voltage\_t**

Enumerator

*kMMC\_ClassifiedVoltageHigh* High-voltage MMC card.  
*kMMC\_ClassifiedVoltageDual* Dual-voltage MMC card.

**54.7.4.43 enum mmc\_classified\_density\_t**

Enumerator

*kMMC\_ClassifiedDensityWithin2GB* Density byte is less than or equal 2GB.

**54.7.4.44 enum mmc\_access\_mode\_t**

Enumerator

*kMMC\_AccessModeByte* The card should be accessed as byte.*kMMC\_AccessModeSector* The card should be accessed as sector.**54.7.4.45 enum mmc\_voltage\_window\_t**

Enumerator

*kMMC\_VoltageWindowNone* voltage window is not define by user*kMMC\_VoltageWindow120* Voltage window is 1.20V.*kMMC\_VoltageWindow170to195* Voltage window is 1.70V to 1.95V.*kMMC\_VoltageWindows270to360* Voltage window is 2.70V to 3.60V.**54.7.4.46 enum mmc\_csd\_structure\_version\_t**

Enumerator

*kMMC\_CsdStrucureVersion10* CSD version No. 1.0*kMMC\_CsdStrucureVersion11* CSD version No. 1.1*kMMC\_CsdStrucureVersion12* CSD version No. 1.2*kMMC\_CsdStrucureVersionInExtcsd* Version coded in Extended CSD.**54.7.4.47 enum mmc\_specification\_version\_t**

Enumerator

*kMMC\_SpecificationVersion0* Allocated by MMCA.*kMMC\_SpecificationVersion1* Allocated by MMCA.*kMMC\_SpecificationVersion2* Allocated by MMCA.*kMMC\_SpecificationVersion3* Allocated by MMCA.*kMMC\_SpecificationVersion4* Version 4.1/4.2/4.3/4.41-4.5-4.51-5.0.**54.7.4.48 anonymous enum**

Enumerator

*kMMC\_ExtendedCsdRevision10* Revision 1.0.*kMMC\_ExtendedCsdRevision11* Revision 1.1.*kMMC\_ExtendedCsdRevision12* Revision 1.2.*kMMC\_ExtendedCsdRevision13* Revision 1.3 MMC4.3.*kMMC\_ExtendedCsdRevision14* Revision 1.4 obsolete.

- kMMC\_ExtendedCsdRevision15* Revision 1.5 MMC4.41.
- kMMC\_ExtendedCsdRevision16* Revision 1.6 MMC4.5.
- kMMC\_ExtendedCsdRevision17* Revision 1.7 MMC5.0.

#### 54.7.4.49 enum mmc\_command\_set\_t

Enumerator

- kMMC\_CommandSetStandard* Standard MMC.
- kMMC\_CommandSet1* Command set 1.
- kMMC\_CommandSet2* Command set 2.
- kMMC\_CommandSet3* Command set 3.
- kMMC\_CommandSet4* Command set 4.

#### 54.7.4.50 anonymous enum

Enumerator

- kMMC\_SupportAlternateBoot* support alternative boot mode
- kMMC\_SupportDDRBoot* support DDR boot mode
- kMMC\_SupportHighSpeedBoot* support high speed boot mode

#### 54.7.4.51 enum mmc\_high\_speed\_timing\_t

Enumerator

- kMMC\_HighSpeedTimingNone* MMC card using none high-speed timing.
- kMMC\_HighSpeedTiming* MMC card using high-speed timing.
- kMMC\_HighSpeed200Timing* MMC card high speed 200 timing.
- kMMC\_HighSpeed400Timing* MMC card high speed 400 timing.
- kMMC\_EnhanceHighSpeed400Timing* MMC card high speed 400 timing.

#### 54.7.4.52 enum mmc\_data\_bus\_width\_t

Enumerator

- kMMC\_DataBusWidth1bit* MMC data bus width is 1 bit.
- kMMC\_DataBusWidth4bit* MMC data bus width is 4 bits.
- kMMC\_DataBusWidth8bit* MMC data bus width is 8 bits.
- kMMC\_DataBusWidth4bitDDR* MMC data bus width is 4 bits ddr.
- kMMC\_DataBusWidth8bitDDR* MMC data bus width is 8 bits ddr.
- kMMC\_DataBusWidth8bitDDRSTROBE* MMC data bus width is 8 bits ddr strobe mode.

#### 54.7.4.53 enum mmc\_boot\_partition\_enable\_t

Enumerator

*kMMC\_BootPartitionEnableNot* Device not boot enabled (default)

*kMMC\_BootPartitionEnablePartition1* Boot partition 1 enabled for boot.

*kMMC\_BootPartitionEnablePartition2* Boot partition 2 enabled for boot.

*kMMC\_BootPartitionEnableUserAera* User area enabled for boot.

#### 54.7.4.54 enum mmc\_boot\_timing\_mode\_t

Enumerator

*kMMC\_BootModeSDRWithDefaultTiming* boot mode single data rate with backward compatible timings

*kMMC\_BootModeSDRWithHighSpeedTiming* boot mode single data rate with high speed timing

*kMMC\_BootModeDDRTiming* boot mode dual date rate

#### 54.7.4.55 enum mmc\_boot\_partition\_wp\_t

Enumerator

*kMMC\_BootPartitionWPDisable* boot partition write protection disable

*kMMC\_BootPartitionPwrWPToBothPartition* power on period write protection apply to both boot partitions

*kMMC\_BootPartitionPermWPToBothPartition* permanent write protection apply to both boot partitions

*kMMC\_BootPartitionPwrWPToPartition1* power on period write protection apply to partition1

*kMMC\_BootPartitionPwrWPToPartition2* power on period write protection apply to partition2

*kMMC\_BootPartitionPermWPToPartition1* permanent write protection apply to partition1

*kMMC\_BootPartitionPermWPToPartition2* permanent write protection apply to partition2

*kMMC\_BootPartitionPermWPToPartition1PwrWPToPartition2* permanent write protection apply to partition1, power on period write protection apply to partition2

*kMMC\_BootPartitionPermWPToPartition2PwrWPToPartition1* permanent write protection apply to partition2, power on period write protection apply to partition1

#### 54.7.4.56 anonymous enum

Enumerator

*kMMC\_BootPartitionNotProtected* boot partition not protected

*kMMC\_BootPartitionPwrProtected* boot partition is power on period write protected

*kMMC\_BootPartitionPermProtected* boot partition is permanently protected

#### 54.7.4.57 enum mmc\_access\_partition\_t

Enumerator

*kMMC\_AccessPartitionUserAera* No access to boot partition (default), normal partition.  
*kMMC\_AccessPartitionBoot1* Read/Write boot partition 1.  
*kMMC\_AccessPartitionBoot2* Read/Write boot partition 2.  
*kMMC\_AccessRPMB* Replay protected mem block.  
*kMMC\_AccessGeneralPurposePartition1* access to general purpose partition 1  
*kMMC\_AccessGeneralPurposePartition2* access to general purpose partition 2  
*kMMC\_AccessGeneralPurposePartition3* access to general purpose partition 3  
*kMMC\_AccessGeneralPurposePartition4* access to general purpose partition 4

#### 54.7.4.58 anonymous enum

Enumerator

*kMMC\_CsdReadBlockPartialFlag* Partial blocks for read allowed.  
*kMMC\_CsdWriteBlockMisalignFlag* Write block misalignment.  
*kMMC\_CsdReadBlockMisalignFlag* Read block misalignment.  
*kMMC\_CsdDsrImplementedFlag* DSR implemented.  
*kMMC\_CsdWriteProtectGroupEnabledFlag* Write protect group enabled.  
*kMMC\_CsdWriteBlockPartialFlag* Partial blocks for write allowed.  
*kMMC\_ContentProtectApplicationFlag* Content protect application.  
*kMMC\_CsdFileFormatGroupFlag* File format group.  
*kMMC\_CsdCopyFlag* Copy flag.  
*kMMC\_CsdPermanentWriteProtectFlag* Permanent write protection.  
*kMMC\_CsdTemporaryWriteProtectFlag* Temporary write protection.

#### 54.7.4.59 enum mmc\_extended\_csd\_access\_mode\_t

Enumerator

*kMMC\_ExtendedCsdAccessModeCommandSet* Command set related setting.  
*kMMC\_ExtendedCsdAccessModeSetBits* Set bits in specific byte in Extended CSD.  
*kMMC\_ExtendedCsdAccessModeClearBits* Clear bits in specific byte in Extended CSD.  
*kMMC\_ExtendedCsdAccessModeWriteBits* Write a value to specific byte in Extended CSD.

#### 54.7.4.60 enum mmc\_extended\_csd\_index\_t

Enumerator

*kMMC\_ExtendedCsdIndexFlushCache* flush cache  
*kMMC\_ExtendedCsdIndexCacheControl* cache control

*kMMC\_ExtendedCsdIndexBootPartitionWP* Boot partition write protect.  
*kMMC\_ExtendedCsdIndexEraseGroupDefinition* Erase Group Def.  
*kMMC\_ExtendedCsdIndexBootBusConditions* Boot Bus conditions.  
*kMMC\_ExtendedCsdIndexBootConfigWP* Boot config write protect.  
*kMMC\_ExtendedCsdIndexPartitionConfig* Partition Config, before BOOT\_CONFIG.  
*kMMC\_ExtendedCsdIndexBusWidth* Bus Width.  
*kMMC\_ExtendedCsdIndexHighSpeedTiming* High-speed Timing.  
*kMMC\_ExtendedCsdIndexPowerClass* Power Class.  
*kMMC\_ExtendedCsdIndexCommandSet* Command Set.

#### 54.7.4.61 anonymous enum

Enumerator

*kMMC\_DriverStrength0* Driver type0 ,nominal impedance 50ohm.  
*kMMC\_DriverStrength1* Driver type1 ,nominal impedance 33ohm.  
*kMMC\_DriverStrength2* Driver type2 ,nominal impedance 66ohm.  
*kMMC\_DriverStrength3* Driver type3 ,nominal impedance 100ohm.  
*kMMC\_DriverStrength4* Driver type4 ,nominal impedance 40ohm.

#### 54.7.4.62 enum mmc\_extended\_csd\_flags\_t

Enumerator

*kMMC\_ExtCsdExtPartitionSupport* partitioning support[160]  
*kMMC\_ExtCsdEnhancePartitionSupport* partitioning support[160]  
*kMMC\_ExtCsdPartitioningSupport* partitioning support[160]  
*kMMC\_ExtCsdPrgCIDCSDInDDRModeSupport* CMD26 and CMD27 are support dual data rate [130].  
*kMMC\_ExtCsdBKOpsSupport* background operation feature support [502]  
*kMMC\_ExtCsdDataTagSupport* data tag support[499]  
*kMMC\_ExtCsdModeOperationCodeSupport* mode operation code support[493]

#### 54.7.4.63 enum mmc\_boot\_mode\_t

Enumerator

*kMMC\_BootModeNormal* Normal boot.  
*kMMC\_BootModeAlternative* Alternative boot.

## 54.7.5 Function Documentation

54.7.5.1 `status_t SDMMC_SelectCard ( sdmmchost_t * host, uint32_t relativeAddress, bool isSelected )`

Parameters

|                        |                                       |
|------------------------|---------------------------------------|
| <i>host</i>            | host handler.                         |
| <i>relativeAddress</i> | Relative address.                     |
| <i>isSelected</i>      | True to put card into transfer state. |

Return values

|                                     |                       |
|-------------------------------------|-----------------------|
| <i>kStatus_SDMMC_TransferFailed</i> | Transfer failed.      |
| <i>kStatus_Success</i>              | Operate successfully. |

#### 54.7.5.2 status\_t SDMMC\_SendApplicationCommand ( *sdmmchost\_t \* host, uint32\_t relativeAddress* )

Parameters

|                        |                        |
|------------------------|------------------------|
| <i>host</i>            | host handler.          |
| <i>relativeAddress</i> | Card relative address. |

Return values

|                                     |                       |
|-------------------------------------|-----------------------|
| <i>kStatus_SDMMC_TransferFailed</i> | Transfer failed.      |
| <i>kStatus_SDMMC_CardNotSupport</i> | Card doesn't support. |
| <i>kStatus_Success</i>              | Operate successfully. |

#### 54.7.5.3 status\_t SDMMC\_SetBlockCount ( *sdmmchost\_t \* host, uint32\_t blockCount* )

Parameters

|                   |               |
|-------------------|---------------|
| <i>host</i>       | host handler. |
| <i>blockCount</i> | Block count.  |

Return values

|                                     |                       |
|-------------------------------------|-----------------------|
| <i>kStatus_SDMMC_TransferFailed</i> | Transfer failed.      |
| <i>kStatus_Success</i>              | Operate successfully. |

#### 54.7.5.4 status\_t SDMMC\_GoIdle ( *sdmmchost\_t \* host* )

Parameters

|             |               |
|-------------|---------------|
| <i>host</i> | host handler. |
|-------------|---------------|

Return values

|                                     |                       |
|-------------------------------------|-----------------------|
| <i>kStatus_SDMMC_TransferFailed</i> | Transfer failed.      |
| <i>kStatus_Success</i>              | Operate successfully. |

#### 54.7.5.5 status\_t SDMMC\_SetBlockSize ( *sdmmchost\_t \* host, uint32\_t blockSize* )

Parameters

|                  |               |
|------------------|---------------|
| <i>host</i>      | host handler. |
| <i>blockSize</i> | Block size.   |

Return values

|                                     |                       |
|-------------------------------------|-----------------------|
| <i>kStatus_SDMMC_TransferFailed</i> | Transfer failed.      |
| <i>kStatus_Success</i>              | Operate successfully. |

#### 54.7.5.6 status\_t SDMMC\_SetCardInactive ( *sdmmchost\_t \* host* )

Parameters

|             |               |
|-------------|---------------|
| <i>host</i> | host handler. |
|-------------|---------------|

Return values

|                                      |                       |
|--------------------------------------|-----------------------|
| <i>kStatus_SDMMC_-TransferFailed</i> | Transfer failed.      |
| <i>kStatus_Success</i>               | Operate successfully. |

# Chapter 55

## CODEC Driver

### 55.1 Overview

The MCUXpresso SDK provides a codec abstraction driver interface to access codec register.

### Modules

- [CODEC Common Driver](#)
- [CODEC I2C Driver](#)
- [CS42888 Driver](#)
- [DA7212 Driver](#)
- [SGTL5000 Driver](#)
- [WM8904 Driver](#)
- [WM8960 Driver](#)

## 55.2 CODEC Common Driver

### 55.2.1 Overview

The codec common driver provides a codec control abstraction interface.

## Modules

- CODEC Adapter
- CS42888 Adapter
- DA7212 Adapter
- SGTL5000 Adapter
- WM8904 Adapter
- WM8960 Adapter

## Data Structures

- struct `codec_config_t`  
*Initialize structure of the codec. [More...](#)*
- struct `codec_capability_t`  
*codec capability [More...](#)*
- struct `codec_handle_t`  
*Codec handle definition. [More...](#)*

## Macros

- #define `CODEC_VOLUME_MAX_VALUE` (100U)  
*codec maximum volume range*

## Enumerations

- enum {
   
  `kStatus_CODEC_NotSupport` = MAKE\_STATUS(kStatusGroup\_CODEC, 0U),
   
  `kStatus_CODEC_DeviceNotRegistered` = MAKE\_STATUS(kStatusGroup\_CODEC, 1U),
   
  `kStatus_CODEC_I2CBusInitialFailed`,
   
  `kStatus_CODEC_I2CCommandTransferFailed` }
   
*CODEC status.*
- enum `codec_audio_protocol_t` {
   
  `kCODEC_BusI2S` = 0U,
   
  `kCODEC_BusLeftJustified` = 1U,
   
  `kCODEC_BusRightJustified` = 2U,
   
  `kCODEC_BusPCMA` = 3U,
   
  `kCODEC_BusPCMB` = 4U,
   
  `kCODEC_BusTDM` = 5U }

*AUDIO format definition.*

- enum {
   
kCODEC\_AudioSampleRate8KHz = 8000U,  
 kCODEC\_AudioSampleRate11025Hz = 11025U,  
 kCODEC\_AudioSampleRate12KHz = 12000U,  
 kCODEC\_AudioSampleRate16KHz = 16000U,  
 kCODEC\_AudioSampleRate22050Hz = 22050U,  
 kCODEC\_AudioSampleRate24KHz = 24000U,  
 kCODEC\_AudioSampleRate32KHz = 32000U,  
 kCODEC\_AudioSampleRate44100Hz = 44100U,  
 kCODEC\_AudioSampleRate48KHz = 48000U,  
 kCODEC\_AudioSampleRate96KHz = 96000U,  
 kCODEC\_AudioSampleRate192KHz = 192000U,  
 kCODEC\_AudioSampleRate384KHz = 384000U }

*audio sample rate definition*

- enum {
   
kCODEC\_AudioBitWidth16bit = 16U,  
 kCODEC\_AudioBitWidth20bit = 20U,  
 kCODEC\_AudioBitWidth24bit = 24U,  
 kCODEC\_AudioBitWidth32bit = 32U }

*audio bit width*

- enum codec\_module\_t {
   
kCODEC\_ModuleADC = 0U,  
 kCODEC\_ModuleDAC = 1U,  
 kCODEC\_ModulePGA = 2U,  
 kCODEC\_ModuleHeadphone = 3U,  
 kCODEC\_ModuleSpeaker = 4U,  
 kCODEC\_ModuleLinein = 5U,  
 kCODEC\_ModuleLineout = 6U,  
 kCODEC\_ModuleVref = 7U,  
 kCODEC\_ModuleMicbias = 8U,  
 kCODEC\_ModuleMic = 9U,  
 kCODEC\_ModuleI2SIn = 10U,  
 kCODEC\_ModuleI2SOut = 11U,  
 kCODEC\_ModuleMixer = 12U }

*audio codec module*

- enum codec\_module\_ctrl\_cmd\_t { kCODEC\_ModuleSwitchI2SInInterface = 0U }

*audio codec module control cmd*

- enum {
   
kCODEC\_ModuleI2SInInterfacePCM = 0U,  
 kCODEC\_ModuleI2SInInterfaceDSD = 1U }

*audio codec module digital interface*

- enum {

- ```

kCODEC_RecordSourceDifferentialLine = 1U,
kCODEC_RecordSourceLineInput = 2U,
kCODEC_RecordSourceDifferentialMic = 4U,
kCODEC_RecordSourceDigitalMic = 8U,
kCODEC_RecordSourceSingleEndMic = 16U }
    audio codec module record source value
```
- enum {
 

```

kCODEC_RecordChannelLeft1 = 1U,
kCODEC_RecordChannelLeft2 = 2U,
kCODEC_RecordChannelLeft3 = 4U,
kCODEC_RecordChannelRight1 = 1U,
kCODEC_RecordChannelRight2 = 2U,
kCODEC_RecordChannelRight3 = 4U,
kCODEC_RecordChannelDifferentialPositive1 = 1U,
kCODEC_RecordChannelDifferentialPositive2 = 2U,
kCODEC_RecordChannelDifferentialPositive3 = 4U,
kCODEC_RecordChannelDifferentialNegative1 = 8U,
kCODEC_RecordChannelDifferentialNegative2 = 16U,
kCODEC_RecordChannelDifferentialNegative3 = 32U }
```

*audio codec record channel*
- enum {
 

```

kCODEC_PlaySourcePGA = 1U,
kCODEC_PlaySourceInput = 2U,
kCODEC_PlaySourceDAC = 4U,
kCODEC_PlaySourceMixerIn = 1U,
kCODEC_PlaySourceMixerInLeft = 2U,
kCODEC_PlaySourceMixerInRight = 4U,
kCODEC_PlaySourceAux = 8U }
```

*audio codec module play source value*
- enum {
 

```

kCODEC_PlayChannelHeadphoneLeft = 1U,
kCODEC_PlayChannelHeadphoneRight = 2U,
kCODEC_PlayChannelSpeakerLeft = 4U,
kCODEC_PlayChannelSpeakerRight = 8U,
kCODEC_PlayChannelLineOutLeft = 16U,
kCODEC_PlayChannelLineOutRight = 32U,
kCODEC_PlayChannelLeft0 = 1U,
kCODEC_PlayChannelRight0 = 2U,
kCODEC_PlayChannelLeft1 = 4U,
kCODEC_PlayChannelRight1 = 8U,
kCODEC_PlayChannelLeft2 = 16U,
kCODEC_PlayChannelRight2 = 32U,
kCODEC_PlayChannelLeft3 = 64U,
kCODEC_PlayChannelRight3 = 128U }
```

*codec play channel*
- enum {

```
kCODEC_VolumeHeadphoneLeft = 1U,  
kCODEC_VolumeHeadphoneRight = 2U,  
kCODEC_VolumeSpeakerLeft = 4U,  
kCODEC_VolumeSpeakerRight = 8U,  
kCODEC_VolumeLineOutLeft = 16U,  
kCODEC_VolumeLineOutRight = 32U,  
kCODEC_VolumeLeft0 = 1UL << 0U,  
kCODEC_VolumeRight0 = 1UL << 1U,  
kCODEC_VolumeLeft1 = 1UL << 2U,  
kCODEC_VolumeRight1 = 1UL << 3U,  
kCODEC_VolumeLeft2 = 1UL << 4U,  
kCODEC_VolumeRight2 = 1UL << 5U,  
kCODEC_VolumeLeft3 = 1UL << 6U,  
kCODEC_VolumeRight3 = 1UL << 7U,  
kCODEC_VolumeDAC = 1UL << 8U }
```

*codec volume setting*

- enum {

```

kCODEC_SupportModuleADC = 1U << 0U,
kCODEC_SupportModuleDAC = 1U << 1U,
kCODEC_SupportModulePGA = 1U << 2U,
kCODEC_SupportModuleHeadphone = 1U << 3U,
kCODEC_SupportModuleSpeaker = 1U << 4U,
kCODEC_SupportModuleLinein = 1U << 5U,
kCODEC_SupportModuleLineout = 1U << 6U,
kCODEC_SupportModuleVref = 1U << 7U,
kCODEC_SupportModuleMicbias = 1U << 8U,
kCODEC_SupportModuleMic = 1U << 9U,
kCODEC_SupportModuleI2SIn = 1U << 10U,
kCODEC_SupportModuleI2SOut = 1U << 11U,
kCODEC_SupportModuleMixer = 1U << 12U,
kCODEC_SupportModuleI2SInSwitchInterface = 1U << 13U,
kCODEC_SupportPlayChannelLeft0 = 1U << 0U,
kCODEC_SupportPlayChannelRight0 = 1U << 1U,
kCODEC_SupportPlayChannelLeft1 = 1U << 2U,
kCODEC_SupportPlayChannelRight1 = 1U << 3U,
kCODEC_SupportPlayChannelLeft2 = 1U << 4U,
kCODEC_SupportPlayChannelRight2 = 1U << 5U,
kCODEC_SupportPlayChannelLeft3 = 1U << 6U,
kCODEC_SupportPlayChannelRight3 = 1U << 7U,
kCODEC_SupportPlaySourcePGA = 1U << 8U,
kCODEC_SupportPlaySourceInput = 1U << 9U,
kCODEC_SupportPlaySourceDAC = 1U << 10U,
kCODEC_SupportPlaySourceMixerIn = 1U << 11U,
kCODEC_SupportPlaySourceMixerInLeft = 1U << 12U,
kCODEC_SupportPlaySourceMixerInRight = 1U << 13U,
kCODEC_SupportPlaySourceAux = 1U << 14U,
kCODEC_SupportRecordSourceDifferentialLine = 1U << 0U,
kCODEC_SupportRecordSourceLineInput = 1U << 1U,
kCODEC_SupportRecordSourceDifferentialMic = 1U << 2U,
kCODEC_SupportRecordSourceDigitalMic = 1U << 3U,
kCODEC_SupportRecordSourceSingleEndMic = 1U << 4U,
kCODEC_SupportRecordChannelLeft1 = 1U << 6U,
kCODEC_SupportRecordChannelLeft2 = 1U << 7U,
kCODEC_SupportRecordChannelLeft3 = 1U << 8U,
kCODEC_SupportRecordChannelRight1 = 1U << 9U,
kCODEC_SupportRecordChannelRight2 = 1U << 10U,
kCODEC_SupportRecordChannelRight3 = 1U << 11U }

```

*audio codec capability*

## Functions

- `status_t CODEC_Init (codec_handle_t *handle, codec_config_t *config)`  
*Codec initialization.*
- `status_t CODEC_Deinit (codec_handle_t *handle)`  
*Codec de-initilization.*
- `status_t CODEC_SetFormat (codec_handle_t *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`  
*set audio data format.*
- `status_t CODEC_ModuleControl (codec_handle_t *handle, codec_module_ctrl_cmd_t cmd, uint32_t data)`  
*codec module control.*
- `status_t CODEC_SetVolume (codec_handle_t *handle, uint32_t channel, uint32_t volume)`  
*set audio codec pl volume.*
- `status_t CODEC_SetMute (codec_handle_t *handle, uint32_t channel, bool mute)`  
*set audio codec module mute.*
- `status_t CODEC_SetPower (codec_handle_t *handle, codec_module_t module, bool powerOn)`  
*set audio codec power.*
- `status_t CODEC_SetRecord (codec_handle_t *handle, uint32_t recordSource)`  
*codec set record source.*
- `status_t CODEC_SetRecordChannel (codec_handle_t *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)`  
*codec set record channel.*
- `status_t CODEC_SetPlay (codec_handle_t *handle, uint32_t playSource)`  
*codec set play source.*

## Driver version

- `#define FSL_CODEC_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))`  
*CLOCK driver version 2.3.1.*

### 55.2.2 Data Structure Documentation

#### 55.2.2.1 struct codec\_config\_t

##### Data Fields

- `uint32_t codecDevType`  
*codec type*
- `void *codecDevConfig`  
*Codec device specific configuration.*

### 55.2.2.2 struct codec\_capability\_t

#### Data Fields

- `uint32_t codecModuleCapability`  
*codec module capability*
- `uint32_t codecPlayCapability`  
*codec play capability*
- `uint32_t codecRecordCapability`  
*codec record capability*
- `uint32_t codecVolumeCapability`  
*codec volume capability*

### 55.2.2.3 struct \_codec\_handle

codec handle declaration

- Application should allocate a buffer with CODEC\_HANDLE\_SIZE for handle definition, such as `uint8_t codecHandleBuffer[CODEC_HANDLE_SIZE]; codec_handle_t *codecHandle = codecHandleBuffer;`

#### Data Fields

- `codec_config_t * codecConfig`  
*codec configuration function pointer*
- `const codec_capability_t * codecCapability`  
*codec capability*
- `uint8_t codecDevHandle [HAL_CODEC_HANDLER_SIZE]`  
*codec device handle*

### 55.2.3 Macro Definition Documentation

#### 55.2.3.1 #define FSL\_CODEC\_DRIVER\_VERSION (MAKE\_VERSION(2, 3, 1))

### 55.2.4 Enumeration Type Documentation

#### 55.2.4.1 anonymous enum

Enumerator

`kStatus_CODEC_NotSupport` CODEC not support status.

`kStatus_CODEC_DeviceNotRegistered` CODEC device register failed status.

`kStatus_CODEC_I2CBusInitialFailed` CODEC i2c bus initialization failed status.

`kStatus_CODEC_I2CCommandTransferFailed` CODEC i2c bus command transfer failed status.

#### 55.2.4.2 enum codec\_audio\_protocol\_t

Enumerator

- kCODEC\_BusI2S* I2S type.
- kCODEC\_BusLeftJustified* Left justified mode.
- kCODEC\_BusRightJustified* Right justified mode.
- kCODEC\_BusPCMA* DSP/PCM A mode.
- kCODEC\_BusPCMB* DSP/PCM B mode.
- kCODEC\_BusTDM* TDM mode.

#### 55.2.4.3 anonymous enum

Enumerator

- kCODEC\_AudioSampleRate8KHz* Sample rate 8000 Hz.
- kCODEC\_AudioSampleRate11025Hz* Sample rate 11025 Hz.
- kCODEC\_AudioSampleRate12KHz* Sample rate 12000 Hz.
- kCODEC\_AudioSampleRate16KHz* Sample rate 16000 Hz.
- kCODEC\_AudioSampleRate22050Hz* Sample rate 22050 Hz.
- kCODEC\_AudioSampleRate24KHz* Sample rate 24000 Hz.
- kCODEC\_AudioSampleRate32KHz* Sample rate 32000 Hz.
- kCODEC\_AudioSampleRate44100Hz* Sample rate 44100 Hz.
- kCODEC\_AudioSampleRate48KHz* Sample rate 48000 Hz.
- kCODEC\_AudioSampleRate96KHz* Sample rate 96000 Hz.
- kCODEC\_AudioSampleRate192KHz* Sample rate 192000 Hz.
- kCODEC\_AudioSampleRate384KHz* Sample rate 384000 Hz.

#### 55.2.4.4 anonymous enum

Enumerator

- kCODEC\_AudioBitWidth16bit* audio bit width 16
- kCODEC\_AudioBitWidth20bit* audio bit width 20
- kCODEC\_AudioBitWidth24bit* audio bit width 24
- kCODEC\_AudioBitWidth32bit* audio bit width 32

#### 55.2.4.5 enum codec\_module\_t

Enumerator

- kCODEC\_ModuleADC* codec module ADC
- kCODEC\_ModuleDAC* codec module DAC
- kCODEC\_ModulePGA* codec module PGA
- kCODEC\_ModuleHeadphone* codec module headphone

*kCODEC\_ModuleSpeaker* codec module speaker  
*kCODEC\_ModuleLinein* codec module linein  
*kCODEC\_ModuleLineout* codec module lineout  
*kCODEC\_ModuleVref* codec module VREF  
*kCODEC\_ModuleMicbias* codec module MIC BIAS  
*kCODEC\_ModuleMic* codec module MIC  
*kCODEC\_ModuleI2SIn* codec module I2S in  
*kCODEC\_ModuleI2SOut* codec module I2S out  
*kCODEC\_ModuleMixer* codec module mixer

#### 55.2.4.6 enum codec\_module\_ctrl\_cmd\_t

Enumerator

*kCODEC\_ModuleSwitchI2SInInterface* module digital interface siwtch.

#### 55.2.4.7 anonymous enum

Enumerator

*kCODEC\_ModuleI2SInInterfacePCM* Pcm interface.  
*kCODEC\_ModuleI2SInInterfaceDSD* DSD interface.

#### 55.2.4.8 anonymous enum

Enumerator

*kCODEC\_RecordSourceDifferentialLine* record source from differential line  
*kCODEC\_RecordSourceLineInput* record source from line input  
*kCODEC\_RecordSourceDifferentialMic* record source from differential mic  
*kCODEC\_RecordSourceDigitalMic* record source from digital microphone  
*kCODEC\_RecordSourceSingleEndMic* record source from single microphone

#### 55.2.4.9 anonymous enum

Enumerator

*kCODEC\_RecordChannelLeft1* left record channel 1  
*kCODEC\_RecordChannelLeft2* left record channel 2  
*kCODEC\_RecordChannelLeft3* left record channel 3  
*kCODEC\_RecordChannelRight1* right record channel 1  
*kCODEC\_RecordChannelRight2* right record channel 2  
*kCODEC\_RecordChannelRight3* right record channel 3  
*kCODEC\_RecordChannelDifferentialPositive1* differential positive record channel 1

*kCODEC\_RecordChannelDifferentialPositive2* differential positive record channel 2  
*kCODEC\_RecordChannelDifferentialPositive3* differential positive record channel 3  
*kCODEC\_RecordChannelDifferentialNegative1* differential negative record channel 1  
*kCODEC\_RecordChannelDifferentialNegative2* differential negative record channel 2  
*kCODEC\_RecordChannelDifferentialNegative3* differential negative record channel 3

#### 55.2.4.10 anonymous enum

Enumerator

*kCODEC\_PlaySourcePGA* play source PGA, bypass ADC  
*kCODEC\_PlaySourceInput* play source Input3  
*kCODEC\_PlaySourceDAC* play source DAC  
*kCODEC\_PlaySourceMixerIn* play source mixer in  
*kCODEC\_PlaySourceMixerInLeft* play source mixer in left  
*kCODEC\_PlaySourceMixerInRight* play source mixer in right  
*kCODEC\_PlaySourceAux* play source mixer in AUX

#### 55.2.4.11 anonymous enum

Enumerator

*kCODEC\_PlayChannelHeadphoneLeft* play channel headphone left  
*kCODEC\_PlayChannelHeadphoneRight* play channel headphone right  
*kCODEC\_PlayChannelSpeakerLeft* play channel speaker left  
*kCODEC\_PlayChannelSpeakerRight* play channel speaker right  
*kCODEC\_PlayChannelLineOutLeft* play channel lineout left  
*kCODEC\_PlayChannelLineOutRight* play channel lineout right  
*kCODEC\_PlayChannelLeft0* play channel left0  
*kCODEC\_PlayChannelRight0* play channel right0  
*kCODEC\_PlayChannelLeft1* play channel left1  
*kCODEC\_PlayChannelRight1* play channel right1  
*kCODEC\_PlayChannelLeft2* play channel left2  
*kCODEC\_PlayChannelRight2* play channel right2  
*kCODEC\_PlayChannelLeft3* play channel left3  
*kCODEC\_PlayChannelRight3* play channel right3

#### 55.2.4.12 anonymous enum

Enumerator

*kCODEC\_VolumeHeadphoneLeft* headphone left volume  
*kCODEC\_VolumeHeadphoneRight* headphone right volume  
*kCODEC\_VolumeSpeakerLeft* speaker left volume  
*kCODEC\_VolumeSpeakerRight* speaker right volume

*kCODEC\_VolumeLineOutLeft* lineout left volume  
*kCODEC\_VolumeLineOutRight* lineout right volume  
*kCODEC\_VolumeLeft0* left0 volume  
*kCODEC\_VolumeRight0* right0 volume  
*kCODEC\_VolumeLeft1* left1 volume  
*kCODEC\_VolumeRight1* right1 volume  
*kCODEC\_VolumeLeft2* left2 volume  
*kCODEC\_VolumeRight2* right2 volume  
*kCODEC\_VolumeLeft3* left3 volume  
*kCODEC\_VolumeRight3* right3 volume  
*kCODEC\_VolumeDAC* dac volume

#### 55.2.4.13 anonymous enum

Enumerator

*kCODEC\_SupportModuleADC* codec capability of module ADC  
*kCODEC\_SupportModuleDAC* codec capability of module DAC  
*kCODEC\_SupportModulePGA* codec capability of module PGA  
*kCODEC\_SupportModuleHeadphone* codec capability of module headphone  
*kCODEC\_SupportModuleSpeaker* codec capability of module speaker  
*kCODEC\_SupportModuleLinein* codec capability of module linein  
*kCODEC\_SupportModuleLineout* codec capability of module lineout  
*kCODEC\_SupportModuleVref* codec capability of module vref  
*kCODEC\_SupportModuleMicbias* codec capability of module mic bias  
*kCODEC\_SupportModuleMic* codec capability of module mic bias  
*kCODEC\_SupportModuleI2SIn* codec capability of module I2S in  
*kCODEC\_SupportModuleI2SOut* codec capability of module I2S out  
*kCODEC\_SupportModuleMixer* codec capability of module mixer  
*kCODEC\_SupportModuleI2SInSwitchInterface* codec capability of module I2S in switch interface  
  
*kCODEC\_SupportPlayChannelLeft0* codec capability of play channel left 0  
*kCODEC\_SupportPlayChannelRight0* codec capability of play channel right 0  
*kCODEC\_SupportPlayChannelLeft1* codec capability of play channel left 1  
*kCODEC\_SupportPlayChannelRight1* codec capability of play channel right 1  
*kCODEC\_SupportPlayChannelLeft2* codec capability of play channel left 2  
*kCODEC\_SupportPlayChannelRight2* codec capability of play channel right 2  
*kCODEC\_SupportPlayChannelLeft3* codec capability of play channel left 3  
*kCODEC\_SupportPlayChannelRight3* codec capability of play channel right 3  
*kCODEC\_SupportPlaySourcePGA* codec capability of set playback source PGA  
*kCODEC\_SupportPlaySourceInput* codec capability of set playback source INPUT  
*kCODEC\_SupportPlaySourceDAC* codec capability of set playback source DAC  
*kCODEC\_SupportPlaySourceMixerIn* codec capability of set play source Mixer in  
*kCODEC\_SupportPlaySourceMixerInLeft* codec capability of set play source Mixer in left  
*kCODEC\_SupportPlaySourceMixerInRight* codec capability of set play source Mixer in right

***kCODEC\_SupportPlaySourceAux*** codec capability of set play source aux

***kCODEC\_SupportRecordSourceDifferentialLine*** codec capability of record source differential line

***kCODEC\_SupportRecordSourceLineInput*** codec capability of record source line input

***kCODEC\_SupportRecordSourceDifferentialMic*** codec capability of record source differential mic

***kCODEC\_SupportRecordSourceDigitalMic*** codec capability of record digital mic

***kCODEC\_SupportRecordSourceSingleEndMic*** codec capability of single end mic

***kCODEC\_SupportRecordChannelLeft1*** left record channel 1

***kCODEC\_SupportRecordChannelLeft2*** left record channel 2

***kCODEC\_SupportRecordChannelLeft3*** left record channel 3

***kCODEC\_SupportRecordChannelRight1*** right record channel 1

***kCODEC\_SupportRecordChannelRight2*** right record channel 2

***kCODEC\_SupportRecordChannelRight3*** right record channel 3

## 55.2.5 Function Documentation

### 55.2.5.1 status\_t CODEC\_Init ( ***codec\_handle\_t \* handle***, ***codec\_config\_t \* config*** )

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configurations.

Returns

kStatus\_Success is success, else de-initial failed.

### 55.2.5.2 status\_t CODEC\_Deinit ( ***codec\_handle\_t \* handle*** )

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

### 55.2.5.3 status\_t CODEC\_SetFormat ( ***codec\_handle\_t \* handle***, ***uint32\_t mclk***, ***uint32\_t sampleRate***, ***uint32\_t bitWidth*** )

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.2.5.4 status\_t CODEC\_ModuleControl ( *codec\_handle\_t \* handle*, *codec\_module\_ctrl\_cmd\_t cmd*, *uint32\_t data* )

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature.

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

#### 55.2.5.5 status\_t CODEC\_SetVolume ( *codec\_handle\_t \* handle*, *uint32\_t channel*, *uint32\_t volume* )

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of _codec_volume_-capability or _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.2.5.6 status\_t CODEC\_SetMute ( *codec\_handle\_t \* handle*, *uint32\_t channel*, *bool mute* )

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of _codec_volume_-capability or _codec_play_channel.
<i>mute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.2.5.7 status\_t CODEC\_SetPower ( *codec\_handle\_t \* handle*, *codec\_module\_t module*, *bool powerOn* )

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.2.5.8 status\_t CODEC\_SetRecord ( *codec\_handle\_t \* handle*, *uint32\_t recordSource* )

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.2.5.9 status\_t CODEC\_SetRecordChannel ( *codec\_handle\_t \* handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel* )

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

#### 55.2.5.10 status\_t CODEC\_SetPlay ( *codec\_handle\_t \* handle, uint32\_t playSource* )

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

## 55.3 CODEC I2C Driver

### 55.3.1 Overview

The codec common driver provides a codec control abstraction interface.

## Data Structures

- struct `codec_i2c_config_t`  
*CODEC I2C configurations structure. [More...](#)*

## Macros

- #define `CODEC_I2C_MASTER_HANDLER_SIZE` HAL\_I2C\_MASTER\_HANDLE\_SIZE  
*codec i2c handler*

## Enumerations

- enum `codec_reg_addr_t` {
   
`kCODEC_RegAddr8Bit` = 1U,  
`kCODEC_RegAddr16Bit` = 2U }  
*CODEC device register address type.*
- enum `codec_reg_width_t` {
   
`kCODEC_RegWidth8Bit` = 1U,  
`kCODEC_RegWidth16Bit` = 2U,  
`kCODEC_RegWidth32Bit` = 4U }  
*CODEC device register width.*

## Functions

- `status_t CODEC_I2C_Init` (void \*handle, uint32\_t i2cInstance, uint32\_t i2cBaudrate, uint32\_t i2cSourceClockHz)  
*Codec i2c bus initialization.*
- `status_t CODEC_I2C_Deinit` (void \*handle)  
*Codec i2c de-initilization.*
- `status_t CODEC_I2C_Send` (void \*handle, uint8\_t deviceAddress, uint32\_t subAddress, uint8\_t subaddressSize, uint8\_t \*txBuff, uint8\_t txBuffSize)  
*codec i2c send function.*
- `status_t CODEC_I2C_Receive` (void \*handle, uint8\_t deviceAddress, uint32\_t subAddress, uint8\_t subaddressSize, uint8\_t \*rxBuff, uint8\_t rxBuffSize)  
*codec i2c receive function.*

## 55.3.2 Data Structure Documentation

### 55.3.2.1 struct codec\_i2c\_config\_t

#### Data Fields

- `uint32_t codecI2CInstance`  
*i2c bus instance*
- `uint32_t codecI2CSourceClock`  
*i2c bus source clock frequency*

## 55.3.3 Enumeration Type Documentation

### 55.3.3.1 enum codec\_reg\_addr\_t

Enumerator

`kCODEC_RegAddr8Bit` 8-bit register address.  
`kCODEC_RegAddr16Bit` 16-bit register address.

### 55.3.3.2 enum codec\_reg\_width\_t

Enumerator

`kCODEC_RegWidth8Bit` 8-bit register width.  
`kCODEC_RegWidth16Bit` 16-bit register width.  
`kCODEC_RegWidth32Bit` 32-bit register width.

## 55.3.4 Function Documentation

### 55.3.4.1 status\_t CODEC\_I2C\_Init ( void \* handle, uint32\_t i2cInstance, uint32\_t i2cBaudrate, uint32\_t i2cSourceClockHz )

Parameters

<code>handle</code>	i2c master handle.
<code>i2cInstance</code>	instance number of the i2c bus, such as 0 is corresponding to I2C0.

<i>i2cBaudrate</i>	i2c baudrate.
<i>i2cSource-ClockHz</i>	i2c source clock frequency.

Returns

kStatus\_HAL\_I2cSuccess is success, else initial failed.

#### 55.3.4.2 status\_t CODEC\_I2C\_Deinit ( void \* *handle* )

Parameters

<i>handle</i>	i2c master handle.
---------------	--------------------

Returns

kStatus\_HAL\_I2cSuccess is success, else deinitial failed.

#### 55.3.4.3 status\_t CODEC\_I2C\_Send ( void \* *handle*, uint8\_t *deviceAddress*, uint32\_t *subAddress*, uint8\_t *subaddressSize*, uint8\_t \* *txBuff*, uint8\_t *txBuffSize* )

Parameters

<i>handle</i>	i2c master handle.
<i>deviceAddress</i>	codec device address.
<i>subAddress</i>	register address.
<i>subaddressSize</i>	register address width.
<i>txBuff</i>	tx buffer pointer.
<i>txBuffSize</i>	tx buffer size.

Returns

kStatus\_HAL\_I2cSuccess is success, else send failed.

#### 55.3.4.4 status\_t CODEC\_I2C\_Receive ( void \* *handle*, uint8\_t *deviceAddress*, uint32\_t *subAddress*, uint8\_t *subaddressSize*, uint8\_t \* *rxBuff*, uint8\_t *rxBuffSize* )

## Parameters

<i>handle</i>	i2c master handle.
<i>deviceAddress</i>	codec device address.
<i>subAddress</i>	register address.
<i>subaddressSize</i>	register address width.
<i>rxBuff</i>	rx buffer pointer.
<i>rxBuffSize</i>	rx buffer size.

## Returns

kStatus\_HAL\_I2cSuccess is success, else receive failed.

## 55.4 CS42888 Driver

### 55.4.1 Overview

The cs42888 driver provides a codec control interface.

## Data Structures

- struct `cs42888_audio_format_t`  
*cs42888 audio format* [More...](#)
- struct `cs42888_config_t`  
*Initialize structure of CS42888.* [More...](#)
- struct `cs42888_handle_t`  
*cs42888 handler* [More...](#)

## Macros

- #define `CS42888_I2C_HANDLER_SIZE` CODEC\_I2C\_MASTER\_HANDLER\_SIZE  
*CS42888 handle size.*
- #define `CS42888_ID` 0x01U  
*Define the register address of CS42888.*
- #define `CS42888_AOUT_MAX_VOLUME_VALUE` 0xFFU  
*CS42888 volume setting range.*
- #define `CS42888_CACHEREGNUM` 28U  
*Cache register number.*
- #define `CS42888_I2C_ADDR` 0x48U  
*CS42888 I2C address.*
- #define `CS42888_I2C_BITRATE` (100000U)  
*CS42888 I2C baudrate.*

## Typedefs

- typedef void(\* `cs42888_reset` )(bool state)  
*cs42888 reset function pointer*

## Enumerations

- enum `cs42888_func_mode` {
   
`kCS42888_ModeMasterSSM` = 0x0,  
`kCS42888_ModeMasterDSM` = 0x1,  
`kCS42888_ModeMasterQSM` = 0x2,  
`kCS42888_ModeSlave` = 0x3
 }
- CS42888 support modes.*

- enum `cs42888_module_t` {
   
kCS42888\_ModuleDACP1 = 0x2,  
 kCS42888\_ModuleDACP2 = 0x4,  
 kCS42888\_ModuleDACP3 = 0x8,  
 kCS42888\_ModuleDACP4 = 0x10,  
 kCS42888\_ModuleADCP1 = 0x20,  
 kCS42888\_ModuleADCP2 = 0x40 }

*Modules in CS42888 board.*

- enum `cs42888_bus_t` {
   
kCS42888\_BusLeftJustified = 0x0,  
 kCS42888\_BusI2S = 0x1,  
 kCS42888\_BusRightJustified = 0x2,  
 kCS42888\_BusOL1 = 0x4,  
 kCS42888\_BusOL2 = 0x5,  
 kCS42888\_BusTDM = 0x6 }

*CS42888 supported audio bus type.*

- enum {
   
kCS42888\_AOUT1 = 1U,  
 kCS42888\_AOUT2 = 2U,  
 kCS42888\_AOUT3 = 3U,  
 kCS42888\_AOUT4 = 4U,  
 kCS42888\_AOUT5 = 5U,  
 kCS42888\_AOUT6 = 6U,  
 kCS42888\_AOUT7 = 7U,  
 kCS42888\_AOUT8 = 8U }

*CS42888 play channel.*

## Functions

- `status_t CS42888_Init (cs42888_handle_t *handle, cs42888_config_t *config)`  
*CS42888 initialize function.*
- `status_t CS42888_Deinit (cs42888_handle_t *handle)`  
*Deinit the CS42888 codec.*
- `status_t CS42888_SetProtocol (cs42888_handle_t *handle, cs42888_bus_t protocol, uint32_t bitWidth)`  
*Set the audio transfer protocol.*
- `void CS42888_SetFuncMode (cs42888_handle_t *handle, cs42888_func_mode mode)`  
*Set CS42888 to differernt working mode.*
- `status_t CS42888_SelectFunctionalMode (cs42888_handle_t *handle, cs42888_func_mode adcMode, cs42888_func_mode dacMode)`  
*Set CS42888 to differernt functional mode.*
- `status_t CS42888_SetAOUTVolume (cs42888_handle_t *handle, uint8_t channel, uint8_t volume)`  
*Set the volume of different modules in CS42888.*
- `status_t CS42888_SetAINVolume (cs42888_handle_t *handle, uint8_t channel, uint8_t volume)`  
*Set the volume of different modules in CS42888.*
- `uint8_t CS42888_GetAOUTVolume (cs42888_handle_t *handle, uint8_t channel)`

- `uint8_t CS42888_GetAINVolume (cs42888_handle_t *handle, uint8_t channel)`  
*Get the volume of different AIN channel in CS42888.*
- `status_t CS42888_SetMute (cs42888_handle_t *handle, uint8_t channelMask)`  
*Mute modules in CS42888.*
- `status_t CS42888_SetChannelMute (cs42888_handle_t *handle, uint8_t channel, bool isMute)`  
*Mute channel modules in CS42888.*
- `status_t CS42888_SetModule (cs42888_handle_t *handle, cs42888_module_t module, bool isEnabled)`  
*Enable/disable expected devices.*
- `status_t CS42888_ConfigDataFormat (cs42888_handle_t *handle, uint32_t mclk, uint32_t sample_rate, uint32_t bits)`  
*Configure the data format of audio data.*
- `status_t CS42888_WriteReg (cs42888_handle_t *handle, uint8_t reg, uint8_t val)`  
*Write register to CS42888 using I2C.*
- `status_t CS42888_ReadReg (cs42888_handle_t *handle, uint8_t reg, uint8_t *val)`  
*Read register from CS42888 using I2C.*
- `status_t CS42888_ModifyReg (cs42888_handle_t *handle, uint8_t reg, uint8_t mask, uint8_t val)`  
*Modify some bits in the register using I2C.*

## Driver version

- `#define FSL_CS42888_DRIVER_VERSION (MAKE_VERSION(2, 1, 3))`  
*cs42888 driver version 2.1.3.*

### 55.4.2 Data Structure Documentation

#### 55.4.2.1 struct cs42888\_audio\_format\_t

##### Data Fields

- `uint32_t mclk_HZ`  
*master clock frequency*
- `uint32_t sampleRate`  
*sample rate*
- `uint32_t bitWidth`  
*bit width*

#### 55.4.2.2 struct cs42888\_config\_t

##### Data Fields

- `cs42888_bus_t bus`  
*Audio transfer protocol.*
- `cs42888_audio_format_t format`  
*cs42888 audio format*

- `cs42888_func_mode ADCMode`  
*CS42888 ADC function mode.*
- `cs42888_func_mode DACMode`  
*CS42888 DAC function mode.*
- `bool master`  
*true is master, false is slave*
- `codec_i2c_config_t i2cConfig`  
*i2c bus configuration*
- `uint8_t slaveAddress`  
*slave address*
- `cs42888_reset reset`  
*reset function pointer*

## Field Documentation

- (1) `cs42888_func_mode cs42888_config_t::ADCMode`
- (2) `cs42888_func_mode cs42888_config_t::DACMode`

### 55.4.2.3 struct cs42888\_handle\_t

#### Data Fields

- `cs42888_config_t * config`  
*cs42888 config pointer*
- `uint8_t i2cHandle [CS42888_I2C_HANDLER_SIZE]`  
*i2c handle pointer*

### 55.4.3 Macro Definition Documentation

#### 55.4.3.1 #define FSL\_CS42888\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 3))

#### 55.4.3.2 #define CS42888\_ID 0x01U

#### 55.4.3.3 #define CS42888\_I2C\_ADDR 0x48U

### 55.4.4 Enumeration Type Documentation

#### 55.4.4.1 enum cs42888\_func\_mode

Enumerator

- kCS42888\_ModeMasterSSM* master single speed mode
- kCS42888\_ModeMasterDSM* master dual speed mode
- kCS42888\_ModeMasterQSM* master quad speed mode
- kCS42888\_ModeSlave* master single speed mode

#### 55.4.4.2 enum cs42888\_module\_t

Enumerator

- kCS42888\_ModuleDACPair1* DAC pair1 (AOUT1 and AOUT2) module in CS42888.
- kCS42888\_ModuleDACPair2* DAC pair2 (AOUT3 and AOUT4) module in CS42888.
- kCS42888\_ModuleDACPair3* DAC pair3 (AOUT5 and AOUT6) module in CS42888.
- kCS42888\_ModuleDACPair4* DAC pair4 (AOUT7 and AOUT8) module in CS42888.
- kCS42888\_ModuleADCPair1* ADC pair1 (AIN1 and AIN2) module in CS42888.
- kCS42888\_ModuleADCPair2* ADC pair2 (AIN3 and AIN4) module in CS42888.

#### 55.4.4.3 enum cs42888\_bus\_t

Enumerator

- kCS42888\_BusLeftJustified* Left justified format, up to 24 bits.
- kCS42888\_BusI2S* I2S format, up to 24 bits.
- kCS42888\_BusRightJustified* Right justified, can support 16bits and 24 bits.
- kCS42888\_BusOL1* One-Line #1 mode.
- kCS42888\_BusOL2* One-Line #2 mode.
- kCS42888\_BusTDM* TDM mode.

#### 55.4.4.4 anonymous enum

Enumerator

- kCS42888\_AOUT1* aout1
- kCS42888\_AOUT2* aout2
- kCS42888\_AOUT3* aout3
- kCS42888\_AOUT4* aout4
- kCS42888\_AOUT5* aout5
- kCS42888\_AOUT6* aout6
- kCS42888\_AOUT7* aout7
- kCS42888\_AOUT8* aout8

### 55.4.5 Function Documentation

#### 55.4.5.1 status\_t CS42888\_Init ( *cs42888\_handle\_t \* handle*, *cs42888\_config\_t \* config* )

The second parameter is NULL to CS42888 in this version. If users want to change the settings, they have to use *cs42888\_write\_reg()* or *cs42888\_modify\_reg()* to set the register value of CS42888. Note: If the *codec\_config* is NULL, it would initialize CS42888 using default settings. The default setting: *codec\_config->bus* = *kCS42888\_BusI2S* *codec\_config->ADCmode* = *kCS42888\_ModeSlave* *codec\_config->DACmode* = *kCS42888\_ModeSlave*

Parameters

<i>handle</i>	CS42888 handle structure.
<i>config</i>	CS42888 configuration structure.

#### 55.4.5.2 status\_t CS42888\_Deinit ( cs42888\_handle\_t \* *handle* )

This function close all modules in CS42888 to save power.

Parameters

<i>handle</i>	CS42888 handle structure pointer.
---------------	-----------------------------------

#### 55.4.5.3 status\_t CS42888\_SetProtocol ( cs42888\_handle\_t \* *handle*, cs42888\_bus\_t *protocol*, uint32\_t *bitWidth* )

CS42888 only supports I2S, left justified, right justified, PCM A, PCM B format.

Parameters

<i>handle</i>	CS42888 handle structure.
<i>protocol</i>	Audio data transfer protocol.
<i>bitWidth</i>	bit width

#### 55.4.5.4 void CS42888\_SetFuncMode ( cs42888\_handle\_t \* *handle*, cs42888\_func\_mode *mode* )

**Deprecated** api, Do not use it anymore. It has been superceded by [CS42888\\_SelectFunctionalMode](#).

Parameters

<i>handle</i>	CS42888 handle structure.
<i>mode</i>	differenht working mode of CS42888.

#### 55.4.5.5 status\_t CS42888\_SelectFunctionalMode ( cs42888\_handle\_t \* *handle*, cs42888\_func\_mode *adcMode*, cs42888\_func\_mode *dacMode* )

Parameters

<i>handle</i>	CS42888 handle structure.
<i>adcMode</i>	differenht working mode of CS42888.
<i>dacMode</i>	differenht working mode of CS42888.

#### 55.4.5.6 status\_t CS42888\_SetAOUTVolume ( *cs42888\_handle\_t \* handle, uint8\_t channel, uint8\_t volume* )

This function would set the volume of CS42888 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	CS42888 handle structure.
<i>channel</i>	AOUT channel, it shall be 1~8.
<i>volume</i>	Volume value need to be set.

#### 55.4.5.7 status\_t CS42888\_SetAINVolume ( *cs42888\_handle\_t \* handle, uint8\_t channel, uint8\_t volume* )

This function would set the volume of CS42888 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	CS42888 handle structure.
<i>channel</i>	AIN channel, it shall be 1~4.
<i>volume</i>	Volume value need to be set.

#### 55.4.5.8 uint8\_t CS42888\_GetAOUTVolume ( *cs42888\_handle\_t \* handle, uint8\_t channel* )

This function gets the volume of CS42888 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	CS42888 handle structure.
<i>channel</i>	AOUT channel, it shall be 1~8.

#### 55.4.5.9 `uint8_t CS42888_GetAINVolume ( cs42888_handle_t * handle, uint8_t channel )`

This function gets the volume of CS42888 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	CS42888 handle structure.
<i>channel</i>	AIN channel, it shall be 1~4.

#### 55.4.5.10 `status_t CS42888_SetMute ( cs42888_handle_t * handle, uint8_t channelMask )`

Parameters

<i>handle</i>	CS42888 handle structure.
<i>channelMask</i>	Channel mask for mute. Mute channel 0, it shall be 0x1, while mute channel 0 and 1, it shall be 0x3. Mute all channel, it shall be 0xFF. Each bit represent one channel, 1 means mute, 0 means unmute.

#### 55.4.5.11 `status_t CS42888_SetChannelMute ( cs42888_handle_t * handle, uint8_t channel, bool isMute )`

Parameters

<i>handle</i>	CS42888 handle structure.
<i>channel</i>	reference _cs42888_play_channel.
<i>isMute</i>	true is mute, falase is unmute.

#### 55.4.5.12 `status_t CS42888_SetModule ( cs42888_handle_t * handle, cs42888_module_t module, bool isEnabled )`

Parameters

<i>handle</i>	CS42888 handle structure.
<i>module</i>	Module expected to enable.
<i>isEnabled</i>	Enable or disable moudles.

#### 55.4.5.13 status\_t CS42888\_ConfigDataFormat ( *cs42888\_handle\_t \* handle, uint32\_t mclk, uint32\_t sample\_rate, uint32\_t bits* )

This function would configure the registers about the sample rate, bit depths.

Parameters

<i>handle</i>	CS42888 handle structure pointer.
<i>mclk</i>	Master clock frequency of I2S.
<i>sample_rate</i>	Sample rate of audio file running in CS42888. CS42888 now supports 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k and 96k sample rate.
<i>bits</i>	Bit depth of audio file (CS42888 only supports 16bit, 20bit, 24bit and 32 bit in HW).

#### 55.4.5.14 status\_t CS42888\_WriteReg ( *cs42888\_handle\_t \* handle, uint8\_t reg, uint8\_t val* )

Parameters

<i>handle</i>	CS42888 handle structure.
<i>reg</i>	The register address in CS42888.
<i>val</i>	Value needs to write into the register.

#### 55.4.5.15 status\_t CS42888\_ReadReg ( *cs42888\_handle\_t \* handle, uint8\_t reg, uint8\_t \* val* )

Parameters

<i>handle</i>	CS42888 handle structure.
<i>reg</i>	The register address in CS42888.
<i>val</i>	Value written to.

#### 55.4.5.16 status\_t CS42888\_ModifyReg ( *cs42888\_handle\_t \* handle, uint8\_t reg, uint8\_t mask, uint8\_t val* )

Parameters

<i>handle</i>	CS42888 handle structure.
<i>reg</i>	The register address in CS42888.
<i>mask</i>	The mask code for the bits want to write. The bit you want to write should be 0.
<i>val</i>	Value needs to write into the register.

## 55.4.6 CS42888 Adapter

### 55.4.6.1 Overview

The cs42888 adapter provides a codec unify control interface.

#### Macros

- `#define HAL_CODEC_CS42888_HANDLER_SIZE (CS42888_I2C_HANDLER_SIZE + 4)`  
*codec handler size*

#### Functions

- `status_t HAL_CODEC_CS42888_Init (void *handle, void *config)`  
*Codec initialization.*
- `status_t HAL_CODEC_CS42888_Deinit (void *handle)`  
*Codec de-initilization.*
- `status_t HAL_CODEC_CS42888_SetFormat (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`  
*set audio data format.*
- `status_t HAL_CODEC_CS42888_SetVolume (void *handle, uint32_t playChannel, uint32_t volume)`  
*set audio codec module volume.*
- `status_t HAL_CODEC_CS42888_SetMute (void *handle, uint32_t playChannel, bool isMute)`  
*set audio codec module mute.*
- `status_t HAL_CODEC_CS42888_SetPower (void *handle, uint32_t module, bool powerOn)`  
*set audio codec module power.*
- `status_t HAL_CODEC_CS42888_SetRecord (void *handle, uint32_t recordSource)`  
*codec set record source.*
- `status_t HAL_CODEC_CS42888_SetRecordChannel (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)`  
*codec set record channel.*
- `status_t HAL_CODEC_CS42888_SetPlay (void *handle, uint32_t playSource)`  
*codec set play source.*
- `status_t HAL_CODEC_CS42888_ModuleControl (void *handle, uint32_t cmd, uint32_t data)`  
*codec module control.*
- `static status_t HAL_CODEC_Init (void *handle, void *config)`  
*Codec initilization.*
- `static status_t HAL_CODEC_Deinit (void *handle)`  
*Codec de-initilization.*
- `static status_t HAL_CODEC_SetFormat (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`  
*set audio data format.*
- `static status_t HAL_CODEC_SetVolume (void *handle, uint32_t playChannel, uint32_t volume)`  
*set audio codec module volume.*
- `static status_t HAL_CODEC_SetMute (void *handle, uint32_t playChannel, bool isMute)`  
*set audio codec module mute.*
- `static status_t HAL_CODEC_SetPower (void *handle, uint32_t module, bool powerOn)`

- static `status_t HAL_CODEC_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- static `status_t HAL_CODEC_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- static `status_t HAL_CODEC_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- static `status_t HAL_CODEC_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*

### 55.4.6.2 Function Documentation

#### 55.4.6.2.1 `status_t HAL_CODEC_CS42888_Init( void * handle, void * config )`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

#### 55.4.6.2.2 `status_t HAL_CODEC_CS42888_Deinit( void * handle )`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

#### 55.4.6.2.3 `status_t HAL_CODEC_CS42888_SetFormat( void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth )`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.4 status\_t HAL\_CODEC\_CS42888\_SetVolume ( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.5 status\_t HAL\_CODEC\_CS42888\_SetMute ( void \* *handle*, uint32\_t *playChannel*, bool *isMute* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.6 status\_t HAL\_CODEC\_CS42888\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* )

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.7 status\_t HAL\_CODEC\_CS42888\_SetRecord ( void \* *handle*, uint32\_t *recordSource* )

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.8 status\_t HAL\_CODEC\_CS42888\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* )

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.9 status\_t HAL\_CODEC\_CS42888\_SetPlay ( void \* *handle*, uint32\_t *playSource* )

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.10 **status\_t HAL\_CODEC\_CS42888\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* )**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.11 **static status\_t HAL\_CODEC\_Init ( void \* *handle*, void \* *config* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

#### 55.4.6.2.12 **static status\_t HAL\_CODEC\_Deinit ( void \* *handle* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

#### 55.4.6.2.13 static status\_t HAL\_CODEC\_SetFormat( void \* *handle*, uint32\_t *mclk*, uint32\_t *sampleRate*, uint32\_t *bitWidth* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.14 static status\_t HAL\_CODEC\_SetVolume( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.15 static status\_t HAL\_CODEC\_SetMute( void \* *handle*, uint32\_t *playChannel*, bool *isMute* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.16 static status\_t HAL\_CODEC\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.17 static status\_t HAL\_CODEC\_SetRecord ( void \* *handle*, uint32\_t *recordSource* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.4.6.2.18 static status\_t HAL\_CODEC\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

**55.4.6.2.19 static status\_t HAL\_CODEC\_SetPlay ( void \* *handle*, uint32\_t *playSource* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

**55.4.6.2.20 static status\_t HAL\_CODEC\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* ) [inline], [static]**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

## 55.5 DA7212 Driver

### 55.5.1 Overview

The da7212 driver provides a codec control interface.

## Data Structures

- struct `da7212_pll_config_t`  
`da7212 pll configuration` *More...*
- struct `da7212_audio_format_t`  
`da7212 audio format` *More...*
- struct `da7212_config_t`  
`DA7212 configure structure.` *More...*
- struct `da7212_handle_t`  
`da7212 codec handler` *More...*

## Macros

- `#define DA7212_I2C_HANDLER_SIZE CODEC_I2C_MASTER_HANDLER_SIZE`  
`da7212 handle size`
- `#define DA7212_ADDRESS (0x1A)`  
`DA7212 I2C address.`
- `#define DA7212_HEADPHONE_MAX_VOLUME_VALUE 0x3FU`  
`da7212 volume setting range`

## Enumerations

- enum `da7212_Input_t` {
   
`kDA7212_Input_AUX` = 0x0,  
`kDA7212_Input_MIC1_Dig`,  
`kDA7212_Input_MIC1_An`,  
`kDA7212_Input_MIC2` }  
`DA7212 input source select.`
- enum `_da7212_play_channel` {
   
`kDA7212_HeadphoneLeft` = 1U,  
`kDA7212_HeadphoneRight` = 2U,  
`kDA7212_Speaker` = 4U }  
`da7212 play channel`
- enum `da7212_Output_t` {
   
`kDA7212_Output_HP` = 0x0,  
`kDA7212_Output_SP` }  
`DA7212 output device select.`

- enum \_da7212\_module {
 kDA7212\_ModuleADC,
 kDA7212\_ModuleDAC,
 kDA7212\_ModuleHeadphone,
 kDA7212\_ModuleSpeaker }
   
*DA7212 module.*
- enum da7212\_dac\_source\_t {
 kDA7212\_DACSourceADC = 0x0U,
 kDA7212\_DACSourceInputStream = 0x3U }
   
*DA7212 functionality.*
- enum da7212\_volume\_t {
 kDA7212\_DACGainMute = 0x7,
 kDA7212\_DACGainM72DB = 0x17,
 kDA7212\_DACGainM60DB = 0x1F,
 kDA7212\_DACGainM54DB = 0x27,
 kDA7212\_DACGainM48DB = 0x2F,
 kDA7212\_DACGainM42DB = 0x37,
 kDA7212\_DACGainM36DB = 0x3F,
 kDA7212\_DACGainM30DB = 0x47,
 kDA7212\_DACGainM24DB = 0x4F,
 kDA7212\_DACGainM18DB = 0x57,
 kDA7212\_DACGainM12DB = 0x5F,
 kDA7212\_DACGainM6DB = 0x67,
 kDA7212\_DACGain0DB = 0x6F,
 kDA7212\_DACGain6DB = 0x77,
 kDA7212\_DACGain12DB = 0x7F }
   
*DA7212 volume.*
- enum da7212\_protocol\_t {
 kDA7212\_BusI2S = 0x0,
 kDA7212\_BusLeftJustified,
 kDA7212\_BusRightJustified,
 kDA7212\_BusDSPMode }
   
*The audio data transfer protocol choice.*
- enum da7212\_sys\_clk\_source\_t {
 kDA7212\_SysClkSourceMCLK = 0U,
 kDA7212\_SysClkSourcePLL = 1U << 14 }
   
*da7212 system clock source*
- enum da7212\_pll\_clk\_source\_t { kDA7212\_PLLClkSourceMCLK = 0U }
   
*DA7212 pll clock source.*
- enum da7212\_pll\_out\_clk\_t {
 kDA7212\_PLLOutputClk11289600 = 11289600U,
 kDA7212\_PLLOutputClk12288000 = 12288000U }
   
*DA7212 output clock frequency.*
- enum da7212\_master\_bits\_t {

```

kDA7212_MasterBits32PerFrame = 0U,
kDA7212_MasterBits64PerFrame = 1U,
kDA7212_MasterBits128PerFrame = 2U,
kDA7212_MasterBits256PerFrame = 3U }
    master mode bits per frame

```

## Functions

- `status_t DA7212_Init (da7212_handle_t *handle, da7212_config_t *codecConfig)`  
*DA7212 initialize function.*
- `status_t DA7212_ConfigAudioFormat (da7212_handle_t *handle, uint32_t masterClock_Hz, uint32_t sampleRate_Hz, uint32_t dataBits)`  
*Set DA7212 audio format.*
- `status_t DA7212_SetPLLConfig (da7212_handle_t *handle, da7212_pll_config_t *config)`  
*DA7212 set PLL configuration This function will enable the GPIO1 FLL clock output function, so user can see the generated fll output clock frequency from WM8904 GPIO1.*
- `void DA7212_ChangeHPVolume (da7212_handle_t *handle, da7212_volume_t volume)`  
*Set DA7212 playback volume.*
- `void DA7212_Mute (da7212_handle_t *handle, bool isMuted)`  
*Mute or unmute DA7212.*
- `void DA7212_ChangeInput (da7212_handle_t *handle, da7212_Input_t DA7212_Input)`  
*Set the input data source of DA7212.*
- `void DA7212_ChangeOutput (da7212_handle_t *handle, da7212_Output_t DA7212_Output)`  
*Set the output device of DA7212.*
- `status_t DA7212_SetChannelVolume (da7212_handle_t *handle, uint32_t channel, uint32_t volume)`  
*Set module volume.*
- `status_t DA7212_SetChannelMute (da7212_handle_t *handle, uint32_t channel, bool isMute)`  
*Set module mute.*
- `status_t DA7212_SetProtocol (da7212_handle_t *handle, da7212_protocol_t protocol)`  
*Set protocol for DA7212.*
- `status_t DA7212_SetMasterModeBits (da7212_handle_t *handle, uint32_t bitWidth)`  
*Set master mode bits per frame for DA7212.*
- `status_t DA7212_WriteRegister (da7212_handle_t *handle, uint8_t u8Register, uint8_t u8RegisterData)`  
*Write a register for DA7212.*
- `status_t DA7212_ReadRegister (da7212_handle_t *handle, uint8_t u8Register, uint8_t *pu8RegisterData)`  
*Get a register value of DA7212.*
- `status_t DA7212_Deinit (da7212_handle_t *handle)`  
*Deinit DA7212.*

## Driver version

- `#define FSL_DA7212_DRIVER_VERSION (MAKE_VERSION(2, 2, 3))`  
*CLOCK driver version 2.2.3.*

## 55.5.2 Data Structure Documentation

### 55.5.2.1 struct da7212\_pll\_config\_t

#### Data Fields

- `da7212_pll_clk_source_t source`  
*pll reference clock source*
- `uint32_t refClock_HZ`  
*pll reference clock frequency*
- `da7212_pll_out_clk_t outputClock_HZ`  
*pll output clock frequency*

### 55.5.2.2 struct da7212\_audio\_format\_t

#### Data Fields

- `uint32_t mclk_HZ`  
*master clock frequency*
- `uint32_t sampleRate`  
*sample rate*
- `uint32_t bitWidth`  
*bit width*
- `bool isBclkInvert`  
*bit clock invertet*

### 55.5.2.3 struct da7212\_config\_t

#### Data Fields

- `bool isMaster`  
*If DA7212 is master, true means master, false means slave.*
- `da7212_protocol_t protocol`  
*Audio bus format, can be I2S, LJ, RJ or DSP mode.*
- `da7212_dac_source_t dacSource`  
*DA7212 data source.*
- `da7212_audio_format_t format`  
*audio format*
- `uint8_t slaveAddress`  
*device address*
- `codec_i2c_config_t i2cConfig`  
*i2c configuration*
- `da7212_sys_clk_source_t sysClkSource`  
*system clock source*
- `da7212_pll_config_t * pll`  
*pll configuration*

## Field Documentation

- (1) `bool da7212_config_t::isMaster`
- (2) `da7212_protocol_t da7212_config_t::protocol`
- (3) `da7212_dac_source_t da7212_config_t::dacSource`

### 55.5.2.4 struct da7212\_handle\_t

#### Data Fields

- `da7212_config_t * config`  
*da7212 config pointer*
- `uint8_t i2cHandle [DA7212_I2C_HANDLER_SIZE]`  
*i2c handle*

### 55.5.3 Macro Definition Documentation

#### 55.5.3.1 #define FSL\_DA7212\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 3))

### 55.5.4 Enumeration Type Documentation

#### 55.5.4.1 enum da7212\_Input\_t

Enumerator

- kDA7212\_Input\_AUX* Input from AUX.
- kDA7212\_Input\_MIC1\_Dig* Input from MIC1 Digital.
- kDA7212\_Input\_MIC1\_An* Input from Mic1 Analog.
- kDA7212\_Input\_MIC2* Input from MIC2.

#### 55.5.4.2 enum \_da7212\_play\_channel

Enumerator

- kDA7212\_HeadphoneLeft* headphone left
- kDA7212\_HeadphoneRight* headphone right
- kDA7212\_Speaker* speaker channel

#### 55.5.4.3 enum da7212\_Output\_t

Enumerator

- kDA7212\_Output\_HP* Output to headphone.

*kDA7212\_Output\_SP* Output to speaker.

#### 55.5.4.4 enum \_da7212\_module

Enumerator

*kDA7212\_ModuleADC* module ADC  
*kDA7212\_ModuleDAC* module DAC  
*kDA7212\_ModuleHeadphone* module headphone  
*kDA7212\_ModuleSpeaker* module speaker

#### 55.5.4.5 enum da7212\_dac\_source\_t

Enumerator

*kDA7212\_DACSourceADC* DAC source from ADC.  
*kDA7212\_DACSourceInputStream* DAC source from.

#### 55.5.4.6 enum da7212\_volume\_t

Enumerator

*kDA7212\_DACGainMute* Mute DAC.  
*kDA7212\_DACGainM72DB* DAC volume -72db.  
*kDA7212\_DACGainM60DB* DAC volume -60db.  
*kDA7212\_DACGainM54DB* DAC volume -54db.  
*kDA7212\_DACGainM48DB* DAC volume -48db.  
*kDA7212\_DACGainM42DB* DAC volume -42db.  
*kDA7212\_DACGainM36DB* DAC volume -36db.  
*kDA7212\_DACGainM30DB* DAC volume -30db.  
*kDA7212\_DACGainM24DB* DAC volume -24db.  
*kDA7212\_DACGainM18DB* DAC volume -18db.  
*kDA7212\_DACGainM12DB* DAC volume -12db.  
*kDA7212\_DACGainM6DB* DAC volume -6db.  
*kDA7212\_DACGain0DB* DAC volume +0db.  
*kDA7212\_DACGain6DB* DAC volume +6db.  
*kDA7212\_DACGain12DB* DAC volume +12db.

#### 55.5.4.7 enum da7212\_protocol\_t

Enumerator

*kDA7212\_BusI2S* I2S Type.

*kDA7212\_BusLeftJustified* Left justified.  
*kDA7212\_BusRightJustified* Right Justified.  
*kDA7212\_BusDSPMode* DSP mode.

#### 55.5.4.8 enum da7212\_sys\_clk\_source\_t

Enumerator

*kDA7212\_SysClkSourceMCLK* da7212 system clock soure from MCLK  
*kDA7212\_SysClkSourcePLL* da7212 system clock soure from pLL

#### 55.5.4.9 enum da7212\_pll\_clk\_source\_t

Enumerator

*kDA7212\_PLLClkSourceMCLK* DA7212 PLL clock source from MCLK.

#### 55.5.4.10 enum da7212\_pll\_out\_clk\_t

Enumerator

*kDA7212\_PLLOutputClk11289600* output 112896000U  
*kDA7212\_PLLOutputClk12288000* output 12288000U

#### 55.5.4.11 enum da7212\_master\_bits\_t

Enumerator

*kDA7212\_MasterBits32PerFrame* master mode bits32 per frame  
*kDA7212\_MasterBits64PerFrame* master mode bits64 per frame  
*kDA7212\_MasterBits128PerFrame* master mode bits128 per frame  
*kDA7212\_MasterBits256PerFrame* master mode bits256 per frame

### 55.5.5 Function Documentation

#### 55.5.5.1 status\_t DA7212\_Init ( da7212\_handle\_t \* handle, da7212\_config\_t \* codecConfig )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>codecConfig</i>	<p>Codec configure structure. This parameter can be NULL, if NULL, set as default settings. The default setting:</p> <pre>* sgtl_init_t codec_config * codec_config.route = kDA7212_RoutePlayback * codec_config.bus = kDA7212_BusI2S * codec_config.isMaster = false *</pre>

#### 55.5.5.2 status\_t DA7212\_ConfigAudioFormat ( *da7212\_handle\_t \* handle, uint32\_t masterClock\_Hz, uint32\_t sampleRate\_Hz, uint32\_t dataBits* )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>masterClock_Hz</i>	Master clock frequency in Hz. If DA7212 is slave, use the frequency of master, if DA7212 as master, it should be 1228000 while sample rate frequency is 8k/12K/16-K/24K/32K/48K/96K, 11289600 whie sample rate is 11.025K/22.05K/44.1K
<i>sampleRate_Hz</i>	Sample rate frequency in Hz.
<i>dataBits</i>	How many bits in a word of a audio frame, DA7212 only supports 16/20/24/32 bits.

#### 55.5.5.3 status\_t DA7212\_SetPLLConfig ( *da7212\_handle\_t \* handle, da7212\_pll\_config\_t \* config* )

Parameters

<i>handle</i>	DA7212 handler pointer.
<i>config</i>	PLL configuration pointer.

#### 55.5.5.4 void DA7212\_ChangeHPVolume ( *da7212\_handle\_t \* handle, da7212\_volume\_t volume* )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>volume</i>	The volume of playback.

#### 55.5.5.5 void DA7212\_Mute ( *da7212\_handle\_t \* handle, bool isMuted* )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>isMuted</i>	True means mute, false means unmute.

#### 55.5.5.6 void DA7212\_ChangeInput ( *da7212\_handle\_t \* handle, da7212\_Input\_t DA7212\_Input* )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>DA7212_Input</i>	Input data source.

#### 55.5.5.7 void DA7212\_ChangeOutput ( *da7212\_handle\_t \* handle, da7212\_Output\_t DA7212\_Output* )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>DA7212_Output</i>	Output device of DA7212.

#### 55.5.5.8 status\_t DA7212\_SetChannelVolume ( *da7212\_handle\_t \* handle, uint32\_t channel, uint32\_t volume* )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>channel</i>	shoule be a value of _da7212_channel.
<i>volume</i>	volume range 0 - 0x3F mapped to range -57dB - 6dB.

**55.5.5.9 status\_t DA7212\_SetChannelMute ( da7212\_handle\_t \* *handle*, uint32\_t *channel*, bool *isMute* )**

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>channel</i>	shoule be a value of _da7212_channel.
<i>isMute</i>	true is mute, false is unmute.

**55.5.5.10 status\_t DA7212\_SetProtocol ( da7212\_handle\_t \* *handle*, da7212\_protocol\_t *protocol* )**

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>protocol</i>	da7212_protocol_t.

**55.5.5.11 status\_t DA7212\_SetMasterModeBits ( da7212\_handle\_t \* *handle*, uint32\_t *bitWidth* )**

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>bitWidth</i>	audio data bitwidth.

**55.5.5.12 status\_t DA7212\_WriteRegister ( da7212\_handle\_t \* *handle*, uint8\_t *u8Register*, uint8\_t *u8RegisterData* )**

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>u8Register</i>	DA7212 register address to be written.
<i>u8RegisterData</i>	Data to be written into register

#### 55.5.5.13 status\_t DA7212\_ReadRegister ( da7212\_handle\_t \* *handle*, uint8\_t *u8Register*, uint8\_t \* *pu8RegisterData* )

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>u8Register</i>	DA7212 register address to be read.
<i>pu8RegisterData</i>	Pointer where the read out value to be stored.

#### 55.5.5.14 status\_t DA7212\_Deinit ( da7212\_handle\_t \* *handle* )

Parameters

<i>handle</i>	DA7212 handle pointer.
---------------	------------------------

## 55.5.6 DA7212 Adapter

### 55.5.6.1 Overview

The da7212 adapter provides a codec unify control interface.

#### Macros

- #define `HAL_CODEC_DA7212_HANDLER_SIZE` (`DA7212_I2C_HANDLER_SIZE + 4`)  
*codec handler size*

#### Functions

- `status_t HAL_CODEC_DA7212_Init` (void \*handle, void \*config)  
*Codec initialization.*
- `status_t HAL_CODEC_DA7212_Deinit` (void \*handle)  
*Codec de-initilization.*
- `status_t HAL_CODEC_DA7212_SetFormat` (void \*handle, uint32\_t mclk, uint32\_t sampleRate, uint32\_t bitWidth)  
*set audio data format.*
- `status_t HAL_CODEC_DA7212_SetVolume` (void \*handle, uint32\_t playChannel, uint32\_t volume)  
*set audio codec module volume.*
- `status_t HAL_CODEC_DA7212_SetMute` (void \*handle, uint32\_t playChannel, bool isMute)  
*set audio codec module mute.*
- `status_t HAL_CODEC_DA7212_SetPower` (void \*handle, uint32\_t module, bool powerOn)  
*set audio codec module power.*
- `status_t HAL_CODEC_DA7212_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- `status_t HAL_CODEC_DA7212_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- `status_t HAL_CODEC_DA7212_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- `status_t HAL_CODEC_DA7212_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*
- static `status_t HAL_CODEC_Init` (void \*handle, void \*config)  
*Codec initilization.*
- static `status_t HAL_CODEC_Deinit` (void \*handle)  
*Codec de-initilization.*
- static `status_t HAL_CODEC_SetFormat` (void \*handle, uint32\_t mclk, uint32\_t sampleRate, uint32\_t bitWidth)  
*set audio data format.*
- static `status_t HAL_CODEC_SetVolume` (void \*handle, uint32\_t playChannel, uint32\_t volume)  
*set audio codec module volume.*
- static `status_t HAL_CODEC_SetMute` (void \*handle, uint32\_t playChannel, bool isMute)  
*set audio codec module mute.*
- static `status_t HAL_CODEC_SetPower` (void \*handle, uint32\_t module, bool powerOn)

- static `status_t HAL_CODEC_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- static `status_t HAL_CODEC_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- static `status_t HAL_CODEC_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- static `status_t HAL_CODEC_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*

## 55.5.6.2 Function Documentation

### 55.5.6.2.1 `status_t HAL_CODEC_DA7212_Init( void * handle, void * config )`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

### 55.5.6.2.2 `status_t HAL_CODEC_DA7212_Deinit( void * handle )`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

### 55.5.6.2.3 `status_t HAL_CODEC_DA7212_SetFormat( void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth )`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.4 status\_t HAL\_CODEC\_DA7212\_SetVolume ( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.5 status\_t HAL\_CODEC\_DA7212\_SetMute ( void \* *handle*, uint32\_t *playChannel*, bool *isMute* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.6 status\_t HAL\_CODEC\_DA7212\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* )

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.7 status\_t HAL\_CODEC\_DA7212\_SetRecord ( void \* *handle*, uint32\_t *recordSource* )

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.8 status\_t HAL\_CODEC\_DA7212\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* )

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.9 status\_t HAL\_CODEC\_DA7212\_SetPlay ( void \* *handle*, uint32\_t *playSource* )

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.10 status\_t HAL\_CODEC\_DA7212\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* )

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.11 static status\_t HAL\_CODEC\_Init ( void \* *handle*, void \* *config* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

#### 55.5.6.2.12 static status\_t HAL\_CODEC\_Deinit ( void \* *handle* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

#### 55.5.6.2.13 static status\_t HAL\_CODEC\_SetFormat( void \* *handle*, uint32\_t *mclk*, uint32\_t *sampleRate*, uint32\_t *bitWidth* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.14 static status\_t HAL\_CODEC\_SetVolume( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.15 static status\_t HAL\_CODEC\_SetMute( void \* *handle*, uint32\_t *playChannel*, bool *isMute* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.16 static status\_t HAL\_CODEC\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.17 static status\_t HAL\_CODEC\_SetRecord ( void \* *handle*, uint32\_t *recordSource* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.5.6.2.18 static status\_t HAL\_CODEC\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

**55.5.6.2.19 static status\_t HAL\_CODEC\_SetPlay ( void \* *handle*, uint32\_t *playSource* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

**55.5.6.2.20 static status\_t HAL\_CODEC\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* ) [inline], [static]**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

## 55.6 SGTL5000 Driver

### 55.6.1 Overview

The sgtl5000 driver provides a codec control interface.

## Data Structures

- struct `sgtl_audio_format_t`  
*Audio format configuration. [More...](#)*
- struct `sgtl_config_t`  
*Initialize structure of sgtl5000. [More...](#)*
- struct `sgtl_handle_t`  
*SGTL codec handler. [More...](#)*

## Macros

- #define `CHIP_ID` 0x0000U  
*Define the register address of sgtl5000.*
- #define `SGTL5000_HEADPHONE_MAX_VOLUME_VALUE` 0x7FU  
*SGTL5000 volume setting range.*
- #define `SGTL5000_I2C_ADDR` 0x0A  
*SGTL5000 I2C address.*
- #define `SGTL_I2C_HANDLER_SIZE` CODEC\_I2C\_MASTER\_HANDLER\_SIZE  
*sgtl handle size*
- #define `SGTL_I2C_BITRATE` 100000U  
*sgtl i2c baudrate*

## Enumerations

- enum `sgtl_module_t` {
   
`kSGTL_ModuleADC` = 0x0,  
`kSGTL_ModuleDAC`,  
`kSGTL_ModuleDAP`,  
`kSGTL_ModuleHP`,  
`kSGTL_ModuleI2SIN`,  
`kSGTL_ModuleI2SOUT`,  
`kSGTL_ModuleLineIn`,  
`kSGTL_ModuleLineOut`,  
`kSGTL_ModuleMicin` }
- Modules in Sgtl5000 board.
- enum `sgtl_route_t` {

```

kSGTL_RouteBypass = 0x0,
kSGTL_RoutePlayback,
kSGTL_RoutePlaybackandRecord,
kSGTL_RoutePlaybackwithDAP,
kSGTL_RoutePlaybackwithDAPandRecord,
kSGTL_RouteRecord }

Sgtl5000 data route.
• enum sgtl_protocol_t {
    kSGTL_BusI2S = 0x0,
    kSGTL_BusLeftJustified,
    kSGTL_BusRightJustified,
    kSGTL_BusPCMA,
    kSGTL_BusPCMB }

The audio data transfer protocol choice.
• enum {
    kSGTL_HeadphoneLeft = 0,
    kSGTL_HeadphoneRight = 1,
    kSGTL_LineoutLeft = 2,
    kSGTL_LineoutRight = 3 }

sgtl play channel
• enum {
    kSGTL_RecordSourceLineIn = 0U,
    kSGTL_RecordSourceMic = 1U }

sgtl record source _sgtl_record_source
• enum {
    kSGTL_PlaySourceLineIn = 0U,
    kSGTL_PlaySourceDAC = 1U }

sgtl play source _stgl_play_source
• enum sgtl_sclk_edge_t {
    kSGTL_SclkValidEdgeRising = 0U,
    kSGTL_SclkValidEdgeFailling = 1U }

SGTL SCLK valid edge.

```

## Functions

- `status_t SGTL_Init (sgtl_handle_t *handle, sgtl_config_t *config)`  
*sgtl5000 initialize function.*
- `status_t SGTL_SetDataRoute (sgtl_handle_t *handle, sgtl_route_t route)`  
*Set audio data route in sgtl5000.*
- `status_t SGTL_SetProtocol (sgtl_handle_t *handle, sgtl_protocol_t protocol)`  
*Set the audio transfer protocol.*
- `void SGTL_SetMasterSlave (sgtl_handle_t *handle, bool master)`  
*Set sgtl5000 as master or slave.*
- `status_t SGTL_SetVolume (sgtl_handle_t *handle, sgtl_module_t module, uint32_t volume)`  
*Set the volume of different modules in sgtl5000.*
- `uint32_t SGTL_GetVolume (sgtl_handle_t *handle, sgtl_module_t module)`  
*Get the volume of different modules in sgtl5000.*

- `status_t SGTL_SetMute (sgtl_handle_t *handle, sgtl_module_t module, bool mute)`  
*Mute/unmute modules in sgtl5000.*
- `status_t SGTL_EnableModule (sgtl_handle_t *handle, sgtl_module_t module)`  
*Enable expected devices.*
- `status_t SGTL_DisableModule (sgtl_handle_t *handle, sgtl_module_t module)`  
*Disable expected devices.*
- `status_t SGTL_Deinit (sgtl_handle_t *handle)`  
*Deinit the sgtl5000 codec.*
- `status_t SGTL_ConfigDataFormat (sgtl_handle_t *handle, uint32_t mclk, uint32_t sample_rate, uint32_t bits)`  
*Configure the data format of audio data.*
- `status_t SGTL_SetPlay (sgtl_handle_t *handle, uint32_t playSource)`  
*select SGTL codec play source.*
- `status_t SGTL_SetRecord (sgtl_handle_t *handle, uint32_t recordSource)`  
*select SGTL codec record source.*
- `status_t SGTL_WriteReg (sgtl_handle_t *handle, uint16_t reg, uint16_t val)`  
*Write register to sgtl using I2C.*
- `status_t SGTL_ReadReg (sgtl_handle_t *handle, uint16_t reg, uint16_t *val)`  
*Read register from sgtl using I2C.*
- `status_t SGTL_ModifyReg (sgtl_handle_t *handle, uint16_t reg, uint16_t clr_mask, uint16_t val)`  
*Modify some bits in the register using I2C.*

## Driver version

- `#define FSL_SGTL5000_DRIVER_VERSION (MAKE_VERSION(2, 1, 1))`  
*CLOCK driver version 2.1.1.*

### 55.6.2 Data Structure Documentation

#### 55.6.2.1 struct sgtl\_audio\_format\_t

##### Data Fields

- `uint32_t mclk_HZ`  
*master clock*
- `uint32_t sampleRate`  
*Sample rate.*
- `uint32_t bitWidth`  
*Bit width.*
- `sgtl_sclk_edge_t sclkEdge`  
*sclk valid edge*

#### 55.6.2.2 struct sgtl\_config\_t

##### Data Fields

- `sgtl_route_t route`

- *Audio data route.*
- `sgtl_protocol_t bus`  
*Audio transfer protocol.*
- `bool master_slave`  
*Master or slave.*
- `sgtl_audio_format_t format`  
*audio format*
- `uint8_t slaveAddress`  
*code device slave address*
- `codec_i2c_config_t i2cConfig`  
*i2c bus configuration*

## Field Documentation

- (1) `sgtl_route_t sgtl_config_t::route`
- (2) `bool sgtl_config_t::master_slave`

True means master, false means slave.

### 55.6.2.3 struct sgtl\_handle\_t

#### Data Fields

- `sgtl_config_t * config`  
*sgtl config pointer*
- `uint8_t i2cHandle [SGTL_I2C_HANDLER_SIZE]`  
*i2c handle*

### 55.6.3 Macro Definition Documentation

#### 55.6.3.1 #define FSL\_SGTL5000\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))

#### 55.6.3.2 #define CHIP\_ID 0x0000U

#### 55.6.3.3 #define SGTL5000\_I2C\_ADDR 0x0A

### 55.6.4 Enumeration Type Documentation

#### 55.6.4.1 enum sgtl\_module\_t

Enumerator

- kSGTL\_ModuleADC* ADC module in SGTL5000.
- kSGTL\_ModuleDAC* DAC module in SGTL5000.
- kSGTL\_ModuleDAP* DAP module in SGTL5000.
- kSGTL\_ModuleHP* Headphone module in SGTL5000.

*kSGTL\_ModuleI2SIN* I2S-IN module in SGTL5000.  
*kSGTL\_ModuleI2SOUT* I2S-OUT module in SGTL5000.  
*kSGTL\_ModuleLineIn* Line-in moudle in SGTL5000.  
*kSGTL\_ModuleLineOut* Line-out module in SGTL5000.  
*kSGTL\_ModuleMicin* Micphone module in SGTL5000.

#### 55.6.4.2 enum sgtl\_route\_t

Note

Only provide some typical data route, not all route listed. Users cannot combine any routes, once a new route is set, the previous one would be replaced.

Enumerator

*kSGTL\_RouteBypass* LINEIN->Headphone.  
*kSGTL\_RoutePlayback* I2SIN->DAC->Headphone.  
*kSGTL\_RoutePlaybackandRecord* I2SIN->DAC->Headphone, LINEIN->ADC->I2SOUT.  
*kSGTL\_RoutePlaybackwithDAP* I2SIN->DAP->DAC->Headphone.  
*kSGTL\_RoutePlaybackwithDAPandRecord* I2SIN->DAP->DAC->HP, LINEIN->ADC->I2SOUT.  
*kSGTL\_RouteRecord* LINEIN->ADC->I2SOUT.

#### 55.6.4.3 enum sgtl\_protocol\_t

Sgtl5000 only supports I2S format and PCM format.

Enumerator

*kSGTL\_BusI2S* I2S Type.  
*kSGTL\_BusLeftJustified* Left justified.  
*kSGTL\_BusRightJustified* Right Justified.  
*kSGTL\_BusPCMA* PCMA.  
*kSGTL\_BusPCMB* PCMB.

#### 55.6.4.4 anonymous enum

Enumerator

*kSGTL\_HeadphoneLeft* headphone left channel  
*kSGTL\_HeadphoneRight* headphone right channel  
*kSGTL\_LineoutLeft* lineout left channel  
*kSGTL\_LineoutRight* lineout right channel

#### 55.6.4.5 anonymous enum

Enumerator

*kSGTL\_RecordSourceLineIn* record source line in  
*kSGTL\_RecordSourceMic* record source single end

#### 55.6.4.6 anonymous enum

Enumerator

*kSGTL\_PlaySourceLineIn* play source line in  
*kSGTL\_PlaySourceDAC* play source line in

#### 55.6.4.7 enum sgtl\_sclk\_edge\_t

Enumerator

*kSGTL\_SclkValidEdgeRising* SCLK valid edge.  
*kSGTL\_SclkValidEdgeFailling* SCLK failling edge.

### 55.6.5 Function Documentation

#### 55.6.5.1 status\_t SGTL\_Init( sgtl\_handle\_t \* handle, sgtl\_config\_t \* config )

This function calls SGTL\_I2CInit(), and in this function, some configurations are fixed. The second parameter can be NULL. If users want to change the SGTL5000 settings, a configure structure should be prepared.

Note

If the codec\_config is NULL, it would initialize sgtl5000 using default settings. The default setting:

```
* sgtl_init_t codec_config
* codec_config.route = kSGTL_RoutePlaybackandRecord
* codec_config.bus = kSGTL_BusI2S
* codec_config.master = slave
*
```

Parameters

---

<i>handle</i>	Sgtl5000 handle structure.
<i>config</i>	sgtl5000 configuration structure. If this pointer equals to NULL, it means using the default configuration.

Returns

Initialization status

#### 55.6.5.2 status\_t SGTL\_SetDataRoute ( sgtl\_handle\_t \* *handle*, sgtl\_route\_t *route* )

This function would set the data route according to route. The route cannot be combined, as all route would enable different modules.

Note

If a new route is set, the previous route would not work.

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>route</i>	Audio data route in sgtl5000.

#### 55.6.5.3 status\_t SGTL\_SetProtocol ( sgtl\_handle\_t \* *handle*, sgtl\_protocol\_t *protocol* )

Sgtl5000 only supports I2S, I2S left, I2S right, PCM A, PCM B format.

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>protocol</i>	Audio data transfer protocol.

#### 55.6.5.4 void SGTL\_SetMasterSlave ( sgtl\_handle\_t \* *handle*, bool *master* )

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>master</i>	1 represent master, 0 represent slave.

### 55.6.5.5 status\_t SGTL\_SetVolume ( *sgtl\_handle\_t \* handle*, *sgtl\_module\_t module*, *uint32\_t volume* )

This function would set the volume of sgtl5000 modules. This interface set module volume. The function assume that left channel and right channel has the same volume.

kSGTL\_ModuleADC volume range: 0 - 0xF, 0dB - 22.5dB  
kSGTL\_ModuleDAC volume range: 0x3C - 0xF0, 0dB - -90dB  
kSGTL\_ModuleHP volume range: 0 - 0x7F, 12dB - -51.5dB  
kSGTL\_ModuleLineOut volume range: 0 - 0x1F, 0.5dB steps

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Sgtl5000 module, such as DAC, ADC and etc.
<i>volume</i>	Volume value need to be set. The value is the exact value in register.

### 55.6.5.6 uint32\_t SGTL\_GetVolume ( *sgtl\_handle\_t \* handle*, *sgtl\_module\_t module* )

This function gets the volume of sgtl5000 modules. This interface get DAC module volume. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Sgtl5000 module, such as DAC, ADC and etc.

Returns

Module value, the value is exact value in register.

### 55.6.5.7 status\_t SGTL\_SetMute ( *sgtl\_handle\_t \* handle*, *sgtl\_module\_t module*, *bool mute* )

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Sgtl5000 module, such as DAC, ADC and etc.
<i>mute</i>	True means mute, and false means unmute.

#### 55.6.5.8 status\_t SGTL\_EnableModule ( *sgtl\_handle\_t \* handle*, *sgtl\_module\_t module* )

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Module expected to enable.

#### 55.6.5.9 status\_t SGTL\_DisableModule ( *sgtl\_handle\_t \* handle*, *sgtl\_module\_t module* )

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Module expected to enable.

#### 55.6.5.10 status\_t SGTL\_Deinit ( *sgtl\_handle\_t \* handle* )

Shut down Sgtl5000 modules.

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
---------------	------------------------------------

#### 55.6.5.11 status\_t SGTL\_ConfigDataFormat ( *sgtl\_handle\_t \* handle*, *uint32\_t mclk*, *uint32\_t sample\_rate*, *uint32\_t bits* )

This function would configure the registers about the sample rate, bit depths.

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
<i>mclk</i>	Master clock frequency of I2S.
<i>sample_rate</i>	Sample rate of audio file running in sgtl5000. Sgtl5000 now supports 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k and 96k sample rate.
<i>bits</i>	Bit depth of audio file (Sgtl5000 only supports 16bit, 20bit, 24bit and 32 bit in HW).

### 55.6.5.12 status\_t SGTL\_SetPlay ( *sgtl\_handle\_t \* handle, uint32\_t playSource* )

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
<i>playSource</i>	play source value, reference _sgtl_play_source.

Returns

kStatus\_Success, else failed.

### 55.6.5.13 status\_t SGTL\_SetRecord ( *sgtl\_handle\_t \* handle, uint32\_t recordSource* )

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
<i>recordSource</i>	record source value, reference _sgtl_record_source.

Returns

kStatus\_Success, else failed.

### 55.6.5.14 status\_t SGTL\_WriteReg ( *sgtl\_handle\_t \* handle, uint16\_t reg, uint16\_t val* )

Parameters

<i>handle</i>	Sgtl5000 handle structure.
---------------	----------------------------

<i>reg</i>	The register address in sgtl.
<i>val</i>	Value needs to write into the register.

### 55.6.5.15 status\_t SGTL\_ReadReg ( *sgtl\_handle\_t \* handle, uint16\_t reg, uint16\_t \* val* )

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>reg</i>	The register address in sgtl.
<i>val</i>	Value written to.

### 55.6.5.16 status\_t SGTL\_ModifyReg ( *sgtl\_handle\_t \* handle, uint16\_t reg, uint16\_t clr\_mask, uint16\_t val* )

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>reg</i>	The register address in sgtl.
<i>clr_mask</i>	The mask code for the bits want to write. The bit you want to write should be 0.
<i>val</i>	Value needs to write into the register.

## 55.6.6 SGTL5000 Adapter

### 55.6.6.1 Overview

The sgtl5000 adapter provides a codec unify control interface.

### Macros

- `#define HAL_CODEC_SGTL_HANDLER_SIZE (SGTL_I2C_HANDLER_SIZE + 4)`  
*codec handler size*

### Functions

- `status_t HAL_CODEC_SGTL5000_Init (void *handle, void *config)`  
*Codec initialization.*
- `status_t HAL_CODEC_SGTL5000_Deinit (void *handle)`  
*Codec de-initilization.*
- `status_t HAL_CODEC_SGTL5000_SetFormat (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`  
*set audio data format.*
- `status_t HAL_CODEC_SGTL5000_SetVolume (void *handle, uint32_t playChannel, uint32_t volume)`  
*set audio codec module volume.*
- `status_t HAL_CODEC_SGTL5000_SetMute (void *handle, uint32_t playChannel, bool isMute)`  
*set audio codec module mute.*
- `status_t HAL_CODEC_SGTL5000_SetPower (void *handle, uint32_t module, bool powerOn)`  
*set audio codec module power.*
- `status_t HAL_CODEC_SGTL5000_SetRecord (void *handle, uint32_t recordSource)`  
*codec set record source.*
- `status_t HAL_CODEC_SGTL5000_SetRecordChannel (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)`  
*codec set record channel.*
- `status_t HAL_CODEC_SGTL5000_SetPlay (void *handle, uint32_t playSource)`  
*codec set play source.*
- `status_t HAL_CODEC_SGTL5000_ModuleControl (void *handle, uint32_t cmd, uint32_t data)`  
*codec module control.*
- `static status_t HAL_CODEC_Init (void *handle, void *config)`  
*Codec initilization.*
- `static status_t HAL_CODEC_Deinit (void *handle)`  
*Codec de-initilization.*
- `static status_t HAL_CODEC_SetFormat (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`  
*set audio data format.*
- `static status_t HAL_CODEC_SetVolume (void *handle, uint32_t playChannel, uint32_t volume)`  
*set audio codec module volume.*
- `static status_t HAL_CODEC_SetMute (void *handle, uint32_t playChannel, bool isMute)`  
*set audio codec module mute.*
- `static status_t HAL_CODEC_SetPower (void *handle, uint32_t module, bool powerOn)`

- static `status_t HAL_CODEC_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- static `status_t HAL_CODEC_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- static `status_t HAL_CODEC_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- static `status_t HAL_CODEC_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*

## 55.6.6.2 Function Documentation

### 55.6.6.2.1 `status_t HAL_CODEC_SGTL5000_Init( void * handle, void * config )`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

### 55.6.6.2.2 `status_t HAL_CODEC_SGTL5000_Deinit( void * handle )`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

### 55.6.6.2.3 `status_t HAL_CODEC_SGTL5000_SetFormat( void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth )`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.4 status\_t HAL\_CODEC\_SGTL5000\_SetVolume ( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.5 status\_t HAL\_CODEC\_SGTL5000\_SetMute ( void \* *handle*, uint32\_t *playChannel*, bool *isMute* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.6 status\_t HAL\_CODEC\_SGTL5000\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* )

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.7 status\_t HAL\_CODEC\_SGTL5000\_SetRecord ( void \* *handle*, uint32\_t *recordSource* )

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.8 status\_t HAL\_CODEC\_SGTL5000\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* )

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.9 status\_t HAL\_CODEC\_SGTL5000\_SetPlay ( void \* *handle*, uint32\_t *playSource* )

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.10 **status\_t HAL\_CODEC\_SGTL5000\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* )**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.11 **static status\_t HAL\_CODEC\_Init ( void \* *handle*, void \* *config* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

#### 55.6.6.2.12 **static status\_t HAL\_CODEC\_Deinit ( void \* *handle* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

#### 55.6.6.2.13 static status\_t HAL\_CODEC\_SetFormat( void \* *handle*, uint32\_t *mclk*, uint32\_t *sampleRate*, uint32\_t *bitWidth* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.14 static status\_t HAL\_CODEC\_SetVolume( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.15 static status\_t HAL\_CODEC\_SetMute( void \* *handle*, uint32\_t *playChannel*, bool *isMute* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.16 static status\_t HAL\_CODEC\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.17 static status\_t HAL\_CODEC\_SetRecord ( void \* *handle*, uint32\_t *recordSource* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.6.6.2.18 static status\_t HAL\_CODEC\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

**55.6.6.2.19 static status\_t HAL\_CODEC\_SetPlay ( void \* *handle*, uint32\_t *playSource* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

**55.6.6.2.20 static status\_t HAL\_CODEC\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* ) [inline], [static]**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

## 55.7 WM8960 Driver

### 55.7.1 Overview

The wm8960 driver provides a codec control interface.

## Data Structures

- struct `wm8960_audio_format_t`  
*wm8960 audio format More...*
- struct `wm8960_master_sysclk_config_t`  
*wm8960 master system clock configuration More...*
- struct `wm8960_config_t`  
*Initialize structure of WM8960. More...*
- struct `wm8960_handle_t`  
*wm8960 codec handler More...*

## Macros

- #define `WM8960_I2C_HANDLER_SIZE` CODEC\_I2C\_MASTER\_HANDLER\_SIZE  
*wm8960 handle size*
- #define `WM8960_LINVOL` 0x0U  
*Define the register address of WM8960.*
- #define `WM8960_CACHEREGNUM` 56U  
*Cache register number.*
- #define `WM8960_CLOCK2_BCLK_DIV_MASK` 0xFU  
*WM8960 CLOCK2 bits.*
- #define `WM8960_IFACE1_FORMAT_MASK` 0x03U  
*WM8960\_IFACE1 FORMAT bits.*
- #define `WM8960_IFACE1_WL_MASK` 0x0CU  
*WM8960\_IFACE1 WL bits.*
- #define `WM8960_IFACE1_LRP_MASK` 0x10U  
*WM8960\_IFACE1 LRP bit.*
- #define `WM8960_IFACE1_DLRSWAP_MASK` 0x20U  
*WM8960\_IFACE1 DLRSWAP bit.*
- #define `WM8960_IFACE1_MS_MASK` 0x40U  
*WM8960\_IFACE1 MS bit.*
- #define `WM8960_IFACE1_BCLKINV_MASK` 0x80U  
*WM8960\_IFACE1 BCLKINV bit.*
- #define `WM8960_IFACE1_ALRSWAP_MASK` 0x100U  
*WM8960\_IFACE1 ALRSWAP bit.*
- #define `WM8960_POWER1_VREF_MASK` 0x40U  
*WM8960\_POWER1.*
- #define `WM8960_POWER2_DACL_MASK` 0x100U  
*WM8960\_POWER2.*
- #define `WM8960_I2C_ADDR` 0x1A  
*WM8960 I2C address.*
- #define `WM8960_I2C_BAUDRATE` (100000U)

- WM8960 I<sub>2</sub>C baudrate.
- #define **WM8960\_ADC\_MAX\_VOLUME\_vVALUE** 0xFFU  
WM8960 maximum volume value.

## Enumerations

- enum **wm8960\_module\_t** {
   
kWM8960\_ModuleADC = 0,  
 kWM8960\_ModuleDAC = 1,  
 kWM8960\_ModuleVREF = 2,  
 kWM8960\_ModuleHP = 3,  
 kWM8960\_ModuleMICB = 4,  
 kWM8960\_ModuleMIC = 5,  
 kWM8960\_ModuleLineIn = 6,  
 kWM8960\_ModuleLineOut = 7,  
 kWM8960\_ModuleSpeaker = 8,  
 kWM8960\_ModuleOMIX = 9
 }
   
*Modules in WM8960 board.*
- enum {
   
kWM8960\_HeadphoneLeft = 1,  
 kWM8960\_HeadphoneRight = 2,  
 kWM8960\_SpeakerLeft = 4,  
 kWM8960\_SpeakerRight = 8
 }
   
*wm8960 play channel*
- enum **wm8960\_play\_source\_t** {
   
kWM8960\_PlaySourcePGA = 1,  
 kWM8960\_PlaySourceInput = 2,  
 kWM8960\_PlaySourceDAC = 4
 }
   
*wm8960 play source*
- enum **wm8960\_route\_t** {
   
kWM8960\_RouteBypass = 0,  
 kWM8960\_RoutePlayback = 1,  
 kWM8960\_RoutePlaybackandRecord = 2,  
 kWM8960\_RouteRecord = 5
 }
   
*WM8960 data route.*
- enum **wm8960\_protocol\_t** {
   
kWM8960\_BusI2S = 2,  
 kWM8960\_BusLeftJustified = 1,  
 kWM8960\_BusRightJustified = 0,  
 kWM8960\_BusPCMA = 3,  
 kWM8960\_BusPCMB = 3 | (1 << 4)
 }
   
*The audio data transfer protocol choice.*
- enum **wm8960\_input\_t** {

```

kWM8960_InputClosed = 0,
kWM8960_InputSingleEndedMic = 1,
kWM8960_InputDifferentialMicInput2 = 2,
kWM8960_InputDifferentialMicInput3 = 3,
kWM8960_InputLineINPUT2 = 4,
kWM8960_InputLineINPUT3 = 5 }

    wm8960 input source
• enum {
    kWM8960_AudioSampleRate8KHz = 8000U,
    kWM8960_AudioSampleRate11025Hz = 11025U,
    kWM8960_AudioSampleRate12KHz = 12000U,
    kWM8960_AudioSampleRate16KHz = 16000U,
    kWM8960_AudioSampleRate22050Hz = 22050U,
    kWM8960_AudioSampleRate24KHz = 24000U,
    kWM8960_AudioSampleRate32KHz = 32000U,
    kWM8960_AudioSampleRate44100Hz = 44100U,
    kWM8960_AudioSampleRate48KHz = 48000U,
    kWM8960_AudioSampleRate96KHz = 96000U,
    kWM8960_AudioSampleRate192KHz = 192000U,
    kWM8960_AudioSampleRate384KHz = 384000U }

        audio sample rate definition
• enum {
    kWM8960_AudioBitWidth16bit = 16U,
    kWM8960_AudioBitWidth20bit = 20U,
    kWM8960_AudioBitWidth24bit = 24U,
    kWM8960_AudioBitWidth32bit = 32U }

        audio bit width
• enum wm8960_sysclk_source_t {
    kWM8960_SysClkSourceMclk = 0U,
    kWM8960_SysClkSourceInternalPLL = 1U }

    wm8960 sysclk source

```

## Functions

- **status\_t WM8960\_Init** (**wm8960\_handle\_t** \*handle, const **wm8960\_config\_t** \*config)  
*WM8960 initialize function.*
- **status\_t WM8960\_Deinit** (**wm8960\_handle\_t** \*handle)  
*Deinit the WM8960 codec.*
- **status\_t WM8960\_SetDataRoute** (**wm8960\_handle\_t** \*handle, **wm8960\_route\_t** route)  
*Set audio data route in WM8960.*
- **status\_t WM8960\_SetLeftInput** (**wm8960\_handle\_t** \*handle, **wm8960\_input\_t** input)  
*Set left audio input source in WM8960.*
- **status\_t WM8960\_SetRightInput** (**wm8960\_handle\_t** \*handle, **wm8960\_input\_t** input)  
*Set right audio input source in WM8960.*
- **status\_t WM8960\_SetProtocol** (**wm8960\_handle\_t** \*handle, **wm8960\_protocol\_t** protocol)  
*Set the audio transfer protocol.*

- void [WM8960\\_SetMasterSlave](#) (wm8960\_handle\_t \*handle, bool master)  
*Set WM8960 as master or slave.*
- status\_t [WM8960\\_SetVolume](#) (wm8960\_handle\_t \*handle, wm8960\_module\_t module, uint32\_t volume)  
*Set the volume of different modules in WM8960.*
- uint32\_t [WM8960\\_GetVolume](#) (wm8960\_handle\_t \*handle, wm8960\_module\_t module)  
*Get the volume of different modules in WM8960.*
- status\_t [WM8960\\_SetMute](#) (wm8960\_handle\_t \*handle, wm8960\_module\_t module, bool isEnabled)  
*Mute modules in WM8960.*
- status\_t [WM8960\\_SetModule](#) (wm8960\_handle\_t \*handle, wm8960\_module\_t module, bool isEnabled)  
*Enable/disable expected devices.*
- status\_t [WM8960\\_SetPlay](#) (wm8960\_handle\_t \*handle, uint32\_t playSource)  
*SET the WM8960 play source.*
- status\_t [WM8960\\_ConfigDataFormat](#) (wm8960\_handle\_t \*handle, uint32\_t sysclk, uint32\_t sample\_rate, uint32\_t bits)  
*Configure the data format of audio data.*
- status\_t [WM8960\\_SetJackDetect](#) (wm8960\_handle\_t \*handle, bool isEnabled)  
*Enable/disable jack detect feature.*
- status\_t [WM8960\\_WriteReg](#) (wm8960\_handle\_t \*handle, uint8\_t reg, uint16\_t val)  
*Write register to WM8960 using I2C.*
- status\_t [WM8960\\_ReadReg](#) (uint8\_t reg, uint16\_t \*val)  
*Read register from WM8960 using I2C.*
- status\_t [WM8960\\_ModifyReg](#) (wm8960\_handle\_t \*handle, uint8\_t reg, uint16\_t mask, uint16\_t val)  
*Modify some bits in the register using I2C.*

## Driver version

- #define [FSL\\_WM8960\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 2, 2))  
*CLOCK driver version 2.2.2.*

### 55.7.2 Data Structure Documentation

#### 55.7.2.1 struct [wm8960\\_audio\\_format\\_t](#)

##### Data Fields

- uint32\_t [mclk\\_HZ](#)  
*master clock frequency*
- uint32\_t [sampleRate](#)  
*sample rate*
- uint32\_t [bitWidth](#)  
*bit width*

### 55.7.2.2 struct wm8960\_master\_sysclk\_config\_t

#### Data Fields

- `wm8960_sysclk_source_t sysclkSource`  
*sysclk source*
- `uint32_t sysclkFreq`  
*PLL output frequency value.*

### 55.7.2.3 struct wm8960\_config\_t

#### Data Fields

- `wm8960_route_t route`  
*Audio data route.*
- `wm8960_protocol_t bus`  
*Audio transfer protocol.*
- `wm8960_audio_format_t format`  
*Audio format.*
- `bool master_slave`  
*Master or slave.*
- `wm8960_master_sysclk_config_t masterClock`  
*master clock configurations*
- `bool enableSpeaker`  
*True means enable class D speaker as output, false means no.*
- `wm8960_input_t leftInputSource`  
*Left input source for WM8960.*
- `wm8960_input_t rightInputSource`  
*Right input source for WM8960.*
- `wm8960_play_source_t playSource`  
*play source*
- `uint8_t slaveAddress`  
*wm8960 device address*
- `codec_i2c_config_t i2cConfig`  
*i2c configuration*

#### Field Documentation

(1) `wm8960_route_t wm8960_config_t::route`

(2) `bool wm8960_config_t::master_slave`

### 55.7.2.4 struct wm8960\_handle\_t

#### Data Fields

- `const wm8960_config_t * config`  
*wm8904 config pointer*
- `uint8_t i2cHandle [WM8960_I2C_HANDLER_SIZE]`  
*i2c handle*

### 55.7.3 Macro Definition Documentation

#### 55.7.3.1 #define WM8960\_LINVOL 0x0U

#### 55.7.3.2 #define WM8960\_I2C\_ADDR 0x1A

### 55.7.4 Enumeration Type Documentation

#### 55.7.4.1 enum wm8960\_module\_t

Enumerator

*kWM8960\_ModuleADC* ADC module in WM8960.  
*kWM8960\_ModuleDAC* DAC module in WM8960.  
*kWM8960\_ModuleVREF* VREF module.  
*kWM8960\_ModuleHP* Headphone.  
*kWM8960\_ModuleMICB* Mic bias.  
*kWM8960\_ModuleMIC* Input Mic.  
*kWM8960\_ModuleLineIn* Analog in PGA.  
*kWM8960\_ModuleLineOut* Line out module.  
*kWM8960\_ModuleSpeaker* Speaker module.  
*kWM8960\_ModuleOMIX* Output mixer.

#### 55.7.4.2 anonymous enum

Enumerator

*kWM8960\_HeadphoneLeft* wm8960 headphone left channel  
*kWM8960\_HeadphoneRight* wm8960 headphone right channel  
*kWM8960\_SpeakerLeft* wm8960 speaker left channel  
*kWM8960\_SpeakerRight* wm8960 speaker right channel

#### 55.7.4.3 enum wm8960\_play\_source\_t

Enumerator

*kWM8960\_PlaySourcePGA* wm8960 play source PGA  
*kWM8960\_PlaySourceInput* wm8960 play source Input  
*kWM8960\_PlaySourceDAC* wm8960 play source DAC

#### 55.7.4.4 enum wm8960\_route\_t

Only provide some typical data route, not all route listed. Note: Users cannot combine any routes, once a new route is set, the previous one would be replaced.

Enumerator

*kWM8960\_RouteBypass* LINEIN->Headphone.  
*kWM8960\_RoutePlayback* I2SIN->DAC->Headphone.  
*kWM8960\_RoutePlaybackandRecord* I2SIN->DAC->Headphone, LINEIN->ADC->I2SOUT.  
*kWM8960\_RouteRecord* LINEIN->ADC->I2SOUT.

#### 55.7.4.5 enum **wm8960\_protocol\_t**

WM8960 only supports I2S format and PCM format.

Enumerator

*kWM8960\_BusI2S* I2S type.  
*kWM8960\_BusLeftJustified* Left justified mode.  
*kWM8960\_BusRightJustified* Right justified mode.  
*kWM8960\_BusPCMA* PCM A mode.  
*kWM8960\_BusPCMB* PCM B mode.

#### 55.7.4.6 enum **wm8960\_input\_t**

Enumerator

*kWM8960\_InputClosed* Input device is closed.  
*kWM8960\_InputSingleEndedMic* Input as single ended mic, only use L/RINPUT1.  
*kWM8960\_InputDifferentialMicInput2* Input as differential mic, use L/RINPUT1 and L/RINPUT2.  
*kWM8960\_InputDifferentialMicInput3* Input as differential mic, use L/RINPUT1 and L/RINPUT3.  
*kWM8960\_InputLineINPUT2* Input as line input, only use L/RINPUT2.  
*kWM8960\_InputLineINPUT3* Input as line input, only use L/RINPUT3.

#### 55.7.4.7 anonymous enum

Enumerator

*kWM8960\_AudioSampleRate8KHz* Sample rate 8000 Hz.  
*kWM8960\_AudioSampleRate11025Hz* Sample rate 11025 Hz.  
*kWM8960\_AudioSampleRate12KHz* Sample rate 12000 Hz.  
*kWM8960\_AudioSampleRate16KHz* Sample rate 16000 Hz.  
*kWM8960\_AudioSampleRate22050Hz* Sample rate 22050 Hz.  
*kWM8960\_AudioSampleRate24KHz* Sample rate 24000 Hz.  
*kWM8960\_AudioSampleRate32KHz* Sample rate 32000 Hz.  
*kWM8960\_AudioSampleRate44100Hz* Sample rate 44100 Hz.  
*kWM8960\_AudioSampleRate48KHz* Sample rate 48000 Hz.

*kWM8960\_AudioSampleRate96KHz* Sample rate 96000 Hz.  
*kWM8960\_AudioSampleRate192KHz* Sample rate 192000 Hz.  
*kWM8960\_AudioSampleRate384KHz* Sample rate 384000 Hz.

#### 55.7.4.8 anonymous enum

Enumerator

*kWM8960\_AudioBitWidth16bit* audio bit width 16  
*kWM8960\_AudioBitWidth20bit* audio bit width 20  
*kWM8960\_AudioBitWidth24bit* audio bit width 24  
*kWM8960\_AudioBitWidth32bit* audio bit width 32

#### 55.7.4.9 enum **wm8960\_sysclk\_source\_t**

Enumerator

*kWM8960\_SysClkSourceMclk* sysclk source from external MCLK  
*kWM8960\_SysClkSourceInternalPLL* sysclk source from internal PLL

### 55.7.5 Function Documentation

#### 55.7.5.1 status\_t **WM8960\_Init** ( **wm8960\_handle\_t \* handle**, **const wm8960\_config\_t \* config** )

The second parameter is NULL to WM8960 in this version. If users want to change the settings, they have to use `wm8960_write_reg()` or `wm8960_modify_reg()` to set the register value of WM8960. Note: If the `codec_config` is NULL, it would initialize WM8960 using default settings. The default setting: `codec_config->route = kWM8960_RoutePlaybackandRecord` `codec_config->bus = kWM8960_BusI2S` `codec_config->master = slave`

Parameters

<i>handle</i>	WM8960 handle structure.
<i>config</i>	WM8960 configuration structure.

#### 55.7.5.2 status\_t **WM8960\_Deinit** ( **wm8960\_handle\_t \* handle** )

This function close all modules in WM8960 to save power.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
---------------	----------------------------------

#### 55.7.5.3 status\_t WM8960\_SetDataRoute ( *wm8960\_handle\_t \* handle, wm8960\_route\_t route* )

This function would set the data route according to route. The route cannot be combined, as all route would enable different modules. Note: If a new route is set, the previous route would not work.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>route</i>	Audio data route in WM8960.

#### 55.7.5.4 status\_t WM8960\_SetLeftInput ( *wm8960\_handle\_t \* handle, wm8960\_input\_t input* )

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

#### 55.7.5.5 status\_t WM8960\_SetRightInput ( *wm8960\_handle\_t \* handle, wm8960\_input\_t input* )

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

#### 55.7.5.6 status\_t WM8960\_SetProtocol ( *wm8960\_handle\_t \* handle, wm8960\_protocol\_t protocol* )

WM8960 only supports I2S, left justified, right justified, PCM A, PCM B format.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>protocol</i>	Audio data transfer protocol.

#### 55.7.5.7 void WM8960\_SetMasterSlave ( **wm8960\_handle\_t \* handle, bool master** )

Parameters

<i>handle</i>	WM8960 handle structure.
<i>master</i>	1 represent master, 0 represent slave.

#### 55.7.5.8 status\_t WM8960\_SetVolume ( **wm8960\_handle\_t \* handle, wm8960\_module\_t module, uint32\_t volume** )

This function would set the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Module:kWM8960\_ModuleADC, volume range value: 0 is mute, 1-255 is -97db to 30db  
 Module:kWM8960\_ModuleDAC, volume range value: 0 is mute, 1-255 is -127db to 0db  
 Module:kWM8960\_ModuleHP, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db  
 Module:kWM8960\_ModuleLineIn, volume range value: 0 - 0x3F is -17.25db to 30db  
 Module:kWM8960\_ModuleSpeaker, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.
<i>volume</i>	Volume value need to be set.

#### 55.7.5.9 uint32\_t WM8960\_GetVolume ( **wm8960\_handle\_t \* handle, wm8960\_module\_t module** )

This function gets the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.

Returns

Volume value of the module.

#### 55.7.5.10 status\_t WM8960\_SetMute ( *wm8960\_handle\_t \* handle, wm8960\_module\_t module, bool isEnabled* )

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Modules need to be mute.
<i>isEnabled</i>	Mute or unmute, 1 represent mute.

#### 55.7.5.11 status\_t WM8960\_SetModule ( *wm8960\_handle\_t \* handle, wm8960\_module\_t module, bool isEnabled* )

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module expected to enable.
<i>isEnabled</i>	Enable or disable moudles.

#### 55.7.5.12 status\_t WM8960\_SetPlay ( *wm8960\_handle\_t \* handle, uint32\_t playSource* )

Parameters

<i>handle</i>	WM8960 handle structure.
<i>playSource</i>	play source , can be a value combine of kWM8960_ModuleHeadphoneSourcePG-A, kWM8960_ModuleHeadphoneSourceDAC, kWM8960_ModulePlaySourceInput, kWM8960_ModulePlayMonoRight, kWM8960_ModulePlayMonoLeft.

Returns

kStatus\_WM8904\_Success if successful, different code otherwise..

**55.7.5.13 status\_t WM8960\_ConfigDataFormat ( *wm8960\_handle\_t \* handle, uint32\_t sysclk, uint32\_t sample\_rate, uint32\_t bits* )**

This function would configure the registers about the sample rate, bit depths.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
<i>sysclk</i>	system clock of the codec which can be generated by MCLK or PLL output.
<i>sample_rate</i>	Sample rate of audio file running in WM8960. WM8960 now supports 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k and 96k sample rate.
<i>bits</i>	Bit depth of audio file (WM8960 only supports 16bit, 20bit, 24bit and 32 bit in HW).

**55.7.5.14 status\_t WM8960\_SetJackDetect ( *wm8960\_handle\_t \* handle, bool isEnabled* )**

Parameters

<i>handle</i>	WM8960 handle structure.
<i>isEnabled</i>	Enable or disable moudles.

**55.7.5.15 status\_t WM8960\_WriteReg ( *wm8960\_handle\_t \* handle, uint8\_t reg, uint16\_t val* )**

Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>val</i>	Value needs to write into the register.

**55.7.5.16 status\_t WM8960\_ReadReg ( *uint8\_t reg, uint16\_t \* val* )**

Parameters

<i>reg</i>	The register address in WM8960.
<i>val</i>	Value written to.

**55.7.5.17 status\_t WM8960\_ModifyReg ( *wm8960\_handle\_t \* handle, uint8\_t reg, uint16\_t mask, uint16\_t val* )**

## Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>mask</i>	The mask code for the bits want to write. The bit you want to write should be 0.
<i>val</i>	Value needs to write into the register.

## 55.7.6 WM8960 Adapter

### 55.7.6.1 Overview

The wm8960 adapter provides a codec unify control interface.

#### Macros

- #define `HAL_CODEC_WM8960_HANDLER_SIZE` (`WM8960_I2C_HANDLER_SIZE + 4`)  
*codec handler size*

#### Functions

- `status_t HAL_CODEC_WM8960_Init` (void \*handle, void \*config)  
*Codec initialization.*
- `status_t HAL_CODEC_WM8960_Deinit` (void \*handle)  
*Codec de-initilization.*
- `status_t HAL_CODEC_WM8960_SetFormat` (void \*handle, uint32\_t mclk, uint32\_t sampleRate, uint32\_t bitWidth)  
*set audio data format.*
- `status_t HAL_CODEC_WM8960_SetVolume` (void \*handle, uint32\_t playChannel, uint32\_t volume)  
*set audio codec module volume.*
- `status_t HAL_CODEC_WM8960_SetMute` (void \*handle, uint32\_t playChannel, bool isMute)  
*set audio codec module mute.*
- `status_t HAL_CODEC_WM8960_SetPower` (void \*handle, uint32\_t module, bool powerOn)  
*set audio codec module power.*
- `status_t HAL_CODEC_WM8960_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- `status_t HAL_CODEC_WM8960_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- `status_t HAL_CODEC_WM8960_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- `status_t HAL_CODEC_WM8960_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*
- static `status_t HAL_CODEC_Init` (void \*handle, void \*config)  
*Codec initilization.*
- static `status_t HAL_CODEC_Deinit` (void \*handle)  
*Codec de-initilization.*
- static `status_t HAL_CODEC_SetFormat` (void \*handle, uint32\_t mclk, uint32\_t sampleRate, uint32\_t bitWidth)  
*set audio data format.*
- static `status_t HAL_CODEC_SetVolume` (void \*handle, uint32\_t playChannel, uint32\_t volume)  
*set audio codec module volume.*
- static `status_t HAL_CODEC_SetMute` (void \*handle, uint32\_t playChannel, bool isMute)  
*set audio codec module mute.*
- static `status_t HAL_CODEC_SetPower` (void \*handle, uint32\_t module, bool powerOn)

- static `status_t HAL_CODEC_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- static `status_t HAL_CODEC_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- static `status_t HAL_CODEC_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- static `status_t HAL_CODEC_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*

### 55.7.6.2 Function Documentation

#### 55.7.6.2.1 `status_t HAL_CODEC_WM8960_Init( void * handle, void * config )`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

#### 55.7.6.2.2 `status_t HAL_CODEC_WM8960_Deinit( void * handle )`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

#### 55.7.6.2.3 `status_t HAL_CODEC_WM8960_SetFormat( void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth )`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.4 status\_t HAL\_CODEC\_WM8960\_SetVolume ( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.5 status\_t HAL\_CODEC\_WM8960\_SetMute ( void \* *handle*, uint32\_t *playChannel*, bool *isMute* )

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.6 status\_t HAL\_CODEC\_WM8960\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* )

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.7 status\_t HAL\_CODEC\_WM8960\_SetRecord ( void \* *handle*, uint32\_t *recordSource* )

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.8 status\_t HAL\_CODEC\_WM8960\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* )

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.9 status\_t HAL\_CODEC\_WM8960\_SetPlay ( void \* *handle*, uint32\_t *playSource* )

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.10 status\_t HAL\_CODEC\_WM8960\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* )

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.11 static status\_t HAL\_CODEC\_Init ( void \* *handle*, void \* *config* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus\_Success is success, else initial failed.

#### 55.7.6.2.12 static status\_t HAL\_CODEC\_Deinit ( void \* *handle* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus\_Success is success, else de-initial failed.

#### 55.7.6.2.13 static status\_t HAL\_CODEC\_SetFormat( void \* *handle*, uint32\_t *mclk*, uint32\_t *sampleRate*, uint32\_t *bitWidth* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.14 static status\_t HAL\_CODEC\_SetVolume( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.15 static status\_t HAL\_CODEC\_SetMute( void \* *handle*, uint32\_t *playChannel*, bool *isMute* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.16 static status\_t HAL\_CODEC\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.17 static status\_t HAL\_CODEC\_SetRecord ( void \* *handle*, uint32\_t *recordSource* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus\_Success is success, else configure failed.

#### 55.7.6.2.18 static status\_t HAL\_CODEC\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* ) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus\_Success is success, else configure failed.

**55.7.6.2.19 static status\_t HAL\_CODEC\_SetPlay ( void \* *handle*, uint32\_t *playSource* ) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus\_Success is success, else configure failed.

**55.7.6.2.20 static status\_t HAL\_CODEC\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* ) [inline], [static]**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus\_Success is success, else configure failed.

## 55.8 WM8904 Driver

### 55.8.1 Overview

The wm8904 driver provides a codec control interface.

## Data Structures

- struct [wm8904\\_fll\\_config\\_t](#)  
*wm8904 fll configuration* [More...](#)
- struct [wm8904\\_audio\\_format\\_t](#)  
*Audio format configuration.* [More...](#)
- struct [wm8904\\_config\\_t](#)  
*Configuration structure of WM8904.* [More...](#)
- struct [wm8904\\_handle\\_t](#)  
*wm8904 codec handler* [More...](#)

## Macros

- #define [WM8904\\_I2C\\_HANDLER\\_SIZE](#) (CODEC\_I2C\_MASTER\_HANDLER\_SIZE)  
*wm8904 handle size*
- #define [WM8904\\_DEBUG\\_REGISTER](#) 0  
*wm8904 debug macro*
- #define [WM8904\\_RESET](#) (0x00)  
*WM8904 register map.*
- #define [WM8904\\_I2C\\_ADDRESS](#) (0x1A)  
*WM8904 I2C address.*
- #define [WM8904\\_I2C\\_BITRATE](#) (400000U)  
*WM8904 I2C bit rate.*
- #define [WM8904\\_MAP\\_HEADPHONE\\_LINEOUT\\_MAX\\_VOLUME](#) 0x3FU  
*WM8904 maximum volume.*

## Enumerations

- enum {
   
*kStatus\_WM8904\_Success* = 0x0,  
*kStatus\_WM8904\_Fail* = 0x1
 }
   
*WM8904 status return codes.*
- enum {
   
*kWM8904\_LRCPolarityNormal* = 0U,  
*kWM8904\_LRCPolarityInverted* = 1U << 4U
 }
   
*WM8904 lrc polarity.*
- enum [wm8904\\_module\\_t](#) {

- ```
kWM8904_ModuleADC = 0,
kWM8904_ModuleDAC = 1,
kWM8904_ModulePGA = 2,
kWM8904_ModuleHeadphone = 3,
kWM8904_ModuleLineout = 4 }
```

*wm8904 module value*
- enum

```
wm8904 play channel
```
- enum `wm8904_timeslot_t` {

```
kWM8904_TimeSlot0 = 0U,
kWM8904_TimeSlot1 = 1U }
```

*WM8904 time slot.*
- enum `wm8904_protocol_t` {

```
kWM8904_ProtocolI2S = 0x2,
kWM8904_ProtocolLeftJustified = 0x1,
kWM8904_ProtocolRightJustified = 0x0,
kWM8904_ProtocolPCMA = 0x3,
kWM8904_ProtocolPCMB = 0x3 | (1 << 4) }
```

*The audio data transfer protocol.*
- enum `wm8904_fs_ratio_t` {

```
kWM8904_FsRatio64X = 0x0,
kWM8904_FsRatio128X = 0x1,
kWM8904_FsRatio192X = 0x2,
kWM8904_FsRatio256X = 0x3,
kWM8904_FsRatio384X = 0x4,
kWM8904_FsRatio512X = 0x5,
kWM8904_FsRatio768X = 0x6,
kWM8904_FsRatio1024X = 0x7,
kWM8904_FsRatio1408X = 0x8,
kWM8904_FsRatio1536X = 0x9 }
```

*The SYSCLK / fs ratio.*
- enum `wm8904_sample_rate_t` {

```
kWM8904_SampleRate8kHz = 0x0,
kWM8904_SampleRate12kHz = 0x1,
kWM8904_SampleRate16kHz = 0x2,
kWM8904_SampleRate24kHz = 0x3,
kWM8904_SampleRate32kHz = 0x4,
kWM8904_SampleRate48kHz = 0x5,
kWM8904_SampleRate11025Hz = 0x6,
kWM8904_SampleRate22050Hz = 0x7,
kWM8904_SampleRate44100Hz = 0x8 }
```

*Sample rate.*
- enum `wm8904_bit_width_t` {

```
kWM8904_BitWidth16 = 0x0,
kWM8904_BitWidth20 = 0x1,
kWM8904_BitWidth24 = 0x2,
```

```

kWM8904_BitWidth32 = 0x3 }

Bit width.
• enum {
    kWM8904_RecordSourceDifferentialLine = 1U,
    kWM8904_RecordSourceLineInput = 2U,
    kWM8904_RecordSourceDifferentialMic = 4U,
    kWM8904_RecordSourceDigitalMic = 8U }
    wm8904 record source
• enum {
    kWM8904_RecordChannelLeft1 = 1U,
    kWM8904_RecordChannelLeft2 = 2U,
    kWM8904_RecordChannelLeft3 = 4U,
    kWM8904_RecordChannelRight1 = 1U,
    kWM8904_RecordChannelRight2 = 2U,
    kWM8904_RecordChannelRight3 = 4U,
    kWM8904_RecordChannelDifferentialPositive1 = 1U,
    kWM8904_RecordChannelDifferentialPositive2 = 2U,
    kWM8904_RecordChannelDifferentialPositive3 = 4U,
    kWM8904_RecordChannelDifferentialNegative1 = 8U,
    kWM8904_RecordChannelDifferentialNegative2 = 16U,
    kWM8904_RecordChannelDifferentialNegative3 = 32U }
    wm8904 record channel
• enum {
    kWM8904_PlaySourcePGA = 1U,
    kWM8904_PlaySourceDAC = 4U }
    wm8904 play source
• enum wm8904\_sys\_clk\_source\_t {
    kWM8904_SysClkSourceMCLK = 0U,
    kWM8904_SysClkSourceFLL = 1U << 14 }
    wm8904 system clock source
• enum wm8904\_fll\_clk\_source\_t { kWM8904_FLLClkSourceMCLK = 0U }
    wm8904 fll clock source

```

## Functions

- [status\\_t WM8904\\_WriteRegister \(wm8904\\_handle\\_t \\*handle, uint8\\_t reg, uint16\\_t value\)](#)  
*WM8904 write register.*
- [status\\_t WM8904\\_ReadRegister \(wm8904\\_handle\\_t \\*handle, uint8\\_t reg, uint16\\_t \\*value\)](#)  
*WM8904 write register.*
- [status\\_t WM8904\\_ModifyRegister \(wm8904\\_handle\\_t \\*handle, uint8\\_t reg, uint16\\_t mask, uint16\\_t value\)](#)  
*WM8904 modify register.*
- [status\\_t WM8904\\_Init \(wm8904\\_handle\\_t \\*handle, \[wm8904\\\_config\\\_t\]\(#\) \\*wm8904Config\)](#)  
*Initializes WM8904.*
- [status\\_t WM8904\\_Deinit \(wm8904\\_handle\\_t \\*handle\)](#)  
*Deinitializes the WM8904 codec.*
- [void WM8904\\_GetDefaultConfig \(\[wm8904\\\_config\\\_t\]\(#\) \\*config\)](#)

*Fills the configuration structure with default values.*

- **status\_t WM8904\_SetMasterSlave** (`wm8904_handle_t *handle, bool master`)
 

*Sets WM8904 as master or slave.*
- **status\_t WM8904\_SetMasterClock** (`wm8904_handle_t *handle, uint32_t sysclk, uint32_t sampleRate, uint32_t bitWidth`)
 

*Sets WM8904 master clock configuration.*
- **status\_t WM8904\_SetFLLConfig** (`wm8904_handle_t *handle, wm8904_fll_config_t *config`)
 

*WM8904 set PLL configuration This function will enable the GPIO1 FLL clock output function, so user can see the generated fll output clock frequency from WM8904 GPIO1.*
- **status\_t WM8904\_SetProtocol** (`wm8904_handle_t *handle, wm8904_protocol_t protocol`)
 

*Sets the audio data transfer protocol.*
- **status\_t WM8904\_SetAudioFormat** (`wm8904_handle_t *handle, uint32_t sysclk, uint32_t sampleRate, uint32_t bitWidth`)
 

*Sets the audio data format.*
- **status\_t WM8904\_CheckAudioFormat** (`wm8904_handle_t *handle, wm8904_audio_format_t *format, uint32_t mclkFreq`)
 

*check and update the audio data format.*
- **status\_t WM8904\_SetVolume** (`wm8904_handle_t *handle, uint16_t volumeLeft, uint16_t volumeRight`)
 

*Sets the module output volume.*
- **status\_t WM8904\_SetMute** (`wm8904_handle_t *handle, bool muteLeft, bool muteRight`)
 

*Sets the headphone output mute.*
- **status\_t WM8904\_SelectLRCPolarity** (`wm8904_handle_t *handle, uint32_t polarity`)
 

*Select LRC polarity.*
- **status\_t WM8904\_EnableDACTDMMMode** (`wm8904_handle_t *handle, wm8904_timeslot_t timeSlot`)
 

*Enable WM8904 DAC time slot.*
- **status\_t WM8904\_EnableADCTDMMMode** (`wm8904_handle_t *handle, wm8904_timeslot_t timeSlot`)
 

*Enable WM8904 ADC time slot.*
- **status\_t WM8904\_SetModulePower** (`wm8904_handle_t *handle, wm8904_module_t module, bool isEnabled`)
 

*SET the module output power.*
- **status\_t WM8904\_SetDACVolume** (`wm8904_handle_t *handle, uint8_t volume`)
 

*SET the DAC module volume.*
- **status\_t WM8904\_SetChannelVolume** (`wm8904_handle_t *handle, uint32_t channel, uint32_t volume`)
 

*Sets the channel output volume.*
- **status\_t WM8904\_SetRecord** (`wm8904_handle_t *handle, uint32_t recordSource`)
 

*SET the WM8904 record source.*
- **status\_t WM8904\_SetRecordChannel** (`wm8904_handle_t *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel`)
 

*SET the WM8904 record source.*
- **status\_t WM8904\_SetPlay** (`wm8904_handle_t *handle, uint32_t playSource`)
 

*SET the WM8904 play source.*
- **status\_t WM8904\_SetChannelMute** (`wm8904_handle_t *handle, uint32_t channel, bool isMute`)
 

*Sets the channel mute.*

## Driver version

- #define FSL\_WM8904\_DRIVER\_VERSION (MAKE\_VERSION(2, 5, 1))  
*WM8904 driver version 2.5.1.*

### 55.8.2 Data Structure Documentation

#### 55.8.2.1 struct wm8904\_fll\_config\_t

##### Data Fields

- `wm8904_fll_clk_source_t source`  
*fll reference clock source*
- `uint32_t refClock_HZ`  
*fll reference clock frequency*
- `uint32_t outputClock_HZ`  
*fll output clock frequency*

#### 55.8.2.2 struct wm8904\_audio\_format\_t

##### Data Fields

- `wm8904_fs_ratio_t fsRatio`  
*SYSCLK / fs ratio.*
- `wm8904_sample_rate_t sampleRate`  
*Sample rate.*
- `wm8904_bit_width_t bitWidth`  
*Bit width.*

#### 55.8.2.3 struct wm8904\_config\_t

##### Data Fields

- `bool master`  
*Master or slave.*
- `wm8904_sys_clk_source_t sysClkSource`  
*system clock source*
- `wm8904_fll_config_t * fll`  
*fll configuration*
- `wm8904_protocol_t protocol`  
*Audio transfer protocol.*
- `wm8904_audio_format_t format`  
*Audio format.*
- `uint32_t mclk_HZ`  
*MCLK frequency value.*
- `uint16_t recordSource`  
*record source*

- `uint16_t recordChannelLeft`  
*record channel*
- `uint16_t recordChannelRight`  
*record channel*
- `uint16_t playSource`  
*play source*
- `uint8_t slaveAddress`  
*code device slave address*
- `codec_i2c_config_t i2cConfig`  
*i2c bus configuration*

#### 55.8.2.4 struct `wm8904_handle_t`

##### Data Fields

- `wm8904_config_t * config`  
*wm8904 config pointer*
- `uint8_t i2cHandle [WM8904_I2C_HANDLER_SIZE]`  
*i2c handle*

#### 55.8.3 Macro Definition Documentation

55.8.3.1 `#define FSL_WM8904_DRIVER_VERSION (MAKE_VERSION(2, 5, 1))`

55.8.3.2 `#define WM8904_I2C_ADDRESS (0x1A)`

55.8.3.3 `#define WM8904_I2C_BITRATE (400000U)`

#### 55.8.4 Enumeration Type Documentation

##### 55.8.4.1 anonymous enum

Enumerator

*kStatus\_WM8904\_Success* Success.  
*kStatus\_WM8904\_Fail* Failure.

##### 55.8.4.2 anonymous enum

Enumerator

*kWM8904\_LRCNormal* LRC polarity normal.  
*kWM8904\_LRCPolarityInverted* LRC polarity inverted.

#### 55.8.4.3 enum wm8904\_module\_t

Enumerator

- kWM8904\_ModuleADC* module ADC
- kWM8904\_ModuleDAC* module DAC
- kWM8904\_ModulePGA* module PGA
- kWM8904\_ModuleHeadphone* module headphone
- kWM8904\_ModuleLineout* module line out

#### 55.8.4.4 anonymous enum

#### 55.8.4.5 enum wm8904\_timeslot\_t

Enumerator

- kWM8904\_TimeSlot0* time slot0
- kWM8904\_TimeSlot1* time slot1

#### 55.8.4.6 enum wm8904\_protocol\_t

Enumerator

- kWM8904\_ProtocolI2S* I2S type.
- kWM8904\_ProtocolLeftJustified* Left justified mode.
- kWM8904\_ProtocolRightJustified* Right justified mode.
- kWM8904\_ProtocolPCMA* PCM A mode.
- kWM8904\_ProtocolPCMB* PCM B mode.

#### 55.8.4.7 enum wm8904\_fs\_ratio\_t

Enumerator

- kWM8904\_FsRatio64X* SYSCLK is  $64 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio128X* SYSCLK is  $128 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio192X* SYSCLK is  $192 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio256X* SYSCLK is  $256 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio384X* SYSCLK is  $384 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio512X* SYSCLK is  $512 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio768X* SYSCLK is  $768 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio1024X* SYSCLK is  $1024 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio1408X* SYSCLK is  $1408 * \text{sample rate} * \text{frame width}$ .
- kWM8904\_FsRatio1536X* SYSCLK is  $1536 * \text{sample rate} * \text{frame width}$ .

#### 55.8.4.8 enum `wm8904_sample_rate_t`

Enumerator

- kWM8904\_SampleRate8kHz* 8 kHz
- kWM8904\_SampleRate12kHz* 12kHz
- kWM8904\_SampleRate16kHz* 16kHz
- kWM8904\_SampleRate24kHz* 24kHz
- kWM8904\_SampleRate32kHz* 32kHz
- kWM8904\_SampleRate48kHz* 48kHz
- kWM8904\_SampleRate11025Hz* 11.025kHz
- kWM8904\_SampleRate22050Hz* 22.05kHz
- kWM8904\_SampleRate44100Hz* 44.1kHz

#### 55.8.4.9 enum `wm8904_bit_width_t`

Enumerator

- kWM8904\_BitWidth16* 16 bits
- kWM8904\_BitWidth20* 20 bits
- kWM8904\_BitWidth24* 24 bits
- kWM8904\_BitWidth32* 32 bits

#### 55.8.4.10 anonymous enum

Enumerator

- kWM8904\_RecordSourceDifferentialLine* record source from differential line
- kWM8904\_RecordSourceLineInput* record source from line input
- kWM8904\_RecordSourceDifferentialMic* record source from differential mic
- kWM8904\_RecordSourceDigitalMic* record source from digital microphone

#### 55.8.4.11 anonymous enum

Enumerator

- kWM8904\_RecordChannelLeft1* left record channel 1
- kWM8904\_RecordChannelLeft2* left record channel 2
- kWM8904\_RecordChannelLeft3* left record channel 3
- kWM8904\_RecordChannelRight1* right record channel 1
- kWM8904\_RecordChannelRight2* right record channel 2
- kWM8904\_RecordChannelRight3* right record channel 3
- kWM8904\_RecordChannelDifferentialPositive1* differential positive record channel 1
- kWM8904\_RecordChannelDifferentialPositive2* differential positive record channel 2
- kWM8904\_RecordChannelDifferentialPositive3* differential positive record channel 3

- kWM8904\_RecordChannelDifferentialNegative1* differential negative record channel 1
- kWM8904\_RecordChannelDifferentialNegative2* differential negative record channel 2
- kWM8904\_RecordChannelDifferentialNegative3* differential negative record channel 3

#### 55.8.4.12 anonymous enum

Enumerator

- kWM8904\_PlaySourcePGA* play source PGA, bypass ADC
- kWM8904\_PlaySourceDAC* play source Input3

#### 55.8.4.13 enum `wm8904_sys_clk_source_t`

Enumerator

- kWM8904\_SysClkSourceMCLK* wm8904 system clock soure from MCLK
- kWM8904\_SysClkSourceFLL* wm8904 system clock soure from FLL

#### 55.8.4.14 enum `wm8904_fll_clk_source_t`

Enumerator

- kWM8904\_FLLClkSourceMCLK* wm8904 FLL clock source from MCLK

### 55.8.5 Function Documentation

#### 55.8.5.1 status\_t `WM8904_WriteRegister` ( `wm8904_handle_t * handle, uint8_t reg, uint16_t value` )

Parameters

|               |                          |
|---------------|--------------------------|
| <i>handle</i> | WM8904 handle structure. |
| <i>reg</i>    | register address.        |
| <i>value</i>  | value to write.          |

Returns

`kStatus_Success`, else failed.

#### 55.8.5.2 status\_t `WM8904_ReadRegister` ( `wm8904_handle_t * handle, uint8_t reg, uint16_t * value` )

Parameters

|               |                          |
|---------------|--------------------------|
| <i>handle</i> | WM8904 handle structure. |
| <i>reg</i>    | register address.        |
| <i>value</i>  | value to read.           |

Returns

kStatus\_Success, else failed.

#### 55.8.5.3 status\_t WM8904\_ModifyRegister ( *wm8904\_handle\_t \* handle, uint8\_t reg, uint16\_t mask, uint16\_t value* )

Parameters

|               |                          |
|---------------|--------------------------|
| <i>handle</i> | WM8904 handle structure. |
| <i>reg</i>    | register address.        |
| <i>mask</i>   | register bits mask.      |
| <i>value</i>  | value to write.          |

Returns

kStatus\_Success, else failed.

#### 55.8.5.4 status\_t WM8904\_Init ( *wm8904\_handle\_t \* handle, wm8904\_config\_t \* wm8904Config* )

Parameters

|                     |                                 |
|---------------------|---------------------------------|
| <i>handle</i>       | WM8904 handle structure.        |
| <i>wm8904Config</i> | WM8904 configuration structure. |

#### 55.8.5.5 status\_t WM8904\_Deinit ( *wm8904\_handle\_t \* handle* )

This function resets WM8904.

Parameters

|               |                          |
|---------------|--------------------------|
| <i>handle</i> | WM8904 handle structure. |
|---------------|--------------------------|

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.6 void WM8904\_GetDefaultConfig ( *wm8904\_config\_t \* config* )

The default values are:

```
master = false; protocol = kWM8904_ProtocolI2S; format.fsRatio = kWM8904_FsRatio64X; format.-sampleRate = kWM8904_SampleRate48kHz; format.bitWidth = kWM8904_BitWidth16;
```

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>config</i> | default configurations of wm8904. |
|---------------|-----------------------------------|

#### 55.8.5.7 status\_t WM8904\_SetMasterSlave ( *wm8904\_handle\_t \* handle, bool master* )

**Deprecated** DO NOT USE THIS API ANYMORE. IT HAS BEEN SUPERCEDED BY [WM8904\\_SetMasterClock](#)

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>handle</i> | WM8904 handle structure.          |
| <i>master</i> | true for master, false for slave. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.8 status\_t WM8904\_SetMasterClock ( *wm8904\_handle\_t \* handle, uint32\_t sysclk, uint32\_t sampleRate, uint32\_t bitWidth* )

User should pay attention to the sysclk parameter ,When using external MCLK as system clock source, the value should be frequency of MCLK, when using FLL as system clock source, the value should be frequency of the output of FLL.

Parameters

|                   |                                |
|-------------------|--------------------------------|
| <i>handle</i>     | WM8904 handle structure.       |
| <i>sysclk</i>     | system clock source frequency. |
| <i>sampleRate</i> | sample rate                    |
| <i>bitWidth</i>   | bit width                      |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.9 status\_t WM8904\_SetFLLConfig ( *wm8904\_handle\_t \* handle,* *wm8904\_fll\_config\_t \* config* )

Parameters

|               |                            |
|---------------|----------------------------|
| <i>handle</i> | wm8904 handler pointer.    |
| <i>config</i> | FLL configuration pointer. |

#### 55.8.5.10 status\_t WM8904\_SetProtocol ( *wm8904\_handle\_t \* handle,* *wm8904\_protocol\_t protocol* )

Parameters

|                 |                          |
|-----------------|--------------------------|
| <i>handle</i>   | WM8904 handle structure. |
| <i>protocol</i> | Audio transfer protocol. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.11 status\_t WM8904\_SetAudioFormat ( *wm8904\_handle\_t \* handle, uint32\_t sysclk, uint32\_t sampleRate, uint32\_t bitWidth* )

User should pay attention to the sysclk parameter ,When using external MCLK as system clock source, the value should be frequency of MCLK, when using FLL as system clock source, the value should be frequency of the output of FLL.

Parameters

|                   |                                |
|-------------------|--------------------------------|
| <i>handle</i>     | WM8904 handle structure.       |
| <i>sysclk</i>     | system clock source frequency. |
| <i>sampleRate</i> | Sample rate frequency in Hz.   |
| <i>bitWidth</i>   | Audio data bit width.          |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.12 status\_t WM8904\_CheckAudioFormat ( *wm8904\_handle\_t \* handle*, *wm8904\_audio\_format\_t \* format*, *uint32\_t mclkFreq* )

This api is used check the fsRatio setting based on the mclk and sample rate, if fsRatio setting is not correct, it will correct it according to mclk and sample rate.

Parameters

|                 |                          |
|-----------------|--------------------------|
| <i>handle</i>   | WM8904 handle structure. |
| <i>format</i>   | audio data format        |
| <i>mclkFreq</i> | mclk frequency           |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.13 status\_t WM8904\_SetVolume ( *wm8904\_handle\_t \* handle*, *uint16\_t volumeLeft*, *uint16\_t volumeRight* )

The parameter should be from 0 to 63. The resulting volume will be. 0 for -57DB, 63 for 6DB.

Parameters

|               |                          |
|---------------|--------------------------|
| <i>handle</i> | WM8904 handle structure. |
|---------------|--------------------------|

|                    |                       |
|--------------------|-----------------------|
| <i>volumeLeft</i>  | left channel volume.  |
| <i>volumeRight</i> | right channel volume. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.14 status\_t WM8904\_SetMute ( *wm8904\_handle\_t \* handle, bool muteLeft, bool muteRight* )

Parameters

|                  |                                              |
|------------------|----------------------------------------------|
| <i>handle</i>    | WM8904 handle structure.                     |
| <i>muteLeft</i>  | true to mute left channel, false to unmute.  |
| <i>muteRight</i> | true to mute right channel, false to unmute. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.15 status\_t WM8904\_SelectLRCPolarity ( *wm8904\_handle\_t \* handle, uint32\_t polarity* )

Parameters

|                 |                          |
|-----------------|--------------------------|
| <i>handle</i>   | WM8904 handle structure. |
| <i>polarity</i> | LRC clock polarity.      |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.16 status\_t WM8904\_EnableDACTDMMode ( *wm8904\_handle\_t \* handle, wm8904\_timeslot\_t timeSlot* )

Parameters

|                 |                          |
|-----------------|--------------------------|
| <i>handle</i>   | WM8904 handle structure. |
| <i>timeSlot</i> | timeslot number.         |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.17 status\_t WM8904\_EnableADCTDMMMode ( *wm8904\_handle\_t \* handle,* *wm8904\_timeslot\_t timeSlot* )

Parameters

|                 |                          |
|-----------------|--------------------------|
| <i>handle</i>   | WM8904 handle structure. |
| <i>timeSlot</i> | timeslot number.         |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.18 status\_t WM8904\_SetModulePower ( *wm8904\_handle\_t \* handle,* *wm8904\_module\_t module, bool isEnabled* )

Parameters

|                                |                                   |
|--------------------------------|-----------------------------------|
| <i>handle</i>                  | WM8904 handle structure.          |
| <i>module</i>                  | wm8904 module.                    |
| <i>isEnabled</i> , <i>true</i> | is power on, false is power down. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise..

#### 55.8.5.19 status\_t WM8904\_SetDACVolume ( *wm8904\_handle\_t \* handle, uint8\_t volume* *)*

Parameters

|               |                          |
|---------------|--------------------------|
| <i>handle</i> | WM8904 handle structure. |
| <i>volume</i> | volume to be configured. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise..

#### 55.8.5.20 status\_t WM8904\_SetChannelVolume ( *wm8904\_handle\_t \* handle, uint32\_t channel, uint32\_t volume* )

The parameter should be from 0 to 63. The resulting volume will be. 0 for -57dB, 63 for 6DB.

Parameters

|                |                          |
|----------------|--------------------------|
| <i>handle</i>  | codec handle structure.  |
| <i>channel</i> | codec channel.           |
| <i>volume</i>  | volume value from 0 -63. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.21 status\_t WM8904\_SetRecord ( *wm8904\_handle\_t \* handle, uint32\_t recordSource* )

Parameters

|                     |                                                                                                                                                                                                      |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i>       | WM8904 handle structure.                                                                                                                                                                             |
| <i>recordSource</i> | record source , can be a value of kCODEC_ModuleRecordSourceDifferential-Line, kCODEC_ModuleRecordSourceDifferentialMic, kCODEC_ModuleRecord-SourceSingleEndMic, kCODEC_ModuleRecordSourceDigitalMic. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise.

#### 55.8.5.22 status\_t WM8904\_SetRecordChannel ( *wm8904\_handle\_t \* handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel* )

Parameters

|                            |                                                                                                                                                                                                            |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i>              | WM8904 handle structure.                                                                                                                                                                                   |
| <i>leftRecord-Channel</i>  | channel number of left record channel when using differential source, channel number of single end left channel when using single end source, channel number of digital mic when using digital mic source. |
| <i>rightRecord-Channel</i> | channel number of right record channel when using differential source, channel number of single end right channel when using single end source.                                                            |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise..

#### 55.8.5.23 status\_t WM8904\_SetPlay ( **wm8904\_handle\_t \* handle, uint32\_t playSource** )

Parameters

|                   |                                                                                                                                                                 |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i>     | WM8904 handle structure.                                                                                                                                        |
| <i>playSource</i> | play source , can be a value of kCODEC_ModuleHeadphoneSourcePGA, kCODEC_ModuleHeadphoneSourceDAC, kCODEC_ModuleLineoutSourcePGA, kCODEC_ModuleLineoutSourceDAC. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise..

#### 55.8.5.24 status\_t WM8904\_SetChannelMute ( **wm8904\_handle\_t \* handle, uint32\_t channel, bool isMute** )

Parameters

|                |                             |
|----------------|-----------------------------|
| <i>handle</i>  | codec handle structure.     |
| <i>channel</i> | codec module name.          |
| <i>isMute</i>  | true is mute, false unmute. |

Returns

kStatus\_WM8904\_Success if successful, different code otherwise..

## 55.8.6 WM8904 Adapter

### 55.8.6.1 Overview

The wm8904 adapter provides a codec unify control interface.

#### Macros

- #define `HAL_CODEC_WM8904_HANDLER_SIZE` (`WM8904_I2C_HANDLER_SIZE + 4`)  
*codec handler size*

#### Functions

- `status_t HAL_CODEC_WM8904_Init` (void \*handle, void \*config)  
*Codec initialization.*
- `status_t HAL_CODEC_WM8904_Deinit` (void \*handle)  
*Codec de-initilization.*
- `status_t HAL_CODEC_WM8904_SetFormat` (void \*handle, uint32\_t mclk, uint32\_t sampleRate, uint32\_t bitWidth)  
*set audio data format.*
- `status_t HAL_CODEC_WM8904_SetVolume` (void \*handle, uint32\_t playChannel, uint32\_t volume)  
*set audio codec module volume.*
- `status_t HAL_CODEC_WM8904_SetMute` (void \*handle, uint32\_t playChannel, bool isMute)  
*set audio codec module mute.*
- `status_t HAL_CODEC_WM8904_SetPower` (void \*handle, uint32\_t module, bool powerOn)  
*set audio codec module power.*
- `status_t HAL_CODEC_WM8904_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- `status_t HAL_CODEC_WM8904_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- `status_t HAL_CODEC_WM8904_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- `status_t HAL_CODEC_WM8904_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*
- static `status_t HAL_CODEC_Init` (void \*handle, void \*config)  
*Codec initilization.*
- static `status_t HAL_CODEC_Deinit` (void \*handle)  
*Codec de-initilization.*
- static `status_t HAL_CODEC_SetFormat` (void \*handle, uint32\_t mclk, uint32\_t sampleRate, uint32\_t bitWidth)  
*set audio data format.*
- static `status_t HAL_CODEC_SetVolume` (void \*handle, uint32\_t playChannel, uint32\_t volume)  
*set audio codec module volume.*
- static `status_t HAL_CODEC_SetMute` (void \*handle, uint32\_t playChannel, bool isMute)  
*set audio codec module mute.*
- static `status_t HAL_CODEC_SetPower` (void \*handle, uint32\_t module, bool powerOn)

- static `status_t HAL_CODEC_SetRecord` (void \*handle, uint32\_t recordSource)  
*codec set record source.*
- static `status_t HAL_CODEC_SetRecordChannel` (void \*handle, uint32\_t leftRecordChannel, uint32\_t rightRecordChannel)  
*codec set record channel.*
- static `status_t HAL_CODEC_SetPlay` (void \*handle, uint32\_t playSource)  
*codec set play source.*
- static `status_t HAL_CODEC_ModuleControl` (void \*handle, uint32\_t cmd, uint32\_t data)  
*codec module control.*

## 55.8.6.2 Function Documentation

### 55.8.6.2.1 `status_t HAL_CODEC_WM8904_Init( void * handle, void * config )`

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | codec handle.        |
| <i>config</i> | codec configuration. |

Returns

kStatus\_Success is success, else initial failed.

### 55.8.6.2.2 `status_t HAL_CODEC_WM8904_Deinit( void * handle )`

Parameters

|               |               |
|---------------|---------------|
| <i>handle</i> | codec handle. |
|---------------|---------------|

Returns

kStatus\_Success is success, else de-initial failed.

### 55.8.6.2.3 `status_t HAL_CODEC_WM8904_SetFormat( void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth )`

Parameters

|                   |                               |
|-------------------|-------------------------------|
| <i>handle</i>     | codec handle.                 |
| <i>mclk</i>       | master clock frequency in HZ. |
| <i>sampleRate</i> | sample rate in HZ.            |
| <i>bitWidth</i>   | bit width.                    |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.4 status\_t HAL\_CODEC\_WM8904\_SetVolume ( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* )

Parameters

|                    |                                                                                   |
|--------------------|-----------------------------------------------------------------------------------|
| <i>handle</i>      | codec handle.                                                                     |
| <i>playChannel</i> | audio codec play channel, can be a value or combine value of _codec_play_channel. |
| <i>volume</i>      | volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.        |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.5 status\_t HAL\_CODEC\_WM8904\_SetMute ( void \* *handle*, uint32\_t *playChannel*, bool *isMute* )

Parameters

|                    |                                                                                   |
|--------------------|-----------------------------------------------------------------------------------|
| <i>handle</i>      | codec handle.                                                                     |
| <i>playChannel</i> | audio codec play channel, can be a value or combine value of _codec_play_channel. |
| <i>isMute</i>      | true is mute, false is unmute.                                                    |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.6 status\_t HAL\_CODEC\_WM8904\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* )

Parameters

|                |                                        |
|----------------|----------------------------------------|
| <i>handle</i>  | codec handle.                          |
| <i>module</i>  | audio codec module.                    |
| <i>powerOn</i> | true is power on, false is power down. |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.7 status\_t HAL\_CODEC\_WM8904\_SetRecord ( void \* *handle*, uint32\_t *recordSource* )

Parameters

|                     |                                                                                     |
|---------------------|-------------------------------------------------------------------------------------|
| <i>handle</i>       | codec handle.                                                                       |
| <i>recordSource</i> | audio codec record source, can be a value or combine value of _codec_record_source. |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.8 status\_t HAL\_CODEC\_WM8904\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* )

Parameters

|                            |                                                                                                                                  |
|----------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i>              | codec handle.                                                                                                                    |
| <i>leftRecord-Channel</i>  | audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel. |
| <i>rightRecord-Channel</i> | audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.          |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.9 status\_t HAL\_CODEC\_WM8904\_SetPlay ( void \* *handle*, uint32\_t *playSource* )

Parameters

|                   |                                                                                 |
|-------------------|---------------------------------------------------------------------------------|
| <i>handle</i>     | codec handle.                                                                   |
| <i>playSource</i> | audio codec play source, can be a value or combine value of _codec_play_source. |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.10 status\_t HAL\_CODEC\_WM8904\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* )

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

|               |                                                                                                                                                                                                                                                                       |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i> | codec handle.                                                                                                                                                                                                                                                         |
| <i>cmd</i>    | module control cmd, reference _codec_module_ctrl_cmd.                                                                                                                                                                                                                 |
| <i>data</i>   | value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations. |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.11 static status\_t HAL\_CODEC\_Init ( void \* *handle*, void \* *config* ) [inline], [static]

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | codec handle.        |
| <i>config</i> | codec configuration. |

Returns

kStatus\_Success is success, else initial failed.

#### 55.8.6.2.12 static status\_t HAL\_CODEC\_Deinit ( void \* *handle* ) [inline], [static]

Parameters

|               |               |
|---------------|---------------|
| <i>handle</i> | codec handle. |
|---------------|---------------|

Returns

kStatus\_Success is success, else de-initial failed.

#### 55.8.6.2.13 static status\_t HAL\_CODEC\_SetFormat( void \* *handle*, uint32\_t *mclk*, uint32\_t *sampleRate*, uint32\_t *bitWidth* ) [inline], [static]

Parameters

|                   |                               |
|-------------------|-------------------------------|
| <i>handle</i>     | codec handle.                 |
| <i>mclk</i>       | master clock frequency in HZ. |
| <i>sampleRate</i> | sample rate in HZ.            |
| <i>bitWidth</i>   | bit width.                    |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.14 static status\_t HAL\_CODEC\_SetVolume( void \* *handle*, uint32\_t *playChannel*, uint32\_t *volume* ) [inline], [static]

Parameters

|                    |                                                                                   |
|--------------------|-----------------------------------------------------------------------------------|
| <i>handle</i>      | codec handle.                                                                     |
| <i>playChannel</i> | audio codec play channel, can be a value or combine value of _codec_play_channel. |
| <i>volume</i>      | volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.        |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.15 static status\_t HAL\_CODEC\_SetMute( void \* *handle*, uint32\_t *playChannel*, bool *isMute* ) [inline], [static]

Parameters

|                    |                                                                                   |
|--------------------|-----------------------------------------------------------------------------------|
| <i>handle</i>      | codec handle.                                                                     |
| <i>playChannel</i> | audio codec play channel, can be a value or combine value of _codec_play_channel. |
| <i>isMute</i>      | true is mute, false is unmute.                                                    |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.16 static status\_t HAL\_CODEC\_SetPower ( void \* *handle*, uint32\_t *module*, bool *powerOn* ) [inline], [static]

Parameters

|                |                                        |
|----------------|----------------------------------------|
| <i>handle</i>  | codec handle.                          |
| <i>module</i>  | audio codec module.                    |
| <i>powerOn</i> | true is power on, false is power down. |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.17 static status\_t HAL\_CODEC\_SetRecord ( void \* *handle*, uint32\_t *recordSource* ) [inline], [static]

Parameters

|                     |                                                                                     |
|---------------------|-------------------------------------------------------------------------------------|
| <i>handle</i>       | codec handle.                                                                       |
| <i>recordSource</i> | audio codec record source, can be a value or combine value of _codec_record_source. |

Returns

kStatus\_Success is success, else configure failed.

#### 55.8.6.2.18 static status\_t HAL\_CODEC\_SetRecordChannel ( void \* *handle*, uint32\_t *leftRecordChannel*, uint32\_t *rightRecordChannel* ) [inline], [static]

Parameters

|                            |                                                                                                                                  |
|----------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i>              | codec handle.                                                                                                                    |
| <i>leftRecord-Channel</i>  | audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel. |
| <i>rightRecord-Channel</i> | audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.          |

Returns

kStatus\_Success is success, else configure failed.

**55.8.6.2.19 static status\_t HAL\_CODEC\_SetPlay ( void \* *handle*, uint32\_t *playSource* ) [inline], [static]**

Parameters

|                   |                                                                                 |
|-------------------|---------------------------------------------------------------------------------|
| <i>handle</i>     | codec handle.                                                                   |
| <i>playSource</i> | audio codec play source, can be a value or combine value of _codec_play_source. |

Returns

kStatus\_Success is success, else configure failed.

**55.8.6.2.20 static status\_t HAL\_CODEC\_ModuleControl ( void \* *handle*, uint32\_t *cmd*, uint32\_t *data* ) [inline], [static]**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

|               |                                                                                                                                                                                                                                                                       |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i> | codec handle.                                                                                                                                                                                                                                                         |
| <i>cmd</i>    | module control cmd, reference _codec_module_ctrl_cmd.                                                                                                                                                                                                                 |
| <i>data</i>   | value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations. |

Returns

kStatus\_Success is success, else configure failed.

# Chapter 56

## Serial Manager

### 56.1 Overview

This chapter describes the programming interface of the serial manager component.

The serial manager component provides a series of APIs to operate different serial port types. The port types it supports are UART, USB CDC and SWO.

### Modules

- [Serial Port SWO](#)
- [Serial Port USB](#)
- [Serial Port Uart](#)

### Data Structures

- struct [serial\\_manager\\_config\\_t](#)  
*serial manager config structure* [More...](#)
- struct [serial\\_manager\\_callback\\_message\\_t](#)  
*Callback message structure.* [More...](#)

### Macros

- #define [SERIAL\\_MANAGER\\_NON\\_BLOCKING\\_MODE](#) (1U)  
*Enable or disable serial manager non-blocking mode (1 - enable, 0 - disable)*
- #define [SERIAL\\_MANAGER\\_RING\\_BUFFER\\_FLOWCONTROL](#) (0U)  
*Enable or ring buffer flow control (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_UART](#) (0U)  
*Enable or disable uart port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_UART\\_DMA](#) (0U)  
*Enable or disable uart dma port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_USBCDC](#) (0U)  
*Enable or disable USB CDC port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_SWO](#) (0U)  
*Enable or disable SWO port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_VIRTUAL](#) (0U)  
*Enable or disable USB CDC virtual port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_RPMSG](#) (0U)  
*Enable or disable rpmsg port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_SPI\\_MASTER](#) (0U)  
*Enable or disable SPI Master port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_SPI\\_SLAVE](#) (0U)  
*Enable or disable SPI Slave port (1 - enable, 0 - disable)*
- #define [SERIAL\\_PORT\\_TYPE\\_BLE\\_WU](#) (0U)  
*Enable or disable BLE WU port (1 - enable, 0 - disable)*

- **#define SERIAL\_MANAGER\_TASK\_HANDLE\_TX (0U)**  
*Enable or disable SerialManager\_Task() handle TX to prevent recursive calling.*
- **#define SERIAL\_MANAGER\_WRITE\_TIME\_DELAY\_DEFAULT\_VALUE (1U)**  
*Set the default delay time in ms used by SerialManager\_WriteTimeDelay().*
- **#define SERIAL\_MANAGER\_READ\_TIME\_DELAY\_DEFAULT\_VALUE (1U)**  
*Set the default delay time in ms used by SerialManager\_ReadTimeDelay().*
- **#define SERIAL\_MANAGER\_TASK\_HANDLE\_RX\_AVAILABLE\_NOTIFY (0U)**  
*Enable or disable SerialManager\_Task() handle RX data available notify.*
- **#define SERIAL\_MANAGER\_WRITE\_HANDLE\_SIZE (44U)**  
*Set serial manager write handle size.*
- **#define SERIAL\_MANAGER\_USE\_COMMON\_TASK (0U)**  
*SERIAL\_PORT\_UART\_HANDLE\_SIZE/SERIAL\_PORT\_USB\_CDC\_HANDLE\_SIZE + serial manager dedicated size.*
- **#define SERIAL\_MANAGER\_HANDLE\_SIZE (SERIAL\_MANAGER\_HANDLE\_SIZE\_TEMP + 124U)**  
*Definition of serial manager handle size.*
- **#define SERIAL\_MANAGER\_HANDLE\_DEFINE(name) uint32\_t name[((SERIAL\_MANAGER\_HANDLE\_SIZE + sizeof(uint32\_t) - 1U) / sizeof(uint32\_t))]**  
*Defines the serial manager handle.*
- **#define SERIAL\_MANAGER\_WRITE\_HANDLE\_DEFINE(name) uint32\_t name[((SERIAL\_MANAGER\_WRITE\_HANDLE\_SIZE + sizeof(uint32\_t) - 1U) / sizeof(uint32\_t))]**  
*Defines the serial manager write handle.*
- **#define SERIAL\_MANAGER\_READ\_HANDLE\_DEFINE(name) uint32\_t name[((SERIAL\_MANAGER\_READ\_HANDLE\_SIZE + sizeof(uint32\_t) - 1U) / sizeof(uint32\_t))]**  
*Defines the serial manager read handle.*
- **#define SERIAL\_MANAGER\_TASK\_PRIORITY (2U)**  
*Macro to set serial manager task priority.*
- **#define SERIAL\_MANAGER\_TASK\_STACK\_SIZE (1000U)**  
*Macro to set serial manager task stack size.*

## Typedefs

- **typedef void \* serial\_handle\_t**  
*The handle of the serial manager module.*
- **typedef void \* serial\_write\_handle\_t**  
*The write handle of the serial manager module.*
- **typedef void \* serial\_read\_handle\_t**  
*The read handle of the serial manager module.*
- **typedef void(\* serial\_manager\_callback\_t )(void \*callbackParam, serial\_manager\_callback\_message\_t \*message, serial\_manager\_status\_t status)**  
*serial manager callback function*
- **typedef int32\_t(\* serial\_manager\_lowpower\_critical\_callback\_t )(int32\_t power\_mode)**  
*serial manager Lowpower Critical callback function*

## Enumerations

- enum `serial_port_type_t` {
   
    `kSerialPort_None` = 0U,
   
    `kSerialPort_Uart` = 1U,
   
    `kSerialPort_UsbCdc`,
   
    `kSerialPort_Swo`,
   
    `kSerialPort_Virtual`,
   
    `kSerialPort_Rpmsg`,
   
    `kSerialPort_UartDma`,
   
    `kSerialPort_SpiMaster`,
   
    `kSerialPort_SpiSlave`,
   
    `kSerialPort_BleWu` }
   
    *serial port type*
- enum `serial_manager_type_t` {
   
    `kSerialManager_NonBlocking` = 0x0U,
   
    `kSerialManager_Blocking` = 0x8F41U }
   
    *serial manager type*
- enum `serial_manager_status_t` {
   
    `kStatus_SerialManager_Success` = `kStatus_Success`,
   
    `kStatus_SerialManager_Error` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 1)`,
   
    `kStatus_SerialManager_Busy` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 2)`,
   
    `kStatus_SerialManager_Notify` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 3)`,
   
    `kStatus_SerialManager_Canceled`,
   
    `kStatus_SerialManager_HandleConflict` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 5)`,
   
    `kStatus_SerialManager_RingBufferOverflow`,
   
    `kStatus_SerialManager_NotConnected` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 7)` }
   
    *serial manager error code*

## Functions

- `serial_manager_status_t SerialManager_Init (serial_handle_t serialHandle, const serial_manager_config_t *config)`

*Initializes a serial manager module with the serial manager handle and the user configuration structure.*
- `serial_manager_status_t SerialManager_Deinit (serial_handle_t serialHandle)`

*De-initializes the serial manager module instance.*
- `serial_manager_status_t SerialManager_OpenWriteHandle (serial_handle_t serialHandle, serial_write_handle_t writeHandle)`

*Opens a writing handle for the serial manager module.*
- `serial_manager_status_t SerialManager_CloseWriteHandle (serial_write_handle_t writeHandle)`

*Closes a writing handle for the serial manager module.*
- `serial_manager_status_t SerialManager_OpenReadHandle (serial_handle_t serialHandle, serial_read_handle_t readHandle)`

*Opens a reading handle for the serial manager module.*
- `serial_manager_status_t SerialManager_CloseReadHandle (serial_read_handle_t readHandle)`

*Closes a reading for the serial manager module.*

- `serial_manager_status_t SerialManager_WriteBlocking (serial_write_handle_t writeHandle, uint8_t *buffer, uint32_t length)`  
*Transmits data with the blocking mode.*
- `serial_manager_status_t SerialManager_ReadBlocking (serial_read_handle_t readHandle, uint8_t *buffer, uint32_t length)`  
*Reads data with the blocking mode.*
- `serial_manager_status_t SerialManager_WriteNonBlocking (serial_write_handle_t writeHandle, uint8_t *buffer, uint32_t length)`  
*Transmits data with the non-blocking mode.*
- `serial_manager_status_t SerialManager_ReadNonBlocking (serial_read_handle_t readHandle, uint8_t *buffer, uint32_t length)`  
*Reads data with the non-blocking mode.*
- `serial_manager_status_t SerialManager_TryRead (serial_read_handle_t readHandle, uint8_t *buffer, uint32_t length, uint32_t *receivedLength)`  
*Tries to read data.*
- `serial_manager_status_t SerialManager_CancelWriting (serial_write_handle_t writeHandle)`  
*Cancels unfinished send transmission.*
- `serial_manager_status_t SerialManager_CancelReading (serial_read_handle_t readHandle)`  
*Cancels unfinished receive transmission.*
- `serial_manager_status_t SerialManager_InstallTxCallback (serial_write_handle_t writeHandle, serial_manager_callback_t callback, void *callbackParam)`  
*Installs a TX callback and callback parameter.*
- `serial_manager_status_t SerialManager_InstallRxCallback (serial_read_handle_t readHandle, serial_manager_callback_t callback, void *callbackParam)`  
*Installs a RX callback and callback parameter.*
- `static bool SerialManager_needPollingIsr (void)`  
*Check if need polling ISR.*
- `serial_manager_status_t SerialManager_EnterLowpower (serial_handle_t serialHandle)`  
*Prepares to enter low power consumption.*
- `serial_manager_status_t SerialManager_ExitLowpower (serial_handle_t serialHandle)`  
*Restores from low power consumption.*
- `void SerialManager_SetLowpowerCriticalCb (const serial_manager_lowpower_critical_CBs_t *pfnCallback)`  
*This function performs initialization of the callbacks structure used to disable lowpower when serial manager is active.*

## 56.2 Data Structure Documentation

### 56.2.1 struct serial\_manager\_config\_t

#### Data Fields

- `uint8_t * ringBuffer`  
*Ring buffer address, it is used to buffer data received by the hardware.*
- `uint32_t ringBufferSize`  
*The size of the ring buffer.*
- `serial_port_type_t type`  
*Serial port type.*
- `serial_manager_type_t blockType`

- *Serial manager port type.*
- `void * portConfig`  
*Serial port configuration.*

## Field Documentation

### (1) `uint8_t* serial_manager_config_t::ringBuffer`

Besides, the memory space cannot be free during the lifetime of the serial manager module.

## 56.2.2 `struct serial_manager_callback_message_t`

### Data Fields

- `uint8_t * buffer`  
*Transferred buffer.*
- `uint32_t length`  
*Transferred data length.*

## 56.3 Macro Definition Documentation

### 56.3.1 `#define SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE (1U)`

### 56.3.2 `#define SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE (1U)`

### 56.3.3 `#define SERIAL_MANAGER_USE_COMMON_TASK (0U)`

Macro to determine whether use common task.

### 56.3.4 `#define SERIAL_MANAGER_HANDLE_SIZE (SERIAL_MANAGER_HANDLE_SIZE_TEMP + 124U)`

### 56.3.5 `#define SERIAL_MANAGER_HANDLE_DEFINE( name ) uint32_t name[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`

This macro is used to define a 4 byte aligned serial manager handle. Then use "(serial\_handle\_t)name" to get the serial manager handle.

The macro should be global and could be optional. You could also define serial manager handle by yourself.

This is an example,

```
* SERIAL_MANAGER_HANDLE_DEFINE(serialManagerHandle);
*
```

## Parameters

|             |                                               |
|-------------|-----------------------------------------------|
| <i>name</i> | The name string of the serial manager handle. |
|-------------|-----------------------------------------------|

**56.3.6 #define SERIAL\_MANAGER\_WRITE\_HANDLE\_DEFINE( *name* ) uint32\_t  
*name*[((SERIAL\_MANAGER\_WRITE\_HANDLE\_SIZE + sizeof(uint32\_t) -  
1U) / sizeof(uint32\_t))]**

This macro is used to define a 4 byte aligned serial manager write handle. Then use "(serial\_write\_handle\_t)*name*" to get the serial manager write handle.

The macro should be global and could be optional. You could also define serial manager write handle by yourself.

This is an example,

```
* SERIAL_MANAGER_WRITE_HANDLE_DEFINE(serialManagerwriteHandle);
*
```

## Parameters

|             |                                                     |
|-------------|-----------------------------------------------------|
| <i>name</i> | The name string of the serial manager write handle. |
|-------------|-----------------------------------------------------|

**56.3.7 #define SERIAL\_MANAGER\_READ\_HANDLE\_DEFINE( *name* ) uint32\_t  
*name*[((SERIAL\_MANAGER\_READ\_HANDLE\_SIZE + sizeof(uint32\_t) - 1U) /  
sizeof(uint32\_t))]**

This macro is used to define a 4 byte aligned serial manager read handle. Then use "(serial\_read\_handle\_t)*name*" to get the serial manager read handle.

The macro should be global and could be optional. You could also define serial manager read handle by yourself.

This is an example,

```
* SERIAL_MANAGER_READ_HANDLE_DEFINE(serialManagerReadHandle);
*
```

Parameters

|             |                                                    |
|-------------|----------------------------------------------------|
| <i>name</i> | The name string of the serial manager read handle. |
|-------------|----------------------------------------------------|

### 56.3.8 #define SERIAL\_MANAGER\_TASK\_PRIORITY (2U)

### 56.3.9 #define SERIAL\_MANAGER\_TASK\_STACK\_SIZE (1000U)

## 56.4 Enumeration Type Documentation

### 56.4.1 enum serial\_port\_type\_t

Enumerator

- kSerialPort\_None* Serial port is none.
- kSerialPort\_Uart* Serial port UART.
- kSerialPort\_UsbCdc* Serial port USB CDC.
- kSerialPort\_Swo* Serial port SWO.
- kSerialPort\_Virtual* Serial port Virtual.
- kSerialPort\_Rpmsg* Serial port RPMSG.
- kSerialPort\_UartDma* Serial port UART DMA.
- kSerialPort\_SpiMaster* Serial port SPIMASTER.
- kSerialPort\_SpiSlave* Serial port SPISLAVE.
- kSerialPort\_BleWu* Serial port BLE WU.

### 56.4.2 enum serial\_manager\_type\_t

Enumerator

- kSerialManager\_NonBlocking* None blocking handle.
- kSerialManager\_Blocking* Blocking handle.

### 56.4.3 enum serial\_manager\_status\_t

Enumerator

- kStatus\_SerialManager\_Success* Success.
- kStatus\_SerialManager\_Error* Failed.
- kStatus\_SerialManager\_Busy* Busy.
- kStatus\_SerialManager\_Notify* Ring buffer is not empty.
- kStatus\_SerialManager\_Canceled* the non-blocking request is canceled

**kStatus\_SerialManager\_HandleConflict** The handle is opened.

**kStatus\_SerialManager\_RingBufferOverflow** The ring buffer is overflowed.

**kStatus\_SerialManager\_NotConnected** The host is not connected.

## 56.5 Function Documentation

### 56.5.1 `serial_manager_status_t SerialManager_Init ( serial_handle_t serialHandle, const serial_manager_config_t * config )`

This function configures the Serial Manager module with user-defined settings. The user can configure the configuration structure. The parameter `serialHandle` is a pointer to point to a memory space of size `SERIAL_MANAGER_HANDLE_SIZE` allocated by the caller. The Serial Manager module supports three types of serial port, UART (includes UART, USART, LPSCI, LPUART, etc), USB CDC and swo. Please refer to `serial_port_type_t` for serial port setting. These three types can be set by using `serial_manager_config_t`.

Example below shows how to use this API to configure the Serial Manager. For UART,

```
* #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
* static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
* static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
* serial_manager_config_t config;
* serial_port_uart_config_t uartConfig;
* config.type = kSerialPort_Uart;
* config.ringBuffer = &s_ringBuffer[0];
* config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
* uartConfig.instance = 0;
* uartConfig.clockRate = 24000000;
* uartConfig.baudRate = 115200;
* uartConfig.parityMode = kSerialManager_UartParityDisabled;
* uartConfig.stopBitCount = kSerialManager_UartOneStopBit;
* uartConfig.enableRx = 1;
* uartConfig.enableTx = 1;
* uartConfig.enableRxRTS = 0;
* uartConfig.enableTxCTS = 0;
* config.portConfig = &uartConfig;
* SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*
```

For USB CDC,

```
* #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
* static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
* static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
* serial_manager_config_t config;
* serial_port_usb_cdc_config_t usbCdcConfig;
* config.type = kSerialPort_UsbCdc;
* config.ringBuffer = &s_ringBuffer[0];
* config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
* usbCdcConfig.controllerIndex =
    kSerialManager_UsbControllerKhci0;
* config.portConfig = &usbCdcConfig;
* SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*
```

Parameters

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>serialHandle</i> | Pointer to point to a memory space of size <a href="#">S SERIAL_MANAGER_HANDLE_SIZE</a> allocated by the caller. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: <a href="#">S SERIAL_MANAGER_HANDLE_DEFINE(serialHandle)</a> ; or <code>uint32_t serialHandle[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code> |
| <i>config</i>       | Pointer to user-defined configuration structure.                                                                                                                                                                                                                                                                                                                                                                                                           |

Return values

|                                      |                                                   |
|--------------------------------------|---------------------------------------------------|
| <i>kStatus_SerialManager_Error</i>   | An error occurred.                                |
| <i>kStatus_SerialManager_Success</i> | The Serial Manager module initialization succeed. |

### 56.5.2 **serial\_manager\_status\_t SerialManager\_Deinit ( serial\_handle\_t serialHandle )**

This function de-initializes the serial manager module instance. If the opened writing or reading handle is not closed, the function will return `kStatus_SerialManager_Busy`.

Parameters

|                     |                                           |
|---------------------|-------------------------------------------|
| <i>serialHandle</i> | The serial manager module handle pointer. |
|---------------------|-------------------------------------------|

Return values

|                                      |                                                 |
|--------------------------------------|-------------------------------------------------|
| <i>kStatus_SerialManager_Success</i> | The serial manager de-initialization succeed.   |
| <i>kStatus_SerialManager_Busy</i>    | Opened reading or writing handle is not closed. |

### 56.5.3 **serial\_manager\_status\_t SerialManager\_OpenWriteHandle ( serial\_handle\_t serialHandle, serial\_write\_handle\_t writeHandle )**

This function Opens a writing handle for the serial manager module. If the serial manager needs to be used in different tasks, the task should open a dedicated write handle for itself by calling [SerialManager\\_OpenWriteHandle](#). Since there can only one buffer for transmission for the writing handle at the same time, multiple writing handles need to be opened when the multiple transmission is needed for a task.

## Parameters

|                     |                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>serialHandle</i> | The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.                                                                                                                                                                                                                                                       |
| <i>writeHandle</i>  | The serial manager module writing handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: <a href="#">SERIAL_MANAGER_WRITE_HANDLE_DEFINE(writeHandle)</a> ; or <code>uint32_t writeHandle[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code> |

## Return values

|                                             |                                |
|---------------------------------------------|--------------------------------|
| <i>kStatus_SerialManager_Error</i>          | An error occurred.             |
| <i>kStatus_SerialManager_HandleConflict</i> | The writing handle was opened. |
| <i>kStatus_SerialManager_Success</i>        | The writing handle is opened.  |

Example below shows how to use this API to write data. For task 1,

```
* static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle1);
* static uint8_t s_nonBlockingWelcome1[] = "This is non-blocking writing log for task1!\r\n";
* SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
*     , (serial_write_handle_t)s_serialWriteHandle1);
* SerialManager_InstallTxCallback()
*     serial_write_handle_t)s_serialWriteHandle1,
*             Task1_SerialManagerTxCallback,
*             s_serialWriteHandle1);
* SerialManager_WriteNonBlocking(
*     serial_write_handle_t)s_serialWriteHandle1,
*             s_nonBlockingWelcome1,
*             sizeof(s_nonBlockingWelcome1) - 1U);
*
*
```

For task 2,

```
* static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle2);
* static uint8_t s_nonBlockingWelcome2[] = "This is non-blocking writing log for task2!\r\n";
* SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
*     , (serial_write_handle_t)s_serialWriteHandle2);
* SerialManager_InstallTxCallback()
*     serial_write_handle_t)s_serialWriteHandle2,
*             Task2_SerialManagerTxCallback,
*             s_serialWriteHandle2);
* SerialManager_WriteNonBlocking(
*     serial_write_handle_t)s_serialWriteHandle2,
*             s_nonBlockingWelcome2,
*             sizeof(s_nonBlockingWelcome2) - 1U);
*
*
```

#### 56.5.4 **serial\_manager\_status\_t SerialManager\_CloseWriteHandle (** **serial\_write\_handle\_t writeHandle )**

This function Closes a writing handle for the serial manager module.

## Parameters

|                    |                                                   |
|--------------------|---------------------------------------------------|
| <i>writeHandle</i> | The serial manager module writing handle pointer. |
|--------------------|---------------------------------------------------|

## Return values

|                                       |                               |
|---------------------------------------|-------------------------------|
| <i>kStatus_SerialManager_-Success</i> | The writing handle is closed. |
|---------------------------------------|-------------------------------|

### 56.5.5 **serial\_manager\_status\_t SerialManager\_OpenReadHandle ( serial\_handle\_t serialHandle, serial\_read\_handle\_t readHandle )**

This function Opens a reading handle for the serial manager module. The reading handle can not be opened multiple at the same time. The error code **kStatus\_SerialManager\_Busy** would be returned when the previous reading handle is not closed. And there can only be one buffer for receiving for the reading handle at the same time.

## Parameters

|                     |                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>serialHandle</i> | The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.                                                                                                                                                                                                                                    |
| <i>readHandle</i>   | The serial manager module reading handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: <b>SERIAL_MANAGER_READ_HANDLE_DEFINE(readHandle)</b> ; or <b>uint32_t readHandle[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</b> |

## Return values

|                                       |                                        |
|---------------------------------------|----------------------------------------|
| <i>kStatus_SerialManager_-Error</i>   | An error occurred.                     |
| <i>kStatus_SerialManager_-Success</i> | The reading handle is opened.          |
| <i>kStatus_SerialManager_-Busy</i>    | Previous reading handle is not closed. |

Example below shows how to use this API to read data.

```
* static SERIAL_MANAGER_READ_HANDLE_DEFINE(s_serialReadHandle);
* SerialManager_OpenReadHandle((serial_handle_t)serialHandle,
*                               (serial_read_handle_t)s_serialReadHandle);
* static uint8_t s_nonBlockingBuffer[64];
* SerialManager_InstallRxCallback(
*   serial_read_handle_t)s_serialReadHandle,
*   APP_SerialManagerRxCallback,
*   s_serialReadHandle);
```

```
*   SerialManager_ReadNonBlocking(
    serial_read_handle_t)s_serialReadHandle,
*
*           s_nonBlockingBuffer,
*           sizeof(s_nonBlockingBuffer));
*
```

### 56.5.6 **serial\_manager\_status\_t SerialManager\_CloseReadHandle ( serial\_read\_handle\_t *readHandle* )**

This function Closes a reading for the serial manager module.

Parameters

|                   |                                                   |
|-------------------|---------------------------------------------------|
| <i>readHandle</i> | The serial manager module reading handle pointer. |
|-------------------|---------------------------------------------------|

Return values

|                                       |                               |
|---------------------------------------|-------------------------------|
| <i>kStatus_SerialManager_-Success</i> | The reading handle is closed. |
|---------------------------------------|-------------------------------|

### 56.5.7 **serial\_manager\_status\_t SerialManager\_WriteBlocking ( serial\_write\_handle\_t *writeHandle*, uint8\_t \* *buffer*, uint32\_t *length* )**

This is a blocking function, which polls the sending queue, waits for the sending queue to be empty. This function sends data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for transmission for the writing handle at the same time.

Note

The function [SerialManager\\_WriteBlocking](#) and the function [SerialManager\\_WriteNonBlocking](#) cannot be used at the same time. And, the function [SerialManager\\_CancelWriting](#) cannot be used to abort the transmission of this function.

Parameters

|                    |                                           |
|--------------------|-------------------------------------------|
| <i>writeHandle</i> | The serial manager module handle pointer. |
|--------------------|-------------------------------------------|

|               |                                     |
|---------------|-------------------------------------|
| <i>buffer</i> | Start address of the data to write. |
| <i>length</i> | Length of the data to write.        |

Return values

|                                       |                                                                  |
|---------------------------------------|------------------------------------------------------------------|
| <i>kStatus_SerialManager_-Success</i> | Successfully sent all data.                                      |
| <i>kStatus_SerialManager_-Busy</i>    | Previous transmission still not finished; data not all sent yet. |
| <i>kStatus_SerialManager_-Error</i>   | An error occurred.                                               |

### 56.5.8 `serial_manager_status_t SerialManager_ReadBlocking ( serial_read_handle_t readHandle, uint8_t * buffer, uint32_t length )`

This is a blocking function, which polls the receiving buffer, waits for the receiving buffer to be full. This function receives data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for receiving for the reading handle at the same time.

Note

The function `SerialManager_ReadBlocking` and the function `SerialManager_ReadNonBlocking` cannot be used at the same time. And, the function `SerialManager_CancelReading` cannot be used to abort the transmission of this function.

Parameters

|                   |                                                       |
|-------------------|-------------------------------------------------------|
| <i>readHandle</i> | The serial manager module handle pointer.             |
| <i>buffer</i>     | Start address of the data to store the received data. |
| <i>length</i>     | The length of the data to be received.                |

Return values

|                                       |                                 |
|---------------------------------------|---------------------------------|
| <i>kStatus_SerialManager_-Success</i> | Successfully received all data. |
|---------------------------------------|---------------------------------|

|                                                |                                                                      |
|------------------------------------------------|----------------------------------------------------------------------|
| <code>kStatus_SerialManager_-<br/>Busy</code>  | Previous transmission still not finished; data not all received yet. |
| <code>kStatus_SerialManager_-<br/>Error</code> | An error occurred.                                                   |

### 56.5.9 `serial_manager_status_t SerialManager_WriteNonBlocking (` `serial_write_handle_t writeHandle, uint8_t * buffer, uint32_t length )`

This is a non-blocking function, which returns directly without waiting for all data to be sent. When all data is sent, the module notifies the upper layer through a TX callback function and passes the status parameter `kStatus_SerialManager_Success`. This function sends data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for transmission for the writing handle at the same time.

Note

The function `SerialManager_WriteBlocking` and the function `SerialManager_WriteNonBlocking` cannot be used at the same time. And, the TX callback is mandatory before the function could be used.

Parameters

|                          |                                           |
|--------------------------|-------------------------------------------|
| <code>writeHandle</code> | The serial manager module handle pointer. |
| <code>buffer</code>      | Start address of the data to write.       |
| <code>length</code>      | Length of the data to write.              |

Return values

|                                                  |                                                                  |
|--------------------------------------------------|------------------------------------------------------------------|
| <code>kStatus_SerialManager_-<br/>Success</code> | Successfully sent all data.                                      |
| <code>kStatus_SerialManager_-<br/>Busy</code>    | Previous transmission still not finished; data not all sent yet. |
| <code>kStatus_SerialManager_-<br/>Error</code>   | An error occurred.                                               |

### 56.5.10 `serial_manager_status_t SerialManager_ReadNonBlocking (` `serial_read_handle_t readHandle, uint8_t * buffer, uint32_t length )`

This is a non-blocking function, which returns directly without waiting for all data to be received. When all data is received, the module driver notifies the upper layer through a RX callback function and passes the

status parameter `kStatus_SerialManager_Success`. This function receives data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for receiving for the reading handle at the same time.

#### Note

The function `SerialManager_ReadBlocking` and the function `SerialManager_ReadNonBlocking` cannot be used at the same time. And, the RX callback is mandatory before the function could be used.

#### Parameters

|                         |                                                       |
|-------------------------|-------------------------------------------------------|
| <code>readHandle</code> | The serial manager module handle pointer.             |
| <code>buffer</code>     | Start address of the data to store the received data. |
| <code>length</code>     | The length of the data to be received.                |

#### Return values

|                                             |                                                                      |
|---------------------------------------------|----------------------------------------------------------------------|
| <code>kStatus_SerialManager_-Success</code> | Successfully received all data.                                      |
| <code>kStatus_SerialManager_-Busy</code>    | Previous transmission still not finished; data not all received yet. |
| <code>kStatus_SerialManager_-Error</code>   | An error occurred.                                                   |

### 56.5.11 `serial_manager_status_t SerialManager_TryRead ( serial_read_handle_t readHandle, uint8_t * buffer, uint32_t length, uint32_t * receivedLength )`

The function tries to read data from internal ring buffer. If the ring buffer is not empty, the data will be copied from ring buffer to up layer buffer. The copied length is the minimum of the ring buffer and up layer length. After the data is copied, the actual data length is passed by the parameter length. And There can only one buffer for receiving for the reading handle at the same time.

#### Parameters

|                             |                                                       |
|-----------------------------|-------------------------------------------------------|
| <code>readHandle</code>     | The serial manager module handle pointer.             |
| <code>buffer</code>         | Start address of the data to store the received data. |
| <code>length</code>         | The length of the data to be received.                |
| <code>receivedLength</code> | Length received from the ring buffer directly.        |

Return values

|                                             |                                                                      |
|---------------------------------------------|----------------------------------------------------------------------|
| <code>kStatus_SerialManager_-Success</code> | Successfully received all data.                                      |
| <code>kStatus_SerialManager_-Busy</code>    | Previous transmission still not finished; data not all received yet. |
| <code>kStatus_SerialManager_-Error</code>   | An error occurred.                                                   |

### 56.5.12 `serial_manager_status_t SerialManager_CancelWriting ( serial_write_handle_t writeHandle )`

The function cancels unfinished send transmission. When the transfer is canceled, the module notifies the upper layer through a TX callback function and passes the status parameter [kStatus\\_SerialManager\\_-Canceled](#).

Note

The function `SerialManager_CancelWriting` cannot be used to abort the transmission of the function `SerialManager_WriteBlocking`.

Parameters

|                          |                                           |
|--------------------------|-------------------------------------------|
| <code>writeHandle</code> | The serial manager module handle pointer. |
|--------------------------|-------------------------------------------|

Return values

|                                             |                                     |
|---------------------------------------------|-------------------------------------|
| <code>kStatus_SerialManager_-Success</code> | Get successfully abort the sending. |
| <code>kStatus_SerialManager_-Error</code>   | An error occurred.                  |

### 56.5.13 `serial_manager_status_t SerialManager_CancelReading ( serial_read_handle_t readHandle )`

The function cancels unfinished receive transmission. When the transfer is canceled, the module notifies the upper layer through a RX callback function and passes the status parameter [kStatus\\_SerialManager\\_-Canceled](#).

## Note

The function [SerialManager\\_CancelReading](#) cannot be used to abort the transmission of the function [SerialManager\\_ReadBlocking](#).

## Parameters

|                   |                                           |
|-------------------|-------------------------------------------|
| <i>readHandle</i> | The serial manager module handle pointer. |
|-------------------|-------------------------------------------|

## Return values

|                                       |                                       |
|---------------------------------------|---------------------------------------|
| <i>kStatus_SerialManager_-Success</i> | Get successfully abort the receiving. |
| <i>kStatus_SerialManager_-Error</i>   | An error occurred.                    |

#### 56.5.14 **serial\_manager\_status\_t SerialManager\_InstallTxCallback (** **serial\_write\_handle\_t writeHandle, serial\_manager\_callback\_t callback,** **void \* callbackParam )**

This function is used to install the TX callback and callback parameter for the serial manager module. When any status of TX transmission changed, the driver will notify the upper layer by the installed callback function. And the status is also passed as status parameter when the callback is called.

## Parameters

|                      |                                           |
|----------------------|-------------------------------------------|
| <i>writeHandle</i>   | The serial manager module handle pointer. |
| <i>callback</i>      | The callback function.                    |
| <i>callbackParam</i> | The parameter of the callback function.   |

## Return values

|                                       |                                    |
|---------------------------------------|------------------------------------|
| <i>kStatus_SerialManager_-Success</i> | Successfully install the callback. |
|---------------------------------------|------------------------------------|

#### 56.5.15 **serial\_manager\_status\_t SerialManager\_InstallRxCallback (** **serial\_read\_handle\_t readHandle, serial\_manager\_callback\_t callback,** **void \* callbackParam )**

This function is used to install the RX callback and callback parameter for the serial manager module. When any status of RX transmission changed, the driver will notify the upper layer by the installed callback

function. And the status is also passed as status parameter when the callback is called.

Parameters

|                      |                                           |
|----------------------|-------------------------------------------|
| <i>readHandle</i>    | The serial manager module handle pointer. |
| <i>callback</i>      | The callback function.                    |
| <i>callbackParam</i> | The parameter of the callback function.   |

Return values

|                                       |                                    |
|---------------------------------------|------------------------------------|
| <i>kStatus_SerialManager_-Success</i> | Successfully install the callback. |
|---------------------------------------|------------------------------------|

### 56.5.16 static bool SerialManager\_needPollingIsr( void ) [inline], [static]

This function is used to check if need polling ISR.

Return values

|             |                  |
|-------------|------------------|
| <i>TRUE</i> | if need polling. |
|-------------|------------------|

### 56.5.17 serial\_manager\_status\_t SerialManager\_EnterLowpower( serial\_handle\_t serialHandle )

This function is used to prepare to enter low power consumption.

Parameters

|                     |                                           |
|---------------------|-------------------------------------------|
| <i>serialHandle</i> | The serial manager module handle pointer. |
|---------------------|-------------------------------------------|

Return values

|                                       |                       |
|---------------------------------------|-----------------------|
| <i>kStatus_SerialManager_-Success</i> | Successful operation. |
|---------------------------------------|-----------------------|

### 56.5.18 serial\_manager\_status\_t SerialManager\_ExitLowpower( serial\_handle\_t serialHandle )

This function is used to restore from low power consumption.

## Parameters

|                     |                                           |
|---------------------|-------------------------------------------|
| <i>serialHandle</i> | The serial manager module handle pointer. |
|---------------------|-------------------------------------------|

## Return values

|                                       |                       |
|---------------------------------------|-----------------------|
| <i>kStatus_SerialManager_-Success</i> | Successful operation. |
|---------------------------------------|-----------------------|

**56.5.19 void SerialManager\_SetLowpowerCriticalCb ( const serial\_manager\_lowpower\_critical\_CBs\_t \* *pfCallback* )**

## Parameters

|                   |                                                                   |
|-------------------|-------------------------------------------------------------------|
| <i>pfCallback</i> | Pointer to the function structure used to allow/disable lowpower. |
|-------------------|-------------------------------------------------------------------|

## 56.6 Serial Port Uart

### 56.6.1 Overview

#### Macros

- #define **SERIAL\_PORT\_UART\_DMA\_RECEIVE\_DATA\_LENGTH** (64U)  
*serial port uart handle size*
- #define **SERIAL\_USE\_CONFIGURE\_STRUCTURE** (0U)  
*Enable or disable the configure structure pointer.*

#### Enumerations

- enum **serial\_port\_uart\_parity\_mode\_t** {
   
    **kSerialManager\_UartParityDisabled** = 0x0U,  
  
    **kSerialManager\_UartParityEven** = 0x2U,  
  
    **kSerialManager\_UartParityOdd** = 0x3U }
   
*serial port uart parity mode*
- enum **serial\_port\_uart\_stop\_bit\_count\_t** {
   
    **kSerialManager\_UartOneStopBit** = 0U,  
  
    **kSerialManager\_UartTwoStopBit** = 1U }
   
*serial port uart stop bit count*

### 56.6.2 Enumeration Type Documentation

#### 56.6.2.1 enum serial\_port\_uart\_parity\_mode\_t

Enumerator

- kSerialManager\_UartParityDisabled*** Parity disabled.  
***kSerialManager\_UartParityEven*** Parity even enabled.  
***kSerialManager\_UartParityOdd*** Parity odd enabled.

#### 56.6.2.2 enum serial\_port\_uart\_stop\_bit\_count\_t

Enumerator

- kSerialManager\_UartOneStopBit*** One stop bit.  
***kSerialManager\_UartTwoStopBit*** Two stop bits.

## 56.7 Serial Port USB

### 56.7.1 Overview

#### Modules

- [USB Device Configuration](#)

#### Data Structures

- struct [serial\\_port\\_usb\\_cdc\\_config\\_t](#)  
*serial port usb config struct* [More...](#)

#### Macros

- #define [SERIAL\\_PORT\\_USB\\_CDC\\_HANDLE\\_SIZE](#) (72U)  
*serial port usb handle size*
- #define [USB\\_DEVICE\\_INTERRUPT\\_PRIORITY](#) (3U)  
*USB interrupt priority.*

#### Enumerations

- enum [serial\\_port\\_usb\\_cdc\\_controller\\_index\\_t](#) {  
    kSerialManager\_UsbControllerKhci0 = 0U,  
    kSerialManager\_UsbControllerKhci1 = 1U,  
    kSerialManager\_UsbControllerEhci0 = 2U,  
    kSerialManager\_UsbControllerEhci1 = 3U,  
    kSerialManager\_UsbControllerLpcIp3511Fs0 = 4U,  
    kSerialManager\_UsbControllerLpcIp3511Fs1 = 5U,  
    kSerialManager\_UsbControllerLpcIp3511Hs0 = 6U,  
    kSerialManager\_UsbControllerLpcIp3511Hs1 = 7U,  
    kSerialManager\_UsbControllerOhci0 = 8U,  
    kSerialManager\_UsbControllerOhci1 = 9U,  
    kSerialManager\_UsbControllerIp3516Hs0 = 10U,  
    kSerialManager\_UsbControllerIp3516Hs1 = 11U }  
*USB controller ID.*

## 56.7.2 Data Structure Documentation

### 56.7.2.1 struct serial\_port\_usb\_cdc\_config\_t

#### Data Fields

- `serial_port_usb_cdc_controller_index_t controllerIndex`  
*controller index*

## 56.7.3 Enumeration Type Documentation

### 56.7.3.1 enum serial\_port\_usb\_cdc\_controller\_index\_t

Enumerator

`kSerialManager_UsbControllerKhci0` KHCI 0U.

`kSerialManager_UsbControllerKhci1` KHCI 1U, Currently, there are no platforms which have two KHCI IPs, this is reserved to be used in the future.

`kSerialManager_UsbControllerEhci0` EHCI 0U.

`kSerialManager_UsbControllerEhci1` EHCI 1U, Currently, there are no platforms which have two EHCI IPs, this is reserved to be used in the future.

`kSerialManager_UsbControllerLpcIp3511Fs0` LPC USB IP3511 FS controller 0.

`kSerialManager_UsbControllerLpcIp3511Fs1` LPC USB IP3511 FS controller 1, there are no platforms which have two IP3511 IPs, this is reserved to be used in the future.

`kSerialManager_UsbControllerLpcIp3511Hs0` LPC USB IP3511 HS controller 0.

`kSerialManager_UsbControllerLpcIp3511Hs1` LPC USB IP3511 HS controller 1, there are no platforms which have two IP3511 IPs, this is reserved to be used in the future.

`kSerialManager_UsbControllerOhci0` OHCI 0U.

`kSerialManager_UsbControllerOhci1` OHCI 1U, Currently, there are no platforms which have two OHCI IPs, this is reserved to be used in the future.

`kSerialManager_UsbControllerIp3516Hs0` IP3516HS 0U.

`kSerialManager_UsbControllerIp3516Hs1` IP3516HS 1U, Currently, there are no platforms which have two IP3516HS IPs, this is reserved to be used in the future.

#### 56.7.4 USB Device Configuration

## 56.8 Serial Port SWO

### 56.8.1 Overview

#### Data Structures

- struct `serial_port_swo_config_t`  
*serial port swo config struct* [More...](#)

#### Macros

- #define `SERIAL_PORT_SWO_HANDLE_SIZE` (12U)  
*serial port swo handle size*

#### Enumerations

- enum `serial_port_swo_protocol_t` {
   
`kSerialManager_SwoProtocolManchester` = 1U,  
`kSerialManager_SwoProtocolNrz` = 2U }
   
*serial port swo protocol*

### 56.8.2 Data Structure Documentation

#### 56.8.2.1 struct `serial_port_swo_config_t`

##### Data Fields

- `uint32_t clockRate`  
*clock rate*
- `uint32_t baudRate`  
*baud rate*
- `uint32_t port`  
*Port used to transfer data.*
- `serial_port_swo_protocol_t protocol`  
*SWO protocol.*

### 56.8.3 Enumeration Type Documentation

#### 56.8.3.1 enum `serial_port_swo_protocol_t`

Enumerator

- `kSerialManager_SwoProtocolManchester` SWO Manchester protocol.  
`kSerialManager_SwoProtocolNrz` SWO UART/NRZ protocol.

# Chapter 57

## Nic301

### 57.1 Overview

#### Functions

- static void **NIC\_SetReadQos** (nic\_reg\_t base, nic\_qos\_t value)  
*Set read\_qos Value.*
- static nic\_qos\_t **NIC\_GetReadQos** (nic\_reg\_t base)  
*Get read\_qos Value.*
- static void **NIC\_SetWriteQos** (nic\_reg\_t base, nic\_qos\_t value)  
*Set write\_qos Value.*
- static nic\_qos\_t **NIC\_GetWriteQos** (nic\_reg\_t base)  
*Get write\_qos Value.*
- static void **NIC\_SetFnModAhb** (nic\_reg\_t base, nic\_fn\_mod\_ahb\_t v)  
*Set fn\_mod\_ahb Value.*
- static nic\_fn\_mod\_ahb\_t **NIC\_GetFnModAhb** (nic\_reg\_t base)  
*Get fn\_mod\_ahb Value.*
- static void **NIC\_SetWrTideMark** (nic\_reg\_t base, uint8\_t value)  
*Set wr\_tidemark Value.*
- static uint8\_t **NIC\_GetWrTideMark** (nic\_reg\_t base)  
*Get wr\_tidemark Value.*
- static void **NIC\_SetFnMod** (nic\_reg\_t base, nic\_fn\_mod\_t value)  
*Set fn\_mod Value.*
- static nic\_fn\_mod\_t **NIC\_GetFnMod** (nic\_reg\_t base)  
*Get fn\_mod Value.*
- static void **NIC\_SetFnMod2** (nic\_reg\_t base, nic\_fn\_mod\_t value)  
*Set fn\_mod2 Value.*
- static nic\_fn\_mod2\_t **NIC\_GetFnMod2** (nic\_reg\_t base)  
*Get fn\_mod2 Value.*

#### Driver version

- #define **FSL\_NIC301\_DRIVER\_VERSION** (**MAKE\_VERSION**(2U, 0U, 1U))  
*NIC301 driver version 2.0.1.*

### 57.2 Macro Definition Documentation

#### 57.2.1 #define **FSL\_NIC301\_DRIVER\_VERSION** (**MAKE\_VERSION**(2U, 0U, 1U))

### 57.3 Function Documentation

#### 57.3.1 static void **NIC\_SetReadQos** ( nic\_reg\_t *base*, nic\_qos\_t *value* ) [**inline**], [**static**]

Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | Base address of GPV address |
| <i>value</i> | Target value (0 - 15)       |

### 57.3.2 static nic\_qos\_t NIC\_GetReadQos ( nic\_reg\_t *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | Base address of GPV address |
|-------------|-----------------------------|

Returns

Current value configured

### 57.3.3 static void NIC\_SetWriteQos ( nic\_reg\_t *base*, nic\_qos\_t *value* ) [inline], [static]

Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | Base address of GPV address |
| <i>value</i> | Target value (0 - 15)       |

### 57.3.4 static nic\_qos\_t NIC\_GetWriteQos ( nic\_reg\_t *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | Base address of GPV address |
|-------------|-----------------------------|

Returns

Current value configured

### 57.3.5 static void NIC\_SetFnModAhb ( nic\_reg\_t *base*, nic\_fn\_mod\_ahb\_t *v* ) [inline], [static]

Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | Base address of GPV address |
| <i>value</i> | Target value                |

### 57.3.6 static nic\_fn\_mod\_ahb\_t NIC\_GetFnModAhb ( nic\_reg\_t *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | Base address of GPV address |
|-------------|-----------------------------|

Returns

Current value configured

### 57.3.7 static void NIC\_SetWrTideMark ( nic\_reg\_t *base*, uint8\_t *value* ) [inline], [static]

Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | Base address of GPV address |
| <i>value</i> | Target value (0 - 7)        |

### 57.3.8 static uint8\_t NIC\_GetWrTideMark ( nic\_reg\_t *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | Base address of GPV address |
|-------------|-----------------------------|

Returns

Current value configured

### 57.3.9 static void NIC\_SetFnMod ( nic\_reg\_t *base*, nic\_fn\_mod\_t *value* ) [inline], [static]

Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | Base address of GPV address |
| <i>value</i> | Target value                |

**57.3.10 static nic\_fn\_mod\_t NIC\_GetFnMod ( nic\_reg\_t *base* ) [inline], [static]**

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | Base address of GPV address |
|-------------|-----------------------------|

Returns

Current value configured

**57.3.11 static void NIC\_SetFnMod2 ( nic\_reg\_t *base*, nic\_fn\_mod\_t *value* ) [inline], [static]**

Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | Base address of GPV address |
| <i>value</i> | Target value                |

**57.3.12 static nic\_fn\_mod2\_t NIC\_GetFnMod2 ( nic\_reg\_t *base* ) [inline], [static]**

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | Base address of GPV address |
|-------------|-----------------------------|

Returns

Current value configured

## 57.3.13 CODEC Adapter

### 57.3.13.1 Overview

#### Enumerations

- enum {  
  kCODEC\_WM8904,  
  kCODEC\_WM8960,  
  kCODEC\_WM8524,  
  kCODEC\_SGTL5000,  
  kCODEC\_DA7212,  
  kCODEC\_CS42888,  
  kCODEC\_CS42448,  
  kCODEC\_AK4497,  
  kCODEC\_AK4458,  
  kCODEC\_TFA9XXX,  
  kCODEC\_TFA9896,  
  kCODEC\_WM8962 }  
    *codec type*

### 57.3.13.2 Enumeration Type Documentation

#### 57.3.13.2.1 anonymous enum

Enumerator

*kCODEC\_WM8904* wm8904  
*kCODEC\_WM8960* wm8960  
*kCODEC\_WM8524* wm8524  
*kCODEC\_SGTL5000* sgtl5000  
*kCODEC\_DA7212* da7212  
*kCODEC\_CS42888* CS42888.  
*kCODEC\_CS42448* CS42448.  
*kCODEC\_AK4497* AK4497.  
*kCODEC\_AK4458* ak4458  
*kCODEC\_TFA9XXX* tfa9xxx  
*kCODEC\_TFA9896* tfa9896  
*kCODEC\_WM8962* wm8962

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