





Jumper JP1:
1-2: PLL generated quadrature clock (internal)
2-3: motherboard supplied quadrature clock (external)

rev 3.0: added tristate logic on \overline{AS} for DMA compatibility
rev 2.2 fixed latching function of U5B
rev 2.1 improved \overline{AS} /DTACK and E logic
rev 2.0 added PLL based clock doubler

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Sheet: /bus interface/
File: bus_interface.sch

Title: 14MHz accelerator SE

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Rev: 3.0

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