

# 8274 MULTI-PROTOCOL SERIAL CONTROLLER (MPSC)

- **Asynchronous, Byte Synchronous and Bit Synchronous Operation**
- **Two Independent Full Duplex Transmitters and Receivers**
- **Fully Compatible with 8048, 8051, 8085, 8088, and 8086 CPU's; 8257 and 8237 DMA Controllers; and 8089 I/O Proc.**
- **4 Independent DMA Channels**
- **Baud Rate: DC to 880K Baud**  
—Future Selections to 1M Baud
- **Asynchronous:**  
—5-8 Bit Character; Odd, Even, or No Parity; 1, 1.5 or 2 Stop Bits  
—Error Detection: Framing, Overrun, and Parity
- **Byte Synchronous:**  
—Character Synchronization, Int. or Ext.  
—One or Two Sync Characters  
—Automatic CRC Generation and Checking (CRC-16)  
—IBM Bisync Compatible
- **Bit Synchronous:**  
—SDLC/HDLC Flag Generation and Recognition  
—8 Bit Address Recognition  
—Automatic Zero Bit Insertion and Deletion  
—Automatic CRC Generation and Checking (CCITT-16)  
—CCITT X.25 Compatible

The Intel® 8274 Multi-Protocol Serial Controller (MPSC) is designed to interface High Speed Communications Lines using Asynchronous, IBM Bisync, and SDLC/HDLC protocol to Intel microcomputer systems. It can be interfaced with Intel's MCS-48, -85, -51; iAPX-86, and -88 families, the 8237 DMA Controller, or the 8089 I/O Processor in polled, interrupt driven, or DMA driven modes of operation.

The MPSC is a 40 pin device fabricated using Intel's High Performance HMOS Technology.

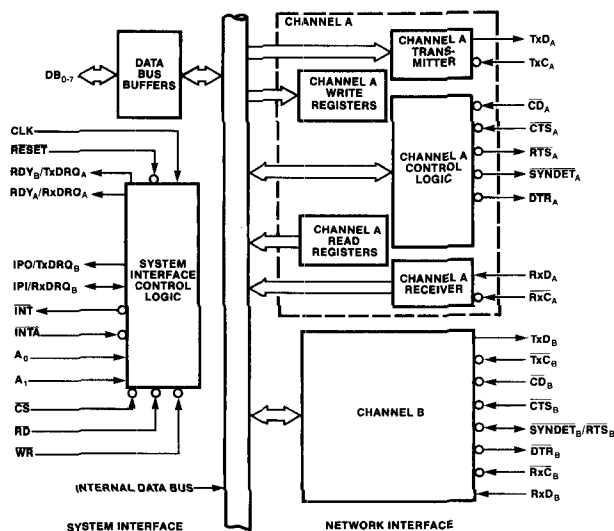


Figure 1. Block Diagram

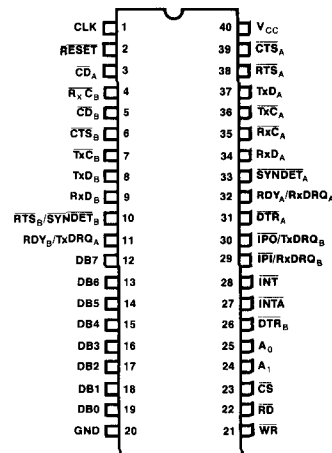


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
CLK	1	I	<b>Clock:</b> System clock, TTL compatible.
RESET	2	I	<b>Reset:</b> A low signal on this pin will force the MPSC to an idle state. TxD <sub>A</sub> and TxD <sub>B</sub> are forced high. The modem interface output signals are forced high. The MPSC will remain idle until the control registers are initialized. Reset must be true for one complete CLK cycle.
CD <sub>A</sub>	3	I	<b>Carrier Detect (Channel A):</b> Carrier Detect (Channel A) signals that the line transmission has started. The MPSC will begin to sample data on the RxD <sub>A</sub> line if modem enables are selected.
RxC <sub>B</sub>	4	I	<b>Receiver Clock:</b> The Receiver Clock (Channel B) clocks in data on the RxD <sub>B</sub> pin.
CD <sub>B</sub>	5	I	<b>Carrier Detect (Channel B):</b> Carrier Detect (Channel B) signals that the line transmission has started. The MPSC will begin to sample data on the RxD <sub>B</sub> line if modem enables are selected.
CTS <sub>B</sub>	6	I	<b>Clear To Send (Channel B):</b> Clear To Send (Channel B) signals that the modem is ready to accept data from the MPSC. Clear To Send will enable Channel B transmitter if modem enables are selected, otherwise this pin may be used as a general purpose input.
TxC <sub>B</sub>	7	I	<b>Transmit Clock (Channel B):</b> Transmit Clock (Channel B) for TxD <sub>B</sub> pin.
TxD <sub>B</sub>	8	O	<b>Transmit Data (Channel B):</b> This line transmits the serial data to the communications channel (Channel B).
RxD <sub>B</sub>	9	I	<b>Receive Data (Channel B):</b> This line receives serial data from the communications channel (Channel B).
SYNDET <sub>B</sub> /RTS <sub>B</sub>	10	I/O	<b>Synchronous Detection (Channel B):</b> This pin is used in byte synchronous mode as either an internal sync detect (output) or as a means to force external synchronization (input). In SDLC mode, this pin is an output indicating flag detection. In asynchronous mode it is a general purpose input (Channel B). Request To Send (Channel B) is a general purpose output, generally used to signal that Channel B is ready to send data.

Symbol	Pin No.	Type	Name and Function
RDY <sub>B</sub> /TxDRQ <sub>A</sub>	11	O	<b>Ready Transmit Data:</b> In mode 0 this pin is used to synchronize data transfers for both Receive and Transmit of Channel B to the controlling processor's READY line (open collector). In modes 1 and 2 this pin requests a DMA transfer of data for a transmit operation (Channel A).
DB7	12	I/O	<b>Data Bus:</b> The Data Bus lines are bi-directional three state lines which interface with the system's Data Bus.
DB6	13		
DB5	14		
DB4	15		
DB3	16		
DB2	17		
DB1	18		
DB0	19		
GND	20		<b>Ground.</b>
V <sub>CC</sub>	40		<b>Power:</b> +5V Supply.
CTS <sub>A</sub>	39	I	<b>Clear To Send (Channel A):</b> This signals that the modem is ready to accept data from the MPSC. Clear To Send will enable Channel B transmitter if modem enables are selected, otherwise this pin may be used as a general purpose input.
RTS <sub>A</sub>	38	O	<b>Request To Send (Channel A):</b> Request To Send (Channel A) is a general purpose output generally used to signal that Channel A is ready to send data.
TxD <sub>A</sub>	37	O	<b>Transmit Data (Channel A):</b> This line transmits the serial data to the communications channel (Channel A).
TxC <sub>A</sub>	36	I	<b>Transmitter Clock (Channel A):</b> The transmitter clock (Channel A) clocks out data on the TxD <sub>A</sub> pin.
RxC <sub>A</sub>	35	I	<b>Receiver Clock (Channel A):</b> The receiver clock (Channel A) clocks in data on the RxD <sub>A</sub> pin.
RxD <sub>A</sub>	34	I	<b>Receive Data (Channel A):</b> This line receives serial data from the communications channel (Channel A).
SYNDET <sub>A</sub>	33	I/O	<b>Synchronous Detection (Channel A):</b> This pin is used in byte synchronous mode as either an internal sync detect (output) or as a means to force external synchronization (input). In SDLC mode, this pin is an output indicating flag detection. In asynchronous mode it is a general purpose input (Channel A).

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{\text{RDY}}/\text{RxDRQ}_A$	32	O	<b>Ready:</b> In mode 0 this pin is used to synchronize data transfers for both receive and transmit of Channel A to the controlling processor's READY line (open collector). In modes 1 and 2 $\text{RxDRQ}_A$ requests a DMA transfer of data for a receive operation for Channel A.
$\text{DTR}_A$	31	O	<b>Data Terminal Ready:</b> This pin is Data Terminal Ready (Channel A) which is a general purpose output.
$\text{IPO}/\text{TxDRQ}_B$	30	O	<b>Interrupt Priority Out:</b> In modes 0 and 1, IPO is Interrupt Priority Out. It is used to establish a hardware interrupt priority scheme with IPI. It is low only if IPI is low and the controlling processor is not servicing an interrupt from this MPSC. In mode 2, $\text{TxDRQ}_B$ requests a DMA transfer of data for a transmit operation for Channel B.
$\text{IPI}/\text{RxDRQ}_B$	29	I/O	<b>Interrupt Priority In:</b> In modes 0 and 1, IPI is Interrupt Priority In. A low on IPI means that no higher priority device is being serviced by the controlling processor's interrupt service routine. In mode 2, $\text{RxDRQ}_B$ requests a DMA transfer of data for a receive operation for Channel B.

Symbol	Pin No.	Type	Name and Function
$\overline{\text{INT}}$	28	O	<b>Interrupt:</b> The interrupt signal indicates that the highest priority internal interrupt requires service (open collector). Priority can be resolved via an external interrupt controller or a daisy-chain scheme.
$\overline{\text{INTA}}$	27	I	<b>Interrupt Acknowledge:</b> This Interrupt Acknowledge allows the highest priority interrupting device to generate an interrupt vector.
$\overline{\text{DTR}}_B$	26	O	<b>Data Terminal Ready (Channel B):</b> This is a general purpose output.
$A_0$	25	I	<b>Address:</b> This line selects Channel A or B during data or command transfers. A low selects Channel A.
$A_1$	24	I	<b>Address:</b> This line selects between data or command information transfer. A low means data.
$\overline{\text{CS}}$	23	I	<b>Chip Select:</b> Chip Select enables RD or WR.
$\overline{\text{RD}}$	22	I	<b>Read:</b> Read controls a data byte or status byte transfer from the MPSC to CPU.
WR	21	I	<b>Write:</b> Write controls transfer of data or commands to the MPSC.

## GENERAL DESCRIPTION

The Intel® 8274 Multi-Protocol Serial Controller is a microcomputer peripheral device which supports Asynchronous (Start/Stop), Byte Synchronous (Monosync, IBM Bisync), and Bit Synchronous (ISO's HDLC, IBM's SDLC) protocols. This controller's flexible architecture allows easy implementation of many variations of these three protocols with low software and hardware overhead.

The Multi-Protocol Serial Controller (MPSC) implements two independent serial receiver/transmitter channels.

The MPSC supports several microprocessor interface options; Polled, Wait, Interrupt driven and DMA driven. The MPSC is designed to support Intel's® MCS-85 and iAPX 86, 88 families.

This data sheet will describe the serial protocol functions, the microprocessor interface, a detailed register and command description, general system operations, specifications, and waveforms.

## FUNCTIONAL DESCRIPTION

This section of the data sheet describes how the Asynchronous and Synchronous protocols are implemented in the MPSC. It describes general considerations, transmit operation, and receive operation for Asynchronous, Byte Synchronous, and Bit Synchronous protocols.

## ASYNCHRONOUS OPERATIONS

### General

For operation in the asynchronous mode, the MPSC must be initialized with the following information: character length (WR3; D7, D6 and WR5; D6, D5), clock rate (WR4; D7, D6), number of stop bits (WR4; D3, D2), odd, even or no parity (WR4; D1, D0), interrupt mode (WR1, WR2), and receiver (WR3; D0) or transmitter (WR5; D3) enable. When loading these parameters into the MPSC, WR4 information must

be written before the WR1, WR3, WR5 parameters/commands. (See Detailed Command Description Section).

For transmission via a modem or RS232C interface, the Request To Send (RTS) (WR5; D1) and Data Terminal Ready (DTR) (WR5; D7) bits must be set along with the Transmit Enable bit (WR5; D3). Setting the Auto Enables (WR3; D5) bit allows the programmer to send the first character of the message without waiting for a clear to send (CTS).

Both the Framing Error and Receive Overrun Error flags are latched and cause an interrupt, i.e., if status affects vector (WR1B; D2) is selected, the interrupt vector indicates a special Receive condition.

If the External/Status Interrupt bit (WR1; D0) is enabled, Break Detect (RR0; D7) and Carrier Detect (RR0; D3) will cause an interrupt. Reset External/Status Interrupts (WR0; D5, D4, D3) will clear Break Detect and Carrier Detect bits if they are set.

A status read after a data read will include error status for the next word in the buffer. If the Interrupt on First Character (WR1; D4, D3) is selected, then data and error status are held until an Error Reset command (WR0; D5, D4, D3) is given.

If the Interrupt on Every Character Mode bit (WR1; D4, D3) is selected, the interrupt vector is different if there is an error status in RR1. When the character is read, the error status bit is set and the Special Receive Condition vector is returned if Status Affects vector (WR1B; D2) is selected.

In a polled environment, the Receive Character Available bit (RR0; D0) must be monitored so that the CPU can determine when data is available. The bit is reset automatically when the data is read.

If the X1 clock mode is selected, the bit synchronization must be accomplished externally.

### Transmit

The transmit function begins when the Transmit Enable bit (WR5; D3) is set. The MPSC automatically adds the start bit, the programmed parity bit (odd, even or no parity) and the programmed number of stop bits (1, 1.5 or 2 bits) to the data character being transmitted.

The Serial data is shifted out from the Transmit Data (TxD) output on the falling edge of the Transmit Clock (TxCl) input, at a rate programmable to 1, 1/16, 1/32nd, or 1/64th of the clock rate supplied to the TxCl input.

The TxD output is held high when the transmitter has no data to send, unless, under program control, the Send Break (WR5; D4) command is issued to hold the TxD low.

If the External/STATUS Interrupt bit (WR1; D0) is set, the status of CD, CTS and SYNDT are monitored, and, if any changes occur for a period of time greater than the minimum specified pulse width, an interrupt is generated. CTS is usually monitored using this interrupt feature.

If the Auto Enables (WR; D5) option is selected the programmer need not wait for the CTS before sending the first character. The MPSC will automatically wait for the CTS pin to go active before the transmission begins.

The Transmit Buffer Empty bit (RR0; D2) is set by the MPSC when the data byte from the buffer is loaded in the transmit shift register. The data is written to the MPSC only when the Tx buffer becomes empty to prevent overwriting.

**Asynchronous Mode Register Setup**

	D7	D6	D5	D4	D3	D2	D1	D0
<b>WR3</b>	00 Rx 5 b/char 01 Rx 7 b/char 10 Rx 6 b/char 11 Rx 8 b/char		AUTO ENABLES	0	0	0	0	Rx ENABLE
<b>WR4</b>	00 X1 Clock 01 X16 Clock 10 X32 Clock 11 X64 Clock		0	0	00 ENABLE SYNC MODES 01 1 STOP BIT 10 1½ STOP BITS 11 2 STOP BITS		EVEN/ ODD PARITY	PARITY ENABLE
<b>WR5</b>		DTR	00 Tx 5 b/char 01 Tx 7 b/char 10 Tx 6 b/char 11 Tx 8 b/char	SEND BREAK	Tx ENABLE	0	RTS	0

## Receive

The receive function begins when the Receive Enable (WR3; D0) bit is set. If the Auto Enables (WR3; D5) option is selected, then Carrier Detect (CD) must also be low. A valid start bit is detected if a low persists for at least 1/2 bit time on the Receive Data (Rx D) input.

The data is sampled at mid-bit time, on the rising edge of Rx C, until the entire character is assembled. The receiver inserts 1's when a character is less than 8 bits. If parity (WR4; D1, D0) is enabled and the character is less than 8 bits the parity bit is not stripped from the character.

The receiver also stores error status for each of the 3 data characters in the data buffer. When a parity error is detected, the parity error flag (RR1; D4) is set and remains set until it is reset by the Error Reset command (WR0; D5, D4, D3).

When a character is assembled without a stop bit being detected, the Framing Error bit (RR1; D6) is set. The detection of a Framing Error adds an additional 1/2 bit time to the character time so the Framing Error is not interpreted as a new start bit.

If the CPU fails to read a data character while more than three characters have been received, the Receive Overrun bit (RR1; D5) is set. Only the overwritten character is flagged with the Receive Overrun bit. When this occurs, the fourth character assembled replaces the third character in the receive buffers. The Receive Overrun bit (RR1; D5) is reset by the Error Reset command (WR0; D5, D4, D3).

## SYNCHRONOUS OPERATION— MONO SYNC, BI SYNC

### General

The MPSC must be initialized with the following parameters: odd or even parity (WR4; D1, D0), X1 clock mode (WR4; D7, D6), 8- or 16-bit sync character (WR4; D5, D4), CRC polynomial (WR5; D2), Transmitter Enable (WR5; D3), interrupt modes (WR1, WR2), transmit character length (WR5; D6, D5) and receive character length (WR3; D7, D6). WR4 parameters must be written before WR1, WR3, WR5, WR6 and WR7.

The data is transmitted on the falling edge of the Transmit Clock, (Tx C) and is received on the rising edge of Receive Clock (Rx C). The X1 clock is used for both transmit and receive operations for all three sync modes: Mono, Bi and External.

### Transmit Set-Up—Monosync, Bisync

Transmit data is held high after channel reset, or if the transmitter is not enabled. A break may be programmed to generate a spacing line that begins as soon as the Send Break (WR5; D4) bit is set. With the transmitter fully initialized and enabled, the default condition is continuous transmission of the 8- or 16-bit sync character.

Using interrupts for data transfer requires that the Transmit Interrupt/DMA Enable bit (WR1; D1) be set. An interrupt is generated each time the transmit buffer becomes empty. The interrupt can be satisfied

**Synchronous Mode Register Setup—Monosync, Bisync**

	D7	D6	D5	D4	D3	D2	D1	D0
<b>WR3</b>	00 Rx 5 b/char 01 Rx 7 b/char 10 Rx 6 b/char 11 Rx 8 b/char		AUTO ENABLES	ENTER HUNT MODE	Rx CRC ENABLE	0	SYNC CHAR LOAD INHIBIT	Rx ENABLE
<b>WR4</b>	0	0	00 8 bit Sync 01 16 bit Sync 11 Ext Sync		0	0	EVEN/ ODD PARITY	PARITY ENABLE
<b>WR5</b>	DTR	00 Tx 5 b/char 01 Tx 7 b/char 10 Tx 6 b/char 11 Tx 8 b/char		SEND BREAK	Tx ENABLE	1 (SELECTS CRC-16)	RTS	Tx CRC ENABLE

either by writing another character into the transmitter or by resetting the Transmitter Interrupt/DMA Pending latch with a Reset Transmitter Interrupt/DMA Pending Command (WR0; D5, D4, D3). If nothing more is written into the transmitter, there can be no further Transmit Buffer Empty interrupt, but this situation does cause a Transmit Underrun condition (RR0; D6).

Data Transfers using the RDY signal are for software controlled data transfers such as block moves. RDY tells the CPU that the MPSC is not ready to accept/provide data and that the CPU must extend the output/input cycle. DMA data transfers use the TxDRQ A/B signals which indicate that the transmit buffer is empty, and that the MPSC is ready to accept the next data character. If the data character is not loaded into the MPSC by the time the transmit shift register is empty, the MPSC enters the Transmit Underrun condition.

The MPSC has two programmable options for solving the transmit underrun condition: it can insert sync characters, or it can send the CRC characters generated so far, followed by sync characters. Following a chip or channel reset, the Transmit Underrun/EOM status bit (RR0; D6) is in a set condition allowing the insertion of sync characters when there is no data to send. The CRC is not calculated on these automatically inserted sync characters. When the CPU detects the end of message, a Reset Transmit Underrun/EOM command can be issued. This allows CRC to be sent when the transmitter has no data to send.

In the case of sync insertion, an interrupt is generated only after the first automatically inserted sync character has been loaded in Transmit Shift Register. The status indicates the Transmit Underrun/EOM bit and the Transmit Buffer Empty bit are set.

In the case of CRC insertion, the Transmit Underrun/EOM bit is set and the Transmit Buffer Empty bit is reset while CRC is being sent. When CRC has been completely sent, the Transmit Buffer Empty status bit is set and an interrupt is generated to indicate to the CPU that another message can begin (this interrupt occurs because CRC has been sent and sync has been loaded into the Tx Shift Register). If no more messages are to be sent, the program can terminate transmission by resetting RTS, and disabling the transmitter (WR5; D3).

**Bisync CRC Generation.** Setting the Transmit CRC enable bit (WR5; D0) indicates CRC accumulation when the program sends the first data character to

the MPSC. Although the MPSC automatically transmits up to two sync characters (16 bit sync), it is wise to send a few more sync characters ahead of the message (before enabling Transmit CRC) to ensure synchronization at the receiving end.

The Transmit CRC Enable bit can be changed on the fly any time in the message to include or exclude a particular data character from CRC accumulation. The Transmit CRC Enable bit should be in the desired state when the data character is loaded from the transmit shift register. To ensure this bit in the proper state, the Transmit CRC Enable bit must be issued before sending the data character to the MPSC.

**Transmit Transparent Mode.** Transparent mode (Bisync protocol) operation is made possible by the ability to change Transmit CRC Enable on the fly and by the additional capability of inserting 16 bit sync characters. Exclusion of DLE characters from CRC calculation can be achieved by disabling CRC calculation immediately preceding the DLE character transfer to the MPSC.

In the transmit mode, the transmitter always sends the programmed number of sync bits (8 or 16) (WR4; D5, D4). When in the Monosync mode, the transmitter sends from WR6 and the receiver compares against WR7. One of two CRC polynomials, CRC 16 or SDLC, may be used with synchronous modes. In the transmit initialization process, the CRC generator is initialized by setting the Reset Transmit CRC Generator command (WR0; D7, D6).

The External/Status interrupt (WR1; D0) mode can be used to monitor the status of the CTS input as well as the Transmit Underrun/EOM latch. Optionally, the Auto Enable (WR3; D5) feature can be used to enable the transmitter when CTS is active. The first data transfer to the MPSC can begin when the External/Status interrupt occurs (CTS (RR0; D5) status bit set) following the Transmit Enable command (WR5; D3).

## Receive

After a channel reset, the receiver is in the Hunt phase, during which the MPSC looks for character synchronization. The Hunt begins only when the receiver is enabled and data transfer begins only when character synchronization has been achieved. If character synchronization is lost, the hunt phase can be re-entered by writing the Enter Hunt Phase (WR3; D4) bit. The assembly of received data continues until the MPSC is reset or until the receiver is

disabled (by command or by  $\overline{CD}$  while in the Auto Enables mode) or until the CPU sets the Enter Hunt Phase bit. Under program control, all the leading sync characters of the message can be inhibited from loading the receive buffers by setting the Sync Character Load Inhibit (WR3; D1) bit. After character synchronization is achieved the assembled characters are transferred to the receive data FIFO.

Data may be transferred with or without interrupts. Transferring data without interrupts is used for a purely polled operation or for off-line conditions. There are three interrupt modes available for data transfer: Interrupt on First Character Only, Interrupt on Every Character, and Special Receive Conditions Interrupt.

Interrupt on First Character Only mode is normally used to start a polling loop, a block transfer sequence using RDY to synchronize the CPU to the incoming data rate or a DMA transfer using the RxDRQ signal. The MPSC interrupts on the first character and thereafter only interrupts after a Special Receive Condition is detected. This mode can be reinitialized using the Enable Interrupt On Next Receive Character (WR0; D5, D4, D3) command which allows the next character received to generate an interrupt. Parity Errors do not cause interrupts, but End of Frame (SDLC operation) and Receive Overrun do cause interrupts in this mode. If the external status interrupts (WR1; D0) are enabled an interrupt may be generated any time the  $\overline{CD}$  changes state.

Interrupt On Every Character mode generates an interrupt whenever a character enters the receive buffer. Errors and Special Receive Conditions generate a special vector if the Status Affects Vector (WR1B; D2) is selected. Also the Parity Error may be

programmed (WR1; D4, D3) not to generate the special vector while in the Interrupt On Every Character mode.

The Special Receive Condition interrupt can only occur while in the Receive Interrupt On First Character Only or the Interrupt On Every Receive Character modes. The Special Receive Condition interrupt is caused by the Receive Overrun (RR1; D5) error condition. The error status reflects an error in the current word in the receive buffer, in addition to any Parity or Overrun errors since the last Error Reset (WR0; D5, D4, D3). The Receive Overrun and Parity error status bits are latched and can only be reset by the Error Reset (WR0; D5, D4, D3) command.

## SYNCHRONOUS OPERATION—SDLC

### General

Like the other synchronous operations the SDLC mode must be initialized with the following parameters: SDLC mode (WR4; D5, D4), SDLC polynomial (WR5; D2), Request to Send, Data Terminal Ready, transmit character length (WR5; D6, D5), interrupt modes (WR1; WR2), Transmit Enable (WR5; D3), Receive Enable (WR3; D0), Auto Enable (WR3; D5) and External/Status Interrupt (WR1; D0). WR4 parameters must be written before WR1, WR3, WR5, WR6 and WR7.

The Interrupt modes for SDLC operation are similar to those discussed previously in the synchronous operations section.

Synchronous Mode Register Setup—SDLC/HDLC

	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 Rx 5b/char 01 Rx 7b/char 10 Rx 6b/char 11 Rx 8b/char		AUTO ENABLES	ENTER HUNT MODE	Rx CRC ENABLE	ADDRESS SEARCH MODE	0	Rx ENABLE
WR4	0	0	1 0 (SELECTS SDLC/ HDLC MODE)		0	0	0	0
WR5	DTR	00 Tx ≤5b/char 01 Tx 7b/char 10 Tx 6b/char 11 Tx 8b/char		0	Tx ENABLE	0 (SELECTS SDLC/ HDLC CRC)	RTS	Tx CRC ENABLE

## Transmit

After a channel reset, the MPSC begins sending SDLC flags.

Following the flags in an SDLC operation the 8-bit address field, control field and information field may be sent to the MPSC by the microprocessor. The MPSC transmits the Frame Check Sequence using the Transmit Underrun feature. The MPSC automatically inserts a zero after every sequence of 5 consecutive 1's except when transmitting Flags or Aborts.

SDLC—like protocols do not have provision for fill characters within a message. The MPSC therefore automatically terminates an SDLC frame when the transmit data buffer and output shift register have no more bits to send. It does this by sending the two bytes of CRC and then one or more flags. This allows very high-speed transmissions under DMA or CPU control without requiring the CPU to respond quickly to the end-of-message situation.

After a reset, the Transmit Underrun/EOM status bit is in the set state and prevents the insertion of CRC characters during the time there is no data to send. Flag characters are sent. The MPSC begins to send the frame when data is written into the transmit buffer. Between the time the first data byte is written, and the end of the message, the Reset Transmit Underrun/EOM (WR0; D5, D4, D1) command must be issued. The Transmit Underrun/EOM status bit (RR0; D6) is in the reset state at the end of the message which automatically sends the CRC characters.

The MPSC may be programmed to issue a send Abort command (WR0; D5, D4, D3). This command causes at least eight 1's but less than fourteen 1's to be sent before the line reverts to continuous flags.

## Receive

After initialization, the MPSC enters the Hunt phase, and remains in the Hunt phase until the first Flag is received. The MPSC never again enters the Hunt phase unless the microprocessor writes the Enter Hunt command.

The MPSC can be programmed to receive all frames or it can be programmed to the Address Search Mode. In the Address Search Mode, only frames with addresses that match the value in WR6 or the global address (0FFH) are received by the MPSC. Extended address recognition must be done by the microprocessor software.

The control and information fields are received as data.

SDLC/HDLC CRC calculation does not have an 8-bit delay, since all characters are included in the calculation, unlike Byte Synchronous Protocols.

Reception of an abort sequence (7 or more 1's) will cause the Break/Abort bit (RR0; D7) to be set and will cause an External/Status interrupt, if enabled. After the Reset External/Status Interrupts Command has been issued, a second interrupt will occur at the end of the abort sequence.

## MPSC

### Detailed Command Description

#### GENERAL

The MPSC supports an extremely flexible set of serial and system interface modes.

The system interface to the CPU consists of 8 ports or buffers:

CS	A <sub>0</sub>	A <sub>1</sub>	Read Operation	Write Operation
0	0	0	Ch. A Data Read	Ch. A Data Write
0	0	1	Ch. A Status Read	Ch. A Command/Parameter
0	1	0	Ch. B Data Read	Ch. B Data Write
0	1	1	Ch. B Status Read	Ch. B Command/Parameter
1	X	X	High Impedance	High Impedance

Data buffers are addressed by A<sub>1</sub> = 0, and Command ports are addressed by A<sub>1</sub> = 1.

Command, parameter, and status information is held in 22 registers within the MPSC (8 write registers and 3 read registers for each channel). They are all accessed via the command ports.

An internal pointer register selects which of the command or status registers will be read or written during a command/status access of an MPSC channel.



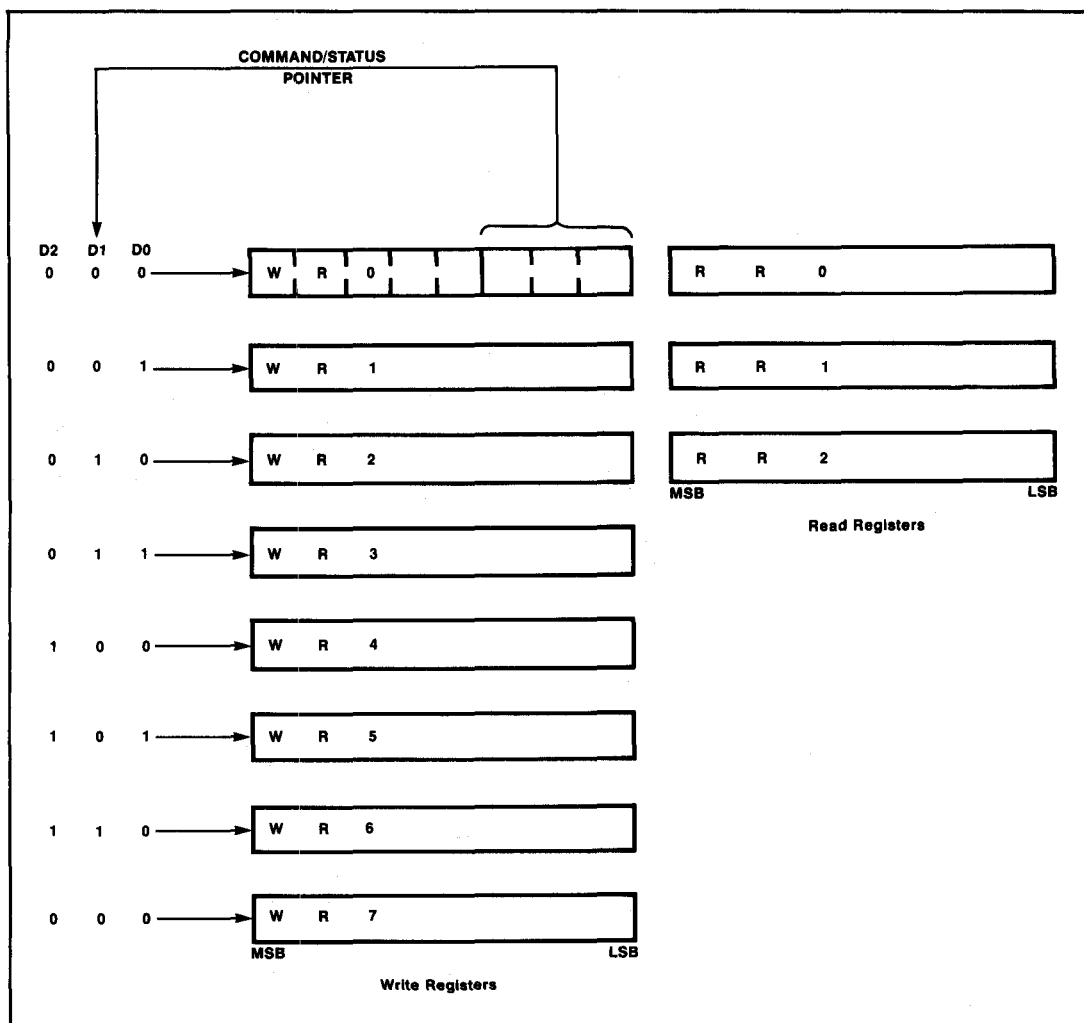


Figure 3. Command/Status Register Architecture (each serial channel)

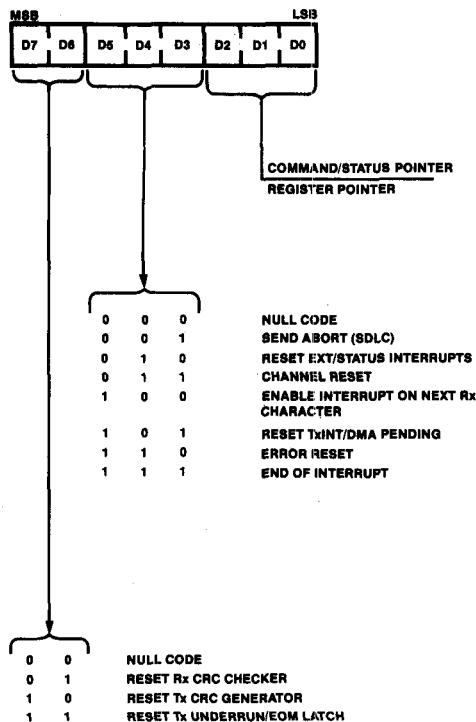
After reset, the contents of the pointer register are zero. The first write to a command register causes the data to be loaded into Write Register 0 (WR0). The three least significant bits of WR0 are loaded

into the Command/Status Pointer. The next read or write operation accesses the read or write register selected by the pointer. The pointer is reset after the read or write operation is completed.

# COMMAND/STATUS DESCRIPTION

The following command and status bytes are used during initialization and execution phases of operation. All Command/Status operations on the two channels are identical, and independent, except where noted.

## Write Register 0 (WR0):



## Detailed Register Description

### WR0

D2, D1, D0—Command/Status Register Pointer bits determine which write-register the next byte is to be written into, or which read-register the next byte is to be read from. After reset, the first byte written into either channel goes into WR0. Following a read or write to any register (except WR0) the pointer will point to WR0.

D5, D4, D3—Command bits determine which of the basic seven commands are to be performed.

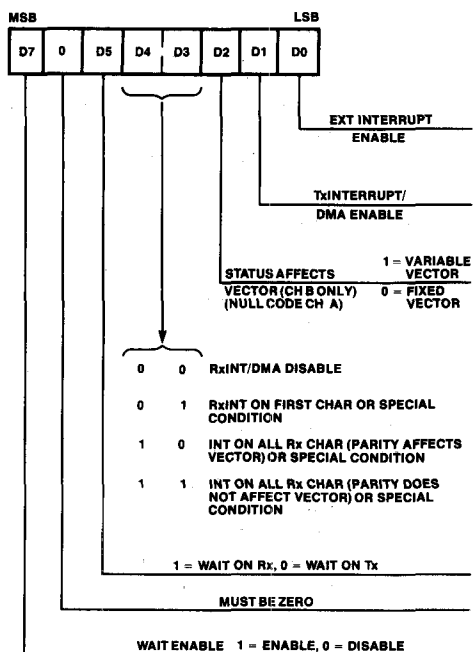
- Command 0 Null—has no effect.
- Command 1 Send Abort—causes the generation of eight to thirteen 1's when in the SDLC mode.
- Command 2 Reset External/Status Interrupts—resets the latched status bits of RR0 and re-enables them, allowing interrupts to occur again.
- Command 3 Channel Reset—resets the Latched Status bits of RR0, the interrupt prioritization logic and all control registers for the channel. Four extra system clock cycles should be allowed for MPSC reset time before any additional commands or controls are written into the channel.
- Command 4 Enable Interrupt on Next Receive Character—if the Interrupt on First Receive Character mode is selected, this command reactivates that mode after each complete message is received to prepare the MPSC for the next message.
- Command 5 Reset Transmitter Interrupt/DMA Pending—if The Transmit Interrupt/DMA Enable mode is selected, the MPSC automatically interrupts or requests DMA data transfer when the transmit buffer becomes empty. When there are no more characters to be sent, issuing this command prevents further transmitter interrupts or DMA requests until the next character has been completely sent.
- Command 6 Error Reset—error latches, Parity and Overrun errors in RR1 are reset.
- Command 7 End of Interrupt—resets the interrupt-in-service latch of the highest-priority internal device under service.
- D7, D6 CRC Reset Code
- 00 Null—has no effect.
- 01 Reset Receive CRC Checker—resets the CRC checker to 0's. If in SDLC mode the CRC checker is initialized to all 1's.

- 10      Reset Transmit CRC Generator  
—resets the CRC generator to 0's. If in SDLC mode the CRC generator's initialized to all 1's.
- 11      Reset Tx Underrun/End of Message Latch.

D1      Transmitter Interrupt/DMA Enable  
—allows the MPSC to interrupt or request a DMA transfer when the transmitter buffer becomes empty.

D2      Status Affects vector—(WR1, D2 active in channel B only.) If this bit is not set, then the fixed vector, programmed in WR2, is returned from an interrupt acknowledge sequence. If the bit is set then the vector returned from an interrupt acknowledge is variable as shown in the Interrupt Vector Table.

### Write Register 1 (WR1):



- D0      External/Status Interrupt Enable  
—allows interrupt to occur as the result of transitions on the CD, CTS or SYNDET inputs. Also allows interrupts as the result of a Break/Abort detection and termination, or at the beginning of CRC, or sync character transmission when the Transmit Underrun/EOM latch becomes set.

D4, D3

- 0   0   Receive Interrupt Mode
- 0   1   Receive Interrupts/DMA Disabled
- 1   0   Receive Interrupt on First Character Only or Special Condition
- 1   1   Interrupt on All Receive Characters or Special Condition (Parity Error is a Special Receive Condition)

D5

Wait on Receive/Transmit—when the following conditions are met the RDY pin is activated, otherwise it is held in the High-Z state. (Conditions: Interrupt Enabled Mode, Wait Enabled, CS = 0, A0 = 0/1, and A1 = 0). The RDY pin is pulled low when the transmitter buffer is full or the receiver buffer is empty and it is driven High when the transmitter buffer is empty or the receiver buffer is full. The RDY<sub>A</sub> and RDY<sub>B</sub> may be wired OR connected since only one signal is active at any one time while the other is in the High Z state.

D6

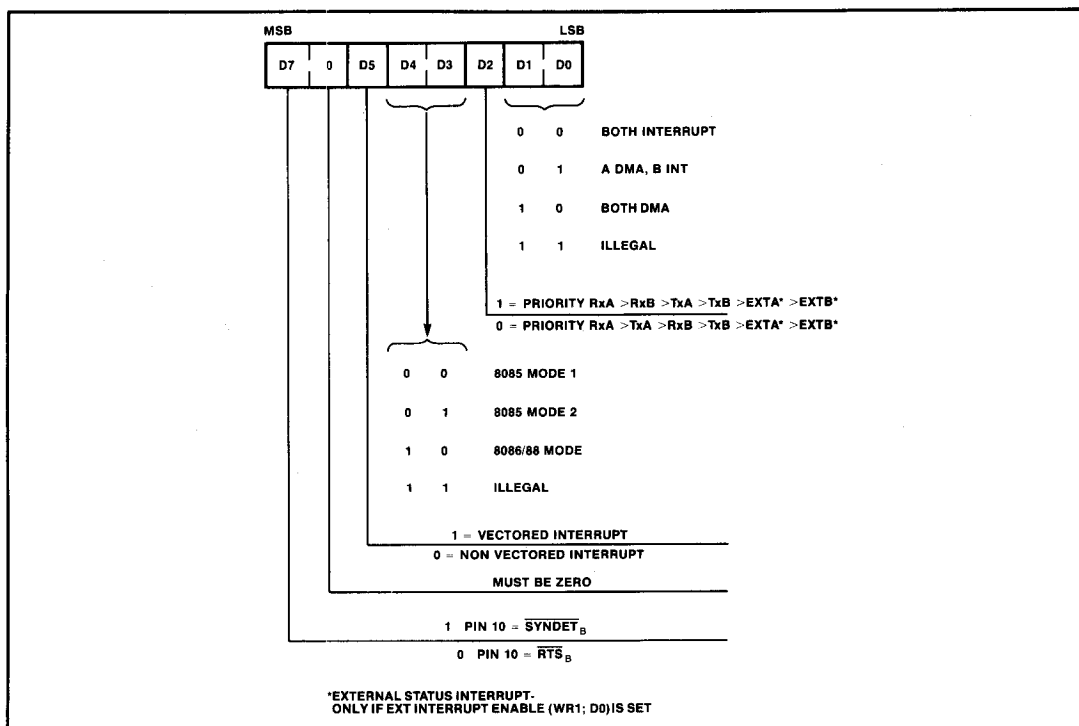
Must be Zero

D7

Wait Enable—enables the wait function.

WR2	Channel A	D5, D4, D3	
D1, D0	System Configuration—These specify the data transfer from MPSC channels to the CPU, either interrupt or DMA based.		Interrupt Code—specifies the behavior of the MPSC when it receives an interrupt acknowledge sequence from the CPU. (See Interrupt Vector Mode Table).
0 0	Channel A and Channel B both use interrupts	0 X X	Non-vectorized interrupts—intended for use with external DMA CONTROLLER. The Data Bus remains in a high impedance state during INTA sequences.
0 1	Channel A uses DMA, Channel B uses interrupt		
1 0	Channel A and Channel B both use DMA	1 0 0	8085 Vector Mode 1—intended for use as the primary MPSC in a daisy chained priority structure. (See System Interface section)
1 1	Illegal Code	1 0 1	8085 Vector Mode 2—intended for use as any secondary MPSC in a daisy chained priority structure. (See System Interface section)
D2	Priority—this bit specifies the relative priorities of the internal MPSC interrupt/DMA sources.	1 1 0	8086/88 Vector Mode—intended for use as either a primary or secondary in a daisy chained priority structure. (See System Interface section)
0	(Highest) RxA, TxA, RxB, TxB ExTA, ExTB (Lowest)		
1	(Highest) RxA, RxB, TxA, TxB, ExTA, ExTB (Lowest)		
		D7, D6	Must be zero.

**Write Register 2 (WR2): Channel A**



The following table describes the MPSC's response to an interrupt acknowledge sequence:

D5	D4	D3	$\overline{\text{IP}}\overline{\text{I}}$	MODE	INTA	Data Bus
0	X	X	X	Non-vector	Any INTA	D7 D0 High Impedance
1	0	0	0	85 Mode 1	1st INTA 2nd INTA 3rd INTA	1 1 0 0 1 1 0 1 V7 V6 V5 V4* V3* V2* V1 V0 0 0 0 0 0 0 0 0
1	0	0	1	85 Mode 1	1st INTA 2nd INTA 3rd INTA	1 1 0 0 1 1 0 1 High Impedance High Impedance
1	0	1	0	85 Mode 2	1st INTA 2nd INTA 3rd INTA	High Impedance High Impedance High Impedance
1	1	0	0	86 Mode	1st INTA	High Impedance V7 V6 V5 V4 V3 V2* V1*V0*
1	1	0	1	86 Mode	1st INTA 2nd INTA	High Impedance High Impedance

\*These bits are variable if the "status affects vector" mode has been programmed, (WR1B, p.2).

#### Interrupt/DMA Mode, Pin Functions, and Priority

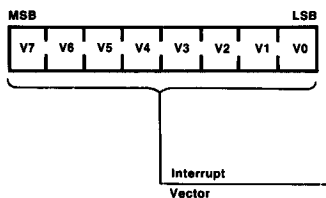
Ch. A WR2			Int/DMA Mode		RDY <sub>A</sub> / RxDRQ <sub>A</sub> Pin 32	Pin Functions		I $\overline{\text{P}}\overline{\text{O}}$ / TxDRQ <sub>B</sub> Pin 30	Priority
D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	CH. A	CH. B		RDY <sub>B</sub> / TxDRQ <sub>A</sub> Pin 11	$\overline{\text{IP}}\overline{\text{I}}$ / RxDRQ <sub>B</sub> Pin 29		
0	0	0	INT	INT	RDY <sub>A</sub>	RDY <sub>B</sub>	$\overline{\text{IP}}\overline{\text{I}}$	$\overline{\text{I}}\overline{\text{P}}\overline{\text{O}}$	Highest Lowest Rx <sub>A</sub> , Tx <sub>A</sub> , Rx <sub>B</sub> , Tx <sub>B</sub> , EXT <sub>A</sub> , EXT <sub>B</sub>
1	0	0	INT	INT					Rx <sub>A</sub> , Rx <sub>B</sub> , Tx <sub>A</sub> , Tx <sub>B</sub> , EXT <sub>A</sub> , EXT <sub>B</sub>
0	0	1	DMA	INT	RxDRQ <sub>A</sub>	TxDRQ <sub>A</sub>	$\overline{\text{IP}}\overline{\text{I}}$	$\overline{\text{I}}\overline{\text{P}}\overline{\text{O}}$	Rx <sub>A</sub> , Tx <sub>A</sub> (DMA) Rx <sub>A</sub> <sup>1</sup> , Rx <sub>B</sub> , Tx <sub>B</sub> , EXT <sub>A</sub> , EXT <sub>B</sub> (INT)
1	0	1	DMA	INT					Rx <sub>A</sub> , Tx <sub>A</sub> (DMA) Rx <sub>A</sub> <sup>1</sup> , Rx <sub>B</sub> , Tx <sub>B</sub> , EXT <sub>A</sub> , EXT <sub>B</sub> (INT)
0	1	0	DMA	DMA	RxDRQ <sub>A</sub>	TxDRQ <sub>A</sub>	RxDRQ <sub>B</sub>	TxDRQ <sub>B</sub>	Rx <sub>A</sub> , Tx <sub>A</sub> , Rx <sub>B</sub> , Tx <sub>B</sub> (DMA) Rx <sub>A</sub> <sup>1</sup> , Rx <sub>B</sub> <sup>1</sup> , EXT <sub>A</sub> , EXT <sub>B</sub> (INT)
1	1	0	DMA	DMA					Rx <sub>A</sub> , Rx <sub>B</sub> , Tx <sub>A</sub> , Tx <sub>B</sub> (DMA) Rx <sub>A</sub> <sup>1</sup> , Rx <sub>B</sub> <sup>1</sup> , EXT <sub>A</sub> , EXT <sub>B</sub> (INT)

<sup>1</sup>Special Receive Condition

Interrupt Vector Mode Table

8085 Modes 8086/88 Mode	V <sub>4</sub> V <sub>2</sub>	V <sub>3</sub> V <sub>1</sub>	V <sub>2</sub> V <sub>0</sub>	Channel	Condition
Note 1: Special Receive Condition= Parity Error, Rx Overrun Error, Framing Error, End of Frame (SDLC)	0	0	0	B	Tx Buffer Empty Ext/Status Change Rx Char. Available Special Rx Condition (Note 1)
	0	0	1		
	0	1	0		
	0	1	1		
	1	0	0	A	Tx Buffer Empty Ext/Status Change Rx Char. Available Special Rx Condition (Note 1)
	1	0	1		
	1	1	0		
	1	1	1		

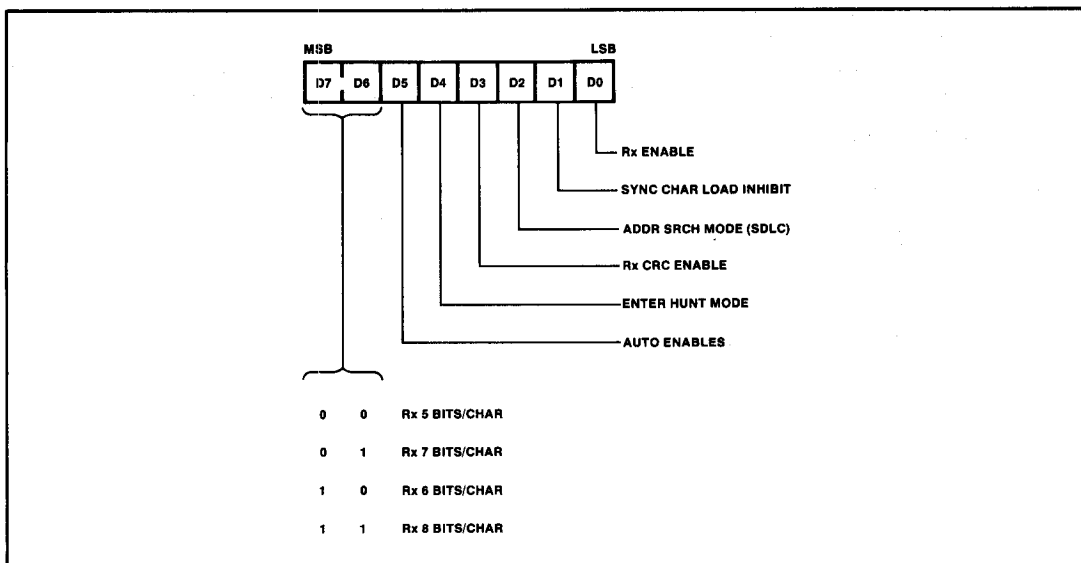
## Write Register 2 (WR2): Channel B



## WR2 CHANNEL B

D7–D0 Interrupt vector—This register contains the value of the interrupt vector placed on the data bus during interrupt acknowledge sequences.

## Write Register 3 (WR3):



**WR3**

**D0** Receiver Enable—A one enables the receiver to begin. This bit should be set only after the receiver has been initialized.

**D1** Sync Character Load Inhibit—A one prevents the receiver from loading sync characters into the receive buffers.

**D2** Address Search Mode—If the SDLC mode has been selected, the MPSC will receive all frames unless this bit is a 1. If this bit is a 1, the MPSC will receive only frames with address bytes that match the global address (0FFH) or the value loaded into WR6. This bit must be zero in non-SDLC modes.

**D3** Receive CRC Enable—A one in this bit enables (or re-enables) CRC calculation. CRC calculation starts with the last character placed in the Receiver FIFO. A zero in this bit disables, but does not reset, the Receiver CRC generator.

**D4** Enter Hunt Phase—After initialization, the MPSC automatically enters the Hunt mode. If synchronization is lost, the Hunt phase can be re-entered by writing a one to this bit.

**D5** Auto Enables—A one written to this bit causes  $\overline{CD}$  to be automatic enable signal for the receiver and  $\overline{CTS}$  to be an automatic enable signal for the transmitter. A zero written to this bit limits the effect of  $\overline{CD}$  and  $\overline{CTS}$  signals to setting/resetting their corresponding bits in the status register (RR0).

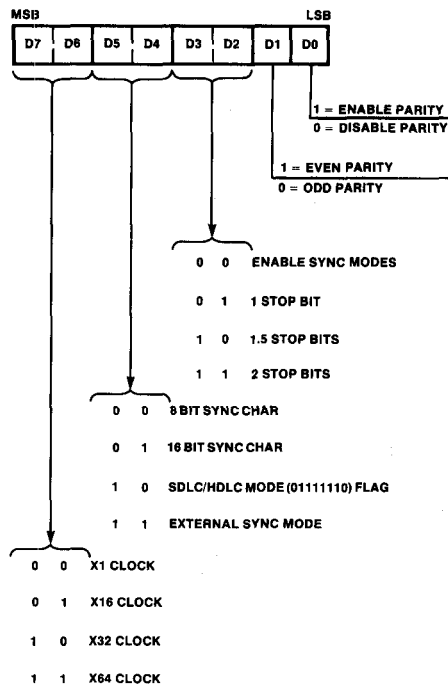
**D7, D6** Receive Character length

0 0 Receive 5 Data bits/character

0 1 Receive 7 Data bits/character

1 0 Receive 6 Data bits/character

1 1 Receive 8 Data bits/character

**Write Register 4 (WR4):****WR4**

**D0**

Parity—a one in this bit causes a parity bit to be added to the programmed number of data bits per character for both the transmitted and received character. If the MPSC is programmed to receive 8 bits per character, the parity bit is not transferred to the microprocessor. With other receiver character lengths, the parity bit is transferred to the microprocessor.

**D1**

Even/Odd Parity—if parity is enabled, a one in this bit causes the MPSC to transmit and expect even parity, and a zero causes it to send and expect odd parity.

**D3, D2** Stop bits/sync mode

- 0 0 Selects synchronous modes.
- 0 1 Async mode, 1 stop bit/character
- 1 0 Async mode, 1-½ stop bits/character
- 1 1 Async mode, 2 stop bits/character

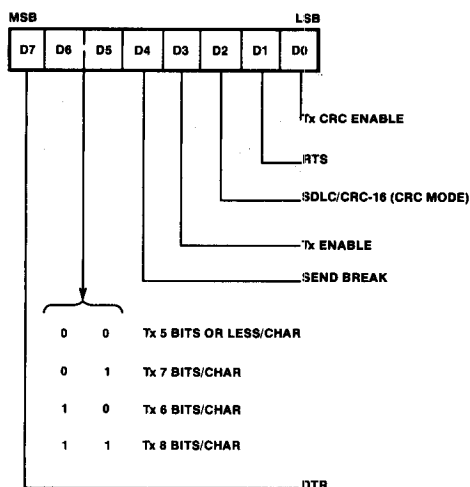
D5, D4 Sync mode select

- 0 0 8 bit sync character
- 0 1 16 bit sync character
- 1 0 SDLC mode (Flag sync)
- 1 1 External sync mode

D7, D6 Clock mode—selects the clock/data rate multiplier for both the receiver and the transmitter. 1x mode must be selected for synchronous modes. If the 1x mode is selected, bit synchronization must be done externally.

- 0 0 Clock rate = Data rate x 1
- 0 1 Clock rate = Data rate x 16
- 1 0 Clock rate = Data rate x 32
- 1 1 Clock rate = Data rate x 64

Write Register 5 (WR5):



WR5

D0 Transmit CRC Enable—a one in this bit enables the transmitter CRC generator. The CRC calculation is done when a character is moved from the transmit buffer into the shift register. A zero in this bit disables CRC calculations. If this bit is not set when a transmitter underrun occurs, the CRC will not be sent.

D1 Request to Send—a one in this bit forces the  $\overline{\text{RTS}}$  pin active (low) and zero in this bit forces the  $\overline{\text{RTS}}$  pin inactive (high).

D2 CRC Select—a one in this bit selects the CRC —16 polynomial ( $X^{16} + X^{15} + X^2 + 1$ ) and a zero in this bit selects the CCITT-CRC polynomial ( $X^{16} + X^{15} + X^5 + 1$ ).

D3 Transmitter Enable—a zero in this bit forces a marking state on the transmitter output. If this bit is set to zero during data or sync character transmission, the marking state is entered after the character has been sent. If this bit is set to zero during transmission of a CRC character, sync or flag bits are substituted for the remainder of the CRC bits.

D4 Send Break—a one in this bit forces the transmit data low. A one in this bit allows normal transmitter operation.

D6, D5 Transmit Character length

- 0 0 Transmit 5 or less bits/character
- 0 1 Transmit 7 bits/character
- 1 0 Transmit 6 bits/character
- 1 1 Transmit 8 bits/character

Bits to be sent must be right justified least significant bit first, eg:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	B5	B4	B3	B2	B1	B0

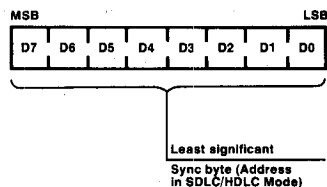


Five or less mode allows transmission of one to five bits per character. The microprocessor must format the data in the following way:

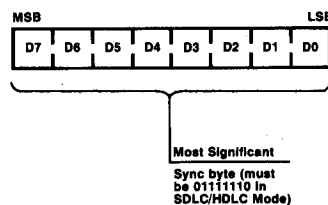
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	B0	Sends one data bit
1	1	1	0	0	0	B1	B0	Sends two data bits
1	1	0	0	0	B2	B1	B0	Sends three data bits
1	0	0	0	B3	B2	B1	B0	Sends four data bits
0	0	0	B4	B3	B2	B1	B0	Sends five data bits

**D7** Data Terminal Ready—when set, this bit forces the  $\overline{\text{DTR}}$  pin active (low). When reset, this bit forces the  $\overline{\text{DTR}}$  pin inactive (high).

#### Write Register 6 (WR6):



#### Write Register 7 (WR7):



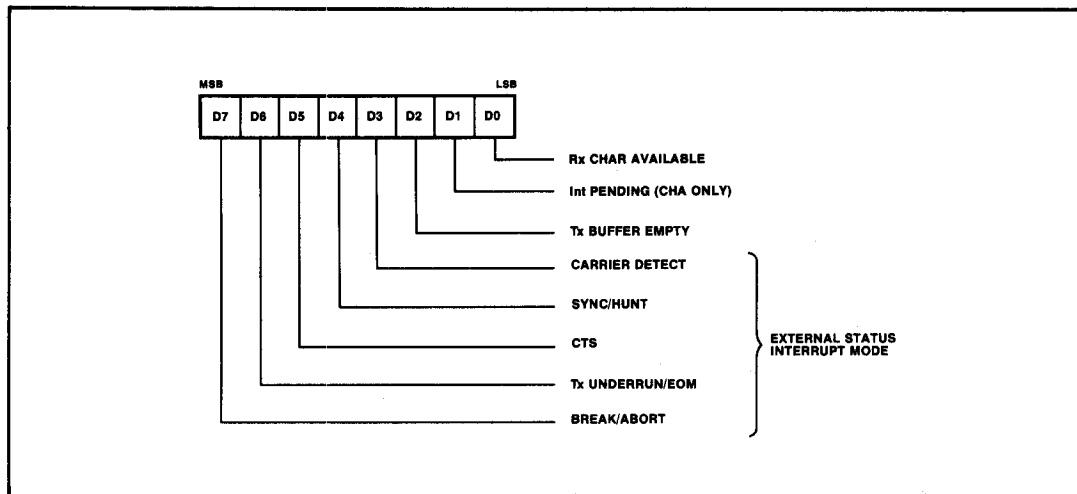
#### WR6

**D7-D0** Sync/Address—this register contains the transmit sync character in Monosync mode, the low order 8 sync bits in Bisync mode, or the Address byte in SDLC mode.

#### WR7

**D7-D0** Sync/Flag—this register contains the receive sync character in Monosync mode, the high order 8 sync bits in Bisync mode, or the Flag character (01111110) in SDLC mode. WR7 is not used in External Sync mode.

## Read Register 0 (RR0):



## RR0

- D0** Receive Character Available—this bit is set when the receive FIFO contains data and is reset when the FIFO is empty.
- D1** Interrupt Pending\*—This Interrupt-Pending bit is reset when an EOI command is issued and there is no other interrupt request pending at that time.
- D2** Transmit Buffer Empty—This bit is set whenever the transmit buffer is empty except when CRC characters are being sent in a synchronous mode. This bit is reset when the transmit buffer is loaded. This bit is set after an MPSC reset.
- D3** Carrier Detect—This bit contains the state of the CD pin at the time of the last change of any of the External/Status bits (CD, CTS, Sync/Hunt, Break/Abort, or Tx Underrun/EOM). Any change of state of the CD pin causes the CD bit to be latched and causes an External/Status interrupt. This bit indicates current state of the CD pin immediately following a Reset External/Status Interrupt command.

- D4** Sync/Hunt—In asynchronous modes, the operation of this bit is similar to the CD status bit, except that Sync/Hunt shows the state of the SYNDET input. Any High-to-Low transition on the SYNDET pin sets this bit, and causes an External/Status interrupt (if enabled). The Reset External/Status Interrupt command is issued to clear the interrupt. A Low-to-High transition clears this bit and sets the External/Status interrupt. When the External/Status interrupt is set by the change in state of any other input or condition, this bit shows the inverted state of the SYNDET pin at time of the change. This bit must be read immediately following a Reset External/Status Interrupt command to read the current state of the SYNDET input.

In the External Sync mode, the Sync/Hunt bit operates in a fashion similar to the Asynchronous mode, except the Enter Hunt Mode control bit enables the external sync detection logic. When the External Sync Mode and Enter Hunt Mode bits are set (for example, when the receiver is enabled following a reset), the SYNDET input must be held High by the external logic until external character synchronization is achieved. A High at the SYNDET input holds the Sync/Hunt status in the reset condition.

\*In vector mode this bit is set at the falling edge of the second INTA in an INTA cycle for an internal interrupt request. In non-vector mode, this bit is set at the falling edge of RD input after pointer 2 is specified. This bit is always zero in Channel B.

When external synchronization is achieved, SYNDET must be driven Low on the second rising edge of RxC after the rising edge of RxC on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the SYNDET input. Once SYNDET is forced Low, it is good practice to keep it Low until the CPU informs the external sync logic that synchronization has been lost or a new message is about to start. The High-to-Low transition of the SYNDET output sets the Sync/Hunt bit, which sets the External/Status interrupt. The CPU must clear the interrupt by issuing the Reset External/Status Interrupt Command.

When the SYNDET input goes High again, another External/Status interrupt is generated that must also be cleared. The Enter Hunt Mode control bit is set whenever character synchronization is lost or the end of message is detected. In this case, the MPSC again looks for a High-to-Low transition on the SYNDET input and the operation repeats as explained previously. This implies the CPU should also inform the external logic that character synchronization has been lost and that the MPSC is waiting for SYNDET to become active.

In the Monosync and Bisync Receive modes, the Sync/Hunt status bit is initially set to 1 by the Enter Hunt Mode bit. The Sync/Hunt bit is reset when the MPSC establishes character synchronization. The High-to-Low transition of the Sync/Hunt bit causes an External/Status interrupt that must be cleared by the CPU issuing the Reset External/Status Interrupt command. This enables the MPSC to detect the next transition of other External/Status bits.

When the CPU detects the end of message or that character synchronization is lost, it sets the Enter Hunt Mode control bit, which sets the Sync/Hunt bit to 1. The Low-to-High transition of the Sync/Hunt bit sets the External/Status Interrupt, which must also be cleared by the Reset External/Status Interrupt Command. Note that the SYNDET pin acts as an output in this mode, and goes low every time a sync pattern is detected in the data stream.

In the SDLC mode, the Sync/Hunt bit is initially set by the Enter Hunt mode bit, or when the receiver is disabled. In any case, it is reset to 0 when the opening flag of the first frame is detected by the MPSC. The External/Status interrupt is also generated, and should be handled as discussed previously.

Unlike the Monosync and Bisync modes, once the Sync/Hunt bit is reset in the SDLC mode, it does not need to be set when the end of message is detected. The MPSC automatically maintains synchronization. The only way the Sync/Hunt bit can be set again is by the Enter Hunt Mode bit, or by disabling the receiver.

- D5 Clear to Send—this bit contains the inverted state of the CTS pin at the time of the last change of any of the External/Status bits (CD, CTS, Sync/Hunt, Break/Abort, or Tx Underrun/EOM). Any change of state of the CTS pin causes the CTS bit to be latched and causes an External/Status interrupt. This bit indicates the inverse of the current state of the CTS pin immediately following a Reset External/Status Interrupt command.
- D6 Transmitter Underrun/End of Message—this bit is in a set condition following a reset (internal or external). The only command that can reset this bit is the Reset Transmit Underrun/EOM Latch command (WR0, D<sub>6</sub> and D<sub>7</sub>). When the Transmit Underrun condition occurs, this bit is set, which causes the External/Status Interrupt which must be reset by issuing a Reset External/Status command (WR0; command 2).
- D7 Break/Abort—in the Asynchronous Receive mode, this bit is set when a Break sequence (null character plus framing error) is detected in the data stream. The External/Status interrupt, if enabled, is set when break is detected. The interrupt service routine must issue the Reset External/Status Interrupt command (WR0, Command 2) to the break detection logic so the Break sequence termination can be recognized.

SDLC Residue Code Table (I Field Bits in 2 Previous Bytes)

	8 bits/char		7 bits/char		6 bits/char		5 bits/char	
RR1 D3, D2, D1	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte	Previous Byte	2nd Prev. Byte
1 0 0	0	3						
0 1 0	0	4			0	6		
1 1 0	0	5						
0 0 1	0	6					0	5
1 0 1	0	7						
0 1 1	0	8						
1 1 1	1	8						
0 0 0	2	8	0	7				

The Break/Abort bit is reset when the termination of the Break sequence is detected in the incoming data stream. The termination of the Break sequence also causes the External/Status interrupt to be set. The Reset External/Status Interrupt command must be issued to enable the break detection logic to look for the next Break sequence. A single extraneous null character is present in the receiver after the termination of a break; it should be read and discarded.

In the SDLC Receive mode, this status bit is set by the detection of an Abort sequence (seven or more 1's). The External/Status interrupt is handled the same way as in the case of a Break. The Break/Abort bit is not used in the Synchronous Receive mode.

D0

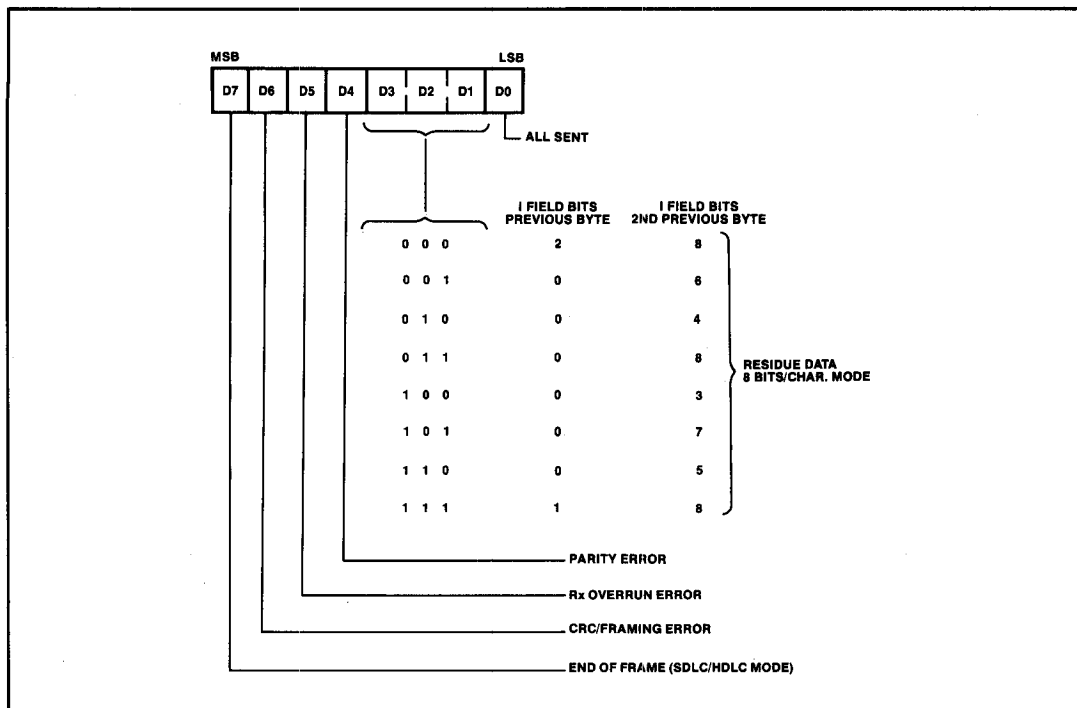
All sent—this bit is set when all characters have been sent, in asynchronous modes. It is reset when characters are in the transmitter, in asynchronous modes. In synchronous modes, this bit is always set.

D3, D2, D1 Residue Codes—bit synchronous protocols allow I-fields that are not an integral number of characters. Since transfers from the MPSC to the CPU are character oriented, the residue codes provide the capability of receiving leftover bits. Residue bits are right justified in the last two data bytes received.

D4

Parity Error—If parity is enabled, this bit is set for received characters whose parity does not match the programmed sense (Even/Odd). This bit is latched. Once an error occurs, it remains set until the Error Reset command is written.

**Read Register 1 (RR1): (Special Receive Condition Mode)**



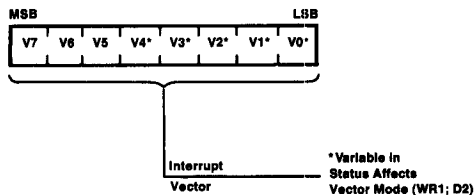
**D5** Receive Overrun Error—this bit indicates that the receive FIFO has been overloaded by the receiver. The last character in the FIFO is overwritten and flagged with this error. Once the overwritten character is read, this error condition is latched until reset by the Error Reset command. If the MPSC is in the status affects vector mode, the overrun causes a special Receive Condition Vector.

**D6** CRC/Framing Error—In async modes, a one in this bit indicates a receive fram-

ing error. In synchronous modes, a one in this bit indicates that the calculated CRC value does not match the last two bytes received. It can be reset by issuing an Error Reset command.

**D7** End of Frame—this bit is valid only in SDLC mode. A one indicates that a valid ending flag has been received. This bit is reset either by an Error Reset command or upon reception of the first character of the next frame.

### Read Register 2 (RR2):



### RR2 Channel B

**D7-D0** Interrupt vector—contains the interrupt vector programmed into WR2. If the status affects vector mode is selected, it contains the modified vector. (See WR2) RR2 contains the modified vector for the highest priority interrupt pending. If no interrupts are pending, the variable bits in the vector are set to one.

## SYSTEM INTERFACE

### General

The MPSC to Microprocessor System interface can be configured in many flexible ways. The basic interface types are polled, wait, interrupt driven, or direct memory access driven.

Polled operation is accomplished by repetitively reading the status of the MPSC, and making decisions based on that status. The MPSC can be polled at any time.

Wait operation allows slightly faster data throughput for the MPSC by manipulating the Ready input to the microprocessor. Block Read or Write Operations to the MPSC are started at will by the microprocessor and the MPSC deactivates its RDY signal if it is not yet ready to transmit the new byte, or if reception of new byte is not completed.

Interrupt driven operation is accomplished via an internal or external interrupt controller. When the MPSC requires service, it sends an interrupt request signal to the microprocessor, which responds with an interrupt acknowledge signal. When the internal or external interrupt controller receives the acknowledge, it vectors the microprocessor to a service routine, in which the transaction occurs.

DMA operation is accomplished via an external DMA controller. When the MPSC needs a data transfer, it request a DMA cycle from the DMA controller. The DMA controller then takes control of the bus and simultaneously does a read from the MPSC and a write to memory or vice-versa.

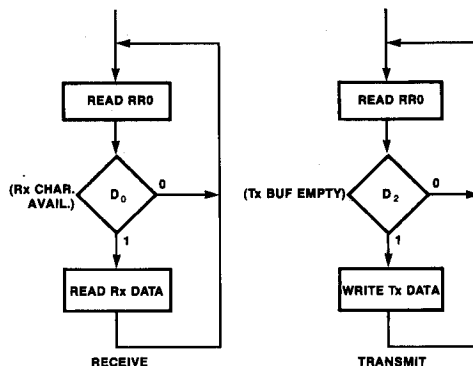
The following section describes the many configurations of these basic types of system interface techniques for both serial channels.

### Polled Operation:

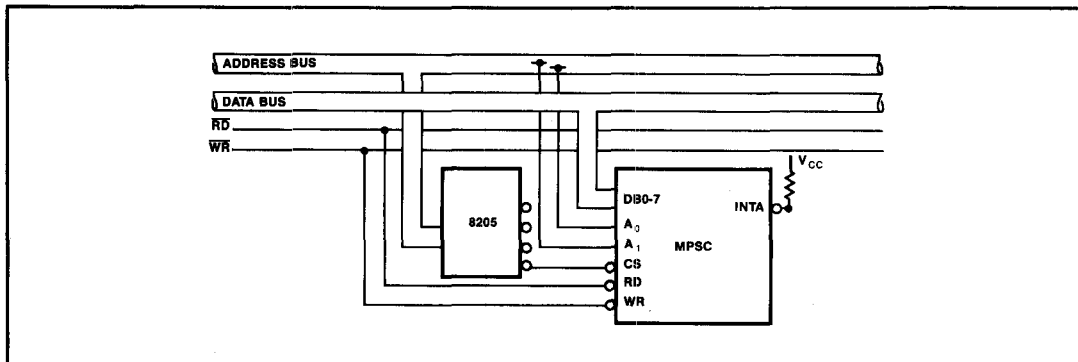
In the polled mode, the CPU must monitor the desired conditions within the MPSC by reading the appropriate bits in the read registers. All data available, status, and error conditions are represented by the appropriate bits in read registers 0 and 1 for channels A and B.

There are two ways in which the software task of monitoring the status of the MPSC has been reduced. One is the "ORing" of all conditions into the Interrupt Pending bit. (RR0; D1 channel A only). This bit is set when the MPSC requires service, allowing the CPU to monitor one bit instead of four status registers. The other is available when the "status-affects-vector" mode is selected. By reading RR2 Channel B, the CPU can read a vector who's value will indicate that one or more of group of conditions has occurred, narrowing the field of possible conditions. See WR2 and RR2 in the Detailed Command Description section.

### Software Flow, Polled Operation



## Hardware Configuration, Polled Operation



### WAIT OPERATION:

Wait Operation is intended to facilitate data transmission or reception using block move operations. If a block of data is to be transmitted, for example, the CPU can execute a String I/O instruction to the MPSC. After writing the first byte, the CPU will attempt to write a second byte immediately as is the case of block move. The MPSC forces the RDY signal low which inserts wait states in the CPU's write cycle until the transmit buffer is ready to accept a new byte. At that time, the RDY signal is high allowing the CPU to finish the write cycle. The CPU then attempts the third write and the process is repeated.

Similar operation can be programmed for the receiver. During initialization, wait on transmit (WR2; D5 = 0) or wait on receive (WR1; D5 = 1) can be selected. The wait operation can be enabled/disabled by setting/resetting the Wait Enable Bit (WR1; D7).

**CAUTION:** ANY CONDITION THAT CAN CAUSE THE TRANSMITTER TO STOP (EG, CTS GOES INACTIVE) OR THE RECEIVER TO STOP (EG, RX DATA STOPS) WILL CAUSE THE MPSC TO HANG THE CPU UP IN WAIT STATES UNTIL RESET. EXTREME CARE SHOULD BE TAKEN WHEN USING THIS FEATURE.

### INTERRUPT DRIVEN OPERATION:

The MPSC can be programmed into several interrupt modes: Non-Vectored, 8085 vectored, and 8088/86 vectored. In both vectored modes, multiple MPSC's can be daisy-chained.

In the vectored mode, the MPSC responds to an interrupt acknowledge sequence by placing a call instruction (8085 mode) and interrupt vector (8085

and 8088/86 mode) on the data bus. In the non-vectored mode, the MPSC does not respond to  $\overline{\text{INTA}}$  sequences and must rely on an external interrupt controller such as the 8259A.

The MPSC can be programmed to cause an interrupt due to up to 14 conditions in each channel. The status of these interrupt conditions is contained in Read Registers 0 and 1. These 14 conditions are all directed to cause 3 different types of internal interrupt request for each channel: receive/interrupts, transmit interrupts and external/status interrupts (if enabled).

This results in up to 6 internal interrupt request signals. The priority of those signals can be programmed to one of two fixed modes:

Highest Priority	Lowest Priority
RxA RxB TxA TxB ExTA ExTB	
RxA TxA RxB TxB ExTA ExTB	

The interrupt priority resolution works differently for vectored and non-vectored modes.

### PRIORITY RESOLUTION: VECTORED MODE

Any interrupt condition can be accepted internally to the MPSC at any time, unless the MPSC's internal  $\overline{\text{INTA}}$  signal is active, unless a higher priority interrupt is currently accepted, or if  $\overline{\text{IPI}}$  is inactive (high). The MPSC's internal  $\overline{\text{INTA}}$  is set on the leading (falling) edge of the first External  $\overline{\text{INTA}}$  pulse and reset on the trailing (rising) edge of the second External  $\overline{\text{INTA}}$  pulse. After an interrupt is accepted internally, an External  $\overline{\text{INT}}$  request is generated and the  $\overline{\text{IPO}}$  goes inactive.  $\overline{\text{IPO}}$  and  $\overline{\text{IPI}}$  are used for daisy-chaining MPSC's together.

```

graph LR
    subgraph CONDITION
        RC[RECEIVE CHARACTER]
        PE[PARITY ERROR]
        ROE[RECEIVE OVERRUN ERROR]
        FE[FRAMING ERROR]
        EOF[END OF FRAME (SDLC ONLY)]
        FDC[FIRST DATA CHARACTER]
        FNSC[FIRST NON-SYNC CHARACTER (SYNC MODES)]
        VAB[VALID ADDRESS BYTE (SDLC ONLY)]
    end

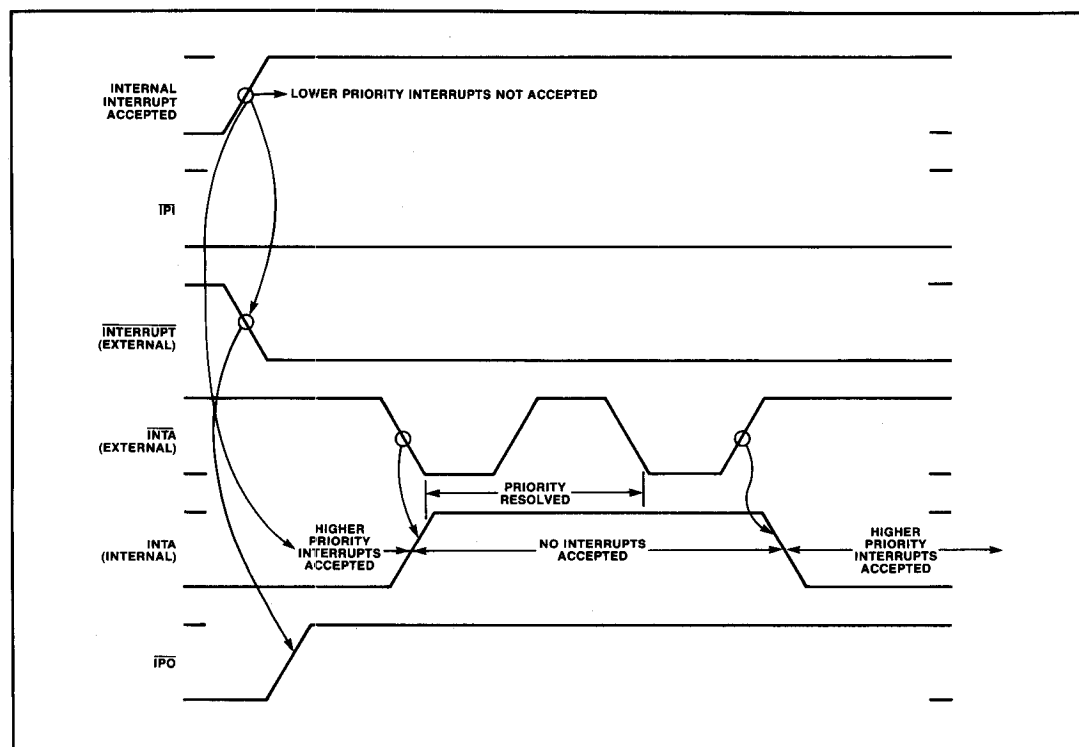
    subgraph MODE
        CD[CD TRANSITION]
        CTS[CTS TRANSITION]
        ST[SYNC TRANSITION]
        TUE[Tx UNDERRUN/EOM]
        BAD[BREAK/ABORT DETECT]
    end

    IIR[INTERNAL INTERRUPT REQUEST]

    SCIB[SPECIAL RECEIVE CONDITION INTERRUPT]
    IARC[INTERRUPT ON ALL RECEIVE CHARACTERS]
    IFRC[INTERRUPT ON FIRST Rx CHARACTER]

    SCIB --> RI[RECEIVE INTERRUPT]
    IARC --> RI
    IFRC --> RI
    IARC --> ESI[EXTERNAL/STATUS INTERRUPT]
    IFRC --> ESI
    IARC --> TI[TRANSMIT INTERRUPT]
    IFRC --> TI

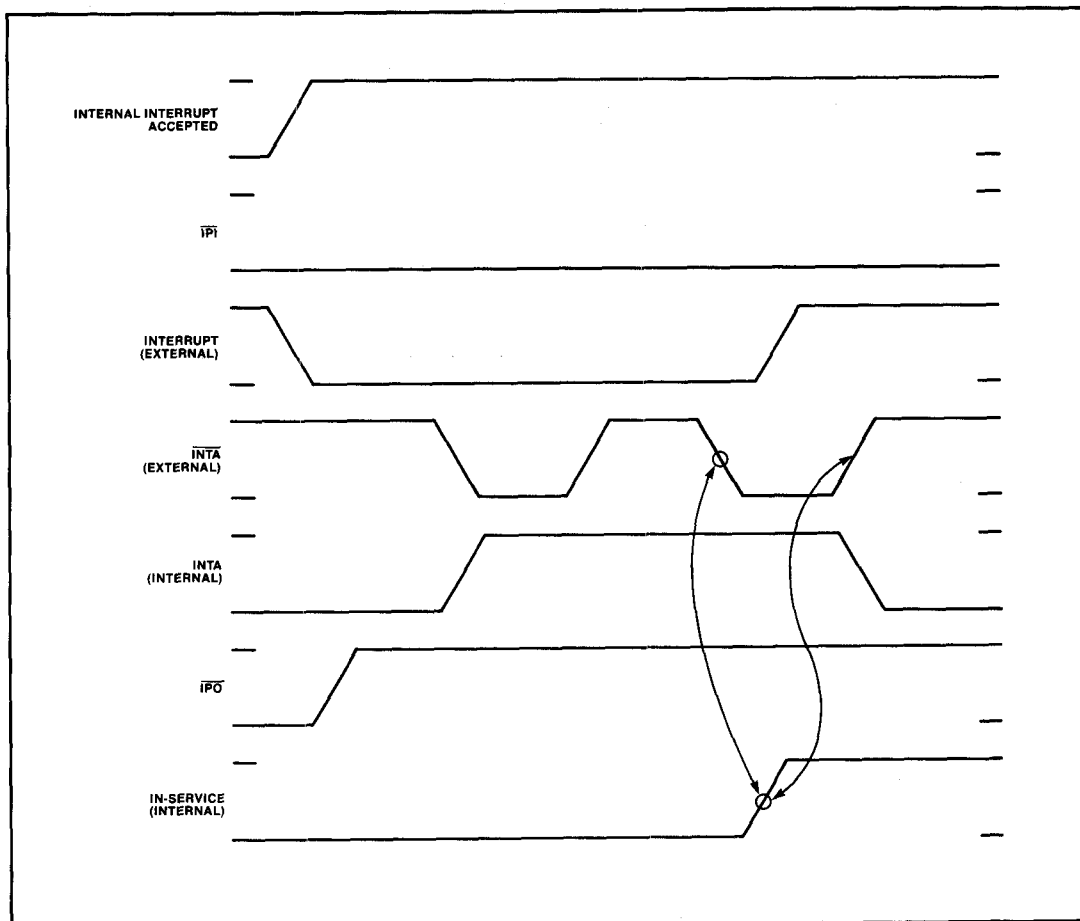
    RC --> SCIB
    RC --> IARC
    RC --> IFRC
    PE --> SCIB
    ROE --> SCIB
    FE --> SCIB
    EOF --> SCIB
    FDC --> IFRC
    FNSC --> IFRC
    VAB --> IFRC
    CD --> ESI
    CTS --> ESI
    ST --> ESI
    TUE --> ESI
    BAD --> ESI
    IIR --> RI
    IIR --> ESI
    IIR --> TI
  
```



an external  $\overline{\text{INT}}$  request is generated and  $\overline{\text{IPO}}$  goes inactive (high).  $\overline{\text{IPO}}$  and  $\overline{\text{IPI}}$  are used for daisy-chaining MPSC's together.



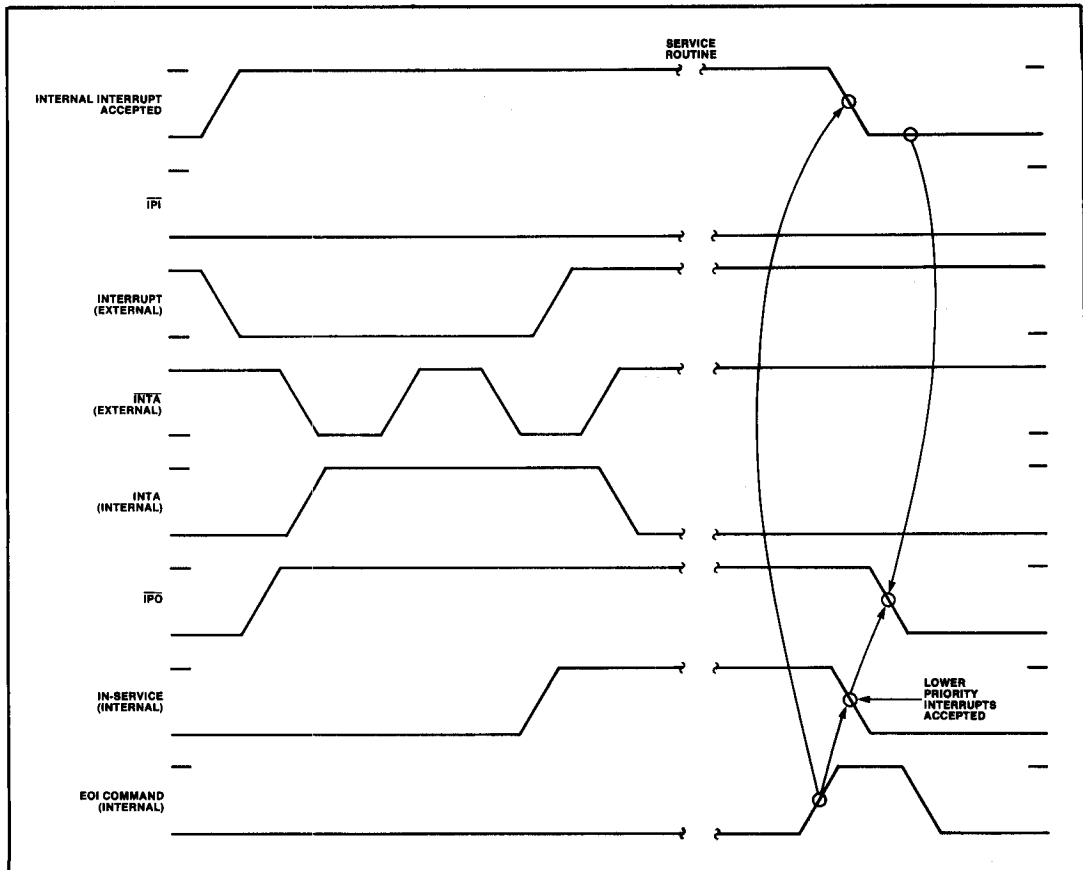
## In-Service Timing



Each of the six interrupt sources has an associated In-Service latch. After priority has been resolved, the

highest priority In-Service latch is set. After the In-Service latch is set, the  $\overline{INT}$  pin goes inactive (high).

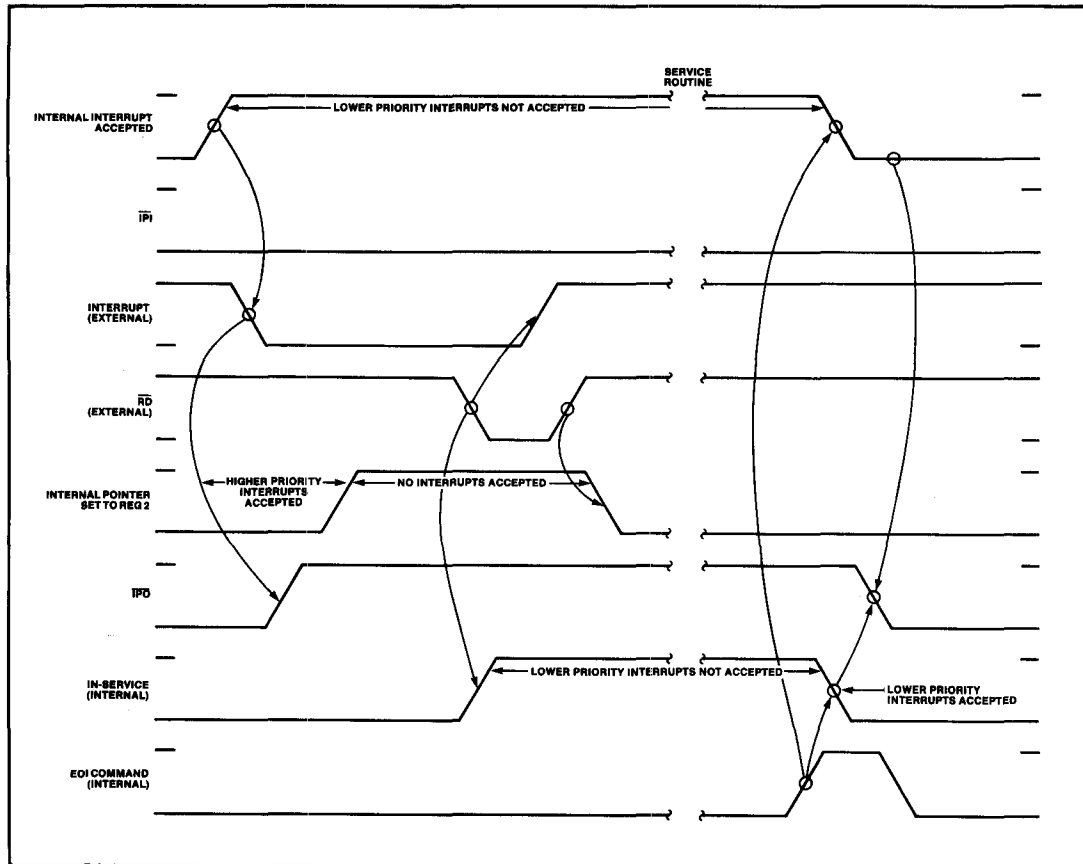
## EOI Command Timing



Lower priority interrupts are not accepted internally while the In-Service latch is set. However, higher priority interrupts are accepted internally and a new external INT request is generated. If the CPU responds with a new INTA sequence, the MPSC will respond as before, suspending the lower priority interrupt.

After the interrupt is serviced, the End-of-Interrupt (EOI) command should be written to the MPSC. This command will cause an internal pulse that is used to reset the In-Service Latch which allows service for lower priority interrupts in the daisy-chain to resume, provided a new INTA sequence does not start for a higher priority interrupt (higher than the highest under service). If there is no interrupt pending internally, the IPO follows IPI.

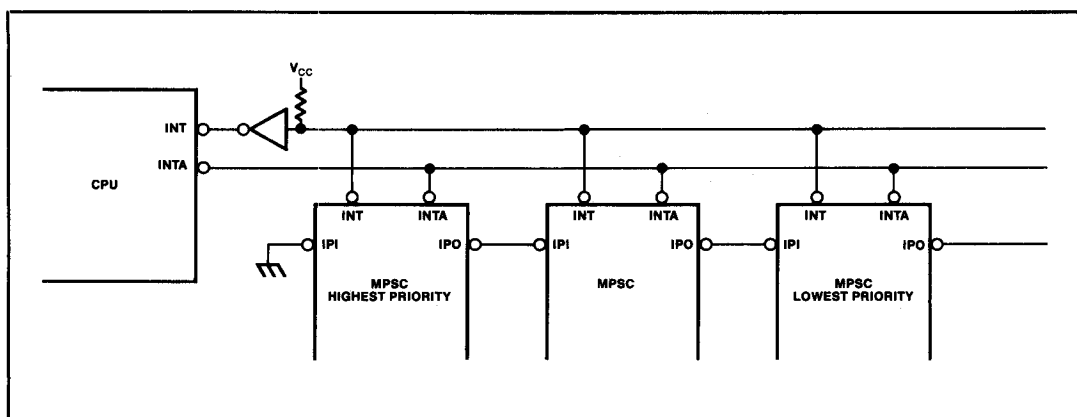
# Non-Vectored Interrupt Timing



## PRIORITY RESOLUTION: NON-VECTORED MODE

In non-vectored mode, the MPSC does not respond to interrupt acknowledge sequences. The MPSC should be programmed to the Status-Affects-Vector mode, and the CPU should read RR2 (Ch. B) in its service routine to determine which interrupt requires service.

In this case, the internal pointer being set to RR2 provides the same function as the internal INTA signal in the vectored mode. It inhibits acceptance of any additional internal interrupts and its leading edge starts the interrupt priority resolution circuit. The interrupt priority resolution is ended by the leading edge of the read signal used by the CPU to retrieve the modified vector. The leading edge of read sets the In-Service latch and forces the external  $\overline{\text{INT}}$  output inactive (high). The internal pointer is reset to zero after the trailing edge of the read pulse.



Note that if  $\overline{RR2}$  is specified but not read, no internal interrupts, regardless of priority, are accepted.

#### DAISY CHAINING MPSC:

In the vectored interrupt mode, multiple MPSC's can be daisy-chained on the same  $\overline{INT}$ ,  $\overline{INTA}$  signals. These signals, in conjunction with the  $\overline{IPI}$  and  $\overline{IPO}$  allow a daisy-chain-like interrupt resolution scheme. This scheme can be configured for either 8085 or 8086/88 based system.

In either mode, the same hardware configuration is called for. The  $\overline{INT}$  request lines are wire-OR'ed together at the input of a TTL inverter which drives the  $\overline{INT}$  pin of the CPU. The  $\overline{INTA}$  signal from the CPU drives all of the daisy-chained MPSC's.

The MPSC drives  $\overline{IPO}$  (Interrupt Priority Output) inactive (high) if  $\overline{IPI}$  (Interrupt Priority Input) is inactive (high), or if the MPSC has an interrupt pending.

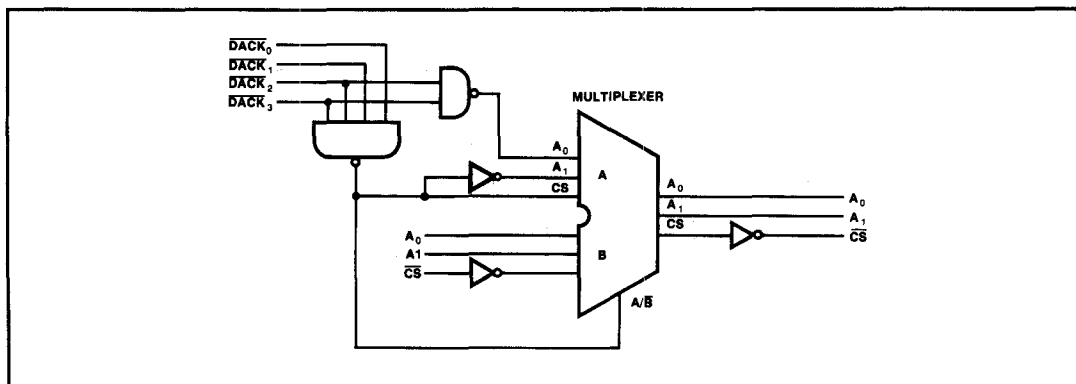
The  $\overline{IPO}$  of the highest priority MPSC is connected to the  $\overline{IPI}$  of the next highest priority MPSC, and so on.

If  $\overline{IPI}$  is active (low), the MPSC knows that all higher priority MPSC's have no interrupts pending. The  $\overline{IPI}$  pin of the highest priority MPSC is strapped active (low) to ensure that it always has priority over the rest.

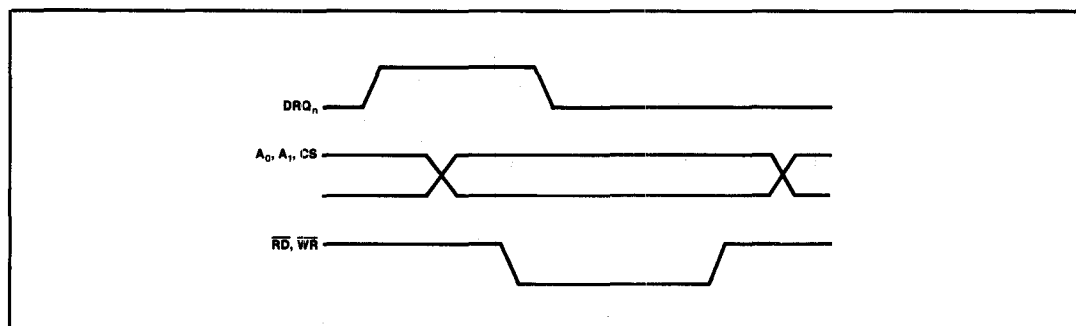
MPSC's Daisy-chained on an 8088/86 CPU should be programmed to the 8088/86 Interrupt mode (WR2; D4, D3 (Ch. A)). MPSC's Daisy-chained on an 8085 CPU should be programmed to 8085 interrupt mode 1 if it is the highest priority MPSC. In this mode, the highest priority MPSC issues the CALL instruction during the first  $\overline{INTA}$  cycle, and the interrupting MPSC provides the interrupt vector during the following  $\overline{INTA}$  cycles. Lower priority MPSC's should be programmed to 8085 interrupt mode 2.

MPSC's used alone in 8085 systems should be programmed to 8085 mode 1 interrupt operation.

### DMA Acknowledge Circuit



## DMA Timing



## DMA OPERATION

Each MPSC can be programmed to utilize up to four DMA channels: Transmit Channel A, Receive Channel A, Transmit Channel B, Receive Channel B. Each DMA Channel has an associated DMA Request line. Acknowledgement of a DMA cycle is done via normal data read or write cycles. This is accomplished by encoding the  $\overline{\text{DACK}}$  signals to generate  $A_0$ ,  $A_1$ , and  $\overline{\text{CS}}$  signals, and multiplexing them with the normal  $A_0$ ,  $A_1$ , and  $\overline{\text{CS}}$  signals.

## PERMUTATIONS

Channels A and B can be used with different system interface modes. In all cases it is impossible to poll the MPSC. The following table shows the possible

permutations of interrupt, wait, and DAM modes for channels A and B. Bits D<sub>1</sub>, D<sub>0</sub> of WR2 Ch. A determine these permutations.

Permutation WR2 Ch. A D <sub>1</sub> D <sub>0</sub>	Channel A	Channel B
0 0	Wait Interrupt Polled	Wait Interrupt Polled
0 1	DMA Polled	Interrupt Polled
1 0	DMA Polled	DMA Polled

**D1, D0 = 1, 1 is illegal.**



**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature  
 Under Bias ..... 0°C to +70°C  
 Storage Temperature  
 (Ceramic Package) ..... -65°C to +150°C  
 (Plastic Package) ..... -40°C to +125°C  
 Voltage On Any Pin With  
 Respect to Ground ..... -0.5V to +7.0V  
 Power Dissipation ..... 1.5W

*\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**D.C. CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC} = +5V \pm 10\%$ )

Symbol	Parameter	Min.	Max.	Units	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5	+0.8	V	
$V_{IH}$	Input High Voltage	+2.0	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage		+0.45	V	$I_{OL} = 2.0\text{mA}$
$V_{OH}$	Output High Voltage	+2.4		V	$I_{OH} = -200\mu\text{A}$
$I_{IL}$	Input Leakage Current		+10	$\mu\text{A}$	$V_{IN} = V_{CC}$ to 0V
$I_{OL}$	Output Leakage Current		+10	$\mu\text{A}$	$V_{OUT} = V_{CC}$ to 0V
$I_{CC}$	$V_{CC}$ Supply Current		180	mA	

**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ;  $V_{CC} = \text{GND} = 0\text{V}$ )

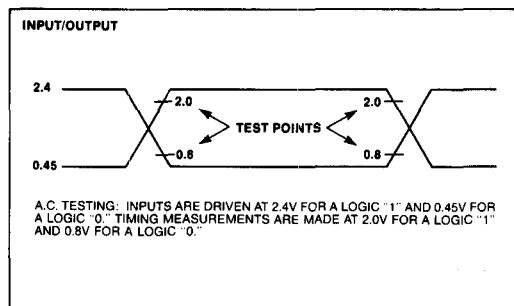
Symbol	Parameter	Min.	Max.	Units	Test Conditions
$C_{IN}$	Input Capacitance		10	pF	$f_c = 1\text{MHz}$ ;
$C_{OUT}$	Output Capacitance		15	pF	Unmeasured
$C_{I/O}$	Input/Output Capacitance		20	pF	pins returned to GND

**A.C. CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC} = +5V \pm 10\%$ )

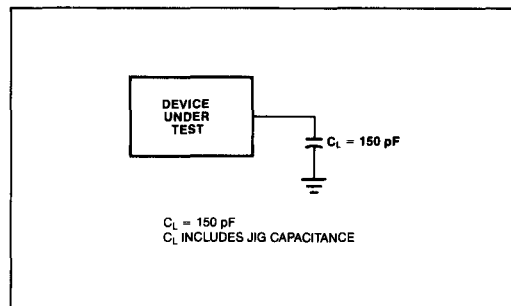
Symbol	Parameter	Min.	Max.	Units	Test Conditions
$t_{CY}$	CLK Period	250	4000	ns	
$t_{CL}$	CLK Low Time	105	2000	ns	
$t_{CH}$	CLK High Time	105	2000	ns	
$t_r$	CLK Rise Time	0	30	ns	
$t_f$	CLK Fall Time	0	30	ns	
$t_{AR}$	A0, A1 Setup to $\overline{RD}\downarrow$	0		ns	
$t_{AD}$	A0, A1 to Data Output Delay		200	ns	$C_L = 150$ pf
$t_{RA}$	A0, A1 Hold After $\overline{RD}\uparrow$	0		ns	
$t_{RD}$	$\overline{RD}\downarrow$ to Data Output Delay		200	ns	$C_L = 150$ pf
$t_{RR}$	$\overline{RD}$ Pulse Width	250		ns	
$t_{DF}$	Output Float Delay		120	ns	
$t_{AW}$	$\overline{CS}$ , A0, A1 Setup to $\overline{WR}\downarrow$	0		ns	
$t_{WA}$	$\overline{CS}$ , A0, A1 Hold after $\overline{WR}\uparrow$	0		ns	
$t_{WW}$	$\overline{WR}$ Pulse Width	250		ns	
$t_{DW}$	Data Setup to $\overline{WR}\uparrow$		150	ns	
$t_{WD}$	Data Hold After $\overline{WR}\uparrow$	0		ns	
$t_{PI}$	$\overline{PI}$ Setup to $\overline{INTA}\downarrow$	0		ns	
$t_{IP}$	$\overline{PI}$ Hold after $\overline{INTA}\uparrow$	0		ns	
$t_{II}$	$\overline{INTA}$ Pulse Width	250		ns	
$t_{IAPO}$	$\overline{INTA}\downarrow$ to $\overline{IPO}$ Delay		200	ns	
$t_{PIPO}$	$\overline{PI}\downarrow$ to $\overline{IPO}$ Delay		100	ns	
$t_{ID}$	$\overline{INTA}\downarrow$ to Data Output Delay		200	ns	
$t_{CQ}$	$\overline{RD}$ or $\overline{WR}$ to $\overline{DRQ}\downarrow$		150	ns	
$t_{RV}$	Recovery Time Between Controls	300		ns	
$t_{CW}$	$\overline{CS}$ , A0, A1 to $\overline{RDY}_A$ or $\overline{RDY}_B$ Delay		120	ns	
$t_{DCY}$	Data Clock Cycle	400		ns	
$t_{DCL}$	Data Clock Low Time	180		ns	
$t_{DCH}$	Data Clock High Time	180		ns	
$t_{TD}$	$\overline{Tx}\overline{C}$ to Tx D Delay		300	ns	
$t_{DS}$	RxD Setup to $\overline{Rx}\overline{C}\uparrow$	0		ns	
$t_{DH}$	RxD Hold after $\overline{Rx}\overline{C}\uparrow$	140		ns	
$t_{ITD}$	$\overline{Tx}\overline{C}$ to $\overline{INT}$ Delay	4	6	tcy	
$t_{IRD}$	RxC to $\overline{INT}$ Delay	7	10	tcy	
$t_{PL}$	$\overline{CTS}$ , $\overline{CD}$ , $\overline{SYNDET}$ Low Time	200		ns	
$t_{PH}$	$\overline{CTS}$ , $\overline{CD}$ , $\overline{SYNDET}$ High Time	200		ns	
$t_{IPD}$	External $\overline{INT}$ from $\overline{CTS}$ , $\overline{CD}$ , $\overline{SYNDET}$		500	ns	



# A.C. TESTING INPUT, OUTPUT WAVEFORM

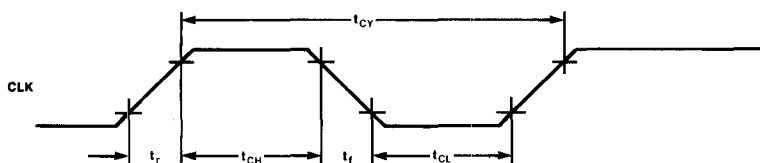


# A.C. TESTING LOAD CIRCUIT

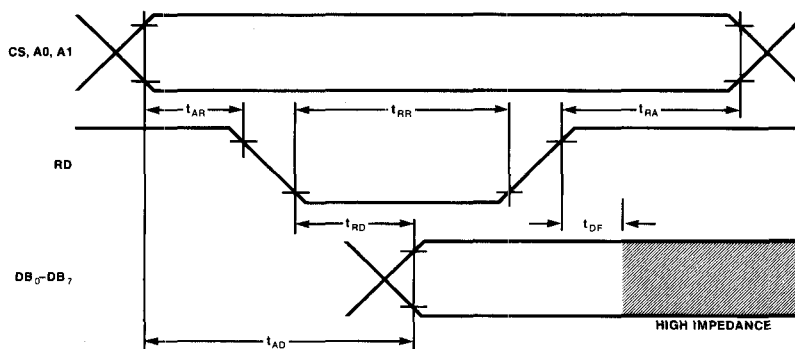


# WAVEFORMS

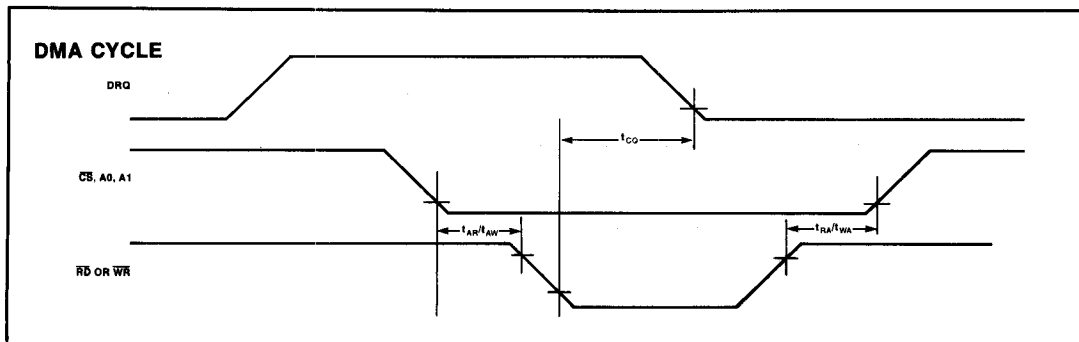
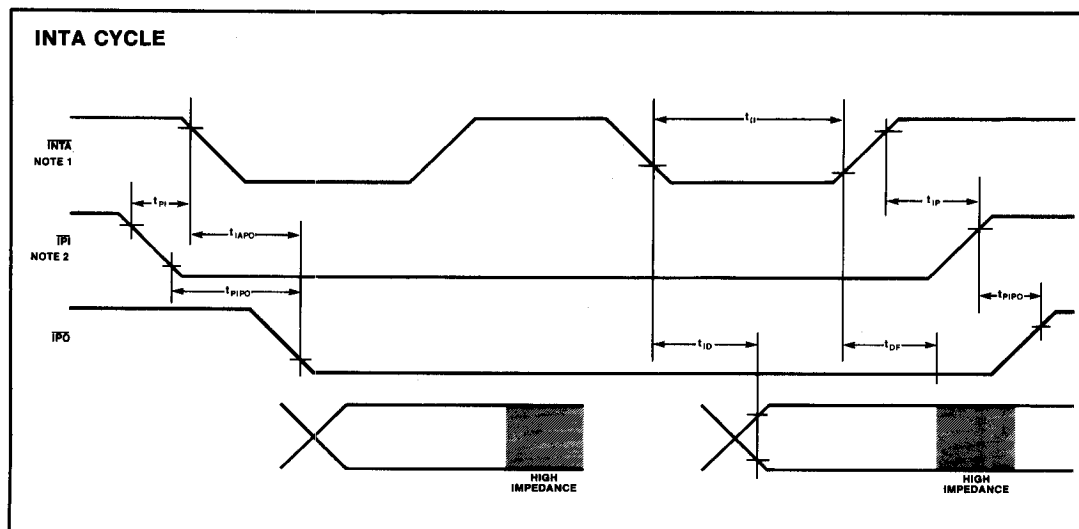
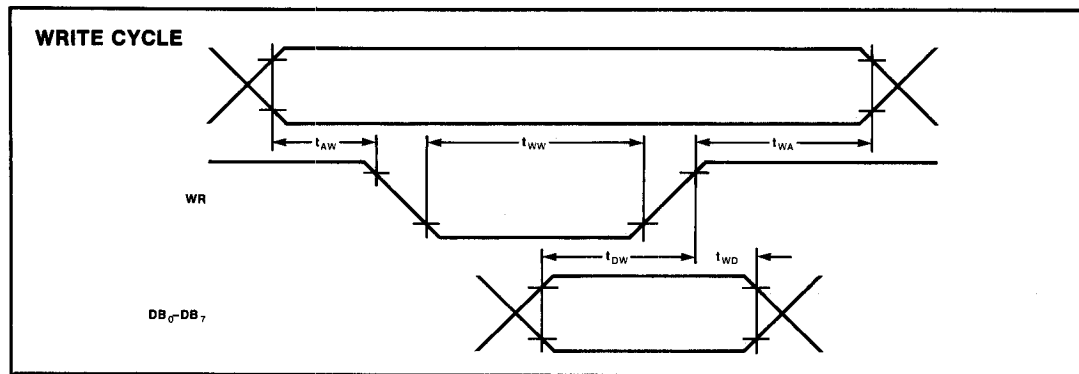
## CLOCK CYCLE



## READ CYCLE



# WAVEFORMS (Continued)



**NOTES:**

1. INTA signal acts as RD signal.
2. IPI signal acts as CS signal.

WAVEFORMS (Continued)

