



**EEDG/CE 6370**  
**Design and Analysis of Reconfigurable Systems**  
**Homework 5**  
**VGA-FPGA Interface**

### 1. Laboratory Objectives

- ☐ Create a VGA interface interfacing the FPGA with a monitor.
- ☐ Prototype the design on the Terasic DE1-SoC FPGA board.
- ☐ Understand the timing reports before and after place and route.

### 2. Summary

In this lab you will learn to interface the DE1-SoC board with a monitor through the VGA controller

### 3. Pre-lab

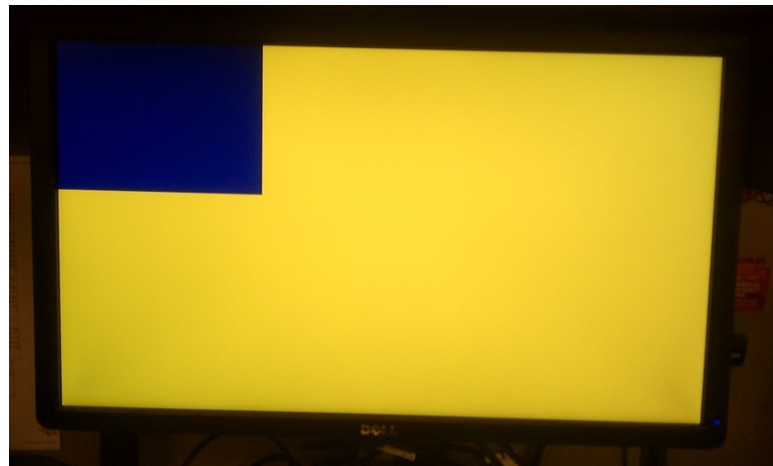
- ☐ Review the lecture slides that covers Physical Design of FPGAs

### 4. Tool Requirements

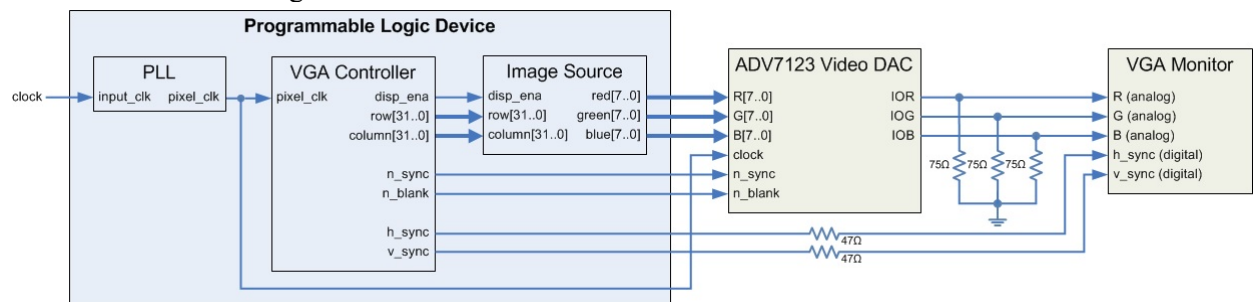
- ☐ Quartus Prime
- ☐ DE1-SoC board

### 5. VGA Interface Description

The given program will draw a blue square over a yellow background on the monitor as shown in the picture below:



The VGA controller should generate the entire control signal to drive the VGA output. The controller should have the following structure:



**Figure 1** VGA controller block diagram  
(source :<http://eewiki.net/pages/viewpage.action?pageId=15925278>)

## VGA Background

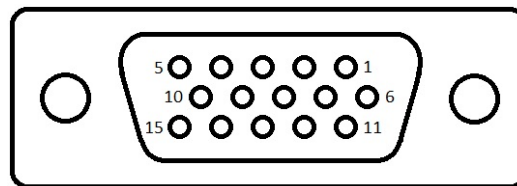
VGA is a standard interface for controlling analog monitors. The computing side of the interface provides the monitor with horizontal and vertical sync signals, color magnitudes, and ground references.

The horizontal and vertical sync signals are 0V/5V digital waveforms that synchronize the signal timing with the monitor. Being digital, they are provided directly by the FPGA (3.3V meets the minimum threshold for a logical high, so 3.3V can be used instead of 5V).

The color magnitudes are 0V-0.7V analog signals sent over the R, G, and B wires. (Alternatively, the green wire can use 0.3V-1V signals that incorporate both the horizontal and vertical sync signals, eliminating the need for those lines. This is called *sync-on-green* and is not addressed here.) The three-color magnitude wires are terminated with 75Ω resistors. These lines are also terminated with 75Ω inside the monitor. To create these analog signals, the FPGA outputs an 8-bit bus for each color to a video DAC, in this example an **ADV71235** from Analog Devices (data sheet attached). This video DAC also requires a pixel clock to latch in these values.

The VGA interface also specifies four wires that can be used to communicate with a ROM in the monitor. This ROM contains EDID (extended display identification data), which consists of the monitor's parameters in a standard format. Several communication standards exist to access this data, but in the simplest case, these lines can be left unconnected.

## Connections



**Figure 2** VGA connector

**Table 1** VGA connections description

| Pin | Signal         | Description                                       | Connection  |
|-----|----------------|---------------------------------------------------|-------------|
| 1   | R              | analog red, 0-0.7V                                | DAC output  |
| 2   | G              | analog green, 0-0.7V or 0.3-1V (if sync-on-green) | DAC output  |
| 3   | B              | analog blue, 0-0.7V                               | DAC output  |
| 4   | EDID Interface | function varies depending on standard used        | no connect  |
| 5   | GND            | general                                           | GND         |
| 6   | GND            | for R                                             | GND         |
| 7   | GND            | for G                                             | GND         |
| 8   | GND            | for B                                             | GND         |
| 9   | no pin         | or optional +5V                                   | no connect  |
| 10  | GND            | for h_sync and v_sync                             | GND         |
| 11  | EDID Interface | function varies depending on standard used        | no connect  |
| 12  | EDID Interface | function varies depending on standard used        | no connect  |
| 13  | h_sync         | horizontal sync, 0V/5V waveform                   | FPGA output |
| 14  | v_sync         | vertical sync, 0V/5V waveform                     | FPGA output |
| 15  | EDID Interface | function varies depending on standard used        | no connect  |

## Pixel Clock

This VGA controller requires the user to provide the pixel clock. This can be brought into the FPGA on a dedicated clock pin or can be derived inside the FPGA using a PLL. In the example project for the ML402 development board, the available 100MHz clock is input into one of the Intel Cyclone V DCM to produce a 193.16MHz pixel clock, as required by the 1920x1200 @60Hz VGA mode or 108 MHz for 1280x1024@60Hz (see appendix for more resolutions or search online, e.g., [https://tomverbeure.github.io/video\\_timings\\_calculator](https://tomverbeure.github.io/video_timings_calculator)).

## Operation

Figure 3 illustrates the timing signals produced by the VGA controller. The controller contains two counters. One counter increments on pixel clocks and controls the timing of the *h\_sync* (horizontal sync) signal. By setting it up such that the display time starts at counter value 0, the counter value equals the pixel's column coordinate during the display time. The horizontal display time is followed by a blanking time, which includes a horizontal front porch, the horizontal sync pulse itself, and the horizontal back porch, each of specified duration. At the end of the row, the counter resets to start the next row.

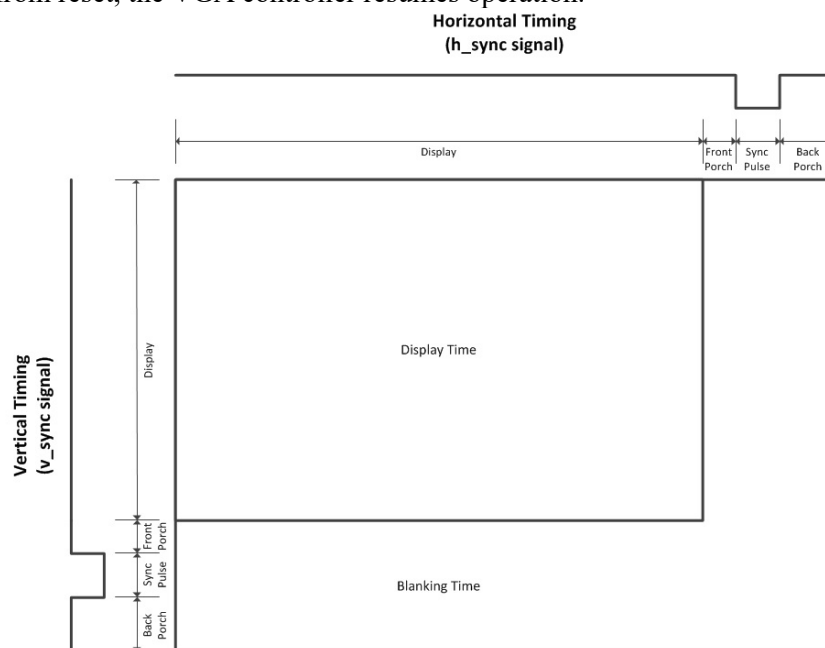
The other counter increments as each row completes, therefore controlling the timing of the *v\_sync* (vertical sync) signal. Again, this is set up such that the display time starts at counter value 0, so the counter value equals the pixel's row coordinate during the display time. As before, the vertical display time is followed by a blanking time, with its corresponding front porch, sync pulse, and back porch. Once the vertical blanking time completes, the counter resets to begin the next screen refresh.

A display enable is defined by the logical AND of the horizontal and vertical display times.

Using these counters, the VGA controller outputs the horizontal sync, vertical sync, display enable, and pixel coordinate signals. The sync pulses are specified as positive or negative polarity for each VGA mode. The GENERIC parameters *h\_pol* (horizontal polarity) and *v\_pol* (vertical polarity) set the polarity of the VGA controller's *h\_sync* and *v\_sync* outputs, respectively.

## Reset

The *reset\_n* input port must have a logic high for the VGA controller component to operate. A low logic level on this port asynchronously resets the component. During reset, the component deasserts the horizontal and vertical counters, clears the pixel coordinates, and disables the display. Once released from reset, the VGA controller resumes operation.



**Figure 3** Signal timing diagram

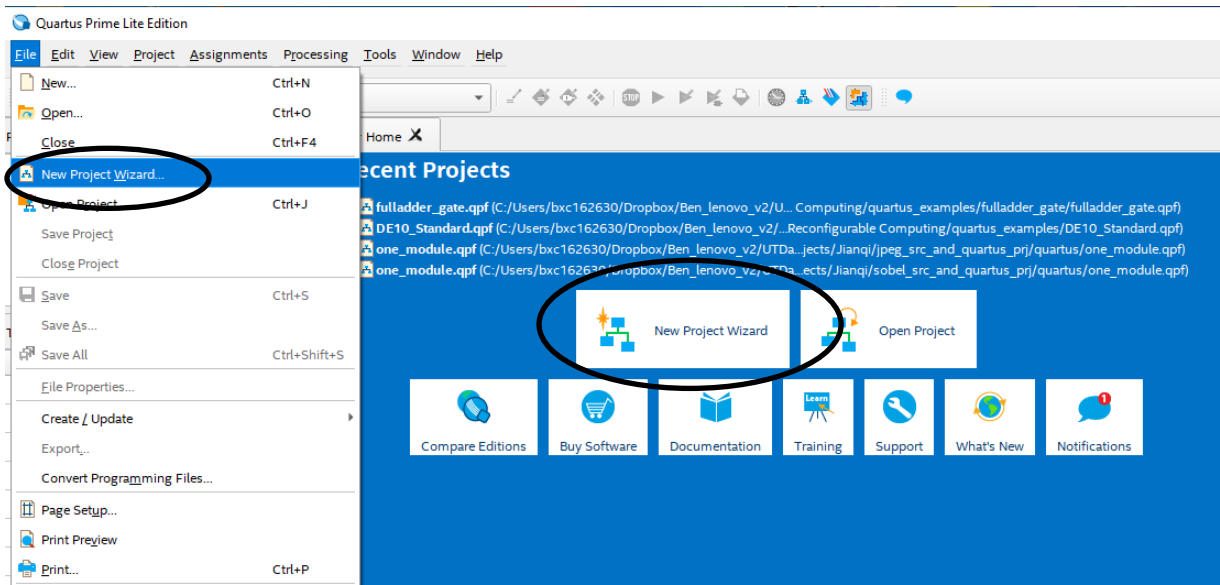
## 6. VGA Controller Design

- ☐ Open Quartus Prime

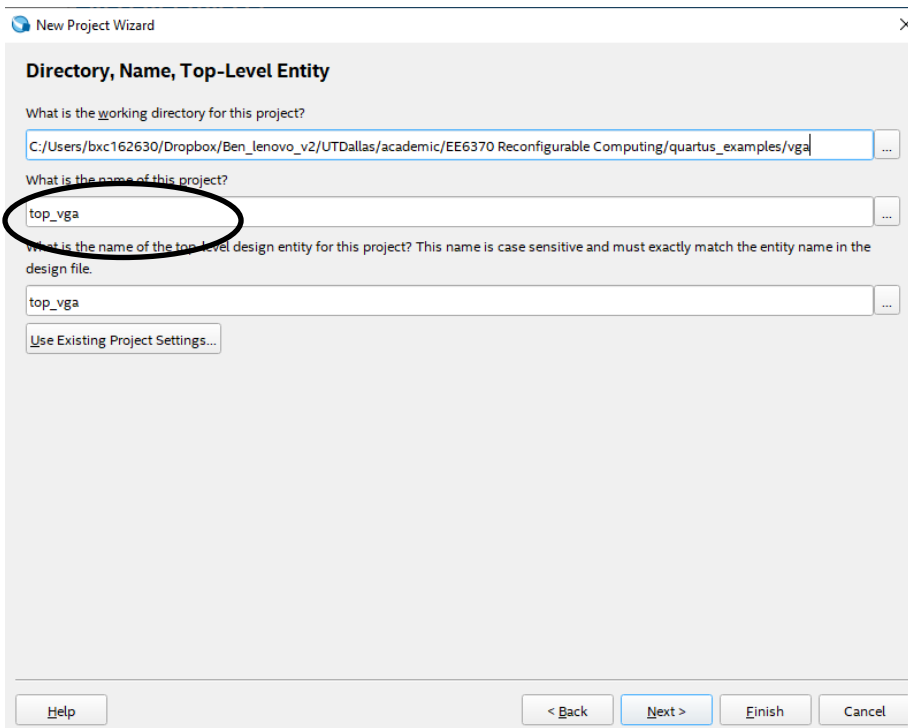


In case of Windows run the tools always as administrator (right

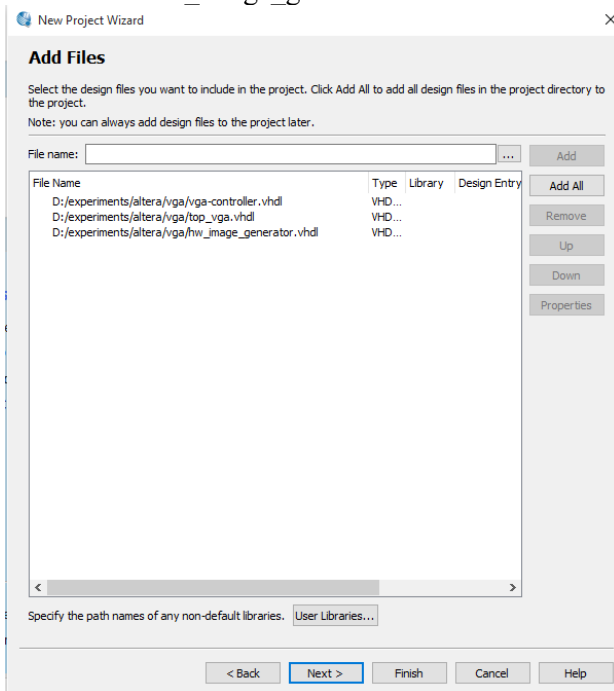
- ☐ Create a new project.  
File → New Project Wizard



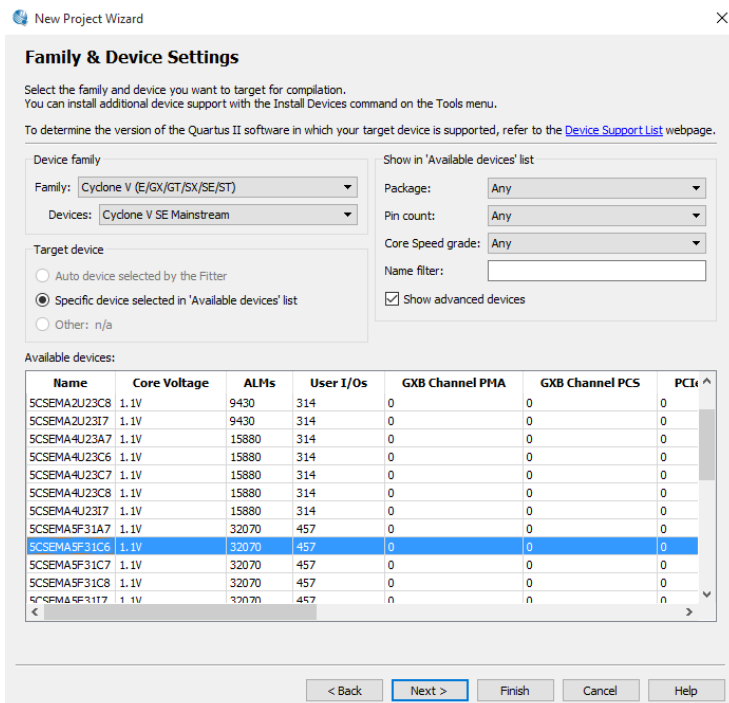
Name the project “top\_vga”



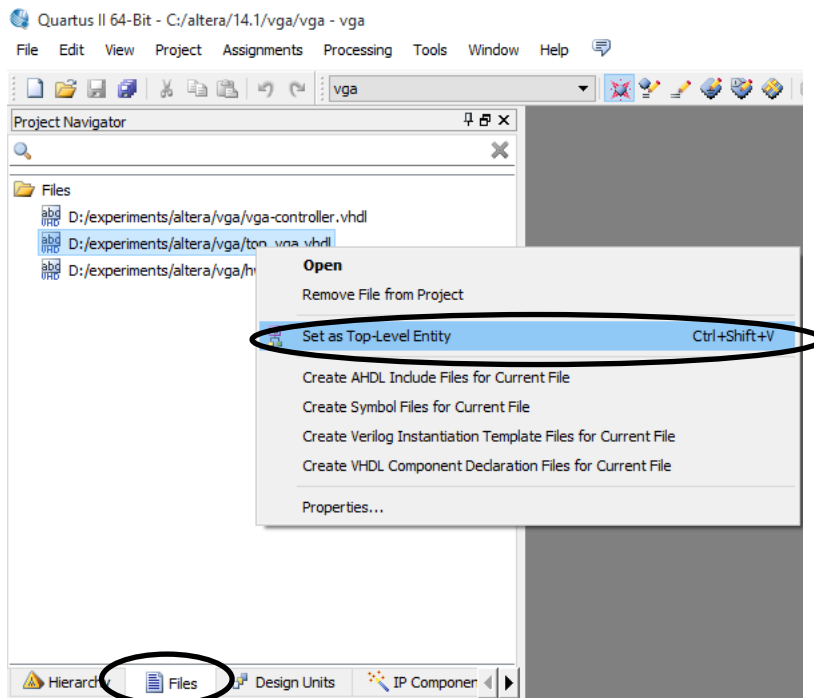
- Add the following files to the project:
  - top\_vga.vhdl
  - vga-controller.vhdl
  - hw\_image\_generator.vhdl



- Click next.
- Select Cyclone V 5CSEMA5F31C6 device



- Click next and Finish.
- Click on Files tab → Right click on “top\_vga.vhdl” → Set as Top-Level Entity



- ☐ Check the resolution of your monitor and modify the Generic parameters of the VGA controller. You need to modify the resolution (h\_pixels and v\_pixels) and the horizontal and vertical porch widths.

Edit source code to the VGA controller:

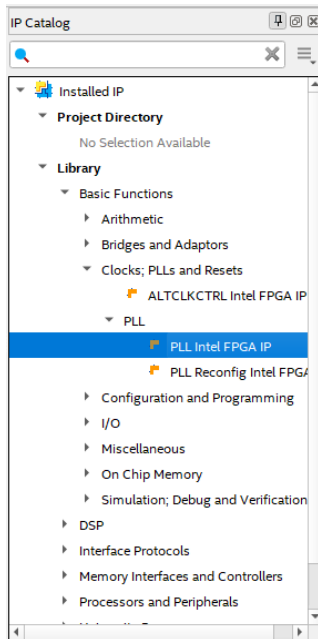
```

LIBRARY ieee;
USE ieee.std_logic_1164.all;

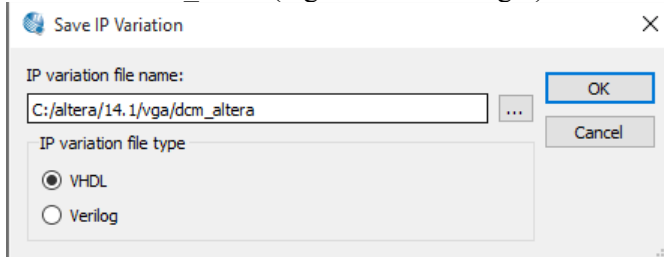
ENTITY vga_controller IS
  GENERIC(
    h_pulse : INTEGER := 208; --horizontal sync pulse width in pixels
    h_bp    : INTEGER := 336; --horizontal back porch width in pixels
    h_pixels : INTEGER := 1280; --horizontal display width in pixels
    h_fp    : INTEGER := 128; --horizontal front porch width in pixels
    h_pol    : STD_LOGIC := '0'; --horizontal sync pulse polarity (1 = positive, 0 = negative)
    v_pulse  : INTEGER := 3; --vertical sync pulse width in rows
    v_bp    : INTEGER := 38; --vertical back porch width in rows
    v_pixels : INTEGER := 1024; --vertical display width in rows
    v_fp    : INTEGER := 1; --vertical front porch width in rows
    v_pol    : STD_LOGIC := '1'; --vertical sync pulse polarity (1 = positive, 0 = negative)
  )
  PORT(
    pixel_clk : IN STD_LOGIC; --pixel clock at frequency of VGA mode being used
  );
END behavior;

```

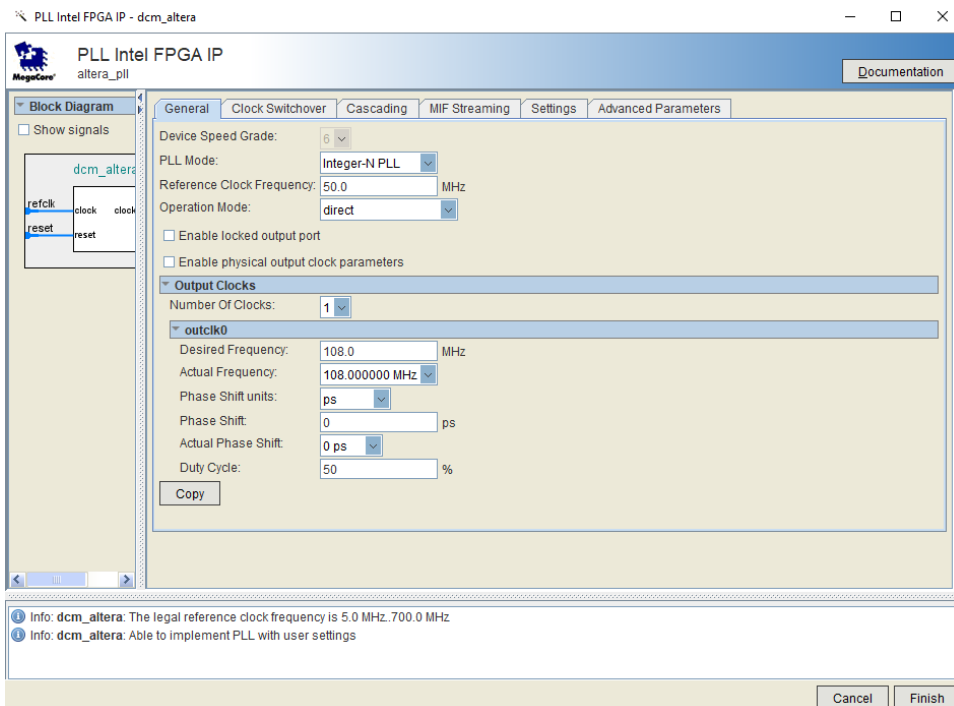
- ☐ The hw\_image\_generator.vhdl block is responsible for drawing the two squares to the screen. Read the code and identify how this is done.
- ☐ Create the pixel clock using Quartus's IP generator (IP catalogue). Go to IP Catalogue (right pane of Quartus) to create a PLL. A new clock depending on the monitor's resolution is needed.
- ☐ Library → Basic Functions → Clocks; PLL and Resets → PLL Intel FPGA IP.



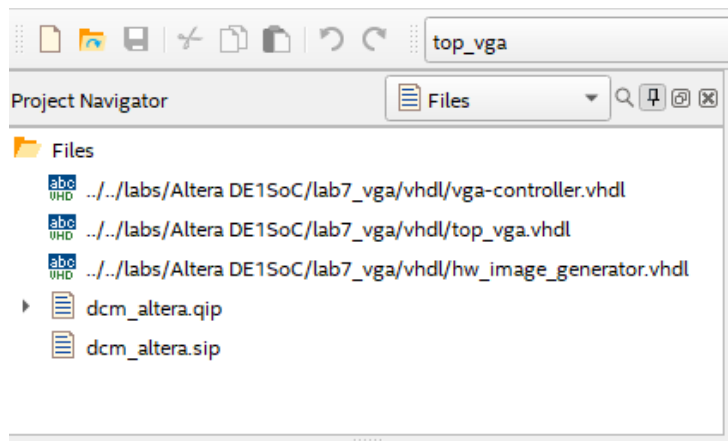
- Call it dcm\_altera (digital clock manager) and select VHDL.



- Enter 50MHz as Reference Clock Frequency
- Disable “Enable locked output port”
- Specify 108MHz as Desired Frequency.



- The project navigator should not show the newly generated PLL:



- Instantiate DCM into top\_vga.vhdl module as a component (top\_vga.vhdl)

```

architecture Behavioral of top_vga is

    COMPONENT dcm_altera is
    port (
        refclk    : in  std_logic;
        rst       : in  std_logic;
        outclk_0  : out std_logic );
    end COMPONENT;

    COMPONENT vga_controller
    PORT (

```

**Note:** the DCM reset is active high and hence it needs to be inverted

```

-- Signals declaration
signal disp_ena : std_logic;
signal row : INTEGER;
signal column : INTEGER;
signal pixel_clk : std_logic;
signal reset_inv : std_logic;

begin

    reset_inv <= NOT reset_n;

    uut1: dcm_altera PORT MAP (
        refclk    => sys_clk_in,
        rst       => reset_inv,
        outclk_0  => pixel_clk);

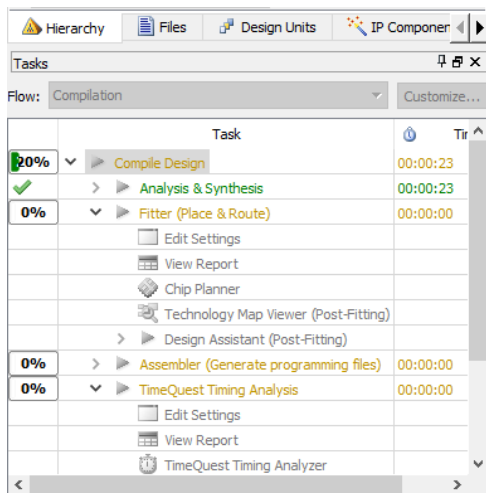
    pixel_clk_out <= pixel_clk;

    uut2: vga_controller PORT MAP (
        pixel_clk => pixel_clk,
        reset_n   => reset_n,
        h_sync    => h_sync,
        v_sync    => v_sync,
        disp_ena  => disp_ena,
        column    => column,
        row       => row,
        n_blank   => n_blank,
        n_sync    => n_sync);

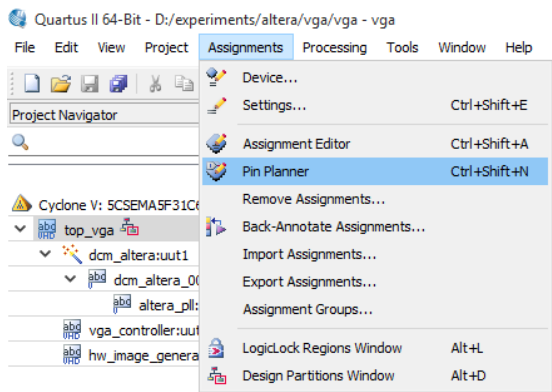
```

- Compile the design to make sure there are no errors by clicking on “Compile Design”





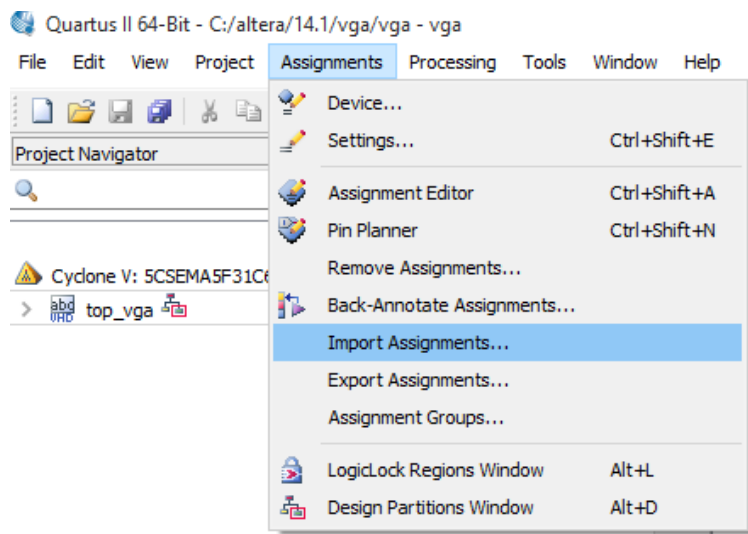
- Go to Pin Planner to assign the top module's IOs to physical pins on the FPGA board.



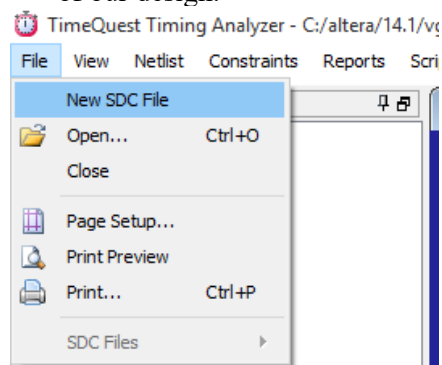
- Assign the IOs to the following pins as indicated in Terasic's DE1-SoC board user manual.

| Node Name     | Direction | Location | I/O Bank | VREF Group | Fitter Location | I/O Standard    |
|---------------|-----------|----------|----------|------------|-----------------|-----------------|
| blue[7]       | Output    | PIN_J14  | 8A       | B8A_NO     | PIN_J14         | 2.5 V (default) |
| blue[6]       | Output    | PIN_G15  | 8A       | B8A_NO     | PIN_G15         | 2.5 V (default) |
| blue[5]       | Output    | PIN_F15  | 8A       | B8A_NO     | PIN_F15         | 2.5 V (default) |
| blue[4]       | Output    | PIN_H14  | 8A       | B8A_NO     | PIN_H14         | 2.5 V (default) |
| blue[3]       | Output    | PIN_F14  | 8A       | B8A_NO     | PIN_F14         | 2.5 V (default) |
| blue[2]       | Output    | PIN_H13  | 8A       | B8A_NO     | PIN_H13         | 2.5 V (default) |
| blue[1]       | Output    | PIN_G13  | 8A       | B8A_NO     | PIN_G13         | 2.5 V (default) |
| blue[0]       | Output    | PIN_B13  | 8A       | B8A_NO     | PIN_B13         | 2.5 V (default) |
| green[7]      | Output    | PIN_E11  | 8A       | B8A_NO     | PIN_E11         | 2.5 V (default) |
| green[6]      | Output    | PIN_F11  | 8A       | B8A_NO     | PIN_F11         | 2.5 V (default) |
| green[5]      | Output    | PIN_G12  | 8A       | B8A_NO     | PIN_G12         | 2.5 V (default) |
| green[4]      | Output    | PIN_G11  | 8A       | B8A_NO     | PIN_G11         | 2.5 V (default) |
| green[3]      | Output    | PIN_G10  | 8A       | B8A_NO     | PIN_G10         | 2.5 V (default) |
| green[2]      | Output    | PIN_H12  | 8A       | B8A_NO     | PIN_H12         | 2.5 V (default) |
| green[1]      | Output    | PIN_J10  | 8A       | B8A_NO     | PIN_J10         | 2.5 V (default) |
| green[0]      | Output    | PIN_J9   | 8A       | B8A_NO     | PIN_J9          | 2.5 V (default) |
| h_sync        | Output    | PIN_B11  | 8A       | B8A_NO     | PIN_B11         | 2.5 V (default) |
| n_blank       | Output    | PIN_F10  | 8A       | B8A_NO     | PIN_F10         | 2.5 V (default) |
| n_sync        | Output    | PIN_C10  | 8A       | B8A_NO     | PIN_C10         | 2.5 V (default) |
| pixel_clk_out | Output    | PIN_A11  | 8A       | B8A_NO     | PIN_A11         | 2.5 V (default) |
| red[7]        | Output    | PIN_F13  | 8A       | B8A_NO     | PIN_F13         | 2.5 V (default) |
| red[6]        | Output    | PIN_E12  | 8A       | B8A_NO     | PIN_E12         | 2.5 V (default) |
| red[5]        | Output    | PIN_D12  | 8A       | B8A_NO     | PIN_D12         | 2.5 V (default) |
| red[4]        | Output    | PIN_C12  | 8A       | B8A_NO     | PIN_C12         | 2.5 V (default) |
| red[3]        | Output    | PIN_B12  | 8A       | B8A_NO     | PIN_B12         | 2.5 V (default) |
| red[2]        | Output    | PIN_E13  | 8A       | B8A_NO     | PIN_E13         | 2.5 V (default) |
| red[1]        | Output    | PIN_C13  | 8A       | B8A_NO     | PIN_C13         | 2.5 V (default) |
| red[0]        | Output    | PIN_A13  | 8A       | B8A_NO     | PIN_A13         | 2.5 V (default) |
| reset_n       | Input     | PIN_AA14 | 3B       | B3B_NO     | PIN_AA14        | 2.5 V (default) |
| sys_clk_in    | Input     | PIN_AF14 | 3B       | B3B_NO     | PIN_AF14        | 2.5 V (default) |
| v_sync        | Output    | PIN_D11  | 8A       | B8A_NO     | PIN_D11         | 2.5 V (default) |

- In case that the input constraint file (.qsf) is given you can import it directly. Assignments → Import Assignments → Choose .qsf file.

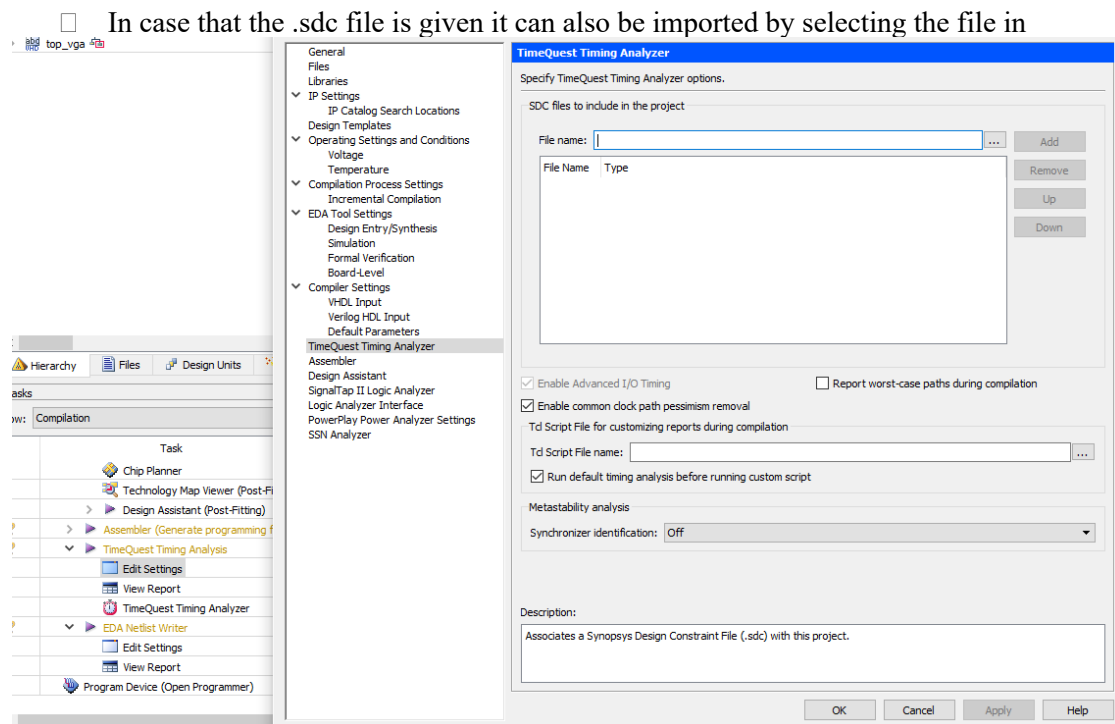


- Finally generate .sdc (Synopsys Design Constraint) file, which includes the timing constraints of our design.

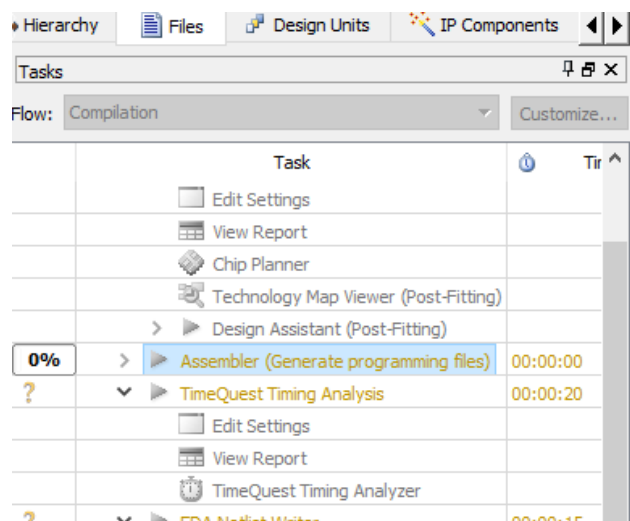


- Add to the new file, where 'sys\_clk\_in' has to be the same name as the input clock

```
create_clock -name "sys_clk_in" -period 20.000ns [get_ports {sys_clk_in}]
derive_pll_clocks
derive_clock_uncertainty
```

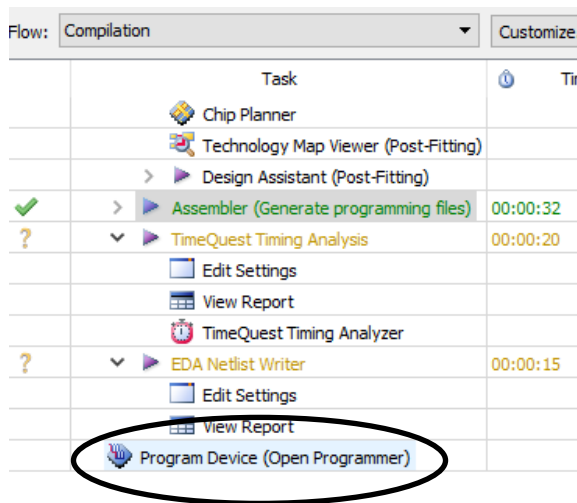


- ☐ When finished the .sdc file should be visible in the project files.
- ☐ Synthesize the entire design by clicking on the “Assembler (Generate programming files)” option

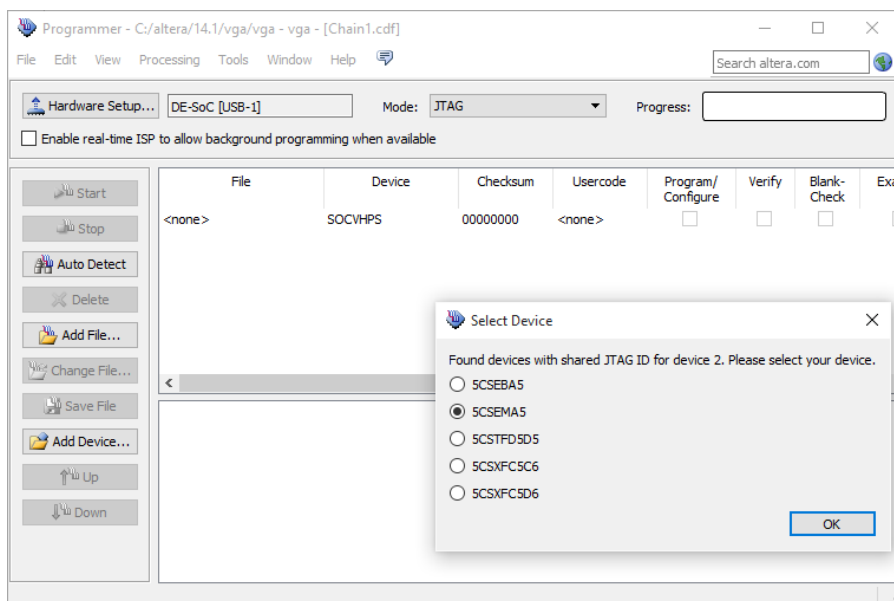


- ☐ This should generate the .sof file to configure the FPGA in output\_files/vga.sof

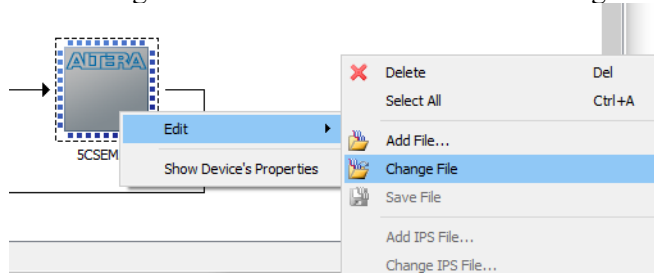
- ☐ Connect the FPGA board to the power, the USB Blaster cable and the VGA cable to the monitor.
- ☐ Power the FPGA on
- ☐ Open the programmer



- ☐ Click on Hardware Setup and select DE-SoC[USB-1] FPGA
- ☐ Click on Auto Detect
- ☐ Select 5CSEMA5



- Right click on 5CSEMA5 device → change file → select /output\_files/vga.sof




- Select Program/Configure on the table with the .sof entry.
- Click on Auto-detect if the start button is not enabled → Start.



- The FPGA should have been successfully programmed.
- Turn the monitor on and see if the design is working.

## 7. Power Consumption Estimation:

Annotate from the synthesis report the total number of Logic Cells, Shift registers, FFs, IOs, BRAM and DSP used in the design. Manually enter this information with the clock frequency (50MHz) at the given Power estimation [excel spreadsheet](#).



[Visit the Online  
Power Management  
Resource Center](#)

**PowerPlay Early Power Estimator**  
**Cyclone® IV, Cyclone® V**  
**V15.0 B05.04**

Comments:

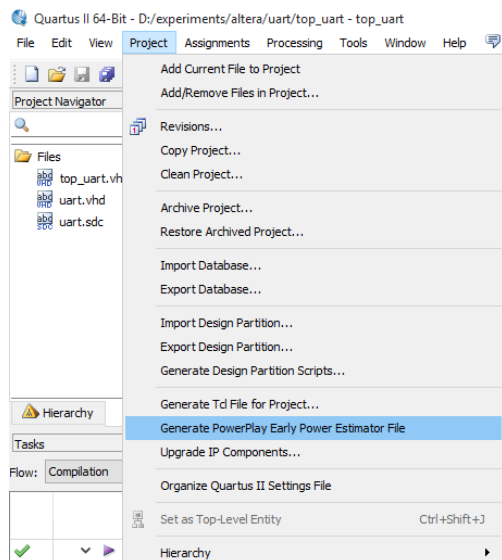
| Input Parameters                                                                                                |                                                     | Thermal Power (W)       |       | Thermal Analysis                    |            |
|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|-------------------------|-------|-------------------------------------|------------|
| Family                                                                                                          | Cyclone IV GX                                       | Logic                   | 0.000 | Junction Temp, T <sub>J</sub> (°C)  | 26         |
| Device                                                                                                          | EP4CGX15B                                           | RAM                     | 0.000 | θ <sub>JA</sub> Junction-Ambient    | 14.20      |
| Package                                                                                                         | F14 (F169)                                          | DSP                     | 0.000 | Maximum Allowed T <sub>A</sub> (°C) | 83.8       |
| Temperature Grade                                                                                               | Commercial                                          | I/O                     | 0.000 | <b>Details</b>                      |            |
| Power Characteristics                                                                                           | Typical                                             | HSDI                    | N/A   | <b>Power Tree Design</b>            |            |
| V <sub>CCINT</sub> Voltage (V)                                                                                  | 1.20                                                | PLL                     | 0.000 |                                     |            |
| Power Model Status                                                                                              | FINAL                                               | Clock                   | 0.000 | Power Rail Configuration            |            |
| <input type="radio"/> User Entered T <sub>J</sub> <input checked="" type="radio"/> Auto Computed T <sub>J</sub> |                                                     | HMC                     | N/A   | N/A                                 |            |
| Ambient Temp, T <sub>A</sub> (°C)                                                                               | 25                                                  | XCVR                    | 0.000 | Voltage    Current                  |            |
| Custom Theta JA                                                                                                 | <input checked="" type="radio"/> Estimated Theta JA | PCS and HIP             | 0.000 | Regulator 1                         | N/A    N/A |
| Heat Sink                                                                                                       | 23 mm - Medium Profile                              | P <sub>static</sub>     | 0.071 | Regulator 2                         | N/A    N/A |
| Airflow                                                                                                         | 200 lfm (1.0 m/s)                                   | <b>Total FPGA</b>       | 0.071 | Regulator 3                         | N/A    N/A |
| Custom θ <sub>SA</sub> (°C/W)                                                                                   | 6.40                                                | HPS                     | N/A   | Regulator 4                         | N/A    N/A |
| Board Thermal Model                                                                                             | None (Conservative)                                 | P <sub>static,HPS</sub> | N/A   | Regulator 5                         | N/A    N/A |
|                                                                                                                 |                                                     | <b>Total SoC</b>        | N/A   | Regulator 6                         | N/A    N/A |
|                                                                                                                 |                                                     |                         |       | Regulator 7                         | N/A    N/A |
|                                                                                                                 |                                                     |                         |       | Regulator 8                         | N/A    N/A |

☒ Set Toggle %

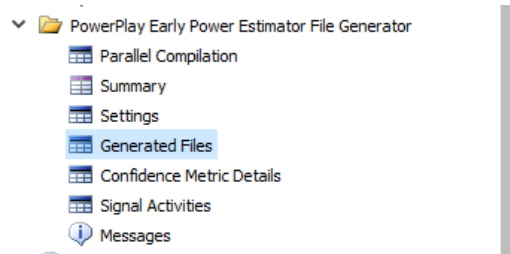
Select Power Regulator

This will give you an initial estimate of the static and power consumption of your design. You can modify the values to analyse different scenarios.

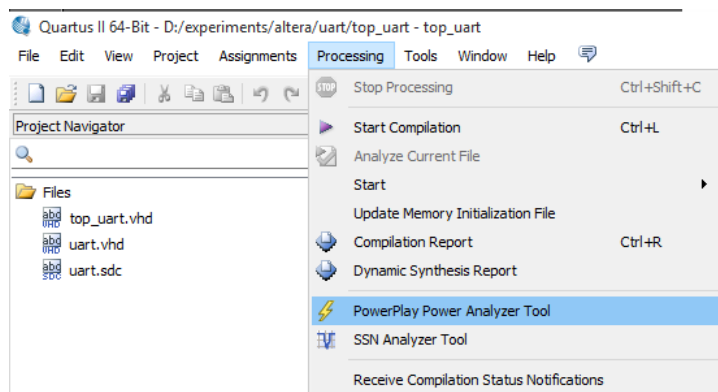
- Altera also provides an automated way of generating the information for this spreadsheet in Quartus Prime. PowerPlay is a tool included at Quartus which displays the power consumption of your design and allows to export an \_pwr.csv file, which can in turn be imported by the Excel spreadsheet.



Import this file into the excel sheet.



- Click on Processing→ PowerPlay Power Analyzer tool



This will open Quartus's power analyser, which allows you to get an estimate of the power consumption and also to export a .xpe file for the Excel spreadsheet.

**Input file**

☐ Use input file(s) to initialize toggle rates and static probabilities during power analysis

Add Power Input File(s)...

**Output file**

☒ Write out signal activities used during power analysis

Output file name: D:\experiments\altera\uart\output\_files\uart.saf

**Default toggle rates for unspecified signals**

Default toggle rate used for input I/O signals: 12.5 %

Default toggle rate used for remaining signals

☐ Use default value: 12.5 %

☒ Use vectorless estimation

HPS Power Calculator...

Cooling Solution and Temperature...

00:00:17 100%

Start Stop Report

- ☐ A PowerPlay Analyzer entry is generated in the report section.

| Table of Contents                                |  |
|--------------------------------------------------|--|
| Flow Summary                                     |  |
| Flow Settings                                    |  |
| Flow Non-Default Global Settings                 |  |
| Flow Elapsed Time                                |  |
| Flow OS Summary                                  |  |
| Flow Log                                         |  |
| > Analysis & Synthesis                           |  |
| > Fitter                                         |  |
| > Assembler                                      |  |
| > PowerPlay Power Analyzer                       |  |
| Parallel Compilation                             |  |
| Summary                                          |  |
| Settings                                         |  |
| Generated Files                                  |  |
| Operating Conditions Used                        |  |
| Thermal Power Dissipation by Block               |  |
| Thermal Power Dissipation by Block Type          |  |
| Thermal Power Dissipation by Hierarchy           |  |
| Core Dynamic Thermal Power Dissipation           |  |
| > Current Drawn from Voltage Supplies            |  |
| Confidence Metric Details                        |  |
| Signal Activities                                |  |
| Messages                                         |  |
| > PowerPlay Early Power Estimator File Generator |  |
| Flow Messages                                    |  |
| Flow Suppressed Messages                         |  |



## Appendix

| Resolution | Refresh Rate<br>(Hz) | Pixel Clock<br>(MHz) | Horizontal (pixel clocks) |                |               |               | Vertical (rows) |                |               |               | Hsync<br>Polarity | Vsync<br>Polarity |
|------------|----------------------|----------------------|---------------------------|----------------|---------------|---------------|-----------------|----------------|---------------|---------------|-------------------|-------------------|
|            |                      |                      | Display                   | Front<br>Porch | Sync<br>Pulse | Back<br>Porch | Display         | Front<br>Porch | Sync<br>Pulse | Back<br>Porch |                   |                   |
| 640x350    | 70                   | 25.175               | 640                       | 16             | 96            | 48            | 350             | 37             | 2             | 60            | p                 | n                 |
| 640x350    | 85                   | 31.5                 | 640                       | 32             | 64            | 96            | 350             | 32             | 3             | 60            | p                 | n                 |
| 640x400    | 70                   | 25.175               | 640                       | 16             | 96            | 48            | 400             | 12             | 2             | 35            | n                 | p                 |
| 640x400    | 85                   | 31.5                 | 640                       | 32             | 64            | 96            | 400             | 1              | 3             | 41            | n                 | p                 |
| 640x480    | 60                   | 25.175               | 640                       | 16             | 96            | 48            | 480             | 10             | 2             | 33            | n                 | n                 |
| 640x480    | 73                   | 31.5                 | 640                       | 24             | 40            | 128           | 480             | 9              | 2             | 29            | n                 | n                 |
| 640x480    | 75                   | 31.5                 | 640                       | 16             | 64            | 120           | 480             | 1              | 3             | 16            | n                 | n                 |
| 640x480    | 85                   | 36                   | 640                       | 56             | 56            | 80            | 480             | 1              | 3             | 25            | n                 | n                 |
| 640x480    | 100                  | 43.16                | 640                       | 40             | 64            | 104           | 480             | 1              | 3             | 25            | n                 | p                 |
| 720x400    | 85                   | 35.5                 | 720                       | 36             | 72            | 108           | 400             | 1              | 3             | 42            | n                 | p                 |
| 768x576    | 60                   | 34.96                | 768                       | 24             | 80            | 104           | 576             | 1              | 3             | 17            | n                 | p                 |
| 768x576    | 72                   | 42.93                | 768                       | 32             | 80            | 112           | 576             | 1              | 3             | 21            | n                 | p                 |
| 768x576    | 75                   | 45.51                | 768                       | 40             | 80            | 120           | 576             | 1              | 3             | 22            | n                 | p                 |
| 768x576    | 85                   | 51.84                | 768                       | 40             | 80            | 120           | 576             | 1              | 3             | 25            | n                 | p                 |
| 768x576    | 100                  | 62.57                | 768                       | 48             | 80            | 128           | 576             | 1              | 3             | 31            | n                 | p                 |
| 800x600    | 56                   | 36                   | 800                       | 24             | 72            | 128           | 600             | 1              | 2             | 22            | p                 | p                 |
| 800x600    | 60                   | 40                   | 800                       | 40             | 128           | 88            | 600             | 1              | 4             | 23            | p                 | p                 |
| 800x600    | 75                   | 49.5                 | 800                       | 16             | 80            | 160           | 600             | 1              | 3             | 21            | p                 | p                 |
| 800x600    | 72                   | 50                   | 800                       | 56             | 120           | 64            | 600             | 37             | 6             | 23            | p                 | p                 |
| 800x600    | 85                   | 56.25                | 800                       | 32             | 64            | 152           | 600             | 1              | 3             | 27            | p                 | p                 |
| 800x600    | 100                  | 68.18                | 800                       | 48             | 88            | 136           | 600             | 1              | 3             | 32            | n                 | p                 |
| 1024x768   | 43                   | 44.9                 | 1024                      | 8              | 176           | 56            | 768             | 0              | 8             | 41            | p                 | p                 |
| 1024x768   | 60                   | 65                   | 1024                      | 24             | 136           | 160           | 768             | 3              | 6             | 29            | n                 | n                 |
| 1024x768   | 70                   | 75                   | 1024                      | 24             | 136           | 144           | 768             | 3              | 6             | 29            | n                 | n                 |
| 1024x768   | 75                   | 78.8                 | 1024                      | 16             | 96            | 176           | 768             | 1              | 3             | 28            | p                 | p                 |
| 1024x768   | 85                   | 94.5                 | 1024                      | 48             | 96            | 208           | 768             | 1              | 3             | 36            | p                 | p                 |
| 1024x768   | 100                  | 113.31               | 1024                      | 72             | 112           | 184           | 768             | 1              | 3             | 42            | n                 | p                 |
| 1152x864   | 75                   | 108                  | 1152                      | 64             | 128           | 256           | 864             | 1              | 3             | 32            | p                 | p                 |
| 1152x864   | 85                   | 119.65               | 1152                      | 72             | 128           | 200           | 864             | 1              | 3             | 39            | n                 | p                 |
| 1152x864   | 100                  | 143.47               | 1152                      | 80             | 128           | 208           | 864             | 1              | 3             | 47            | n                 | p                 |
| 1152x864   | 60                   | 81.62                | 1152                      | 64             | 120           | 184           | 864             | 1              | 3             | 27            | n                 | p                 |
| 1280x1024  | 60                   | 108                  | 1280                      | 48             | 112           | 248           | 1024            | 1              | 3             | 38            | p                 | p                 |
| 1280x1024  | 75                   | 135                  | 1280                      | 16             | 144           | 248           | 1024            | 1              | 3             | 38            | p                 | p                 |
| 1280x1024  | 85                   | 157.5                | 1280                      | 64             | 160           | 224           | 1024            | 1              | 3             | 44            | p                 | p                 |
| 1280x1024  | 100                  | 190.96               | 1280                      | 96             | 144           | 240           | 1024            | 1              | 3             | 57            | n                 | p                 |
| 1280x800   | 60                   | 83.46                | 1280                      | 64             | 136           | 200           | 800             | 1              | 3             | 24            | n                 | p                 |
| 1280x960   | 60                   | 102.1                | 1280                      | 80             | 136           | 216           | 960             | 1              | 3             | 30            | n                 | p                 |
| 1280x960   | 72                   | 124.54               | 1280                      | 88             | 136           | 224           | 960             | 1              | 3             | 37            | n                 | p                 |
| 1280x960   | 75                   | 129.86               | 1280                      | 88             | 136           | 224           | 960             | 1              | 3             | 38            | n                 | p                 |
| 1280x960   | 85                   | 148.5                | 1280                      | 64             | 160           | 224           | 960             | 1              | 3             | 47            | p                 | p                 |
| 1280x960   | 100                  | 178.99               | 1280                      | 96             | 144           | 240           | 960             | 1              | 3             | 53            | n                 | p                 |
| 1368x768   | 60                   | 85.86                | 1368                      | 72             | 144           | 216           | 768             | 1              | 3             | 23            | n                 | p                 |
| 1400x1050  | 60                   | 122.61               | 1400                      | 88             | 152           | 240           | 1050            | 1              | 3             | 33            | n                 | p                 |
| 1400x1050  | 72                   | 149.34               | 1400                      | 96             | 152           | 248           | 1050            | 1              | 3             | 40            | n                 | p                 |
| 1400x1050  | 75                   | 155.85               | 1400                      | 96             | 152           | 248           | 1050            | 1              | 3             | 42            | n                 | p                 |
| 1400x1050  | 85                   | 179.26               | 1400                      | 104            | 152           | 256           | 1050            | 1              | 3             | 49            | n                 | p                 |
| 1400x1050  | 100                  | 214.39               | 1400                      | 112            | 152           | 264           | 1050            | 1              | 3             | 58            | n                 | p                 |
| 1440x900   | 60                   | 106.47               | 1440                      | 80             | 152           | 232           | 900             | 1              | 3             | 28            | n                 | p                 |
| 1600x1200  | 60                   | 162                  | 1600                      | 64             | 192           | 304           | 1200            | 1              | 3             | 46            | p                 | p                 |
| 1600x1200  | 65                   | 175.5                | 1600                      | 64             | 192           | 304           | 1200            | 1              | 3             | 46            | p                 | p                 |
| 1600x1200  | 70                   | 189                  | 1600                      | 64             | 192           | 304           | 1200            | 1              | 3             | 46            | p                 | p                 |
| 1600x1200  | 75                   | 202.5                | 1600                      | 64             | 192           | 304           | 1200            | 1              | 3             | 46            | p                 | p                 |
| 1600x1200  | 85                   | 229.5                | 1600                      | 64             | 192           | 304           | 1200            | 1              | 3             | 46            | p                 | p                 |
| 1600x1200  | 100                  | 280.64               | 1600                      | 128            | 176           | 304           | 1200            | 1              | 3             | 67            | n                 | p                 |
| 1680x1050  | 60                   | 147.14               | 1680                      | 104            | 184           | 288           | 1050            | 1              | 3             | 33            | n                 | p                 |
| 1792x1344  | 60                   | 204.8                | 1792                      | 128            | 200           | 328           | 1344            | 1              | 3             | 46            | n                 | p                 |
| 1792x1344  | 75                   | 261                  | 1792                      | 96             | 216           | 352           | 1344            | 1              | 3             | 69            | n                 | p                 |
| 1856x1392  | 60                   | 218.3                | 1856                      | 96             | 224           | 352           | 1392            | 1              | 3             | 43            | n                 | p                 |
| 1856x1392  | 75                   | 288                  | 1856                      | 128            | 224           | 352           | 1392            | 1              | 3             | 104           | n                 | p                 |
| 1920x1200  | 60                   | 193.16               | 1920                      | 128            | 208           | 336           | 1200            | 1              | 3             | 38            | n                 | p                 |
| 1920x1440  | 60                   | 234                  | 1920                      | 128            | 208           | 344           | 1440            | 1              | 3             | 56            | n                 | p                 |
| 1920x1440  | 75                   | 297                  | 1920                      | 144            | 224           | 352           | 1440            | 1              | 3             | 56            | n                 | p                 |

[END]