

Rui (Rick) Xie

Email: xier2018@mail.sustech.edu.cn

xr@ieee.org

Portfolio: rickxie.xyz

Mobile: +86-13048877424

(Updated Sep. 2021)

EDUCATION

- **Southern University of Science and Technology (SUSTech), BEng (Honor Class)** China
GPA: 3.7/4.0, Rank: 17/60
Advisor: Quan Chen
Expected Summer 2022

EXPERIENCE

- **University of Oxford** Oxford, United Kingdom
Oxford International Study Abroad Programme
Jul. 2019 – Aug. 2019
 - **Big Data and Social Media:** R Programming and Data Analysis.
 - **University, Tutorial System and Interdisciplinary:** Research on Mass Psychology and Higher Education.
- **The University of Hong Kong** Remote
Online Summer Research (Host: Zhongrui Wang)
Jun. 2021 – Aug. 2021
 - **Feedback States Convergence Adjustment of Memristor:** Adjust the device to I-V curve.
 - **ARC One Implementation:** Converge method of memristor device on *ArC ONE* and Keysights B1500A.

RESEARCH INTERESTS

- **EDA Circuits Simulation**
Electronic Design Automation
 - **Steady-State Memristor Crossbar Array (MCA) Circuit Simulation:**
 1. Exploited the structural regularity of MCAs to develop preconditioner;
 2. Designed the inverse process by Kronecker product and block matrix formula;
 3. Tested the numerical verification of the flow;
 4. Obtained a Fund of **10,000 CHY**.
 - **Surrogate Modeling of Electro-Thermal Simulation:**
 1. Used *Ansys Icepak* and simulated the process of SiC sandwich devices;
 2. Designed the surrogate model.
 - **RRAM (Resistive RAM) Non-Ideal Simulation:**
 1. Designed the multiply-add method;
 2. Developed the simulator by noise model and non-linearity.

HONORS AND AWARDS

- **Third Class of the Merit Student Scholarship** Sep. 2019
SUSTech < 20%
- **Second Class of the Merit Student Scholarship** Sep. 2020
SUSTech < 7%
- **Third Prize of China College IC Competition in Southern China** Jul. 2020
Ministry of Industry and Information Technology < 10%
- **First Prize of College Student Innovation and Entrepreneurship Training Program** Mar. 2021
School of Microelectronics, SUSTech 10%
- **Outstanding Cadre Award of Zhicheng College** May. 2021
Zhicheng College, SUSTech 3%
- **First Class of the Merit Student Scholarship** Sep. 2021
SUSTech < 3%

SKILLS

- **Programming Languages:** Python, MATLAB, C, Java, Verilog HDL, Scala
- **Software:** Virtuoso, Quartus, ModelSim, Icepack, Silvaco, LTSPICE, Comsol, SolidWorks, AutoCAD
- **Spoken Languages:** Mandarin, English, Cantonese, Japanese (Learning)

PUBLICATIONS

1. **Xie, R.**, Song, M., Zhou, J., Mei, J., & Chen, Q. (2021). A Fast Method for Steady-State Memristor Crossbar Array Circuit Simulation. IEEE ICTA 2021

PATENTS

1. Chen, Q. Fan, D. **Xie, R.** Song, M. Construction and optimization of neural networks for memristor arrays based on circuit simulation. CN 202110673101.5 (Pending)

PROJECTS

- **An optimization algorithm for demosaicing using DE-1 FPGA and camera with LCD screen display:**

1. Crafted parallel demosaic algorithm, with median filtering and gamma correction;
2. Four pipelines to store 4×4 pixel data for speed up;
3. Deployed on DE1 FPGA, 5CSEMA5F31C6.

- **SOBEL operator edge detection on FPGA based on ARM architecture:**

1. Customized architecture by CMSDK of Arm Cortex-M3 DesignStart Eval IP;
2. Float-avoid operations by lookup tables, simplify the square and multiplication operations;
3. Pixel thresholds tests to ensure accuracy of real-time display.

- **TPU development based on RISC-V and Chisel based on Scala:**

1. A Google TPU structure based on systolic array using Chisel;
2. Redesigned look up table multiplier;
3. VGG-16 network test, $10\times$ less energy consumption than common structure.

- **Campus Bus Travel Time Prediction Based on LSTM and Big Data Techniques:**

1. LSTM based prediction method, showing the congestion level and arrival time;
2. Friendly UI and Deployed on WeChat Program, accepted by SUSTech Campus Bus;
3. Got a fund of **10,000 CHY**;
4. Won the first prize of 2021 School of Microelectronics Innovation Competition.

- **A design of 4×4 Bits array multiplier based on virtuoso:**

1. A 4×4 array multiplier of $180nm$ technique on Virtuoso of Cadence with special carry method;
2. $10\times$ less area consumption than common design;
3. Designed with layered structure and organized locating and wiring.

- **Neural architectural search for RRAM-based AI accelerator:**

1. An organized network with One-Shot NAS by NNI (An open source AutoML toolkit by Microsoft);
2. For EDathon 2021 project, an competition held by CEDA Hong Kong with graduate students;
3. Ranked **7/24** in the EDathon 2021 with graduates.

- **An innovative single-threaded automatic target detection system based on Raspberry Pi:**

1. Sophomore course project with Raspberry Pi;
2. Designed the technique of logical value with dichotomous approximation;
3. *AutoCAD* and *SolidWorks* based design.