D.1 MEC172x Pin State on Exit

All Pins will be in the hardware defined default state except the following pins listed in the table.

TABLE D-1: BOOT ROM PIN STATE ON EXIT

Pin Name	Alternate Function Selected	GPIO Pin Control Register Value (Note 1)	GPIO Pin Control Register 2 Value (Note 1)
JTAG Interface (DEBUG_EN = 1 - Enabled by JTAG_RST# pin)			
GPIO147/SMB08_DATA/JTAG_CLK	JTAG_CLOCK	N/A	N/A
GPIO150/SMB08_CLK/JTAG_TMS	JTAG_DATA	N/A	N/A
ESPI MAFS Interface			
GPIO061/ESPI_RESET#	ESPI_RESET#	0000_1040h	0000_0031h
GPIO063/ESPI_ALERT#	ESPI_ALERT#	0000_1040h	0000_0031h
GPIO065/ESPI_CLK	ESPI_CLK	0000_1040h	0000_0031h
GPIO066/ESPI_CS#	ESPI_CS#	0000_1040h	0000_0031h
GPIO070/ESPI_IO0	ESPI_IO0	0000_1040h	0000_0031h
GPIO071/ESPI_IO1	ESPI_IO1	0000_1040h	0000_0031h
GPIO072/ESPI_IO2	ESPI_IO2	0000_1040h	0000_0031h
GPIO073/ESPI_IO3	ESPI_IO3	0000_1040h	0000_0031h
Power Sequencing Pin Interface			
GPIOxxx(DPWREN) (Note 3)	GPIO	0001_0240h	hardware default
GPIOxxx(DSW_PWROK) (Note 3)	GPIO	0001_0240h	hardware default
GPIOxxx(SUS_PWR_EN) (Note 3)	GPIO	0001_0240h	hardware default
GPIO055(RSMRST#) (Note 3)	GPIO	ESPI: 0001_0240h QSPI: hardware default	hardware default
Comparator 0 Interface (OTP Byte 92 - Bits[0] CMP_STRAP Enable=1)			
GPIO057/CMP_VIN0	CMP_VIN0	0000_2000h	hardware default
GPIO226/CMP_VREF0	CMP_VREF0	0000_3000h	hardware default
GPIO241/CMP_VOUT0	CMP_VOUT0	0003_31F0h	hardware default

Note 1: All other pins should be in their hardware default state since they are not manipulated by the Boot ROM. Please refer to the MEC172x Data Sheet for the GPIO Pin Control register and the GPIO Pin Control 2 register defaults.

2: 'X' is nibble is undefined. 'x' is bit is undefined.

3: GPIOxxx indicates OTP may be configured to use any GPIO for that function