

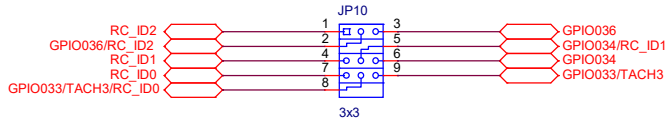
JOSHUATREE EVB

Mates with JoshuaTree Daughter Cards

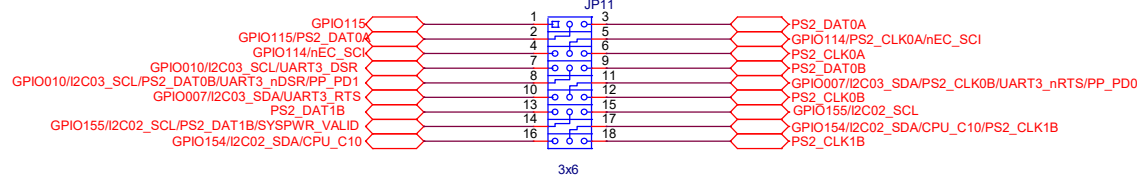
Description	Sheet
Title Page	1
Joshua Tree Daughter Card and Straps	2
Demux Signals - 1	3
Demux Signals - 2	4
Power and Resets	5
Power FET's	6
GPIO	7
SMBus Headers	8
JTAG, PECl, FANs and SPI	9
UARTs, RC_ID, and Trace FIFO Header	10
Therm Diodes, Key Scan	11
ESPI & LPC Fingers	12
ADC, Comparator	13
PS2, Battery Logic	14
FT4222 & PP	15
UART 2 & 3	16
USB	17

Revision History
Rev 1.0: Initial Release

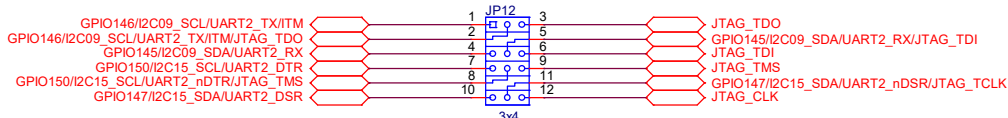
RC IDENTIFICATION DETECTION DEMUX



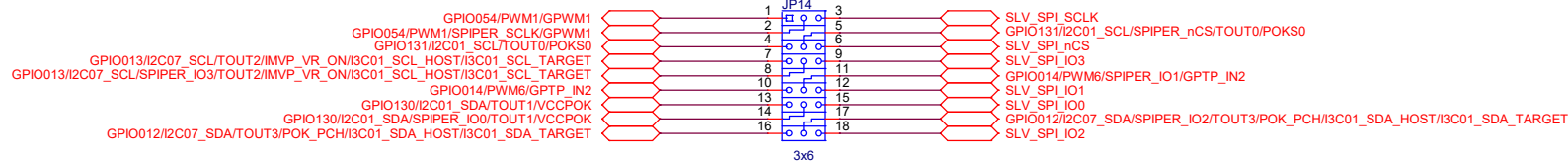
PS2 SIGNAL DEMUX



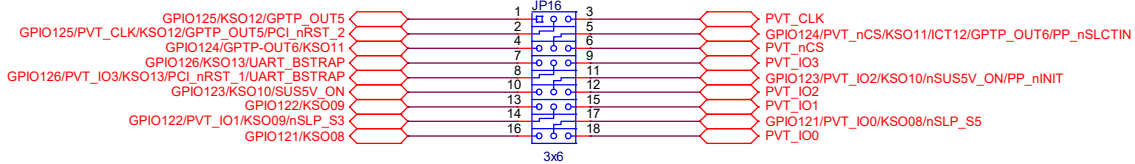
JTAG SIGNAL DEMUX



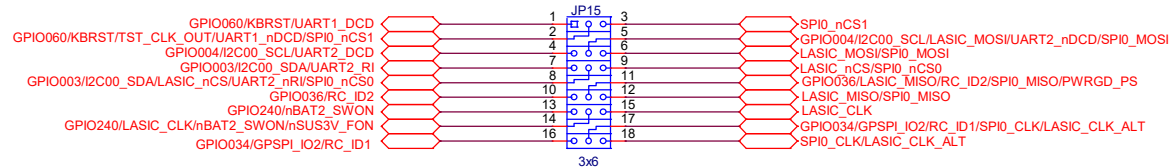
SLAVE SPI SIGNALS DEMUX



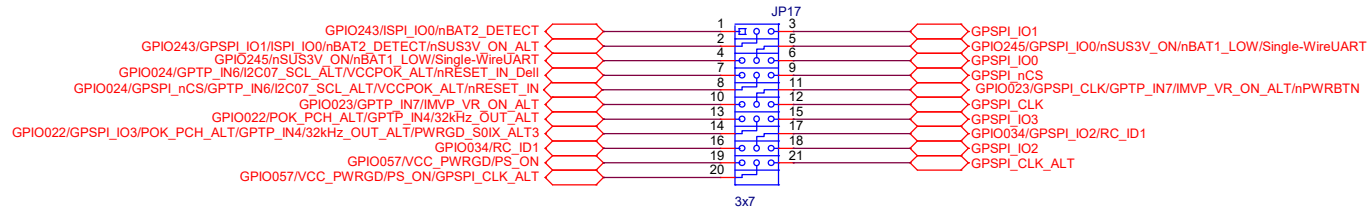
PRIVATE SPI SIGNALS DEMUX



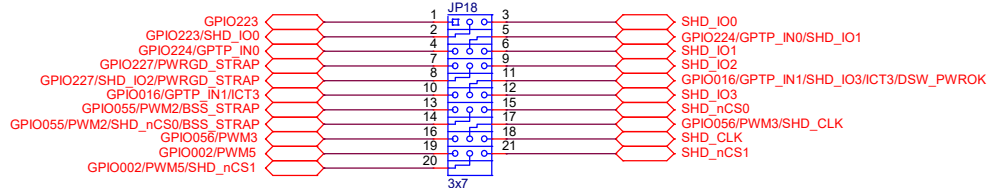
LASIC SPI & SPI0 SIGNAL DEMUX



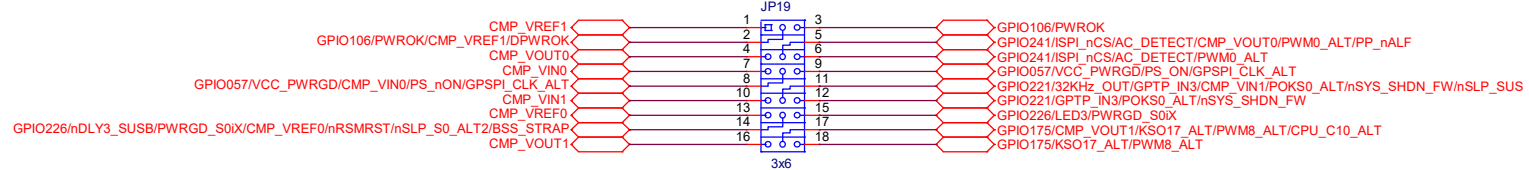
GENERAL PURPOSE SPI SIGNAL DEMUX



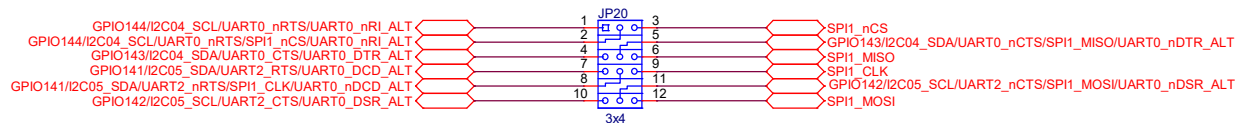
SHARED SPI SIGNAL DEMUX



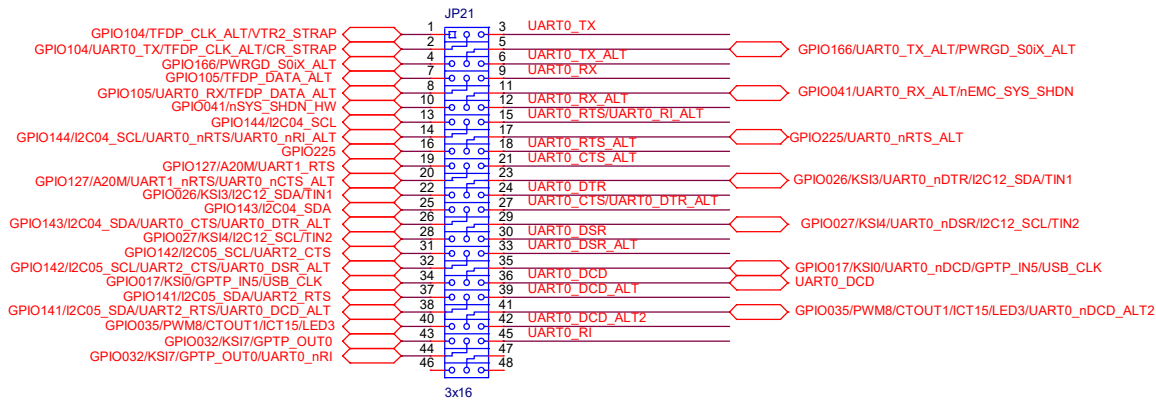
COMPARATOR SIGNAL DEMUX



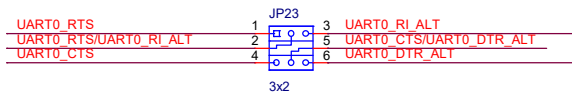
SPI1 SIGNAL DEMUX



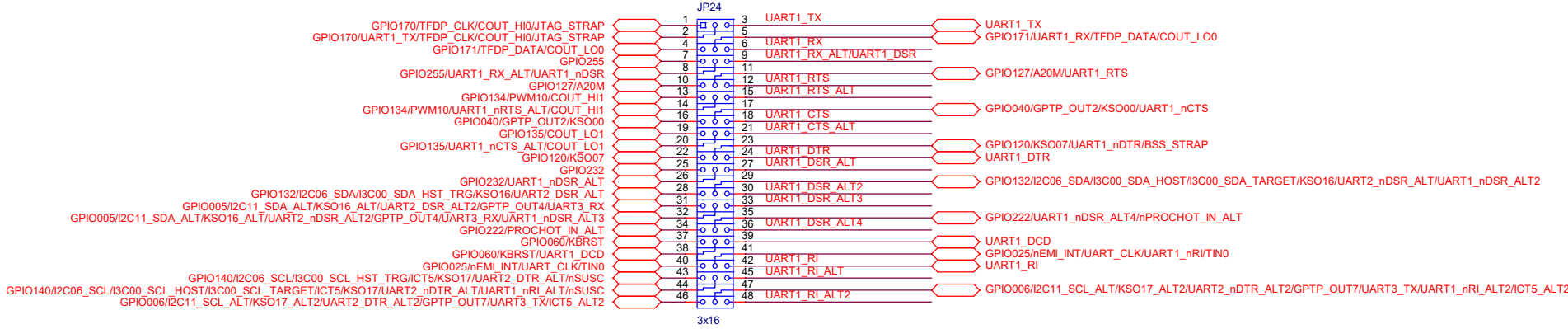
UART-0 SIGNAL DEMUX



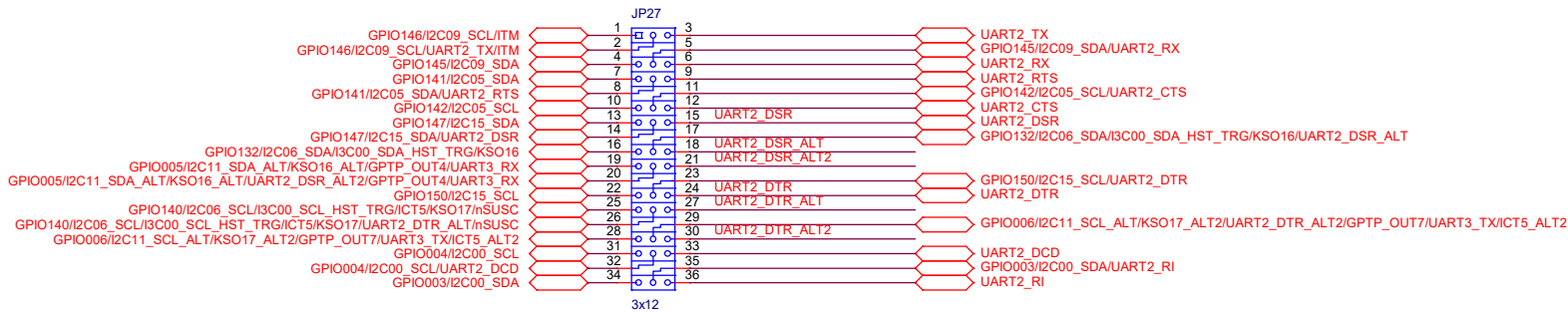
UART-0 MULTI SIGNAL DEMUX



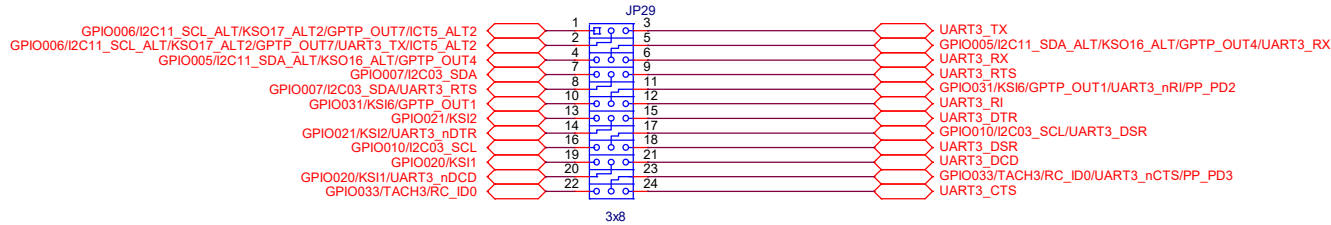
UART-1 SIGNAL DEMUX



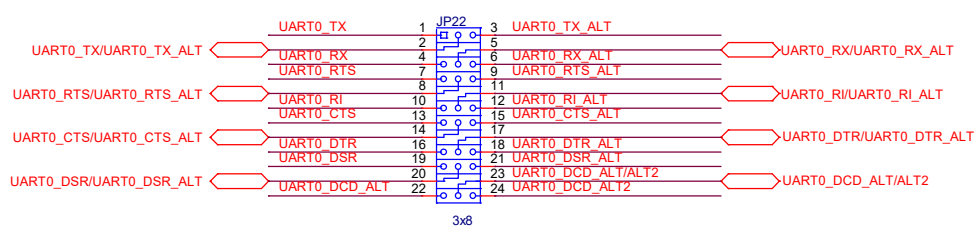
UART-2 SIGNAL DEMUX



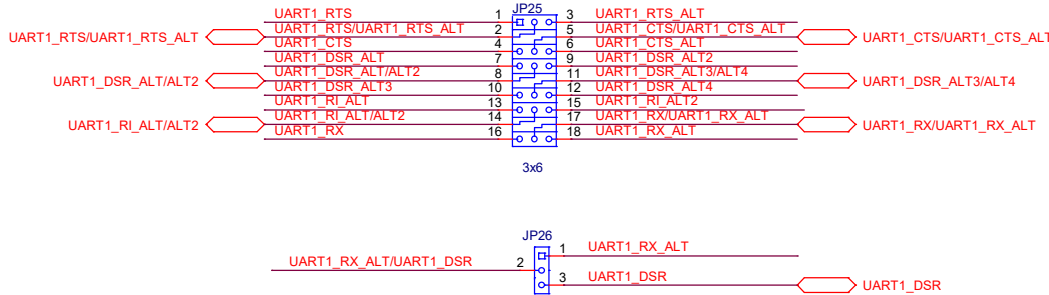
UART-3 SIGNAL DEMUX



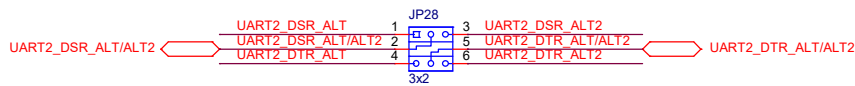
UART-0 ALTERNATE SIGNAL DEMUX



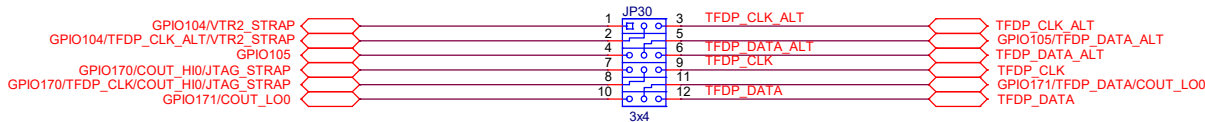
UART-1 ALTERNATE SIGNAL DEMUX



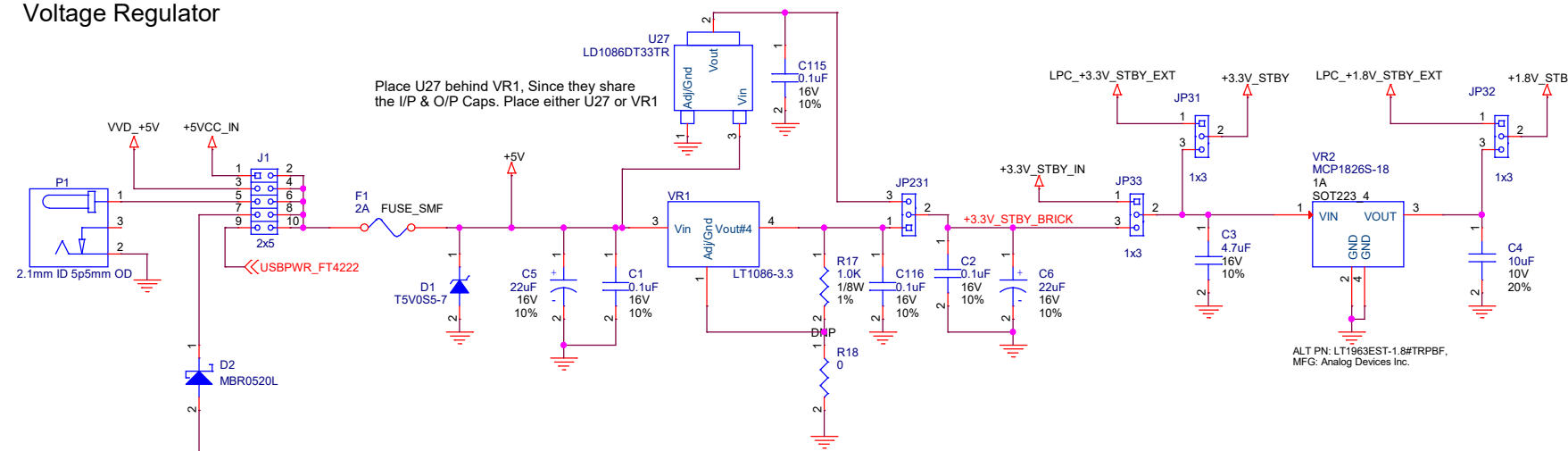
UART-2 ALTERNATE SIGNAL DEMUX



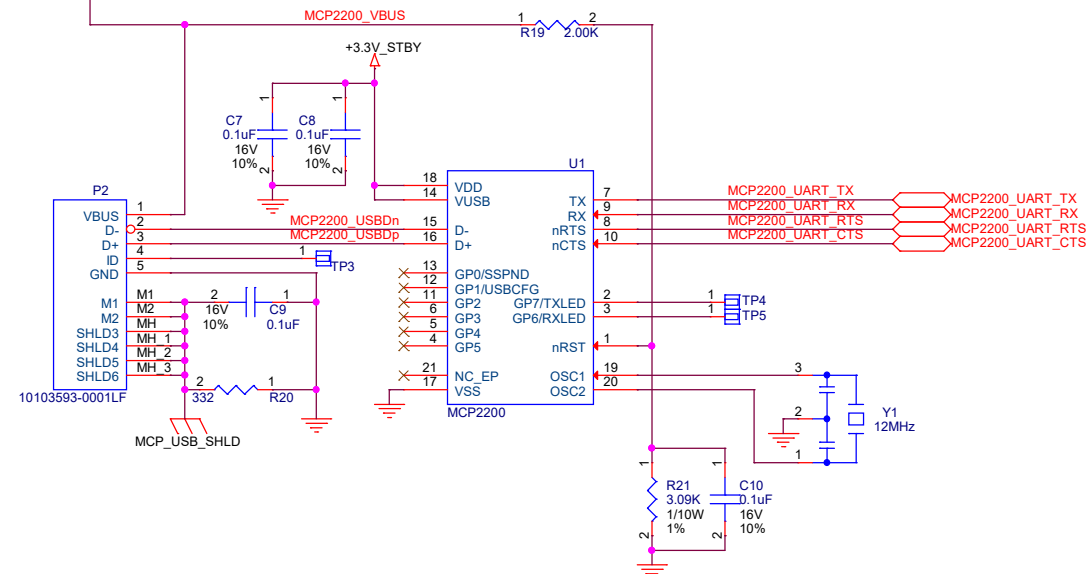
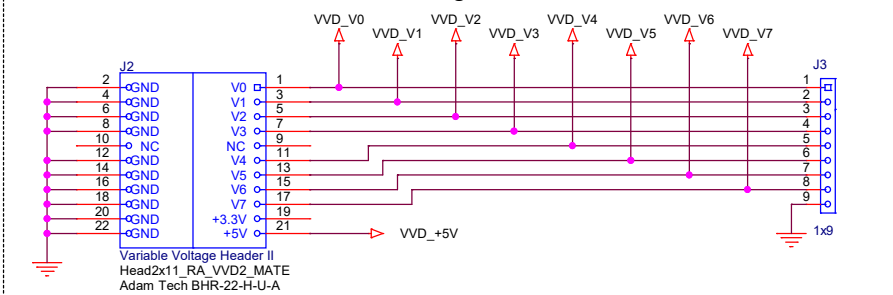
TRACE FIFO DEBUG SIGNAL DEMUX



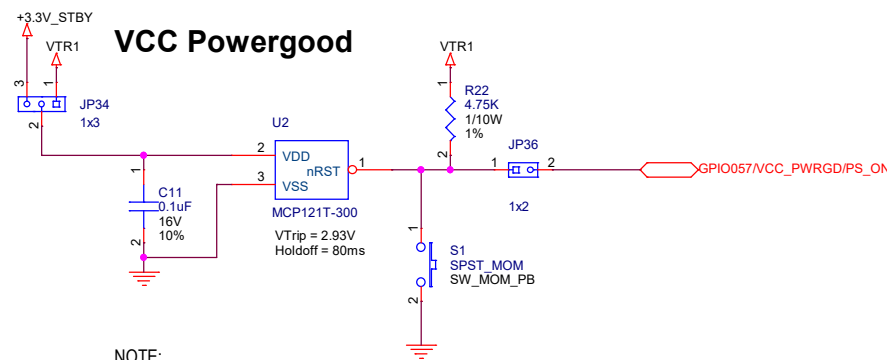
Voltage Regulator



Variable Voltage Header II

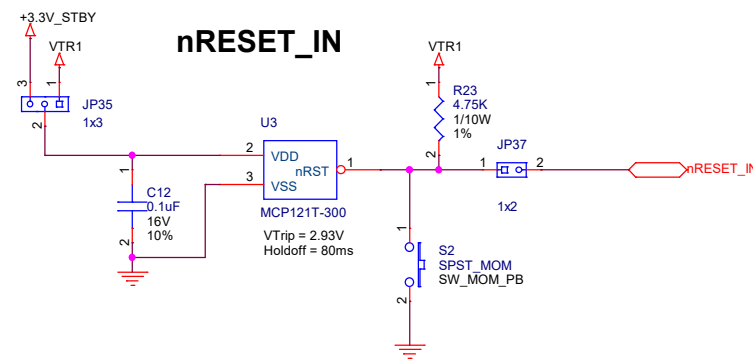


VCC Powergood



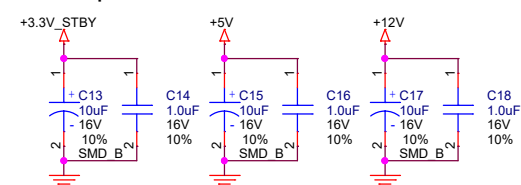
NOTE:
+3.3V powered with pull-up to VTR1

nRESET_IN

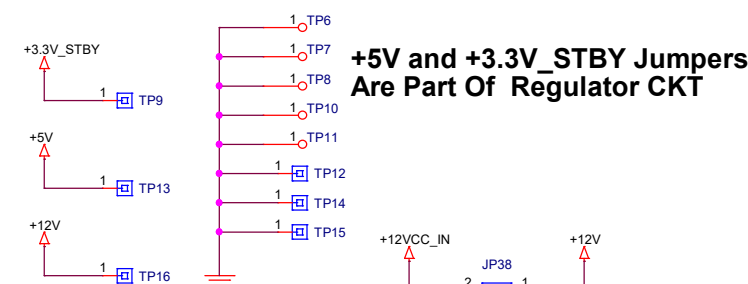


NOTE:
+3.3V_STBY powered with
pull-up to VTR1

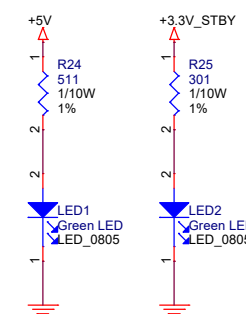
General Board Capacitors



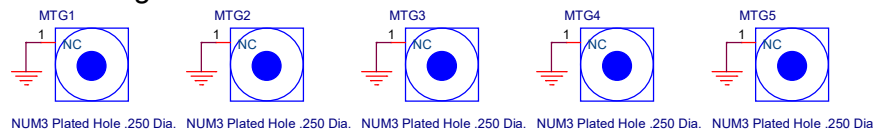
Test Points

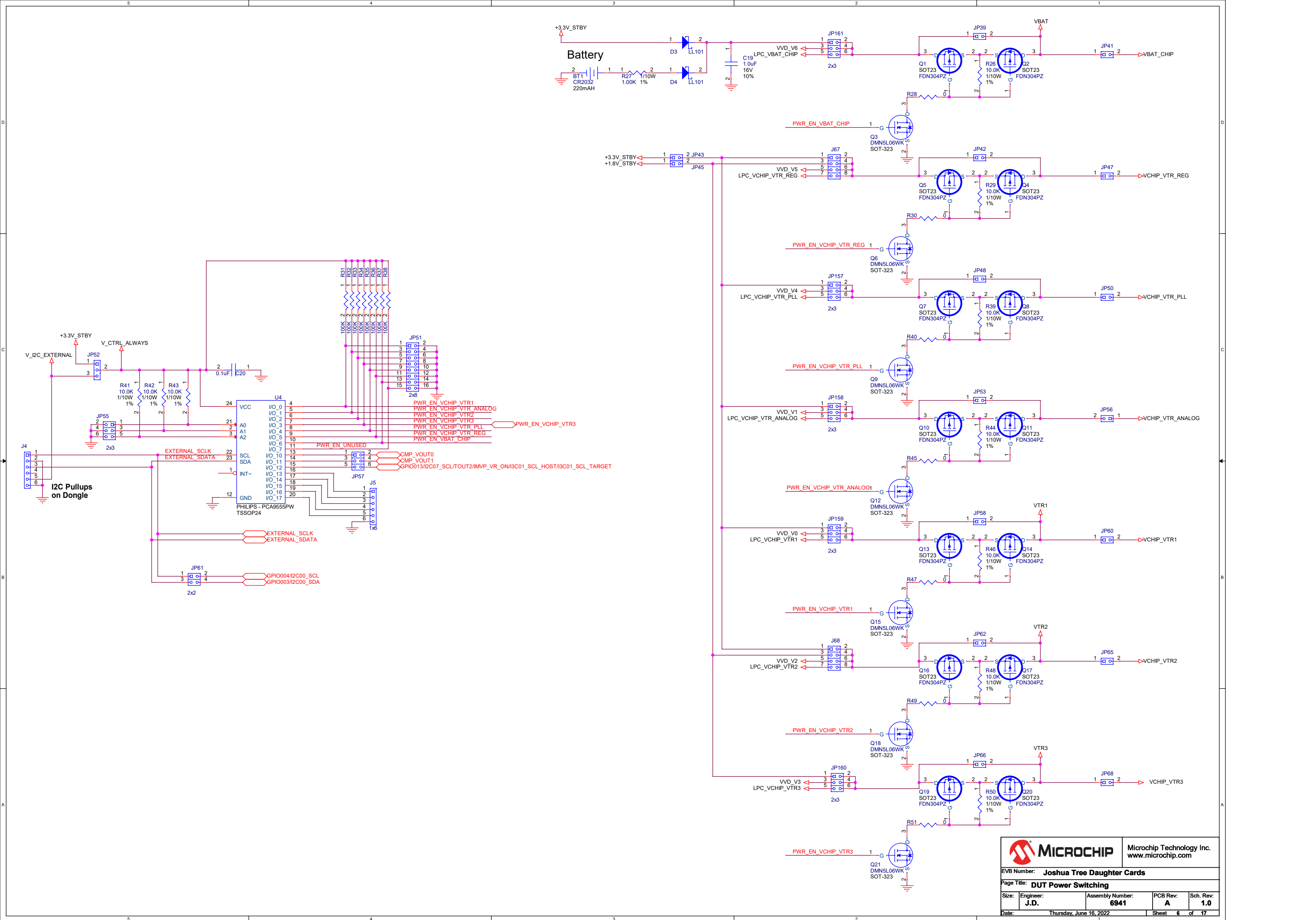


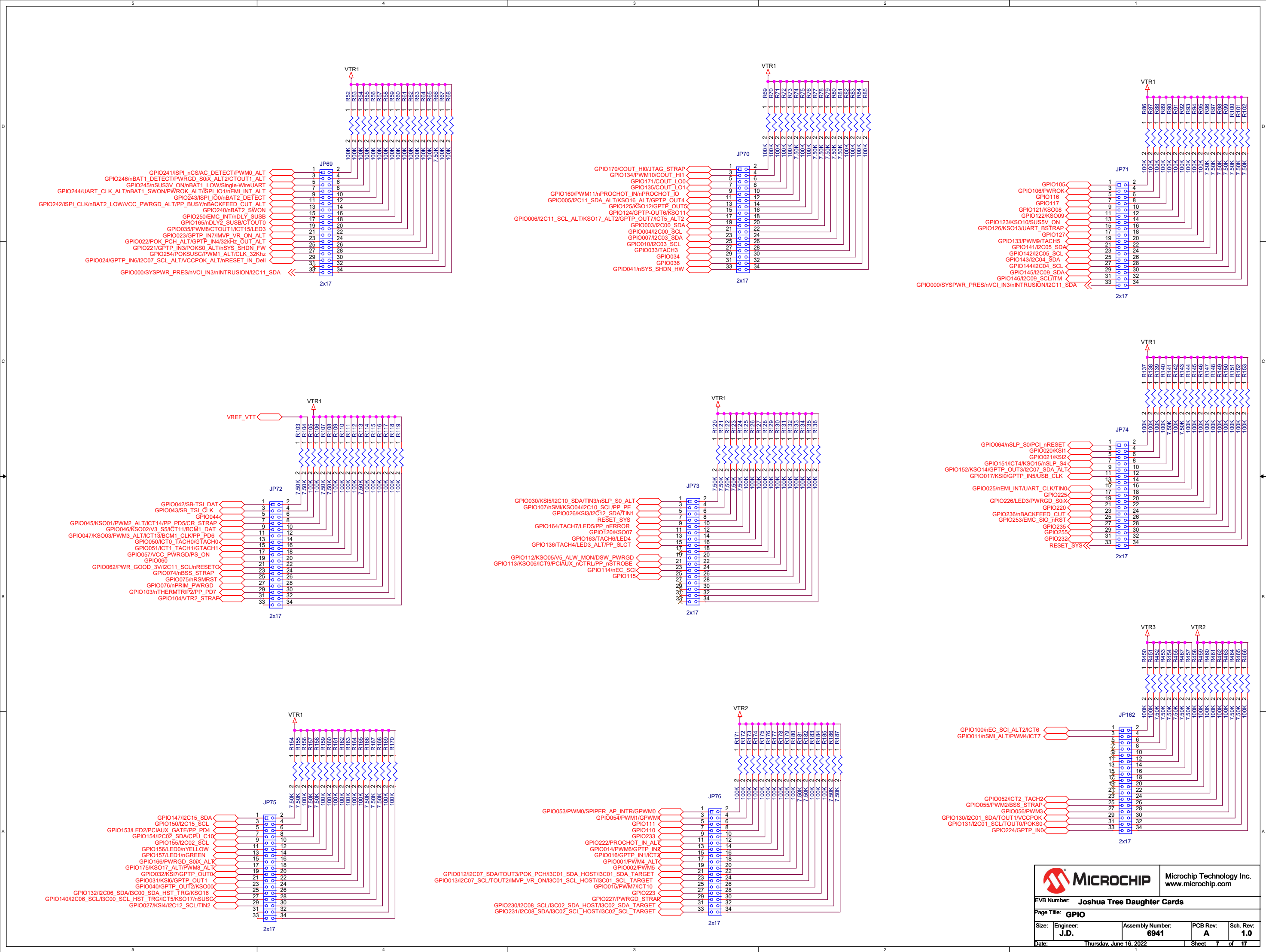
Power LEDs



Mounting Holes

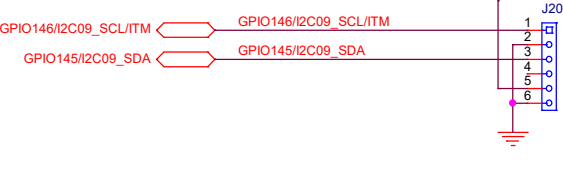
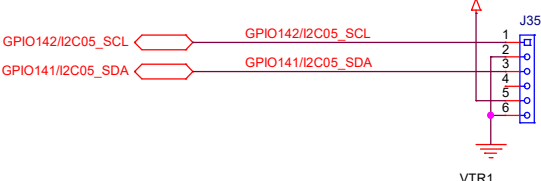
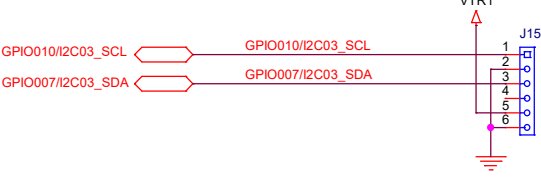
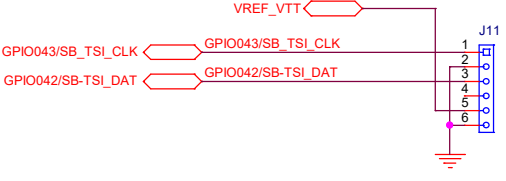
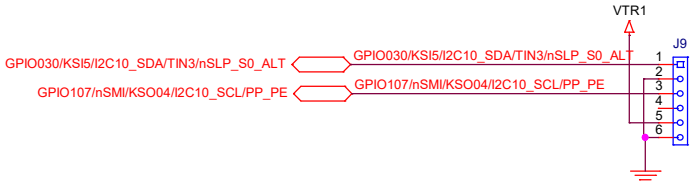
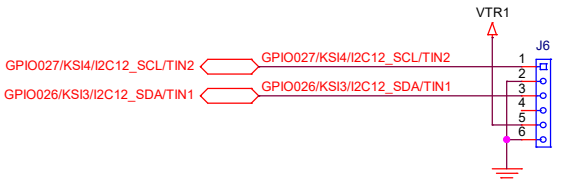
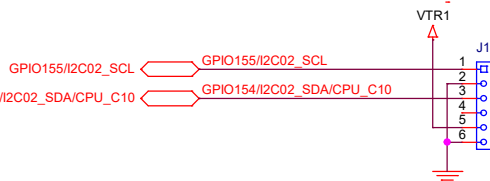
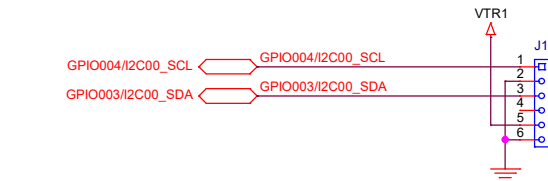
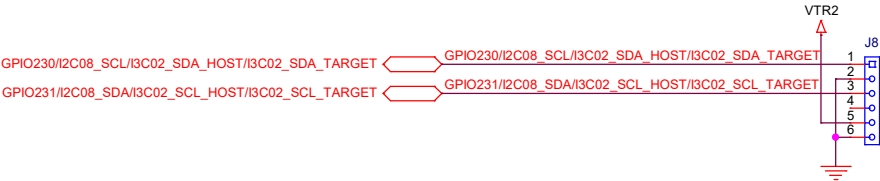




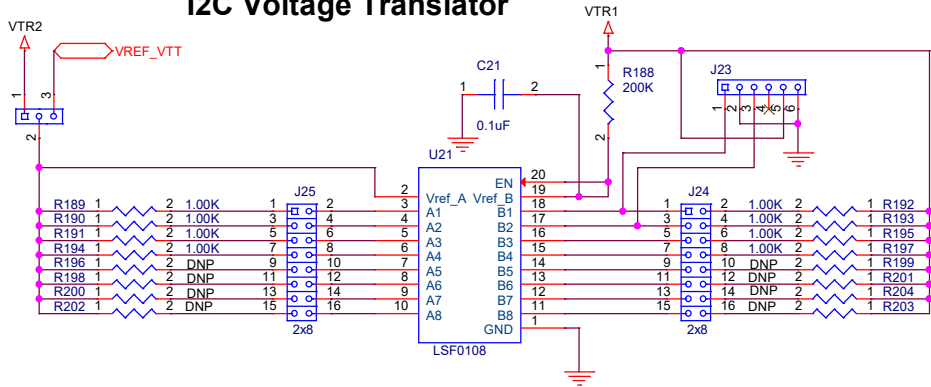


Access Bus Interface

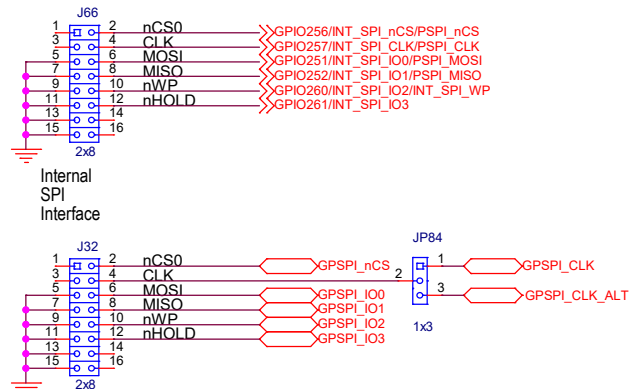
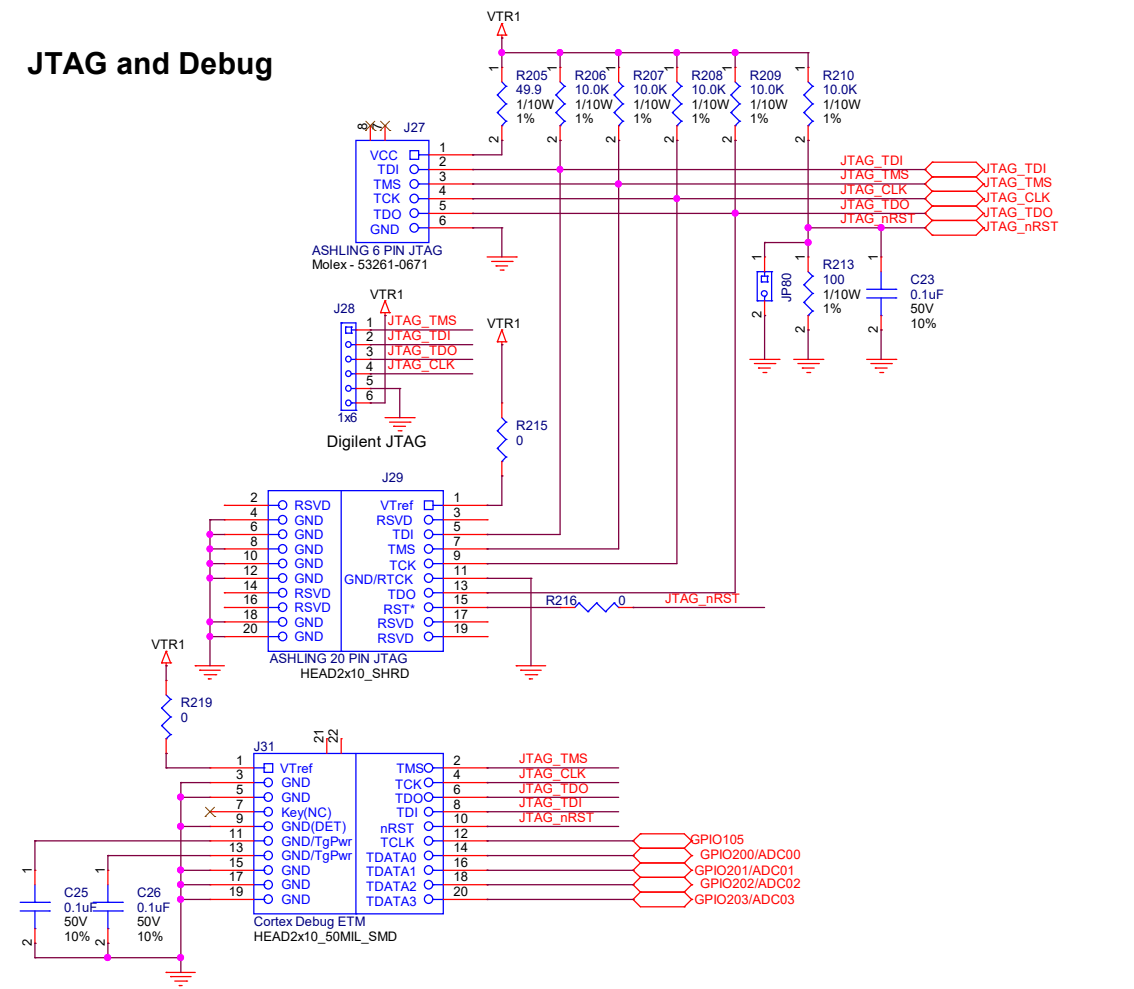
NOTE:
All pull-ups can be jumpered in at
the GPIO Headers - 7.5K Ohm.



I2C Voltage Translator

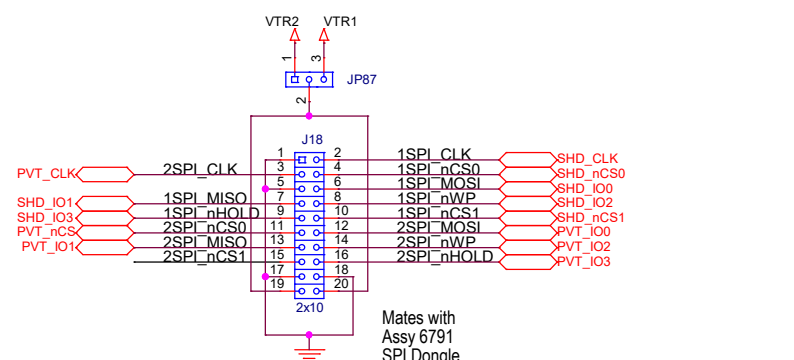



JTAG and Debug



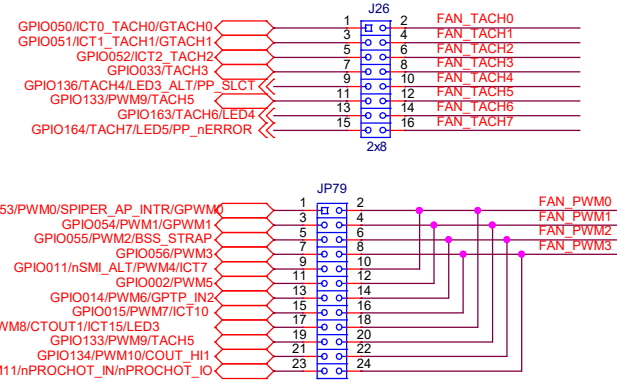
Mates with
Assy 6791
SPI Dongle
GPSPI is
VTR1 J33

Mates with Assy 6791
SPI Dongle
SLV_SPI is VTR2



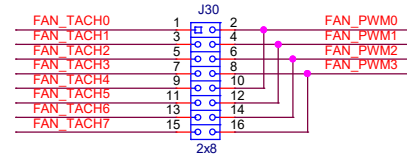
NOTE:  SPI Dongle
SHD SPI is VTR2; PVT SPI is VTR1
For proper operation, set VTR1 & VTR2 to the same voltage.

FAN and TACH Headers

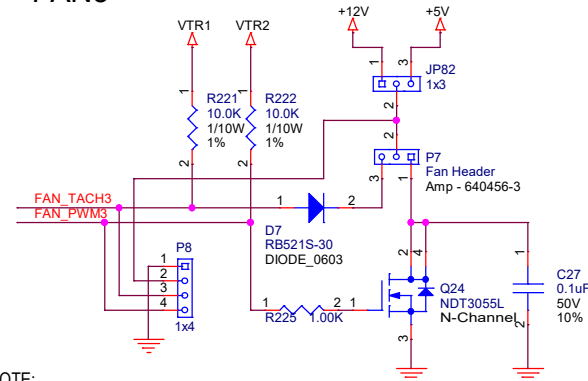


NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V

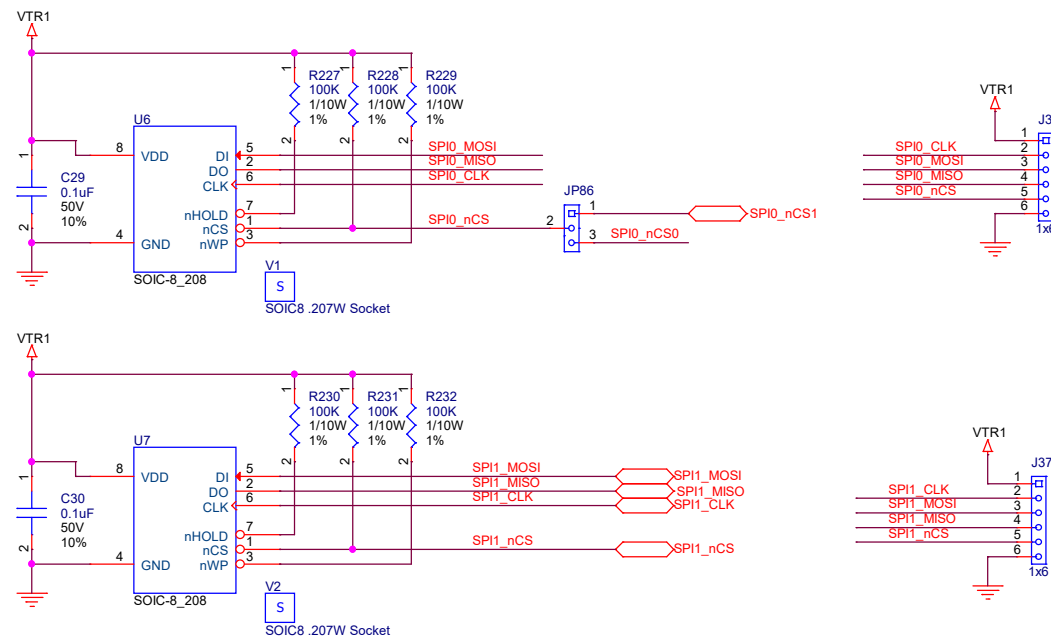
FAN and TACH Loopback



FAN3

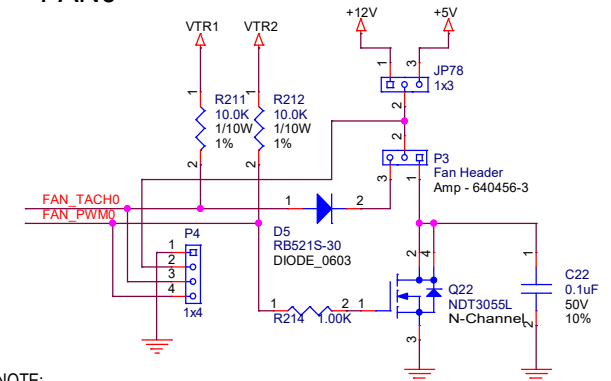


NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V



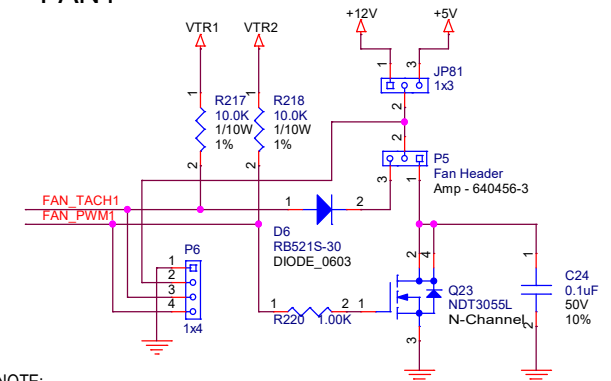
NOTE:
These SPI interfaces go to a SOIC8 socket so that +3.3V or +1.8V parts can be used.

FANO



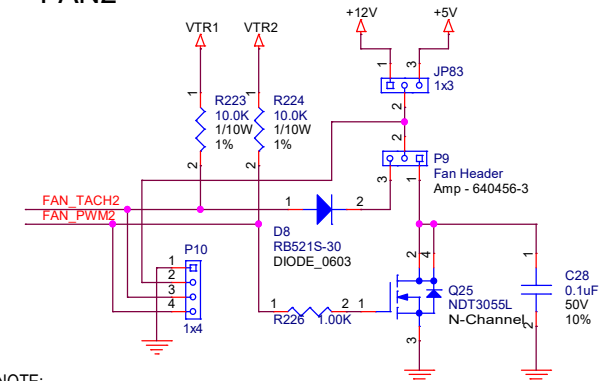
NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V

FAN1

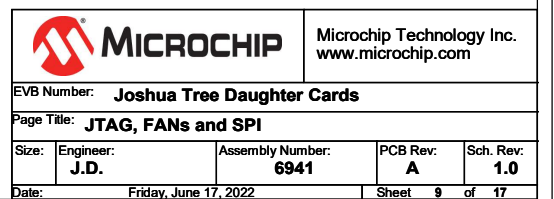
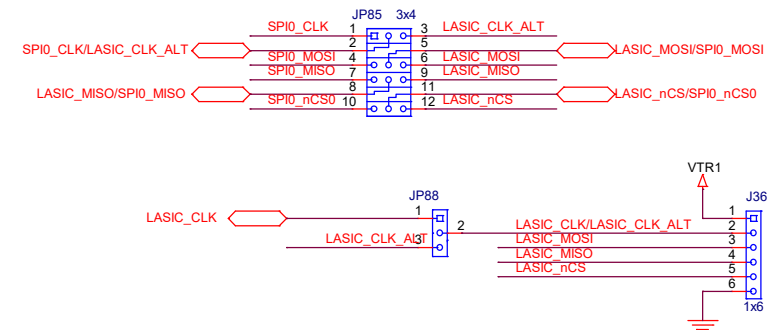


NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V

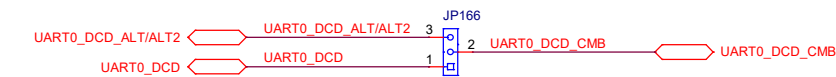
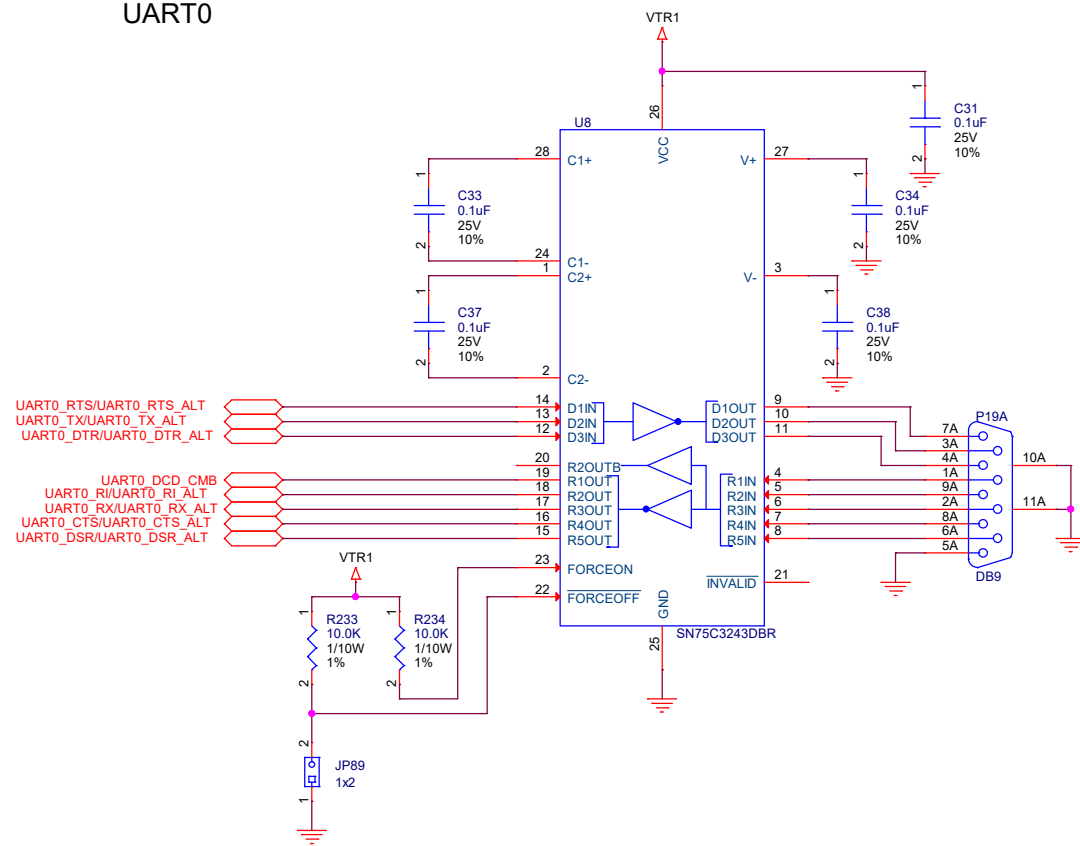
FAN2



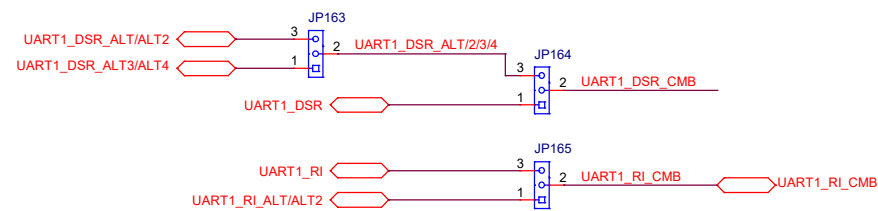
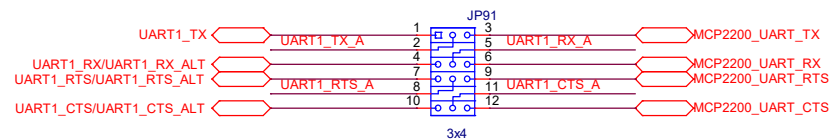
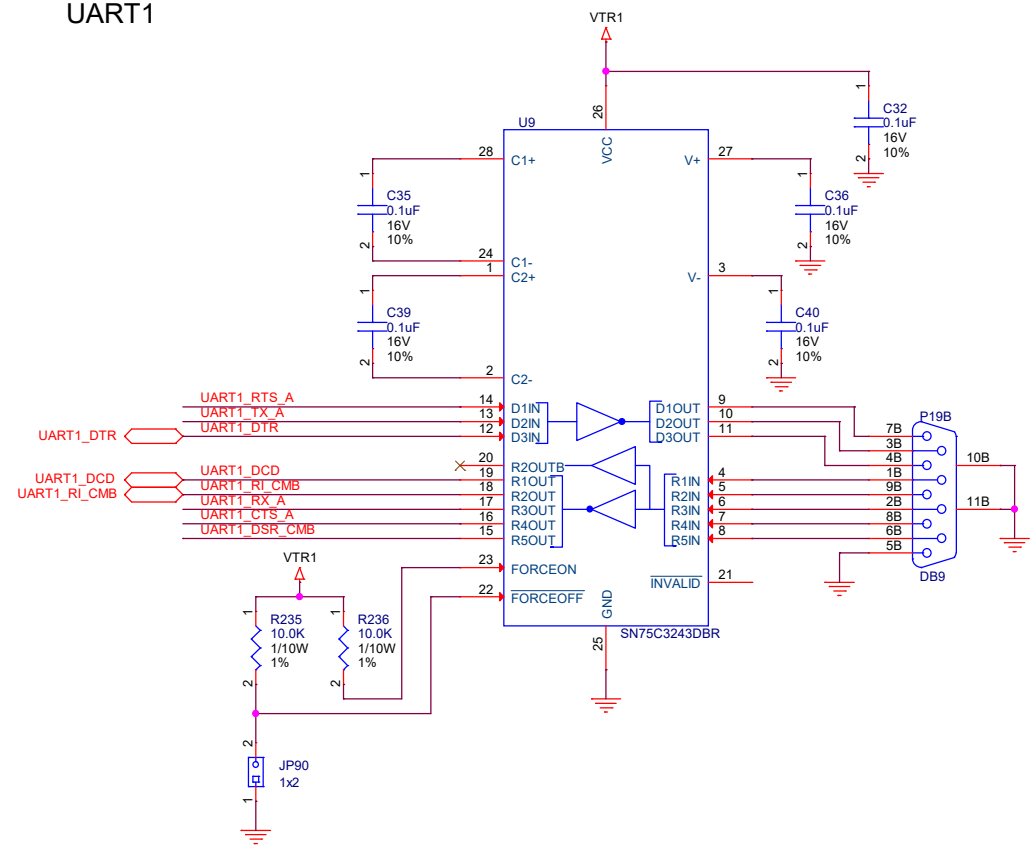
NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V



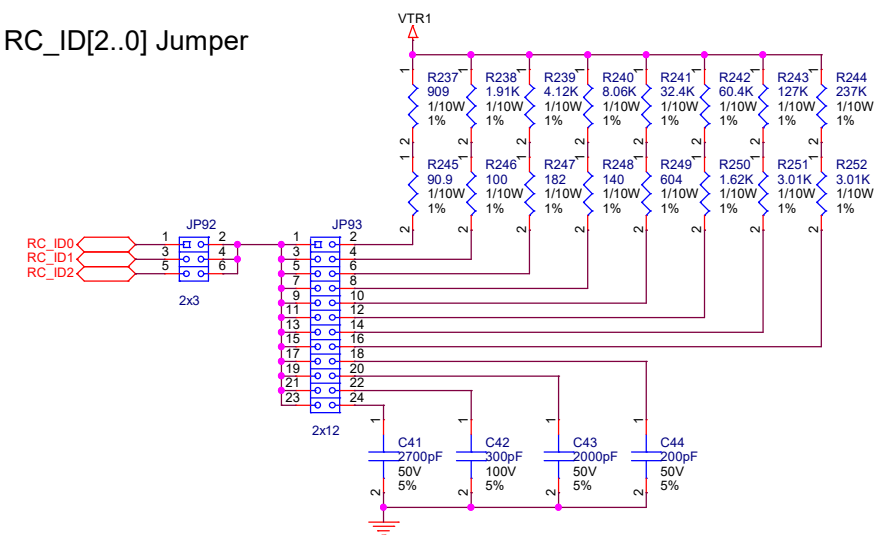
UART0



UART1



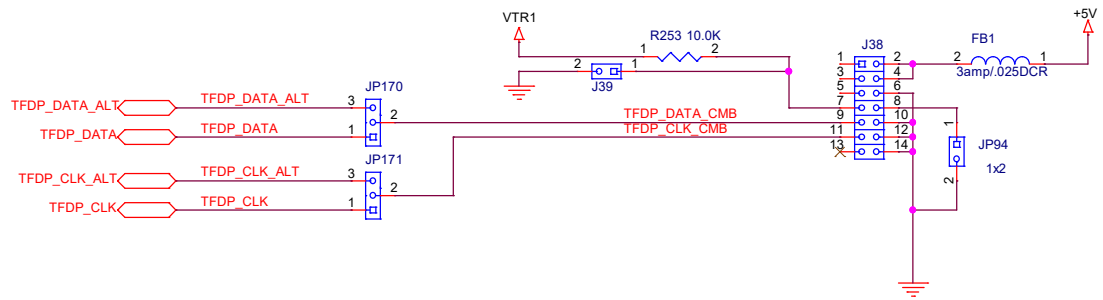
RC_ID[2..0] Jumper



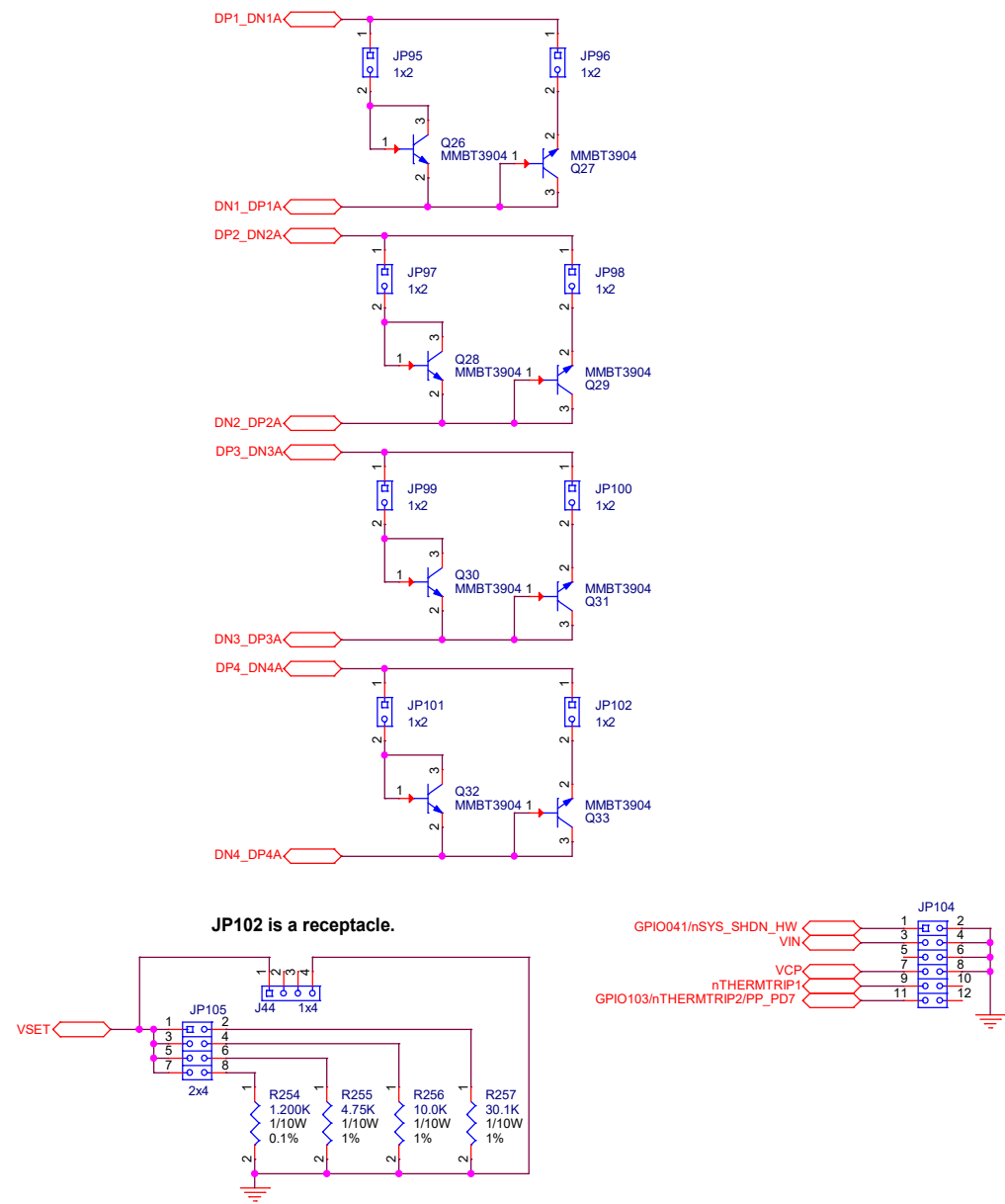
NOTE:
If VTR1 is supplied with 1.8V, the RC_ID logic will not function correctly.
VTR1 must be connected to a +3.3V supply for the RC_ID block to operate.

Software Developers Debug Interface

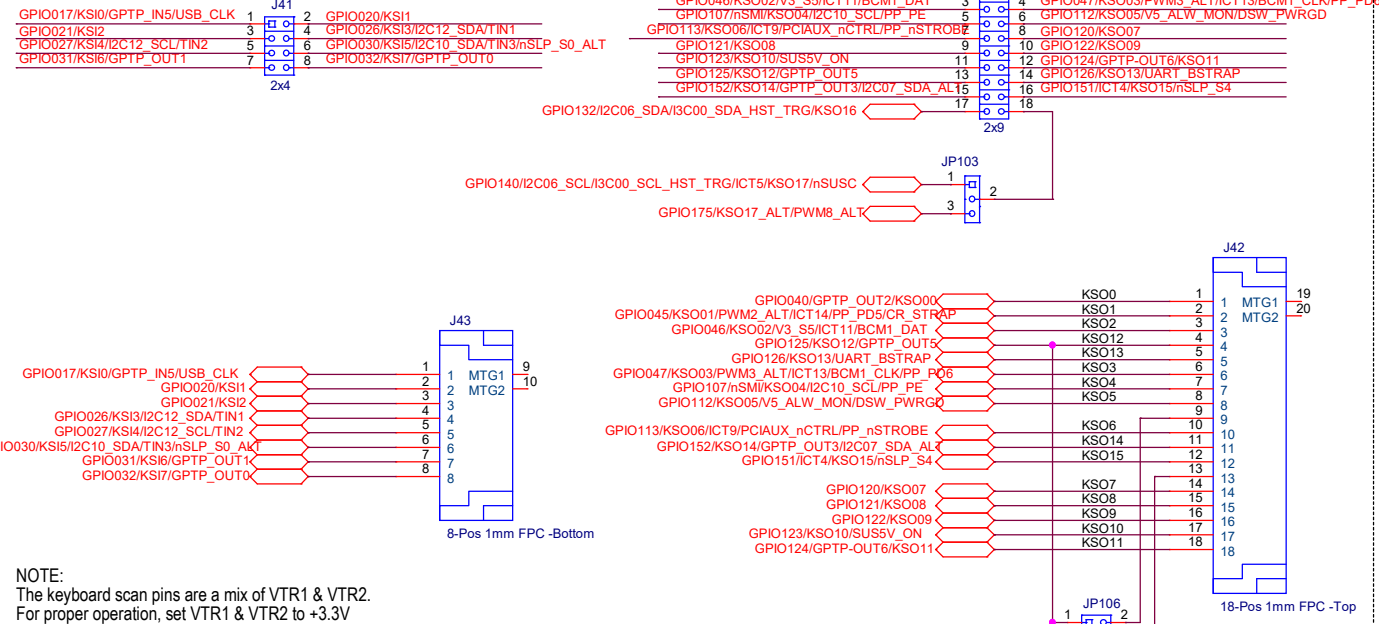
Mates with: Trace FIFO Board (Assy 6227)
Pegasus Debugger (Assy 6345)



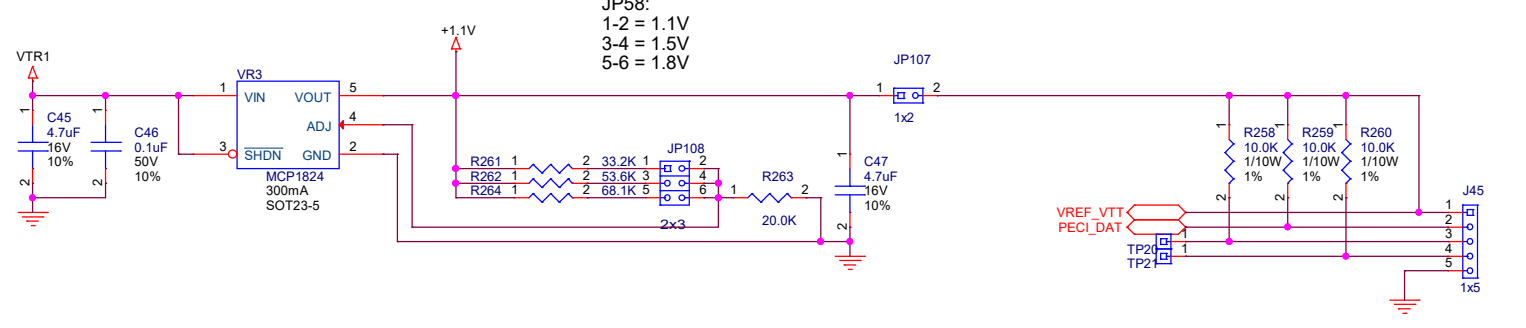
Remote Temperature Monitoring

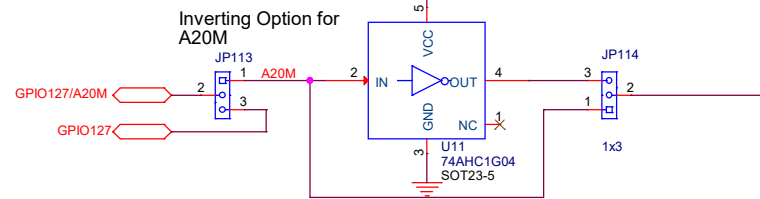
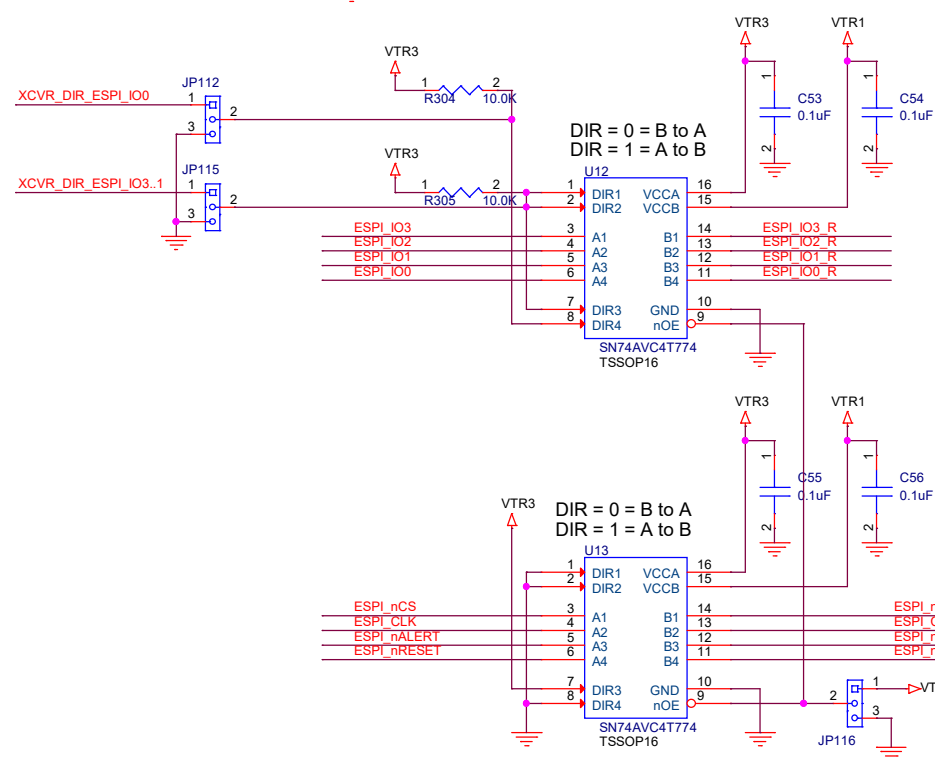
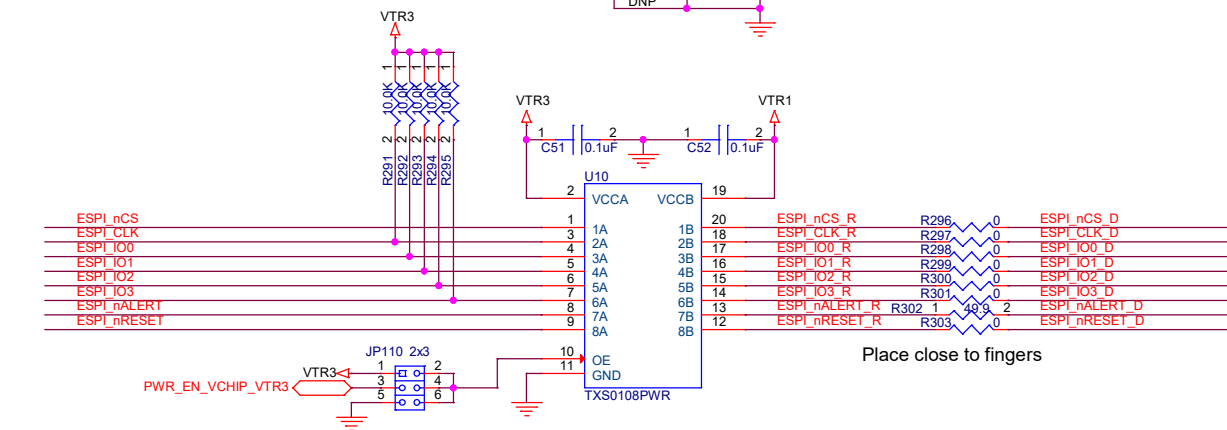
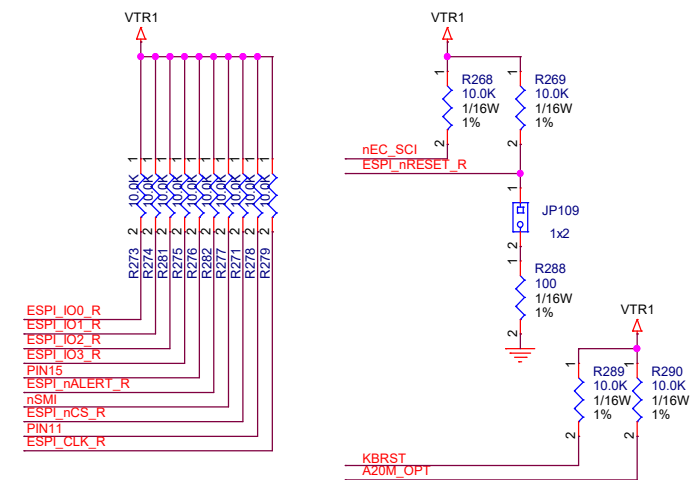
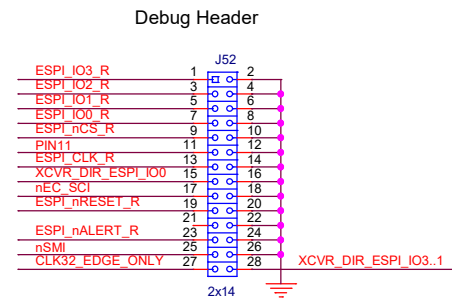
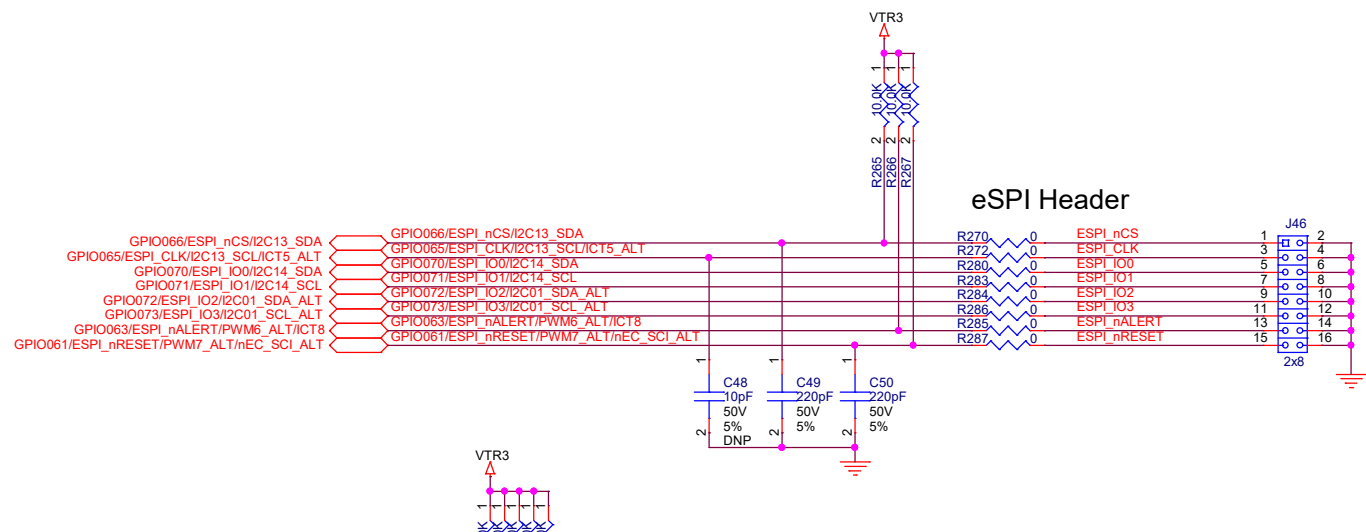


Keyboard Interface

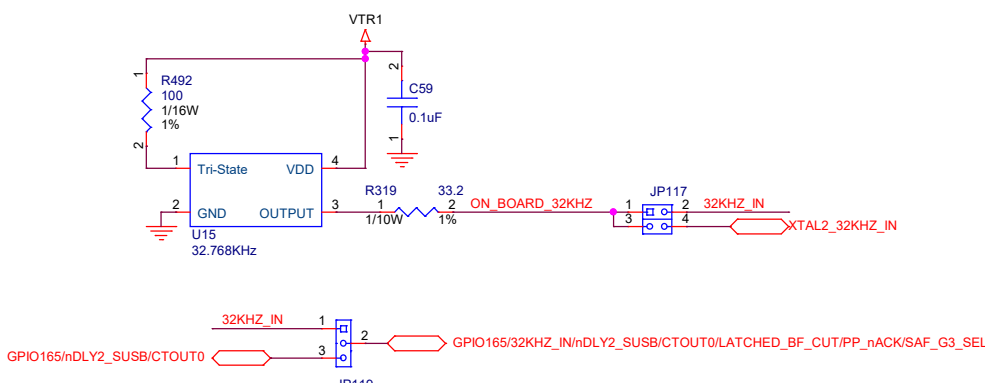
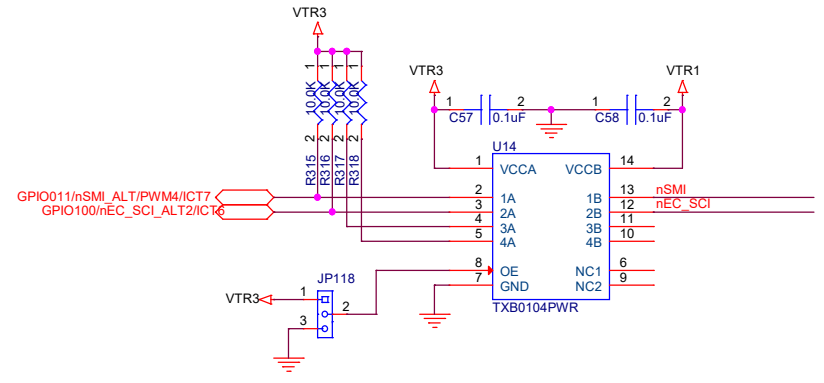
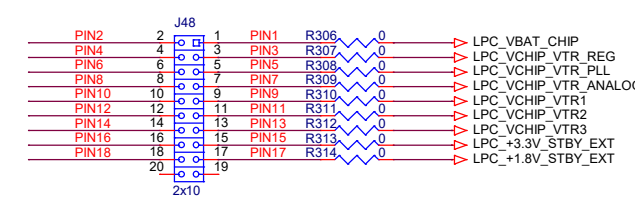
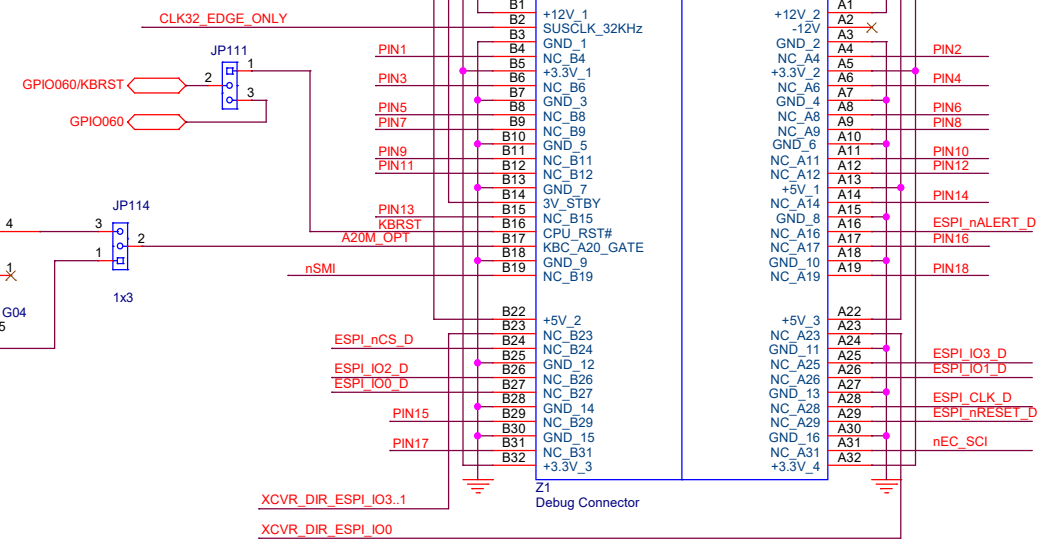


PECI Interface

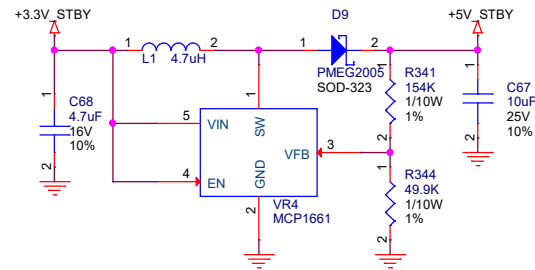




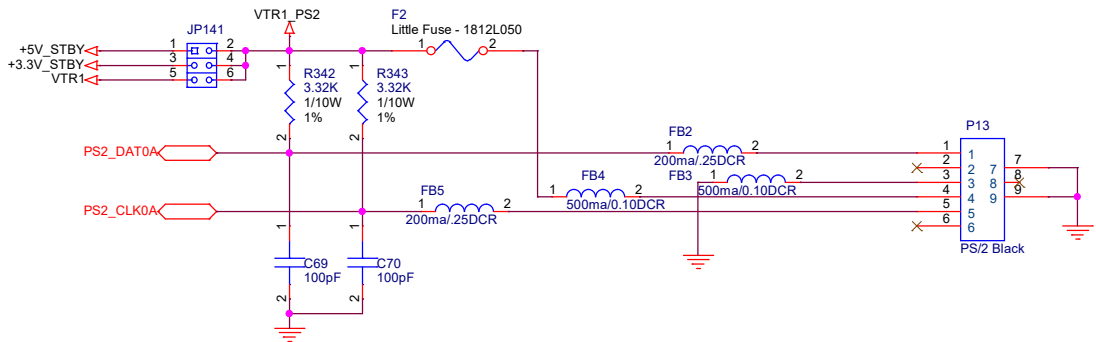
NOTE:
VTR1 powered 32kHz Osc
on EVB
This signal is not used on
this EVB



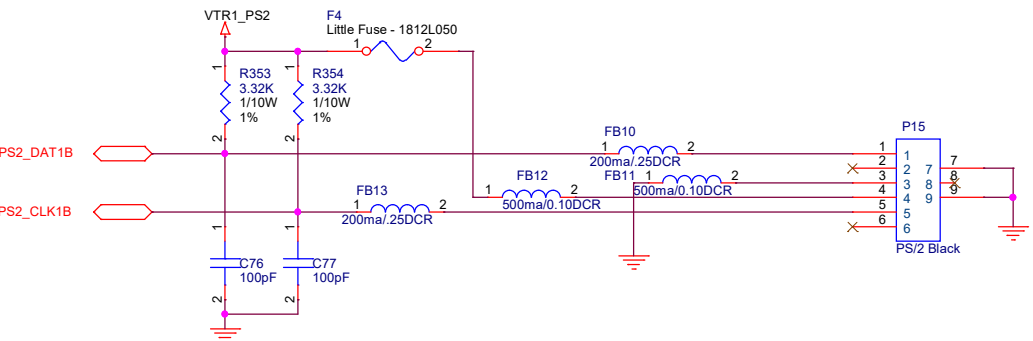
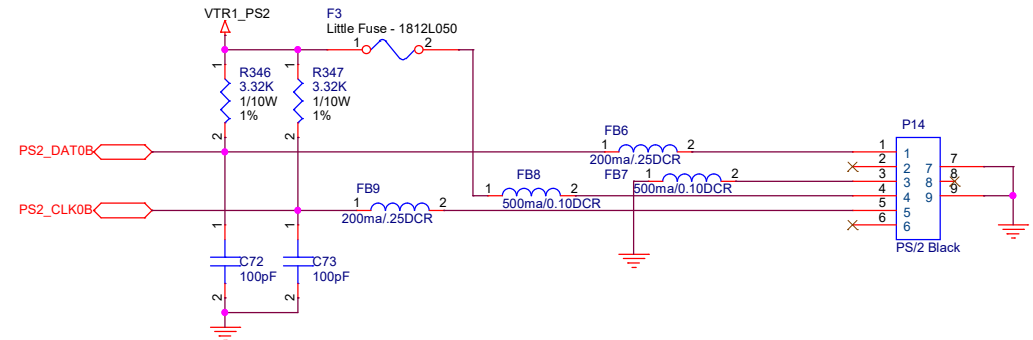
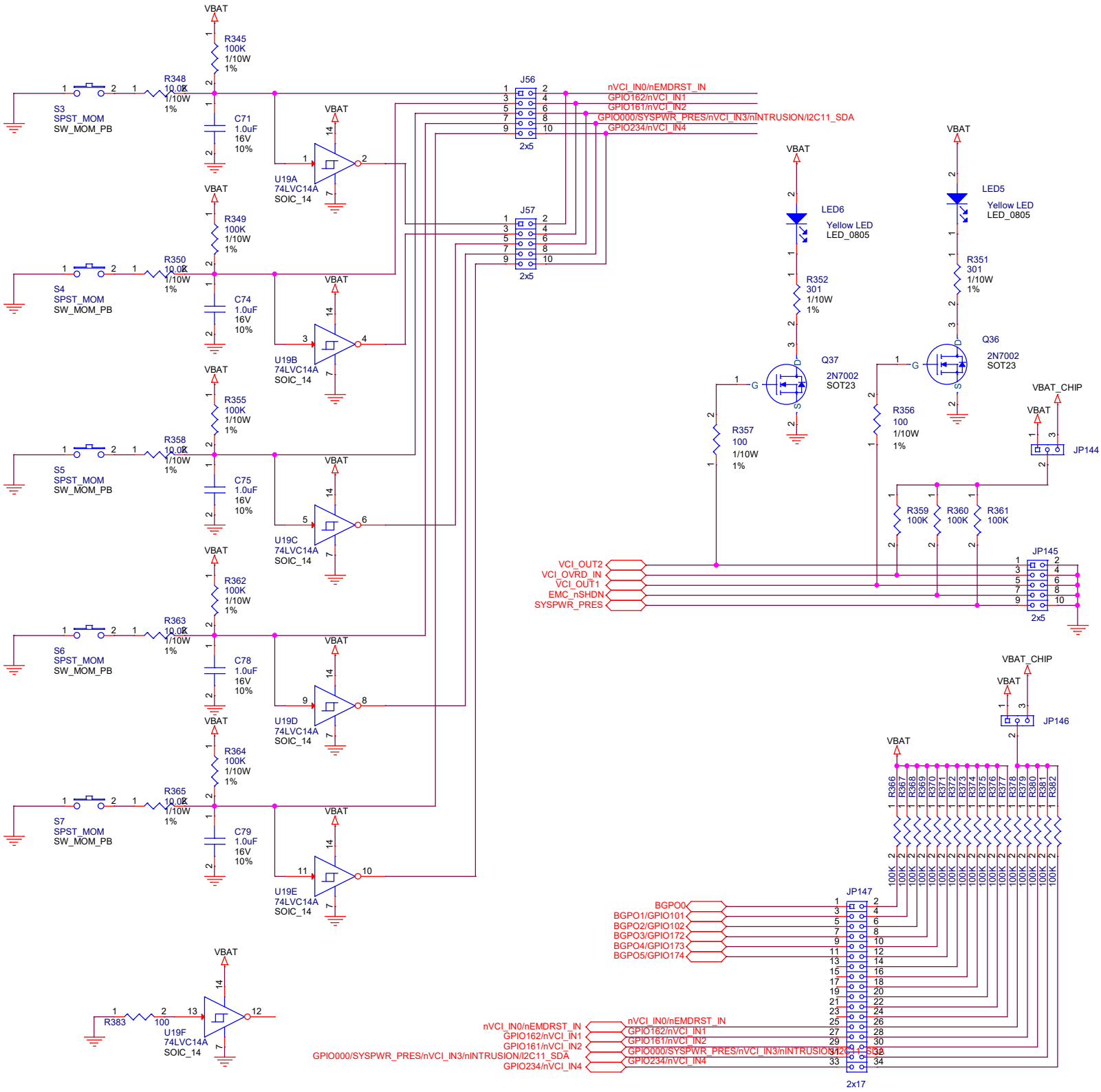
3.3V to 5.0V Boost Regulator

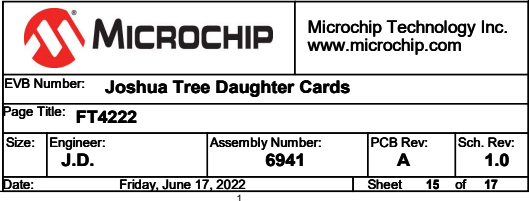


PS2 Interface

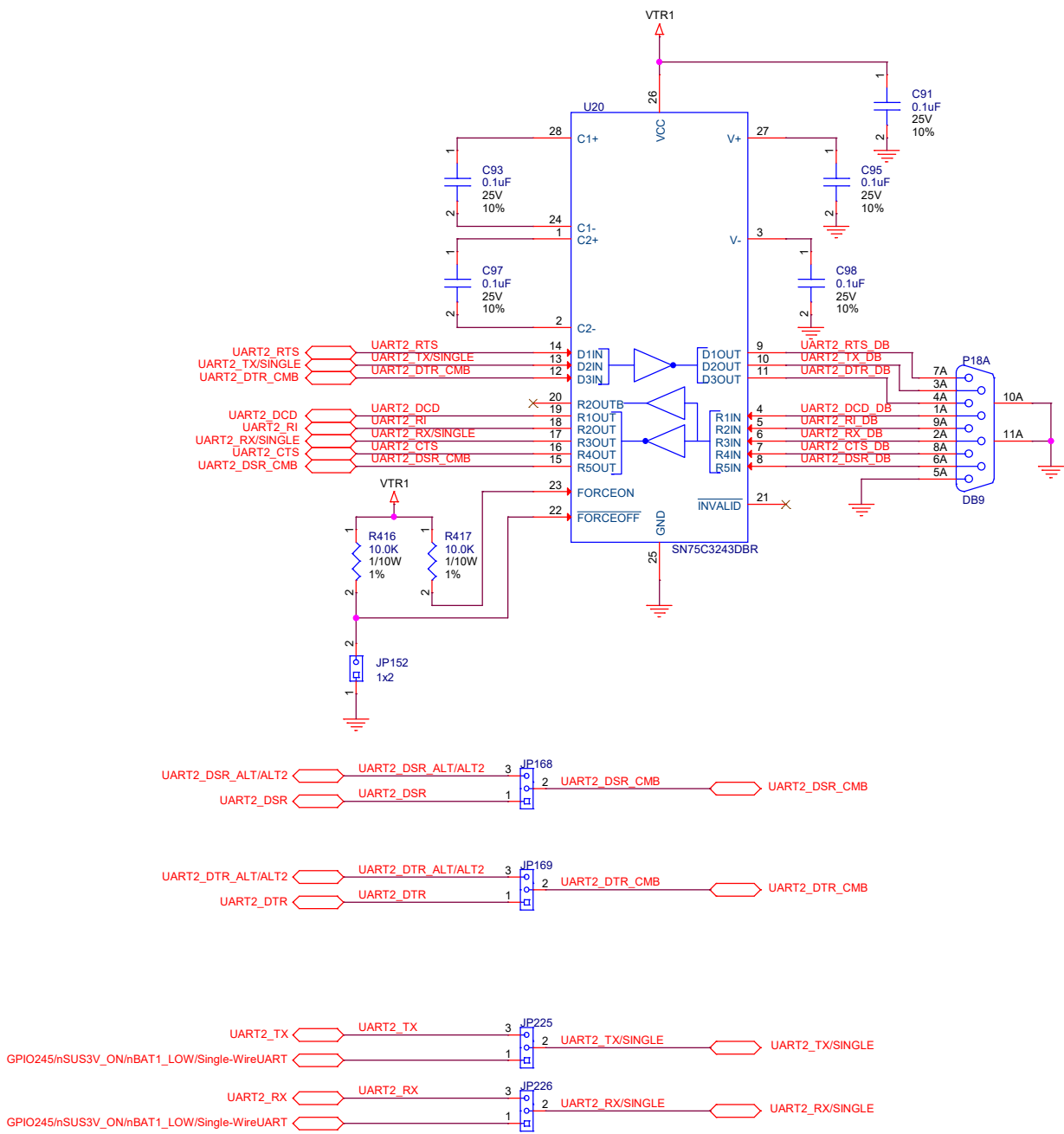


VCI Interface / Battery Well Glue logic





UART2



UART3

