

CARLSBAD EVB

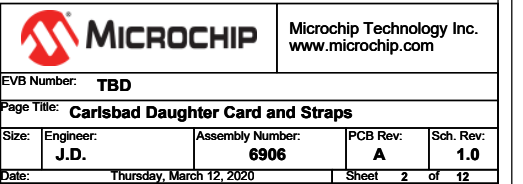
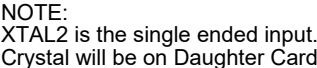
BLOCK DIAGRAM

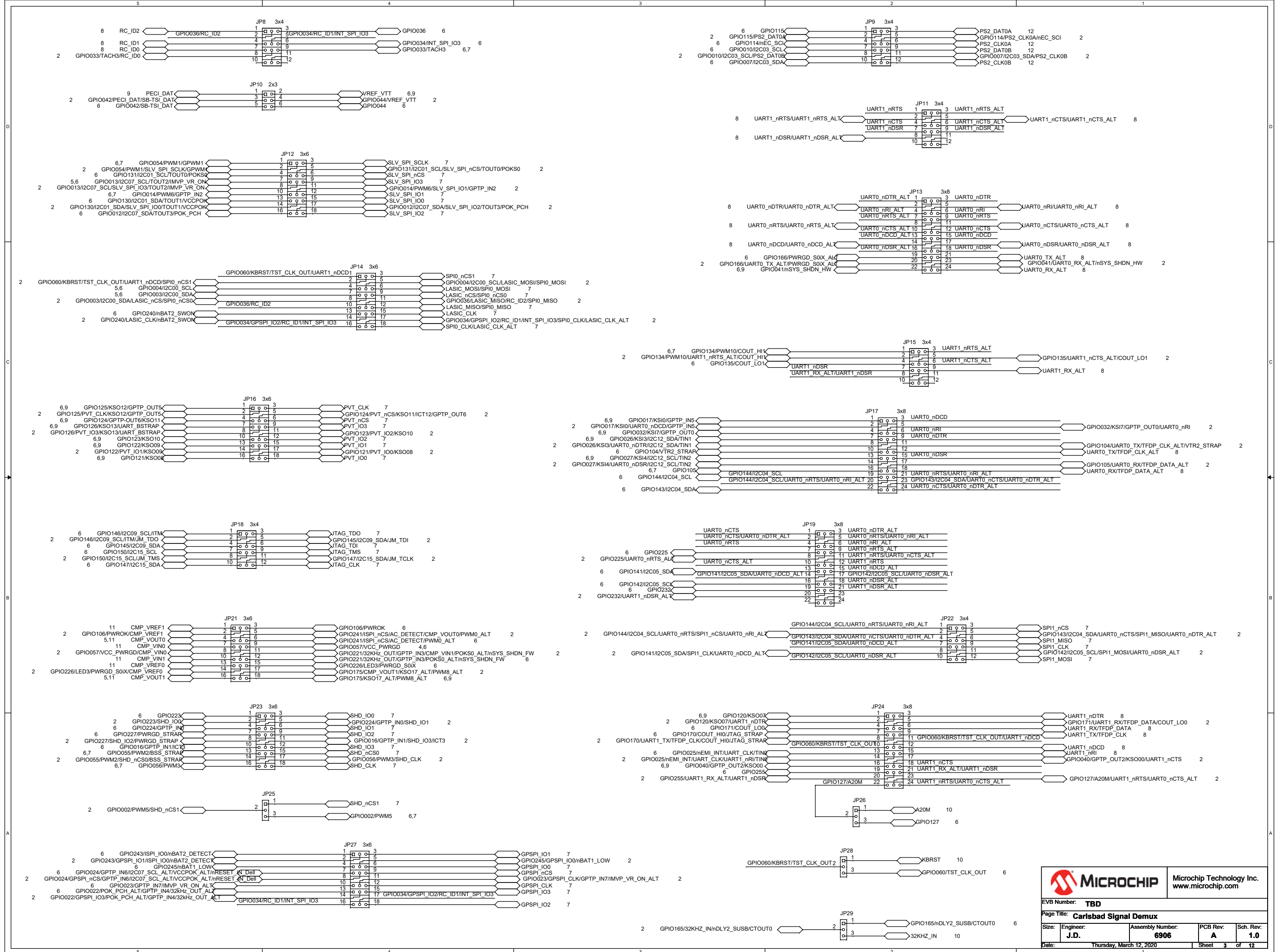
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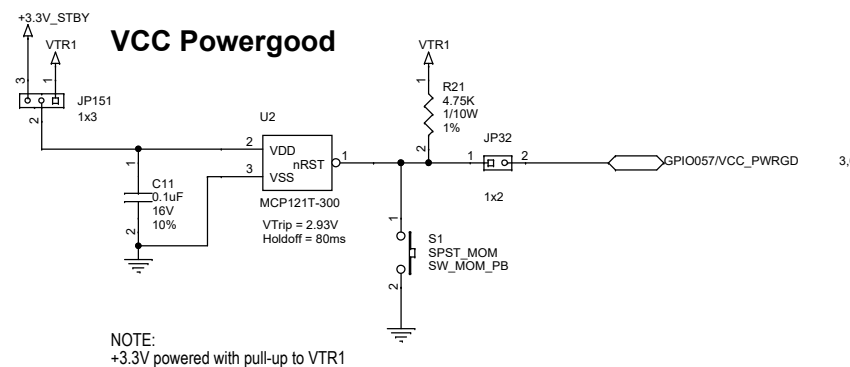
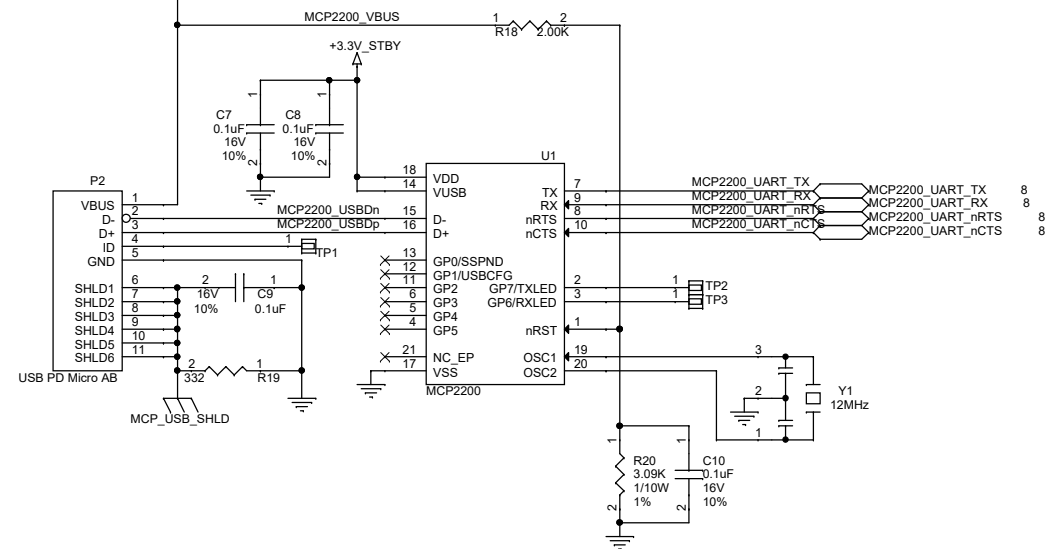
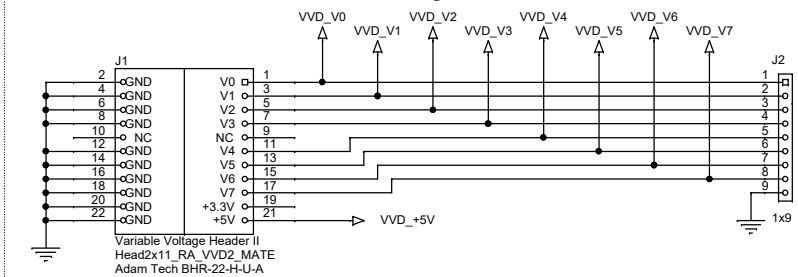
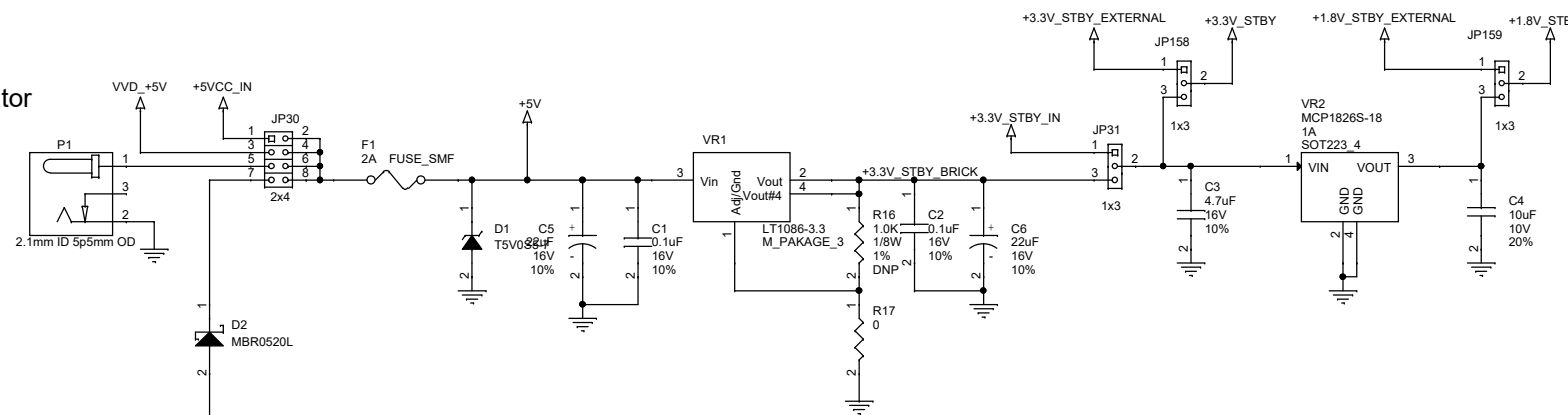
Revision History

Rev 1.0:
Initial Release

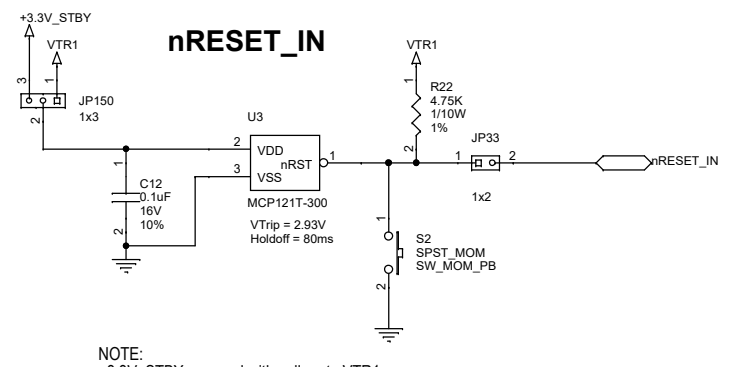
Rev 1.1:





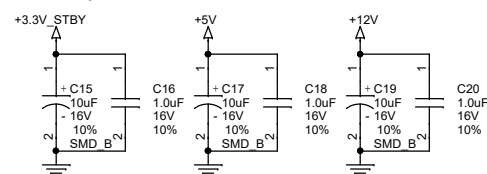


NOTE:
+3.3V powered with pull-up to VTR1

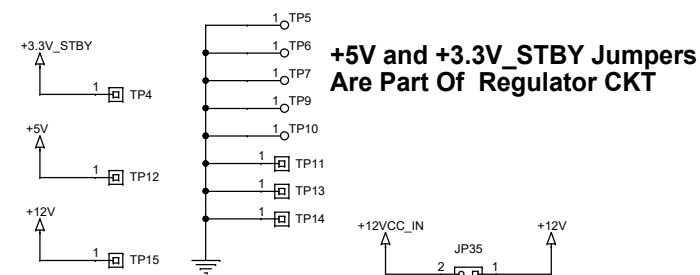


NOTE:
+3.3V_STBY powered with pull-up to VTR1

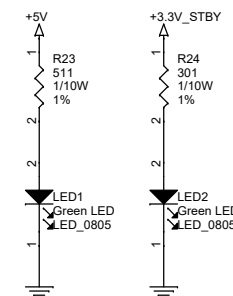
General Board Capacitors



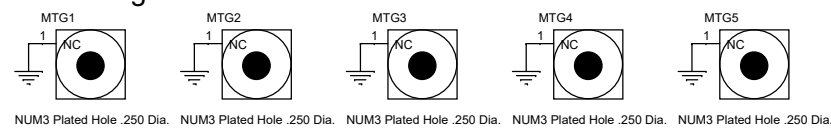
Test Points



Power LEDs



Mounting Holes



I2C Pullups
on Dongle

J3

+3.3V_STBY

V_I2C_EXTERNAL

V_CTRL_ALWAYS

R41

10.0K

1/10W

1%

R42

10.0K

1/10W

1%

R43

10.0K

1/10W

1%

JP53

2x3

EXTERNAL_SCLK

EXTERNAL_SDATA

22

23

SCL

SDA

INT-

I/O_0

I/O_1

I/O_2

I/O_3

I/O_4

I/O_5

I/O_6

I/O_7

I/O_8

I/O_9

I/O_10

I/O_11

I/O_12

I/O_13

I/O_14

I/O_15

I/O_16

I/O_17

GND

PHILIPS - PCA9555PW

TSSOP24

EXTERNAL_SCLK

EXTERNAL_SDATA

11

11

GPIO004/I2C00_SCL

GPIO003/I2C00_SDA

3,6

3,6

2x2

JP58

2

4

2x2

1

3

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4

2x2

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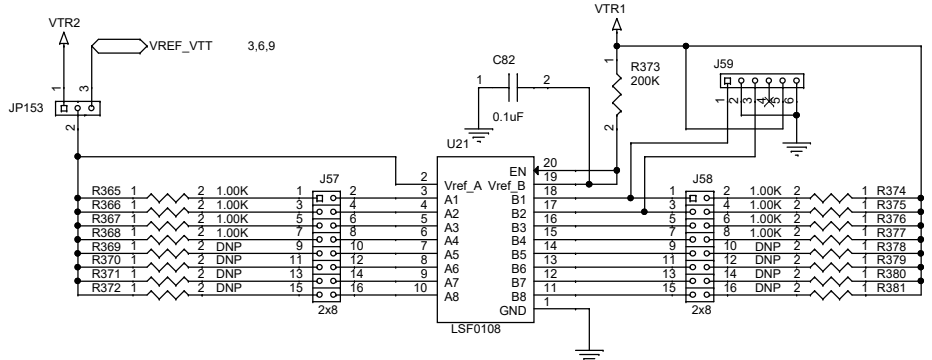
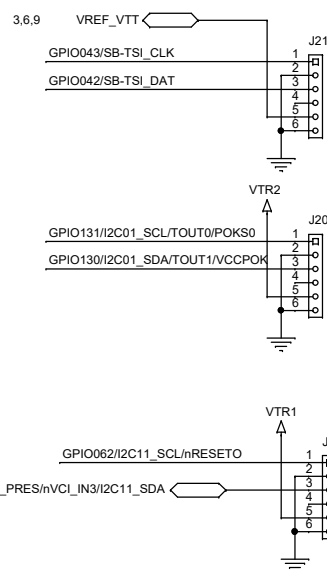
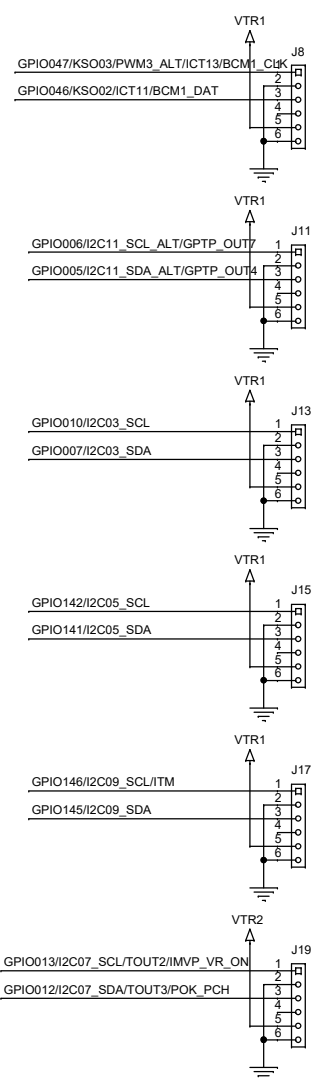
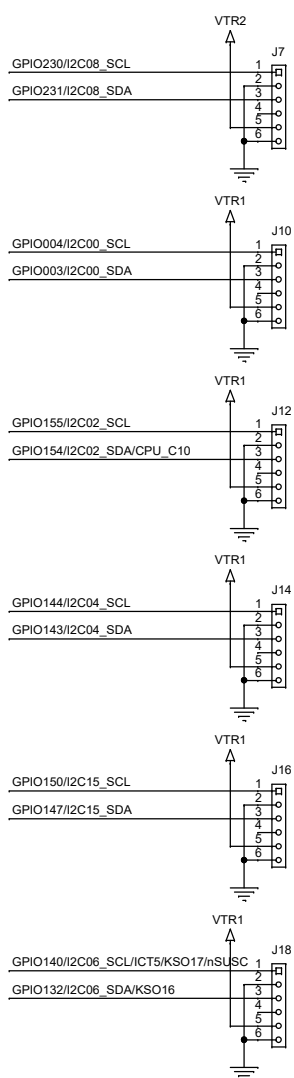
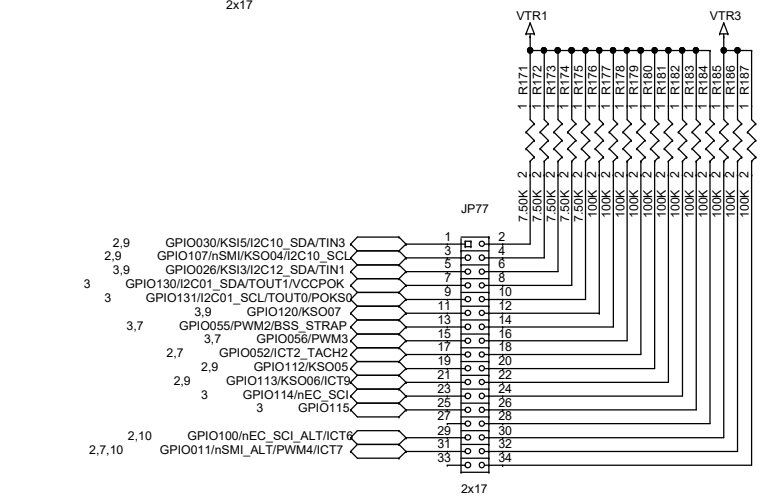
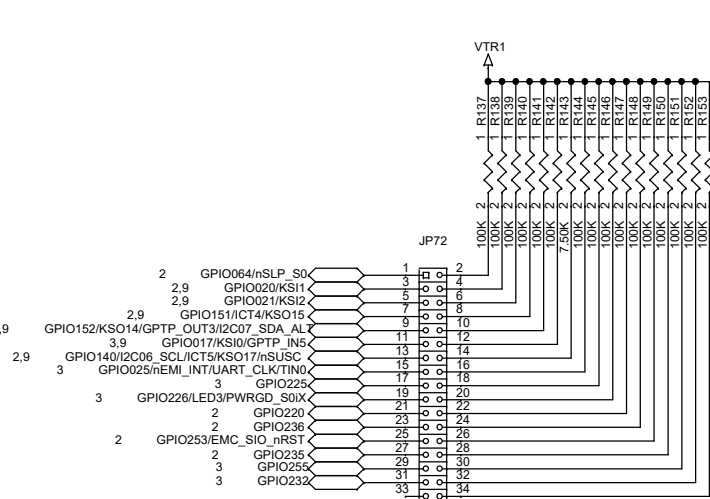
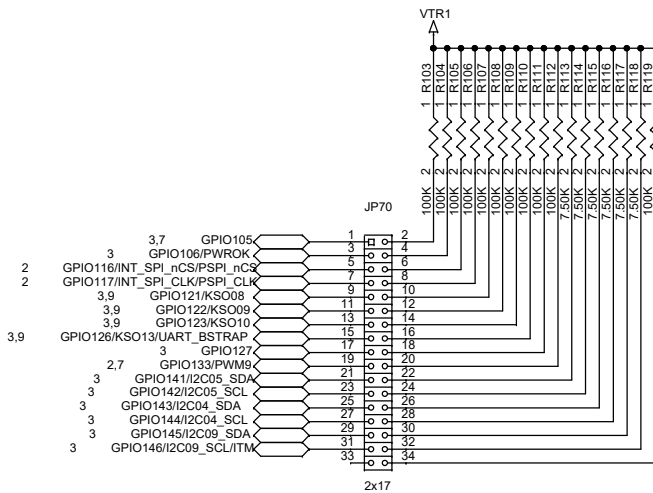
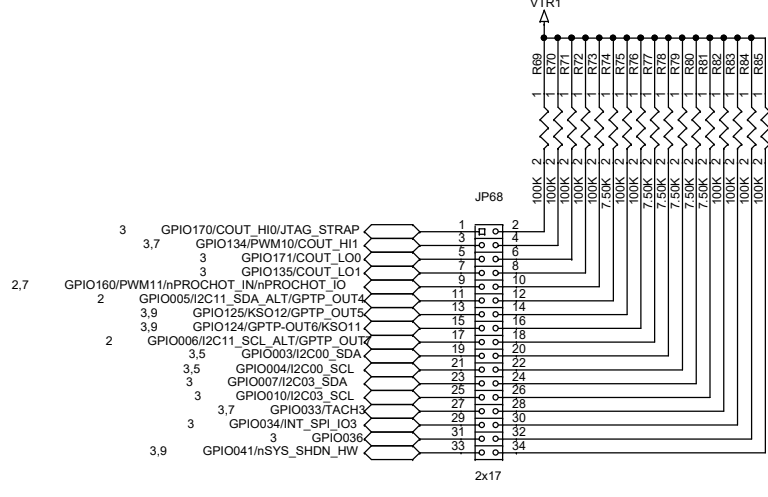
1

3

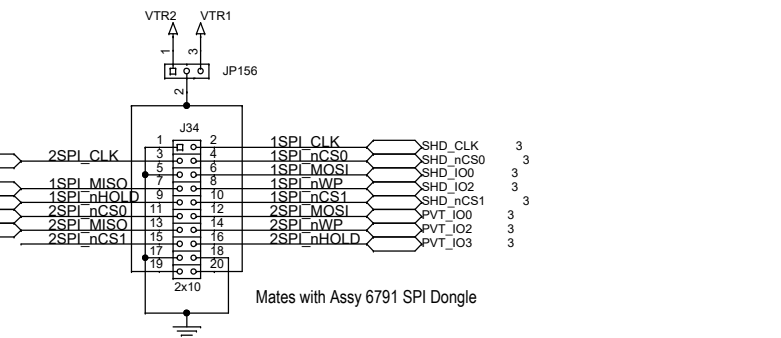
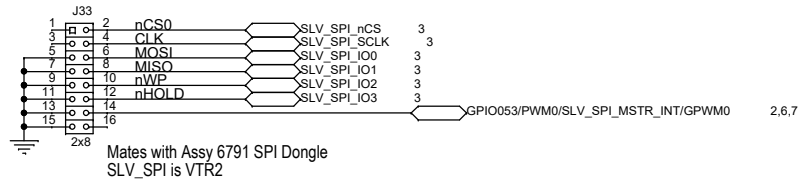
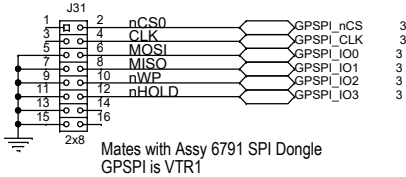
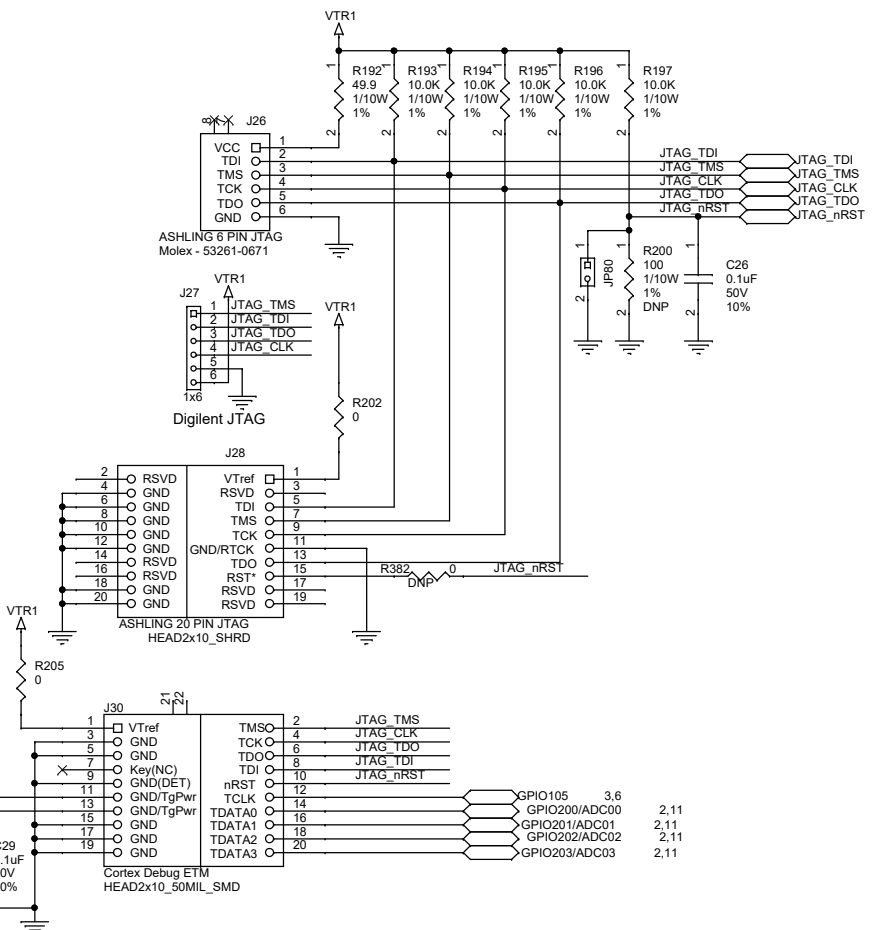
2

4

2x2

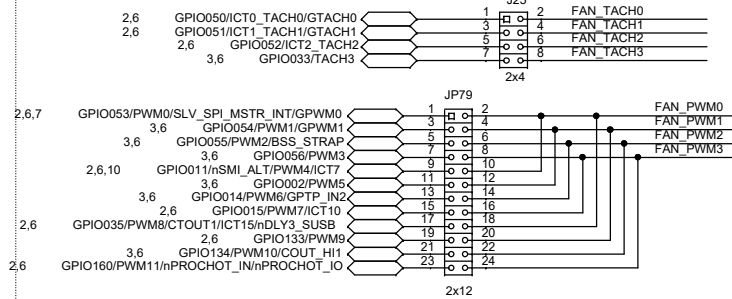


JTAG and Debug



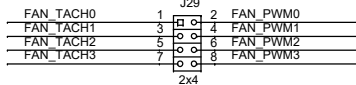
NOTE:
SHD SPI is VTR2; PVT SPI is VTR1
For proper operation, set VTR1 & VTR2 to the same voltage.

FAN and TACH Headers

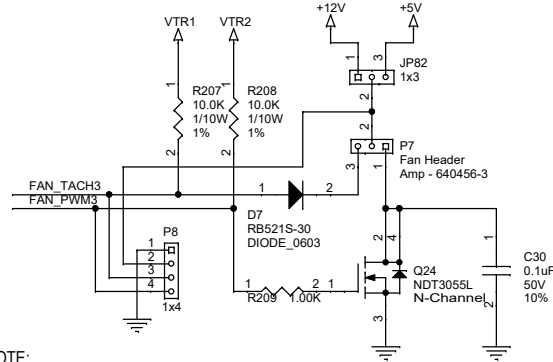


NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V

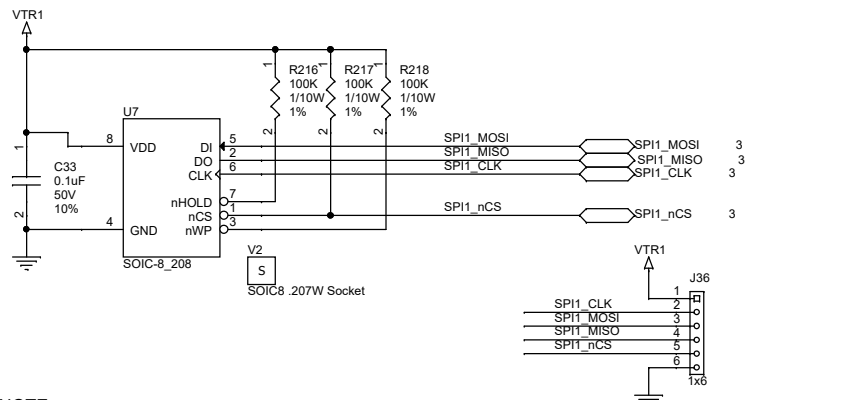
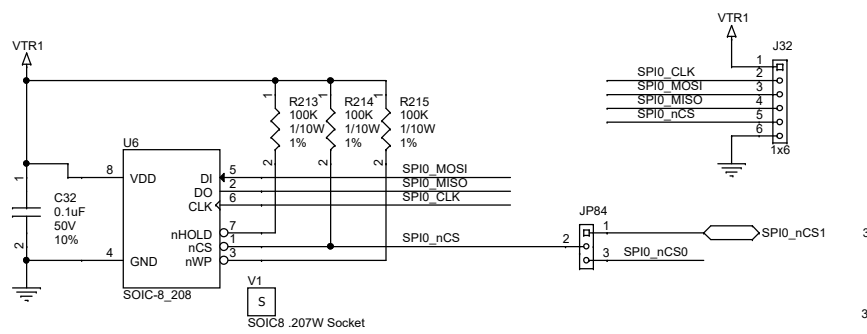
FAN and TACH Loopback



FAN3

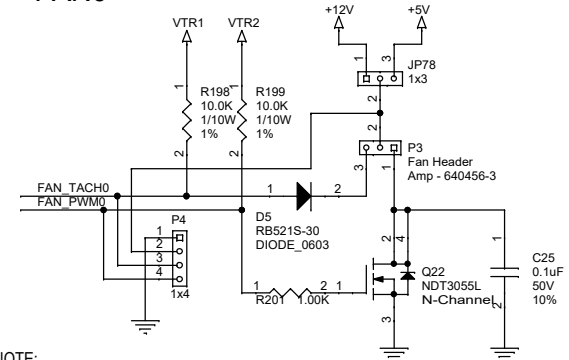


NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V



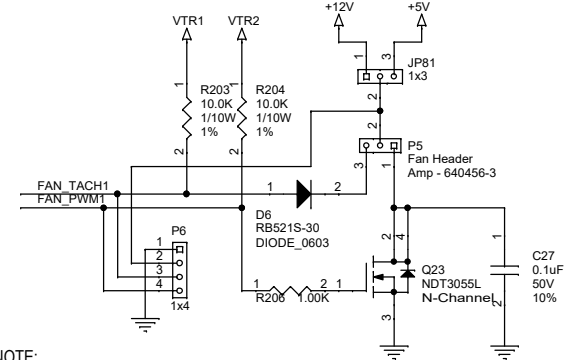
NOTE:  These SPI interfaces go to a SOIC8 socket so that +3.3V or +1.8V parts can be used.

FANO



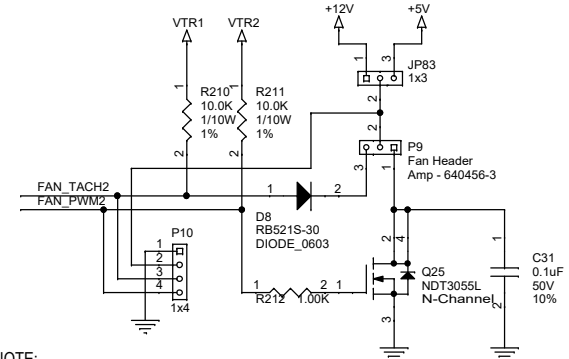
NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V

FAN1

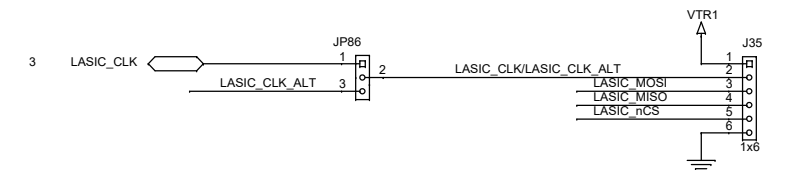
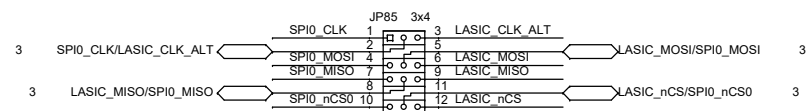


NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V

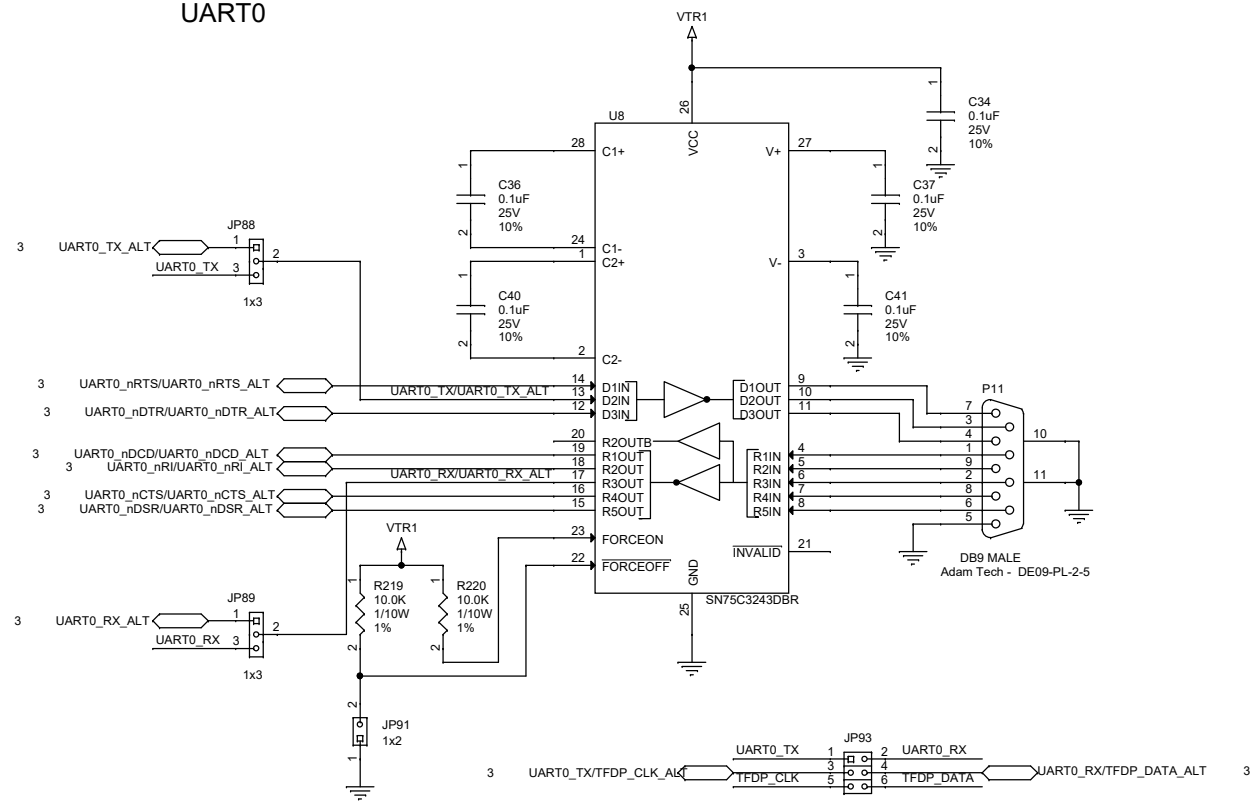
FAN2



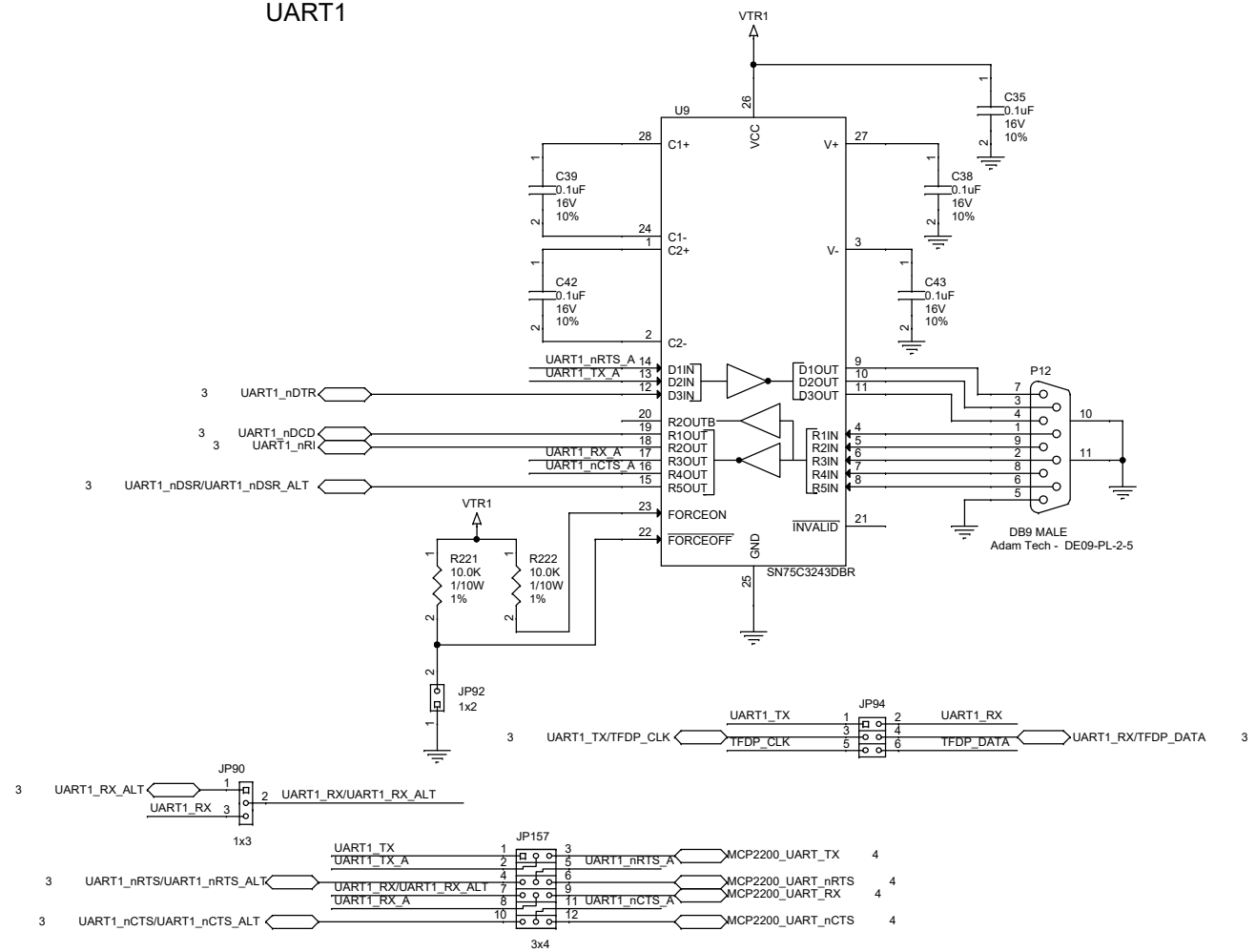
NOTE:
The PWM and TACH pins are a mix of VTR1 & VTR2.
For proper operation, set VTR1 & VTR2 to +3.3V



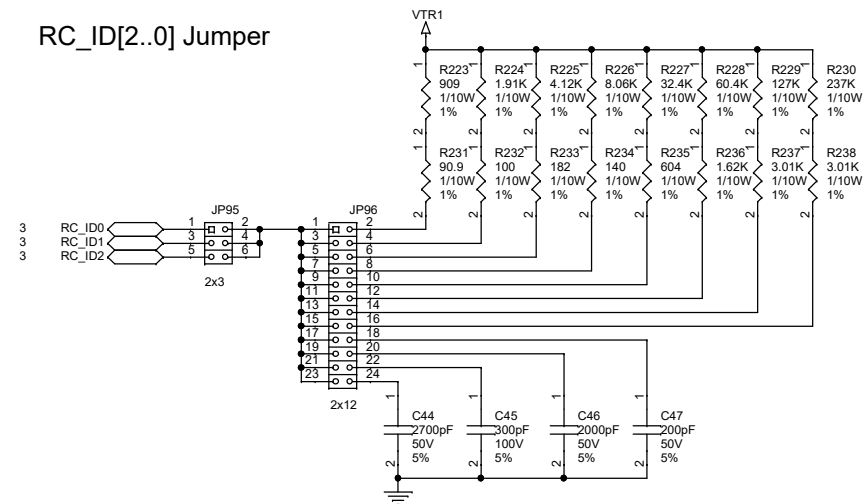
UART0



UART1



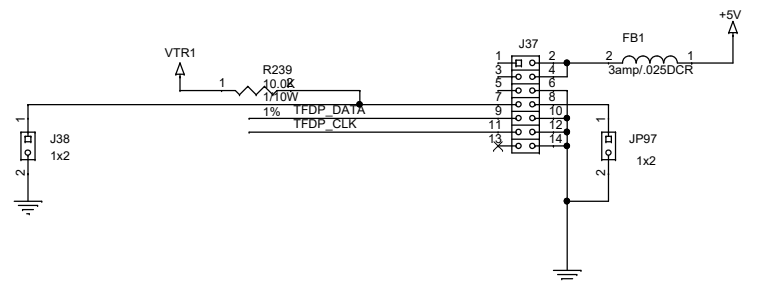
RC_ID[2..0] Jumper



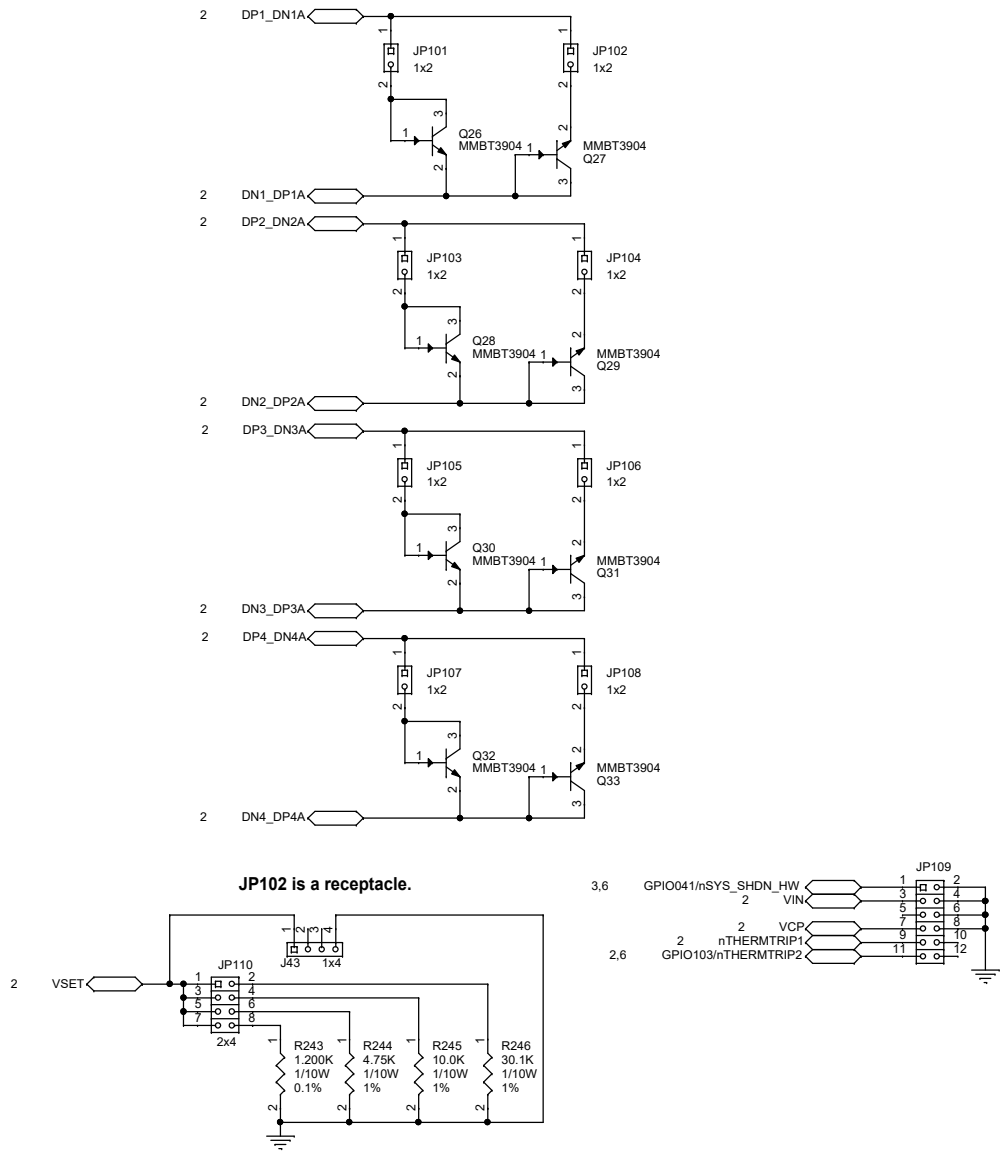
NOTE:
If VTR1 is supplied with 1.8V, the RC_ID logic will not function correctly.
VTR1 must be connected to a +3.3V supply for the RC_ID block to operate.

Software Developers Debug Interface

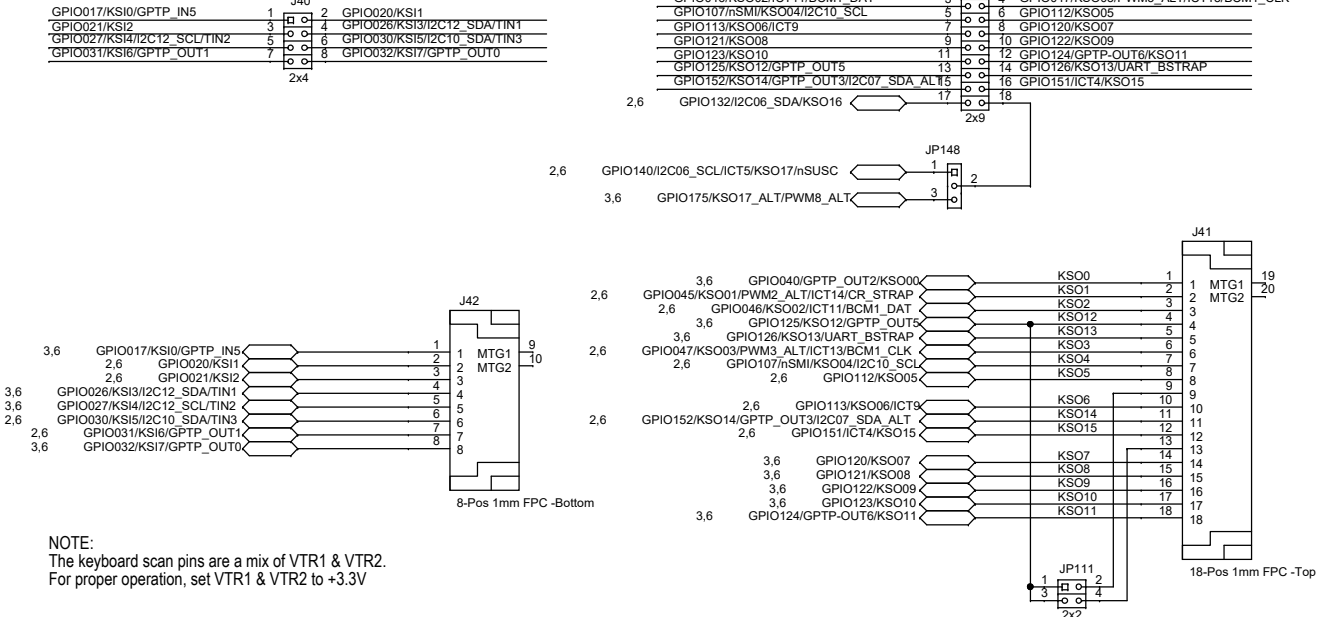
Mates with: Trace FIFO Board (Assy 6227)
Pegasus Debugger (Assy 6345)



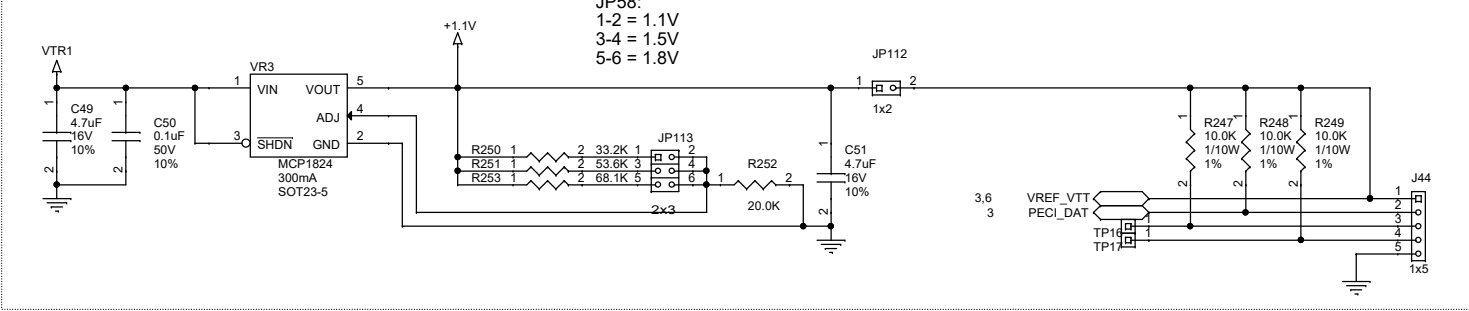
Remote Temperature Monitoring

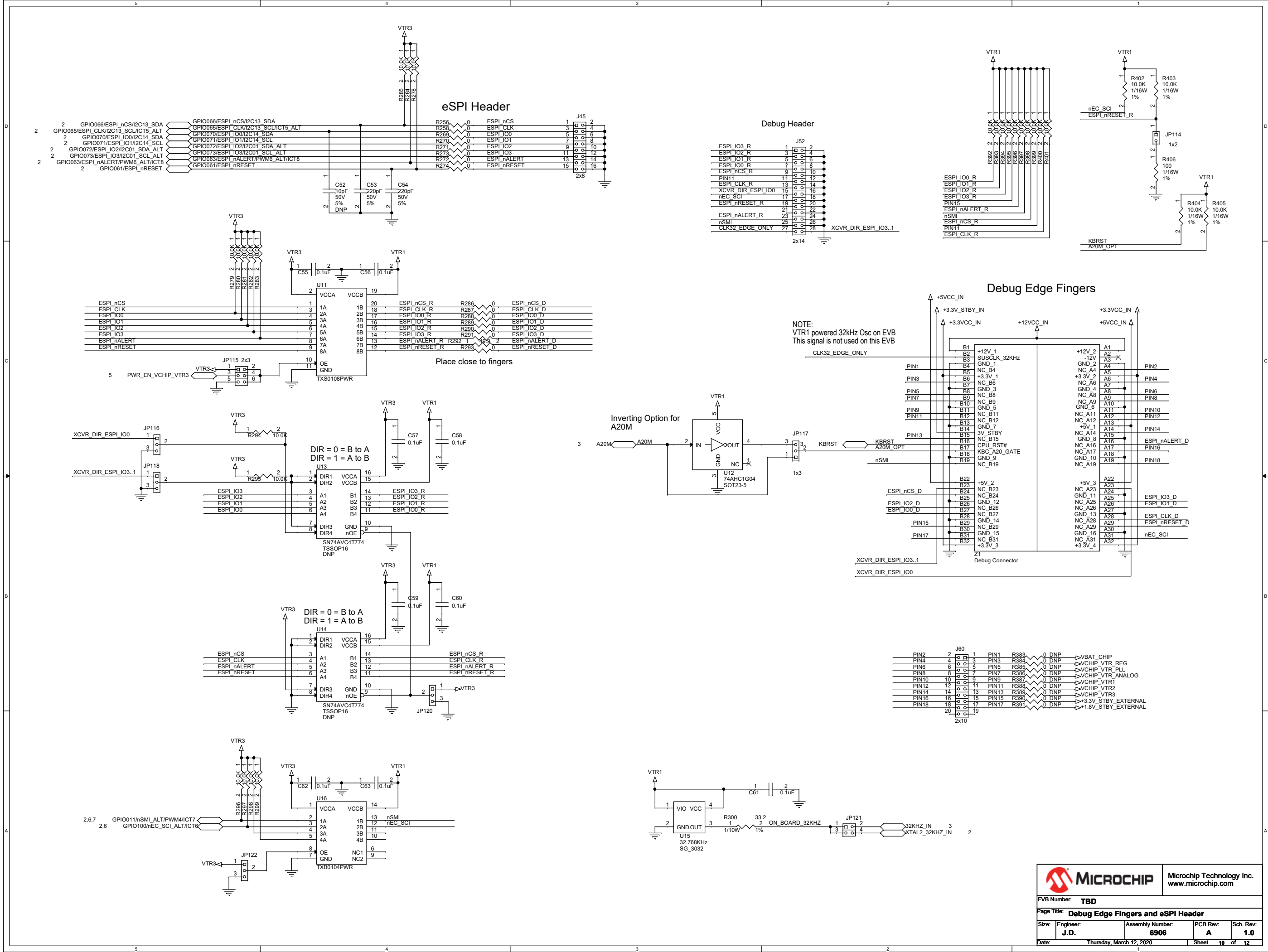


Keyboard Interface

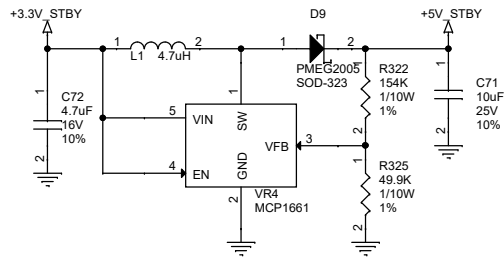


PECI Interface

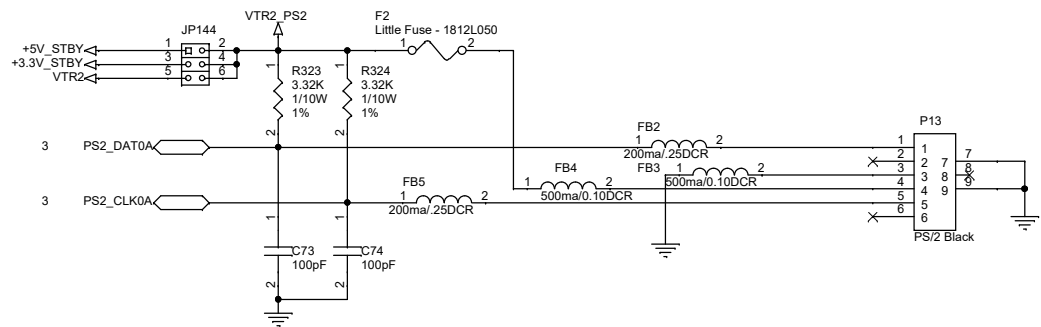




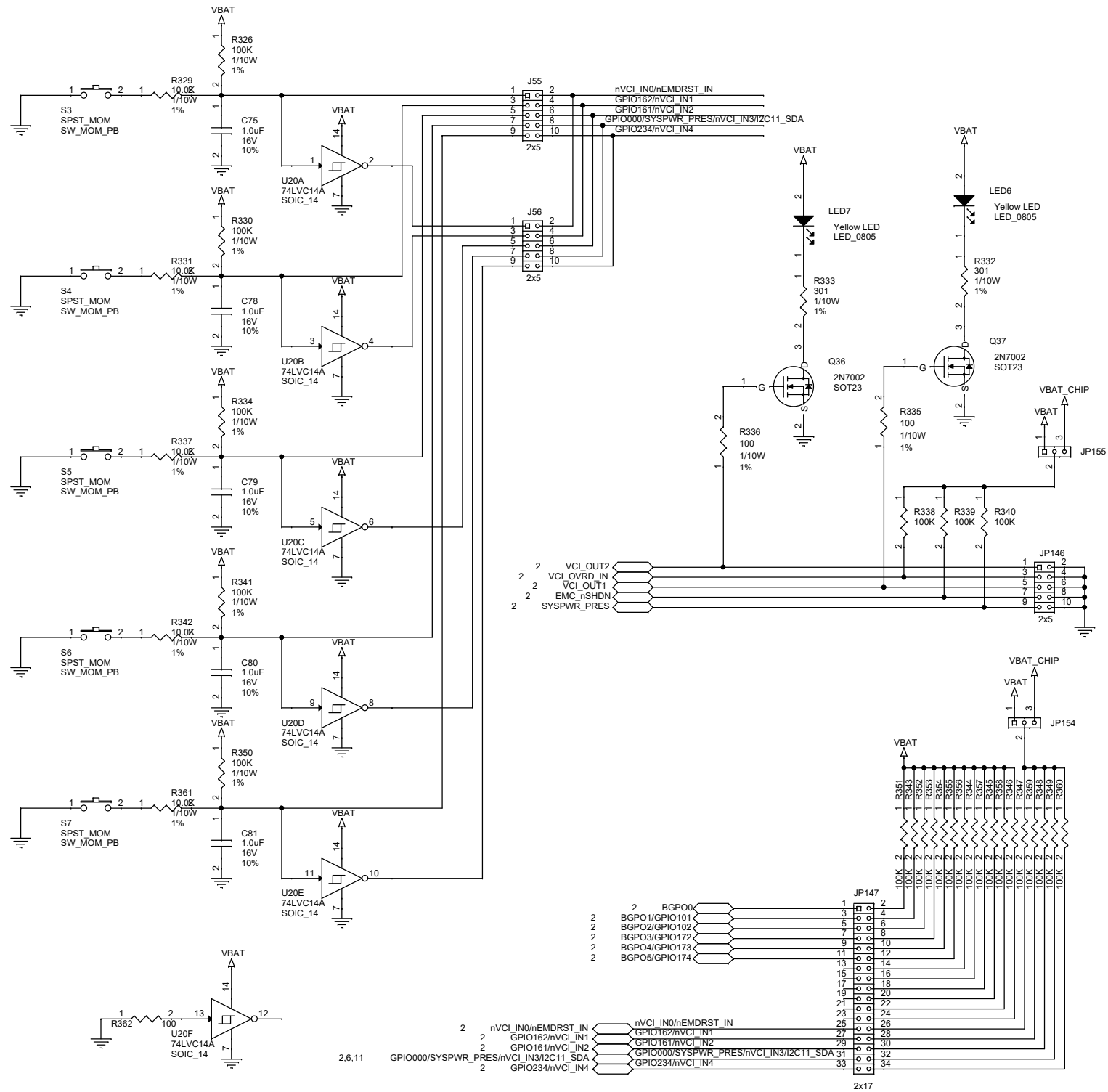
3.3V to 5.0V Boost Regulator



PS2 Interface



VCI Interface / Battery Well Glue logic



NOTE:
For proper operation, set VTR1 to +3.3V

