MEC174X

Embedded Controller for Notebook PC

Operating Conditions

- Operating Voltages: 3.3 V and 1.8 V
- Operating Temperature Range: -40 °C to 85°C

Low Power Modes

- Chip is designed to always operate in Lowest Power state during Normal Operation
- Supports all 5 ACPI Power States for PC platforms
- Supports 2 Chip-level Sleep Modes: Light Sleep and Heavy Sleep
  - Low Standby Current in Sleep Modes
- Supports Modern Standby

ARM® Cortex-M4F Embedded Processor

- Programmable clock frequency up to 96 MHz
- Floating Point Unit (FPU) processor
- Single 4GByte Addressing Space
- Nested Vectored Interrupt Controller (NVIC)
  - Maskable Interrupt Controller
  - Maskable hardware wake up events
  - 8 Levels of priority, individually assignable by vector
- EC Interrupt Aggregator expands number of Interrupt sources supported or reduces number of vectors needed
- Complete ARM® Standard debug support
  - JTAG-Based DAP port, comprised of SWJ-DP and AHB-AP debugger access functions
- Memory Protection Unit (MPU) support

Memory Components

- Code and Data SRAM options
  - 448 KB (Code: 384KB; Data: 64 KB)
- 128 Bytes Battery Powered SRAM
- 4 K bits user programmable OTP
  - Lockable on 32 Bytes boundaries to prevent read access or write access
  - In circuit programmable
- ROM
  - Contains Boot ROM
  - Contains Runtime APIs for built-in functions
- Optional internal EEPROM or internal SPI
  - Size TBD

Clocks

- 96 MHz Internal PLL
- 32 kHz Clock Sources
  - Internal 32 kHz silicon oscillator (+/-2%)
  - External 32 kHz crystal (XTAL) source
  - External single-ended 32 kHz clock source
- 32kHz Clock Monitor
  - XTAL clock health check

Package Options

- 176 WFBGA 10x10 Body 0.65 Ball Pitch

Security Features

- Boot ROM Secure Boot Loader
  - Supports 2 Code Images in external SPI Flash (Primary and Fall-back image)
  - Authenticates SPI Flash image before loading
  - Support AES-256 Encrypted SPI Flash images
  - Supports Signed and Unsigned Code Images
  - Key Revocation - 5 Keys
  - Code Rollback Protection - 127
  - Firmware ID Support
  - Chip Unique Identifier
  - Native SPI Encryption API using Chip Unique Identifier Stored in OTP
    - Includes anti-replay protection for data stored by the EC in the SPI. This emulates EC NVRAM variable storage.
- Hardware Accelerators:
  - Multi purpose AES Crypto Engine:
    - Support for 128-bit - 256-bit key length
    - Supports Battery Authentication applications
  - Digital Signature Algorithm Support
    - Support for ECDSA and EC-KCDSA
  - Cryptographic Hash Engine
    - Support for SHA-1, SHA-256 to SHA-512
  - Public Key Crypto Engine
    - Hardware support for RSA and Elliptic Curve asymmetric public key algorithms
    - RSA keys length of 1024 to 4096 bits
    - ECC Prime Field keys up to 571 bits
    - ECC Binary Field keys up to 571 bits
    - Microcoded support for standard public key algorithms
- Optional PUF Memory

- OTP for storing Keys and IDs
- Non Deterministic Random Number Generator
  - Includes conditioning and health test
  - 1K bit FIFO
- JTAG Disabled by default

System Host interface

- Enhanced Serial Peripheral Interface (eSPI)
  - Intel eSPI Specification compliant
    - eSPI Interface Base Spec, Intel Doc. #327432-004, Rev. 1.0.
    - eSPI Compatibility Spec, Intel Doc. #562633, Rev. 0.6
  - Support for Master Attached Flash Sharing (MAFS)
  - Support for Slave Attached Flash Sharing (SAFS)
  - Supports all four channels:
    - Peripheral Channel
    - Virtual Wires Channel
    - Out-of-Band (OOB) Tunneled Message Channel
    - Run-time Flash Access Channel
  - Supports EC Bus Master to Host Memory
  - Supports up to 66 MHz maximum operating frequency
  - Supports DnX feature
  - Supports RPMC feature enhancements.
    - New RPMC registers.
    - Supports ERPMC in software.
- One Serial Peripheral Interface (SPI) Slave
  - Quad SPI (half-duplex) or Single wire (full duplex) support
  - Mode 0 and Mode 3 operation
  - Programmable wait time for response delay
- System to EC Message Interface
  - Up to Three Embedded Memory Interfaces
    - Provides Two Windows to On-Chip SRAM for Host Access
    - Two Register Mailbox Command Interface
  - Mailbox Registers Interface
    - Thirty-two 8-bit registers
    - Two Register Mailbox Command Interfaces
    - Two Register SMI Source Interfaces
  - Five ACPI Embedded Controller Interfaces
    - Four EC Interfaces
    - One Power Management Interface
- One Serial Peripheral Interface (SPI) Master Controller
  - Dual and Quad I/O Support
  - Flexible Clock Rates
  - Support for 1.8V and 3.3V slave devices
  - SPI Burst Capable
  - SPI Controller Operates with Internal DMA Controller with CRC Generation
  - Mappable to the following ports (only 1 port active at a time)
    - 1 shared SPI Interface
    - 1 General purpose SPI
    - 1 Private SPI Interface
- Two General Purpose Serial Peripheral Interface Controllers (ECGP-SPI)
  - One 3-pin EC-driven Full Duplex Serial Communication Interface
  - Flexible Clock Rates
  - SPI Burst Capable
- 8042 Emulated Keyboard Controller
  - 8042 Style Host Interface
  - Port 92 Legacy A20M Support
- Fast GATEA20 & Fast CPU_RESET
- PECI Interface 3.1
  - Support Intel's low voltage PECI
- Port 80 BIOS Debug Port
  - Two Ports, Assignable to Any eSPI IO Address
  - 24-bit Timestamp with Adjustable Timebase
  - 16-Entry FIFO
  - 32 bit Port 80 support
  - Output Port 80 over UART

Peripheral Features

- Internal DMA Controller
  - Hardware or Firmware Flow Control
  - Firmware Initiated Memory-to-Memory transfers
  - Hardware CRC-32 Generator on Channel 0
  - 16-Hardware DMA Channels Support Five SMBus Master/Slave Controllers and One SPI Controller
- I2C/SMBus Controllers
  - Five I2C/SMBus controllers
  - Up to 16 Configurable I2C ports
    - Full Crossbar switch allows any port to be connected to any controller
  - Supports Promiscuous mode of operation
  - Fully Operational on Standby Power
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
  - 1 MHz Capable
  - Supports DMA Network Layer
- I3C Controllers
  - One I3C Host with HCI 1.1 port
  - One I3C Debug Target port support with UART Network Adapter.
- General Purpose I/O Pins

  - Inputs
    - Asynchronous rising and falling edge wakeup detection Interrupt High or Low Level
  - Outputs:
    - Push Pull or Open Drain output
    - Programmable power well emulation
  - Pull up or pull down resistor control
    - Automatically disabling pull-up resistors when output driven low
    - Automatically disabling pull-down resistors when output driven high
  - Programmable drive strength
  - Two separate1.8V/3.3V configurable IO regions
  - Group or individual control of GPIO data
  - 12- Over voltage tolerant GPIO pins
  - Glitch protection and Under-Voltage Protection on all GPIO pins
  - 8 GPIO Pass-Through Port (GPTP)
- Input Capture and Compare timer
  - Six 32-bit Capture Registers
  - 16 Input Pins (ICT[15:0])
    - Full Crossbar switch allows any port to be connected to any controller
  - 32-bit Free-running timer
  - Two 32-bit Compare Registers
  - Capture, Compare and Overflow Interrupts
- Universal Asynchronous Receiver Transmitter (UART)
  - Two High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
    - Up to 4 configurable 8 Pin UARTs in 176 pin package
  - Programmable Main Power or Standby Power Functionality
  - Standard Baud Rates to 115.2 Kbps, Custom Baud Rates to 1.5 Mbps
- Programmable Timer Interface
  - Four 16-bit Auto-reloading Timer Instances
    - 16 bit Pre-Scale divider
    - Halt and Reload control
    - Auto Reload
  - Two 32-bit Auto-reloading Timer Instances
    - 16 bit Pre-Scale divider
    - Halt and Reload control
    - Auto Reload
  - Three Operating Modes per Instance: Timer (Reload or Free-Running) or One-shot.
    - Event Mode is not supported
- 32-bit RTOS Timer
  - Runs Off 32kHz Clock Source
  - Continues Counting in all the Chip Sleep States regardless of Processor Sleep State
  - Counter is Halted when Embedded Controller is Halted (e.g. JTAG debugger active, break points)
  - Generates wake-capable interrupt event
- Watch Dog Timer (WDT)
  - Watchdog reset IRQ vector
- Integrated Standby Power Reset Generator (Embedded RESET Engine)
  - Reset Output Pin
- Up to 12 Programmable Pulse Width Modulator (PWM) outputs
  - Multiple Clock Rates
  - 16-Bit ON & 16-Bit OFF Counters
- Up to 4 Fan Tachometer Inputs
  - 16 Bit Resolution
- Two RPM-Based Fan Speed Controllers
  - Each includes one Tach input and one PWM output
  - 3% accurate from 500 RPM to 16k RPM
  - Automatic Tachometer feedback
  - Aging Fan or Invalid Drive Detection
  - Spin Up Routine
  - Ramp Rate Control
  - RPM-based Fan Speed Control Algorithm
- Breathing LED Interface
  - Four Blinking/Breathing LEDs
  - Programmable Blink Rates
  - Piecewise Linear Breathing LED Output Controller
    - Provides for programmable rise and fall waveforms
  - Operational in EC Sleep States
- PS2 Controller
  - Two PS2 controller
  - Three PS2 ports
  - 5 volt tolerant
  - Analog Features
- ADC Interface
  - 10-bit or 12-bit readings supported
  - ADC Conversion time 800nS/channel
  - 16 Channels
  - External voltage reference
  - Supports thermistor temperature readings
    - Additional voltage reference for thermistor readings
- Two Analog Comparators
  - May be used for Hardware Shutdown
    - Detection of voltage limit event
    - Detection of Thermistor Over-Temp Event
- Microchip BC-Link Interconnection Bus
  - One Low Speed Bus Master Controller
- Three Resistor/Capacitor Identification Detection (RC_ID) ports

  - Single Pin Interface to External Inexpensive RC Circuit
  - Replacement for Multiple GPIOs
  - Provides 8 Quantized States on One Pin

Battery Powered Peripherals

- Real Time Clock (RTC)
  - VBAT Powered
  - 32KHz Crystal Oscillator or External single-ended 32 kHz clock source
  - Time-of-Day and Calendar Registers
  - Programmable Alarms
  - Supports Leap Year and Daylight Savings Time
- Hibernation Timer Interface
  - Two 32.768 KHz Driven Timers
  - Programmable Wake-up from 0.5ms to 128 Minutes
- Week Timer
  - System Power Present Input Pin
    - Week Alarm Event only generated when System Power is Available
  - Power-up Event
  - Week Alarm Interrupt with 1 Second to 8.5 Year Time-out
  - Sub-Week Alarm Interrupt with 0.50 Seconds - 72.67 hours time-out
  - 1 Second and Sub-second Interrupts
- VBAT-Powered Control Interface (VCI)
  - 64 Active-low VCI Inputs
    - VCI_IN0# Dedicated Pin - always enabled
    - VCI_IN[1:4]# MUX with GPIO - default off
  - 1 dedicated VCI_OVRD_IN Pin - always enabled
  - 1 Active-high VCI Input Pin
  - 1 Active-high VCI Output Pin
  - System Power Present Detection for gating RTC wake events
  - Optional filter and latching
- Up to six Battery-Powered General Purpose Output (BGPO) Pins
  - 1 Dedicated - BGPO0
  - Up to 5 muxed with VTR Powered GPIO pins

Debug Features

- 2-pin Serial Wire Debug (SWD) interface
  - SWD I/F debugger and programmer
- 4-Pin JTAG interface for Boundary Scan
- Trace FIFO Debug Port (TFDP)

Additional Features

- Support multiple RPMC channel over eSPI.
- Support Power pins that move from 3.3V to 1.8V.
- Support Life cycle feature of chip.
- User OTP size increased to 4K bits.

Additional Features Under Investigation

- Add SPI Flash anti Tamper feature
  - Only monitors CS during run-time
  - G3 - attempt to GND the SPI pins at EC
  - Allow external programming of SPI when EC is held in reset or debug authorization
  - Validate the SPI at every POR
  - SPI pins are backdrive protected and allows external SPI programming
- OTP Life Cycle- change of ownership / refurbish process.

TABLE 1: MEC174X FEATURE LIST

Feature	MEC1743 MEC1747	MEC1747
Package	144 WFBGA	176 WFBGA
Total SRAM	480 KB	448 KB
SRAM Code/Data (Primary use)	448KB/64KB	384KB/64KB
Battery Backed SRAM	128 bytes	128 bytes
Optional EEPROM	8K Bytes in MEC1743	TBD Bytes
Optional Internal SPI Provision	512K Bytes in MEC1747	512KB Bytes
eSPI Host Interface	Yes	Yes
eSPI SAF Interface	Yes	Yes
RPMC	Yes	Yes
Environment Monitor Controller (EMC)	No	No
PowerGuard (Without EMC)	2	2
Embedded Memory Interface (EMI)	3	3
Mailbox Register Interface	1	1
ACPI Embedded Memory Controller	5	5
ACPI PM1 Block Interface	1	1
8042 Emulated Keyboard Controller	Yes	Yes
Trace FIFO Debug Port	Yes	Yes
Internal DMA Channels	16	16
16-bit Timer	4	4
32-bit Timer	2	2
16-bit Counter Timer	4	4
Capture Timer	6	6
Compare Timer	2	2
ICT Channels	16	16
Watchdog Timer (WDT)	1	1
Hibernation Timer	2	2
Week Timer	1	1
Sub Week Timer	1	1
RTOS Timer	1	1
RTC	1	1
Battery-Powered General Purpose Output (BGPO) Dedicated	1	1
Battery-Powered General Purpose Output (BGPO) muxed with GPIO	2	5
Active Low VBAT-Powered Control Interface (VCI)	4	5
Active High VBAT-Powered Control Interface input	1	1
Active High VCI Output	1	1
Keyboard Matrix Scan Support	Yes	Yes
Port 80 BIOS Debug Port	2	2
I3C Host Controller	Yes	Yes
I3C Target Controller	Yes	Yes
SMB/I2C Host Controllers	5	5
SMB/I2C Ports	16	16
PS2 Controllers	2	2

TABLE 1: MEC174X FEATURE LIST (CONTINUED)

Feature	MEC1743 MEC1747	MEC1747
Package	144 WFBGA	176 WFBGA
PS2 Ports	3	3
PECI-3.1	Yes	Yes
Blinking/Breathing LED	4	4
GP-SPI Master Controller	2	2
QSPI Master Controller	1	1
10/12-bit ADC Channels	8	16
VREF-2 ADC	Yes	Yes
Analog Comparators	Yes	Yes
RPM to PWM Fan Controller	2	2
PWMs	12	12
TACHs	4	4
UARTs	3 UART0: up to 8-pin UART1: up to 8-pin UART2: up to 4-pin	4 UART0: up to 8-pin UART1: up to 8-pin UART2: up to 8-pin UART3: up to 4-pin
AES Hardware Support	128-256 bit	128-256 bit
SHA Hashing Support	SHA-1 to SHA-512	SHA-1 to SHA-512
Public Key Cryptography Support	RSA: 4K bit ECC: 571 bit	RSA: 4K bit ECC: 571 bit
Random Number Generator (TRNG) with Health test	1K bit FIFO	1K bit FIFO
GPIOs	129	155
Pass Through GPIOs	8	8
Over Voltage Protected Pads	12	12
32KHz Clock Monitor	Yes	Yes
BC-Link (Low Speed)	1	1
Optional Prochot Monitor Input Only	Yes	Yes
Optional Prochot Monitor IO	Yes	Yes
SYS_SHDN# Feature	1	1
2 pin SWD	Yes	Yes
4 pin JTAG	Yes	Yes
Boundary Scan	1	1
DRNG	Yes	Yes
Optional PUF Support	2K bit	2K bit
DPA Tamper	Yes	Yes
OTP - Total Size - In Circuit Programmable for User	4K bits for user	4K bits for user
Root Of Trust	Yes	Yes
Secure Boot	Yes	Yes
Immutable Code	Yes	Yes
Key Revocation	Yes	Yes
Max Key Revocation Support	5	5
Code Rollback Support	127	127
Firmware ID	1	1

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1.0 GENERAL DESCRIPTION

The device is a low power integrated embedded controller designed for Notebook PC applications. The chip is a highly-configurable, mixed-signal, advanced I/O controller. It contains a 32-bit ARM® Cortex-M4F processor core with closely-coupled memory for optimal code execution and data access. An internal ROM, embedded in the design, is used to store the power on/boot sequence and APIs available during run time. When VTR is applied to the device, the secure boot loader API is used to download the custom firmware image from the system's shared SPI Flash device, thereby allowing system designers to customize the device's behavior.

The chip device is directly powered by a minimum of two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on' and system power management functions. The MEC174x has two banks of I/O pins that are able to operate at either 3.3 V or 1.8 V. Operating at 1.8V allows the MEC174x to interface with the latest platform controller hubs and will lower the overall power consumed by the device. Whereas 3.3V allows this device to be integrated into legacy platforms that require 3.3V operation.

The host interface is the Intel® Enhanced Serial Peripheral Interface (eSPI). The eSPI Interface is a 1.8V interface that operates in single, double and quad I/O modes. The eSPI Interface supports all four eSPI channels: Peripheral Channel, Virtual Wires Channel, OOB Message Channel, and Run-time Flash Access Channel. The eSPI hardware Flash Access Channel is used by the Boot ROM to support Master Attached Flash Sharing (MAFS). In addition, the MEC174x has specially designed hardware to support Slave Attached Flash Sharing (SAFS). The eSPI SAFS Bridge imposes Region-Based Protection and Locking security feature, which limits access to certain regions of the flash to specific masters. There may be one or more masters (e.g., BIOS, ME, etc.) that will access the SAF via the eSPI interface. The ARM® Cortex-M4F processor is also considered a master, which will also have its access limited to EC only regions of SPI Flash as determined by the customer firmware application.

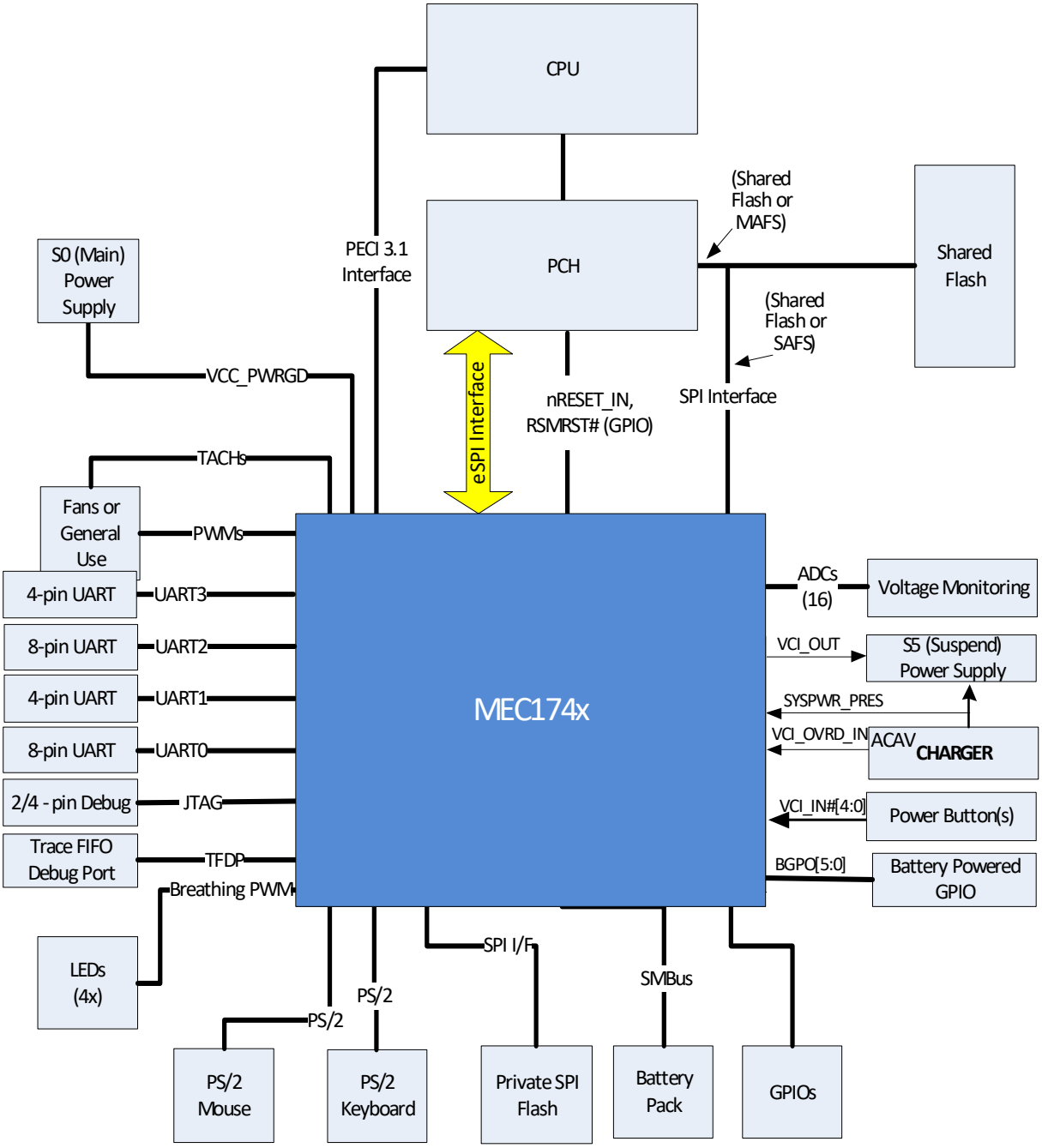
The MEC174x secure boot loader authenticates and optionally decrypts the SPI Flash OEM boot image using the AES-256, ECDSA, SHA-384 cryptographic hardware accelerators. The on-chip hardware accelerators support 128-bit and 256-bit AES encryption, ECDSA and EC_KCDSA signing algorithms, RSA and Elliptic asymmetric public key algorithms and a Non Deterministic Random Number Generator (NDRNG). Runtime APIs are provided in the ROM for customer application code to use the cryptographic hardware. Additionally, the device offers lockable OTP storage for private keys and IDs.

The chip is designed to be incorporated into low power PC architecture designs and supports ACPI sleep states (S0-S5). During normal operation, the hardware always operates in the lowest power state for a given configuration. The chip power management logic offers two low power states: light sleep and heavy sleep. These features can be used to support S0 Connected Standby state and the lower ACPI S3-S5 system sleep states. In connected standby, any eSPI command will wake the device and be processed. When the chip is sleeping, it has many wake events that can be configured to return the device to normal operation. Some examples of supported wake events are PS2 wake events, RTC, Week Alarm, Hibernation Timer, or any GPIO pin.

The Auxiliary Serial (Lenovo ASIC) Interface (ASIF) block allows the eSPI host and the EC to use index addressing to access registers residing in an external IC, which is connected to the MEC174x via SPI. The block presents similar but separate logical, i.e., programming, interfaces to the host and EC. Control logic functions as hardware SPI driver, interpreting commands issued to these interfaces and controlling an embedded SPI module to effect transfers to the external IC.

The chip offers a software development system interface that includes a Trace FIFO Debug port, a host accessible serial debug port with a 16C550A register interface, a Port 80 BIOS Debug Port, and a 2-pin Serial Wire Debug (SWD) interface. Also included is a 4-wire JTAG interface used for Boundary Scan testing.

1.1 System Block Diagram



2.0 PINOUTS

MEC1747Q-A0-I/SZ, MEC1743Q-A0-I/SZ, MEC1743Q-F0-I/SZ- Ballmap 144 pin WFBGA Package	MEC1747Q-A0-I/LJ, MEC1743Q-A0-I/LJ- Ballmap 176 pin WFBGA Package	Pin Description
Not Final	Not Final	
A5	A7	BGPO0
A4	B6	BGPO1/GPIO101
B5	C6	BGPO2/GPIO102
	A6	BGPO3/GPIO172
	C5	BGPO4/GPIO173
	B5	BGPO5/GPIO174
B3	C4	SYSPWR_PRES&VCI_IN3#/GPIO000/I2C11_SDA
	N9	GPIO001/PWM4_ALT
M8	P10	GPIO002/PWM5/SHD_CS1#
F5	F6	GPIO003/I2C00_SDA/UART2_RI#/SPI0_CS0#
C6	B8	GPIO004/I2C00_SCL/UART2_DCD#/SPI0_MOSI
	E6	GPIO005/I2C11_SDA_ALT/I3C00_SDA_HOST/I3C00_SDA_TARGET/GPTP_OUT4/UART3_RX
	C7	GPIO006/I2C11_SCL_ALT/I3C00_SCL_HOST/I3C00_SCL_TARGET/GPTP_OUT7/UART3_TX
B12	B14	GPIO007/I2C03_SDA/PS2_CLK0B/UART3_RTS#
C10	C12	GPIO010/I2C03_SCL/PS2_DAT0B/UART3_DSR#
J6	M4	GPIO011/nSMI_ALT/PWM4/ICT7
N6	N5	GPIO012/I2C07_SDA/SPIPER_IO2/TOUT3/I3C01_SDA_HOST/I3C01_SDA_TARGET
M7	K6	GPIO013/I2C07_SCL/SPIPER_IO3/TOUT2/I3C01_SCL_HOST/I3C01_SCL_TARGET
M9	P11	GPIO014/PWM6/SPIPER_IO1/GPTP_IN2
J7	N10	GPIO015/PWM7/ICT10
N3	P6	GPIO016/GPTP_IN1/SHD_IO3/ICT3(DSW_PWROK)
J8	M14	GPIO017/KSI0/UART0_DCD#/GPTP_IN5
L7	K9	GPIO020/KSI1/UART3_DCD#
N9	P14	GPIO021/KSI2/UART3_DTR#
E2	B4	GPIO022/GPSPI_IO3/GPTP_IN4/32kHz_OUT_ALT
C3	F2	GPIO023/GPSPI_CLK/GPTP_IN7
C2	A3	GPIO024/GPSPI_CS#/GPTP_IN6/I2C07_SCL_ALT
M12	L13	GPIO025/nEMI_INT/UART_CLK/UART1_RI#/TIN0
N13	K10	GPIO026/KSI3/UART0_DTR#/I2C12_SDA/TIN1
K11	L14	GPIO027/KSI4/UART0_DSR#/I2C12_SCL/TIN2

J9	K12	GPIO030/KSI5/I2C10_SDA/TIN3
M11	M10	GPIO031/KSI6/GPTP_OUT1/UART3_RI#
L10	M13	GPIO032/KSI7/GPTP_OUT0/UART0_RI#
B2	B3	GPIO033/TACH3/RC_ID0/UART3_CTS#
H12	J9	GPIO034/GPSPI_IO2/RC_ID1/SPI0_CLK
E13	H12	GPIO035/PWM8/CTOUT1/ICT15/LED3
H13	H14	GPIO036/RC_ID2/SPI0_MISO
M10	M9	GPIO040/GPTP_OUT2/KSO00/UART1_CTS#
	B1	GPIO041
J12	J12	GPIO042/PECI_DAT/SB-TSI_DAT
J13	J10	GPIO043/SB-TSI_CLK
H11	H13	GPIO044/VREF_VTT
E8	F7	GPIO045/KSO01/PWM2_ALT/ICT14[CR_STRAP]
E9	F12	GPIO046/KSO02/ICT11/BCM1_DAT
F13	G10	GPIO047/KSO03/PWM3_ALT/ICT13/BCM1_CLK
F3	D1	GPIO050/ICT0_TACH0/GTACH0
B1	C1	GPIO051/ICT1_TACH1/GTACH1
L8	K7	GPIO052/ICT2_TACH2
M13	P12	GPIO053/PWM0/SPIPER_MSTR_INT/GPWM0
L12	K8	GPIO054/PWM1/SPIPER_SCLK/GPWM1
N4	M5	GPIO055/PWM2/SHD_CS0#[BSS_STRAP]
N5	P9	GPIO056/PWM3/SHD_CLK
D1	B2	GPIO057/VCC_PWRGD/CMP_VIN0
D2	E2	GPIO060/KBRST/TST_CLK_OUT/UART1_DCD#/SPI0_CS1#
N1	K1	GPIO061/ESPI_RESET#
A2	C3	GPIO062/I2C11_SCL(RESETO#)
M4	P4	GPIO063/ESPI_ALERT#/PWM6_ALT/ICT8
J5	M3	GPIO064/SLP_S0#
M2	M1	GPIO065/ESPI_CLK/I2C13_SCL/ICT5_ALT
M1	L1	GPIO066/ESPI_CS#/I2C13_SDA
L2	J7	GPIO067/VREF2_ADC
L3	N1	GPIO070/ESPI_IO0/I2C14_SDA
N2	P1	GPIO071/ESPI_IO1/I2C14_SCL
M3	P2	GPIO072/ESPI_IO2/I2C01_SDA_ALT
L4	P3	GPIO073/ESPI_IO3/I2C01_SCL_ALT
H7	N3	GPIO100/nEC_SCI_ALT/ICT6
F11	G12	GPIO104/UART0_TX
F9	E14	GPIO105/UART0_RX
E3	A2	GPIO106/PWROK/CMP_VREF1
L13	K14	GPIO107/nSMI/KSO04/I2C10_SCL
	N11	GPIO110
	P13	GPIO111
K13	J14	GPIO112/KSO05(DSW_PWRGD)
J11	K13	GPIO113/KSO06/ICT9
H9	J13	GPIO114/PS2_CLK0A/nEC_SCI

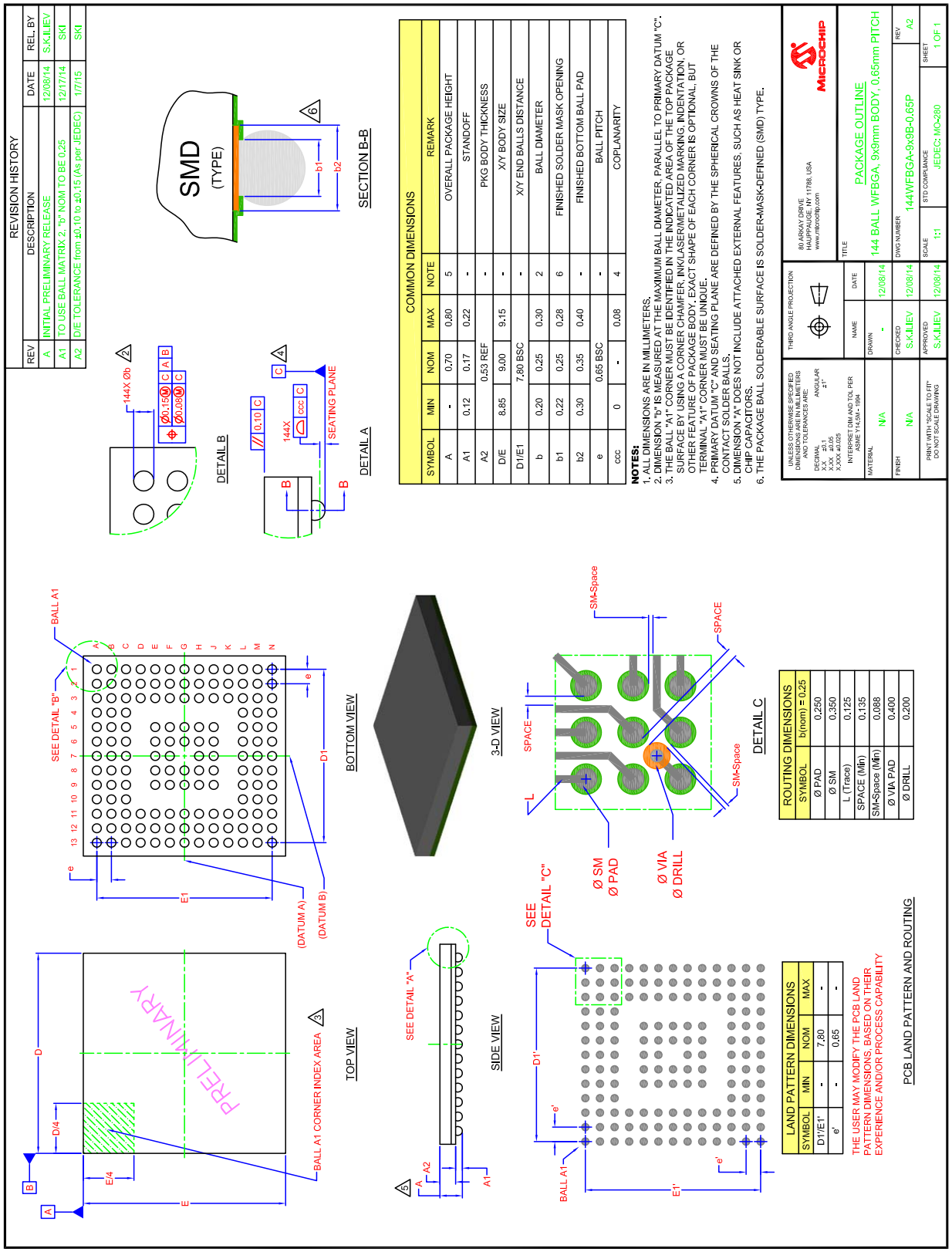
N12	M12	GPIO115/PS2_DAT0A
K12	K11	GPIO120/KSO07/UART1_DTR#
F12	E13	GPIO121/PVT_IO0/KSO08
E11	G9	GPIO122/PVT_IO1/KSO09
E12	E12	GPIO123/PVT_IO2/KSO10
C11	D14	GPIO124/PVT_CS#/KSO11/ICT12/GPTP_OUT6
D11	E11	GPIO125/PVT_CLK/KSO12/GPTP_OUT5
D12	F10	GPIO126/PVT_IO3/KSO13[UART_BSTRAP]
D13	C14	GPIO127/A20M/UART1_RTS#/UART0_CTS#_ALT
N8	N6	GPIO130/I2C01_SDA/SPIPER_IO0/TOUT1
N7	N7	GPIO131/I2C01_SCL/SPIPER_CS#/TOUT0
N11	L10	GPIO132/I2C06_SDA/KSO16/UART2_DSR#_ALT
	F9	GPIO133/PWM9
	G13	GPIO134/PWM10/UART1_RTS#_ALT
	H9	GPIO135/UART1_CTS#_ALT
L11	M11	GPIO140/I2C06_SCL/ICT5/KSO17/UART2_DTR#_ALT
B7	E7	GPIO141/I2C05_SDA/SPI1_CLK/UART2_RTS#/UART0_DCD#_ALT
F7	C8	GPIO142/I2C05_SCL/SPI1_MOSI/UART2_CTS#/UART0_DSR#_ALT
A7	B9	GPIO143/I2C04_SDA/SPI1_MISO/UART0_DTR#_ALT
E7	A9	GPIO144/I2C04_SCL/UART0_RTS#/SPI1_CS#/UART0_RI#_ALT
A8	C9	GPIO145/I2C09_SDA/UART2_RX/JM_TDI
G8	B10	GPIO146/I2C09_SCL/UART2_TX/ITM/JM_TDO
C7	A11	GPIO147/I2C15_SDA/UART2_DSR#/JM_TCLK
F8	A10	GPIO150/I2C15_SCL/UART2_DTR#/JM_TMS
L9	M8	GPIO151/ICT4/KSO15
N10	N12	GPIO152/KSO14/GPTP_OUT3/I2C07_SDA_ALT
C12	D12	GPIO153/LED2
A12	D11	GPIO154/I2C02_SDA/CPU_C10/PS2_CLK1B
C9	E10	GPIO155/I2C02_SCL/PS2_DAT1B(SYSPWR_VALID)
A13	B13	GPIO156/LED0
B13	C13	GPIO157/LED1
	F14	GPIO160/PWM11/PROCHOT_IN#/PROCHOT_IO#
C4	D4	VCI_IN2#/GPIO161
A6	B7	VCI_IN1#/GPIO162
A9	B11	GPIO165/32KHZ_IN/CTOUT0
	D2	GPIO166/PWRGD_S0iX_ALT
G12	H10	GPIO170/UART1_TX/TFDP_CLK[JTAG_STRAP]
G9	G14	GPIO171/UART1_RX/TFDP_DATA
C13	D13	GPIO175/CMP_VOUT1/PWM8_ALT
H3	G6	GPIO200/ADC00
J3	G1	GPIO201/ADC01
J2	G2	GPIO202/ADC02
J1	H3	GPIO203/ADC03
H2	J3	GPIO204/ADC04
K3	J1	GPIO205/ADC05

L1	K3	GPIO206/ADC06
K2	L3	GPIO207/ADC07[CMP_STRAP]
	H6	GPIO210/ADC08
	G3	GPIO211/ADC09
	H2	GPIO212/ADC10
	H1	GPIO213/ADC11
	J2	GPIO214/ADC12
	K2	GPIO215/ADC13
	L2	GPIO216/ADC14
	M2	GPIO217/ADC15
	N14	GPIO220
C1	C2	GPIO221/32KHz_OUT/GPTP_IN3/CMP_VIN1/SYS_SHDN_FW#
L5	N4	GPIO222/PROCHOT_IN#_ALT
M6	P8	GPIO223/SHD_IO0
M5	P5	GPIO224/GPTP_IN0/SHD_IO1
	A14	GPIO225/UART0_RTS#_ALT
F2	A1	GPIO226/PWRGD_S0iX/CMP_VREF0
L6	P7	GPIO227/SHD_IO2[PWRGD_STRAP]
	N8	GPIO230/I2C08_SCL
	M6	GPIO231/I2C08_SDA
	N2	GPIO232/UART1_DSR#_ALT
	M7	GPIO233
	E3	VCI_IN4#/GPIO234
	N13	GPIO235
	L11	GPIO236
G13	L12	GPIO240
B8	C11	GPIO241/CMP_VOUT0/PWM0_ALT
A10	C10	GPIO242/VCC_PWRGD_ALT
C8	A13	GPIO243/GPSPI_IO1
A11	B12	GPIO244/UART_CLK_ALT/PWROK_ALT
B11	F8	GPIO245/GPSPI_IO0
B10	D10	GPIO246/PWRGD_S0iX_ALT2/CTOUT1_ALT
	E9	GPIO253
B9	A12	GPIO254
B6	E8	GPIO255/UART1_RX_ALT/UART1_DSR#
G11	F13	JTAG_RST#
D3	D3	nRESET_IN
E6	A8	VCI_IN0#(EMDRST_IN)
C5	D5	VCI_OUT2
F1	E5	VCI_OVRD_IN
A3	A5	XTAL1
A1	A4	XTAL2
B4	F3	VSS_ANALOG
E1	G5	VTR_PLL
E5	E4	VBAT

F6	K5	VSS
G1	E1	VTR_REG
G2	K4	VREF_ADC
K1	J6	VSS_ADC
G5	J5	VTR1
G6	H5	VTR_ANALOG
H1	F1	VR_CAP
G3	F5	VSS
H8	L5	VTR2
H6	L4	VTR3
H5	J8	VSS

3.0 PACKAGES

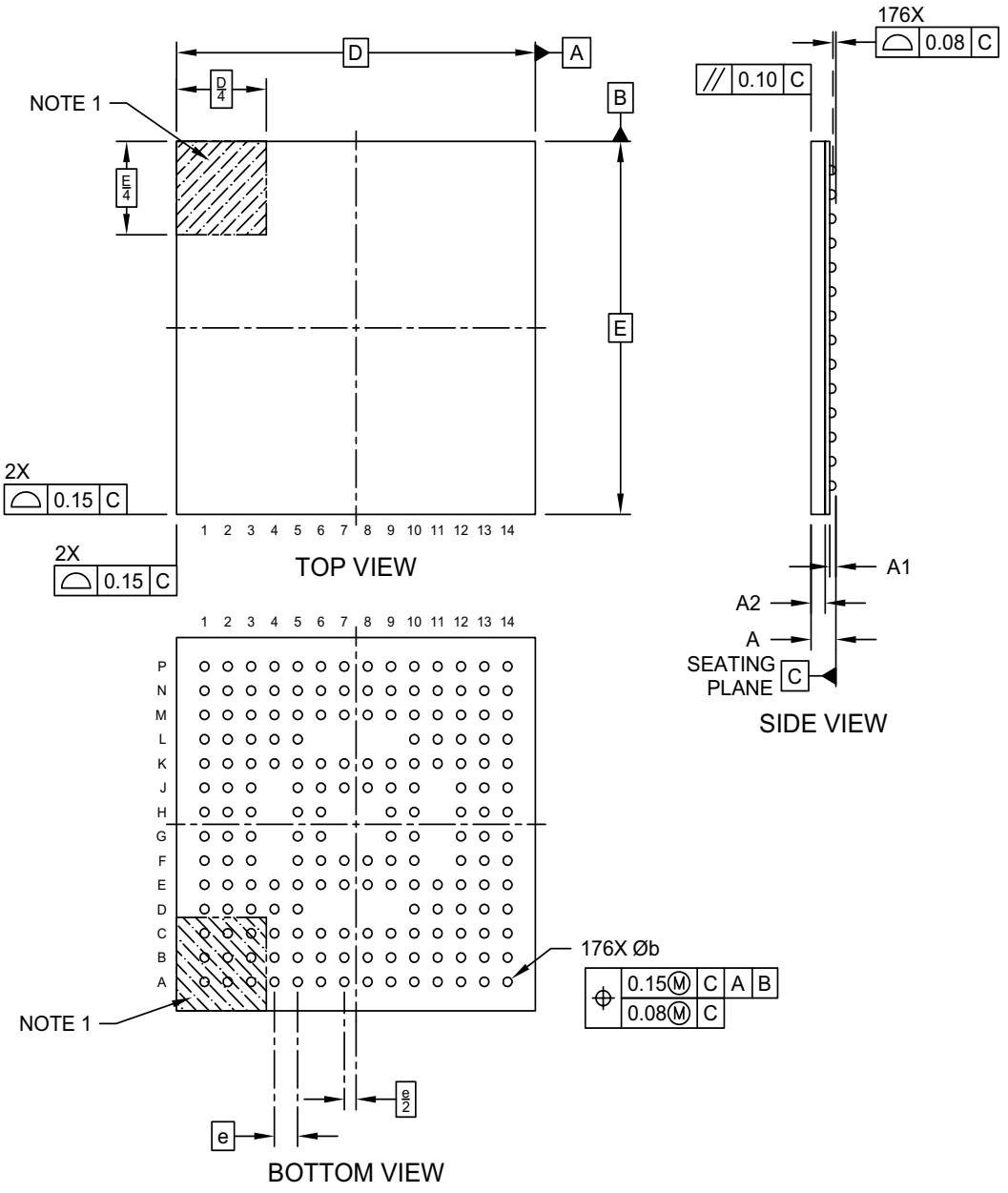
3.1 144 pin WFBGA (SZ)(Preliminary, Do not use for layout)



3.2 176 pin WFBGA (LJ)(Preliminary, Do not use for layout)

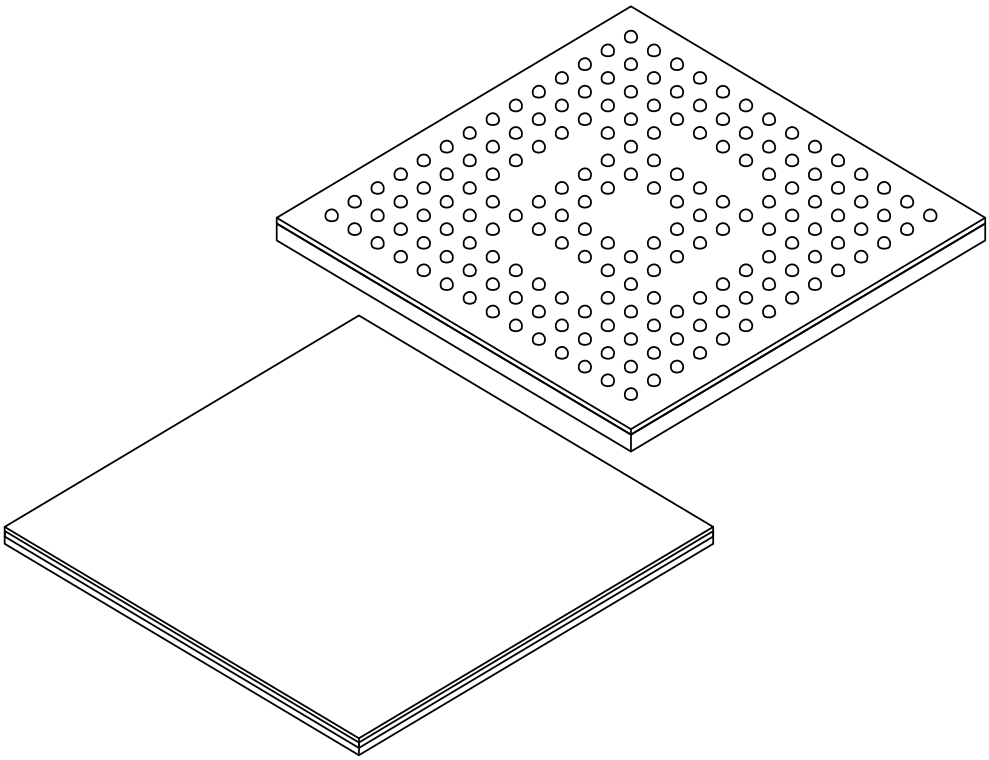
176-Ball Very, Very Thin Fine Pitch Ball Grid Array (LJX) - 10x10 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



176-Ball Very, Very Thin Fine Pitch Ball Grid Array (LJX) - 10x10 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		176	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	0.80
Standoff	A1	0.12	0.17	-
Mold Cap Thickness	A2	0.35	0.40	0.45
Overall Length	D		10.00 BSC	
Overall Width	E		10.00 BSC	
Ball Diameter	b	0.20	0.25	0.30

Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.