

MEC1501 Modular EC Card

Mates with the Intel RVP3 SkyLake Platform

BLOCK DIAGRAM

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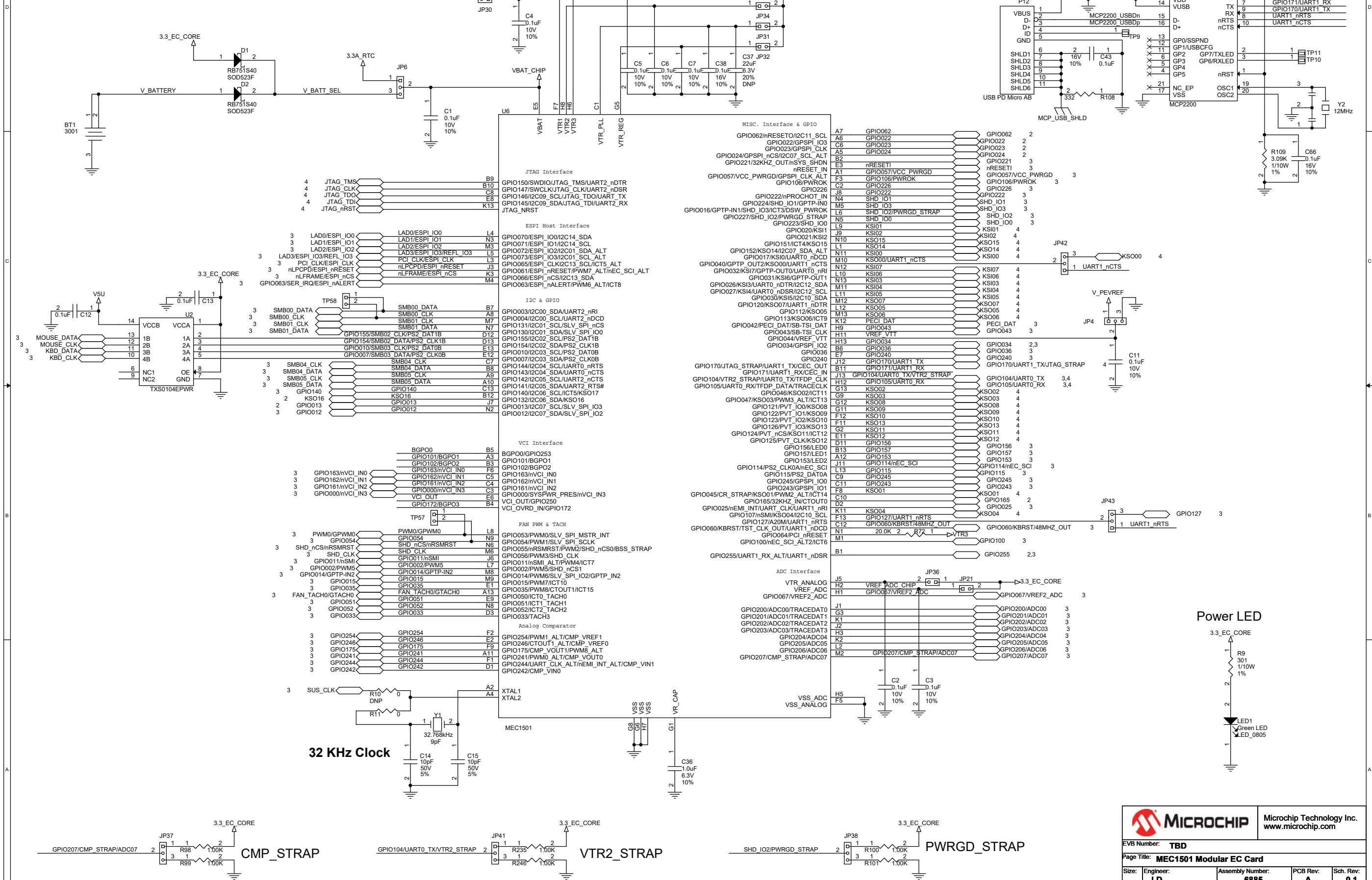
Revision History

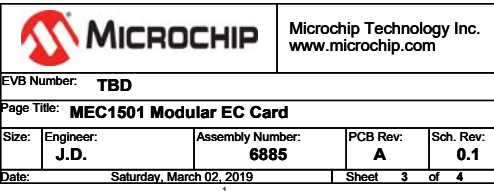
Rev 1.0:
Initial Release

Pinout diagram for J50 connector:

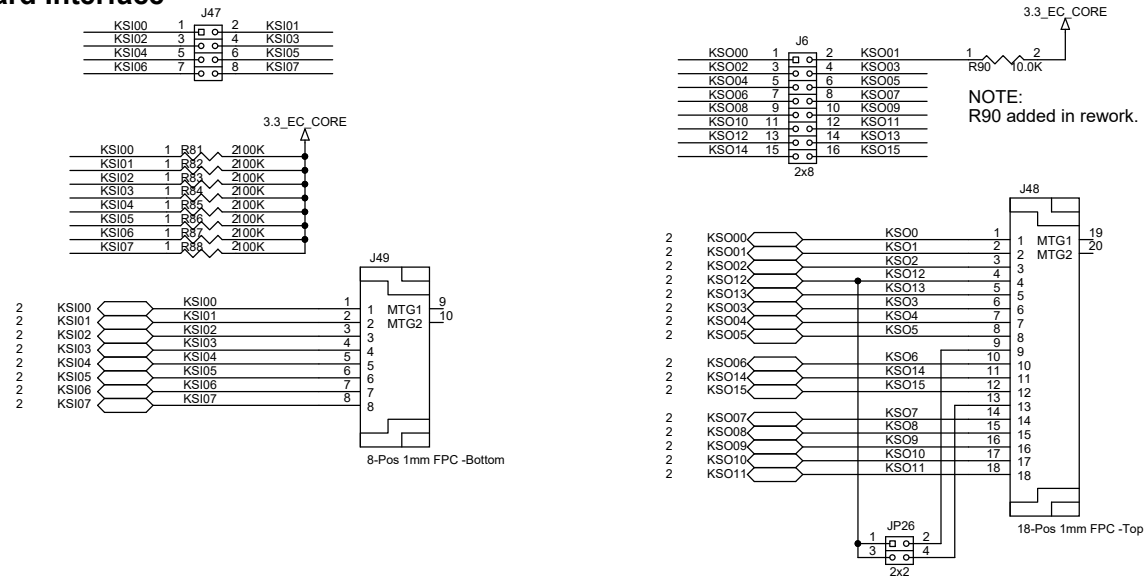
Pin	Signal	Notes
1	Ground	
2	GPIO013	
3	Ground	
4	GPIO022	
5	Ground	
6	GPIO023	
7	Ground	
8	GPIO024	
9	Ground	
10	GPIO062	
11	VCI_OUT	
12	Ground	
13	BGPO0	
14	Ground	
15	Ground	
16	GPIO034	2.3

+3.3V LDO ^{VR2} MCP1826S-33 Voltage Regulator



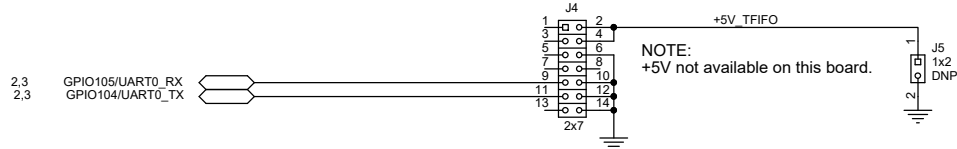


Keyboard Interface

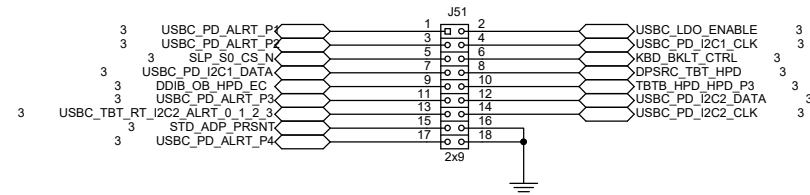


Software Developers Debug Interface

Mates with: Trace FIFO Board (Assy 6227)
Pegasus Debugger (Assy 6345)



Ver 0.9 Header



JTAG

