MEC172x
Silicon Errata and Data Sheet Clarification

TABLE 1: SILICON IDENTIFICATION

Part Number	Silicon Identifier	Functional Revision A	Functional Revision B(4)
MEC1721N-B0-I/LJ	Device ID(1)	0022_27h	0022_27h
	Revision ID for Silicon Revision(2)	00h	01h
MEC1723N-B0-I/SZ	Device ID(1)	0022_34h	0022_34h
	Revision ID for Silicon Revision(2)	00h	01h
MEC1723N-F0-I/SZ	Device ID(1)	0022_44h	0022_44h
	Revision ID for Silicon Revision(2)	00h	01h
MEC1723N-B0-I/LJ	Device ID(1)	0022_37h	0022_37h
	Revision ID for Silicon Revision(2)	00h	01h
MEC1725N-B0-I/LJ	Device ID(1)	0022_57h	0022_57h
	Revision ID for Silicon Revision(2)	00h	01h
MEC1727N-B0-I/SZ	Device ID(1)	0022_74h	0022_74h
	Revision ID for Silicon Revision(2)	00h	01h
MEC1727N-B0-I/LJ	Device ID(1)	0022_77h	0022_77h
	Revision ID for Silicon Revision(2)	00h	01h

Note 1: The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h.
2: The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h.
3: Product Identification System (PIS) is defined in the Product Data Sheet.
4: The Rev B fixes have not been validated with silicon at this time. This is the current expectations.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions (1)	Affected Revisions (1)
				A	B
QMSPI Controller	SPI Write	1.	API “api_qmspi_flash_cmd” does not write 3rd data byte for SPI Write only operation.	X	X
eSPI SAF	Prefetch data	2.	EC may return stale data to a eSPI 64 Byte read access, if prefetch and execute from Cache is enabled at the same time.	X	X
PCR	Processor Clock	3.	Processor clock switching may cause a clock glitch.	X	X
QMSPI	Shared SPI	4.	The SHD_SPI interface may not work at 96Mhz across all voltage and temperature ranges with sufficient margin.	X	

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions (1)	Affected Revisions (1)
				A	B
SAF Bridge	Flash memory Sleep	5.	When eSPI Pre-fetch, Flash memory Sleep and Individual sleep enables are enabled together the EC may not enter sleep state	X	
PCR	JTAG Reset Status	6.	JTAG_RST# status does not reflect correctly on bit 7 of PCR Power Reset Status Register.	X	
Pads	5VT pad	7.	High leakage current on 5V Tolerant (5VT) pads	X	
Blinking/Breathing LED	LED3	8.	LED3 is on GPIO226 alternate function 1 and not GPIO035 alternate function 4.	X	
Boot ROM	TAG1 Image Authentication	9.	Boot ROM does not authenticate the TAG1 image after Soft Reset.	X	
Boot ROM	JTAG Enable	10.	Boot ROM may take a long time to open JTAG port in case of Boot failure.	X	
Boot ROM	e(UDS) CRC	11.	Boot ROM clears E(UDS) CRC status bit in error when clearing SRAM.	X	
Boot ROM	Authentication	12.	Boot ROM revokes keys without authentication.	X	
PCR	VCC_PWRGD Status	13.	VCC_PWRGD status bit does not reflect the VCC_PWRGD pin status	X	X
EC Subsystem	Crypto	14.	Crypto operations grab very high AHB bus bandwidth making other applications wait till Crypto operations are over.	X	X
CACHE Controller	CACHE	15.	The Cache Controller is not enabled in these parts	X	X
ADC	Gain Error	16.	Analog to Digital converter Gain Error correction	X	X
QMSPI	LDMA TX	17.	Local DMA TX channel needs Block Soft reset after every transfer	X	X

Silicon Errata Issues

1. Module: QMSPI Controller

DESCRIPTION

API “api_qmspi_flash_cmd” does not write 3rd data byte for SPI Write only operation.

While initiating a flash command with only transmit function (write) and having more than 3 bytes, API “api_qmspi_-flash_cmd” fails to transmit the third byte.

END USER IMPLICATIONS

While initiating a flash command with only transmit function (SPI Flash memory write) and having more than 3 bytes, API “api_qmspi_flash_cmd” fails to transmit the third byte. This issue is only observed while running the QMSPI block at 12MHz clock frequency or lower. The CLIB/PLIB collateral will have a recommended solution for this issue as a PLIB function.

2. Module: eSPI SAF Block

DESCRIPTION

EC may return stale data to a eSPI 64 Byte read access, if prefetch and execute from Cache is enabled at the same time.

if a flash is being modified over eSPI and verified 64 bytes at a time, and if the Prefetch feature and the new Cache feature are both active, eSPI may return stale data from before the Write was performed.

END USER IMPLICATIONS

User may not be able to use the exact below sequence.

Program aligned 64 bytes, Read back the same 64 bytes, Program next 64 bytes, Read back these 64 bytes.

Work Around

Only the above described sequence is affected when eSPI 64 Byte read access to the previously written location is done with Prefetch and execute from Cache enabled at the same time. It is recommended that eSPI read some other address in between Write and Read to the same 64 Byte address or read the same 64 Byte address twice.

3. Module: PCR Block

DESCRIPTION

Processor clock switching may cause a clock glitch.

Glitch on the clock may corrupt the instruction and data fetch from the memory.

END USER IMPLICATIONS

Processor may end up in unknown state.

Work Around

The above problem can be completely avoided by using 4 NOP instruction before and after the processor clock switch instruction followed by Data and Instruction Barrier instruction as shown in the sample code below.

```
__nop; __nop; __nop; __nop;
(*(unsigned char*) 0x4008_0104 = Clock Divide value;
__nop; __nop; __nop; __nop;
__DSB(); // Data instruction barrier to complete any write before the next instruction
__ISB(); //Instruction barrier to complete the instruction and to flush the pipe
```

4. Module: QMSPI Block

DESCRIPTION

The SHD_SPI interface may not work at 96Mhz across all voltage and temperature ranges with sufficient margin.

END USER IMPLICATIONS

When used at 96MHz, the Shared SPI interface (SHD_* pins) may not transfer data properly at 96MHz across all voltage and temperature ranges.

Work Around

For Rev A parts, 96Mhz on Shared SPI interface should not be used for production.

5. Module: SAF Bridge Block

DESCRIPTION

When eSPI Pre-fetch, Flash memory sleep and Individual block sleep enables are enabled together the EC may not enter sleep state.

END USER IMPLICATIONS

When eSPI Pre-fetch, Flash memory sleep and Individual block sleep enables are enabled together the EC may not enter sleep state and continue to consume normal power.

Work Around

This problem can be solved by using Sleep All bit instead of Individual block sleep enable bits.

6. Module: PCR Block

DESCRIPTION

JTAG_RST# status does not reflect correctly on bit 7 of PCR Power Reset Status Register.

END USER IMPLICATIONS

Raw JTAG RESET pin (JTAG_RST#) status does not reflect correctly on bit 7 of PCR Power Reset Status Register. This bit status should not be used to determine the JTAG_RST# pin status by the application code.

Work Around

Currently there is no workaround for this problem.

7. Module: Pads Block

DESCRIPTION

High leakage current on 5V Tolerant (5VT) pads.

END USER IMPLICATIONS

5V-tolerant (5VT) pads show leakage of about 12uA at room when applying 5V with all VTRs down.

Work Around

There is no workaround for this issue in Rev A.

8. Module: Blinking/Breathing LED Block

DESCRIPTION

LED3 is on GPIO226 alternate function 1 and not GPIO035 alternate function 4.

END USER IMPLICATIONS

LED3 is on alternate function 1 on GPIO226.

Work Around

LED3 is not on GPIO0035 alternate function 4. LED3 is on alternate function 1 on GPIO226 in Rev A parts. This needs to be considered for PCB design.

9. Module: Boot ROM Block

DESCRIPTION

Boot ROM does not authenticate the TAG1 image after Soft Reset, if the key hash Blob was authenticated previously.

END USER IMPLICATIONS

When Boot ROM validates a key hash blob, it sets an associated flag in a scratch register to indicate that the blob was checked. If a “checked” flag is already set following a soft reset, the Boot ROM will not use the associated key hash blob to authenticate a TAGx image.

Work Around

There is no workaround for this issue in Rev A.

10. Module: Boot ROM Block

DESCRIPTION

Boot ROM may take a long time to open JTAG port in case of Boot failure.

END USER IMPLICATIONS

By default at Power On Reset (POR) the JTAG port is disabled and locked. When Boot ROM runs the final Boot exit sequence, it enables the JTAG port if Debug is enabled through the OTP bit. In case of Boot failure, the Boot ROM may try up to 15 attempts to authenticate, decrypt and load the application image taking considerable time. In case power sequencing feature is enabled through OTP, there may be even longer delay or wait for power up event, before JTAG port is enabled.

Work Around

If the JTAG port is not been opened up and power sequencing feature is enabled in the part, please ensure all Power sequencing event complete as expected. There is no workaround for this issue in Rev A parts. This issue is fixed in Rev B.

11. Module: Boot ROM

DESCRIPTION

Boot ROM clears E(UDS) CRC status bit in error when clearing SRAM.

END USER IMPLICATIONS

Application code does not know if the E(UDS) value stored in the read/write locked OTP memory has been altered from its original programmed value.

Work Around

None. There is no fix for this problem in Rev A parts, however it is fixed in Rev B parts.

12. Module: Boot ROM

DESCRIPTION

Boot ROM only set the authentication status bits if authentication is enabled and the authentication check fails.These bits are not set when:

- Authentication enabled and authentication passes.
- Authentication disabled and the hash integrity check fails.

END USER IMPLICATIONS

If authentication is not enabled, the authentication status of both images is unknown. User must not use these bits when authentication is disabled.

Work Around

We have common status bit which will tell which TAG image has been loaded for images with integrity check.

TABLE 3: ROM ACTION FLAG 64 BITS TOTAL (0X1F4)

Bit Number	Description
27	RLOG_LOAD_FROM_TAG0
28	RLOG_LOAD_FROM_TAG1

There is no fix for this problem in Rev A parts, however it is fixed in Rev B parts.

13. Module: PCR Block

DESCRIPTION

VCC_PWRGD status at bit[2] in PCR Power Reset Status Register does not give the value of VCC_PWRGD pin.

END USER IMPLICATIONS

VCC_PWRGD status at bit[2] in PCR Power Reset Status Register at offset 0x10 in PCR block does not give the status of VCC_PWRGD pin. If the EC application code waits for this bit to be asserted before asserting PWR_INV bit, the code will not proceed further.

Work Around

VCC_PWRGD is on GPIO057 (GPIO057/VCC_PWRGD). The workaround is to read the GPIO input register of GPIO057 in place of VCC_PWRGD status. This will give the value of VCC_PWRGD pin.

14. Module: EC Subsystem Block

DESCRIPTION

Crypto operations grab very high AHB bus bandwidth making other applications wait till Crypto operations are over.

END USER IMPLICATIONS

The Crypto block grabs the complete bandwidth of the internal AHB bus when in operation. To make sure optimal bus utilization and system performance when Crypto operation are running, the bandwidth of the Crypto operation has to be limited.

Work Around

Program 0x0500 at register offset 0x58 in EC Subsystem for proper system performance while Crypto operations are running. This will ensure that there is sufficient AHB bandwidth for other high speed peripheral to share the AHB bus while Crypto operations are being executed.

15. Module: CACHE Controller Block

DESCRIPTION

The Cache Controller is not enabled in these parts.

END USER IMPLICATIONS

Cache Controller is not enabled in MEC172x parts. User should not use Cache Controller for this family of parts.

Work Around

There is currently no workaround for this.

16. Module: Analog to Digital converter Gain Error Correction

DESCRIPTION

VREF observed at ADC input is less than VREF applied to external pin and requires correction in ADC calculations.

END USER IMPLICATIONS

Real internal VREF is less then external one. This causes gain error.

Work Around

For all measurements,10 or 12 bit ADC, VREF value has to be corrected by application code as below.

VREF_ACTUAL = VREF- VREF/Alpha, where VREF_ACTUAL is the actual ADC reference. Rounding of VREF_ACTUAL to the nearest allowable precision digit should be done as the last step before substituting the value in the below equation to calculate the input voltage.

VREF is the external ADC reference.

Input Voltage = (ADC Reading + [Beta])*(VREF_ACTUAL)/((2^res)-1) where res = 10 or 12, respectively, depending on bit resolution used.

TABLE 4: ALPHA AND BETA VALUE FOR ADC READING CORRECTION

Vref	Alpha	Beta for 10 bit resolution	Beta for 12 bit resolution
3.3V	0x86	1	3
3.0V	0x10E	1	3

17. Module: QMSPI LDMA TX Channel Requires Soft Reset After Every Transfer

DESCRIPTION

The QMSPI LDMA TX Channel has a corner case where the transfer may not happen on the SPI bus. This condition only occurs for the FW initiated QMSPI LDMA TX Channel and does not affect any other transfer from any other source.

END USER IMPLICATIONS

When the error condition happens, the transfer does not happen on the SPI bus and there is no indication of this error to the EC.

Work Around

The QMSPI LDMA TX requires soft reset after every transfer to reset all the internal variables. This would mean that all the registers will have to be reprogrammed after soft reset. Our recommendation is to save and restore the following QMSPI registers after every soft reset: Mode, Interface Control, CS Timing, Mode ALT1, TAPS, TAPS ADJ, TAPS CTRL. These registers do not change for every transaction. All other registers will need to be reprogrammed.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet.

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 5: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
Boot ROM	1.	In MEC172x ROM description addendum TABLE 5-5: FIRMWARE IMAGE HEADER FORMAT, in Byte “0x14 to 0x17”, Bits [5:0] should be read as Bits [6:0]
ARM M4F	2.	ARM M4F base address is 0xE000ED00 and is incorrect in Table 3-5 in the data sheet.

1. Module: Boot ROM

In the MEC172x ROM description addendum document TABLE 5-5: FIRMWARE IMAGE HEADER FORMAT, in “Byte 0x14 to 0x17” row “Bits [5:0] must be 0” should be read as “Bits [6:0] must be 0” so as to be evenly divisible by 128.

2. Module: ARM M4F

ARM M4F module base address and registers mentioned in Table 3-5 REGISTER MAP are incorrect. The correct addresses of the registers are given in the below table.

TABLE 3-5 REGISTER MAP

Block	Instance	Register	Host Type	Register Address
ARM M4F	0	Auxiliary_Control		E000E008
ARM M4F	0	SystemTick_Ctrl_Status		E000E010
ARM M4F	0	SystemTick_Reload_Value		E000E014
ARM M4F	0	SystemTick_Current_Value		E000E018
ARM M4F	0	SystemTick_Calibration_Value		E000E01C
ARM M4F	0	CPU_ID		E000ED00
ARM M4F	0	Interrupt_Ctl_and_State		E000ED04
ARM M4F	0	Vector_Table_Offset		E000ED08
ARM M4F	0	Application_Interrupt_and_Reset_Ctl		E000ED0C
ARM M4F	0	System_Ctl		E000ED10
ARM M4F	0	Config_and_Ctl		E000ED14
ARM M4F	0	System_Handler_Priority1		E000ED18
ARM M4F	0	System_Handler_Priority2		E000ED1C
ARM M4F	0	System_Handler_Priority3		E000ED20
ARM M4F	0	System_Handler_Ctl_and_State		E000ED24
ARM M4F	0	Configurable_Fault_Status		E000ED28
ARM M4F	0	Hard_Fault_Status		E000ED2C
ARM M4F	0	Debug_Fault_Status		E000ED30
ARM M4F	0	Debug_Halting_Ctl_and_Status		E000EDF0
ARM M4F	0	Debug_Core_Register_Selector		E000EDF4
ARM M4F	0	Debug_Core_Register_Data		E000EDF8
ARM M4F	0	Debug_Exception_and_Monitor_Ctl		E000EDFC
ARM M4F	0	Bus_Fault_Address		E000ED38

Block	Instance	Register	Host Type	Register Address
ARM M4F	0	Auxiliary_Fault_Status		E000ED3C
ARM M4F	0	Processor_Feature0		E000ED40
ARM M4F	0	Processor_Feature1		E000ED44
ARM M4F	0	Debug_Features0		E000ED48
ARM M4F	0	Auxiliary_Features0		E000ED4C
ARM M4F	0	Memory_Model_Feature0		E000ED50
ARM M4F	0	Memory_Model_Feature1		E000ED54
ARM M4F	0	Memory_Model_Feature2		E000ED58
ARM M4F	0	Memory_Model_Feature3		E000ED5C
ARM M4F	0	Instruction_Set_Attributes0		E000ED60
ARM M4F	0	Instruction_Set_Attributes1		E000ED64
ARM M4F	0	Instruction_Set_Attributes2		E000ED68
ARM M4F	0	Instruction_Set_Attributes3		E000ED6C
ARM M4F	0	Instruction_Set_Attributes4		E000ED70
ARM M4F	0	Coprocessor_Access_Ctl		E000ED88
ARM M4F	0	Software_Triggered_Interrupt		E000EF00

APPENDIX A: DOCUMENT REVISION HISTORY

Revision	Description
DS80000913B (01-21-21)	Added Data Sheet Clarification 2. for ARM M4F module base address and registers mentioned in Table 3-5. Revision ID changed from 0x82 to 0x00 for Functional Revision A and 0x82 to 0x01 for Functional Revision B in Table 1.
DS80000913A (10-22-20)	Added Errata 16. for ADC Gain Error Correction.
	Added Errata 17. for QMSPI LDMA TX
	Added MEC1727N-B0-I/SZ and MEC1727N-B0-I/LJ packages.
	Added Errata 15. and removed MEC1723N-P0-I/9Y package.
	Added Errata 14.
	Added Errata 4. to 13.
	Initial release.

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