

Submission 5

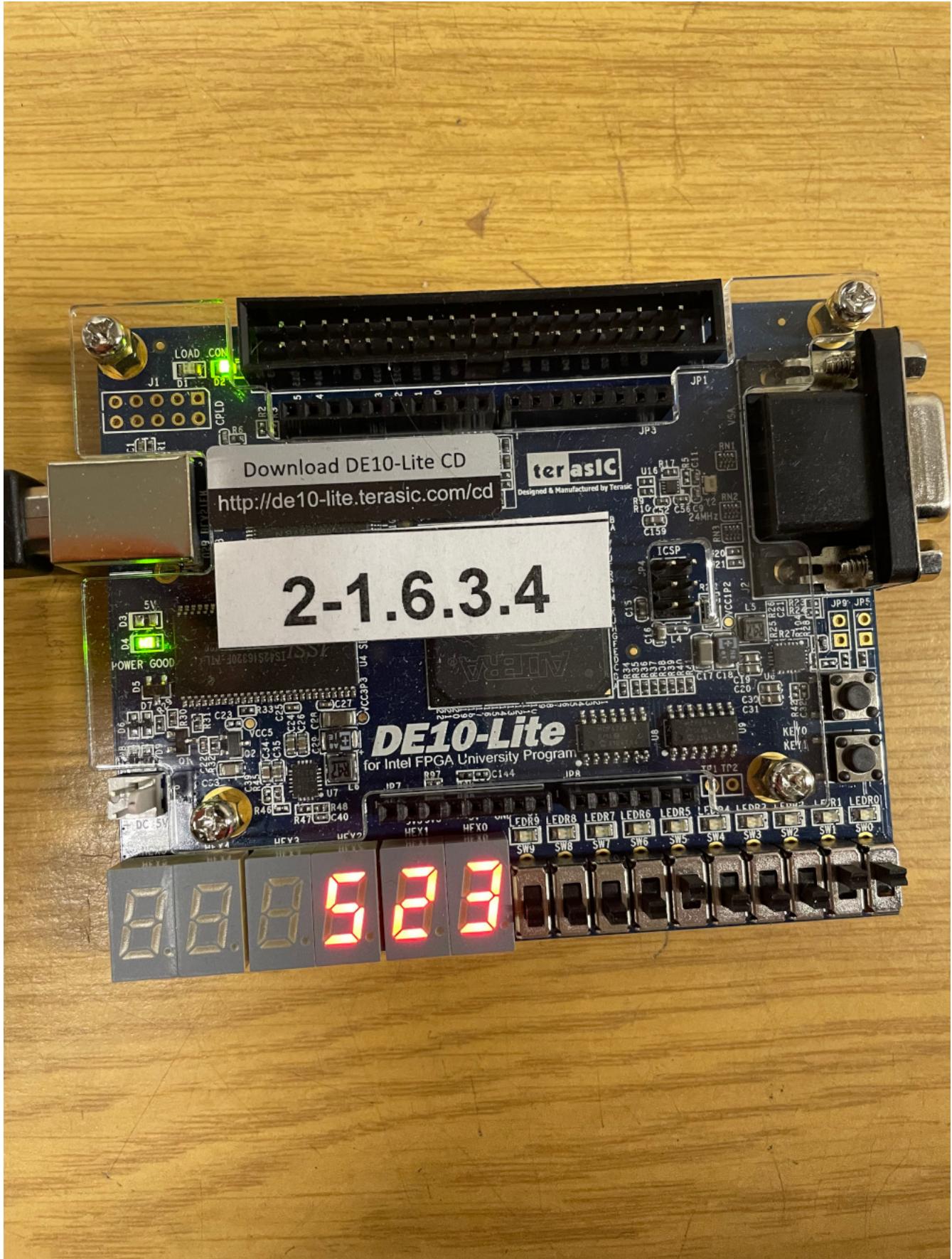
5.1.1

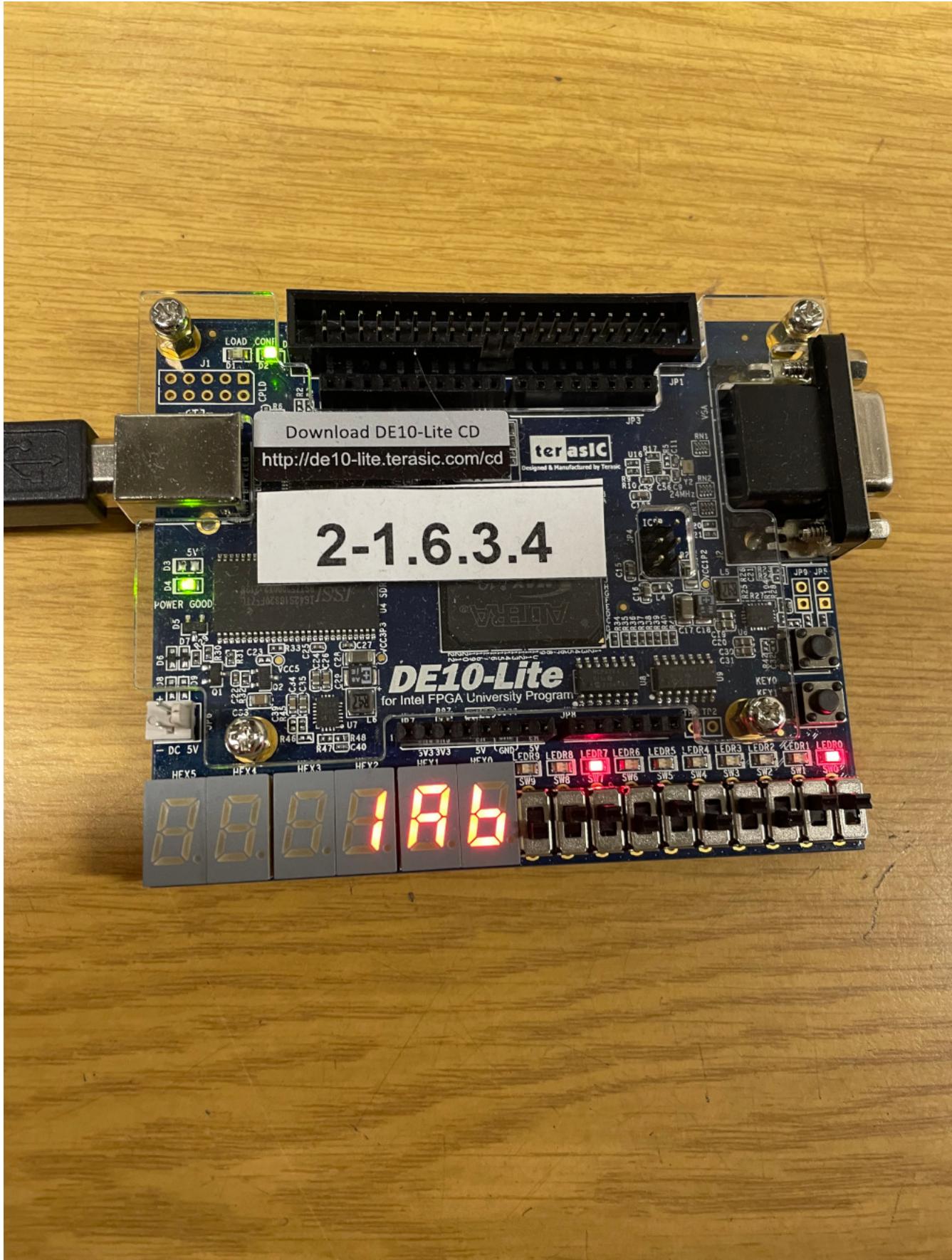
i_a	i_b	i_alu_ctrl	o_result	o_carry_out
8'b0000_0000	8'b0000_0000	2'b00	8'b0000_0000	1'b0
8'b1011_1101	8'b1010_0101	2'b00	8'b0110_0010	1'b1
8'b1011_1101	8'b1010_0101	2'b01	8'b0001_1000	1'b1
8'b1011_1101	8'b1010_0101	2'b10	8'b1010_0101	1'b1
8'b1011_1101	8'b1010_0101	2'b11	8'b1011_1101	1'b1

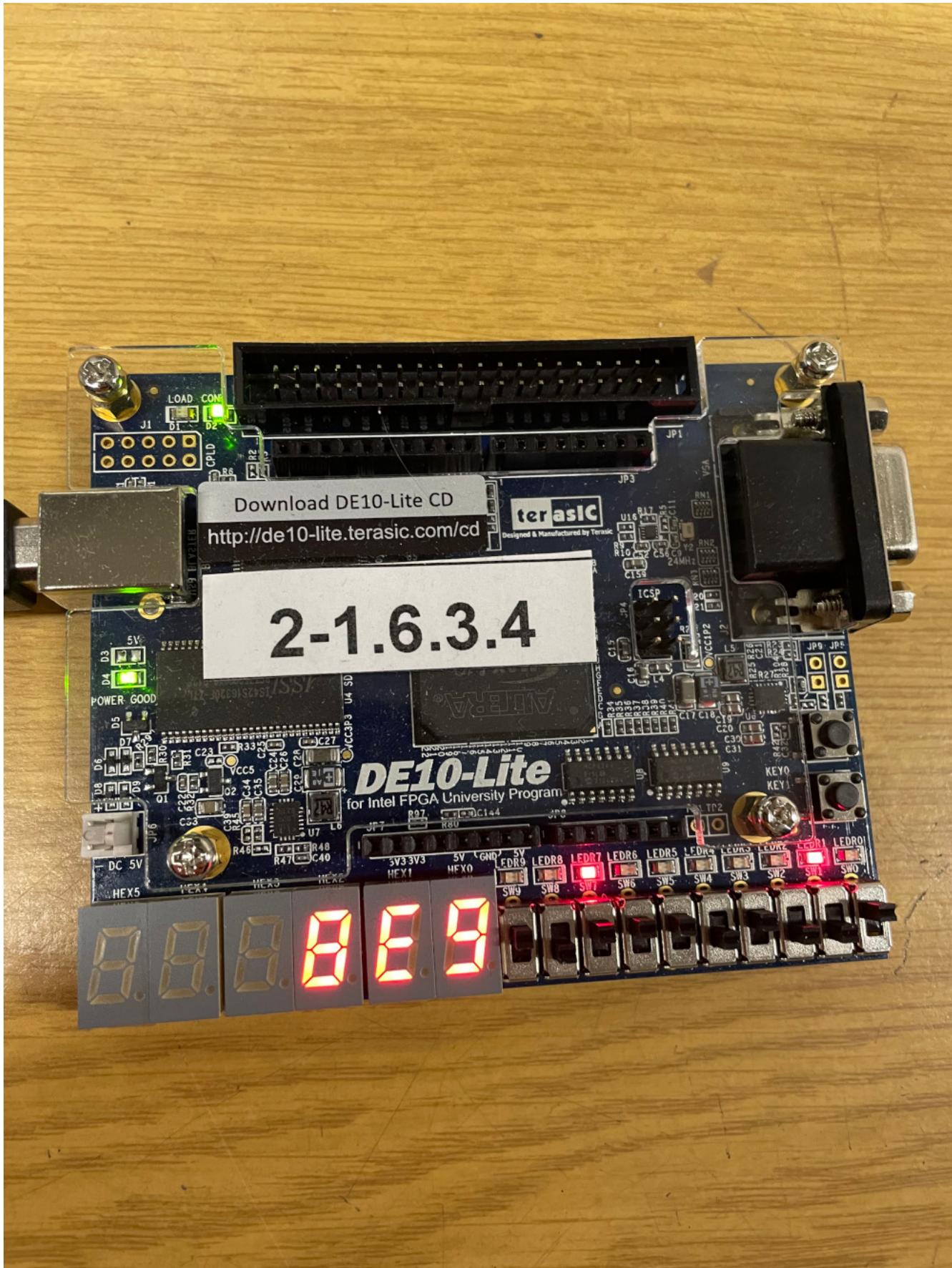
5.1.3

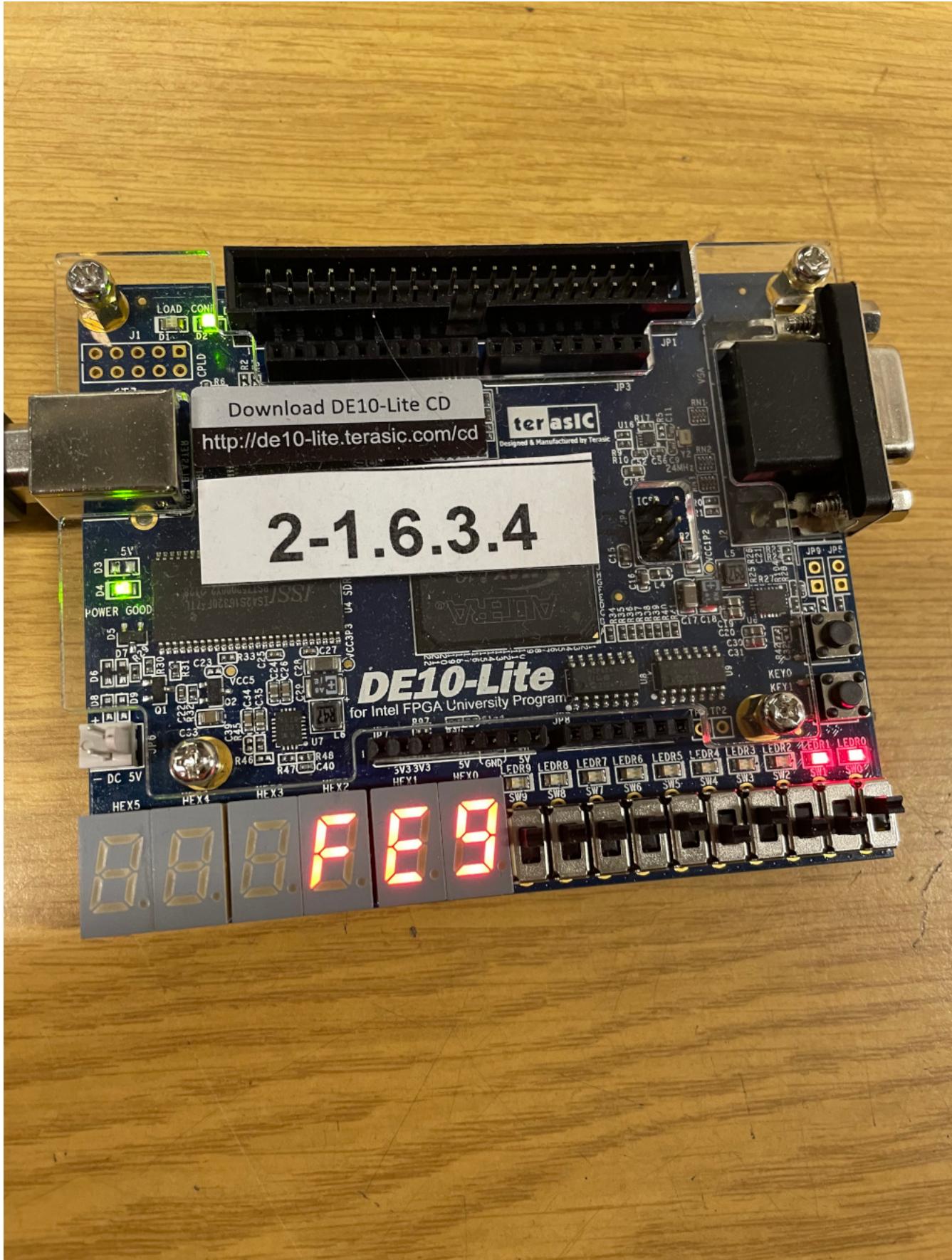


5.2.3







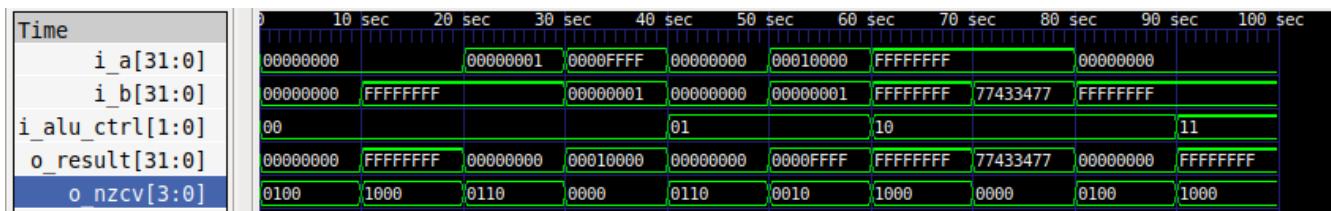


5.3.2

i_a	i_b	i_alu_ctrl	o_result	o_nzcv
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32'h0000_0000	32'h0000_0000	2'b00	32'h0000_0000	4'b0100
32'h0000_0000	32'hffff_ffff	2'b00	32'hffff_ffff	4'b1000
32'h0000_0001	32'hffff_ffff	2'b00	32'h0000_0000	4'b0110
32'h0000_ffff	32'h0000_0001	2'b00	32'h0001_0000	4'b0000
32'h0000_0000	32'h0000_0000	2'b01	32'h0000_0000	4'b0110
32'h0001_0000	32'h0000_0001	2'b01	32'h0000_ffff	4'b0010
32'hffff_ffff	32'hffff_ffff	2'b10	32'hffff_ffff	4'b1000
32'hffff_ffff	32'h7743_3477	2'b10	32'h7743_3477	4'b0000
32'h0000_0000	32'hffff_ffff	2'b10	32'h0000_0000	4'b0100
32'h0000_0000	32'hffff_ffff	2'b11	32'hffff_ffff	4'b1000

5.3.3



5.4.1

Raw (bits)	Unsigned	Signed (two's complement)
0000 ₂	0 ₁₀	0 ₁₀
0001 ₂	1 ₁₀	1 ₁₀
0010 ₂	2 ₁₀	2 ₁₀
0011 ₂	3 ₁₀	3 ₁₀
0100 ₂	4 ₁₀	4 ₁₀
0101 ₂	5 ₁₀	5 ₁₀
0110 ₂	6 ₁₀	6 ₁₀
1000 ₂	8 ₁₀	-(2 ³ -0) = -8 ₁₀
1001 ₂	9 ₁₀	-(2 ³ -1) = -7 ₁₀
1010 ₂	10 ₁₀	-(2 ³ -2) = -6 ₁₀
1101 ₂	13 ₁₀	-(2 ³ -5) = -3 ₁₀

5.4.2

i_a	i_b	i_alu_ctrl	o_result	o_nzcv
4'b0100	4'b0100	2'b00	4'b1000	4'b1001

4'b1101	4'b0011	2'b00	4'b0000	4'b0110
4'b0100	4'b1010	2'b01	4'b1010	4'b1001
4'b0110	4'b1001	2'b10	4'b0000	4'b0100
4'b0110	4'b0101	2'b11	4'b0111	4'b0000

unsigned integer:

n ⇒ no meaning

z ⇒ zero

c ⇒ overflow in addition / subtraction

v ⇒ no meaning

signed integer:

n ⇒ negative

z ⇒ zero

c ⇒ no meaning

v ⇒ overflow in addition / subtraction

5.4.3

Addition

ADDS (immediate)

64-bit: ADDS <Xd>, <Xn | SP>, #<imm>{, <shift>}

32-bit: ADDS <Wd>, <Wn | WSP>, #<imm>{, <shift>}

Subtraction

SUBS (immediate)

64-bit: SUBS <Xd>, <Xn | SP>, #<imm>{, <shift>}

32-bit: SUBS <Wd>, <Wn | WSP>, #<imm>{, <shift>}

5.5.3

