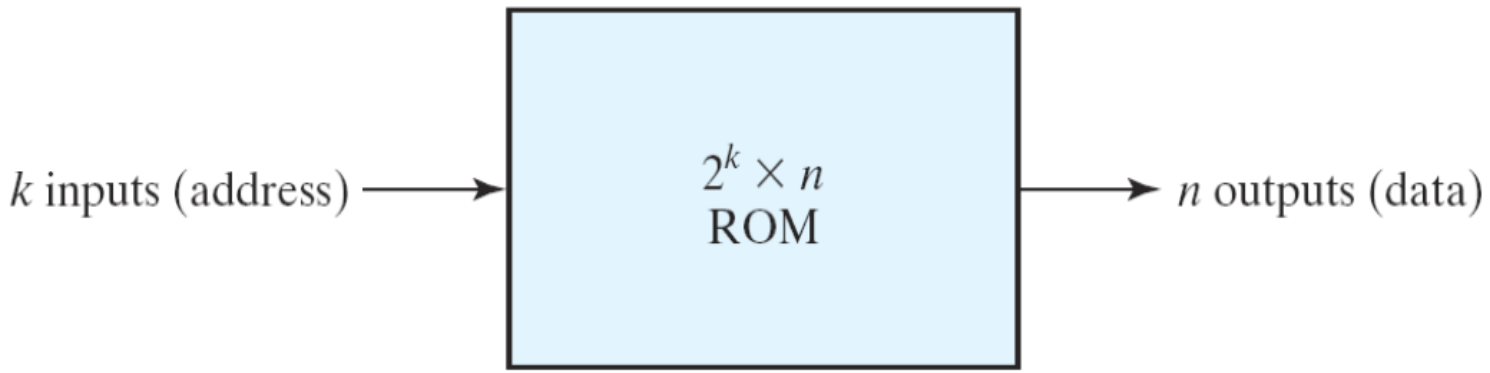
Chapter 7

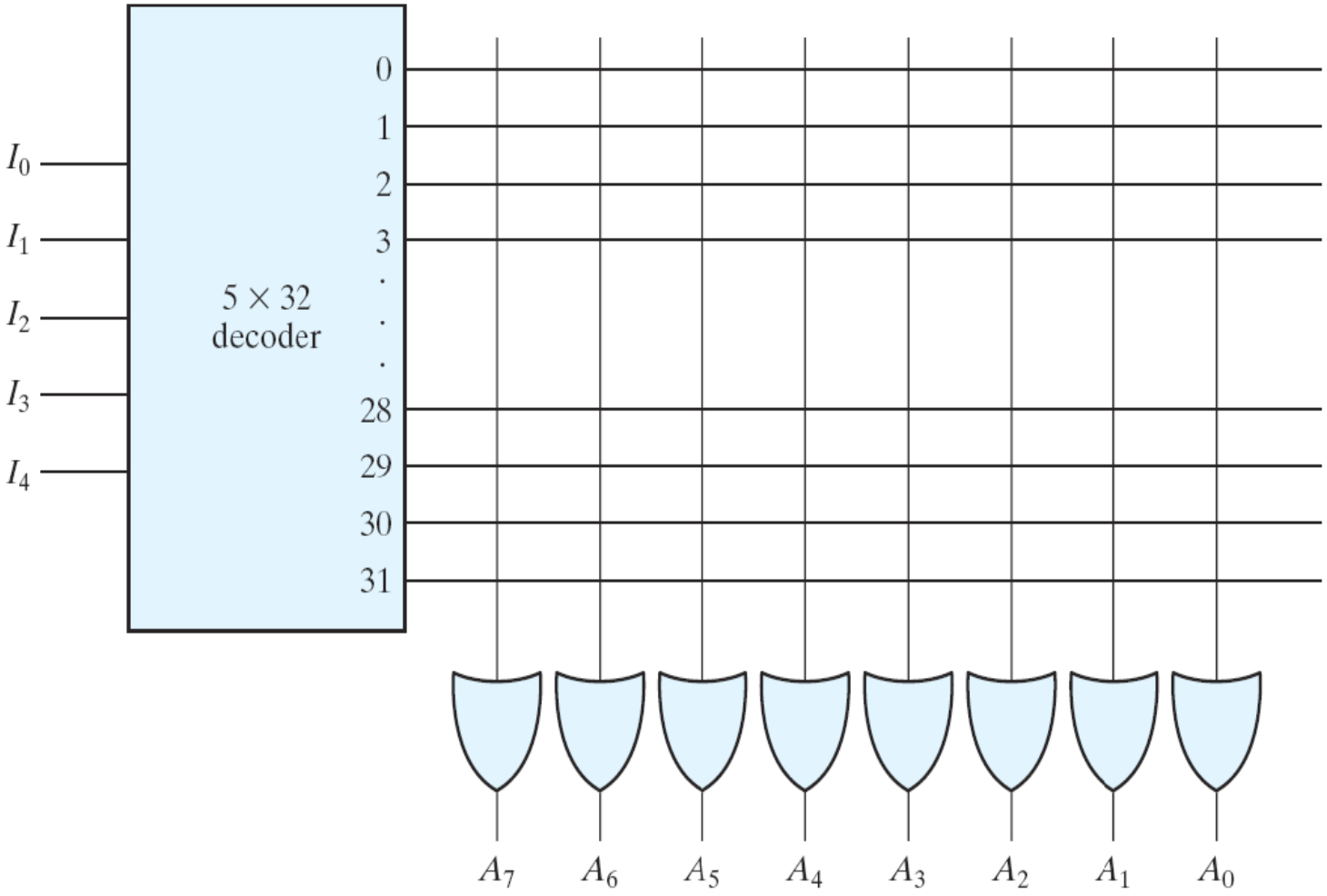
ROM, PLA, PAL, SPLD

Read Only Memory

- Permanent Storage
- Allows for configuration of devices to be stored on device without requiring load



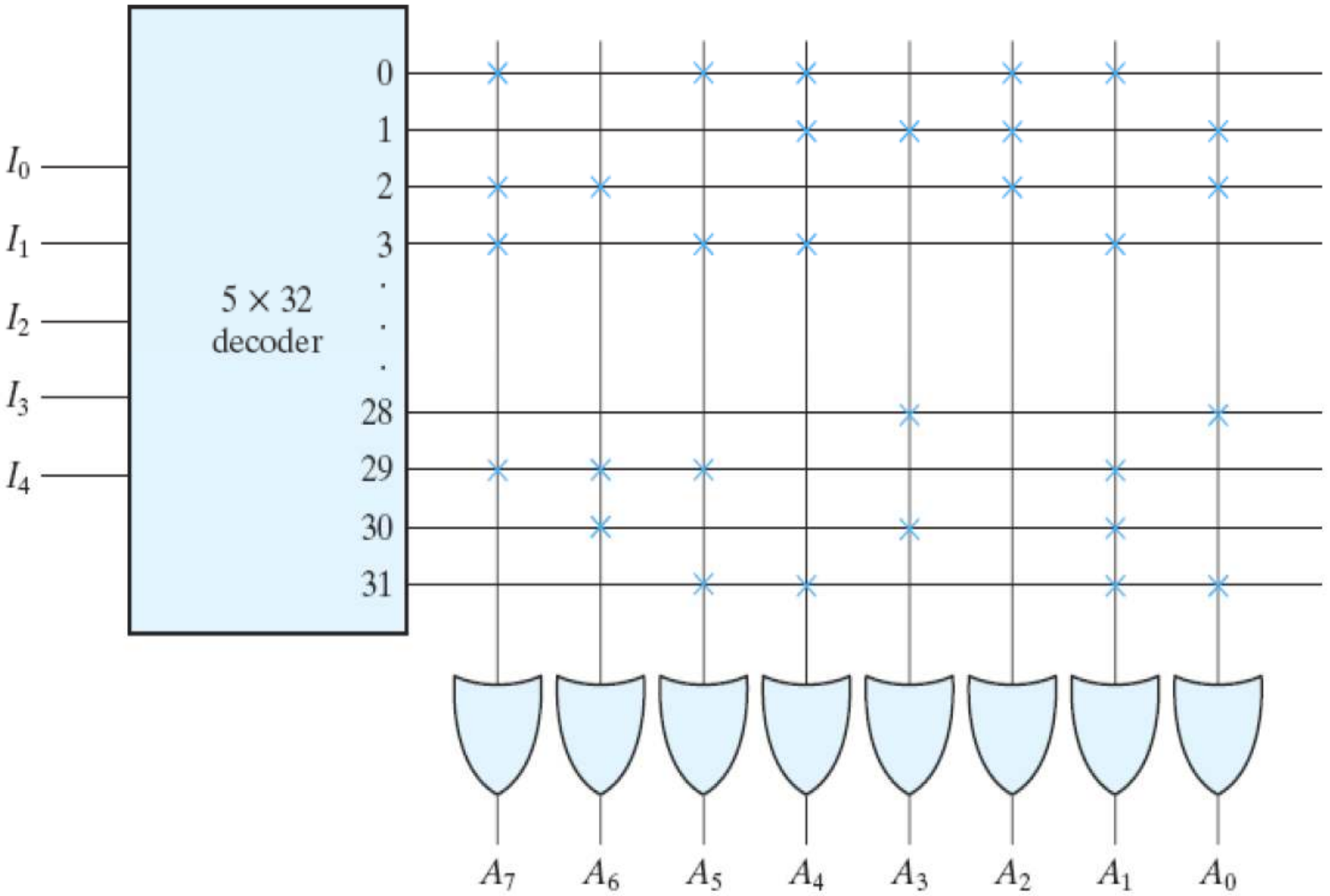
32x8 ROM



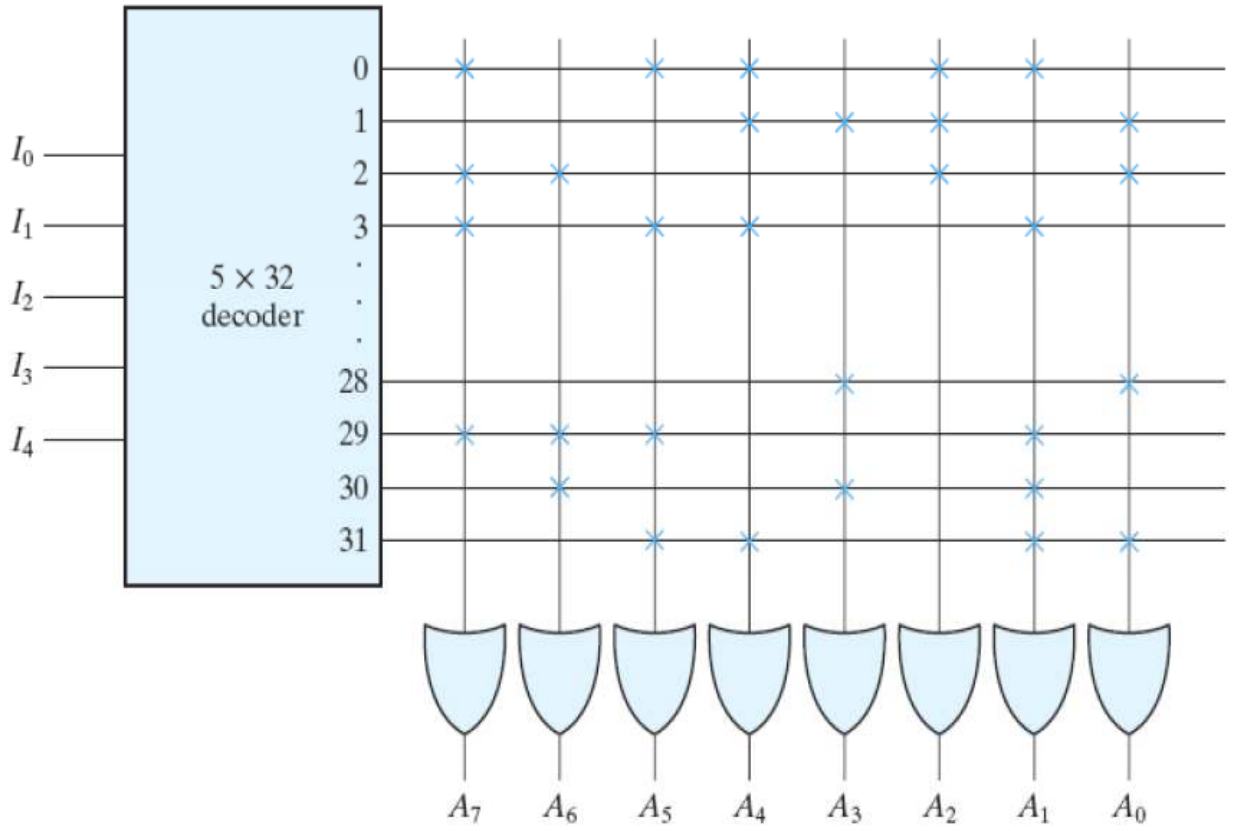
ROM Truth Table

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		⋮						⋮				
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Configured ROM



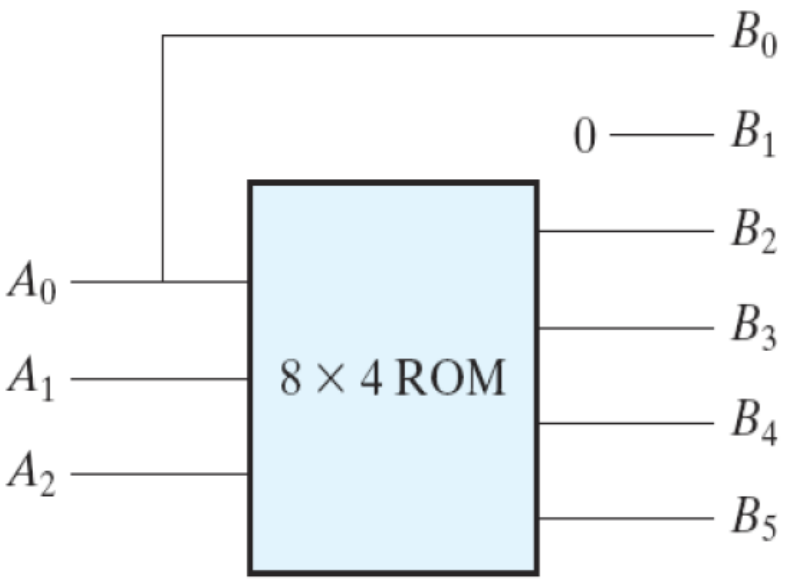
ROM as a Combinational Circuit



ROM 'Circuit' Example

Inputs			Outputs						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

ROM 'Circuit' Example



(a) Block diagram

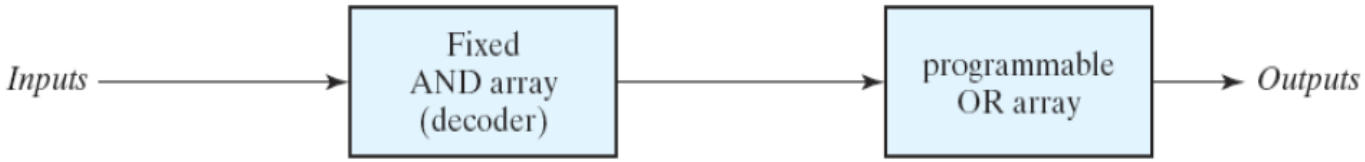
A_2	A_1	A_0	B_5	B_4	B_3	B_2
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

4 Types of ROMs

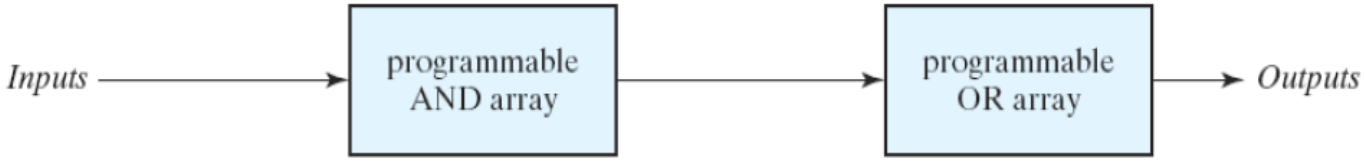
- Mask Programming
  - Done during the fab process
- Programmable ROM (PROM)
  - All fuses are intact (set to 1) and are ‘Blown’
- Erasable PROM (EPROM)
  - Ultraviolet light used to reprogram
- Electronically Erasable PROM (EEPROM)
  - Programmed connections can be erased via signal

Combinational PLDs



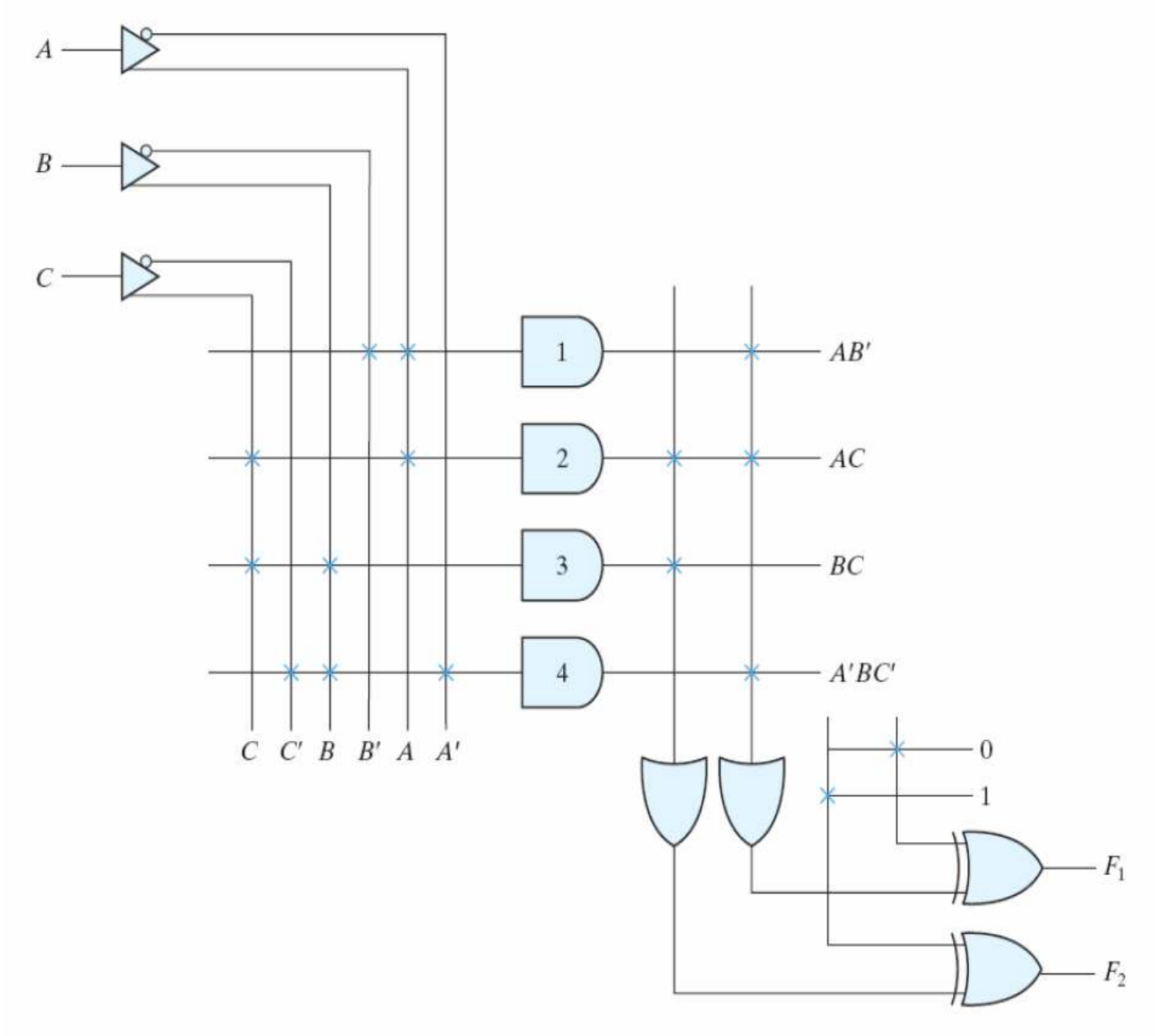
(a) Programmable read-only memory (PROM)

(b) Programmable array logic (PAL)



(c) Programmable logic array (PLA)

Programmable Logic Arrays



Programming PLAs

		Inputs			Outputs (T)	(C)
	Product Term	***A***	***B***	***C***	F_1	F_2
AB'	1	1	0	—	1	—
AC	2	1	—	1	1	1
BC	3	—	1	1	—	1
$A'BC'$	4	0	1	0	1	—

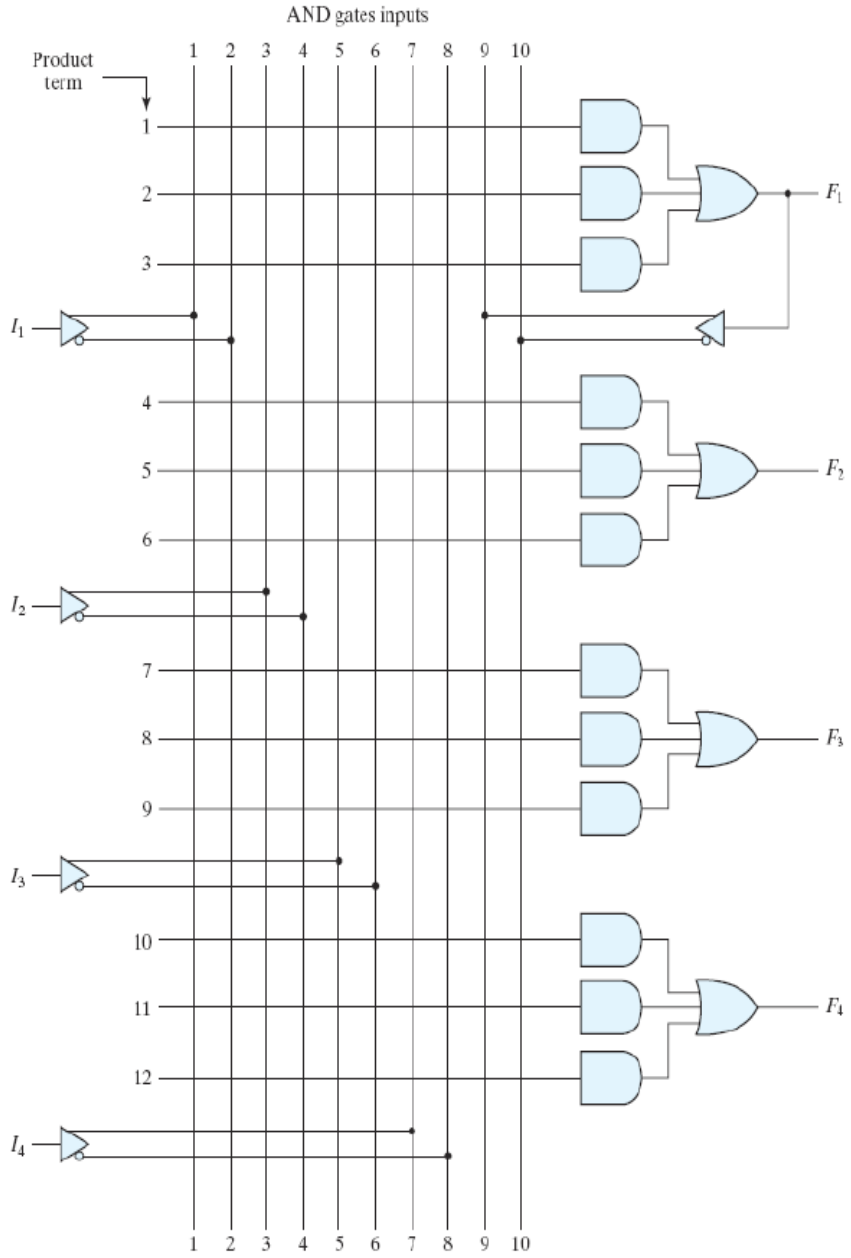
PLA Example

- $F_1(ABC) = Sum(0,1,2,4)$
- $F_2(ABC) = Sum(0,5,6,7)$

PLA programming table

Product term	Inputs			Outputs (C)	Outputs (T)
	A	B	C	F_1	F_2
AB				1	
AC				2	
BC				3	
$A'B'C'$				4	

Programmable Array Logic



Example

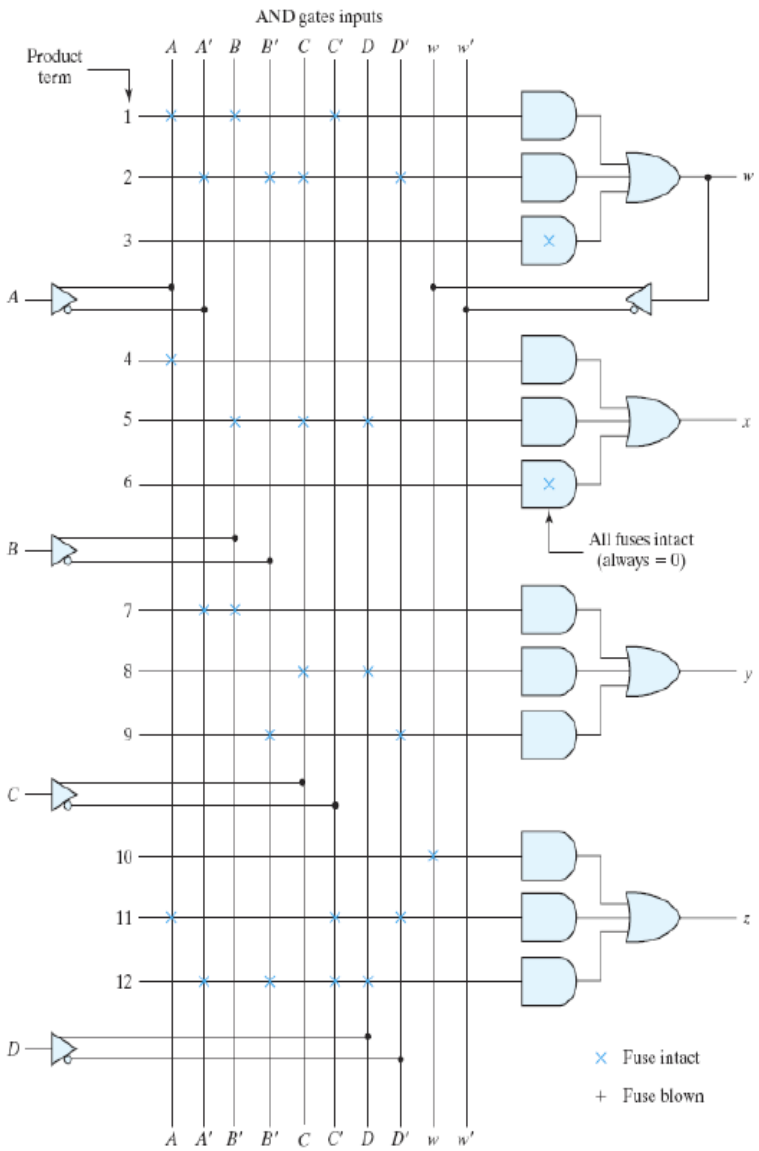
- X = A + BCD
- Y = A'B + CD + B'D'
- Z = ABC' + A'B'CD' + AC'D' + A'B'C'D

- W = ABC' + A'B'CD'
- Z = W + AC'D' + A'B'C'D

PAL Programming Table

	AND Inputs					
Product Term	***A***	***B***	***C***	***D***	***w***	**Outputs**
1	1	1	0	—	—	$w = ABC' + A'B'CD'$
2	0	0	1	0	—	
3	—	—	—	—	—	
4	1	—	—	—	—	$x = A + BCD$
5	—	1	1	1	—	
6	—	—	—	—	—	
7	0	1	—	—	—	$y = A'B + CD + B'D'$
8	—	—	1	1	—	
9	—	0	—	0	—	
10	—	—	—	—	1	$z = w + AC'D' + A'B'C'D$
11	1	—	0	0	—	
12	0	0	0	1	—	

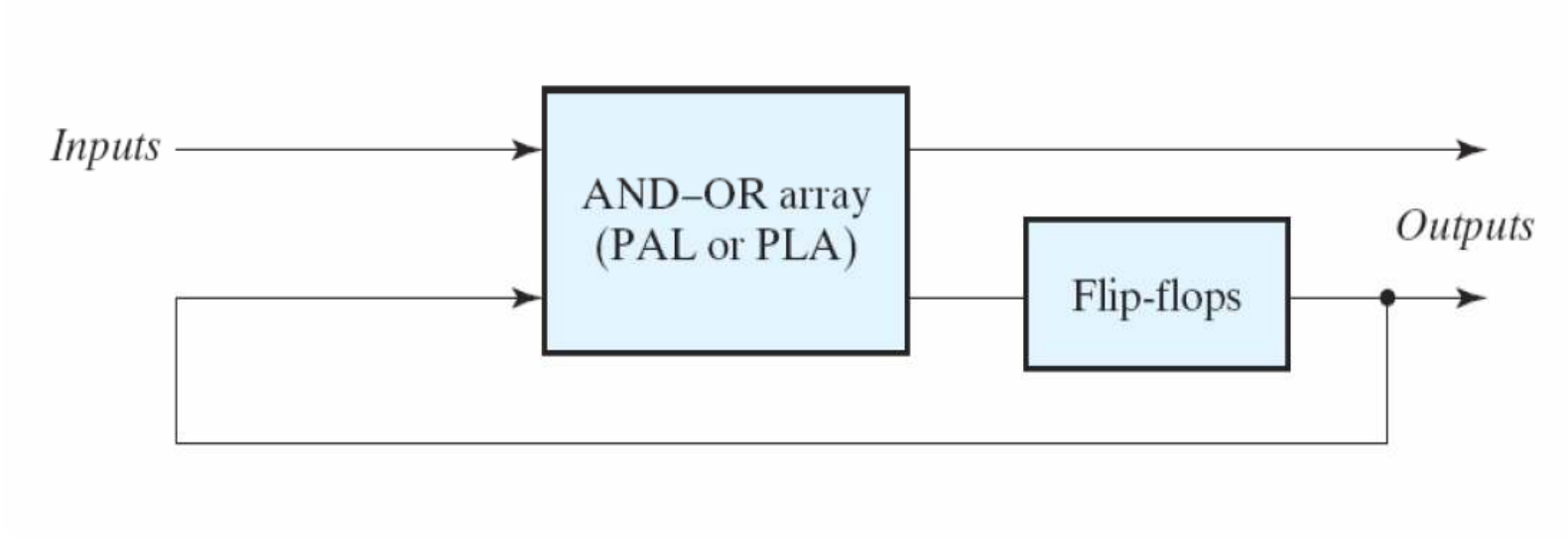
Configured PAL



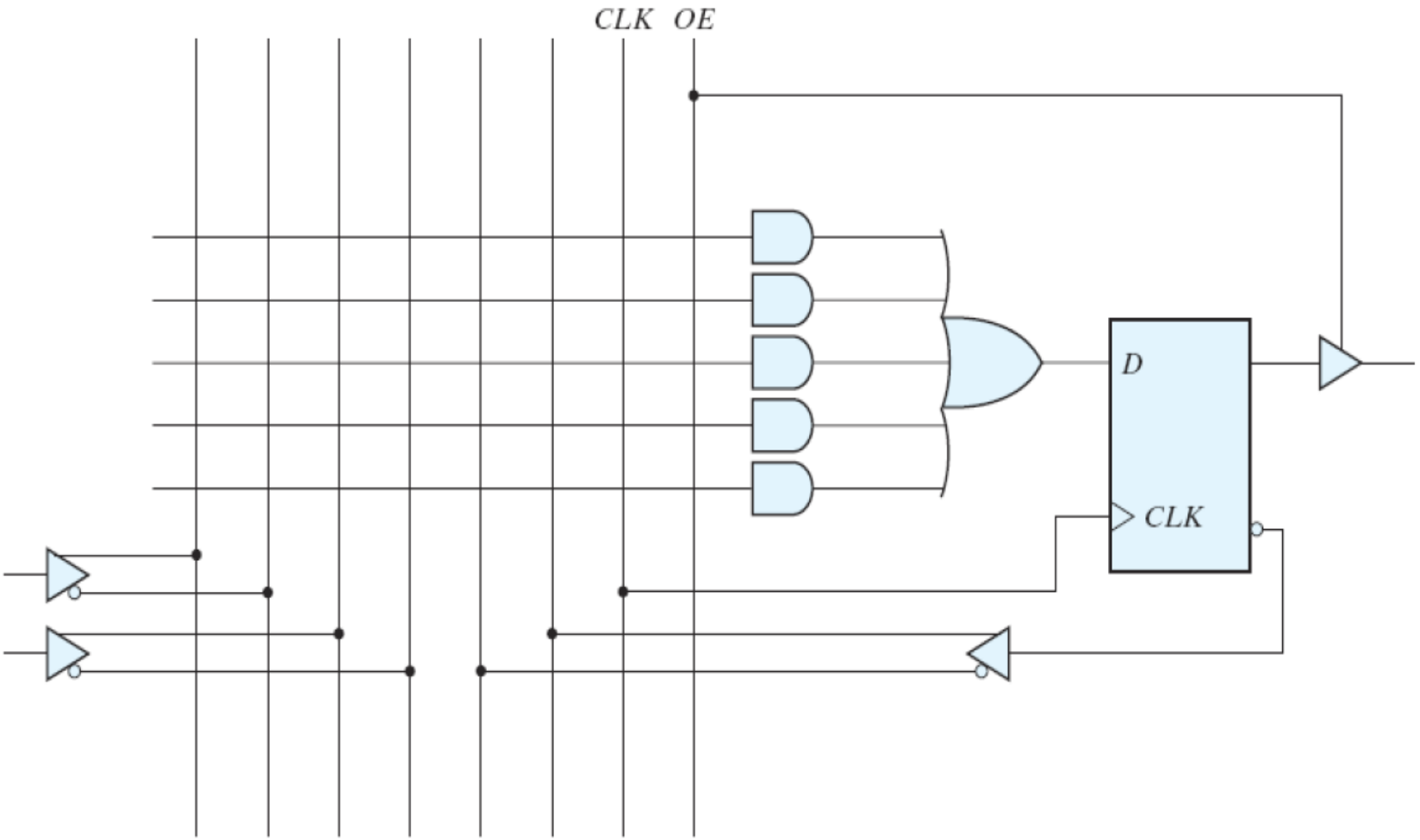
Sequential Programmable Devices

- Sequential Programmable Logic Device (SPLD)
- Complex Programmable Logic Device (CPLD)

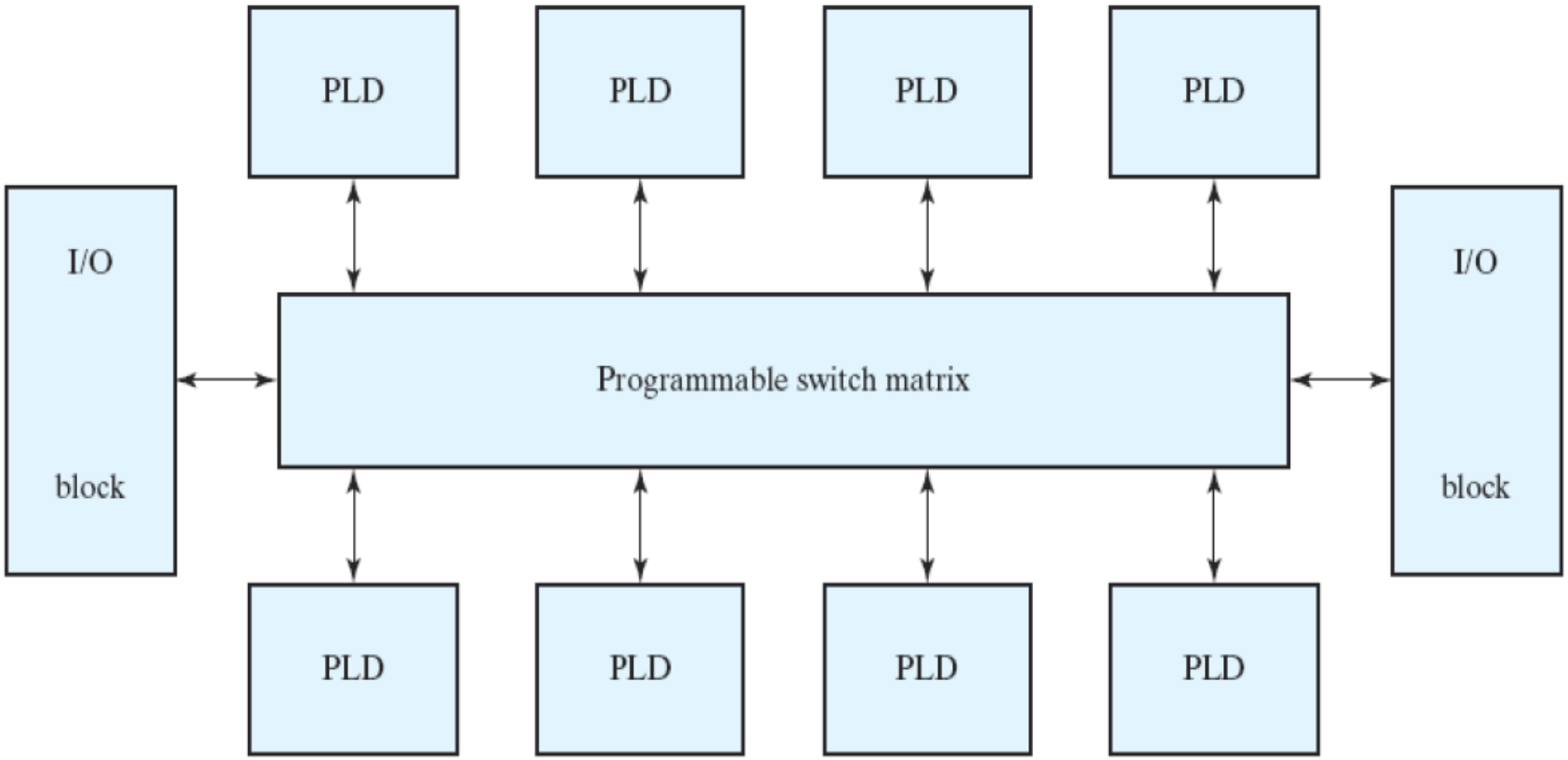
SPLDs



SPLD Macrocell



CPLD


PLD
PLD
PLD
PLD
I/O
block
Programmable switch matrix
I/O
block
PLD
PLD
PLD
PLD