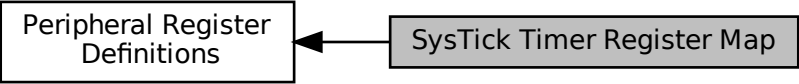


Peripheral Register
Definitions

SysTick Timer Register Map



```
graph LR; A[SysTick Timer Register Map] --> B[Peripheral Register Definitions];
```

The diagram consists of two rectangular boxes. The box on the left is white with a black border and contains the text 'Peripheral Register Definitions' in two lines. The box on the right is gray with a black border and contains the text 'SysTick Timer Register Map' in one line. A black arrow points from the right side of the gray box to the left side of the white box, indicating a relationship or flow from the SysTick Timer Register Map to the Peripheral Register Definitions.