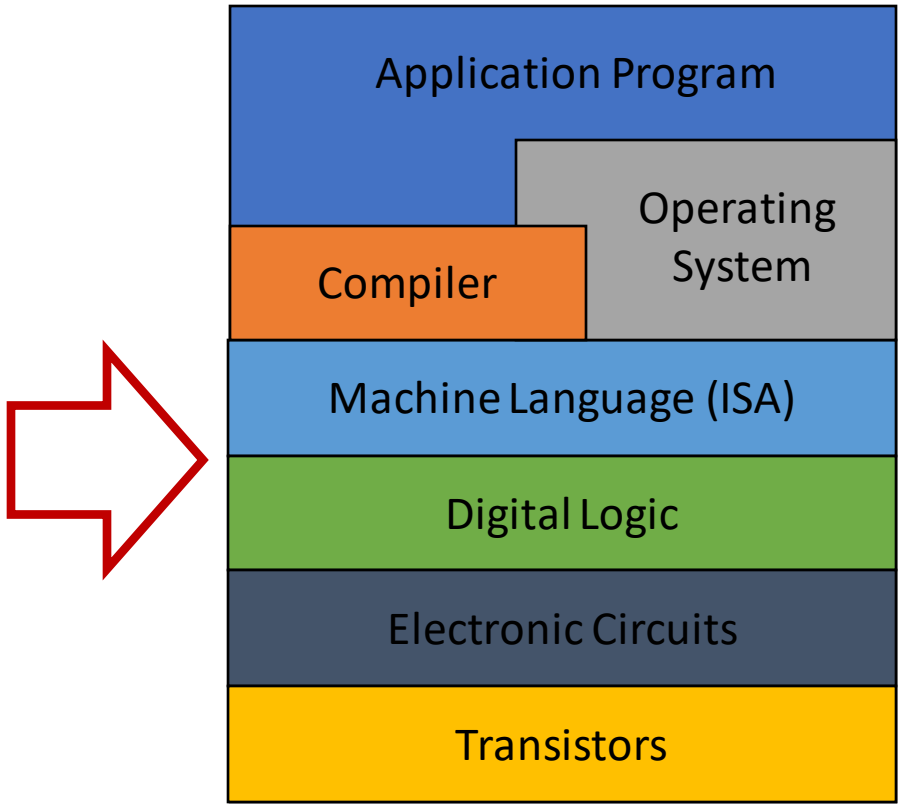
The LC-3 DataPath

EECS388 Fall 2022

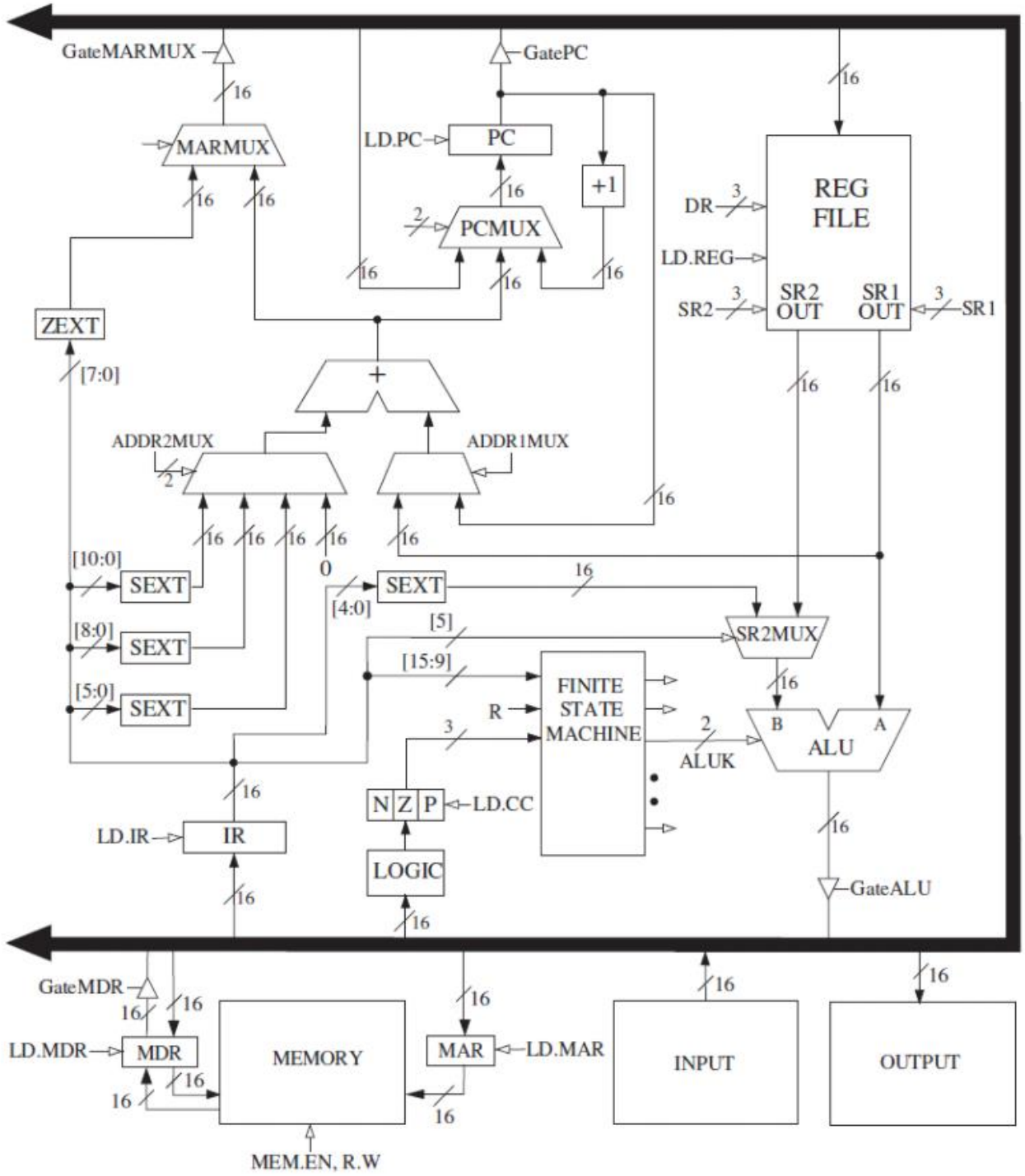
Context

- Recommended reading

Chapter 5 of “Introduction to Computing,” Patt, Patel



** Picture in the slides are in part taken from “Introduction to Computing From bits & gates to C and beyond” Patt, Patel


GateMARMUX
GatePC
16
MARMUX
LD.PC
PC
+1
PCMUX
2
DR
3
REG
FILE
LD.REG
SR2
SR2
OUT
SR1
OUT
SR1
ZEXT
[7:0]
+
ADDR2MUX
ADDR1MUX
[10:0]
SEXT
[8:0]
SEXT
[5:0]
SEXT
0
[4:0]
SEXT
[5]
SR2MUX
[15:9]
FINITE
STATE
MACHINE
R
3
2
ALUK
B
A
ALU
N
Z
P
LD.CC
LD.IR
IR
LOGIC
GateALU
GateMDR
LD.MDR
MDR
MEMORY
MAR
LD.MAR
INPUT
OUTPUT
MEM.EN, R.W

- Basic Components of LC-3 Datapath
  - The Global Bus
  - Memory
  - The ALU and Register File
  - The PC and the PCMUX
  - The MARMUX

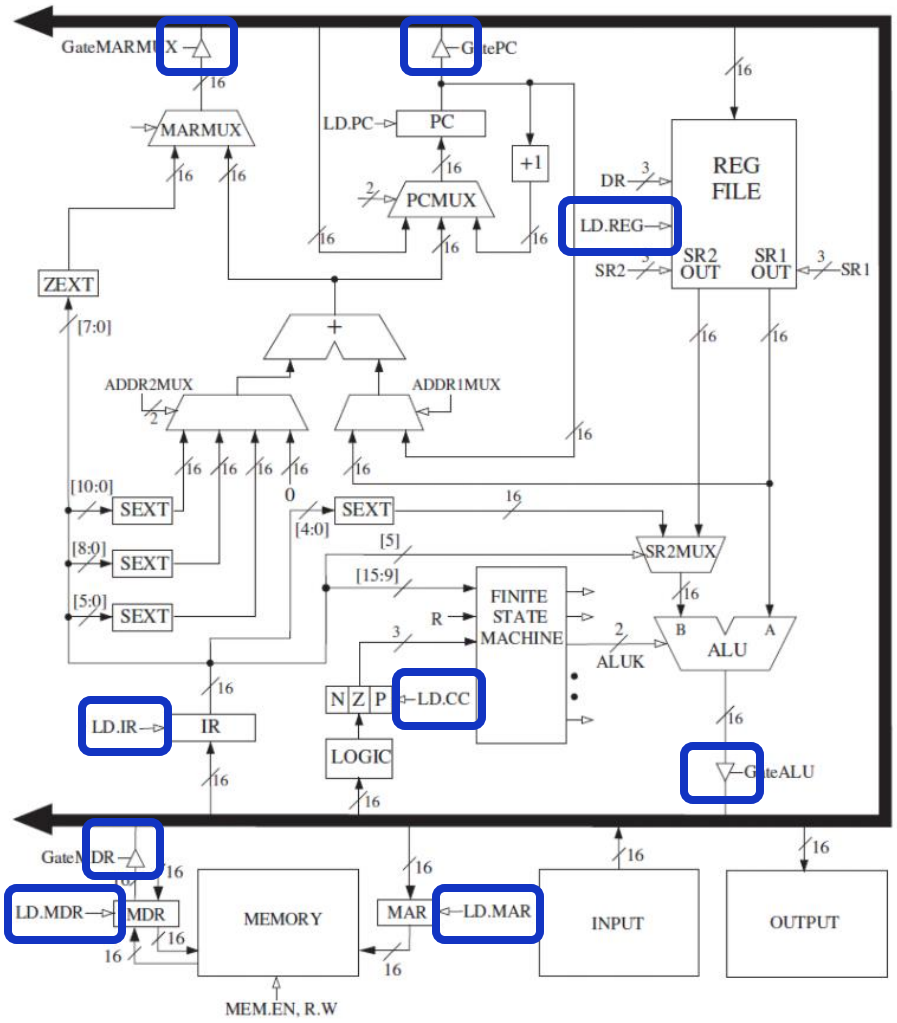
The Global Bus

- The thick arrow
  - 16bits wide

- Tristate device
  - Switch on/off
  - Allow only one supplier for the bus

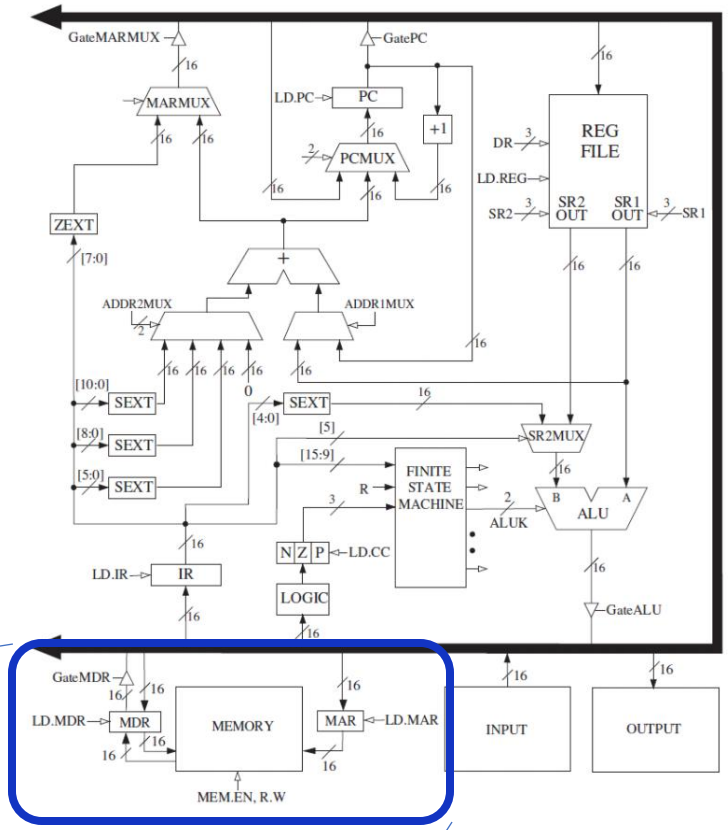
- Load from bus by LD.X signal

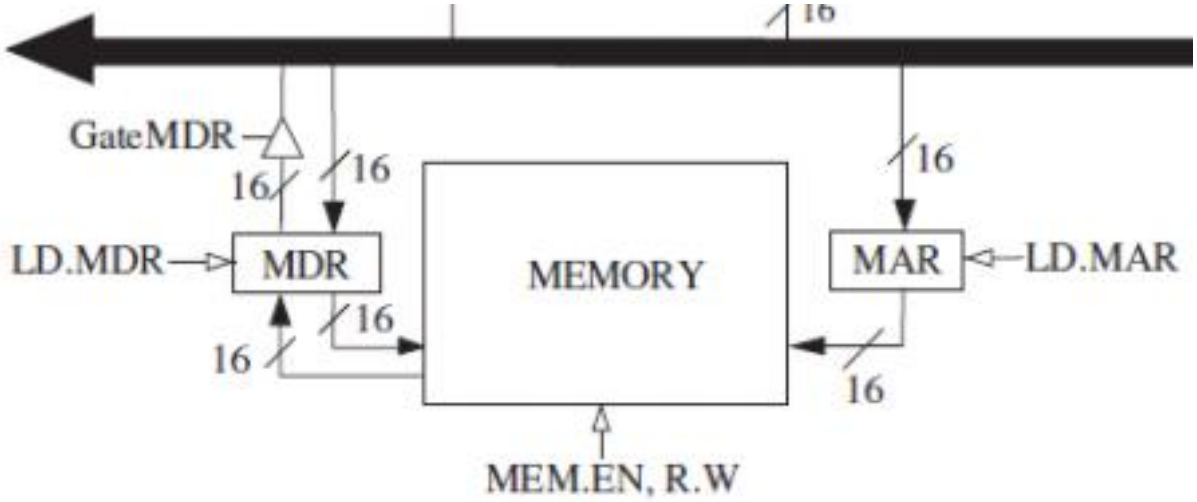
- Single shared bus vs. dedicated interconnect



Memory

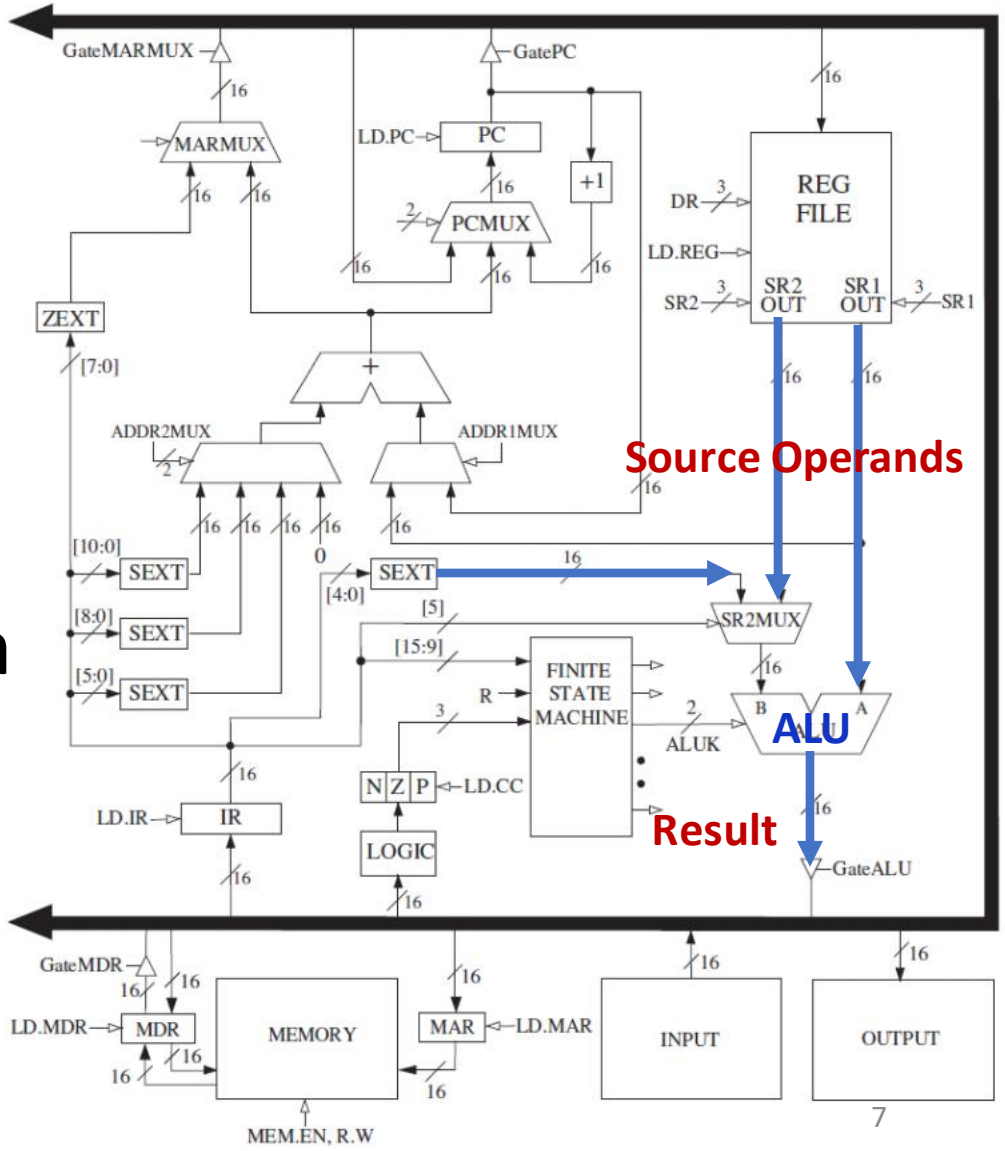
- Write to MAR
- Read/Write from/to MDR
- Tristate GateMDR





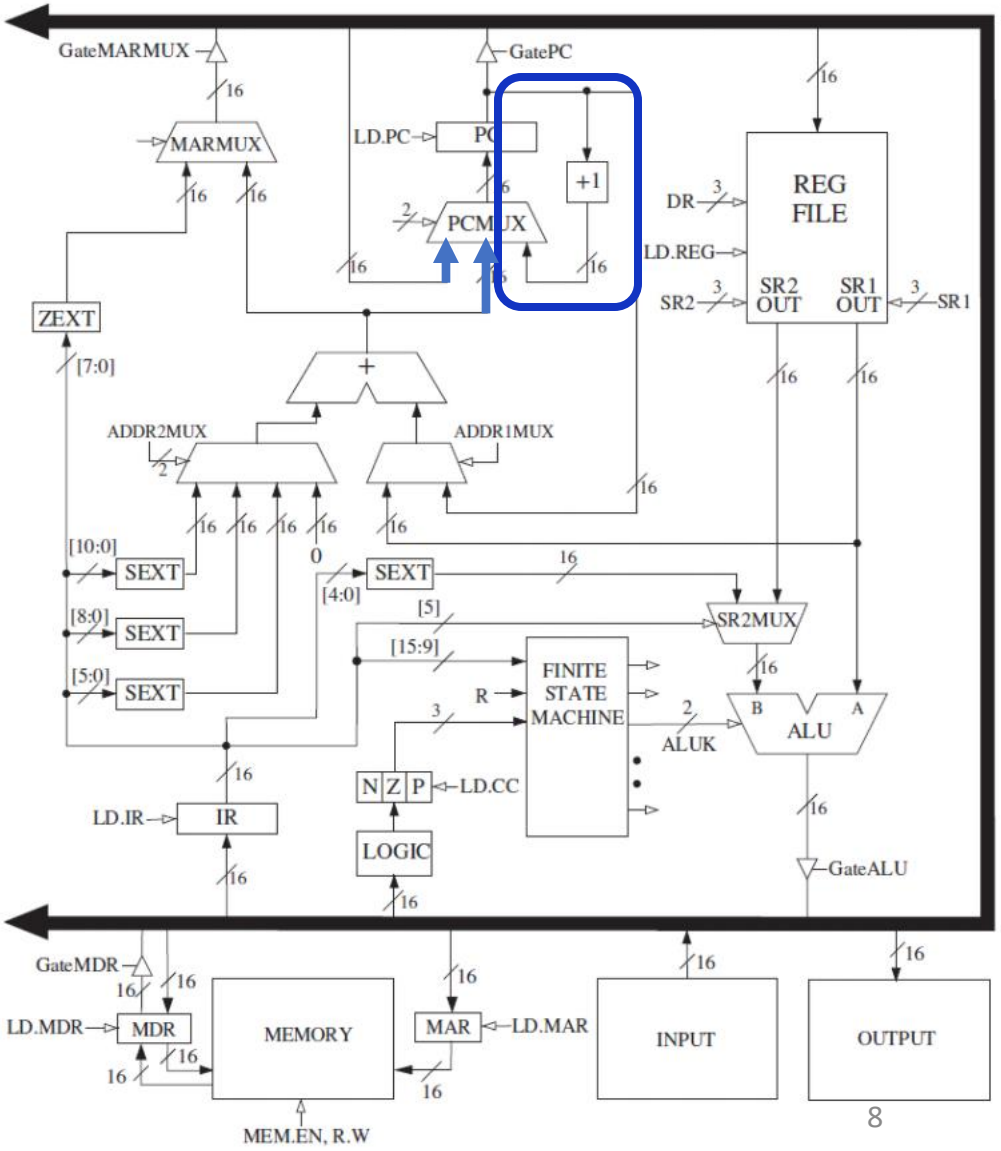
ALU and Reg File

- ALU sources
  - Register or SEXT
  - Controlled by IR[5]
- Condition codes
  - Comparator logic
- Control signals from FSM



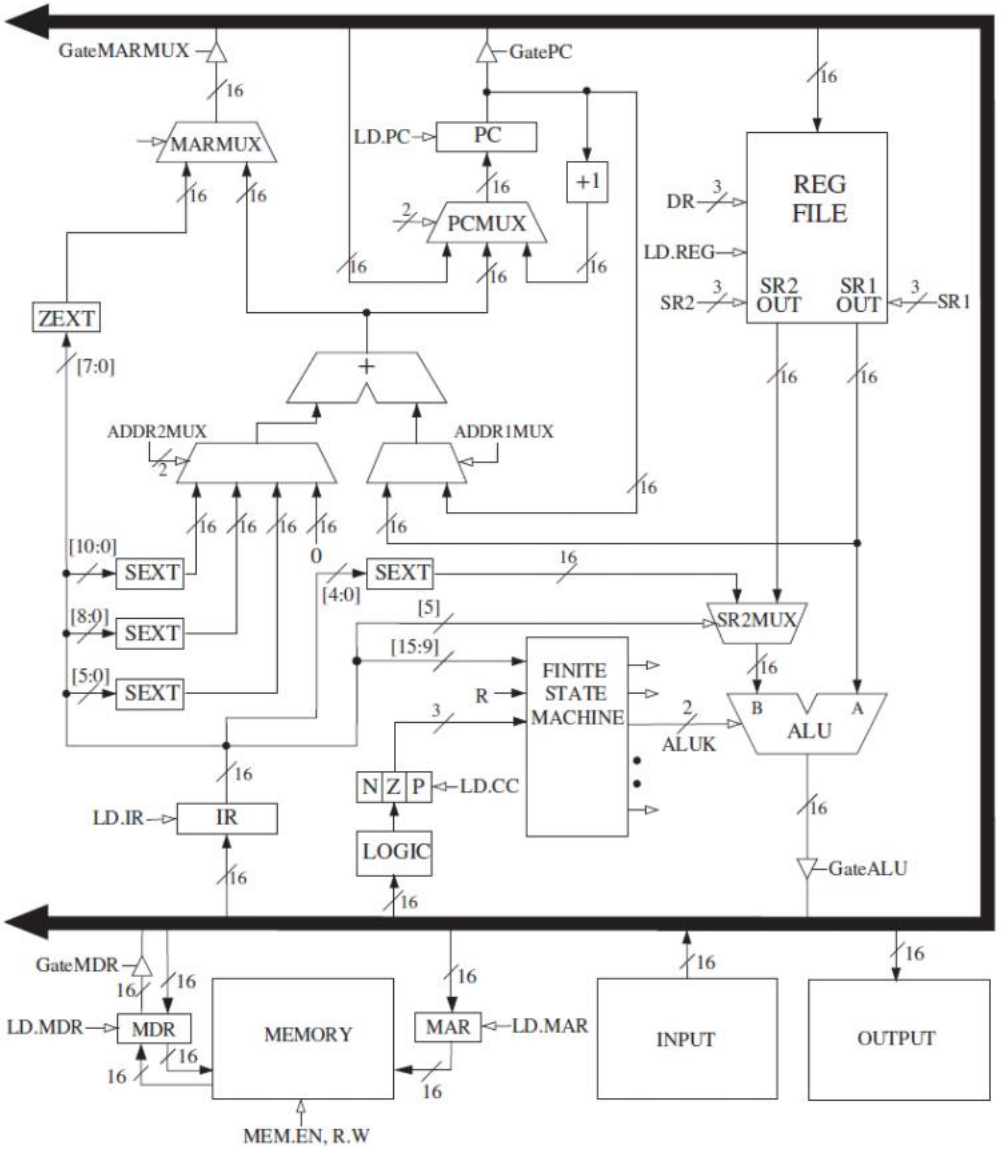
PC and PC MUX

- FETCH stage:
  - PC <- PC + 1
- Control instructions

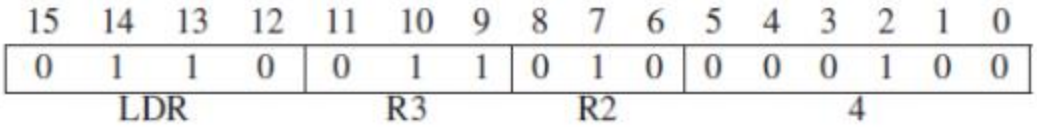


MARMUX

- Supply address for load/store/TRAP
- Memory addressing modes
  - PC-relative
  - Indirect
  - Base+offset

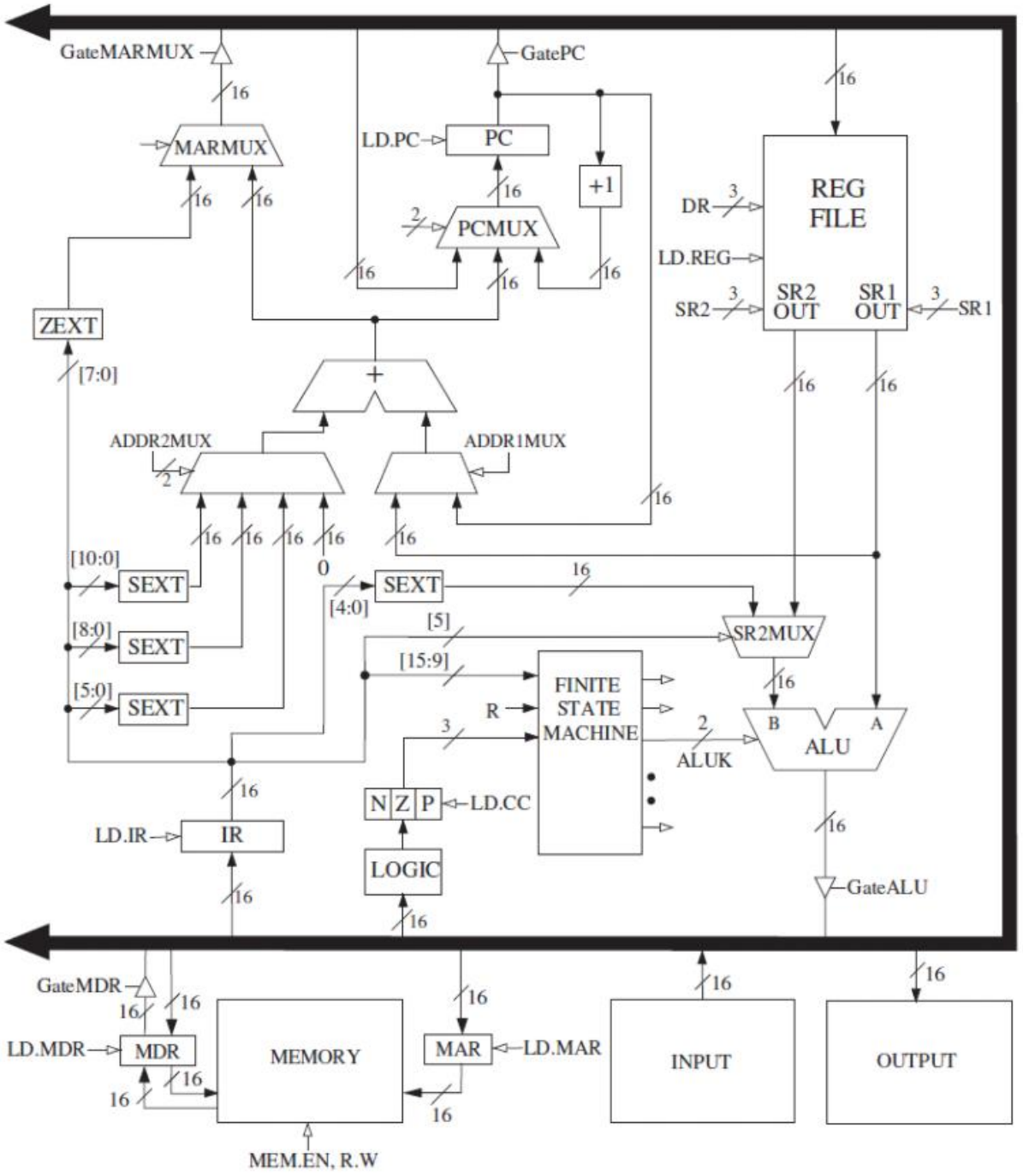


PC = 0x3456 0x3456:



Instruction Cycle in LC-3

- Fetch
  - Load IR
- Decode
- Evaluate Address
- Operand Fetch
- Execute
  - Not required
- Store Result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