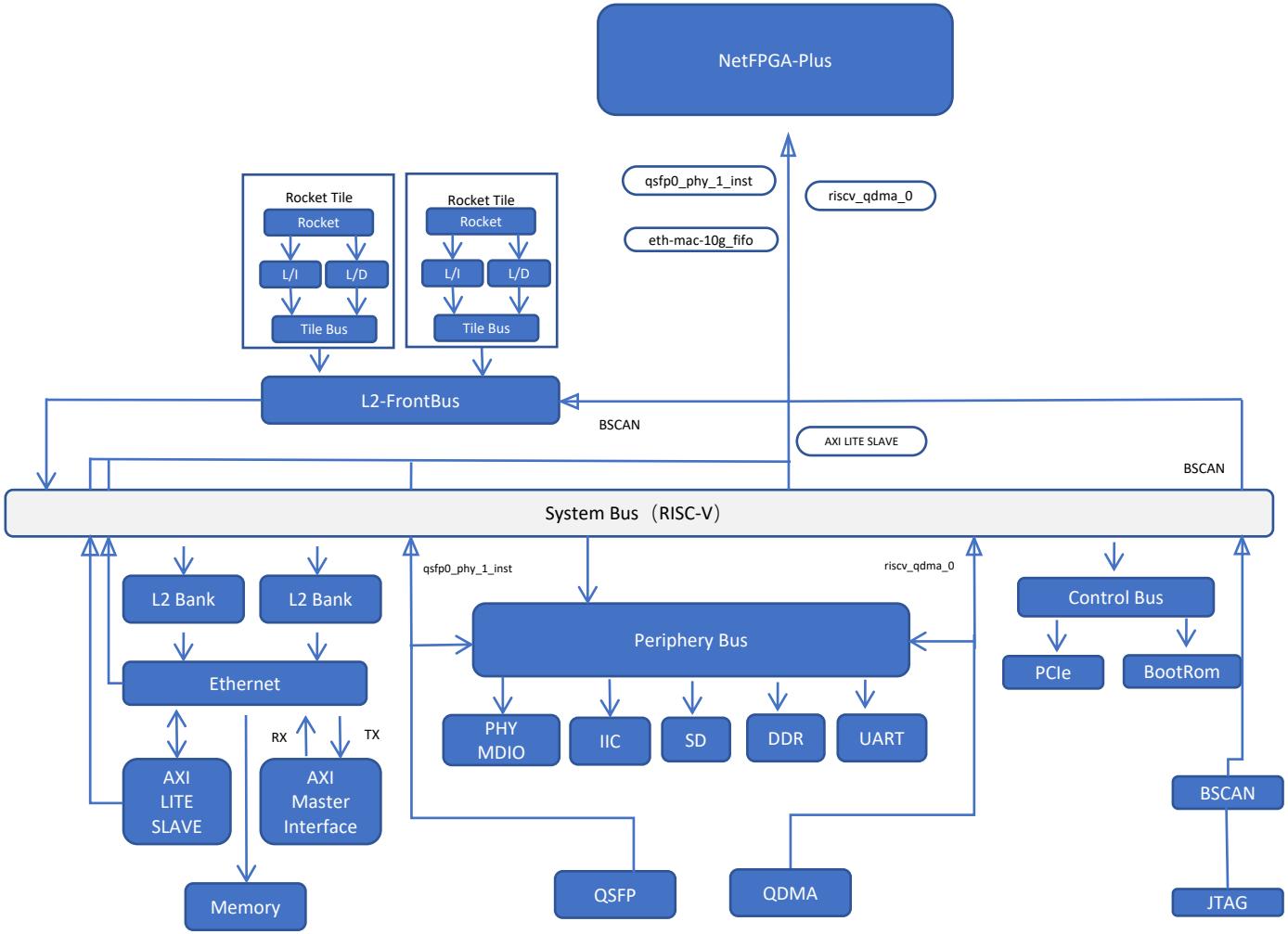
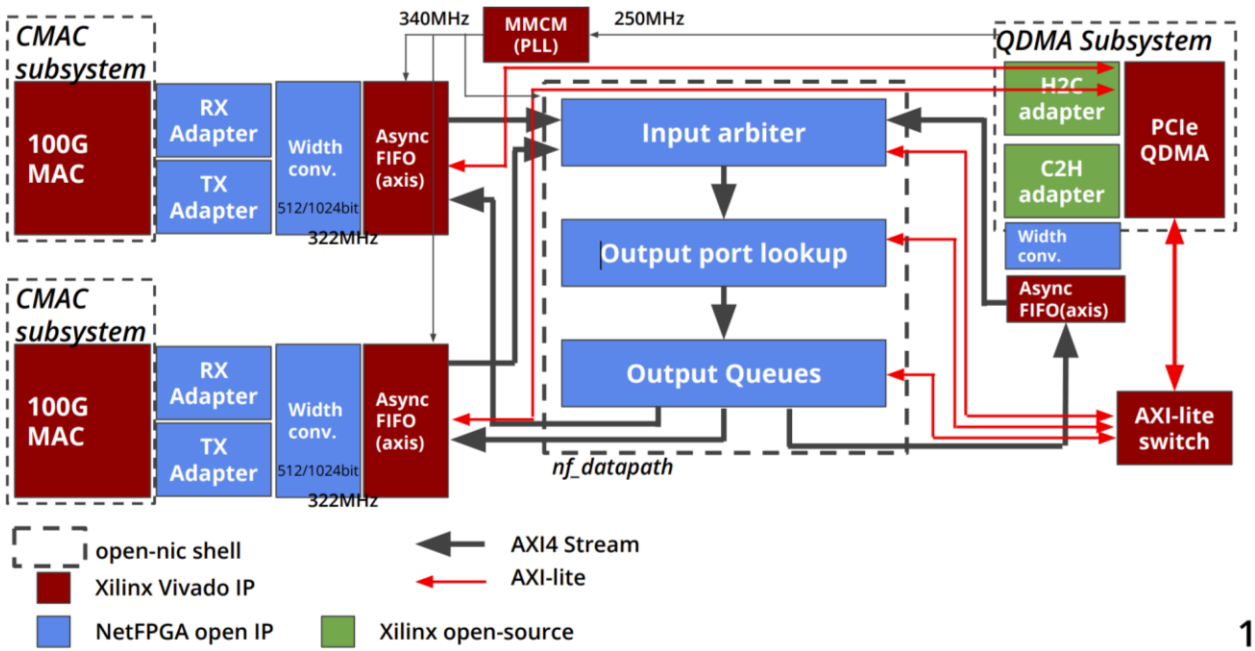
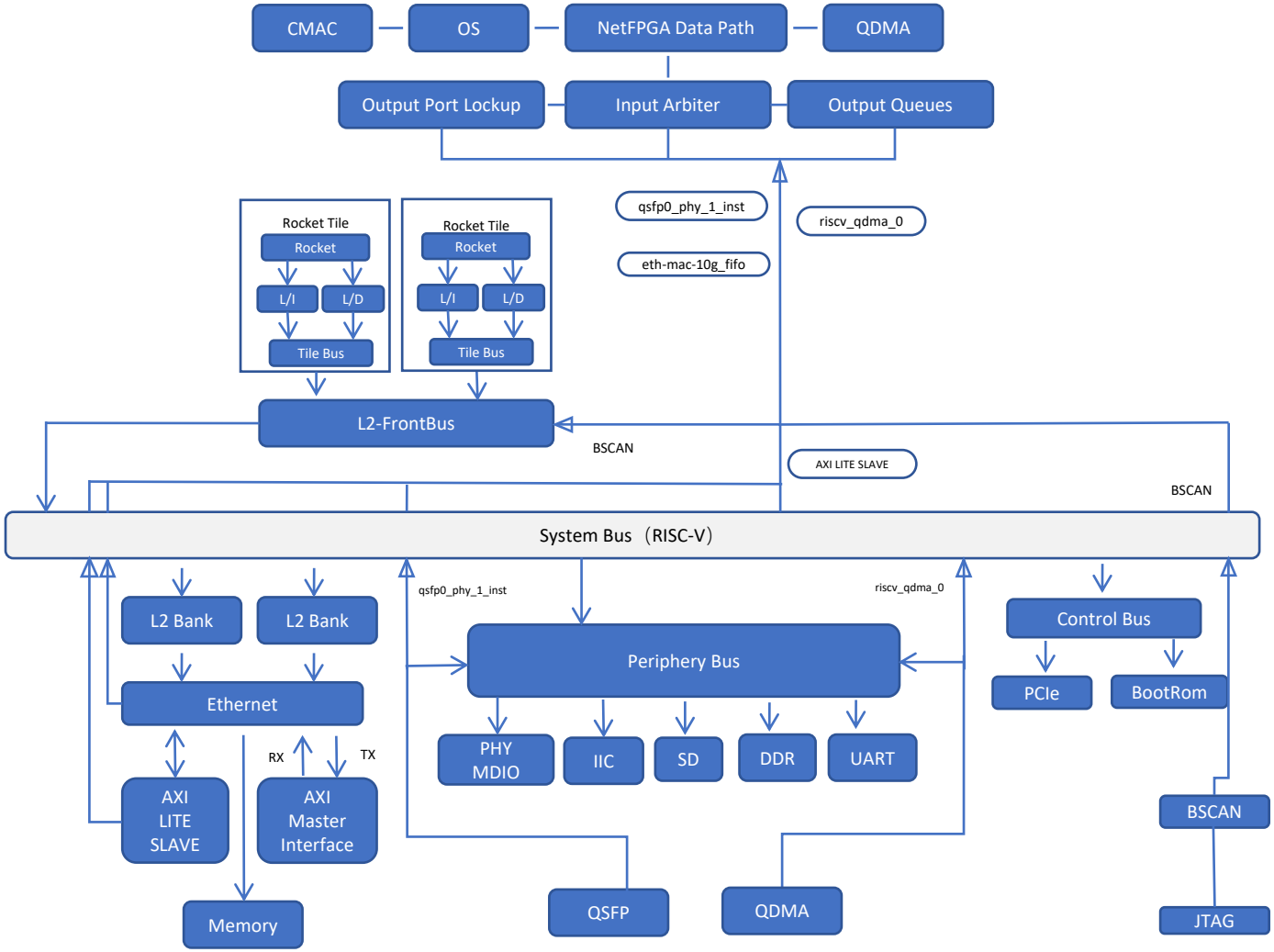

NetFPGA-Plus
qsfp0_phy_1_inst
riscv_qdma_0
eth-mac-10g_fifo
Rocket Tile
Rocket
L/I
L/D
Tile Bus
Rocket Tile
Rocket
L/I
L/D
Tile Bus
L2-FrontBus
BSCAN
AXI LITE SLAVE
BSCAN
System Bus（RISC-V）
L2 Bank
L2 Bank
Ethernet
RX
TX
AXI LITE SLAVE
AXI Master Interface
Memory
qsfp0_phy_1_inst
riscv_qdma_0
Periphery Bus
PHY MDIO
IIC
SD
DDR
UART
QSFP
QDMA
Control Bus
PCIe
BootRom
BSCAN
JTAG


CMAC subsystem
100G MAC
RX Adapter
TX Adapter
Width conv.
512/1024bit
322MHz
Async FIFO (axis)
340MHz
MMCM (PLL)
250MHz
QDMA Subsystem
H2C adapter
C2H adapter
Width conv.
Async FIFO(axis)
PCIe QDMA
Input arbiter
Output port lookup
Output Queues
nf_datapath
AXI-lite switch
open-nic shell
Xilinx Vivado IP
NetFPGA open IP
Xilinx open-source
AXI4 Stream
AXI-lite


CMAC
OS
NetFPGA Data Path
QDMA
Output Port Lockup
Input Arbiter
Output Queues
qsfp0_phy_1_inst
riscv_qdma_0
eth-mac-10g_fifo
Rocket Tile
Rocket
L/I
L/D
Tile Bus
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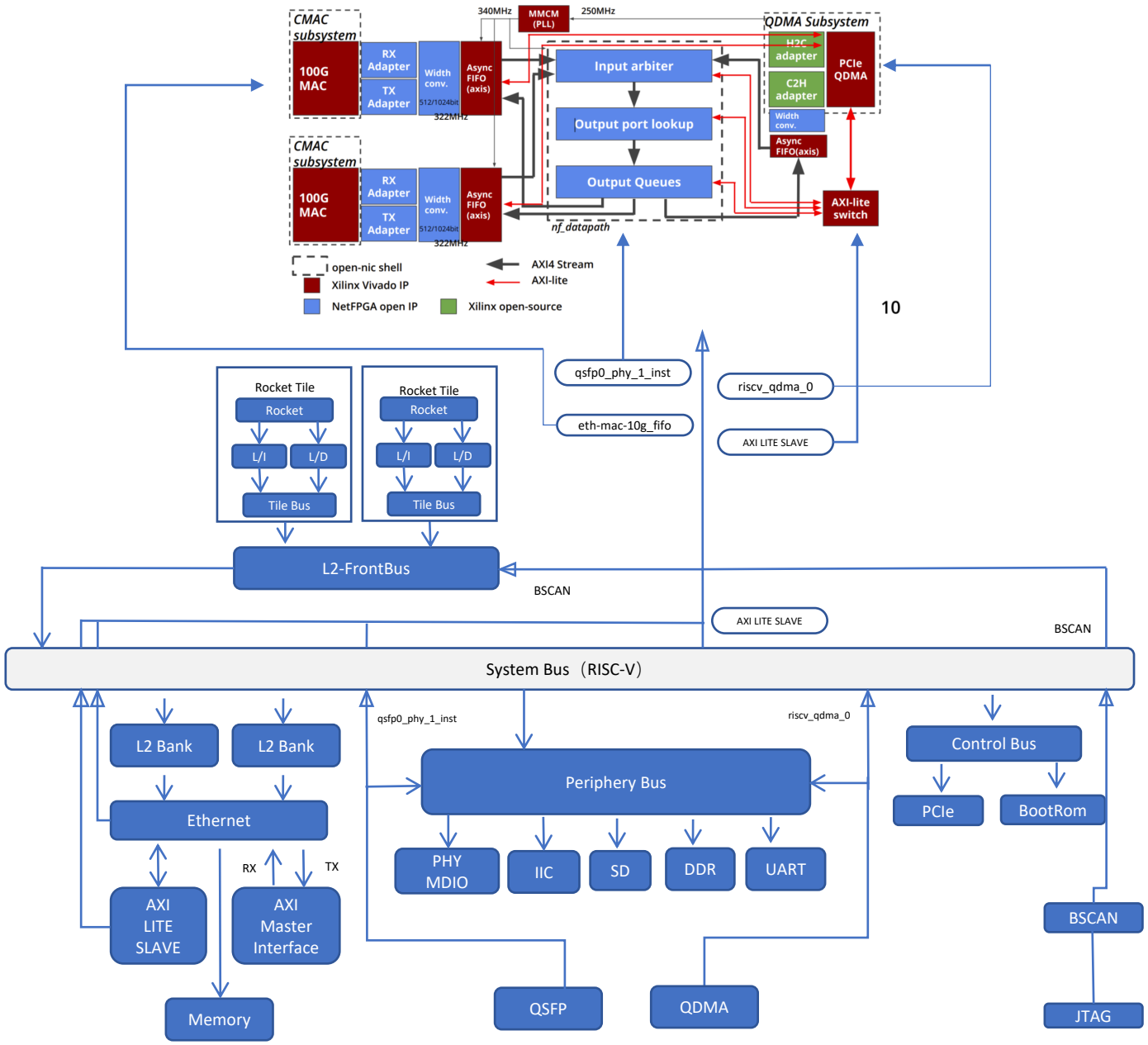
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