Logic Synthesis & Verification, Fall 2025

National Taiwan University

Programming Assignment 1

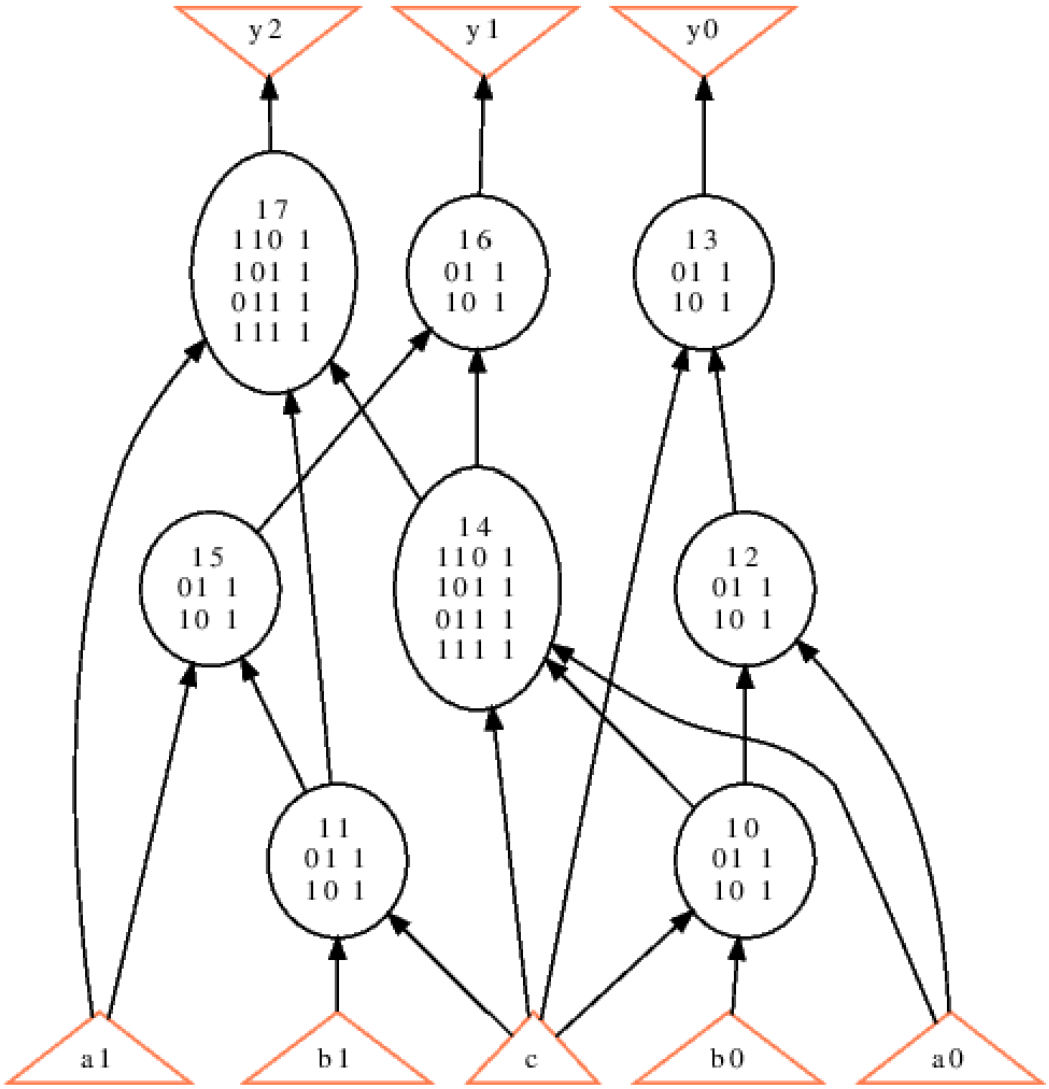
2 (b)

- read_blif、print_stats

```
abc 01> read alu.blif
abc 02> print_stats
alu                         : i/o =    5/    3  lat =    0  nd =     8  edge =     18  cube =    20  lev = 3
```

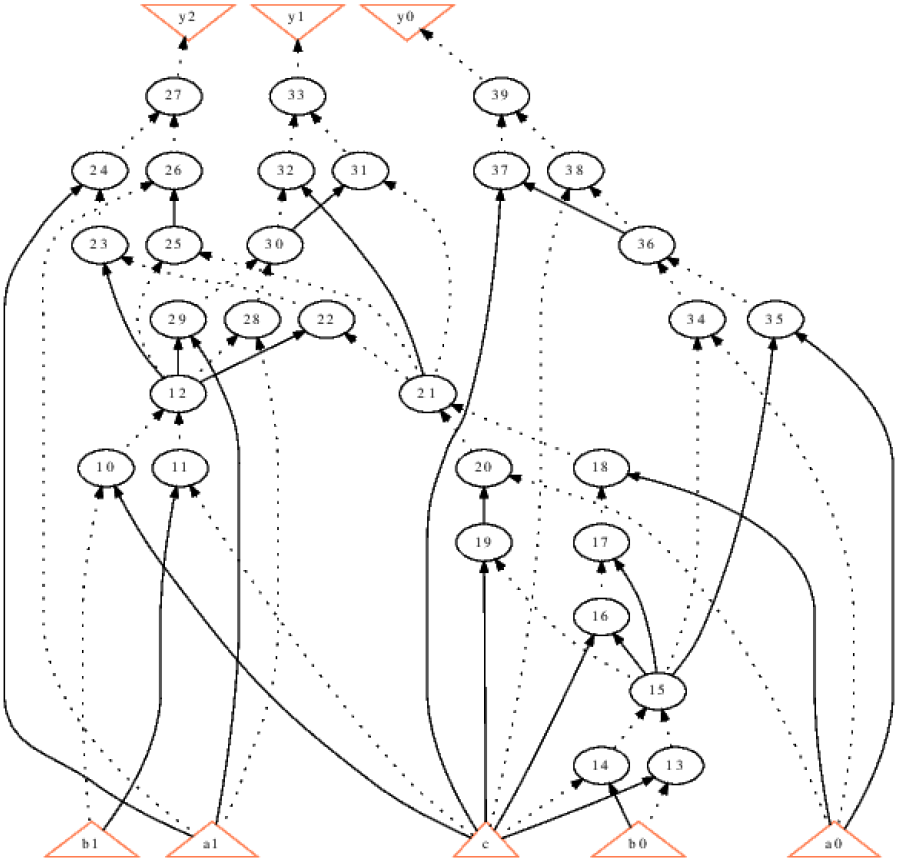
- show

The network contains 8 logic nodes and 0 latches.

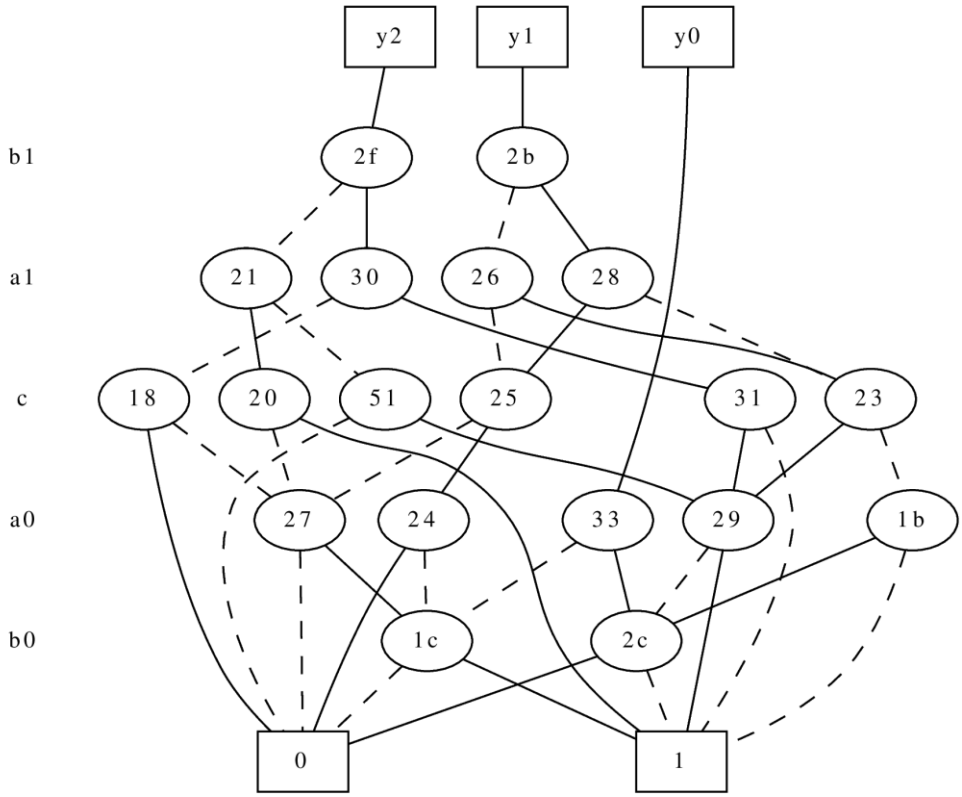


- strash、show

The network contains 30 logic nodes and 0 latches.



- collapse、show_bdd -g



3 (a)

1. After running aig, the circuit still contains SOP nodes, showing only 8 logic nodes with depth 3, and it only reports that 30 AND gates would be required if expanded.
   After running strash, the network is fully converted into an AIG with 30 AND nodes and depth 10.
   Therefore, aig provides a higher-level AIG view, while strash performs the full structural hashing to obtain the true AIG representation.

```
abc 11> read alu.blif
abc 12> aig
abc 12> print_stats
alu                         : i/o =    5/    3  lat =    0  nd =     8  edge =     18  aig  =    30  lev = 3
abc 12> strash
abc 13> print_stats
alu                         : i/o =    5/    3  lat =    0  and =     30  lev = 10
```

2. bdd produces separate BDDs, while collapse creates a collapsed BDD with reduced size and depth.

```
abc 13> read alu.blif
abc 14> bdd
abc 14> print_stats
alu                         : i/o =    5/    3  lat =    0  nd =     8  edge =     18  bdd  =    20  lev = 3
abc 14> collapse
abc 15> print_stats
alu                         : i/o =    5/    3  lat =    0  nd =     3  edge =     12  bdd  =    18  lev = 1
```

3 (b)

read alu.blif; strash; collapse; sop

```
abc 15> read alu.blif
abc 16> print_stats
alu                         : i/o =    5/    3  lat =    0  nd =     8  edge =     18  cube =    20  lev = 3
abc 16> strash
abc 17> print_stats
alu                         : i/o =    5/    3  lat =    0  and =     30  lev = 10
abc 17> collapse
abc 18> print_stats
alu                         : i/o =    5/    3  lat =    0  nd =     3  edge =     12  bdd  =    18  lev = 1
abc 18> sop
abc 18> print_stats
alu                         : i/o =    5/    3  lat =    0  nd =     3  edge =     12  cube =    19  lev = 1
```

The network contains 3 logic nodes and 0 latches.