Logic Synthesis & Verification PA1

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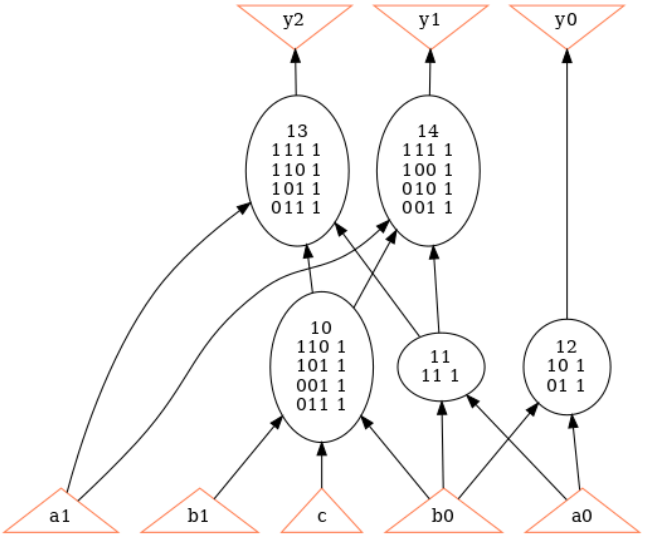
2. (b)

```
abc 01> read ./lsv/pa1/alu.blif
abc 02> print_stats
alu                            : i/o =    5/    3  lat =    0  nd =     5  edg
e =     13  cube =    15  lev = 2
```

```
abc 02> show
```

Network structure visualized by ABC
Benchmark "alu". Time was Wed Sep 10 14:28:46 2025.

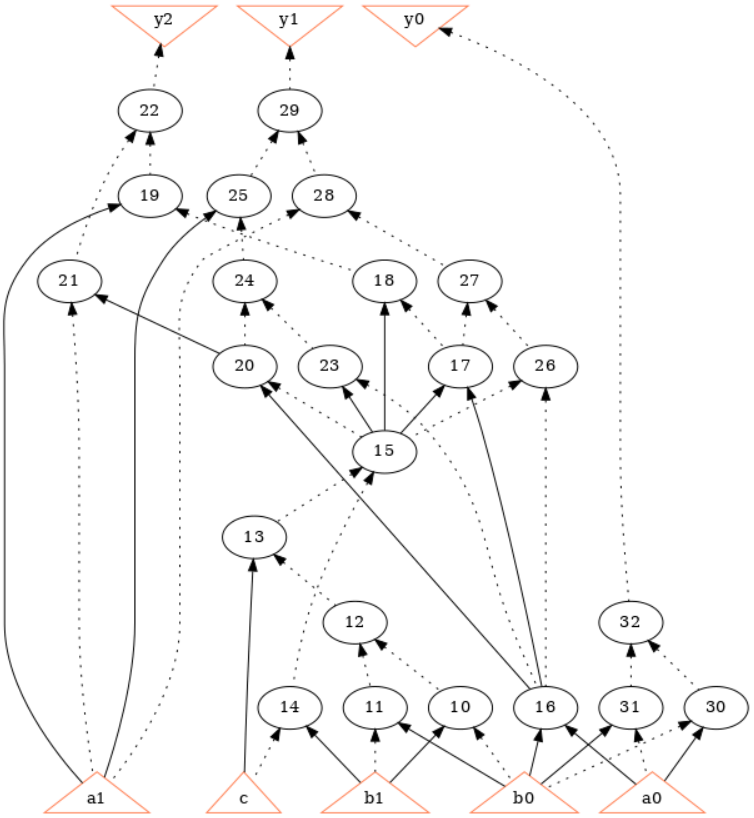
The network contains 5 logic nodes and 0 latches.



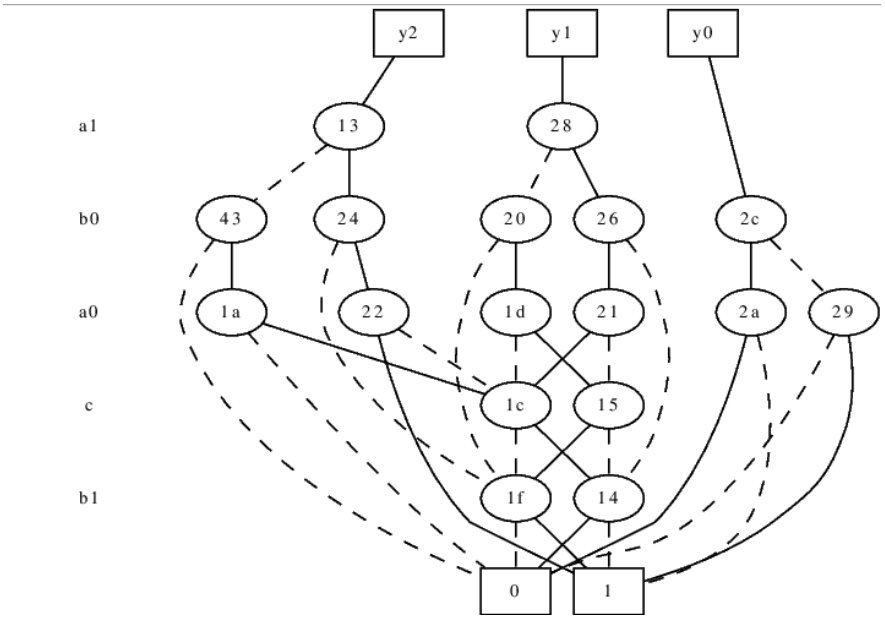
```
abc 02> strash
abc 03> show
```

Network structure visualized by ABC
Benchmark "alu". Time was Wed Sep 10 14:30:27 2025.

The network contains 23 logic nodes and 0 latches.




```
abc 03> collapse
abc 04> show_bdd
```

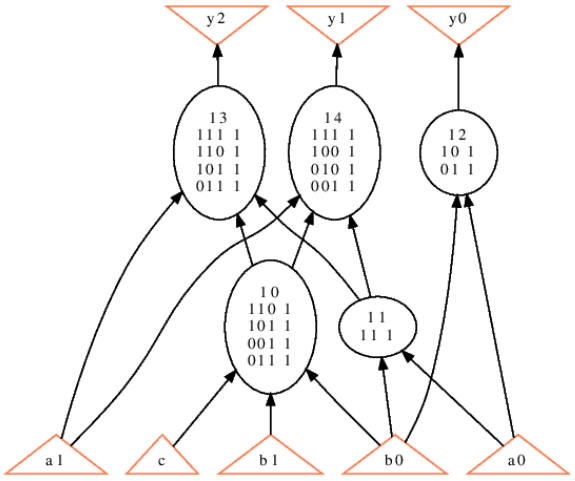


3. (a)

1.

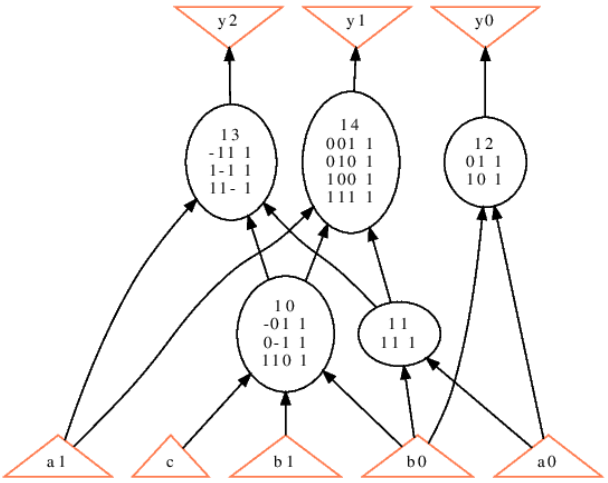
- read .blif (logic network)

The network contains 5 logic nodes and 0 latche



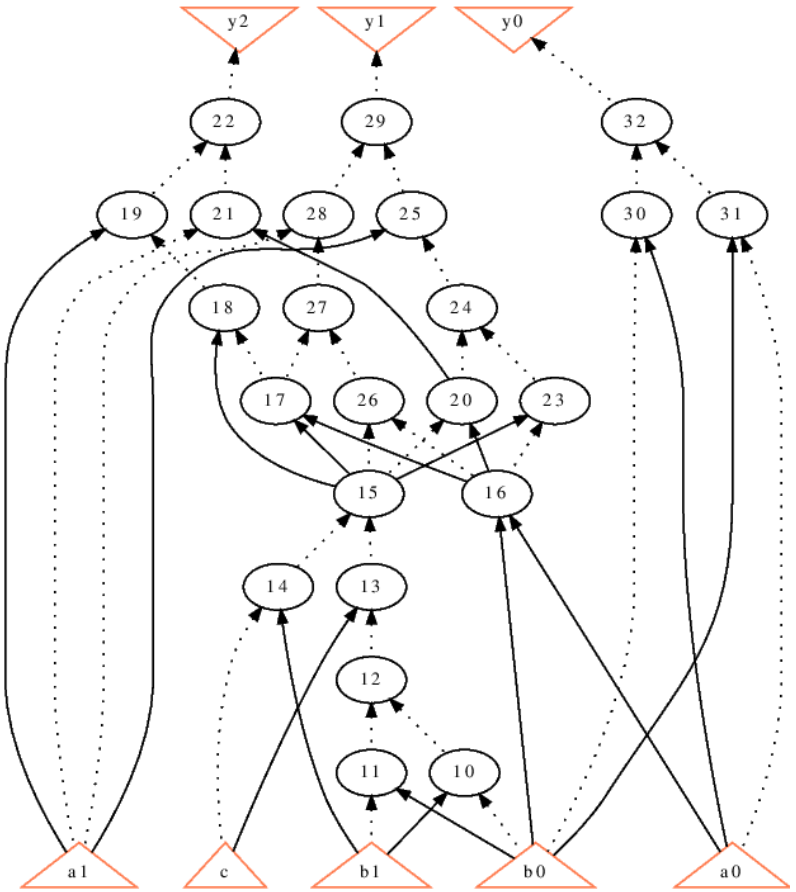
- aig (logic network in AIG)

The network contains 5 logic nodes and 0 latche



- strash (structurally hashed AIG)

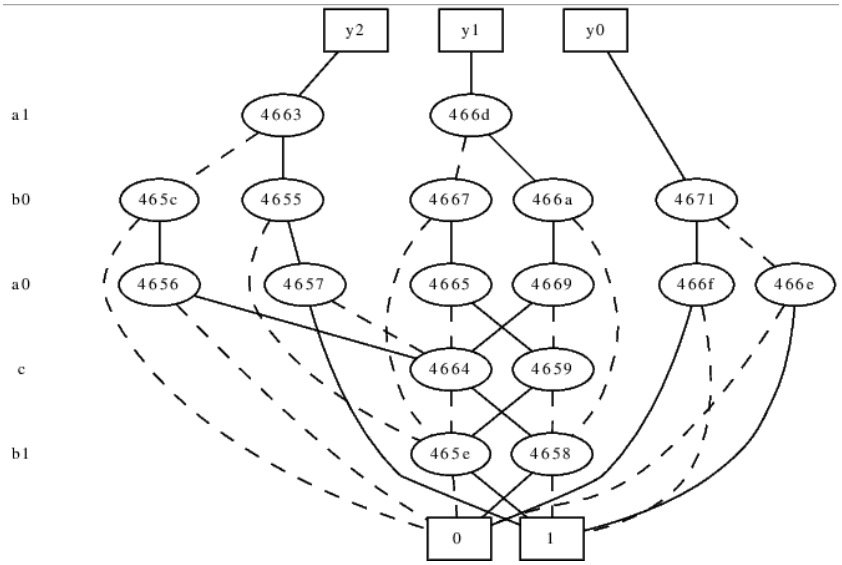
The network contains 23 logic nodes and 0 latches.



When we use the “aig” command, it just simplifies some nodes, but keeps the logic structure. As for “strash” command, it rebuilds an equivalent AIG with only AND gates and INV gates.

2.

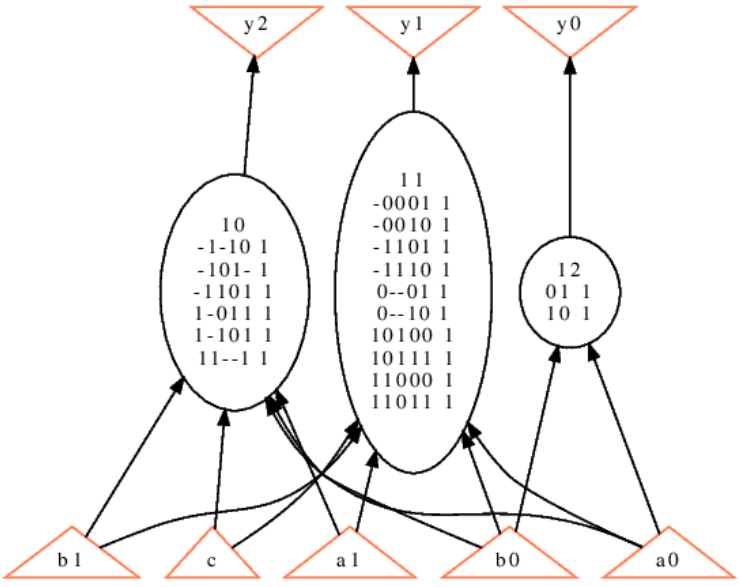
- bdd + show_bdd -g
- collapse + show_bdd -g



Both commands ultimately represent the same canonical BDD for each output function, even though “bdd” preserves the network structure internally while “collapse” eliminates it. For small circuits, these two views may converge to the same reduced BDD.

- bdd + show
- collapse + show

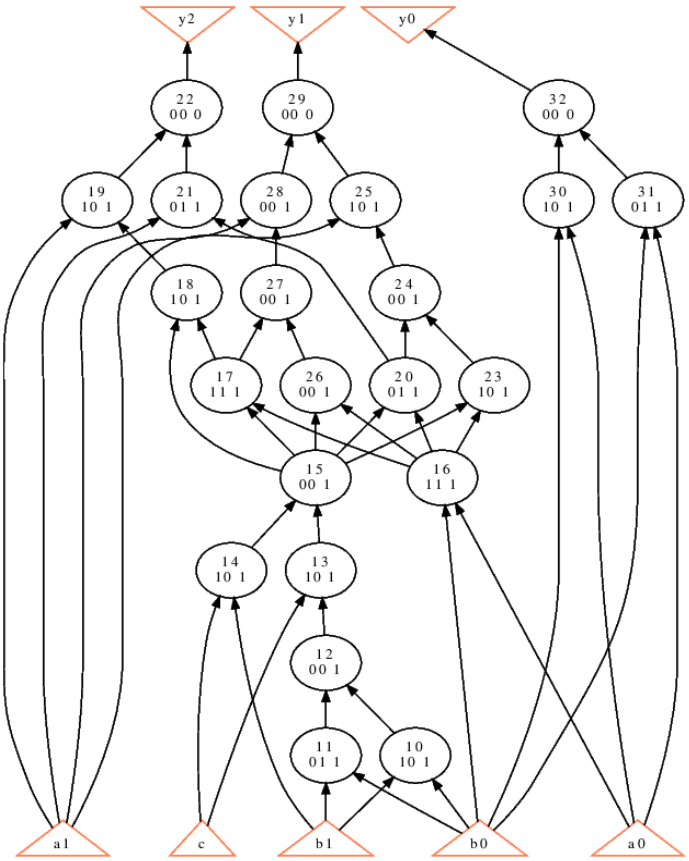
The network contains 3 logic nodes and 0 latches.



3. (b)

read alu.blif □ strash □ logic

The network contains 23 logic nodes and 0 latches.



Since the command “logic” is one that converts circuit to a logic network with node function expressed in sum-of-products (SOP).