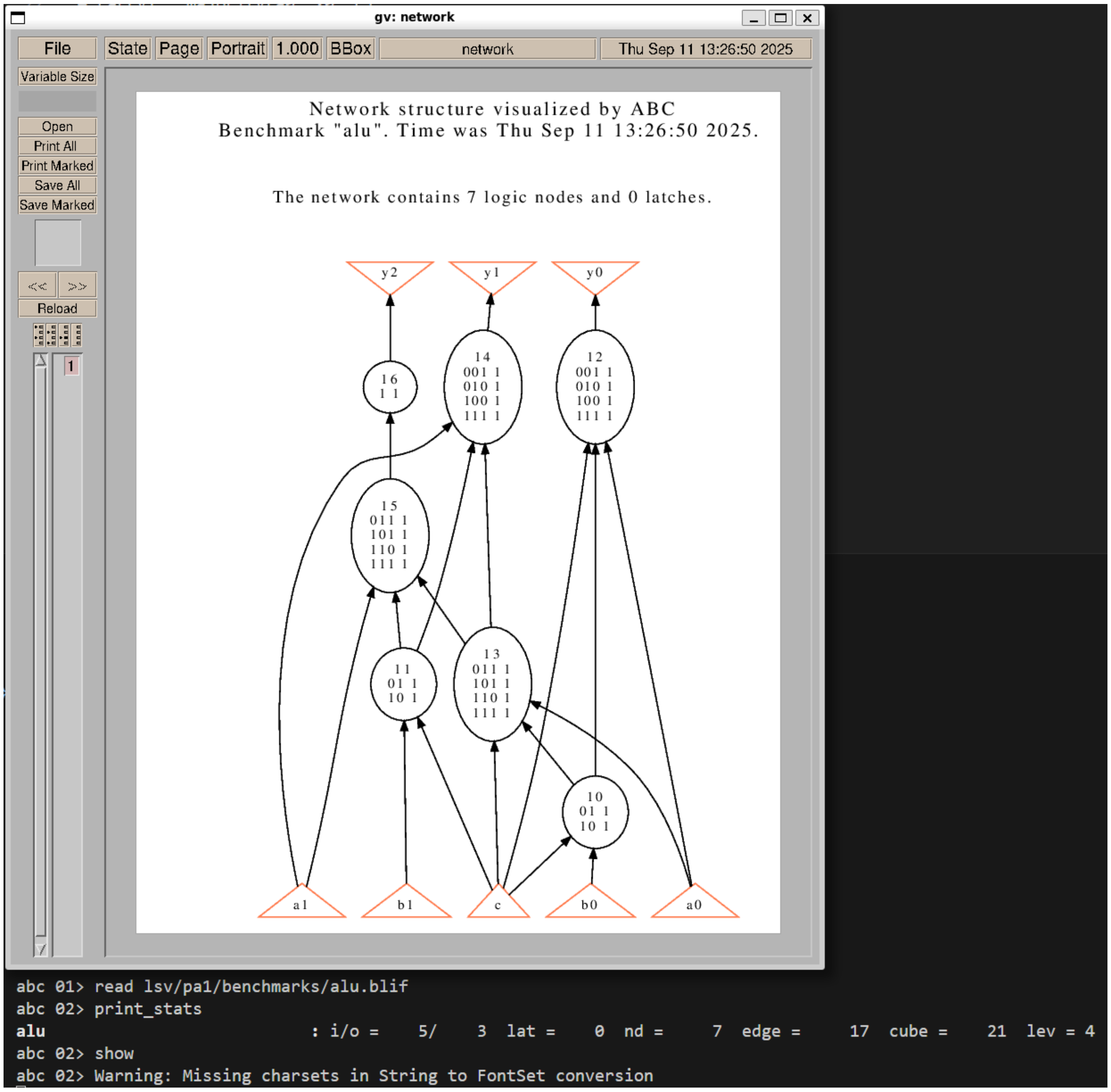
LSV PA1 report

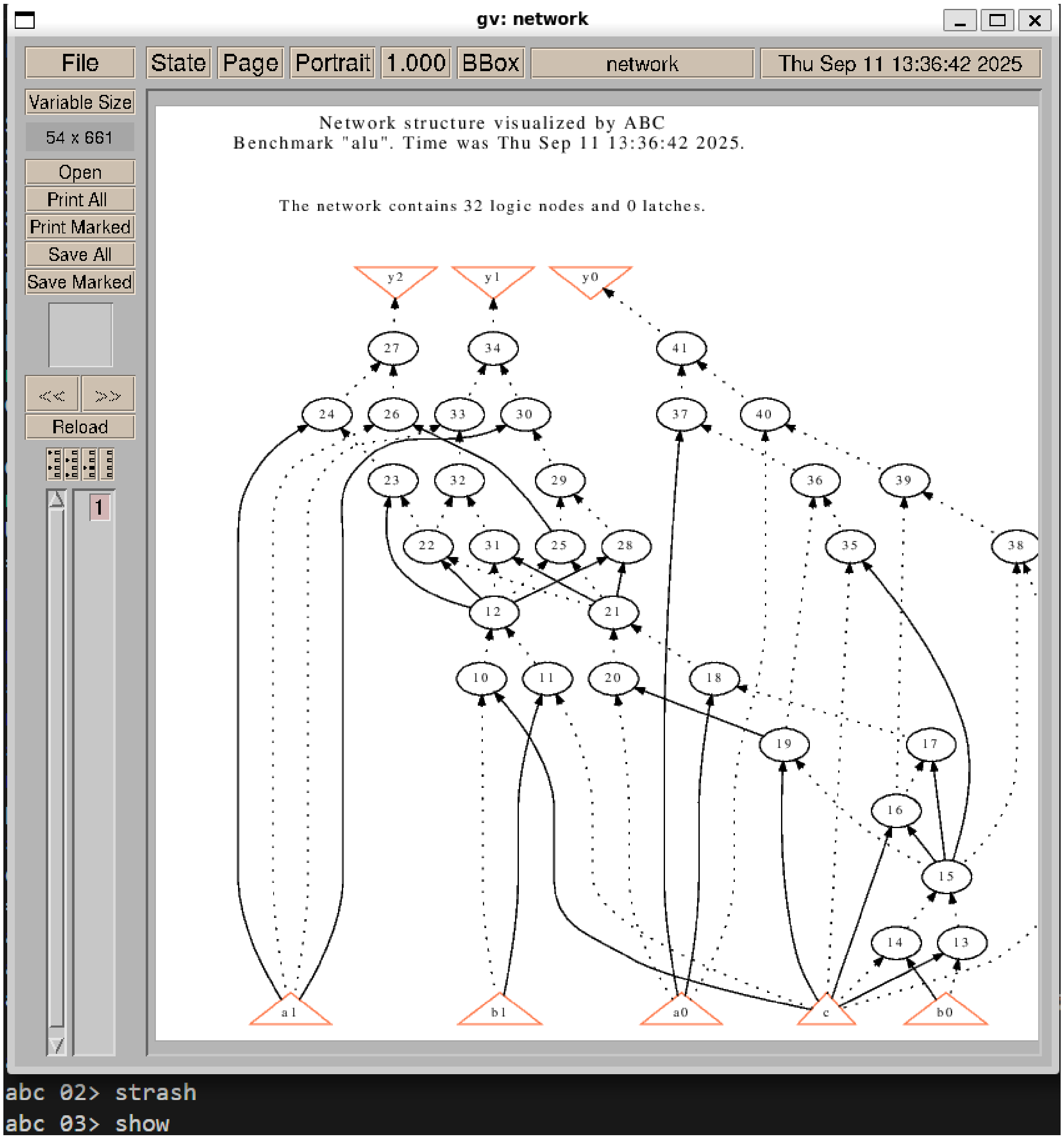
2(b)

1. read the BLIF file into ABC (command "read")
2. check statistics (command "print stats")
3. visualize the network structure (command "show")



```
abc 01> read lsv/pa1/benchmarks/alu.blif
abc 02> print_stats
alu                           : i/o =    5/    3  lat =    0  nd =     7  edge =     17  cube =     21  lev = 4
abc 02> show
abc 02> Warning: Missing charsets in String to FontSet conversion
```

4. convert to AIG (command “strash”)
5. visualize the AIG (command “show”)

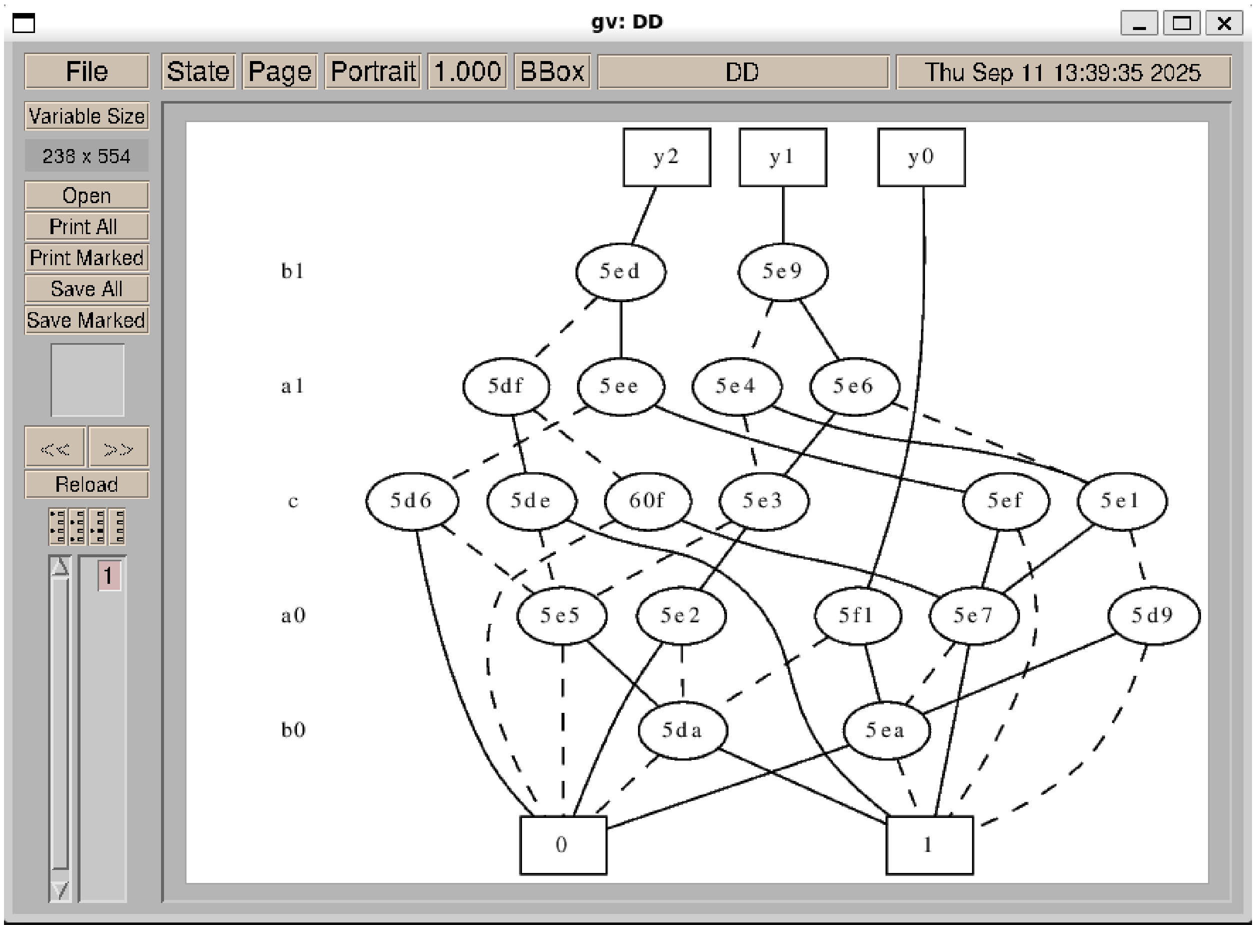


Network structure visualized by ABC
Benchmark "alu". Time was Thu Sep 11 13:36:42 2025.

The network contains 32 logic nodes and 0 latches.

```
abc 02> strash
abc 03> show
```

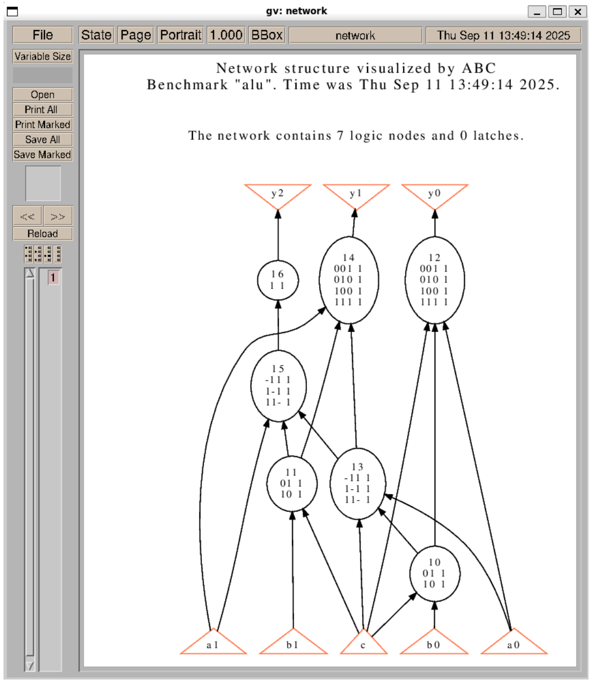
6. convert to BDD (command “collapse”)
7. visualize the BDD (command “show bdd -g”; note that “show bdd” only shows the first PO; option “-g” can be applied to show all POs)



```
abc 04> collapse
abc 05> show_bdd -g
```

3(a)

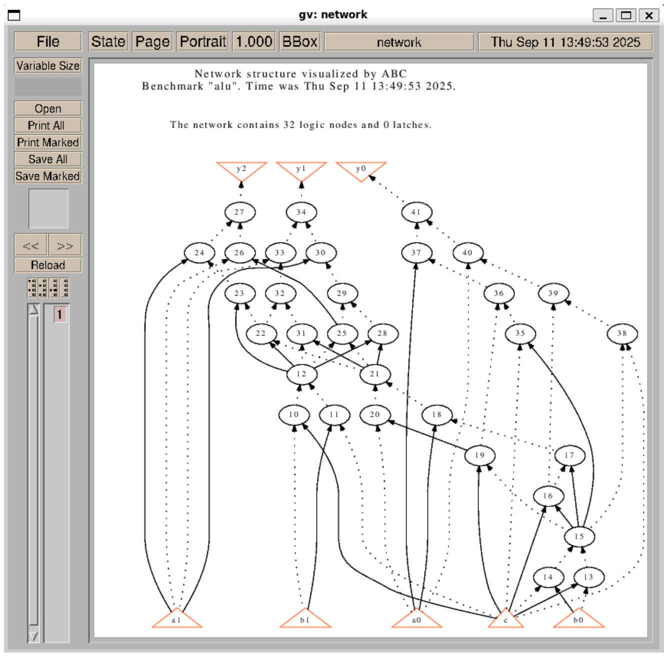
1. logic network in AIG (by command “aig”)



Network structure visualized by ABC
Benchmark "alu". Time was Thu Sep 11 13:49:14 2025.

The network contains 7 logic nodes and 0 latches.

structurally hashed AIG (by command “strash”)

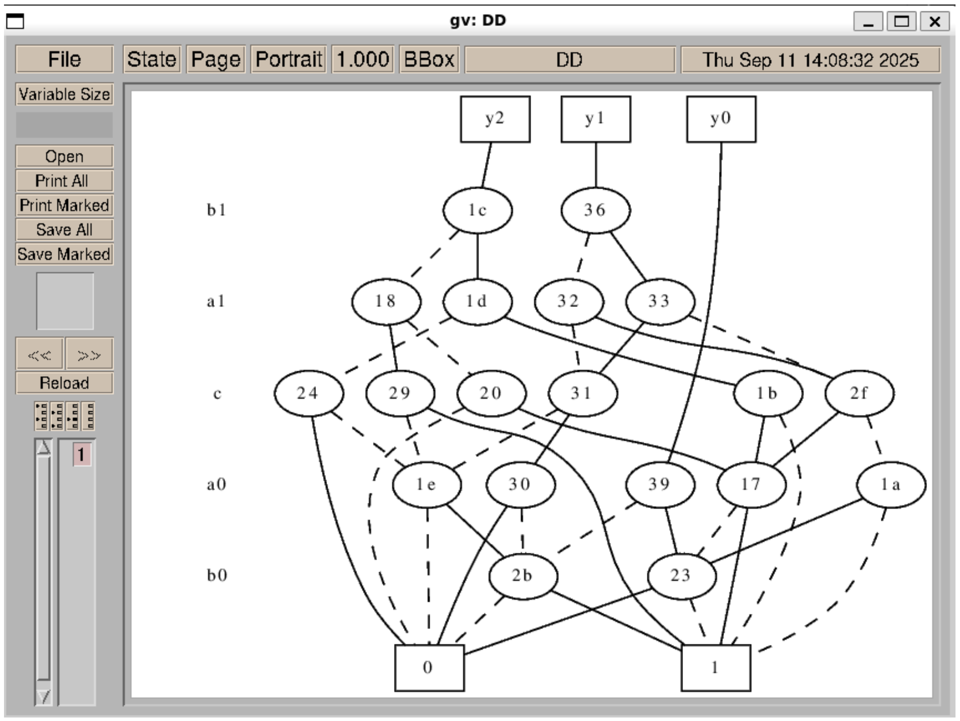


Network structure visualized by ABC
Benchmark "alu". Time was Thu Sep 11 13:49:53 2025.

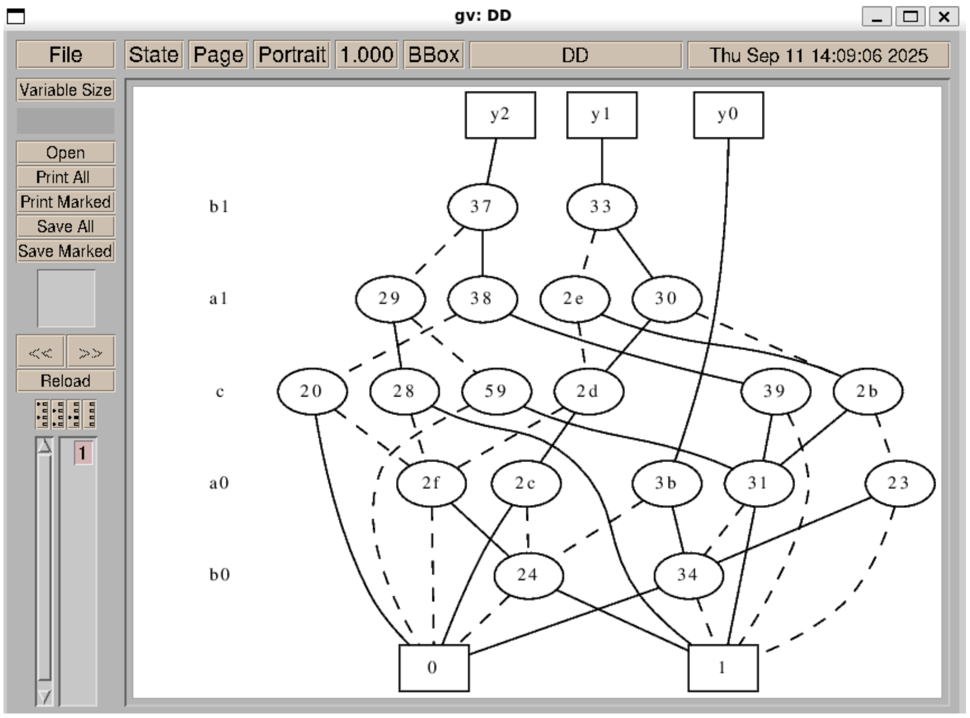
The network contains 32 logic nodes and 0 latches.

The AIG graph from the aig command is a direct translation of the BLIF. It contains only 7 logic nodes. After applying strash, the structurally hashed AIG contains 32 nodes, showing how ABC expands and re-encodes the circuit while merging redundancies.

2. logic network in BDD (by command “bdd”)

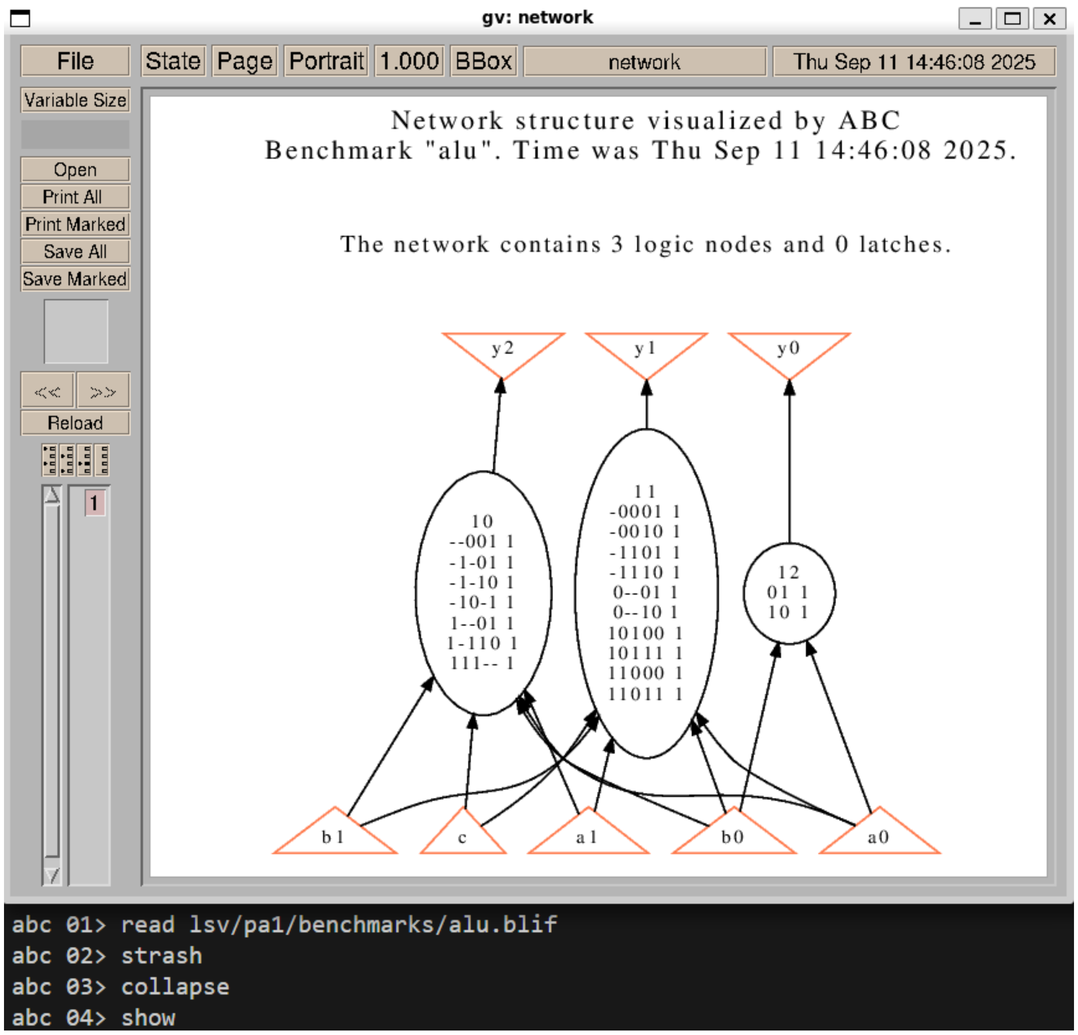


collapsed BDD (by command “collapse”)



For this small ALU circuit, the BDD (bdd) and collapsed BDD (collapse) look identical. This is because the circuit has limited redundancy among outputs, and the chosen variable ordering already minimizes duplication. In larger circuits, collapse would reduce the BDD size by merging common subgraphs across outputs.

3(b)



Network structure visualized by ABC
Benchmark "alu". Time was Thu Sep 11 14:46:08 2025.

The network contains 3 logic nodes and 0 latches.

```
abc 01> read lsv/pa1/benchmarks/alu.blif
abc 02> strash
abc 03> collapse
abc 04> show
```