
STM32
CubeMX

1. Description

1.1. Project

Project Name	NUFSR
Board Name	custom
Generated with:	STM32CubeMX 6.11.1
Date	04/29/2024

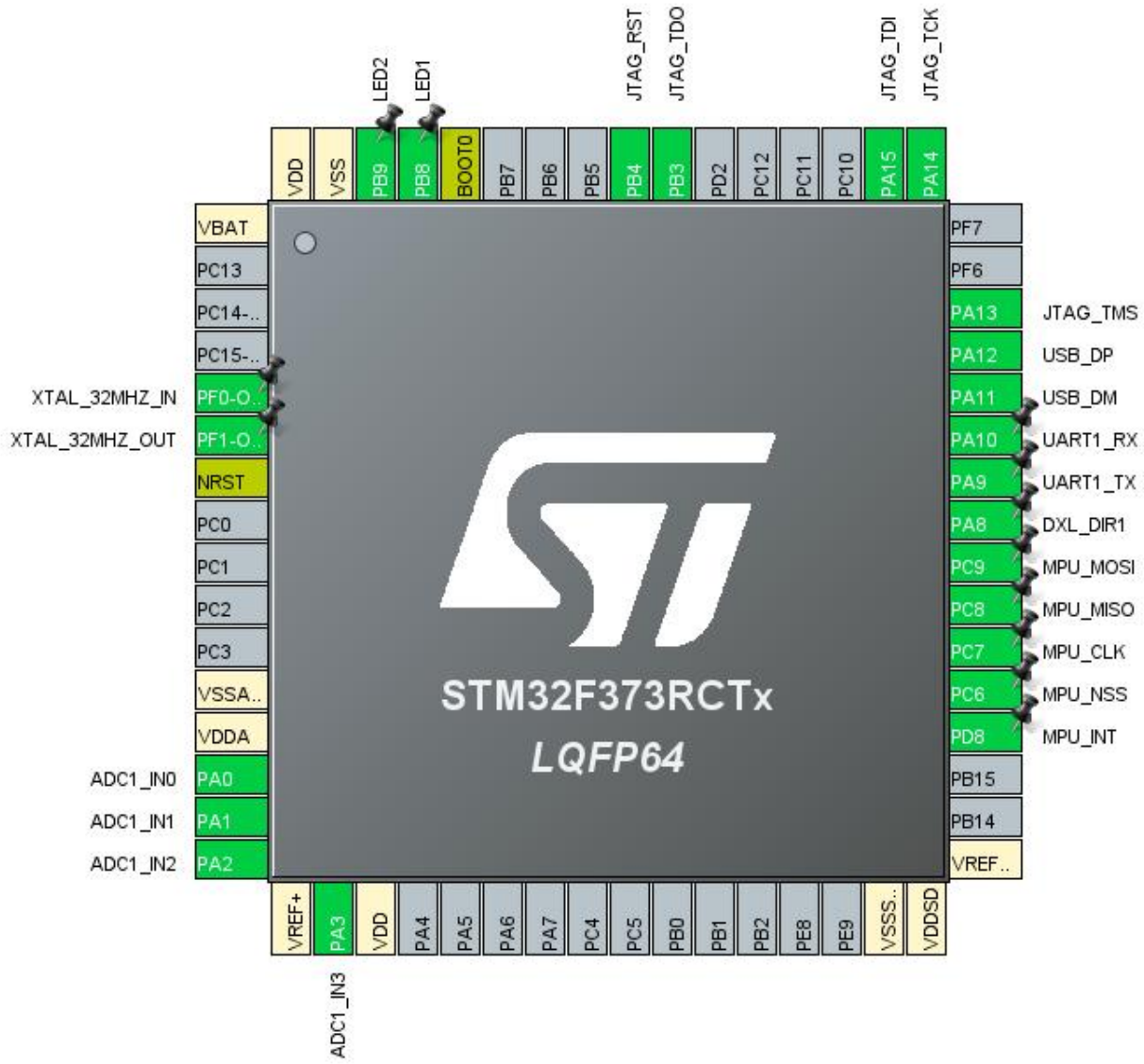
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F373
MCU name	STM32F373RCTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

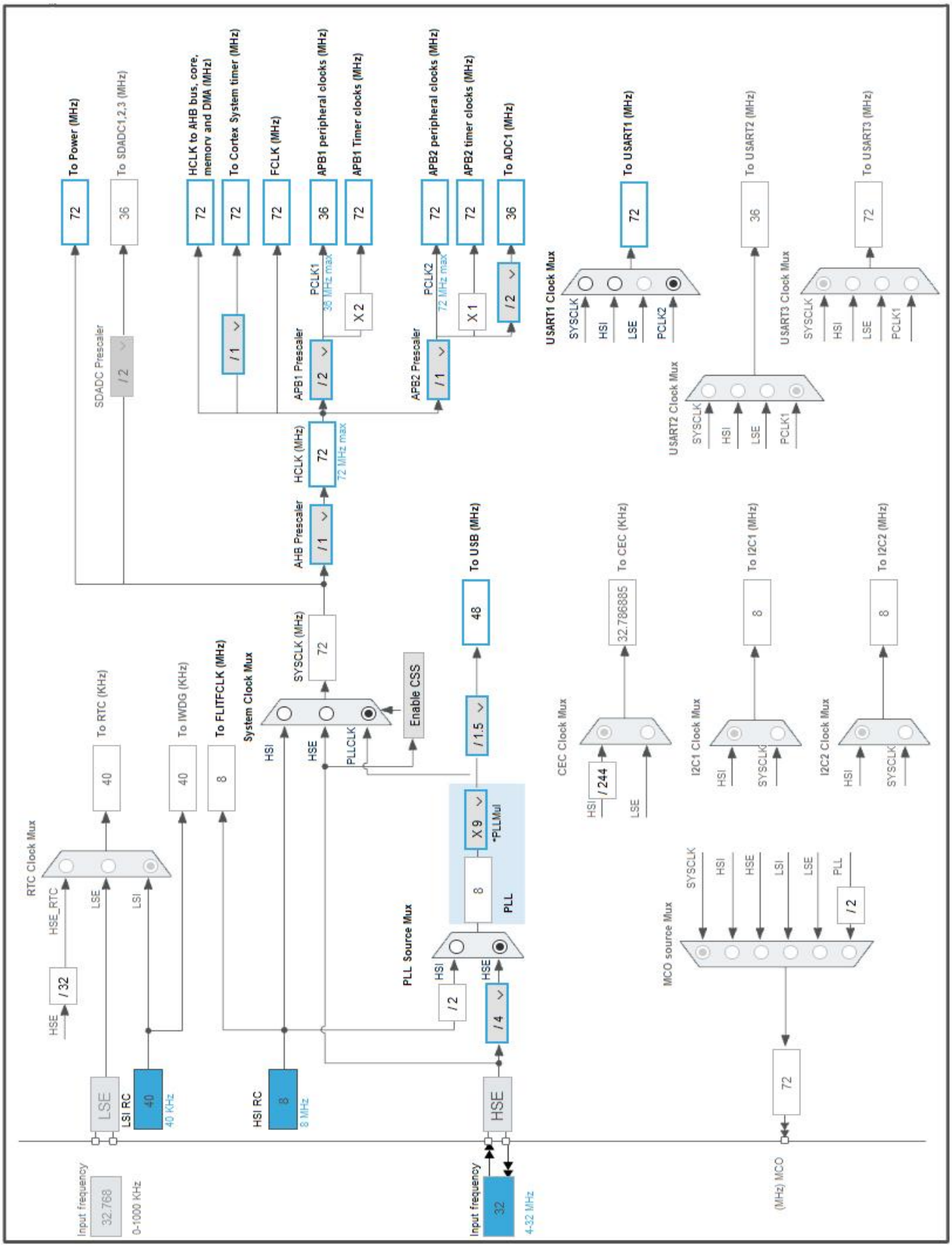


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PF0-OSC_IN	I/O	RCC_OSC_IN	XTAL_32MHZ_IN
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	XTAL_32MHZ_OUT
7	NRST	Reset		
12	VSSA/VREF-	Power		
13	VDDA	Power		
14	PA0	I/O	ADC1_IN0	
15	PA1	I/O	ADC1_IN1	
16	PA2	I/O	ADC1_IN2	
17	VREF+	Power		
18	PA3	I/O	ADC1_IN3	
19	VDD	Power		
31	VSSSD/VREFSD-	Power		
32	VDDSD	Power		
33	VREFSD+	Power		
36	PD8	I/O	GPIO_EXTI8	MPU_INT
37	PC6	I/O	SPI1_NSS	MPU_NSS
38	PC7	I/O	SPI1_SCK	MPU_CLK
39	PC8	I/O	SPI1_MISO	MPU_MISO
40	PC9	I/O	SPI1_MOSI	MPU_MOSI
41	PA8 *	I/O	GPIO_Output	DXL_DIR1
42	PA9	I/O	USART1_TX	UART1_TX
43	PA10	I/O	USART1_RX	UART1_RX
44	PA11	I/O	USB_DM	
45	PA12	I/O	USB_DP	
46	PA13	I/O	SYS_JTMS-SWDIO	JTAG_TMS
49	PA14	I/O	SYS_JTCK-SWCLK	JTAG_TCK
50	PA15	I/O	SYS_JTDI	JTAG_TDI
55	PB3	I/O	SYS_JTDO-TRACESWO	JTAG_TDO
56	PB4	I/O	SYS_NJTRST	JTAG_RST
60	BOOT0	Boot		
61	PB8 *	I/O	GPIO_Output	LED1
62	PB9 *	I/O	GPIO_Output	LED2
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	NUFSR
Project Folder	D:\Github\NUware\NUFSR
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_SPI1_Init	SPI1
6	MX_USART1_UART_Init	USART1
7	MX_USB_PCD_Init	USB
8	MX_TIM3_Init	TIM3

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F3
Line	STM32F373
MCU	STM32F373RCTx
Datasheet	DS8845_Rev7

1.2. Parameter Selection

Temperature	25
Vdd	3.6

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

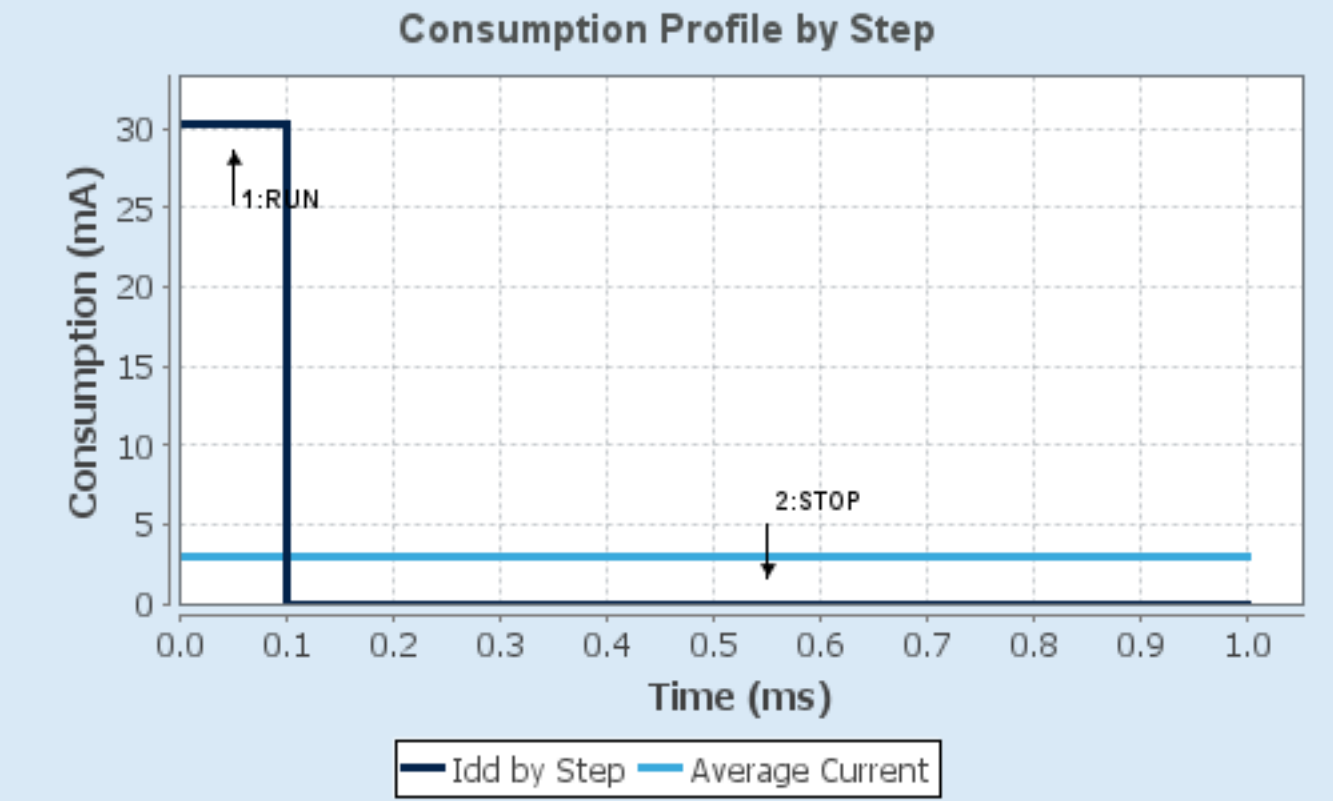
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	RAM	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSEBYP PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	30.25 mA	10.9 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	3.03 mA
Battery Life	1 month, 16 days, 4 hours	Average DMIPS	90.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC1

mode: IN0

mode: IN1

mode: IN2

mode: IN3

2.1.1. Parameter Settings:

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**4 ***
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	1.5 Cycles
Rank	**3 ***
Channel	**Channel 2 ***
Sampling Time	1.5 Cycles
Rank	**4 ***
Channel	**Channel 3 ***
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

2.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

2.3. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

2.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**4.5 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

2.4. SYS

Debug: JTAG (5 pins)

Timebase Source: SysTick

2.5. TIM3

Clock Source : Internal Clock

2.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

2.6. USART1

Mode: Asynchronous

2.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.7. USB
mode: Device (FS)

2.7.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy

Power Parameters:

Low Power	Disabled
Battery Charging	Disabled

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	XTAL_32MHZ_IN
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	XTAL_32MHZ_OUT
SPI1	PC6	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	MPU_NSS
	PC7	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	MPU_CLK
	PC8	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	MPU_MISO
	PC9	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	MPU_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	JTAG_TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	JTAG_TCK
	PA15	SYS_JTDI	n/a	n/a	n/a	JTAG_TDI
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	JTAG_TDO
	PB4	SYS_NJTRST	n/a	n/a	n/a	JTAG_RST
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	UART1_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	UART1_RX
USB	PA11	USB_DM	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA12	USB_DP	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
GPIO	PD8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	MPU_INT
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DXL_DIR1
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2

3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	**Very High ***
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
ADC1 interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
SPI1 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM3 global interrupt	unused		
USB high priority global interrupt	unused		
USB low priority global interrupt	unused		
Floating point unit interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

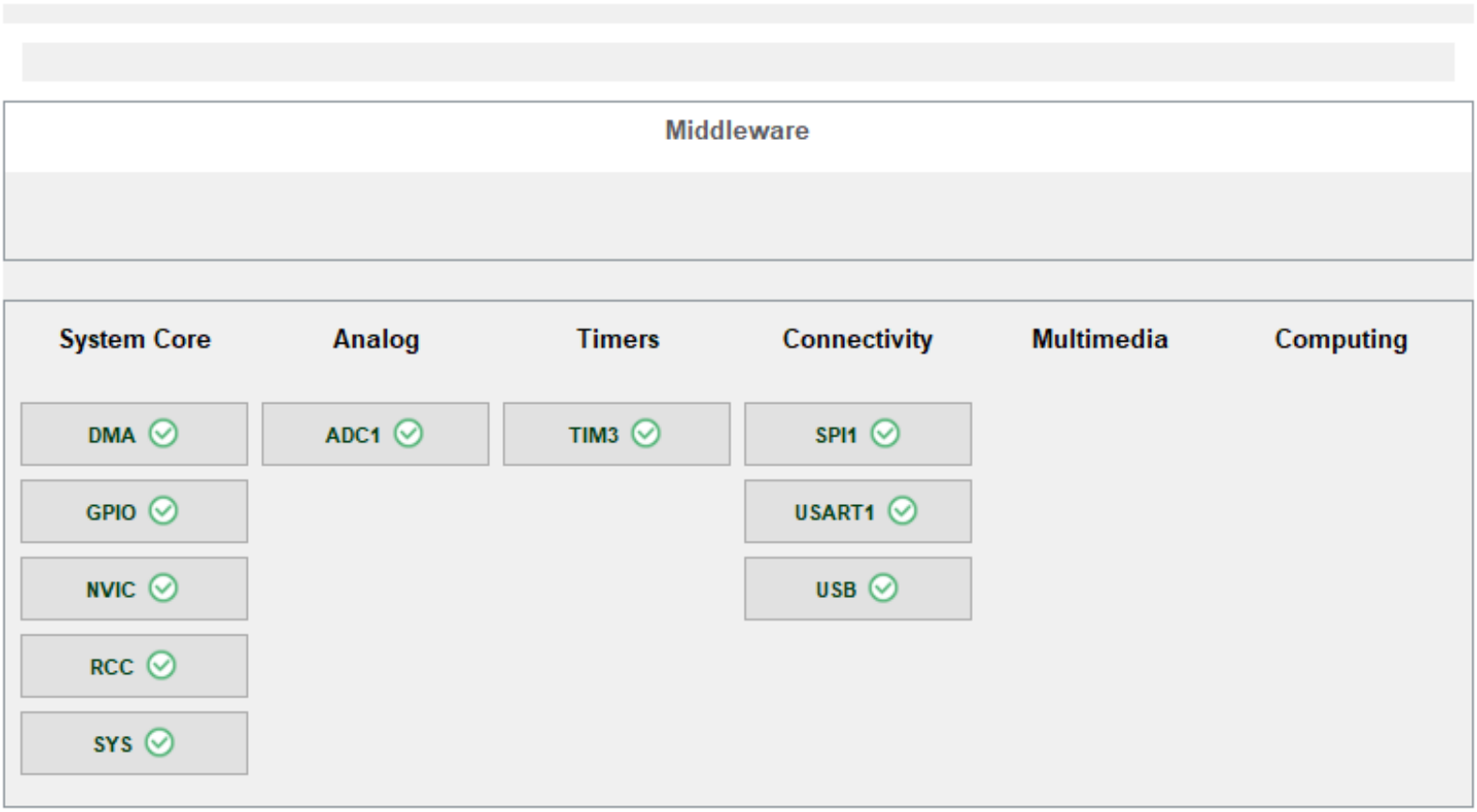
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA1 channel1 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
ADC1 interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
SPI1 global interrupt	false	true	true
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	false	true	true

*** User modified value**

4. System Views

4.1. Category view

4.1.1. Current



5. Docs & Resources

Type	Link