UNIVERSITY OF TEXAS AT ARLINGTON

MICROPROCESSOR SYSTEMS

SPRING 2020

SDRAM CONTROLLER DESIGN

Guided by,

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➢ Overview:

The goal of this project is to design an SDRAM controller that allows SDRAM memory to be interfaced with a microprocessor having only asynchronous memory support. There is no requirement to build the hardware, but a complete written report containing schematics and theory of operation is required.

➢ Detailed Requirements:

The SDRAM controller should be designed to interface with one or more SDRAM memory devices. The minimum requirement is that support for a single MT48LC4M16A2 be provided. It is strongly suggested that you attempt to provide interfacing with the 80386DX processor, but you may interface with another 32-bit data bus processor provided SDRAM memory support is not already provided for that processor.

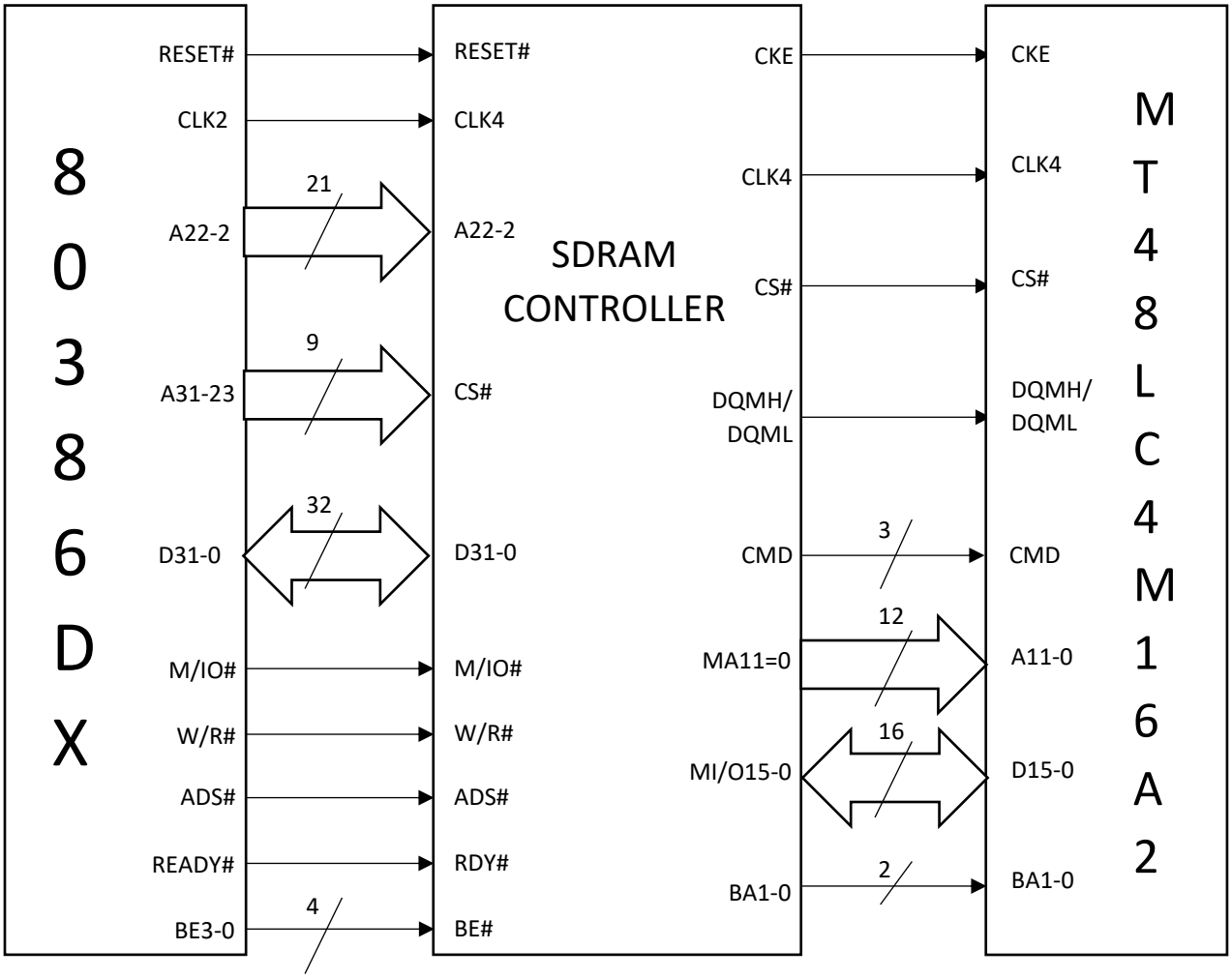
• The detailed requirements follow:

1. Support the MT48LC4M16A2 memory device is required.
2. Support for an 80386DX or similar processor with 32-bit data bus not having SDRAM support is required.
3. The use of "northbridge/MCH/IMCH" chipsets, SDRAM controllers (including reference design or commercial FPGA/CPLD/ASIC/hard copy solutions are not allowed).
4. A complete controller solution including state machine, row, column, and bank signal generation, data masking, data flow, ready logic, and refresh support must be provided.
5. Interfacing with ~ADS, W/~R, and M/~IO control signals (or equivalent) will be required.
6. Support the sending of AUTO REFRESH commands at a rate sufficient to ensure memory integrity. Steps to minimize microprocessor waiting due to refresh will be worth more credit.
7. Support the READY logic of the selected microprocessor system, especially when refresh is occurring, unless a bus locking protocol is used.
8. Support is only required for burst length 2 transfers, although you may add higher burst length support for DMA operations if you wish for extra credit or support lower bit-width memories with higher burst lengths as an option.
9. Extra credit steps:
   a. Adding hardware external I/O control pins to support variable timing, with changes in both the FSM timing and the LMR values being loaded.
   b. Adding hardware external I/O to support 4- and 8-bit wide memories with burst lengths of 8 and 4 appropriately with all changes needed to the FSM and SDRAM interface

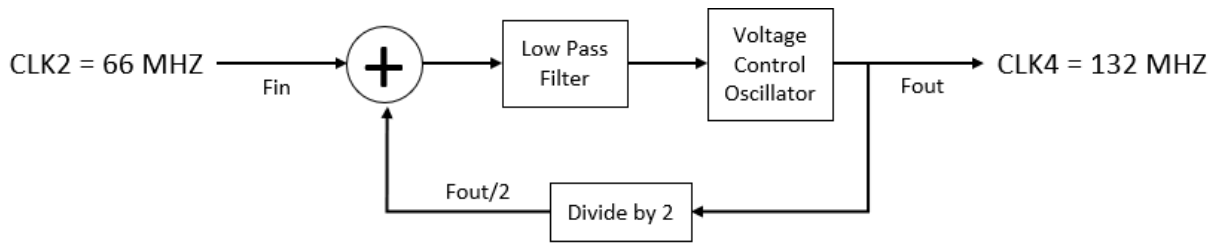
➢ Our Design:

- MT48LC4M16A2 Memory Chip (1 Meg x 16 x 4 banks)
- Speed Garde: -7E
- Clock frequency: 133 MHZ
- Clock Period: 7.5 ns
- CAS Latency: 2
- Burst Length: 2
- Refresh Time: 64 ms

➢ Interfacing Diagram:



➢ Phase Lock Loop:



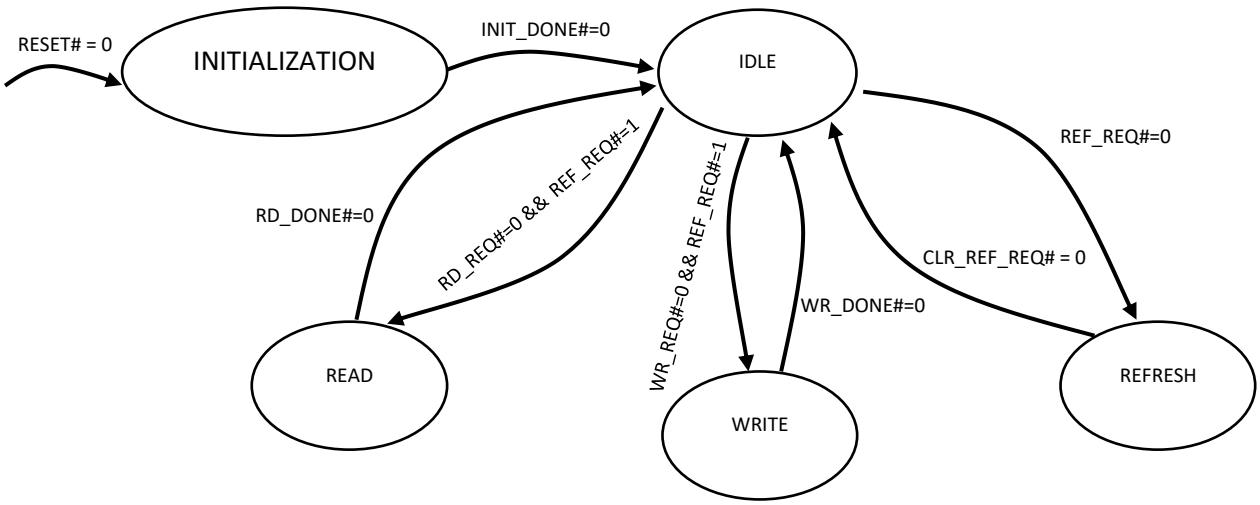
Clock Cycle Time = tCK = 1/132MHZ = 7.5ns

➢ Decoder Implementation (BL=2):

DCD_SDRAM#	BA	RA	CA	X X
A31-23	A22-21	A20-9	A8-2	X X

- Decoder Address: A31-23 (9 bit)
- Bank Address: A22-21 (2 bit)
- Row Address: A20-9 (12 bit)
- Column Address: A8-2 (8 bit)

➢ Project: Finite State Machine (Top Level):



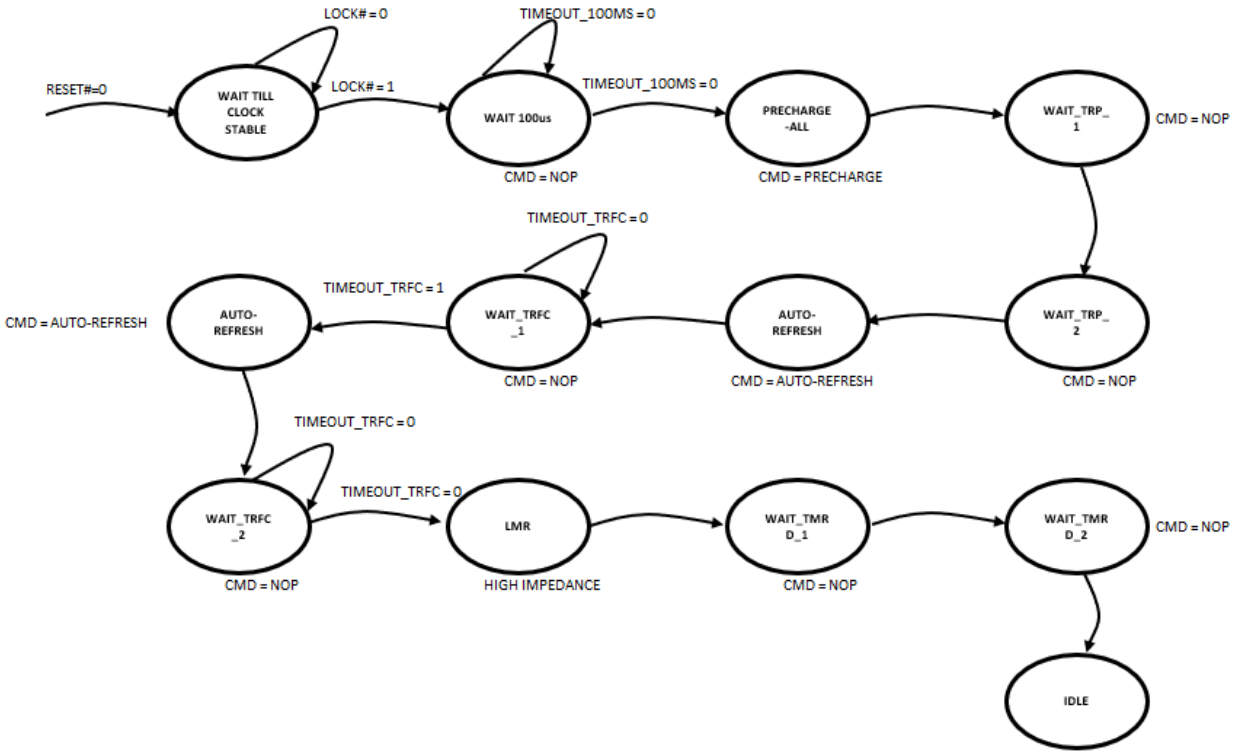
➢ General Finite State Machine Transition Table

Current State	Condition	Next State
X	RESET# = 0	INITIALIZATION
INITIALIZATION	INIT_DONE#=0	IDLE
IDLE	REF_REQ#=0	REFRESH
REFRESH	CLR_REF_REQ# = 0	IDLE
IDLE	RD_REQ#=0 && REF_REQ#=1	READ
READ	RD_DONE#=0	IDLE
IDLE	WR_REQ#=0 && REF_REQ#=1	WRITE
WRITE	WR_DONE#=0	IDLE

➢ Clock Calculations (General):

Parameter	Symbol	Value (ns)	No. of Clocks Required
Clock cycle time	tCK	7.5	-
CLK low-level width	tCL	2.5	-
CLK high-level width	tCH	2.5	-
CKE setup time	tCKS	1.5	-
CKE hold time	tCKH	0.8	-
CS#, RAS#, CAS#, WE#, DQM setup time	tCMS	1.5	-
CS#, RAS#, CAS#, WE#, DQM hold time	tCMH	0.8	-
Address setup time	tAS	1.5	-
Address hold time	tAH	0.8	-

➢ Initialization: State Diagram:



➢ Initialization: State Transition Table:

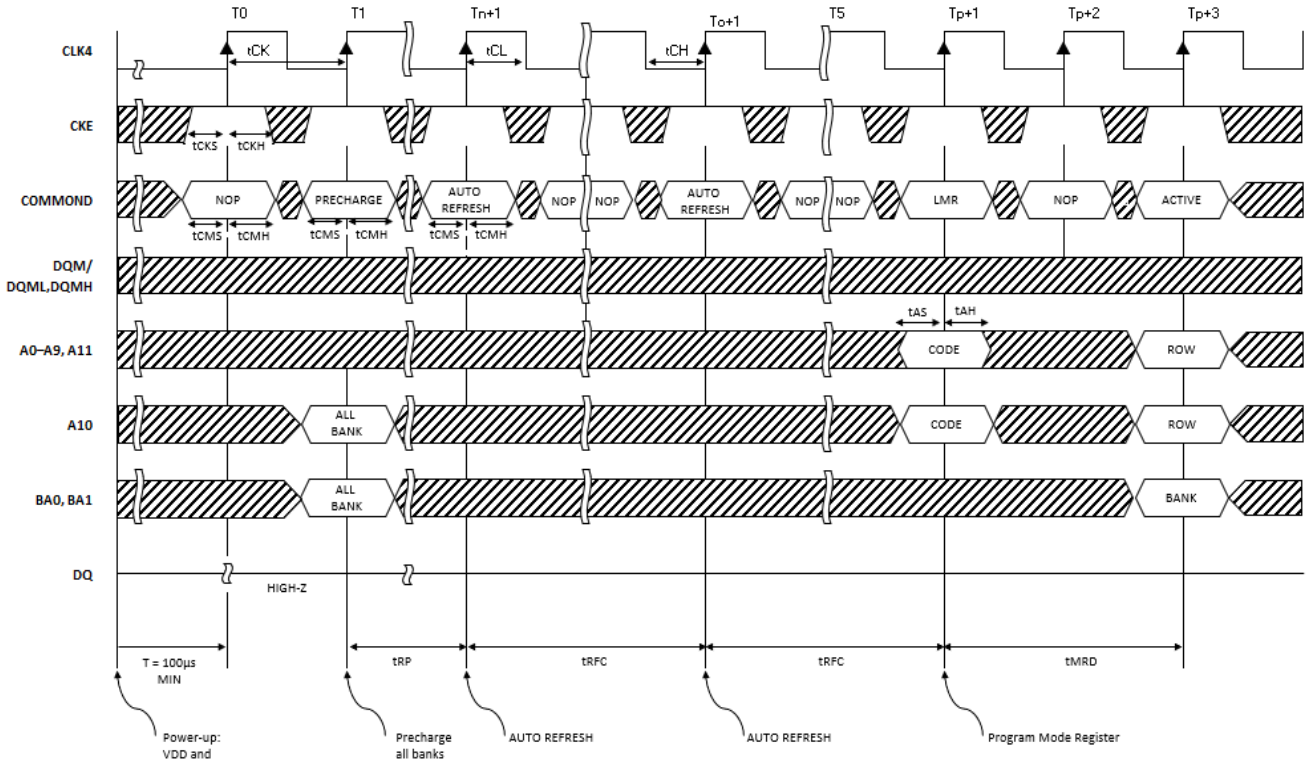
Current State	Condition	Next State
X	RESET# = 0	WAIT CLOCK STABLE
WAIT CLOCK STABLE	LOCK = 0	WAIT CLOCK STABLE
WAIT CLOCK STABLE	LOCK = 1	WAIT 100us
WAIT 100us	TIMEOUT_100MS = 0	WAIT 100us
WAIT 100us	TIMEOUT_100MS = 1	PRECHARGE ALL
PRECHARGE ALL	NEXT CLOCK	WAIT_TRP_1

WAIT_TRP_1	NEXT CLOCK	WAIT_TRP_2
WAIT_TRP_2	NEXT CLOCK	AUTO-REFRESH
AUTO-REFRESH	NEXT CLOCK	WAIT_TRFC_1
WAIT_TRFC_1	TIMEOUT_TRFC = 0	WAIT_TRFC_1
WAIT_TRFC_1	TIMEOUT_TRFC = 1	AUTO-REFRESH
AUTO-REFRESH	NEXT CLOCK	WAIT_TRFC_2
WAIT_TRFC_2	TIMEOUT_TRFC = 0	WAIT_TRFC_2
WAIT_TRFC_2	TIMEOUT_TRFC = 1	LMR
LMR	NEXT CLOCK	WAIT_TMRD_1
WAIT_TMRD_1	NEXT CLOCK	WAIT_TMRD_2
WAIT_TMRD_2	NEXT CLOCK	IDLE

➢ Initialization: Output Table:

Output	Equation
CKE	STATE = NOP | AUTO-REFRESH | PRECHARGE |LMR | IDLE
CS#	STATE = NOP | AUTO-REFRESH | PRECHARGE |LMR | IDLE
RAS#	STATE = AUTO-REFRESH | PRECHARGE | LMR
CAS#	STATE = AUTO-REFRESH | LMR
WE#	STATE = PRECHARGE |LMR
A0-A9/A11	STATE = LMR
A10	STATE = PRECHARGE | LMR
DQs	STATE = HIGH Z
BA0,BA1	STATE = PRECHARGE

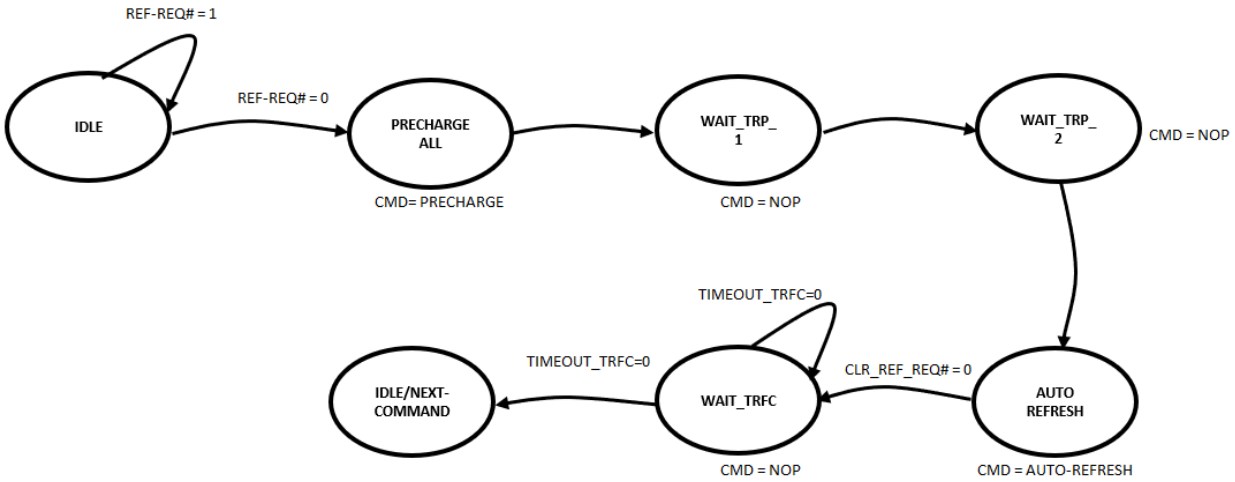
➢ Initialization: Timing Diagram:



➢ Clock Calculations (Initialization):

Parameter	Symbol	Value (ns)	No. of Clocks Required
Timeout 100 us	t100us	100 us	13300
PRECHARGE command period	tRP	15	2
AUTO REFRESH period	tRFC	66	9
LOAD MODE REGISTER command to ACTIVE or REFRESH command	tMRD	15	2

➢ AUTO REFRESH: State Diagram:



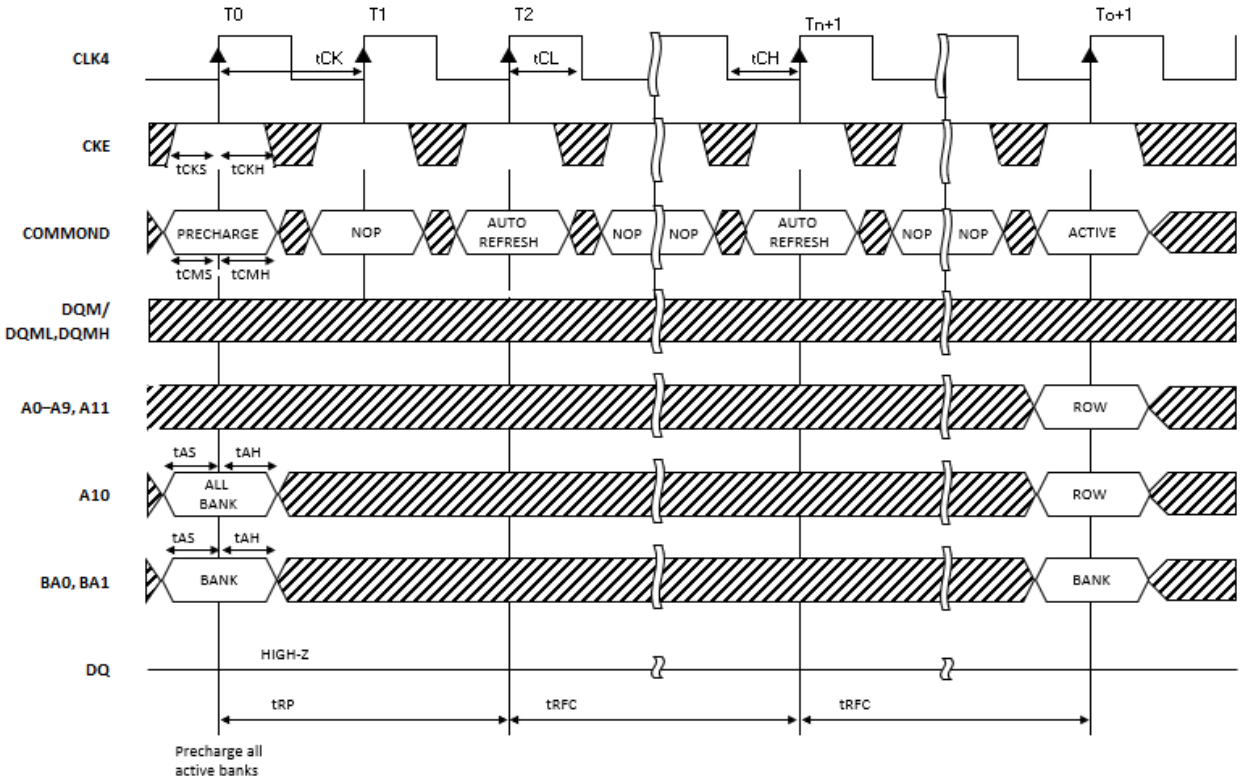
➢ AUTO REFRESH: Transition Table:

Current State	Condition	Next State
IDLE	REQ_REQ# = 0	PRECHARGE ALL
PRECHARGE ALL	NEXT CLOCK	WAIT_TRP_1
WAIT_TRP_1	NEXT_CLOCK	WAIT_TRP_2
WAIT_TRP_2	NEXT_CLOCK	AUTO-REFRESH
AUTO-REFRESH	CLR_REF_REQ# = 0	WAIT_TRFC
WAIT_TRFC	TIMEOUT_TRFC=0	WAIT_TRFC
WAIT_TRFC	TIMEOUT_TRFC=1	IDLE/NEXT_COMMAND

➢ AUTO REFRESH: Output Table:

Output	Equation
CKE	STATE= NOP | AUTO-REFRESH | PRECHARGE
CS#	STATE = NOP | AUTO-REFRESH | PRECHARGE
RAS#	STATE = AUTO-REFRESH | PRECHARGE
CAS#	STATE = AUTO-REFRESH
WE#	STATE = PRECHARGE
DQs	STATE = HIGH Z

➢ AUTO REFRESH: Timing Diagram:



➢ Clock Calculations: (Auto Refresh):

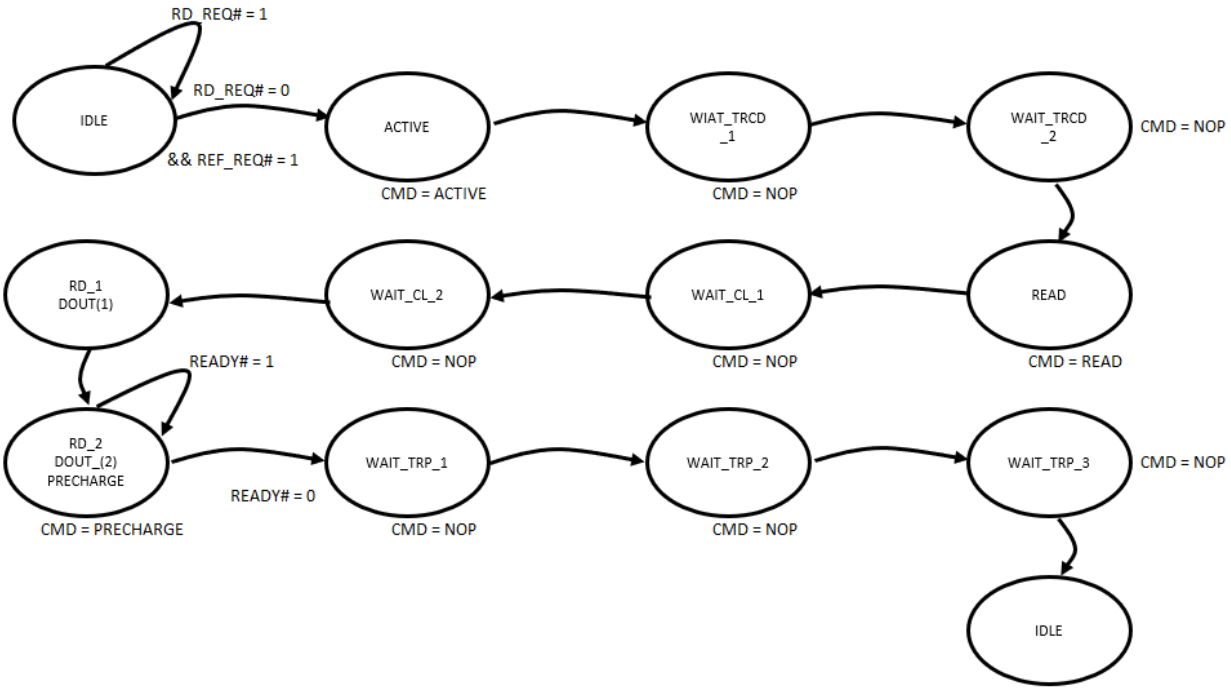
Parameter	Symbol	Value (ns)	No. of Clocks Required
PRECHARGE command period	tRP	15	2
AUTO REFRESH period	tRFC	66	9

➢ Load Mode Register:

Address Bus	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
Parameter	Reserved		WB	Op Mode		CAS Latency			BT	Burst Length		
Value	0	0	0	0	0	0	1	0	0	0	0	1

- Program: M11, M10: 0, 0: To ensure compatibility with future device
- Write Burst Mode: M9: 0: Program Burst Length
- Operating Mode: M8, M7: 0, 0: Standard Operation
- CAS latency: M6, M5, M4: 0, 1, 0: Two Clock Cycle
- Burst Type: M3: 0: Sequential
- Burst length: M2, M1, M0: 0, 0, 1: Two

➢ Read: State Diagram:



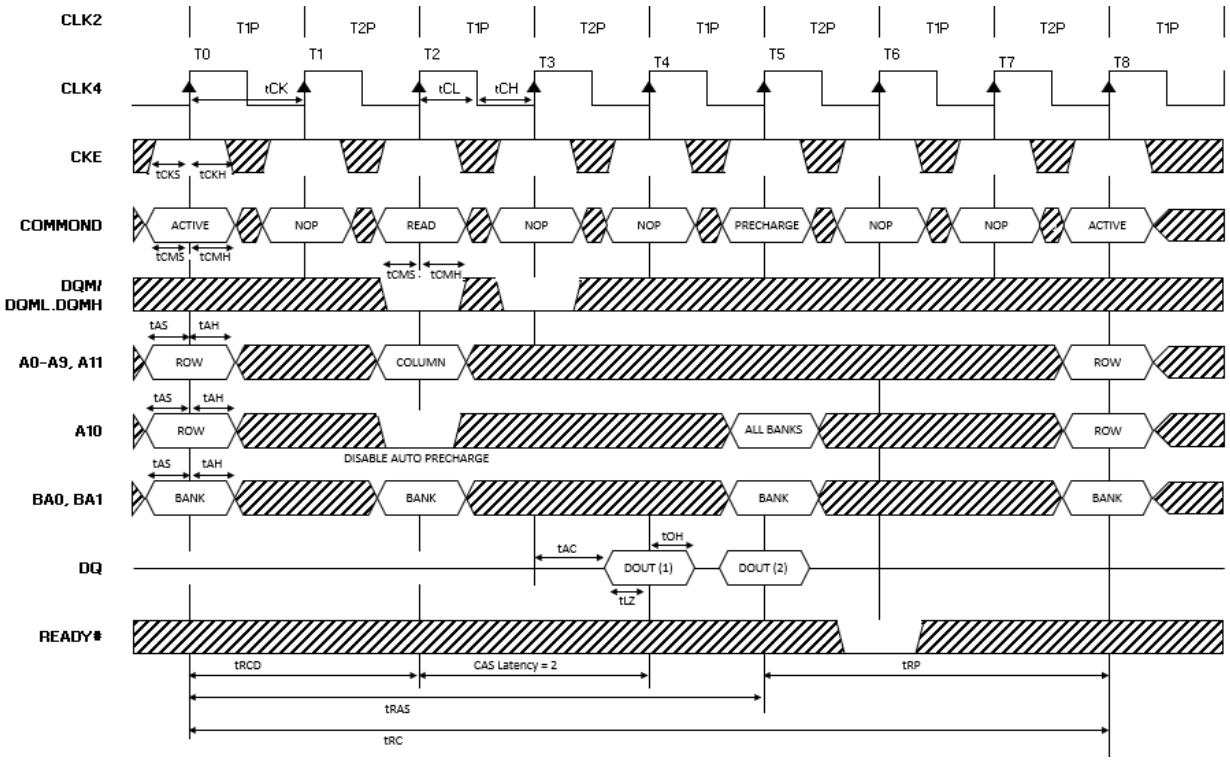
➢ Read: State Transition Table:

Current State	Condition	Next State
IDLE	RD_REQ# = 1	IDLE
IDLE	RD_REQ# = 0 && REF_REQ# = 1	ACTIVE
ACTIVE	NEXT CLOCK	WAIT_TRCD_1
WAIT_TRCD_1	NEXT CLOCK	WAIT_TRCD_2
WAIT_TRCD_2	NEXT CLOCK	READ
READ	NEXT CLOCK	WAIT_CL_1
WAIT_CL_1	NEXT CLOCK	WAIT_CL_2
WAIT_CL_2	NEXT CLOCK	RD_1/DOUT(1)
RD_1/DOUT (1)	NEXT CLOCK	RD_2/DOUT (2)/PRECHARGE
RD_2/DOUT (2)/PRECHARGE	READY# = 1	RD_2/DOUT (2)/PRECHARGE
RD_2/DOUT (2)/PRECHARGE	READY# = 0	WAIT_TRP_1
WAIT_TRP_1	NEXT CLOCK	WAIT_TRP_2
WAIT_TRP_2	NEXT CLOCK	WAIT_TRP_3
WAIT_TRP_3	NEXT CLOCK	IDLE

➢ Read: Output Table:

Output	Equation
CKE	STATE = NOP | ACTIVE | PRECHARGE |READ |RD_N | IDLE
CS#	STATE = NOP | ACTIVE | PRECHARGE |READ | IDLE
RAS#	STATE = ACTIVE
CAS#	STATE = READ
WE#	STATE = READ
A0-A9/A11	STATE = ACTIVE |READ
A10	STATE = PRECHARGE | READ | ACTIVE
DQs	STATE = RD_1 | RD_2
DQM	STATE = READ | NOP
BA0, BA1	STATE = PRECHARGE |ACTIVE

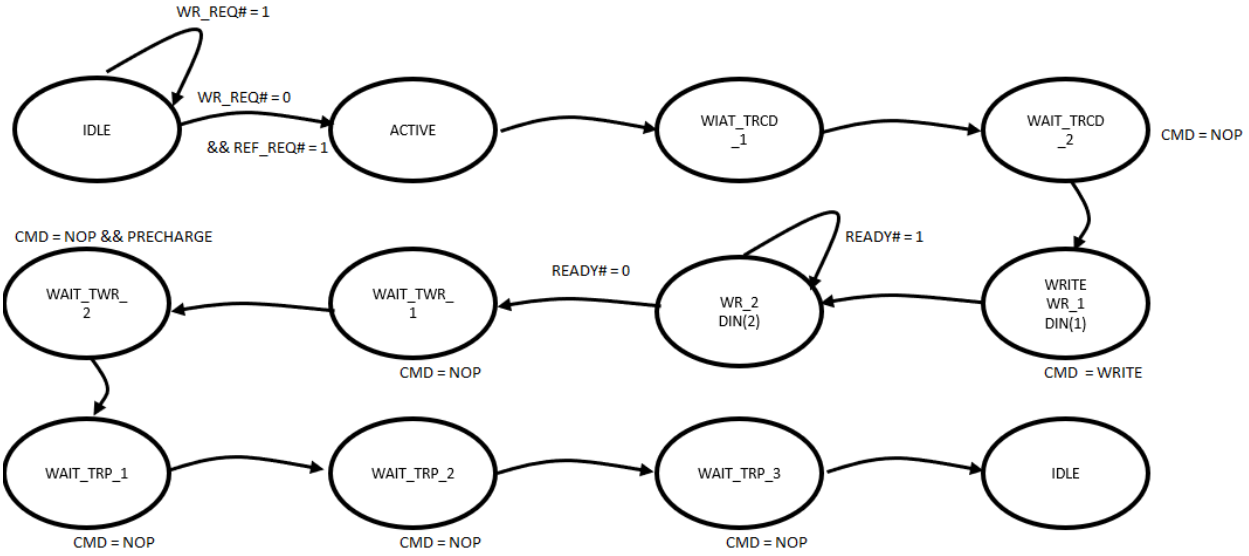
➢ Read: Timing Diagram:



➢ Clock Calculations (Read):

Parameter	Symbol	Value (ns)	No. of Clocks Required
Data-out Low-Z time	tLZ	1	-
Access time from CLK (positive edge)	tAC	5.4	-
Data-out hold time (load)	tOH	3	-
Data-out High-Z time	tHZ	5.4	-
ACTIVE-to-READ or WRITE delay	tRCD	15	2
PRECHARGE command period	tRP	22.5	3
ACTIVE-to-PRECHARGE command	tRAS	37	5
ACTIVE-to-ACTIVE command period	tRC	60	8
CAS Latency	CL	15	2

➢ Write: State Diagram:



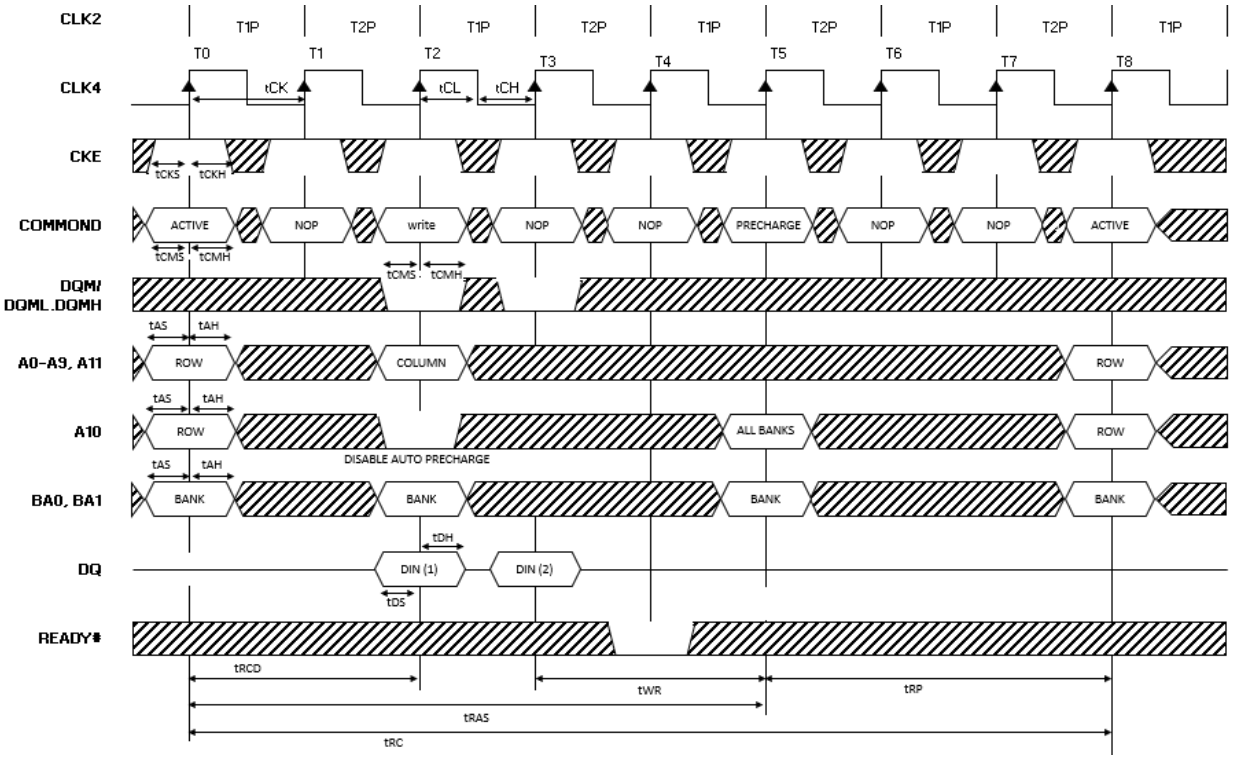
➢ Write: State Transition Table:

Current State	Condition	Next State
IDLE	WR_REQ# = 1	IDLE
IDLE	WR_REQ# = 0 && REF_REQ# = 1	ACTIVE
ACTIVE	NEXT CLOCK	WAIT_TRCD_1
WAIT_TRCD_1	NEXT CLOCK	WAIT_TRCD_2
WAIT_TRCD_2	NEXT CLOCK	WRITE/WR_1/DIN (1)
WRITE/WR_1/DIN (1)	NEXT CLOCK	WR_2/DIN (2)
WR_2/DIN (2)	READY# = 1	WR_2/DIN (2)
WR_2/DIN (2)	READY# = 0	WAIT_TWR_1
WAIT_TWR_1	NEXT CLOCK	WAIT_TWR_2
WAIT_TWR_2	NEXT CLOCK	WAIT_TRP_1
WAIT_TRP_1	NEXT CLOCK	WAIT_TRP_2
WAIT_TRP_2	NEXT CLOCK	WAIT_TRP_3
WAIT_TRP_3	NEXT CLOCK	WAIT_TRP_3
WAIT_TRP_3	NEXT CLOCK	IDLE

➢ Write: Output Table:

Output	Equation
CKE	STATE = NOP | ACTIVE | PRECHARGE |WRITE |WR_N | IDLE
CS#	STATE = NOP | ACTIVE | PRECHARGE |WRITE | IDLE
RAS#	STATE = ACTIVE
CAS#	STATE = WRITE
WE#	STATE = WRITE
A0-A9/A11	STATE = ACTIVE | WRITE
A10	STATE = PRECHARGE | WRITE |ACTIVE
DQM	STATE = WR_1 | WR_2
DQs	STATE = WR_1 | WR_2
BA0, BA1	STATE = PRECHARGE |ACTIVE

➢ Write: Timing Diagram:

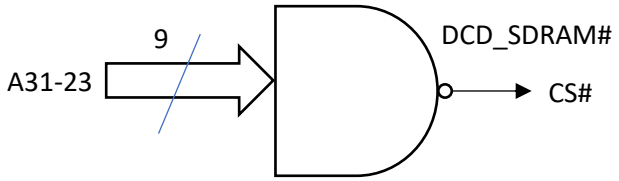


➢ Clock Calculations (Write):

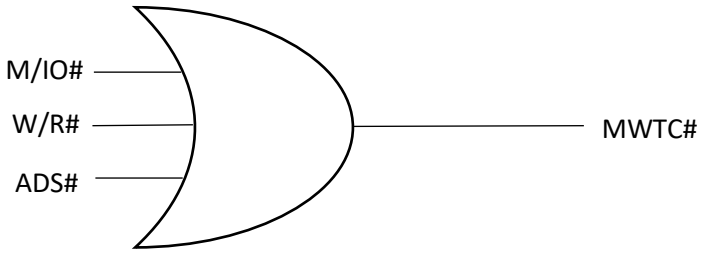
Parameter	Symbol	Value (ns)	No. of Clocks Required
Data-in setup time	tDS	1.5	-
Data-in hold time	tDH	0.8	-
ACTIVE-to-READ or WRITE delay	tRCD	15	2
WRITE recovery time	tWR	14.5	2
PRECHARGE command period	tRP	22.5	3
ACTIVE-to-PRECHARGE command	tRAS	37	5
ACTIVE-to-ACTIVE command period	tRC	60	8

➢ Generation of Chip Signals:

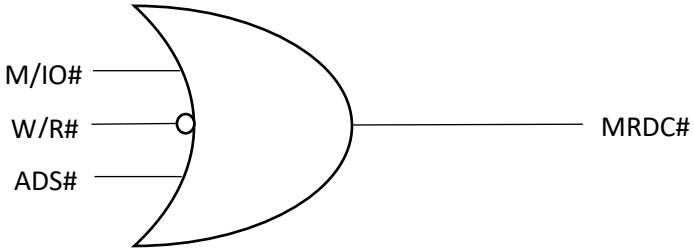
- **Generation of Chip Select:**



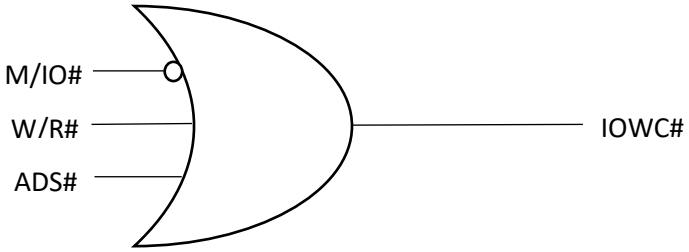
- **Generation of MWTC#:**



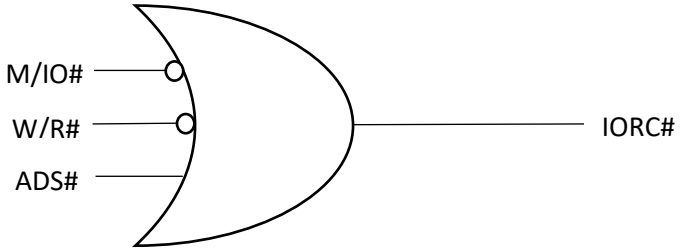
- **Generation of MRDC#:**



- **Generation of IOWC#:**



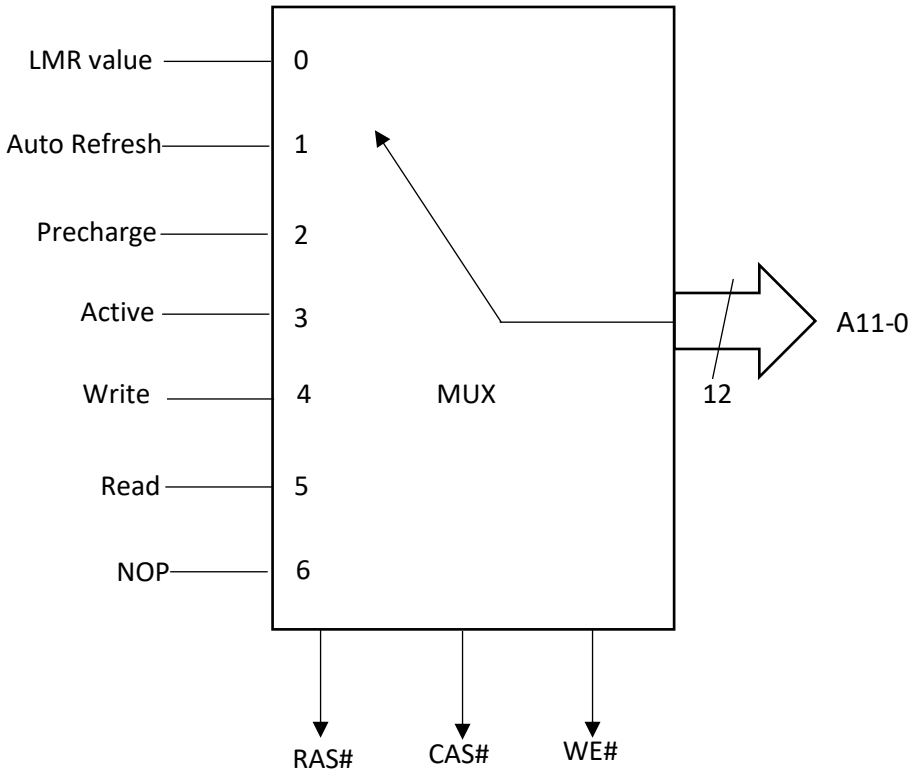
- **Generation of IORC#:**



OE# = DCD_SDRAM# + MRDC#

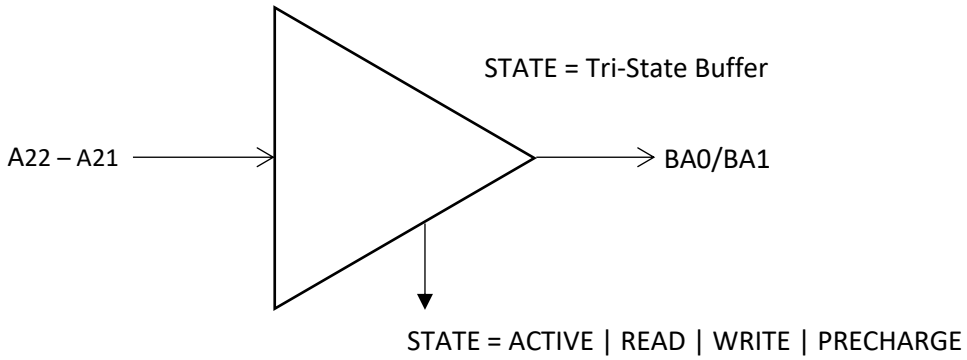
WE# = DCD_SDRAM# + MWTC#

- **Generation of Command Signal:**

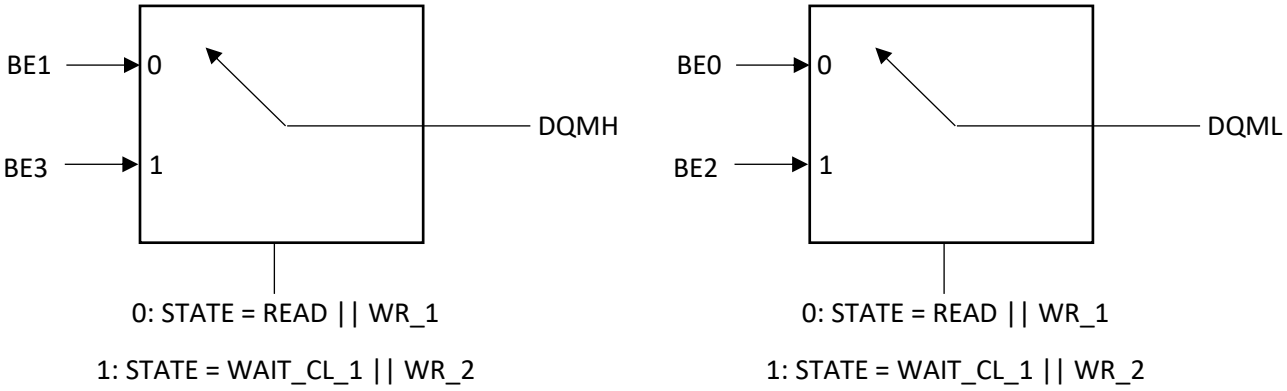


STATE	Command	RAS#	CAS#	WE#
0	LMR	0	0	0
1	AUTO REFRESH	0	0	1
2	PRECHARGE	0	1	0
3	ACTIVE	0	1	1
4	WRITE	1	0	0
5	READ	1	0	1
6	NOP	1	1	1

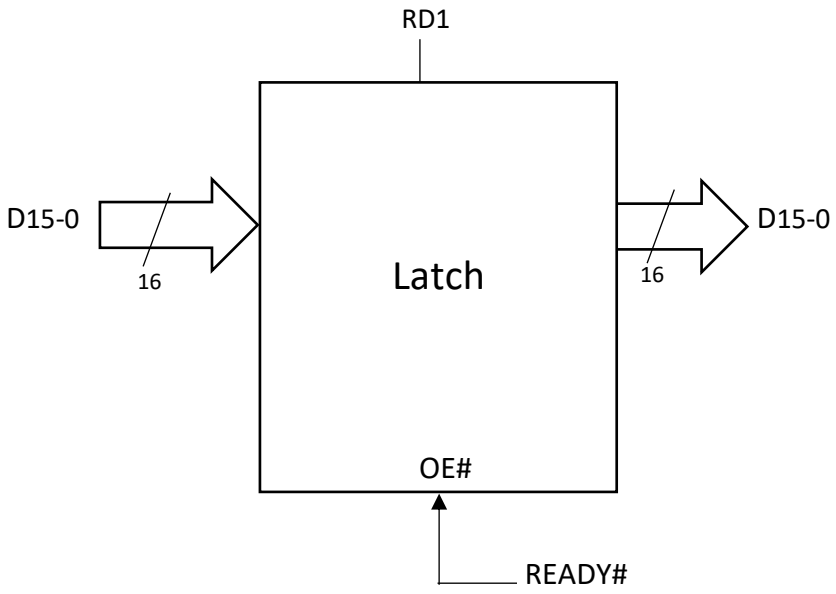
- **Generation of Bank Address:**

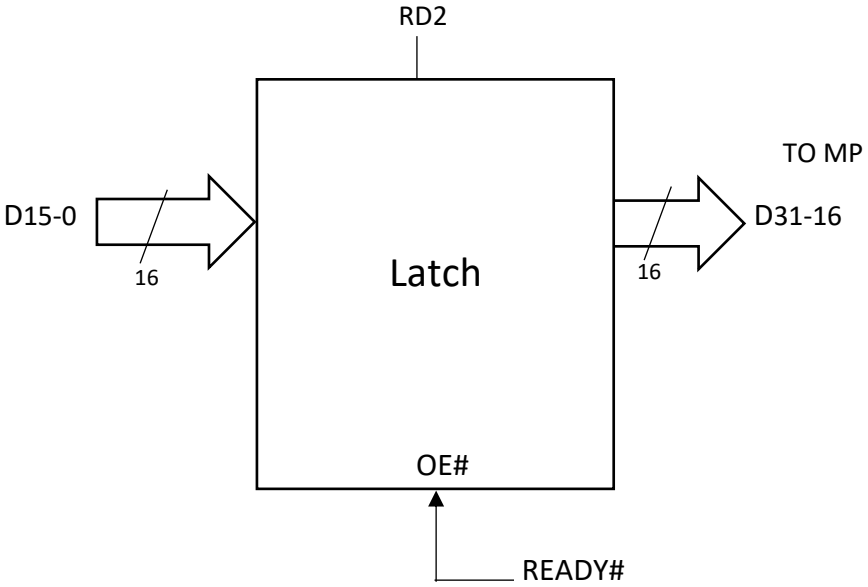


- **Generation of DQM/ DQMH, DQML:**

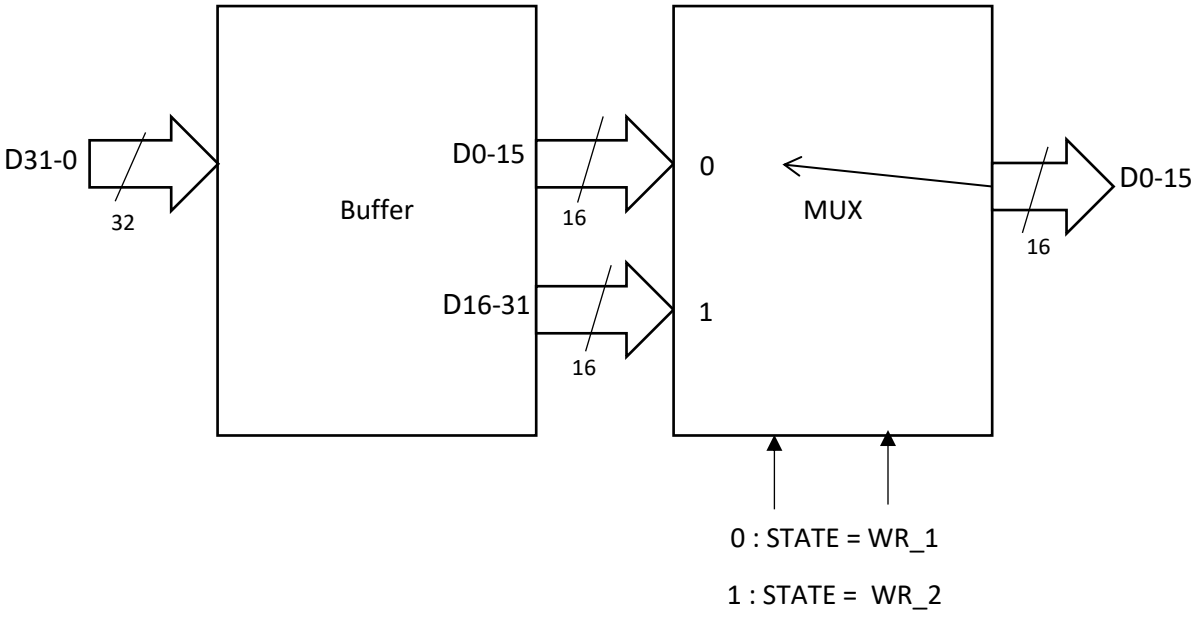


- **Data Latch for Read:**

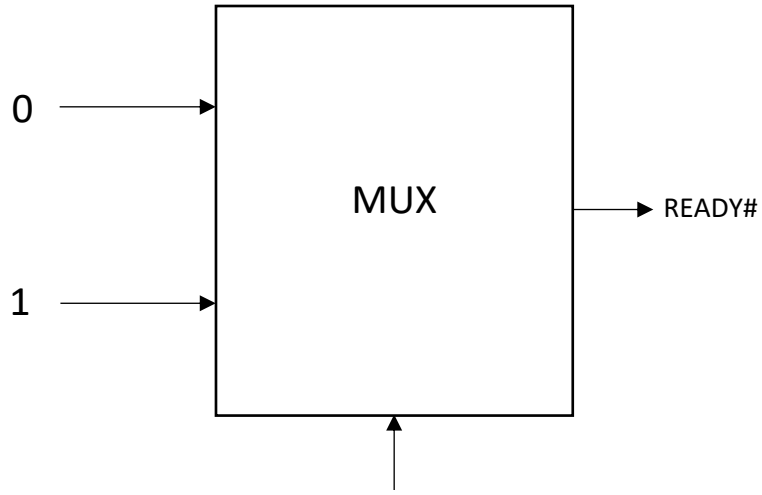




- **Data MUX for Write:**



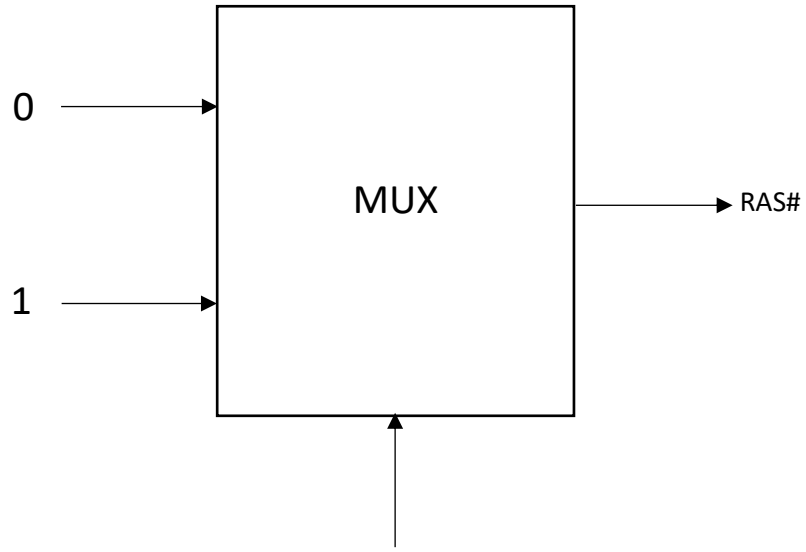
- **Generation of Ready Signal:**



1 = STATE! = RD_2 | WR_2

0 = STATE= RD_2 | WR_2

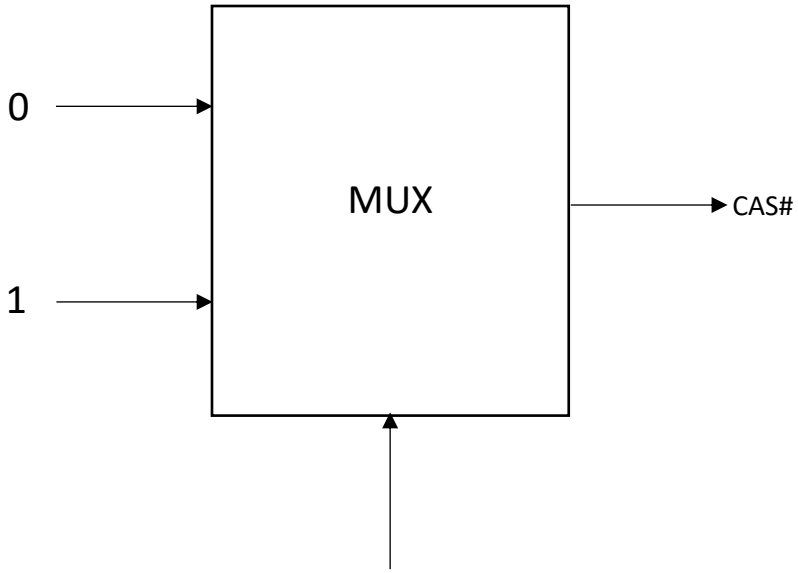
- **Generation of RAS# Signal:**



STATE= 0= ACTIVE || PRECHARGE || AUTO REFRESH || LMR

STATE= 1= NOP || READ || WRITE

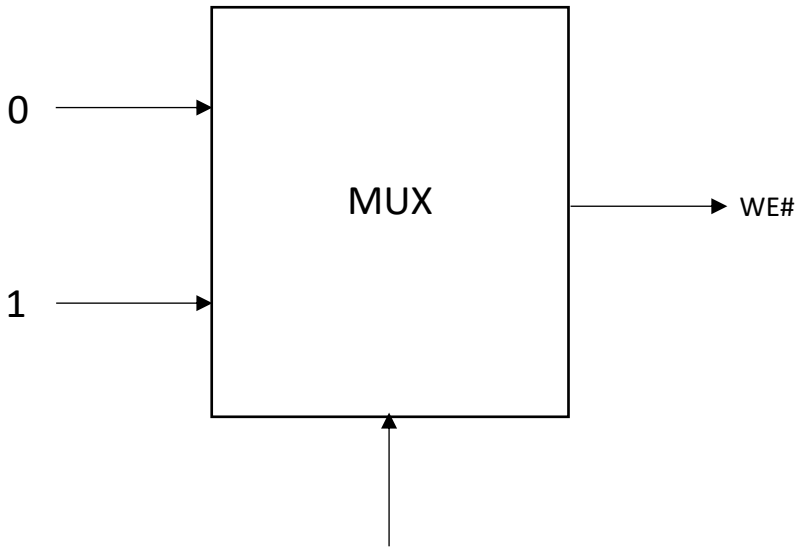
- **Generation of CAS# Signal:**



0: STATE= READ || WRITE || AUTO REFRESH || LMR

1: STATE= NOP || ACTIVE || PRECHARGE

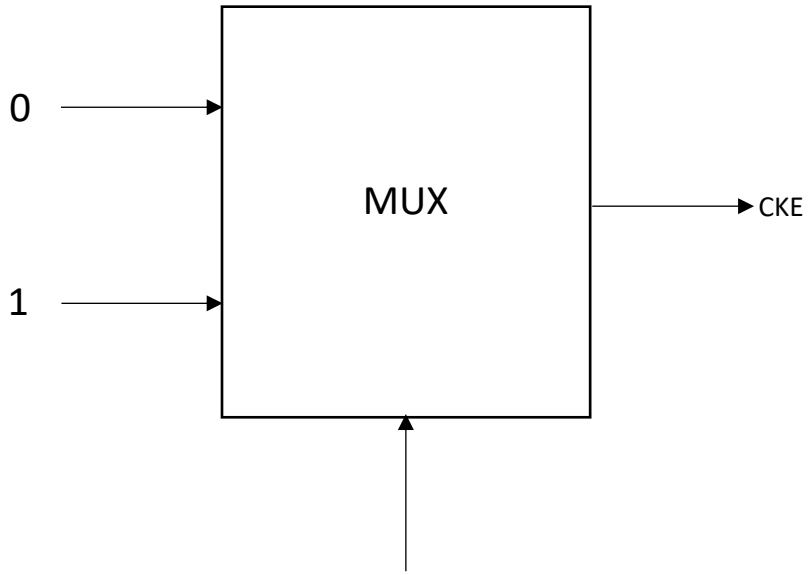
- **Generation of WE# Signal:**



0: WRITE || PRECHARGE || LMR

1: STATE= NOP || ACTIVE || READ || AUTO REFRESH

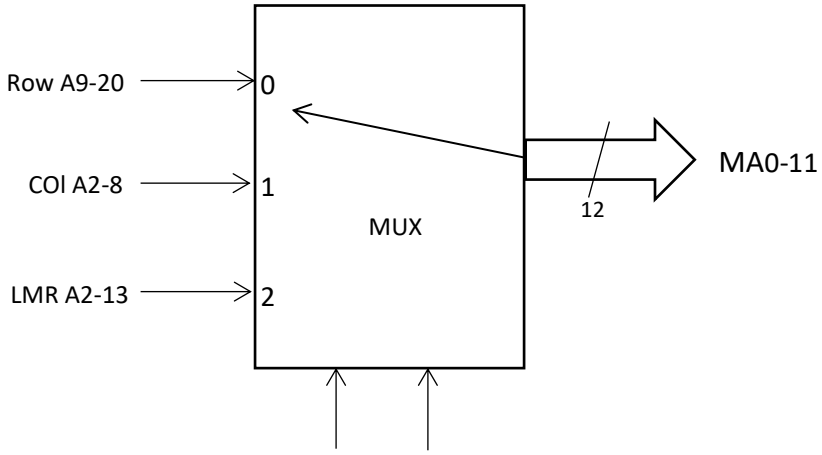
- **Generation of CKE Signal:**



0: STATE= RESET# || WAIT FOR CLK STABLE (PLL) (LOCK=0)

1= STATE = RESET# && WAIT FOR CLK STABLE (PLL) (LOCK=1)

- **Generation of ROW and COLUMN Address:**

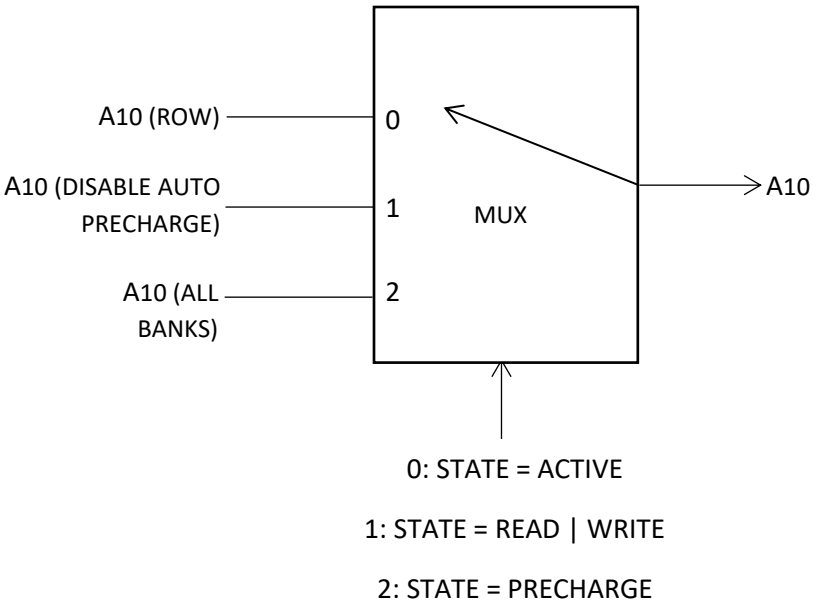


0: STATE = ACTIVE (ROW)

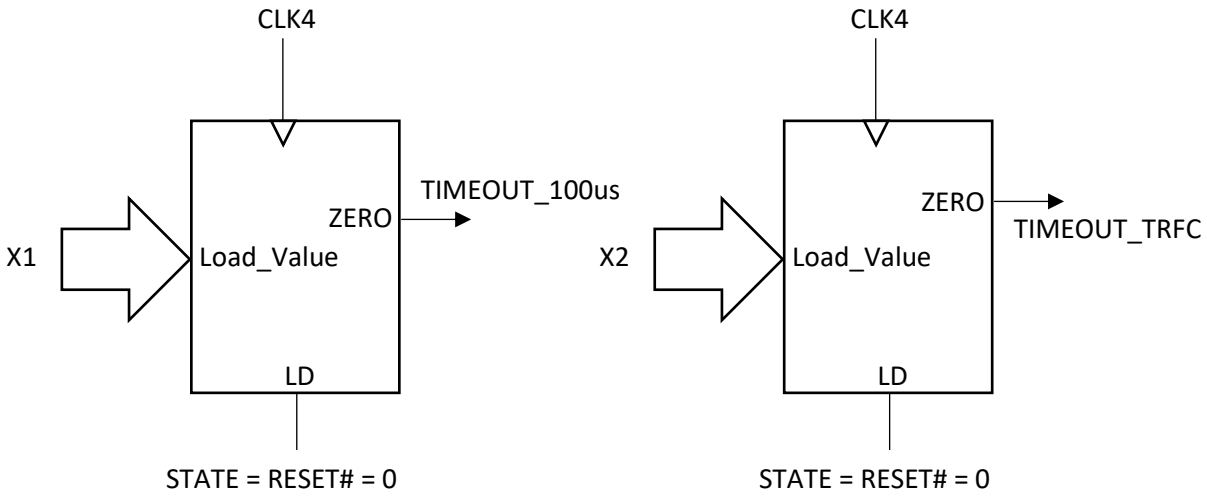
1: STATE = READ | WRITE

2: STATE = LMR

- **Generation of AUTO PRECHARGE (A10) Signal:**



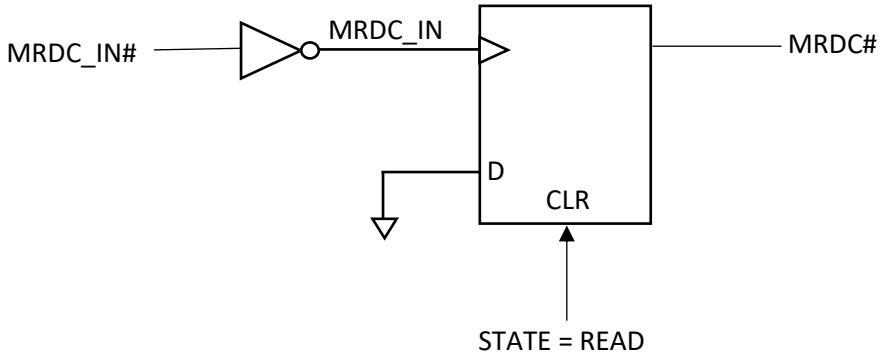
- **Generation of Counter Signal:**



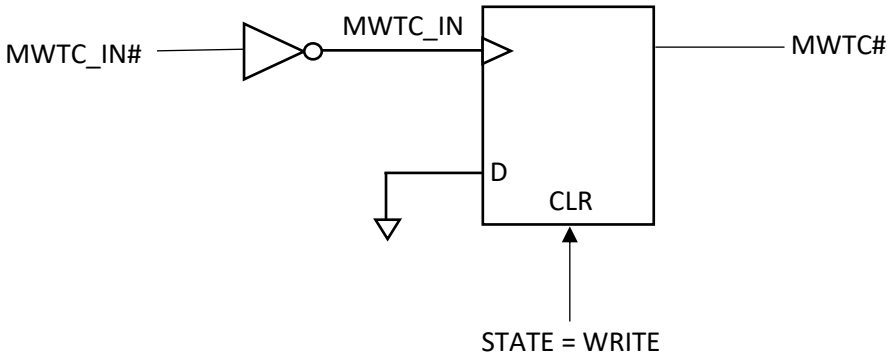
X1 = 100us * 133 MHZ = 13300 count

X2 = 66 ns * 133 MHZ = 9 count

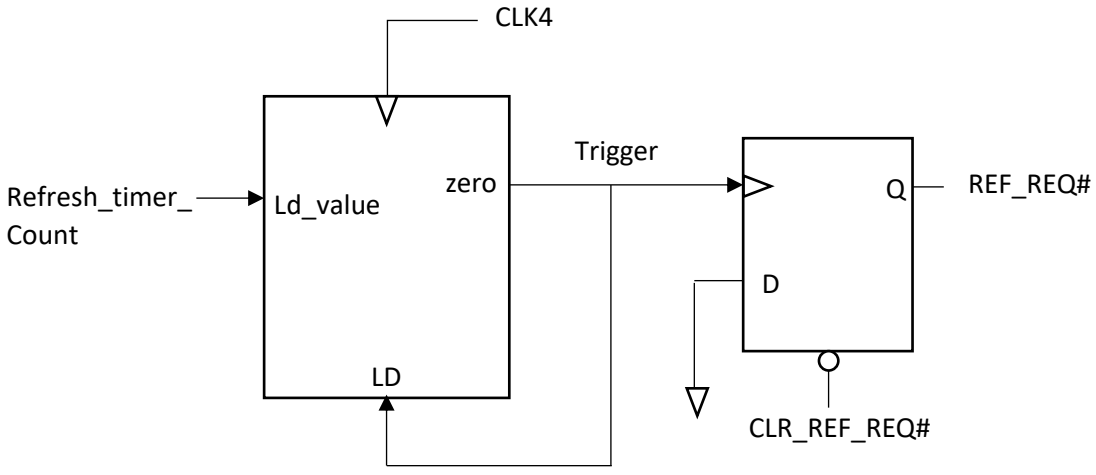
- **Generation of MRDC# Latches:**



- **Generation of MWTC# Latches:**



- **Generation of REFRESH Timer:**



Refresh_timer_Count = 64ms * 133 MHZ = 8512

Extra Credit Implementation

➢ EC Design_1:

- MT48LC8M8A2 Memory Chip (2 Meg x 8 x 4 banks)
- Speed Garde: -7E
- Clock frequency: 133 MHZ
- Clock Period: 7.5 ns
- CAS Latency: 2
- Burst Length: 4
- Refresh Time: 64 ms

➢ Decoder Implementation (BL=4):

DCD_SDRAM#	BA	RA	CA	X X
A31-23	A22-21	A20-9	A8-2	X X

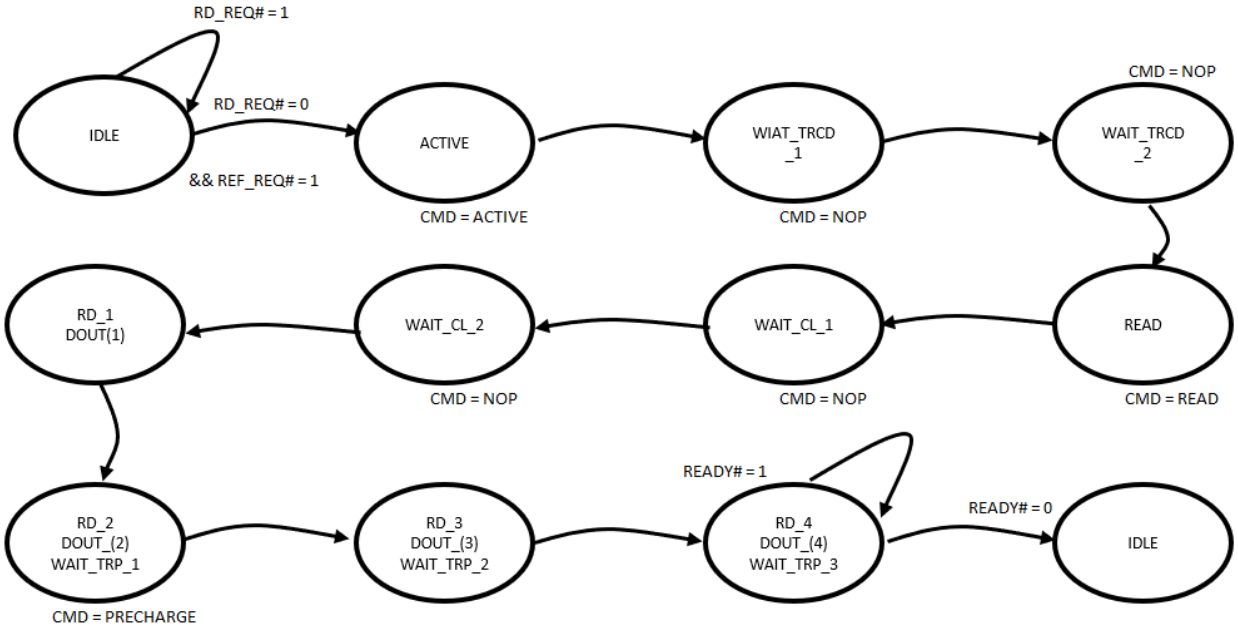
- Decoder Address: A31-23 (9 bit)
- Bank Address: A22-21 (2 bit)
- Row Address: A20-9 (12 bit)
- Column Address: A8-2 (8 bit)

➢ Load Mode Register:

Address Bus	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
Parameter	Reserved		WB	Op Mode		CAS Latency			BT	Burst Length		
Value	0	0	0	0	0	0	1	0	0	0	1	0

- Program: M11, M10: 0, 0: To ensure compatibility with future device
- Write Burst Mode: M9: 0: Program Burst Length
- Operating Mode: M8, M7: 0, 0: Standard Operation
- CAS latency: M6, M5, M4: 0, 1, 0: Two Clock Cycle
- Burst Type: M3: 0: Sequential
- Burst length: M2, M1, M0: 0, 1, 0: Four

➢ Read: Finite State Diagram:



➢ Read: State Transition table:

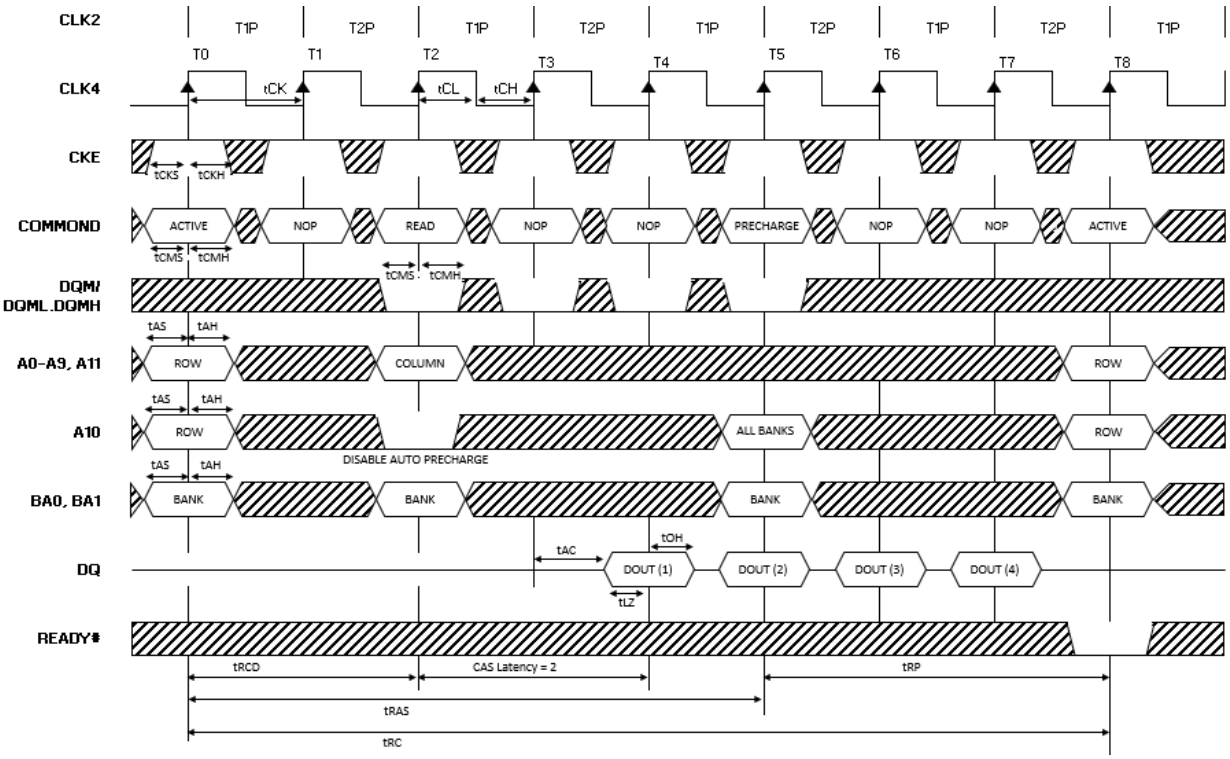
Current State	Condition	Next State
IDLE	RD_REQ# = 1	IDLE
IDLE	RD_REQ# = 0 && REF_REQ# = 1	ACTIVE
ACTIVE	NEXT CLOCK	WAIT_TRCD_1
WAIT_TRCD_1	NEXT CLOCK	WAIT_TRCD_2
WAIT_TRCD_2	NEXT CLOCK	READ
READ	NEXT CLOCK	WAIT_CL_1
WAIT_CL_1	NEXT CLOCK	WAIT_CL_2
WAIT_CL_2	NEXT CLOCK	RD_1/DOUT (1)
RD_1/DOUT (1)	NEXT CLOCK	RD_2/DOUT (2)/WAIT_TRP_1
RD_2/DOUT (2)/WAIT_TRP_1	NEXT CLOCK	RD_3/DOUT (3)/ WAIT_TRP_2
RD_3/DOUT (3)/ WAIT_TRP_2	NEXT CLOCK	RD_4/DOUT (4)/ WAIT_TRP_3
RD_4/DOUT (4)/ WAIT_TRP_3	READY# = 1	RD_4/DOUT (4)/ WAIT_TRP_3
RD_4/DOUT (4)/ WAIT_TRP_3	READY# = 0	IDLE

➢ Read: Output Signal:

Output	Equation
CKE	STATE = NOP | ACTIVE | PRECHARGE |READ |RD_N | IDLE
CS#	STATE = NOP | ACTIVE | PRECHARGE |READ | IDLE
RAS#	STATE = ACTIVE
CAS#	STATE = READ
WE#	STATE = READ

A0-A9/A11	STATE = ACTIVE |READ
A10	STATE = PRECHARGE | READ | ACTIVE
DQs	STATE = RD_1 | RD_2|RD_3|RD_4
DQM	STATE = READ | NOP | RD_1 | RD_2
BA0,BA1	STATE = PRECHARGE |ACTIVE

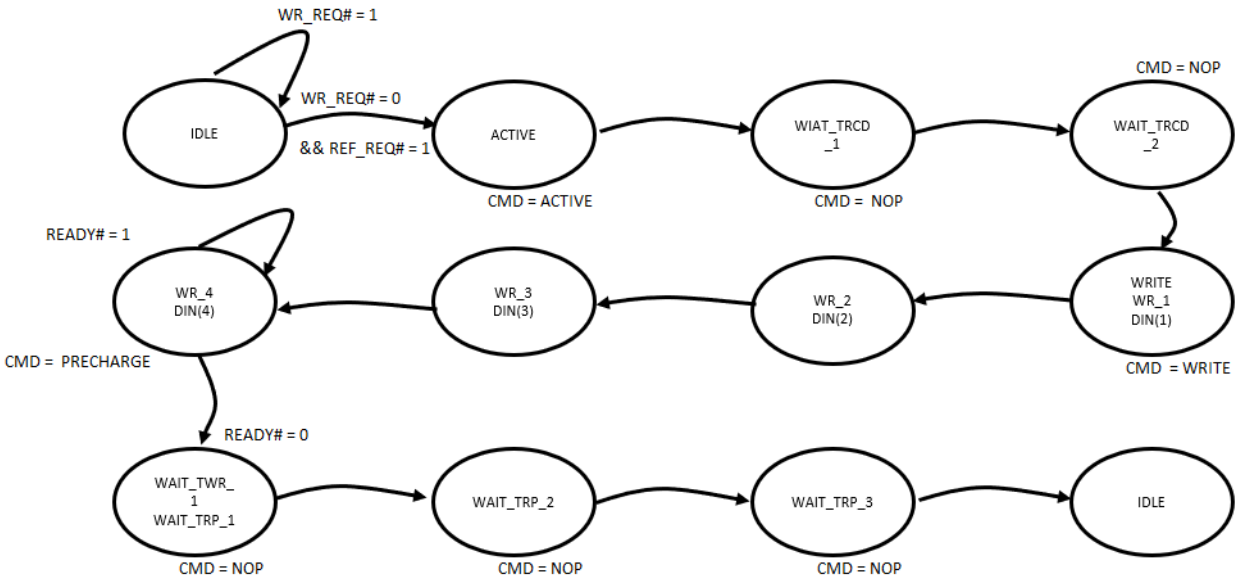
➢ Read: Timing Diagram:



➢ Read: Clock Generation:

Parameter	Symbol	Value (ns)	No. of Clocks Required
Data-out Low-Z time	tLZ	1	-
Access time from CLK (positive edge)	tAC	5.4	-
Data-out hold time (load)	tOH	3	-
Data-out High-Z time	tHZ	5.4	-
ACTIVE-to-READ or WRITE delay	tRCD	15	2
PRECHARGE command period	tRP	22.5	3
ACTIVE-to-PRECHARGE command	tRAS	37	5
ACTIVE-to-ACTIVE command period	tRC	60	8
CAS Latency	CL	15	2

➢ Write: Finite State Diagram:



➢ Write: State Transition table:

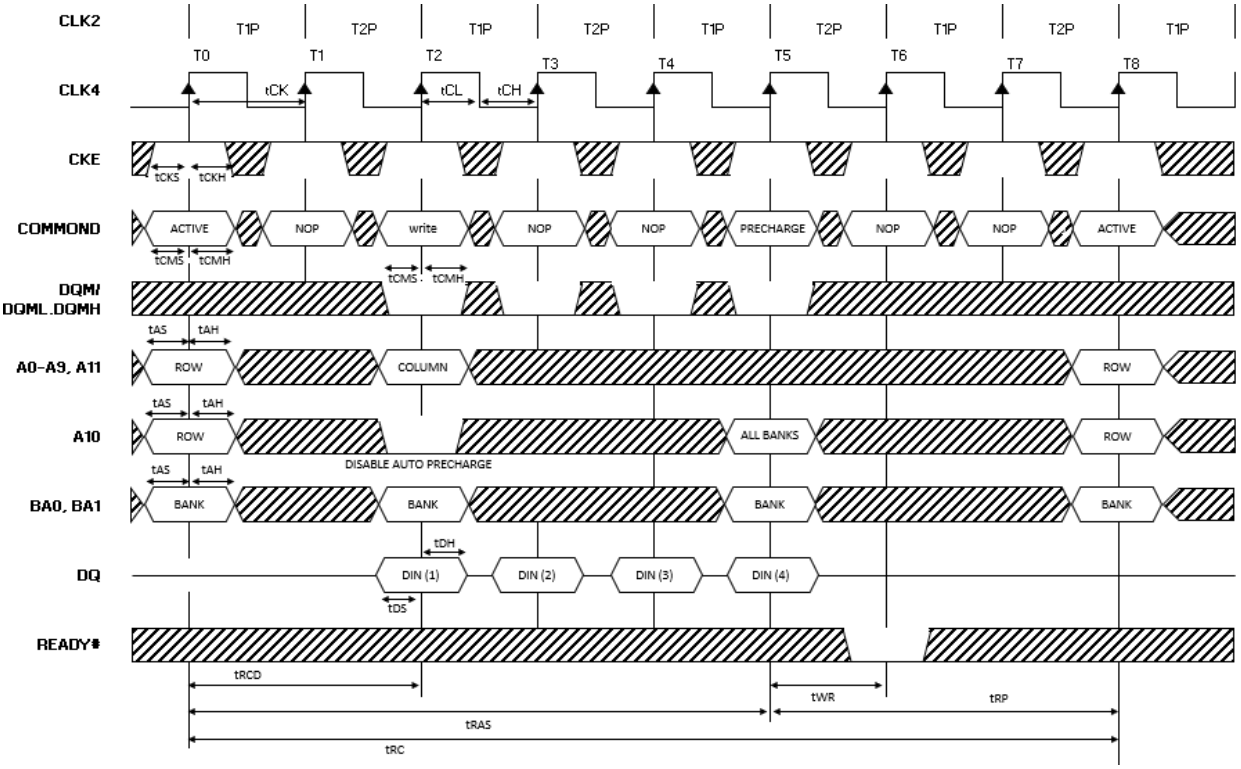
Current State	Condition	Next State
IDLE	WR_REQ# = 1	IDLE
IDLE	WR_REQ# = 0 && REF_REQ# = 1	ACTIVE
ACTIVE	NEXT CLOCK	WAIT_TRCD_1
WAIT_TRCD_1	NEXT CLOCK	WAIT_TRCD_2
WAIT_TRCD_2	NEXT CLOCK	WRITE/WR_1/DIN(1)
WRITE/WR_1/DIN(1)	NEXT CLOCK	WR_2/DIN(2)
WR_2/DIN(2)	NEXT CLOCK	WR_3/DIN(3)
WR_3/DIN(3)	NEXT CLOCK	WR_4/DIN(4)
WR_4/DIN(4)	READY# = 1	WR_4/DIN(4)
WR_4/DIN(4)	READY# = 0	WAIT_TWR_1/WAIT_TRP_1
WAIT_TWR_1/WAIT_TRP_1	NEXT CLOCK	WAIT_TRP_2
WAIT_TRP_2	NEXT CLOCK	WAIT_TRP_3
WAIT_TRP_3	NEXT CLOCK	IDLE

➢ Write: Output Signal:

Output	Equation
CKE	STATE = NOP | ACTIVE | PRECHARGE |WRITE |WR_N | IDLE
CS#	STATE = NOP | ACTIVE | PRECHARGE |WRITE | IDLE
RAS#	STATE = ACTIVE
CAS#	STATE = WRITE
WE#	STATE = WRITE
A0-A9/A11	STATE = ACTIVE | WRITE

A10	STATE = PRECHARGE | WRITE |ACTIVE
DQM	STATE = WR_1 | WR_2|WR_3 |WR_4
DQs	STATE = WR_1 | WR_2 |WR_3 |WR_4
BA0,BA1	STATE = PRECHARGE |ACTIVE

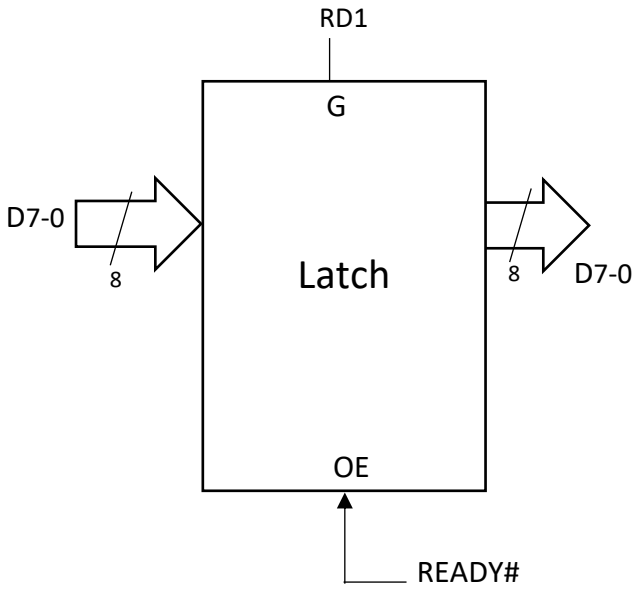
➢ Write: Timing Diagram:

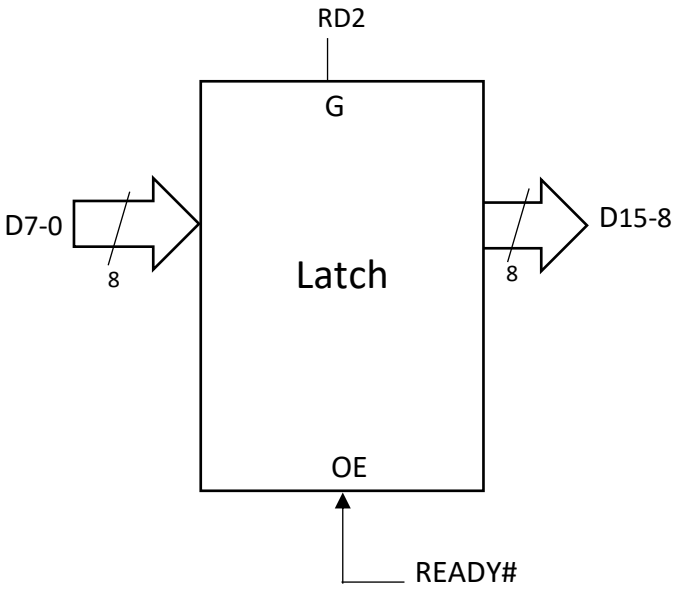


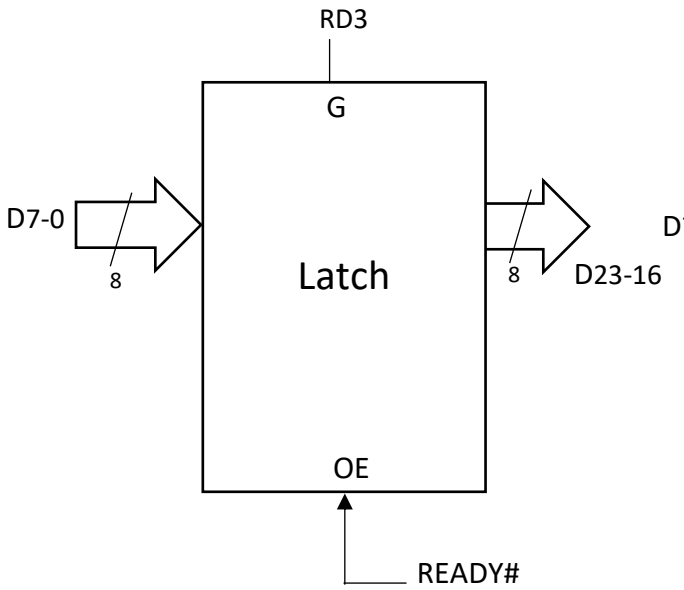
➢ Write: Clock Generation:

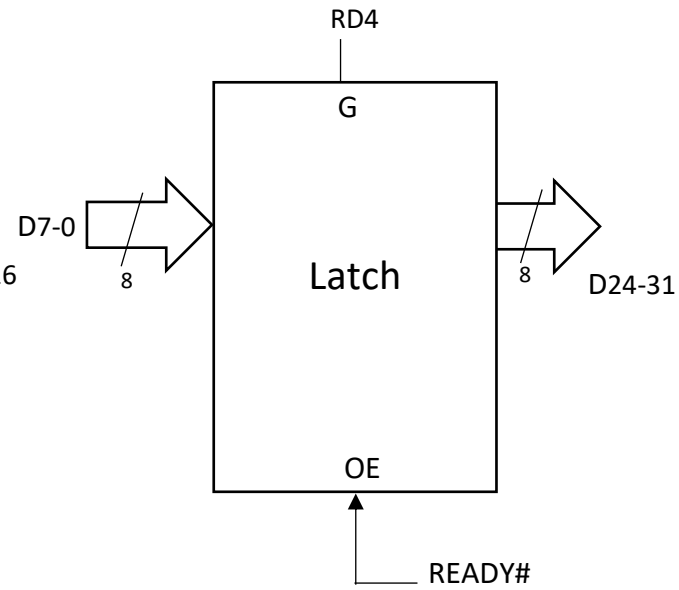
Parameter	Symbol	Value (ns)	No. of Clocks Required
Data-in setup time	tDS	1.5	-
Data-in hold time	tDH	0.8	-
ACTIVE-to-READ or WRITE delay	tRCD	15	2
WRITE recovery time	tWR	7.5	2
PRECHARGE command period	tRP	22.5	3
ACTIVE-to-PRECHARGE command	tRAS	37	5
ACTIVE-to-ACTIVE command period	tRC	60	8

- **Generation of Chip Signals:**
  - **Read Data Latch:**

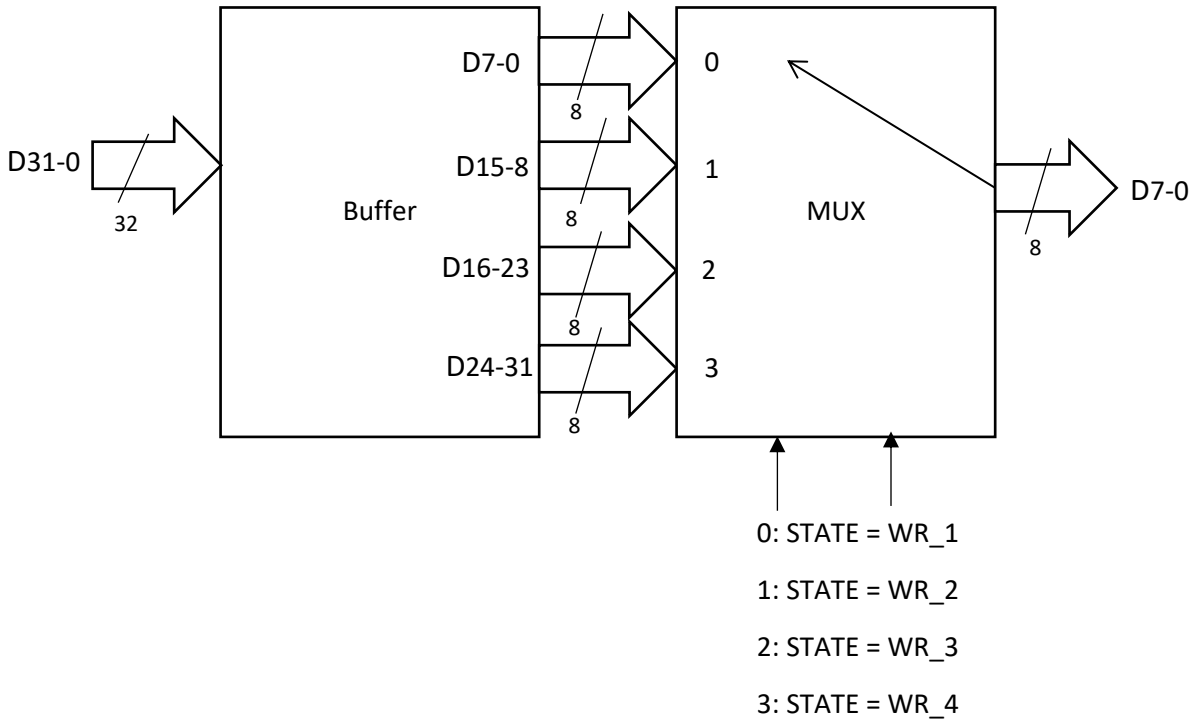


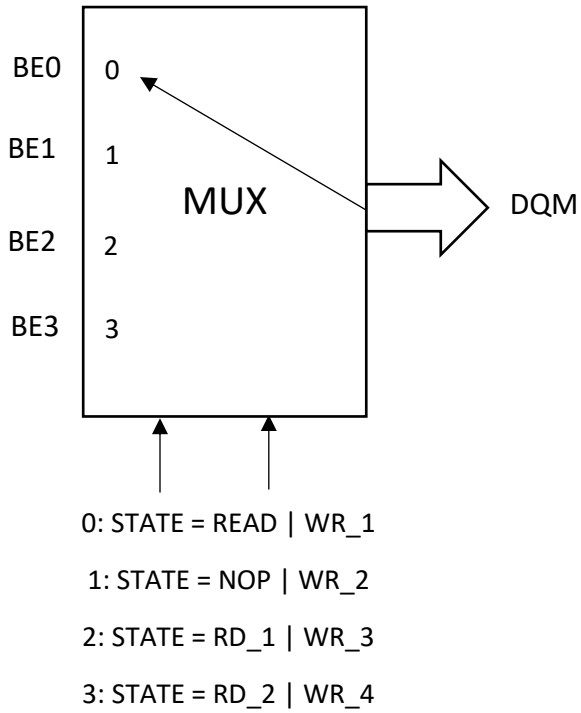






- **Write Data Latch:**





➢ EC Design_2:

- MT48LC16M4A2 Memory Chip (16 Meg x 4 x 4 banks)
- Speed Garde: -7E
- Clock frequency: 133 MHZ
- Clock Period: 7.5 ns
- CAS Latency: 2
- Burst Length: 8
- Refresh Time: 64 ms

➢ Decoder Implementation (BL=8):

DCD_SDRAM#	BA	RA	CA	X X
A31-23	A22-21	A20-9	A8-2	X X

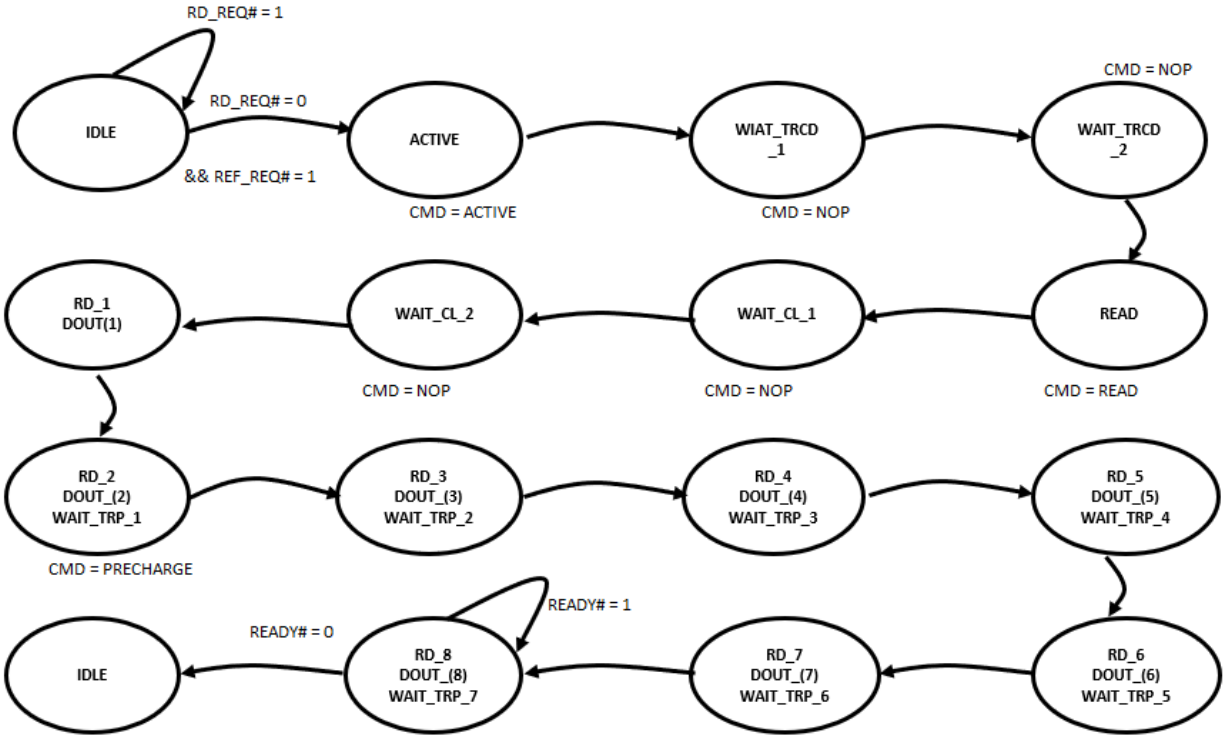
- Decoder Address: A31-23 (9 bit)
- Bank Address: A22-21 (2 bit)
- Row Address: A20-9 (12 bit)
- Column Address: A8-2 (8 bit)

➢ Load Mode Register:

Address Bus	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
Parameter	Reserved		WB	Op Mode		CAS Latency			BT	Burst Length		
Value	0	0	0	0	0	0	1	0	0	0	1	1

- Program: M11, M10: 0, 0: To ensure compatibility with future device
- Write Burst Mode: M9: 0: Program Burst Length
- Operating Mode: M8, M7: 0, 0: Standard Operation
- CAS latency: M6, M5, M4: 0, 1, 0: Two Clock Cycle
- Burst Type: M3: 0: Sequential
- Burst length: M2, M1, M0: 0, 1, 0: Eight

➢ Read: Finite State Diagram:



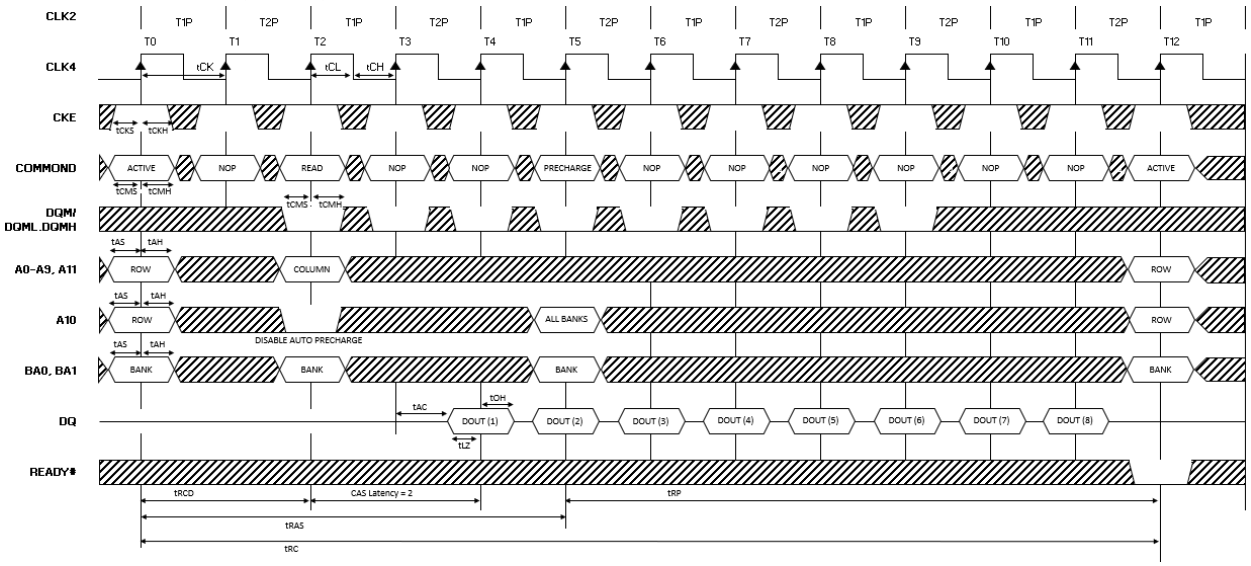
➢ Read: State Transition table:

Current State	Condition	Next State
IDLE	RD_REQ# = 1	IDLE
IDLE	RD_REQ# = 0 && REF_REQ# = 1	ACTIVE
ACTIVE	NEXT CLOCK	WAIT_TRCD_1
WAIT_TRCD_1	NEXT CLOCK	WAIT_TRCD_2
WAIT_TRCD_2	NEXT CLOCK	READ
READ	NEXT CLOCK	WAIT_CL_1
WAIT_CL_1	NEXT CLOCK	WAIT_CL_2
WAIT_CL_2	NEXT CLOCK	RD_1/DOUT(1)
RD_1/DOUT(1)	NEXT CLOCK	RD_2/DOUT(2)/WAIT_TRP_1
RD_2/DOUT(2)/WAIT_TRP_1	NEXT CLOCK	RD_3/DOUT(3)/ WAIT_TRP_2
RD_3/DOUT(3)/ WAIT_TRP_2	NEXT CLOCK	RD_4/DOUT(4)/ WAIT_TRP_3
RD_4/DOUT(4)/ WAIT_TRP_3	NEXT CLOCK	RD_5/DOUT(5)/ WAIT_TRP_4
RD_5/DOUT(5)/ WAIT_TRP_4	NEXT CLOCK	RD_6/DOUT(6)/ WAIT_TRP_5
RD_6/DOUT(6)/ WAIT_TRP_5	NEXT CLOCK	RD_7/DOUT(7)/ WAIT_TRP_6
RD_7/DOUT(7)/ WAIT_TRP_6	NEXT CLOCK	RD_8/DOUT(8)/ WAIT_TRP_7
RD_8/DOUT(8)/ WAIT_TRP_7	READY#=1	RD_8/DOUT(8)/ WAIT_TRP_7
RD_8/DOUT(8)/ WAIT_TRP_7	READY#=0	IDLE

➢ Read: Output Signal:

Output	Equation
CKE	STATE = NOP | ACTIVE | PRECHARGE |READ |RD_N | IDLE
CS#	STATE = NOP | ACTIVE | PRECHARGE |READ | IDLE
RAS#	STATE = ACTIVE
CAS#	STATE = READ
WE#	STATE = READ
A0-A9/A11	STATE = ACTIVE |READ
A10	STATE = PRECHARGE | READ | ACTIVE
DQs	STATE = RD_1 | RD_2|RD_3|RD_4|RD_5|RD_6|RD_7|RD_8
DQM	STATE = READ | NOP | RD_1 | RD_2|RD_3|RD_4|RD_5|RD_6
BA0, BA1	STATE = PRECHARGE |ACTIVE

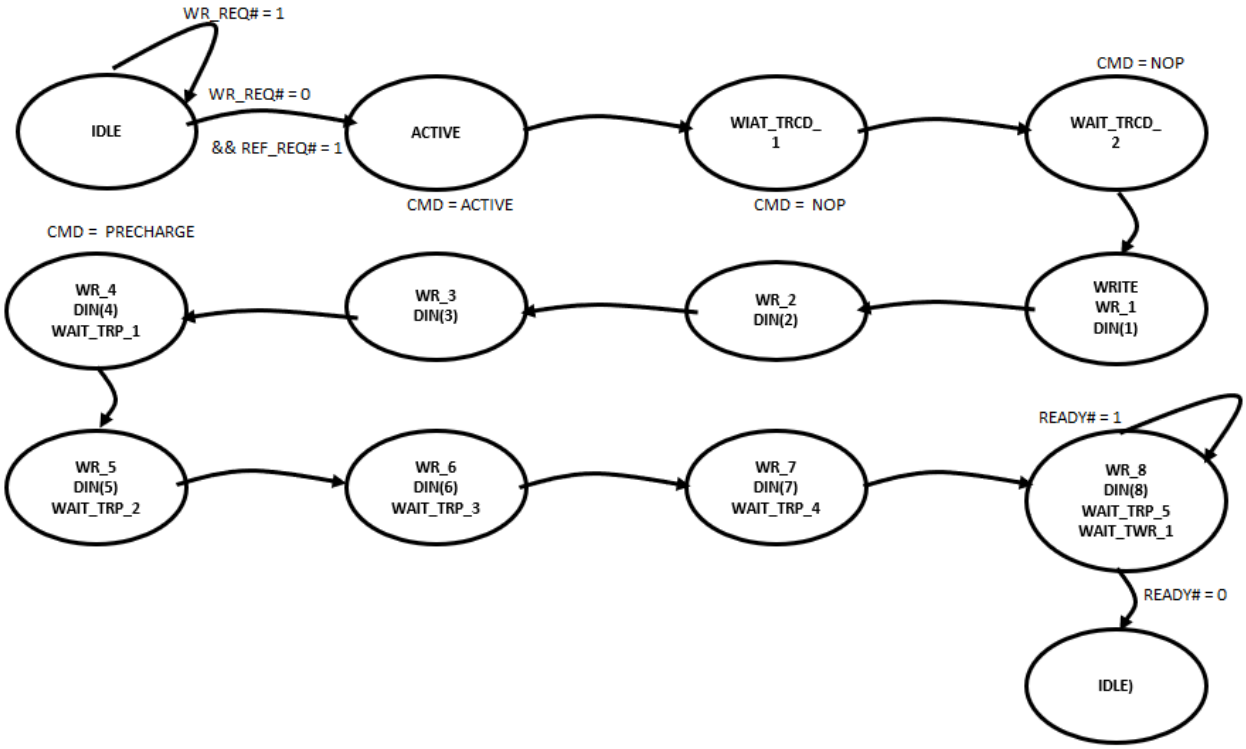
➢ Read: Timing Diagram:



➢ Read: Clock Generation:

Parameter	Symbol	Value (ns)	No. of Clocks Required
Data-out Low-Z time	tLZ	1	-
Access time from CLK (positive edge)	tAC	5.4	-
Data-out hold time (load)	tOH	3	-
Data-out High-Z time	tHZ	5.4	-
ACTIVE-to-READ or WRITE delay	tRCD	15	2
PRECHARGE command period	tRP	52.5	7
ACTIVE-to-PRECHARGE command	tRAS	37	5
ACTIVE-to-ACTIVE command period	tRC	90	12
CAS Latency	CL	15	2

➢ Write: Finite State Diagram:



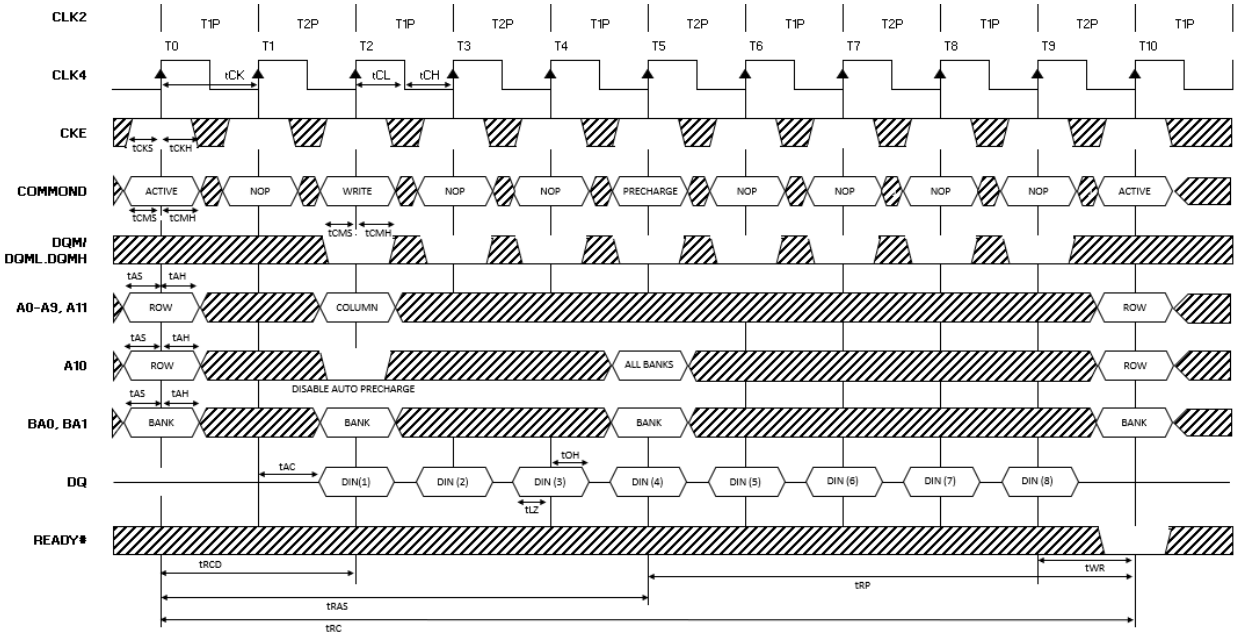
➢ Write: State Transition table:

Current State	Condition	Next State
IDLE	WR_REQ# = 1	IDLE
IDLE	WR_REQ# = 0 && REF_REQ# = 1	ACTIVE
ACTIVE	NEXT CLOCK	WAIT_TRCD_1
WAIT_TRCD_1	NEXT CLOCK	WAIT_TRCD_2
WAIT_TRCD_2	NEXT CLOCK	WRITE/WR_1/DIN (1)
WRITE/WR_1/DIN (1)	NEXT CLOCK	WR_2/DIN (2)
WR_2/DIN (2)	NEXT CLOCK	WR_3/DIN (3)
WR_3/DIN (3)	NEXT CLOCK	WR_4/DIN (4)/ WAIT_TRP_1
WR_4/DIN (4)/ WAIT_TRP_1	NEXT CLOCK	WR_5/DIN (5)/ WAIT_TRP_2
WR_5/DIN (5)/ WAIT_TRP_2	NEXT CLOCK	WR_6/DIN (6)/ WAIT_TRP_3
WR_6/DIN (6)/ WAIT_TRP_3	NEXT CLOCK	WR_7/DIN (7)/ WAIT_TRP_4
WR_7/DIN (7)/ WAIT_TRP_4	NEXT CLOCK	WR_8/DIN (8)/ WAIT_TRP_5 WAIT_TWR_1
WR_8/DIN (8)/ WAIT_TRP_5 WAIT_TWR_1	READY# = 1	WR_8/DIN (8)/ WAIT_TRP_5 WAIT_TWR_1
WR_8/DIN (8)/ WAIT_TRP_5 WAIT_TWR_1	READY# = 0	IDLE

➢ Write: Output Signal:

Output	Equation
CKE	STATE = NOP | ACTIVE | PRECHARGE |WRITE |WR_N | IDLE
CS#	STATE = NOP | ACTIVE | PRECHARGE |WRITE | IDLE
RAS#	STATE = ACTIVE
CAS#	STATE = WRITE
WE#	STATE = WRITE
A0-A9/A11	STATE = ACTIVE | WRITE
A10	STATE = PRECHARGE | WRITE |ACTIVE
DQM	STATE = WR_1 | WR_2|WR_3 |WR_4|WR_5|WR_6|WR_7|WR_8
DQs	STATE = WR_1 | WR_2 |WR_3 |WR_4|WR_5|WR_6|WR_7|WR_8
BA0, BA1	STATE = PRECHARGE |ACTIVE

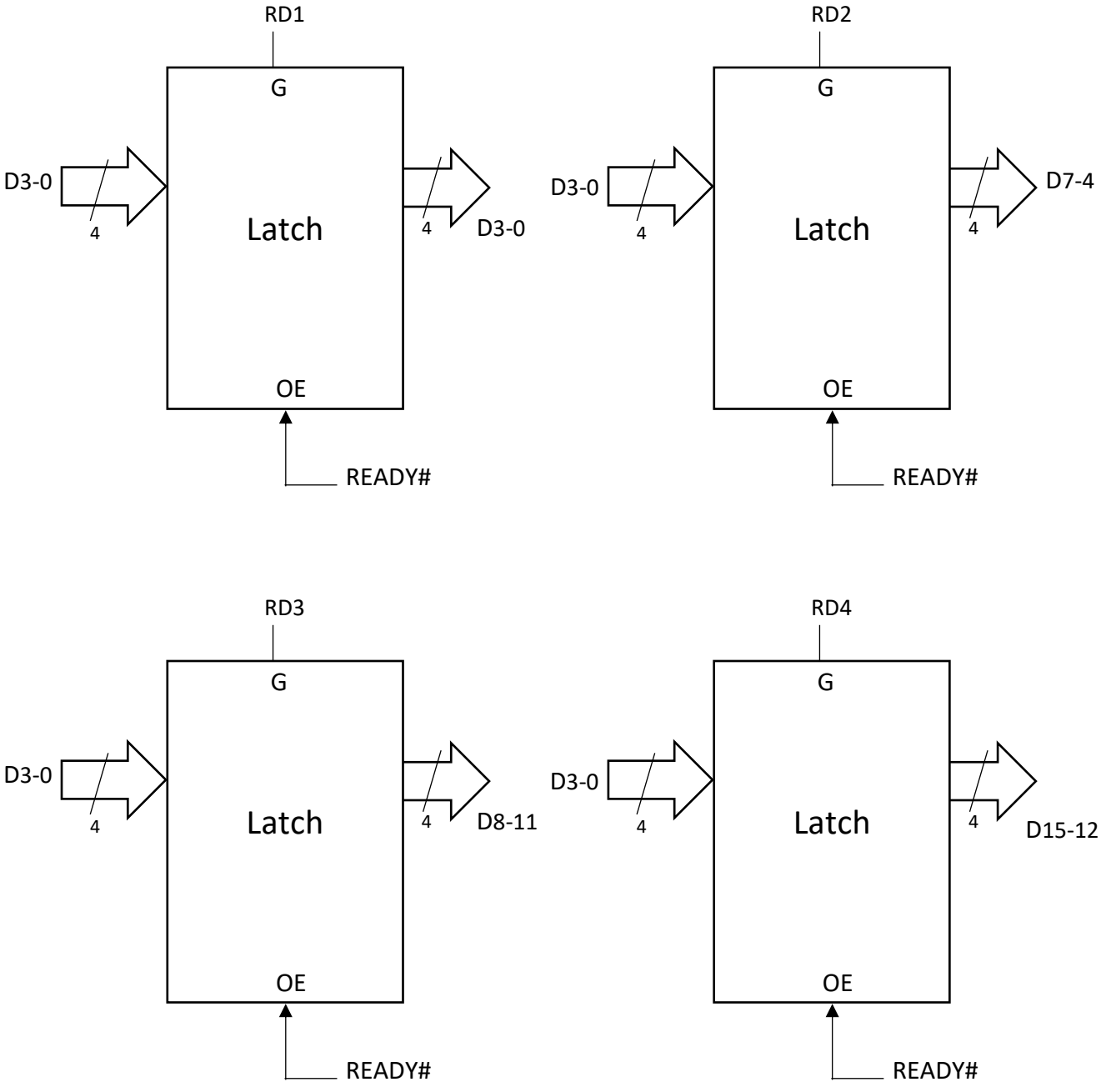
➢ Write: Timing Diagram:

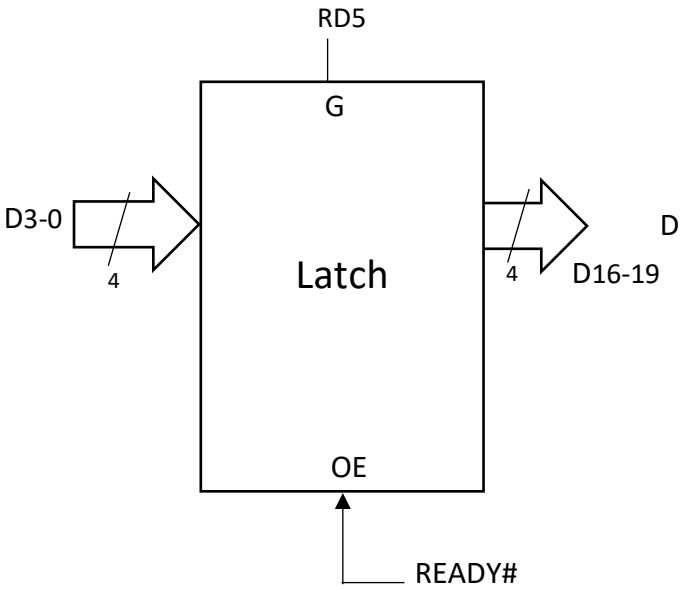


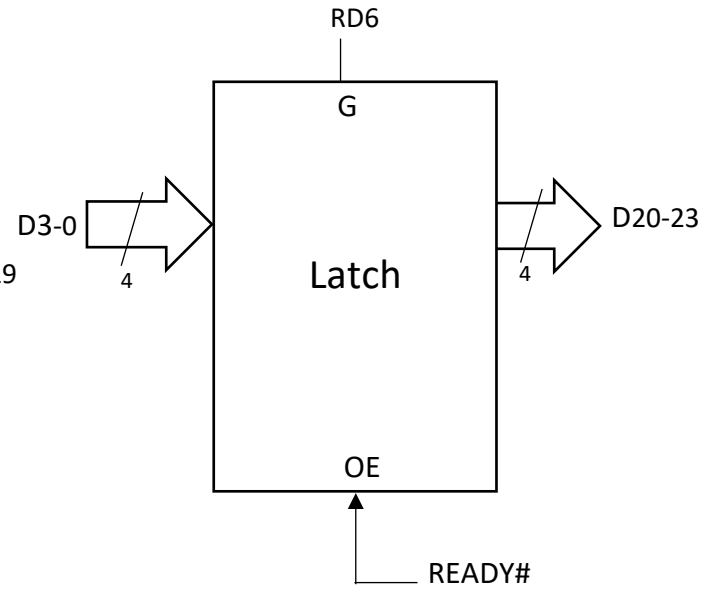
➢ Write: Clock Generation:

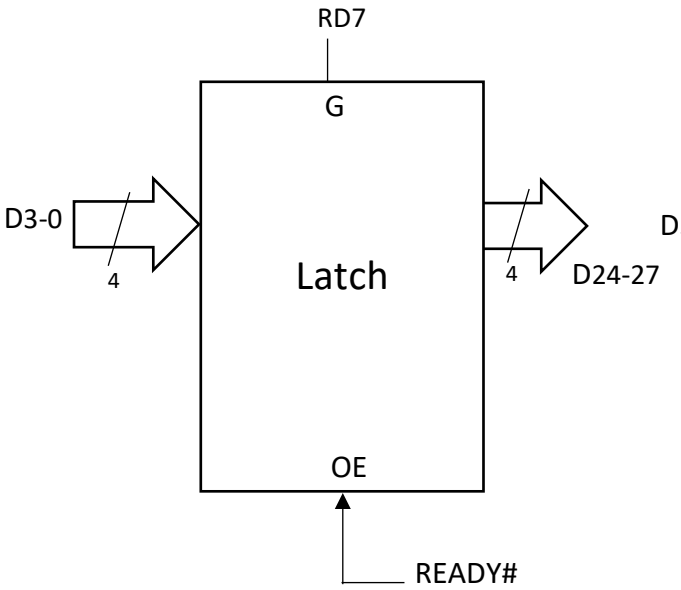
Parameter	Symbol	Value (ns)	No. of Clocks Required
Data-in setup time	tDS	1.5	-
Data-in hold time	tDH	0.8	-
ACTIVE-to-READ or WRITE delay	tRCD	15	2
WRITE recovery time	tWR	7.5	2
PRECHARGE command period	tRP	37.5	5
ACTIVE-to-PRECHARGE command	tRAS	37	5
ACTIVE-to-ACTIVE command period	tRC	75	10

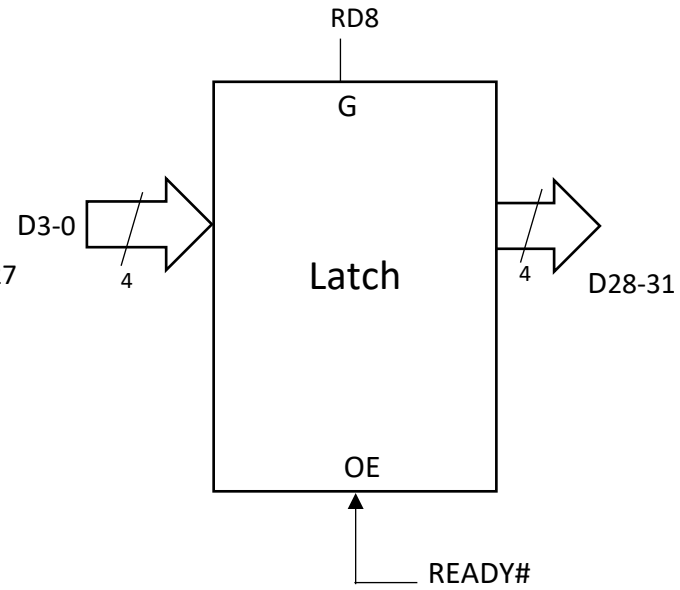
- **Generation of Chip Signals:**
  - **Read Data Latch:**



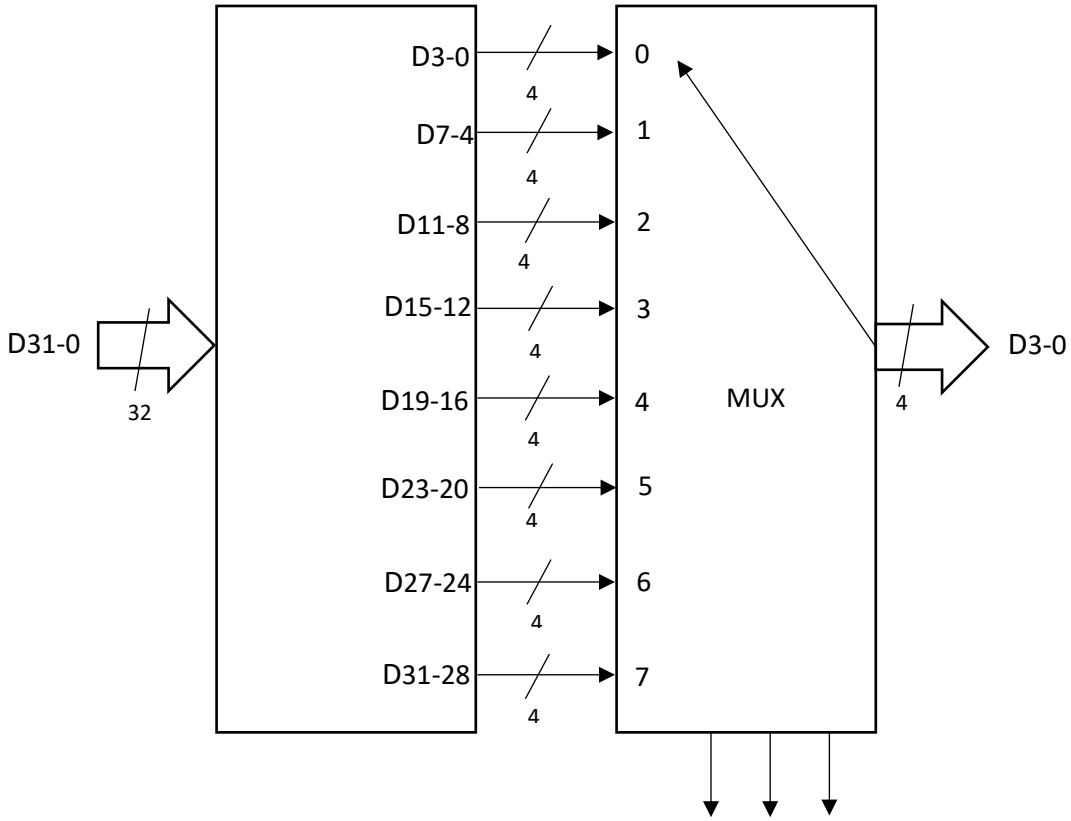

RD5
G
D3-0
4
Latch
4
D16-19
OE
READY#

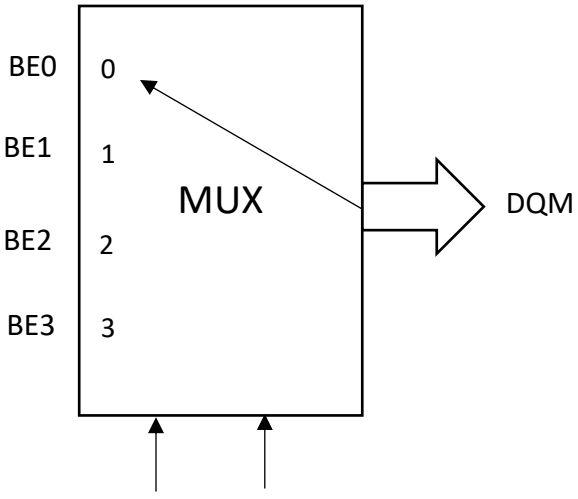

RD6
G
D3-0
4
Latch
4
D20-23
OE
READY#


RD7
G
D3-0
4
Latch
4
D24-27
OE
READY#


RD8
G
D3-0
4
Latch
4
D28-31
OE
READY#

- **Write Data Latch:**





0: STATE = WR_1

1: STATE = WR_2

2: STATE = WR_3

3: STATE = WR_4

4: STATE = WR_5

5: STATE = WR_6

6: STATE = WR_7

7: STATE = WR_8

0: STATE = READ | NOP | WR_1 | WR_2

1: STATE = RD_1 | RD_2 | WR_3 | WR_4

2: STATE = RD_3 | RD_4 | WR_5 | WR_6

3: STATE = RD_5 | RD_6 | WR_7 | WR_8