VIT

Vellore Institute of Technology

SCHOOL OF ELECTRONICS ENGINEERING

CAT – I (25/08/2024)

Fall Semester 2024 - 2025

B.Tech – in VLSI Design

Class Number: VL2024250104065
Course Name: BEVD204L, Electronic Circuits
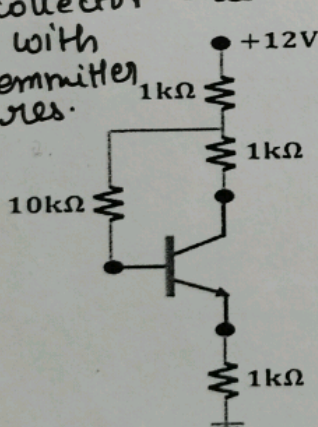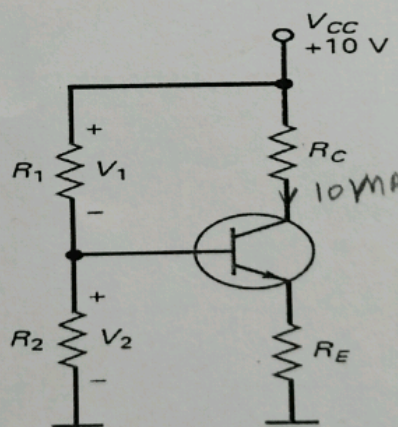Faculty-In-Charge: Abdul Majeed K. K

Time : 09.30 AM – 11.00 AM
Max. Marks : 50
Slot : A1 + TA1

Answer **ALL** Questions

Assume data wherever necessary.

| S.No.	Section – A Question	Max. Marks
1.	a). Define stability factor and derive the stability factor of Common base BJT configuration. b) What is mean by Operating point? Derive the expression for the I_B, I_C and V_{CE} of the base biased with collector feedback BJT circuits.	10
2.	a) A transistor having $\alpha = 0.99$ and $V_{BE} = 0.7$ is used in the circuit shown in Fig. 1 below. Calculate the currents I_C, I_B, I_E (4 M) collector bias with emmitter res. Fig. 1 Fig.2 b) Determine the resistor values to meet this specification given below for the circuit shown in Fig.2 (6 M) Vcc=10 V, I_C= 10m A, V_{CE} @ midpoint and $\beta=100$	10
	Calculate the base, collector, emitter currents, power dissipation and the C-E voltage for a common emitter circuit shown in Fig. 3. Assume $V_{BB} = 7$ V, $V_{CC} = 12$ V, $R_C = 4k\ \Omega$, $R_B = 200k\ \Omega$ and $\beta =300$. Calculate operating point using graphical method and find out I_{CQ} and V_{CEQ}.	10
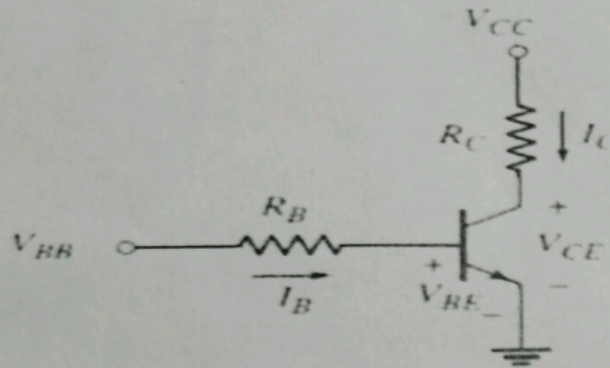
Fig.3

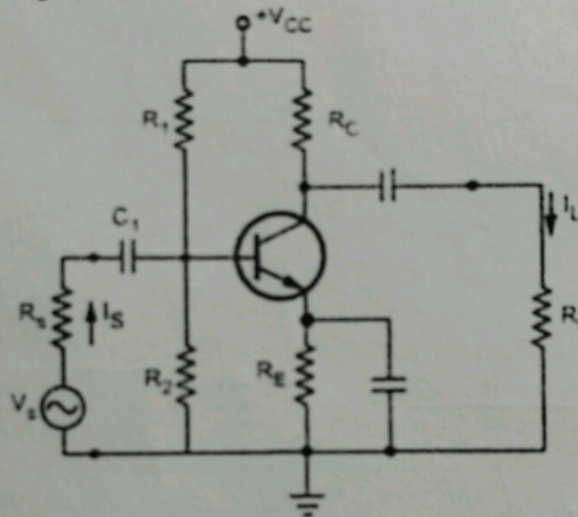| 4.	Consider a single stage CE amplifier with $R_s = 1k\Omega$, $R_1 = 50\ K\Omega$, $R_2 = 2\ K\Omega$, $R_C = 1\ K\Omega$, $R_L = 1.2\ K\Omega$, $h_{fe} = 50$, $h_{ie} = 1.1\ K$, $hoe = 25\mu\ A/V$ and $hre = 2.5\ x\ 10^{-4}$, as shown in Fig.4. Find A_i, R_i, A_v, A_{vs}, A_{IS} and R_0.	10

Fig.4

5.	Design and implement a circuit to realise the following wave form given in Fig. 5 using OP-AMP	10

Fig.5