A Low Power 4th Order Low Pass Gm-C Filter in 130nm CMOS

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Abstract: A Low Voltage, Low Power 4th order Gm-C Elliptic filter is proposed in this paper. For supply voltage of 1.4V, the Operational Transconductance Amplifier is designed to dissipate low Power of 1.4mW. The two stage fully differential Operational Transconductance Amplifier is designed in 130nm CMOS technology for high linearity and large Output Voltage swing. The Filter is designed using Mentor Graphics tools and the simulation for an input voltage of 150mV (PP), a Total Harmonic Distortion of less than -60dB is achieved.

Keywords: Transconductance, Elliptic Filter, Biquad, Harmonic distortion, Common Mode Feedback, Continuous Time, Voltage Swing.

I. Introduction

Two Methods of filtering technique are widely used in most of the applications, Switched capacitor filter and Continuous Time filter. The former has the advantage of accurate corner frequency; however, it has issues such as aliasing, trade-off in choosing sample rate, effects of sample and hold circuit and noise [1]. This has led to the design complexity of these filters, Moreover the power consumption is more and occupies large silicon area. The later even though does not have accurate corner frequency; it can be designed for a wider dynamic range. Gm-C filter is one of the popular continuous time filters which is widely used in both higher frequency range applications of up to 2GHz and Low frequency range applications from 0.1 Hz. Applications such as WiMax, Hand held devices, Sensor's readout circuit, Medical signal conditioning, Seismic and other Wireless Communications are attracted towards these filters.

One of the major challenge in designing the Gm-C filter in Deep Submicron technology is the short channel effects [2], [3], this can cause non linearity, ways to reduce this nonlinearity must be found. Also there is a variation in cut-off frequency due to temperature and supply voltage variations. Even though Gm-C filters are preferred for their ease of full integration on chip capability; their power dissipation is very high. In most of the previous work, in order to reduce the power consumption, supply voltages are reduced and the transistors are scaled down, however these filters designed with Operational Transconductance Amplifier provides only maximum of 400mV Output Voltage swing. This is due to the increase in overdrive voltage of the transistors. This paper proposes a design which overcomes all these limitations with low noise.

The paper is organized as, in section II the design of OTA is discussed, in section III the Overall design of the Elliptic Filter topology is described and in section IV Simulation results are proved.

II. OTA Design

In most of the design where filter's attenuation is critical, the Transconductance of the OTA must be designed carefully so that it must not affect the gain provided by the previous stage [4]. To maintain the gain of the previous Transconductance stage of the filter, it is important to maintain a proper biasing current. The biasing current will decide the gm of the particular stage.

There is a trade-off between biasing current and the output voltage swing. As the biasing current is chosen appropriately to obtain a proper gm, overdrive voltage increases as they are inversely proportional and hence the output voltage swing decreases. A two stage fully differential OTA is designed in this paper to achieve an output voltage swing of 600mV. Also in Deep Submicron technology to reduce the second order effects, the aspect ratio of the transistors must be designed appropriately. The design of OTA with Common mode feedback circuit is shown in Figure 1[4].

Transistors Q1 to Q6 forms the fully differential first stage of the OTA, Q1 and Q2 are the input transistors and has diode connected loads Q5 & Q6. Cascoded load is avoided so that there will be sufficient headroom for the desired output swing. The bias current for this stage is provided by transistors Q3 & Q4. A bias circuit was also designed with NMOS transistors as a current source and PMOS as current mirror circuit, so that the design will have robustness to corner frequency variation because of temperature and power supply variations.

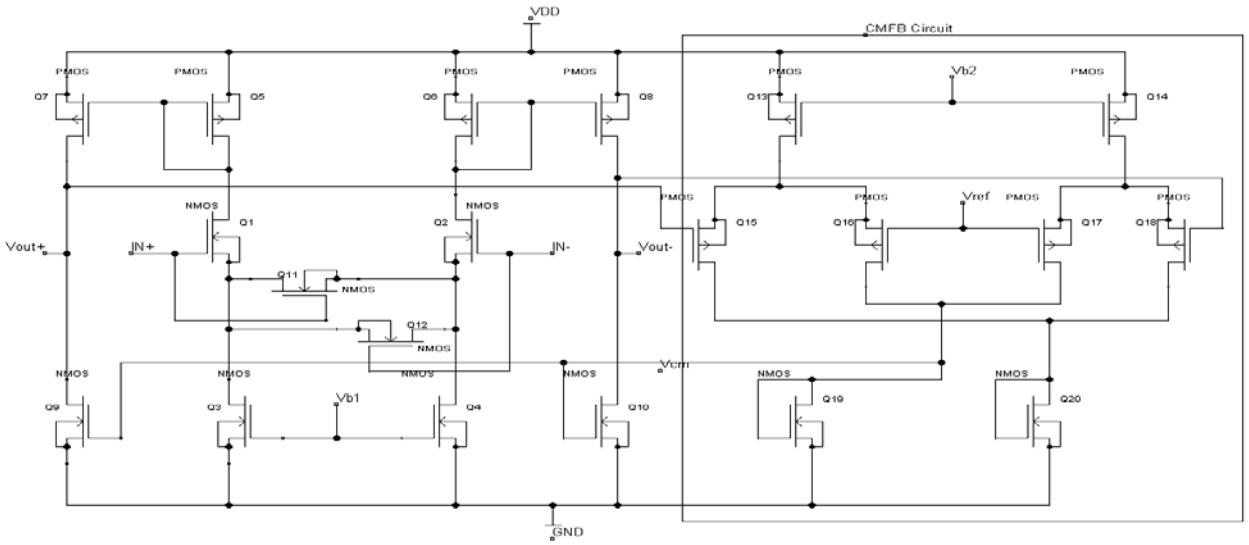

Figure 1. OTA Schematic with CMFB.

All transistors are kept in saturation and their aspect ratios are optimised to get the desired Transconductance.

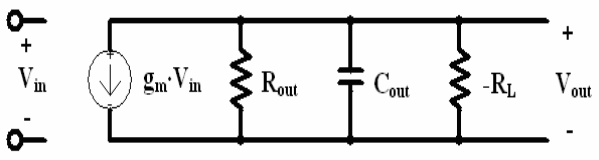

Figure 2. Small Signal model of OTA with negative resistive load

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{sC_{out} + \frac{1}{R_{out}} - \frac{1}{R_L}} \quad (1)$$

The Output impedance of the single stage amplifier is low; hence the gain will also be low. In order to overcome the attenuation caused by the first stage, a second stage of common source amplifier Transistors Q7 to Q10 is included in this design. Transistors Q11 and Q12 is connected to form source degeneration, which provides linearity for higher cut-off frequencies. These transistors aspect ratios are kept lower than the input transistors and are biased in triode region, so that power consumption will be less.

To further increase the Output impedance without introducing unwanted poles, a negative resistance load is included so that the design will resemble almost like an ideal integrator [5]. The equivalent circuit is shown in Figure 2. The Fully differential amplifier's common mode voltage has to be stabilized by adjusting the common mode output current. For this reason Common mode feedback circuit is employed in this design.

The Differential Difference Amplifier which is a Continuous Time CMFB is employed here [4]. Although DDA is linear only for limited input range, the aspect ratio is chosen smaller to operate for larger Voltage swing.

The DDA shown in Figure 1 uses four identical transistors (Q15 – Q18) to average and compare the common mode voltage. A common mode voltage reference of 0.6V is given to the gates of transistors Q16 & Q17 and the voltage output of OTA is fed to the gates of Q15 & Q18. The output common mode Voltage is obtained from the source of transistors Q16 & Q17 which has a diode connected load. The common mode output voltage is feedback to the gates of transistors Q9 & Q10 that will adjust the common mode level of the fully differential amplifier

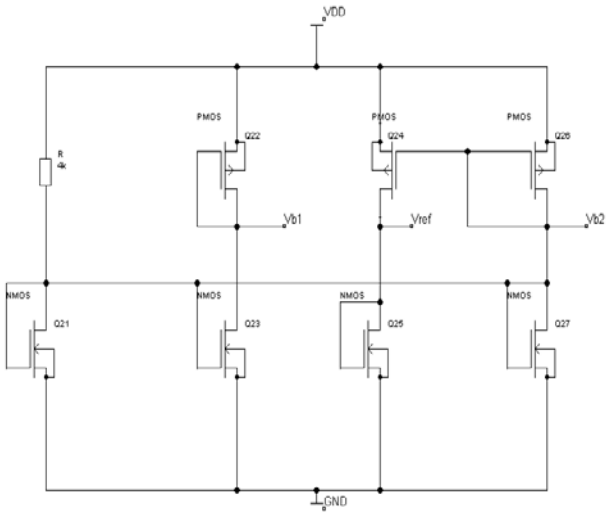

Figure 3 Biasing Circuit for OTA

The Biasing Circuit in Figure 3 is designed to bias the OTA. Transistor Q21 acts as a current source and the drain current of Q21 is copied and scaled by Q23 & Q27; the drain outputs of these transistor provides stable biasing current and their drain voltages Vb1 and Vb2 biases the OTA transistors Q3, Q4 and Q13, Q14 respectively. Transistors Q24 – Q27 are designed as a cascode current source to scale down the biasing voltage to obtain V_{ref}, which is the Common mode reference voltage to the CMFB Circuit.

III. Filter Design

Elliptic filters are important in applications requiring sharp magnitude response. They are preferred in wireless communication and sensor readout circuit because their ripples are divided in both pass band and stop band unlike Chebyshev filter. Biquad Circuit has the advantage of ease in cascaded design; hence a Biquad structure is used as the first stage [6],[7].

The Topology of the 4th order elliptic filter is shown in figure 4. Three Transconductance gm_1, gm_2 and gm_3 with C1 and C2, forms the second order Biquad structure [6],[7]. This Biquad structure is preferred for its low power consumption unlike the Biquad in [4]. Two first order filters are cascaded in the later stages instead of cascading Biquad, thus further reducing the area and power requirement. Transconductance gm_4 and gm_5 is a first order structure with negative resistance load which improves the Output impedance, the passive resistance in [6] is replaced by an active resistance thus improving the impedance by keeping the attenuation low. Another advantage of using the active resistance is, during design the gm can be varied for the desired resistance without affecting the gain and cut-off frequency. The third stage is a lossless fully differential Integrator which will introduce a further 20dB/decade roll-off.

The Transfer function of the second order Biquad Structure is given by

$$H_2(s) = \frac{K\omega_b^2}{s^2 + \omega_b/Qs + \omega_b^2} \tag{2}$$

Where,

$$K = \frac{gm_1}{gm_3} \tag{3}$$

$$\omega_o = \frac{\sqrt{gm_3 gm_2}}{C_1 C_2} \tag{4}$$

$$Q = \sqrt{\frac{C_1}{C_2} \times gm_3 gm_2} \tag{5}$$

The transfer function of the first order section with negative resistance is given by

$$H_1(s) = \frac{gm_4 \times 1/gm_5}{1 + sC_3/gm_5} \tag{6}$$

The Transfer function of lossless Integrator is given by

$$H_o(s) = \frac{gm_6}{sC_4} \tag{7}$$

Transconductance gm_6 is varied to compensate for the attenuation caused by the previous stages. One of the Major advantages of using a gm-C filter is it has a wider bandwidth [8].

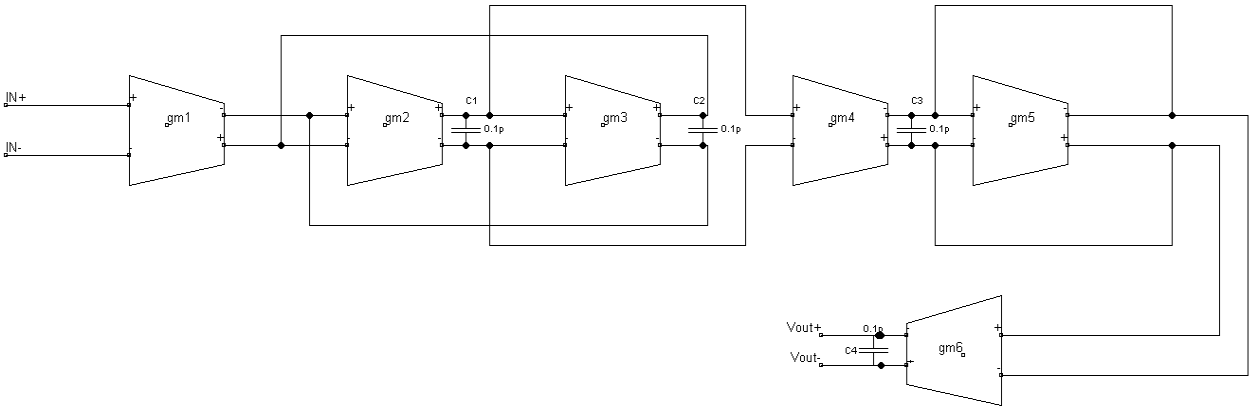

Figure 4. Fourth Order Elliptic Filter Topology

Gm-C filter has excellent gain-bandwidth properties and cascading these structures is quite simple and easy. In this design the passive elements are replaced by their active counterpart, which will give lower sensitivity due to component variations [9].

IV. Simulation Results

Mentor Graphics tool is used to design the filter in 130nm CMOS technology. Making use of the advantage of fully differential amplifier, the short channel effects and the noise is reduced.

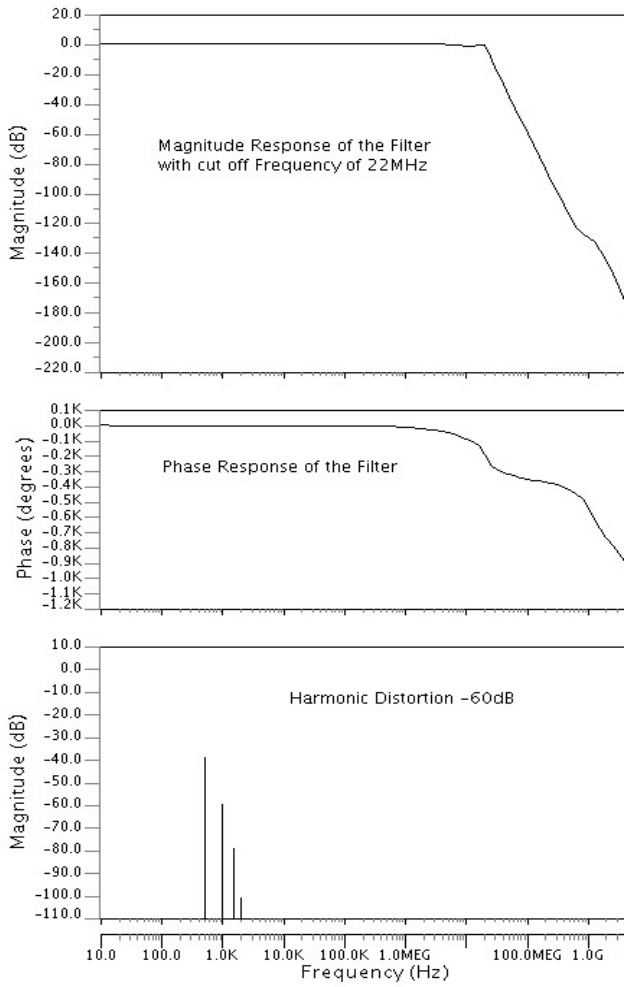

Figure 5. Simulation Output of Magnitude, Phase response & Harmonic distortion

Furthermore, fully differential amplifier design can also suppress even order harmonics and increase output voltage swing [10] – [12], which is most appropriate for the 4th order filter design. Thus as shown in Figure 5 the magnitude response of the filter having a roll off of 80db/decade is achieved well with the use of the proposed gm-C topology.

A larger cut-off frequency of 22 MHz with high linearity is obtained by appropriately designing the OTA. Phase response in figure 5 shows that the filter is linear throughout the wider cut off frequency of 22MHz. Even if the cut-off frequency is increased by altering the value of the capacitance in the design, it is found that the filter's response is still linear up to GHz range. The supply Voltage of 1.4V is used and the power consumption is reduced to 1.4mW. The Filter design has a Total Harmonic Distortion of -60dB for an input voltage of 150mV. The Transconductance of the OTA is adjusted to get a fully differential Output Voltage swing of 600mV Peak to Peak. The complete simulation results are listed in table1 below.

V. Conclusion

The Low power 4th order gm-C filter has been designed to overcome limitations such as high Power Consumption, non linearity, and low output Voltage swing. The fully differential OTA in 130nm CMOS technology has also been designed in 1.4V supply voltage with CMFB. The simulation result shows a roll-off of 80dB/decade and high linearity of the filter for a wider frequency bandwidth. The Total Harmonic Distortion observed for a differential input voltage of 150mV peak to peak is -60dB, which is less than 1%.

TABLE 1 SIMULATION RESULTS

Technology	130 nm CMOS
Supply Voltage	1.4 Volts
Filter type	4th Order Elliptic
Power Consumption	1.4mW
THD(@150mV)	-60dB
Output voltage swing (fully differential)	600mV (P-P)
Current Consumption (static)	0.7mA
No. of gm –C unit	6
Total On chip Capacitance	0.4pf
Cut off Frequency of the Filter	22MHz
Total no. of Transistors per OTA	20
Area of the Filter in Layout	0.5mm^2

TABLE 2 COMPARISONS OF DIFFERENT FILTER DESIGNS

References	Filter Parameters					
	Technology	**Supply Voltage**	**Filter Type**	**Power Consumption**	**THD@150mV input**	**Output Voltage Swing (fully diff.)**
[4]	65nm CMOS	1.8V	5ht Order Bessel	21.6mW	-40dB	400mV
[5]	180nm TSMC CMOS	1.8V	5^{th} Order FLF	67mW	-40dB	400mV
[6]	120nm CMOS	1.5mV	3^{rd} Order	14.25mW	-49dB	400mV
[10]	90nm CMOS	0.9V	5^{th} Order Elliptic	1.5mW	-66dB	300mV
[11]	180nm CMOS	1.8V	2^{nd} Order	8.1mW	-40dB	450mV
[12]	0.35um CMOS	1.0V	1^{st} Order	005nW	-40.3dB	
This Work	130 nm IBM CMOS	1.4 Volts	4^{th} Order Elliptic	1.4mW	-60dB	600mV

The Parameters of various filter designs are compared in Table 2 and it is evident that this work has contributed an overall best filter design with a very good Output voltage swing and minimum Power consumption.

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