Cubeth EPS design review

Semester project

Prepared by:

PABLO KLEMM

Checked by:

Approved by:

Space Center EPFL
Lausanne
Switzerland

June 19, 2014

Record of Revisions

Issue	Revision	Date	Modifications	Created/modified by
1	0	06.06.2014	First draft	Pablo Klemm
1	1	15.06.2014		Your Name

Contents

List of Tables

List of Figures

1 Requirement

Here will be presented the requirements directly related to the EPS and this project, the whole requirement list can be found in appendix A.

- **MR.1** The EPS shall provide enough power for nominal operations in sunlight as well as during eclipses.
- **MR.2** The EPS shall operate between -30°C and +40 °C
- **MR.4** The power supply shall be regulated at +3.3V ± 0.3V.
- **MR.5** The EPS shall be able to deliver currents up to 2A while irradiated by the Sun.

Additional requirements where added exclusively for this project:

- The batteries should charge if the bus voltage > 3.3V
- The batteries should discharge if the bus voltage < 3.3 V
- Power excess in case of high insolation should get dissipated in dedicated resistors

2 Acronyms

ABF Add Before Flight.

ADCS Attitude Determination and Control System.

ADS Antenna Deployment System.

CDMS Command and Data Management System.

COM Communication.

EPS Electrical Power Subsystem.

MB Motherboard.

PMB Power Management Board.

P-POD Poly Picosatellite Orbital Deployer.

RBF Remove before flight.

Rf Radio Frequency.

SC Solar Cell.

3 Introduction

The CubETH mission is the second CubeSat picosatellite mission developed by EPFL and ETHZ. Satellite science goal is Precise Orbit Determination and attitude determination based on Global Navigation Satellite System (GNSS) technologies. ETHZ is in charge of the science mission payload. The hardware and software design of the other subsystems is run by EPFL.
The goal of this project originally was to to test the Electrical Power Subsystem (EPS) board, however due to the numerous errors found in the schematics and the mounting mistakes, the project has been reoriented towards debugging the card from all these flaws. The problems that appeared will be presented followed by their solution. In this project the PCB that has been used is the one that has been manufactured according to Quentin Cabrol's report [1] and diagrams.

3.1 Electrical Power Subsystem (EPS) role

The Electrical Power Subsystem (EPS) is an essential block of a satellite. It gathers energy from the sun and earth albedo through solar panels and provides the energy supply to all the other satellite subsystems. Depending on the availability of the energy it can turn on or off certain modules. If the EPS was to fail, the satellite would die. Therefore redundancy and reliability in this module are critical. EPS is also in charge of controlling the charge/discharge cycle of the embedded batteries to ensure an uninterrupted functioning of the satellite. The previous version of the EPS ensured overcurrent protection, but for space availability concerns on the PCB this latch-up protection is now embedded locally on each other subsystem. However the EPS still ensures that the batteries never get overcharged and that the supply voltages remain between acceptable bounds in any cases thanks to a system of power management implemented with dissipation resistors that dissipate the electrical current that is not needed by the system and could damage it. The Direct Energy Transfer (DET) architecture has been picked up preferentially to the alternative Maximum Peak Power Tracking (MPPT) for several reasons: it is simpler, allows to have redundancy without the need to implement backup analogic circuitry for the peak tracking algorithm and do not need as many power consuming voltage regulators as the later. EPS controls as well the temperature of the solar panels, the current they provide, the voltage of the power bus, the charge and discharge currents of one of the batteries and their temperature. All these data allow the microcontroller to take real time decisions in whether a module should be turned ON or OFF depending on the current state of the available power and satellite temperatures.

In brief, the EPS missions are:

- Power gathering and storage,
- Power distribution,
- Power and temperature monitoring,
- Dissipation of power for battery protection.

As an additional role, the EPS as its own microcontroller embedded that receives and treat housekeeping data (HK) from the other modules.

The basic functioning of the EPS MB is presented in this following flowchart.

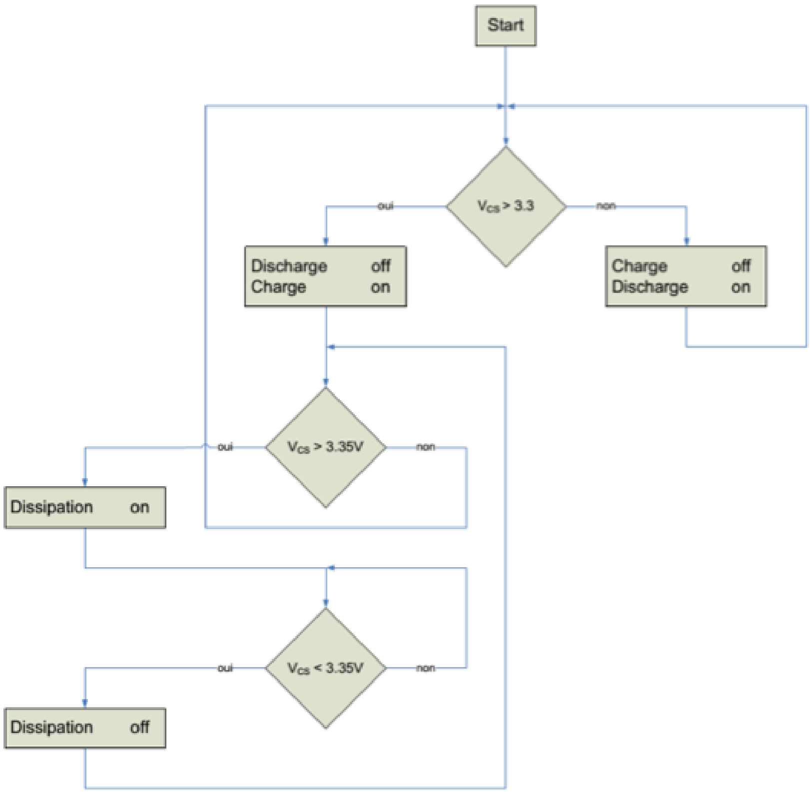


Figure 1: EPS MB functioning flowchart

3.2 Project Goal

As it has been briefly said in the introduction, the project has been redefined from testing the card to debugging it and getting it to work for future tests. Three main functions of the EPS had to be checked and debugged, these are the dissipation, the charge and the discharge of the battery. Details about these functions will be provided further in this report. The mistakes that had to be detected where can be separated in two groups, the first one is mounting mistakes that occur due to careless mistakes or if the schematic of the layout of the pcb isn't clear, e.g : Names of components overlapping each other. The second group is due to mistakes that can be found in the electrical schematics. The mistakes from the first group need a careful review of the components mounted on the PCB, the values and the orientation of each component need to be thoroughly checked. The mistakes of the second group can be found comparing the schemes of Cubeth with the schemes of SwissCube, since the systems from the first one are largely inspired from the second one. Finally another goal of this project is to provide a comprehensive document (almost like an user's manual) about the functioning of the EPS MB (mother board) in order to allow following students to work on the EPS test it and understand it, without having to struggle with large quantities of previous reports.

The main tasks are summarized in this list :

- Litterature Review
- Swisscube design review
- Mounting of components review
- Debug of the card
- Provide a corrected electronic diagram
- Basic test to check if the card works
- Write an user's manual for the next student

4 Power budget

The power consumption is taken as the sum of the powers used by each of the subsystems of the CubETH. The main power consuming modules are the ADCS and the COM board that transmits information over RF signals.Table 1 sums up the consumption of the different modules in mW. In reality all the modules are not constantly turned on and most of the time the satellite consumes less than the maximum power. Typically the COM board transmission (Tx) is shut down most of the time and only a Morse beacon is transmitted from the satellite. The COM board is enabled when it receives an incoming transmission from the ground segment.

Subsytem	Power (mW)
EPS	150
Payload acquisition	200
Payload measurements	300
CDMS mean	100
Beacon	55
ADCS Magnetometer	20
ADCS Gyroscope	20
ADSCS Sun Sensors	100
ADCS Magnetotorquers	225
COM Rx	90
COM Tx	3000

Table 1: Power budget

5 Mounting mistakes

5.1 OPAs mounted backwards

Problem symptoms : When a voltage is applied between the VCC and the GND, the power source gets stuck at 0.7 V and the current rises up the limit imposed by the user on the current limitator.

Source of the problem : The OPAs 2333 U8 and U9 (so it concerns 4 components because of redundancy) had been soldered backwards,i.e the pin 1 was soldered on pad 8 and vice-versa.

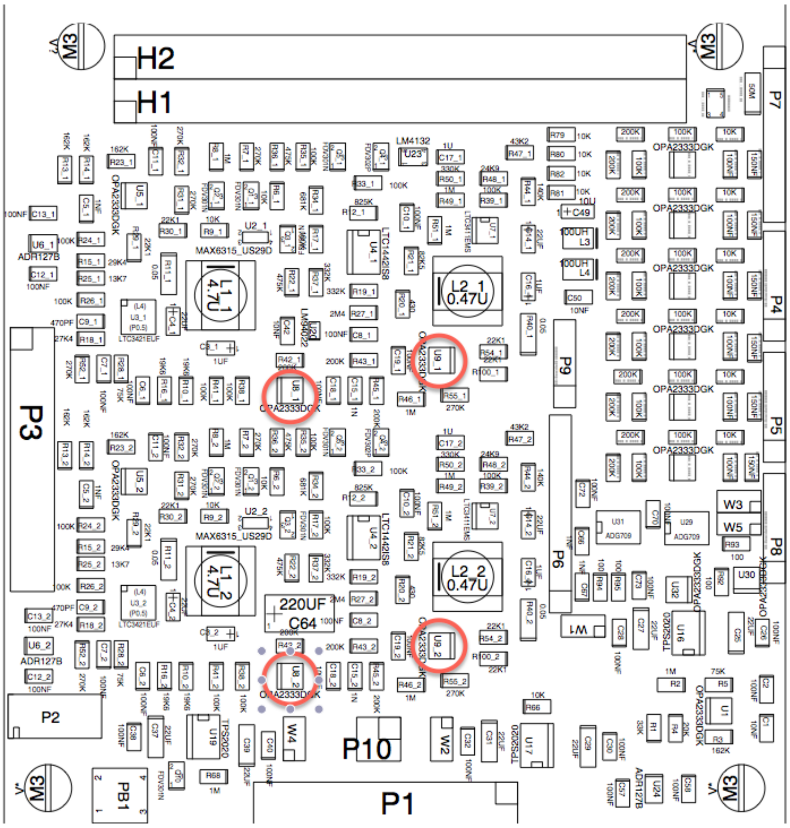


Figure 2: OPAs that were mounted backwards

Fix: Unsolder them and resolder them in the correct orientation.

Proposition: Serigraph the positions of the pins "1" for active components for future prototypes in order to avoid loosing time due to mounting problems, that are not easy to detect due to the large amount of components. For the card that will be embarked if serigraphy is not possible, extra care is needed during mounting.

5.2 Wrong inductances mounted in the discharge circuit

Problem symptoms: None because problem was detected before trying discharge. According to the datasheet a wrong inductor could affect the discharge current.

Source of the problem : 4.7 μH inductors had been used instead of 0.47 μH. Component is named "L2" on the diagrams.

Fix: Replaced them with correct inductances.

5.3 Misplaced components due to unclear diagram

Problem symptoms: None, was detected by after a visual inspection.

Source of the problem : Due to an unclear electrical diagram a resistor and a capacitor had been misplaced as it can be seen on fig. 3. C85 was at the place of R108 and vice versa.

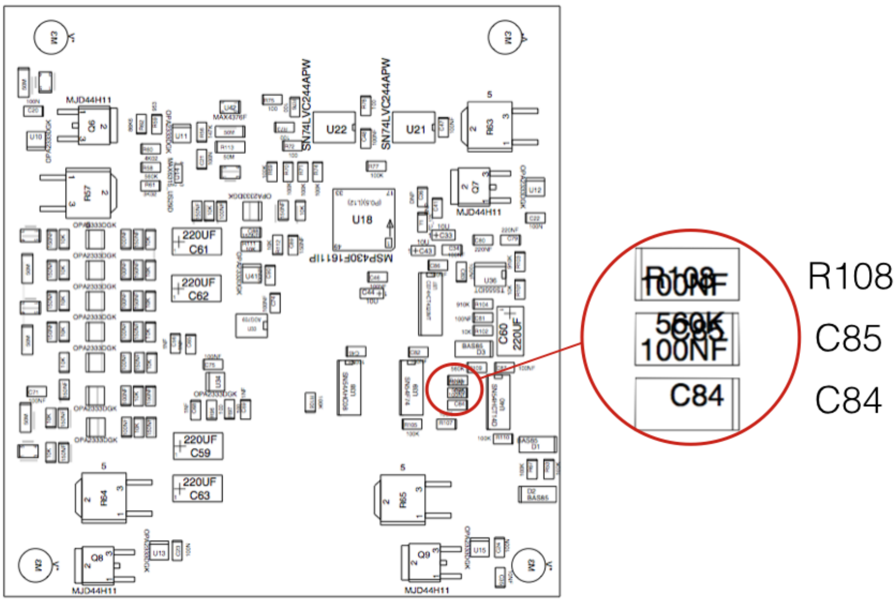


Figure 3: PCB of the bottom with the positions of the components clearly presented

Fix : Resoldered properly the components and specified the correct order as seen on fig. 3.

6 Electrical diagram mistakes

6.1 VCC disconnected from ABF

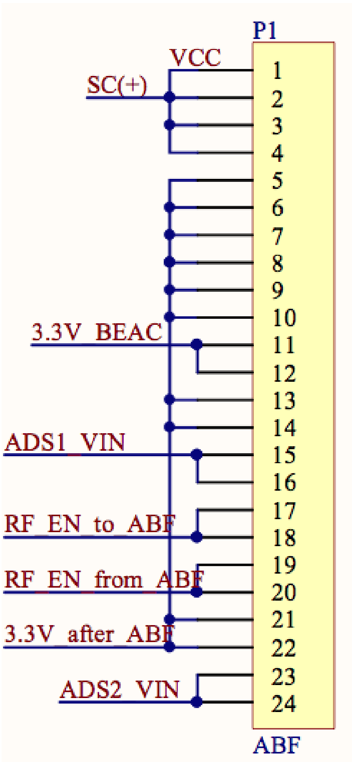


Figure 4: ABF pins

Problem symptoms : VCC is at 0 V even though SC+ was set at 3.3 V through a power source.

Source of the problem : As it can be seen on fig. 4, SC+ and VCC should be connected together through the ABF, however a mistake in Altium Designer was made, and the VCC line was not connected to the SC+ line.

Fix: The plans have been corrected on Altium. A cable connecting the too of them has been soldered on the card.

6.2 Grounded reference

Problem symptoms : The charge command (CHG CMD) was always on a high level and dissipation was always active.

Source of the problem : As it can be seen on fig. 5, the Vref line is connected to the GND, for this reason the comparators in the "Dissipation box" and the "Battery Control" box where comparing the voltage of the bus with the GND, so naturally the charge was always activated as well as the dissipation. Also the routing was made in such a way that R60 was grounded instead of being connected to Vref (U24 pin 4), and the pins 1 an 5 of U1 where at GND instead of being on the Vref line.

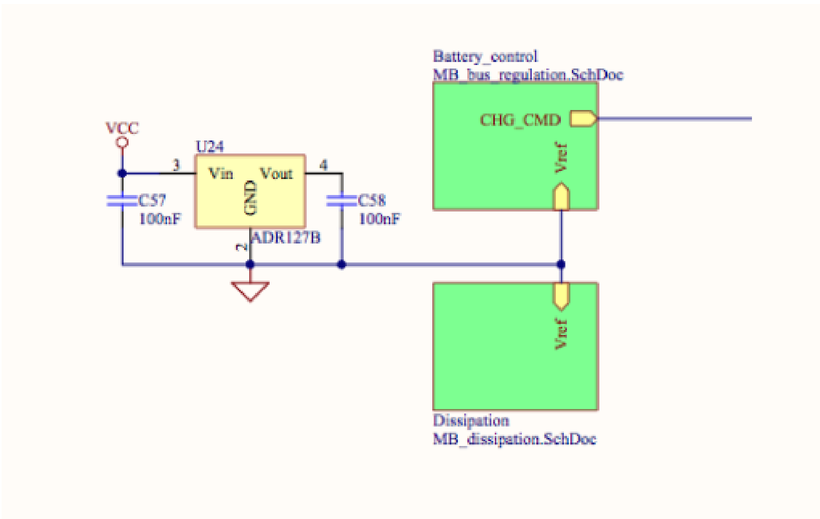


Figure 5: The output of the ADR 127 B has been mistakenly connected to the ground

Fix: The plans have been on Altium as it can be seen in fig. 6, and the PCB has been corrected physically as seen on fig. 7

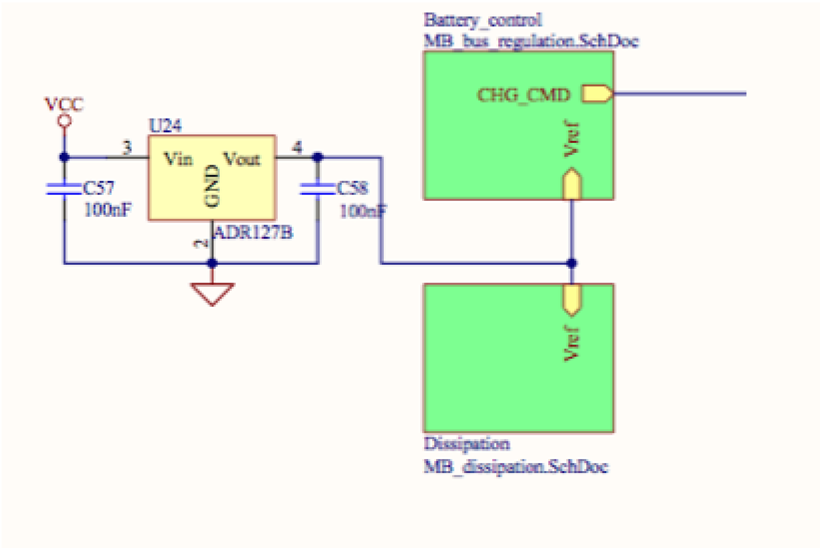


Figure 6: The corrected schematic

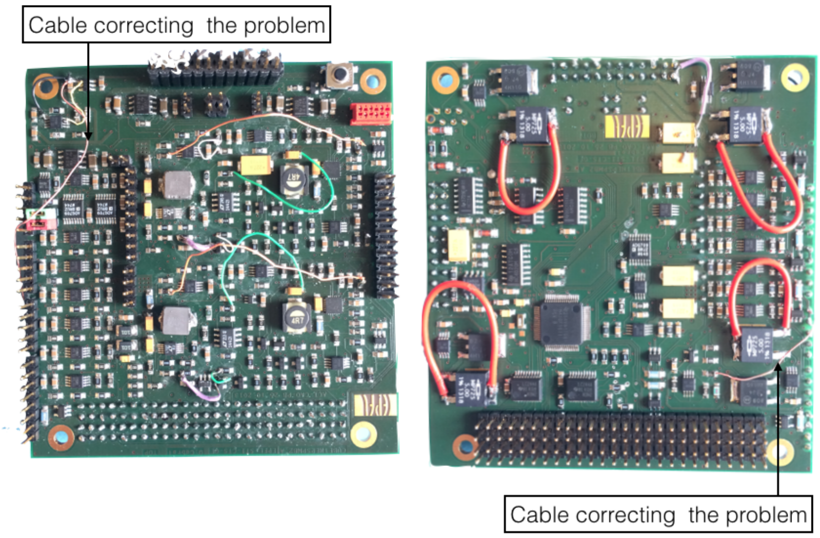


Figure 7: The thin pink cable corrects the aforementioned problem

6.3 Ground missing in the charge circuit

Problem symptoms : The charge was never activated due to the shutdown always activated (active low so level was at 0).

Source of the problem : As seen on fig. 8, at the node of R19,C8 and R27 there should be a ground.

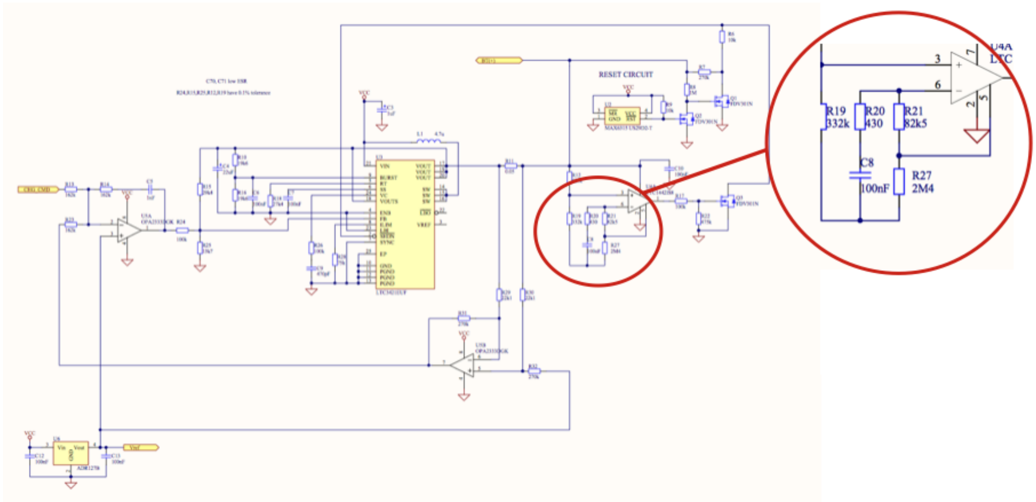


Figure 8: The charge diagram with the missing ground

Fix : Added the ground on the diagram and cabled it on the PCB.

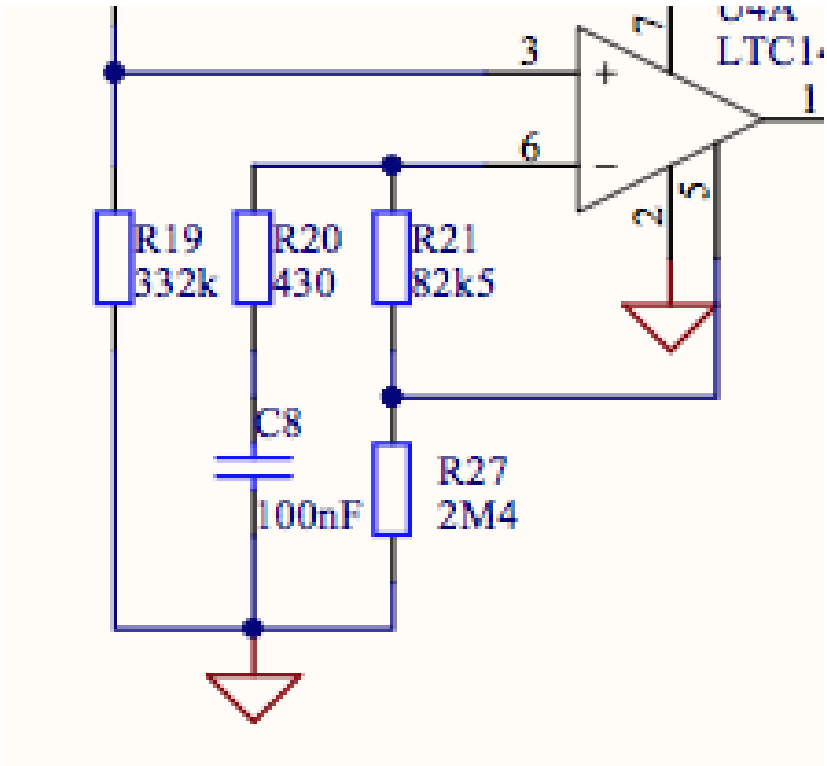


Figure 9: The corrected charge diagram with the ground added

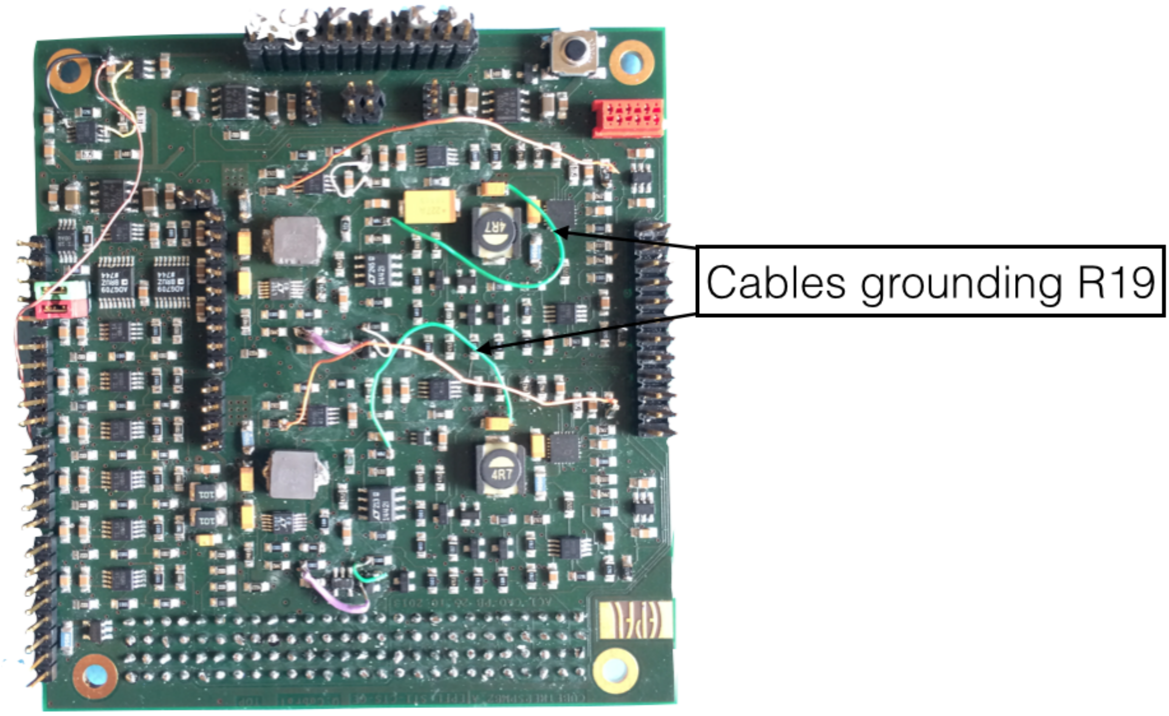


Figure 10: The cables added in order to ground the node of R19,C8 and R27

6.4 The importance of drawing properly oriented transistors

Problem symptoms : The discharge never got activated even when the bus voltage was under 3.3 V and the battery was fully charged.

Source of the problem : In the electrical diagram of the discharge, transistor Q4 had been inverted, the drain was at BT(+) whereas it should have been the source as it can be seen on fig. 12.

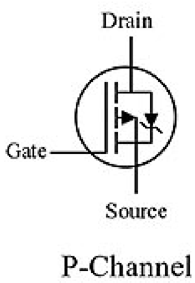


Figure 11: A P channel MOSFET transistor

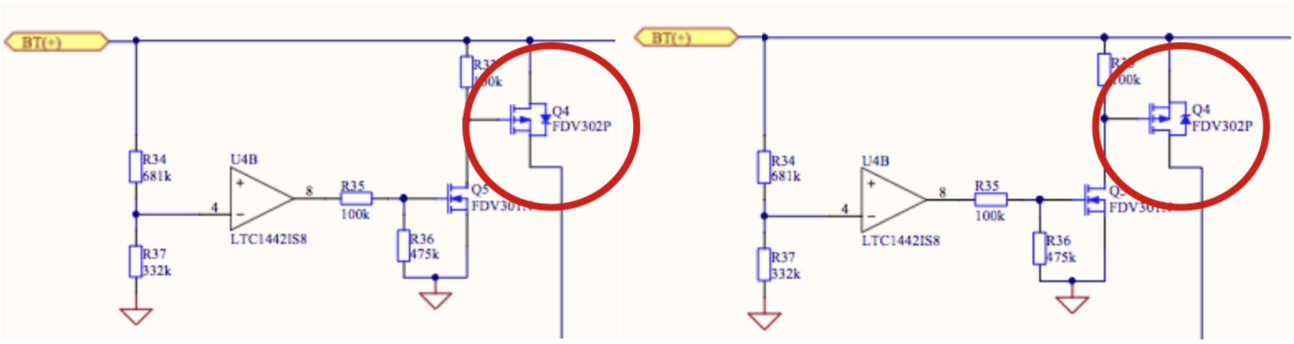


Figure 12: On the left the erroneously placed transistor, on the right the corrected diagram

Fix : Swisscube diagrams where checked and the transistor has been replaced correctly on the altium plans of Cubeth and a bypass has been made on the PCB.

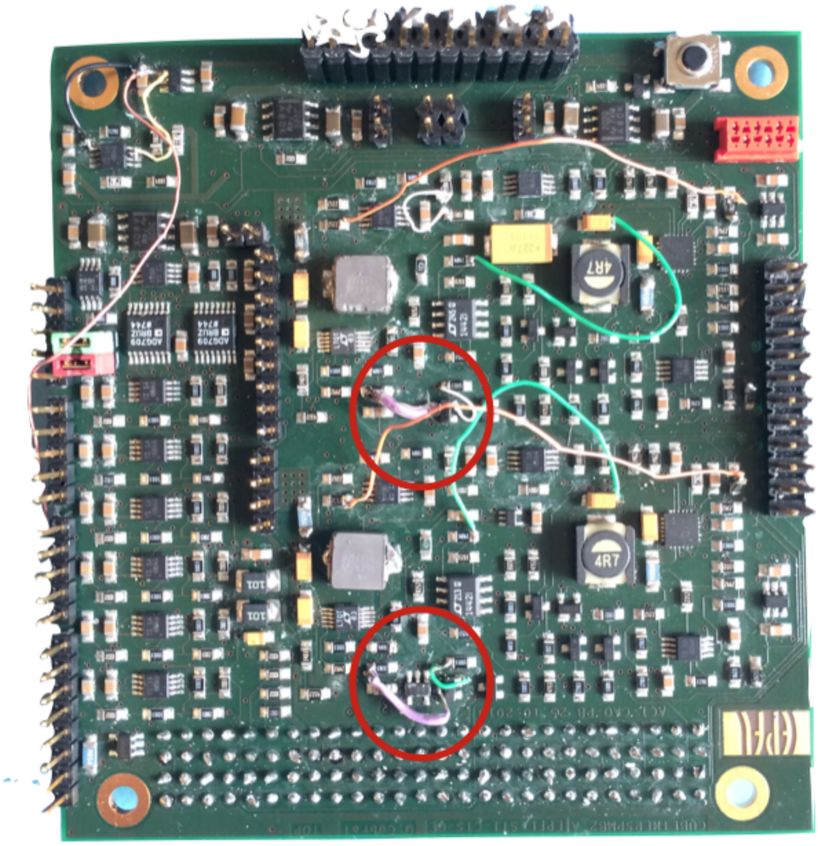


Figure 13: In the red circles, the bypass that has been made in order to fix the problem

6.5 Dissipation resistors erroneously routed

Dissipation resistors are R57,R63,R64 and R65

Problem symptoms: Incoherency voltages measured at the pins of the resistors, impossibility to verify if they are dissipating or not.

Source of the problem : Even though the electrical schematics where correct, the routing has been done incorrectly. Pin 2 seen on fig. 14 is the heat sink, it is clearly mentioned in the datasheet that "Resistor element is electrically isolated from the metal heat sink tab". This means that if we look at fig. 15, we should have for example pin 1 on the emitter of Q7 and pin 3 to the ground. However it was found on the PCB that pin 3 hadn't been grounded, only pin 2 (which is grounded for heat dissipation purposes).

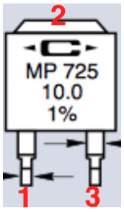


Figure 14: MP 725-5 dissipation resistors

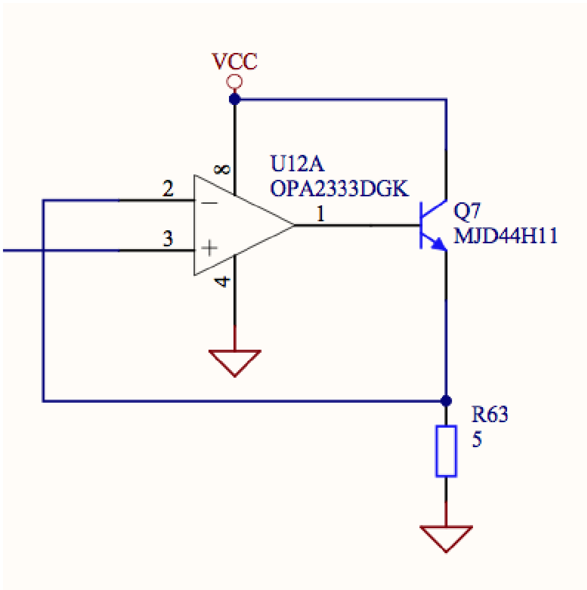


Figure 15: One of the four dissipation command circuits

Fix: Pin 3 was grounded by adding a cable.

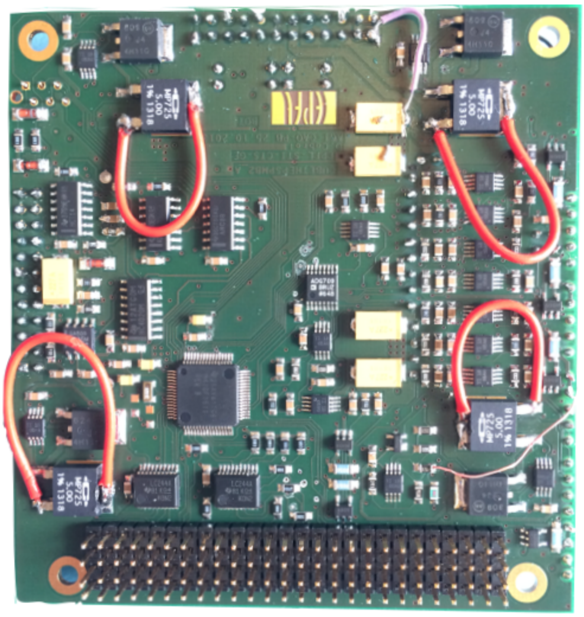


Figure 16: The red cables ground pin 3 of the resistors (ground is under the heat sink)

Proposition: Clarify this point with the person that does the routing and check it before PCB is manufactured.

6.6 Wrongly placed reference

Problem symptoms : Charge and discharge were activated at the same time.

Source of the problem : As we can see on fig. 17 whoch is taken from the discharge diagram, Vref was arriving over R54.

Fix : Looking at Swisscube's design the diagram has been corrected (Vref arrives under R54), as well as the PCB.

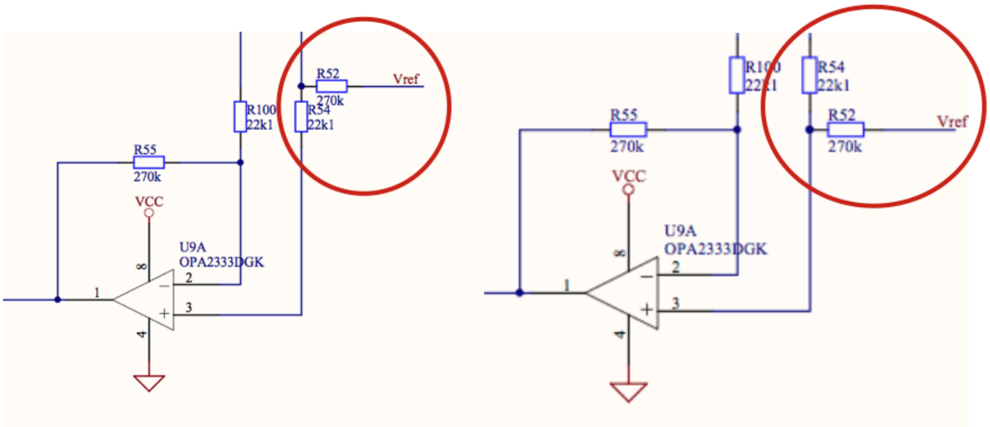


Figure 17: On the left the erroneously placed reference, on the right the corrected diagram

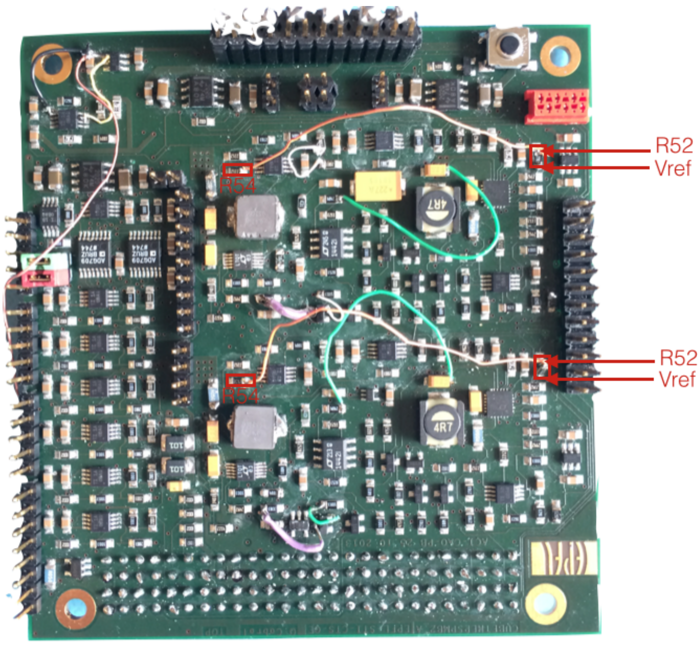


Figure 18: The problem has been fixed by disconnecting the pin of R52 that was on the pad connected to R54 and a bypass with the orange wire

7 EPS user's manual

7.1 The power source

Cubeth will be equipped with 5 faces containing each two solar panels in series. Each panel has theoretical output current of 520 mA (at 0° incidence), therefore for two pannels in series, the max current is 520 mA. In consequence we will **set the current limitator of our source at 520 mA**. The circuit can tolerate higher currents but the user **shouldn't go over 1 A**.

7.2 Cabling

ABF

The Add Before Flight (ABF) connector has been plugged on connector P1 in order to power all the subsytems of the cubesat as it is shown here in fig . 19. The plug can be split in 5 separate parts permitting customized activation during prototyping and tests. The first part is the main plug activating the power bus of the satellite, the others permit to activate respectively the beacon, the first ADS, the RF power on the communication board, and the second ADS.

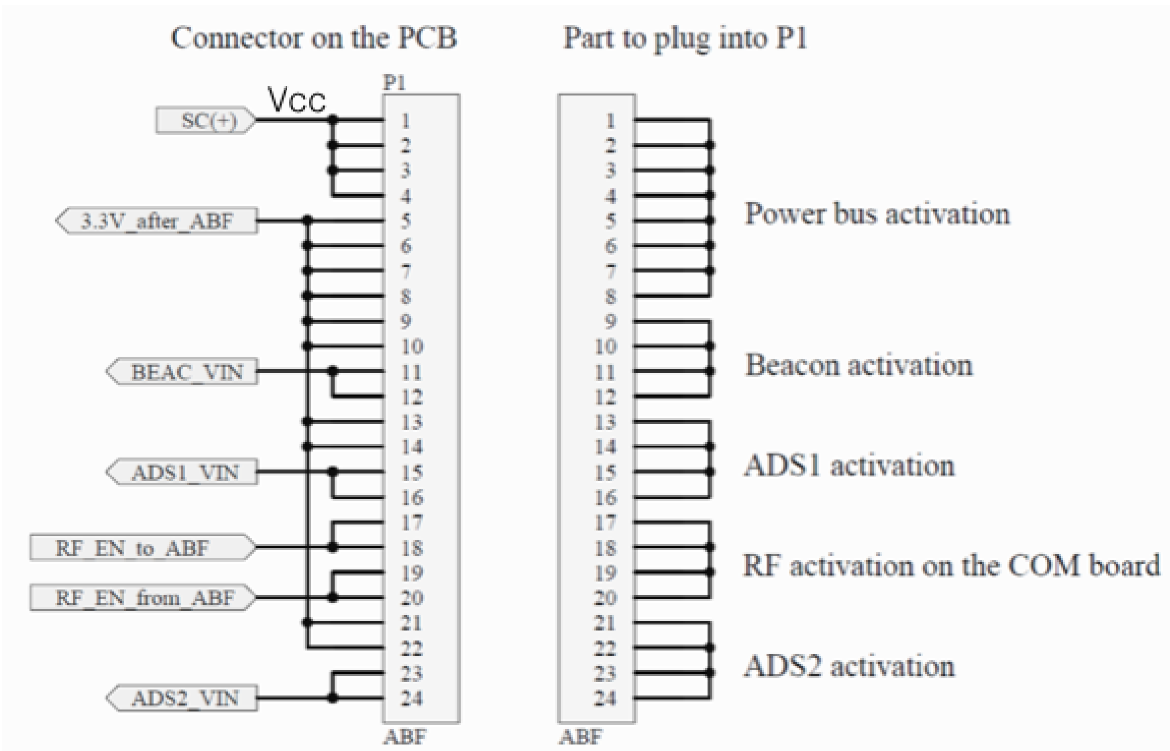


Figure 19: The P1 connector on the left, on the right the part to plug in P1

Kill switches

In order to connect the SC (-) to the ground (and there for close the circuit to get the EPS to work), jumpers should be added over W3 and W5. Their position is shown on fig 20.

Other jumpers to eventually add

Should the user want to use the PMB part of the EPS, a jumper will have to be added on W1 in order to connect +3.3 V EPS. If the ADS1 and ADS2 want to be used, jumpers over W2 and W4 will have to be added in to connect +3.3 V ADS1 and/or ADS2.

VCC

In order to power the EPS by simulating our solar panels, we will connect the (+) output of our power source to the pins labelled "VCC" on the diagram, this can be done at pins P3-9 and/or P3-10 , or directly at one of the pins of the ABF if it's connected. The (-) output of the source is connected to the GND pins, which are pins P3-21 to P-24 for example.

Batteries

As it can be seen on fig. 20, the EPS presents a redundancy, the upper part is powered by battery 1 (or charges it), the battery is connected between pins BT1(+) i.e P3-3 or P3-4 and the GND. For the lower part the second battery is connected between BT2(+) i.e P3-5 or P3-6 and the GND.

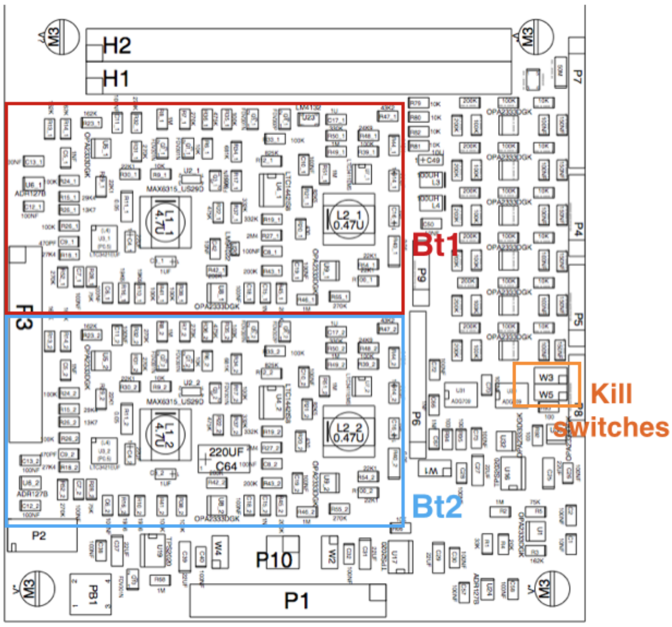


Figure 20: The EPS redundancy shown, the upper part powered by battery 1 and the lower part by battery 2. Kill switches to be jumped are also shown

Note : In Quentin Cabrol's PCB the GND was not kept properly at 0 V when a voltage higher than 3 V was applied, in order to pull the GND closer to 0V, the user can connect more than one pin to the (-) of the power source, for examples pins P3 21 to 24. Same advice goes for the VCC, more than one pin can be connected (on the service pins P3 or on the ABF for example.//

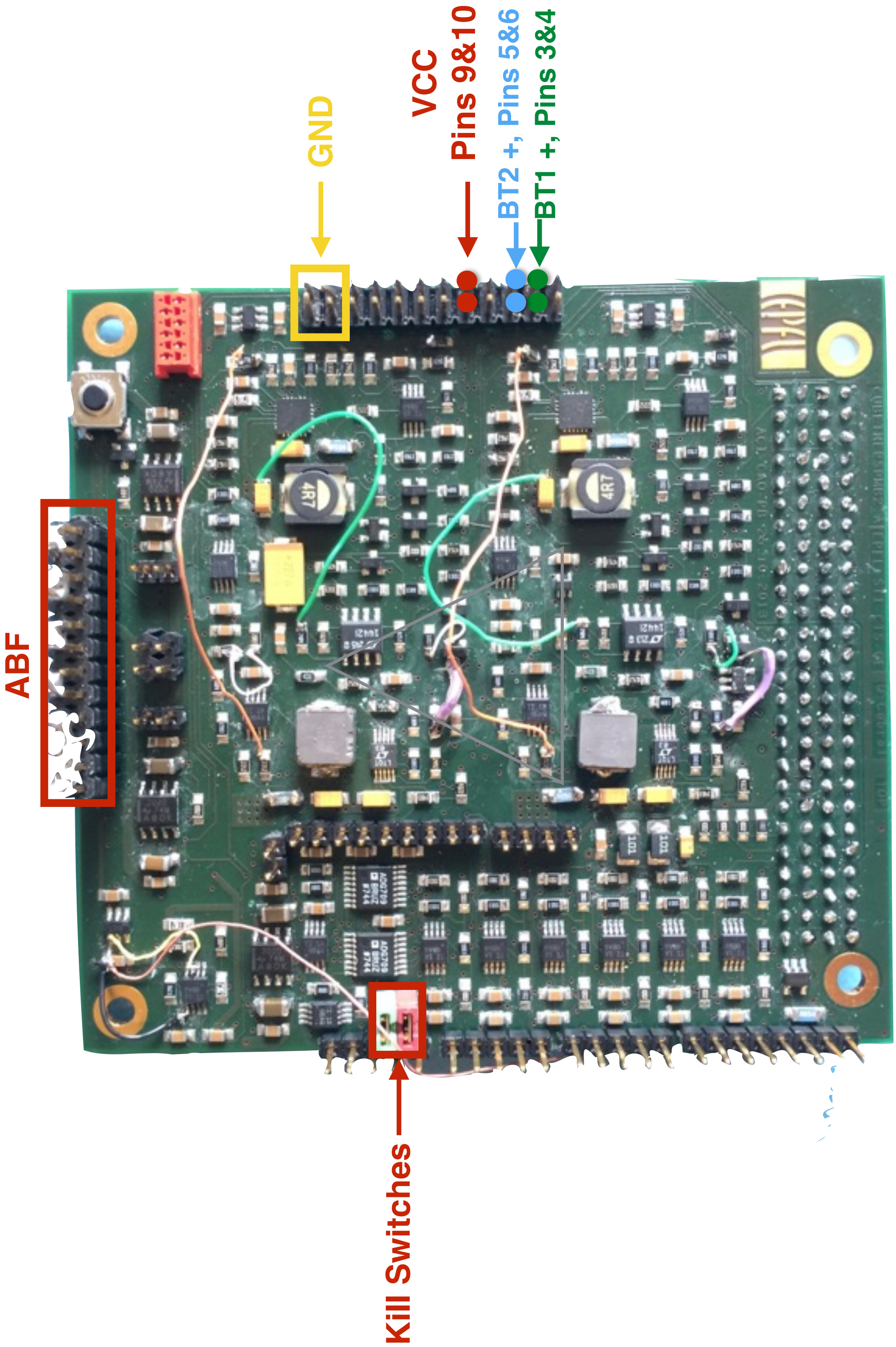


Figure 21: Useful pins to get the EPS to wroks

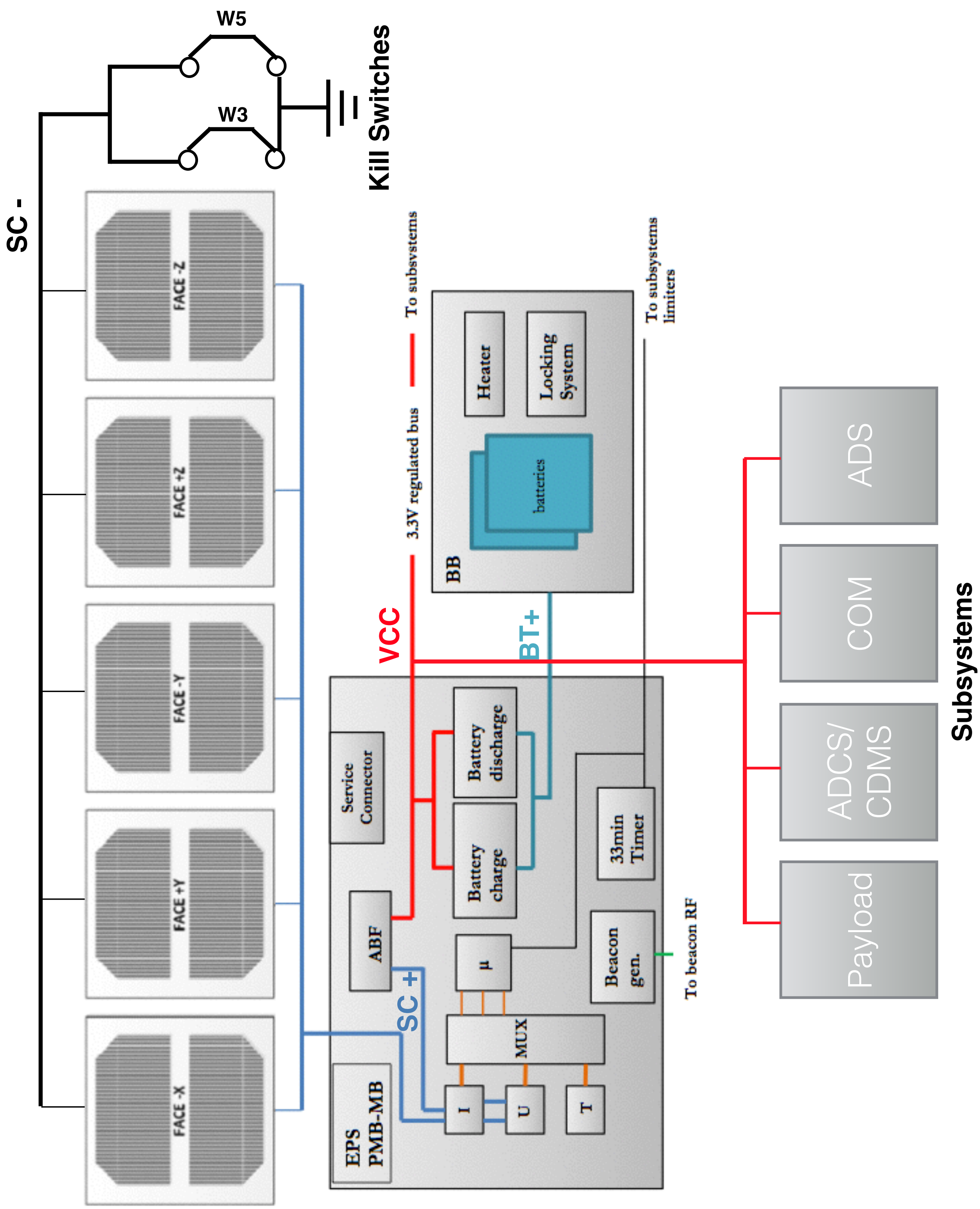


Figure 22: Architecture of the EPS

7.3 Getting the EPS to work

If the batteries are connected, once turning on the power source, it should be already at 3.3 V since the batteries are being discharged in order to maintain this voltage. Also it is useful to connect an ampere meter to the batteries to check the discharging current (negative) or the charging current (positive). If we try to raise the voltage with our power source over 3.3 V, the charge will get activated and the power source will quickly reach our current limit. The reader will find in appendix G the diagrams annottated with the voltages obtained at different inputs and outputs of the components for charge and discharge.

7.4 Basic tests

Should the reader want to test a single function of the EPS MB , the following lines explain the procedures.

Charge
It suffices to plug the battery as explained previously and monitor with an ampere meter if the current flows into the battery for voltages over 3.3 V.
Discharge
It suffices to plug the battery as explained previously and monitor with an ampere meter if the current flows out of the battery for voltages under 3.3 V. The bus voltage should be kept at 3.3 V during discharge.

Dissipation
To test dissipation, one can remove the batteries and exclusively monitor the voltage of the dissipation resistors (R57, R63, R64, R65) to see if dissipation is activated for voltages over 3.3V. Once dissipation is active the bus should be kept down at 3.3 V and the reader will see the current rise on the power source display which is consumed by the resistors).

8 Conclusions

The main goal of this project has been reached, this was to debug the EPS PCB from the different mistakes that were made and test charge/discharge and dissipation at standard temperature and pressure conditions.
Debugging this card has been a tough challenge since mistake sources were multiple. With so many components on the PCB, it is difficult to see where the problems are. Also one wouldn't immediately think about mounting mistakes (wrong component, wrong placement) ,but for such projects where everything is done by hand, I have learned that if I am confronted to such a challenge again, it is important to verify **each** component and it's placement, to avoid bad surprises. The process of finding all the errors has been long, but thanks to this project I have learned how to tackle such problems, and another positive point is that the method I have acquired could be applied to any engineering challenge.

Also during this project, running simulations of the circuit helped me a lot in order to find where the problems where. It would be a good thing in the projects to have simulations run before delivering the diagrams, just to be sure no mistakes where made.

Another lesson I learned is that it is very easy do a small mistake when designing the electrical diagrams (as it has been seen in the report), for this reason it is important upon drawing such diagrams, to have a third party re read and check the diagrams, even if it takes some time explaining the task to this external person, it could save a lot of time for the future.

9 Future Work

Now that the card has been debugged a thorough testing part needs to be conducted with the new PCB. The main functions which are charge, discharge and dissipation should be tested as explained during this report. Extensive testing can be done following the protocols established by Nicolas Steiner for Swisscube in his report [5], where it is explained which tests to run and at which temperature and pressure conditions .Then other functions should be tested such as the timer that should last 33 mins and the functioning of all the PMB part,which has been untouched in this project. The details about the functions can be found in Kevin Boca's [2] and Quentin cabrol's [1] reports . Also the power budget should be reviewed and updated once all the subsystems are available, tests by simulating the various subsystem consumptions or even by plugging them directly to the EPS should be run should the hardware be available.

References

[1] Quentin Cabrol, *Electrical Power Subsystem (EPS)*, Semester Minor Project, Swiss Space Center EPFL, 2013

[2] Kevin Boca, *Electrical Power Subsystem (EPS) for CubETH nanosatellite*, Master Thesis, Swiss Space Center EPFL, 2013

[3] Belloni Federico, Boca Kevin, Kronig Luzius, Masson Louis, Rincon Gil Edgar, Rossi Stefano, Olchevski Ivan, Ivanov Anton *CubETH Bus Design Report* Swiss Space Center EPFL, 2013

[4] Fabien Jordan, *Electrical Power System (EPS)*, Report of Diploma, Institut d'Automatisation Industrielle, HEIG-VD, 2006

[5] Nicolas Steiner, *EPS subsystem: Electrical qualification tests*, Institut d'Automatisation Industrielle, HEIG-VD, 2007

[6] *Satellite Power System* , US Department of Energy and the National Aeronautics and Space Administration, 1978

A Requirements

The requirements have been taken from Kevin Boca's thesis [2], as they haven't changed since then. Starting from the cubesat design specifications which lists all the characteristics and safety future a satellite shall have in order to be classified as a cubesat and be allowed to be placed on a launcher. Note that this document is valid for 1U satellites as well as 3U ones. The Electrical Requirement (ER) of the cubsat standard are listed here below.

ER.1 No electronics shall be active during launch to prevent any electrical or RF interference with the launch vehicle and primary payloads. CubeSats with batteries shall be fully deactivated during launch or launch with discharged batteries.

ER.2 The CubeSat shall include at least one deployment switch on the designated rail standoff (shown in Figure 3) to completely turn off satellite power once actuated. In the actuated state, the deployment switch shall be centered at or below the level of the standoff.

ER.2.1 All systems shall be turned off, including real time clocks.

ER.3 To allow for CubeSat diagnostics and battery charging after the CubeSats have been in- tegrated into the P-POD all CubeSat umbilical connectors shall be within the designated Access Port locations, green shaded areas shown in Figure 3.

ER.3.1 Triple CubeSats shall use the designated Access Port locations.

ER.3.2 Note: CubeSat deployment switch shall be depressed while inside the P-POD. All diagnostics and battery charging shall be done while the deployment switch is de- pressed.

ER.4 The CubeSat shall include a Remove Before Flight (RBF) pin or launch with batteries fully discharged. The RBF pin shall be removed from the CubeSat after integration into the P-POD.

ER.4.1 The RBF pin shall be accessible from the Access Port location, green shaded areas shown in 23.

ER.4.1.1 Triple CubeSats shall locate their RBF pin in one of the 3 designated Access Port locations .

ER.4.2 The RBF pin shall cut all power to the satellite once it is inserted into the satellite.

ER.4.3 The RBF pin shall not protrude more than 6.5 mm from the rails when it is fully inserted into the satellite.

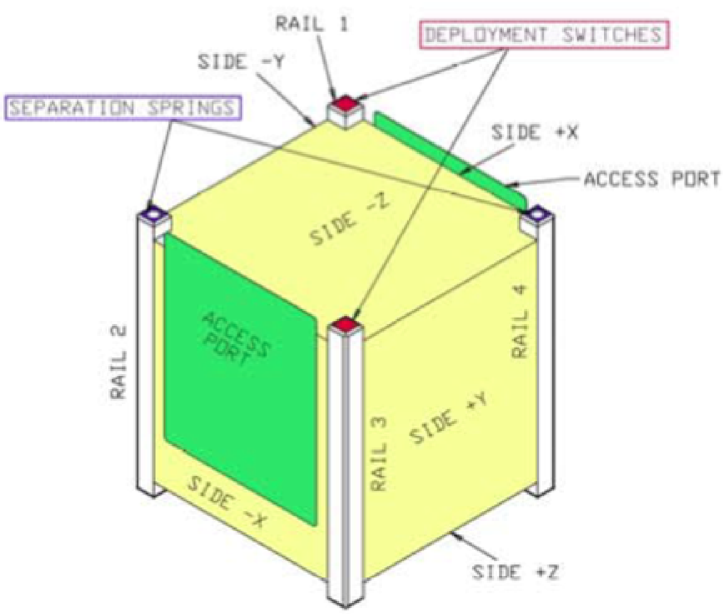


Figure 23: Drawing of the satellite specifying the interfaces such as switches, springs and area where the service connector shall be located

There are also some Operational Requirement (**OR**) defined in the cubsat design specification which could affect the design of the EPS. These selected required conditions are listed here below.

OR.1 CubeSats with batteries shall have the capability to receive a transmitter shutdown com- mand, as per Federal Communications Commission (FCC) regulation.

OR.2 All deployables such as booms, antennas, and solar panels shall wait to deploy a minimum of 30 minutes after the CubeSat's deployment switch(es) are activated from P-POD ejection.

OR.3 RF transmitters greater than 1 mW shall wait to transmit a minimum of 30 minutes after the CubeSat's deployment switch(es) are activated from P-POD ejection.

The last group of requirements comes from the system and is specific to the CubETH mission. These are listed here and identified with the label Mission Requirement (**MR**).

MR.1 The EPS shall provide enough power for nominal operations in sunlight as well as during eclipses.

MR.2 The EPS shall operate between -30°C and +40 °C.

MR.3 The EPS shall provide separated power lines with overcurrent protection for the different subsystems.

MR.4 The power supply shall be regulated at +3.3V ± 0.3V .

MR.5 The EPS shall be able to deliver currents up to 2A while irradiated by the Sun.

MR.6 The EPS shall fully recharge thebatteries inless than [TBD] orbits after any of the defined modes of operation.

MR.7 The energy storage (batteries) shall be redundant.

MR.8 From activation, after ejection from the P-POD, the EPS shall always stay on.

MR.9 The mission and therefore the EPS shall last at least 2 years.

B Under voltage discharge hysteresis protection

The discharge of the battery is protected by a hysteresis comparator (U4B), it's characteristics are presented here under in fig. 25. When the comparator has an output at 0 V, discharge can take place.

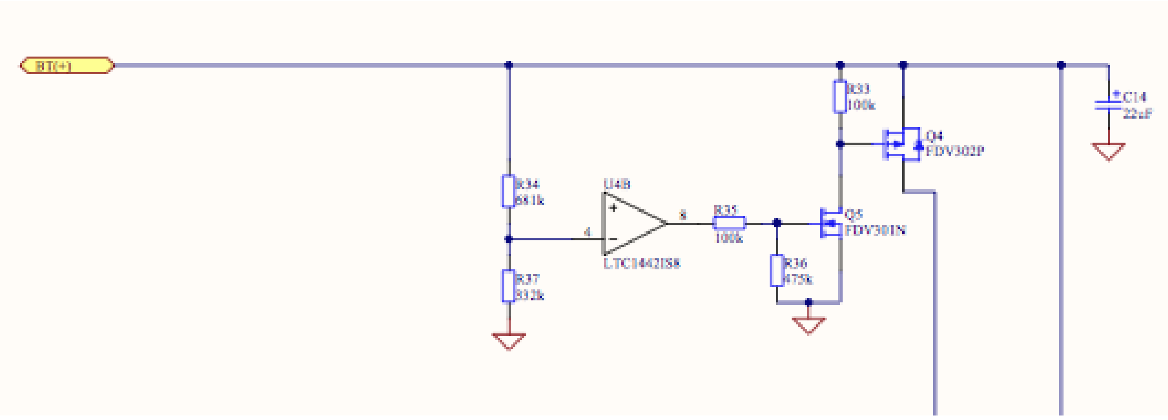


Figure 24: Hysteresis comparator in the discharge diagram

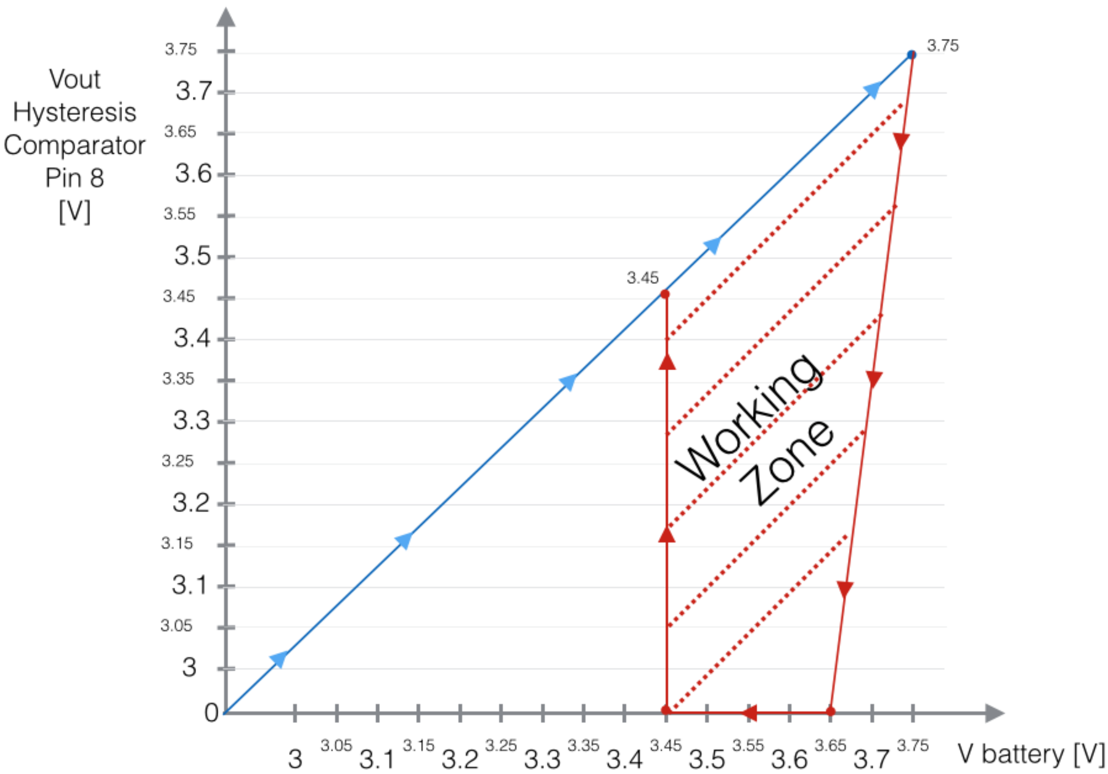


Figure 25: Hysteresis curve of the comparator

C Troubleshoot

Symptoms	Section	Page
When a voltage is applied between the VCC and the GND, the power source gets stuck at 0.7 V and the current rises up the limit imposed by the user on the current limitator.	5.1	13.
VCC is at 0 V even though SC+ was set at 3.3 V through a power source.	6.1	16
The charge command (CHG CMD) is always on a high level and dissipation is always active.	6.2	17
The charge is never activated due to the shutdown always activated	6.3	18
The discharge never gets activated even when the bus voltage is under 3.3 V and the battery is fully charged	6.4	20
Incoherency for the voltages measured at the pins of the resistors, impossibility to verify if they are dissipating or not	6.5	22
Charge and discharge get activated at the same time	6.6	24

Table 2: Troubleshoot table

D Simulations

In order to help find the bugs, during the project a couple simulations have been run on two different programs :

- **Multisim from National Instruments** : With multisim, the "bus reg" and the "dissipation" circuits have been simulated. (c.f appendix F). EPFL has licenses for Multisim in the electronics lab if needed.

- **LT spice from Linear Technologies** : The "charge" has been simulated with LT spice IV , the software can be downloaded from http://www.linear.com/designtools/software/. I recommend the windows version over the mac one, since it is much more complete.

These simulations will be joined to the project folder. Also, in order to visualiser the routing of Quentin Cabrol's [1] pcb routing, the software **Allegro Viewer** was used.

E JTAG-MM6 connector

A JTAG-MM6 connector was also built during this project in order to facilitate the flashing of the EPS for the programming phase.

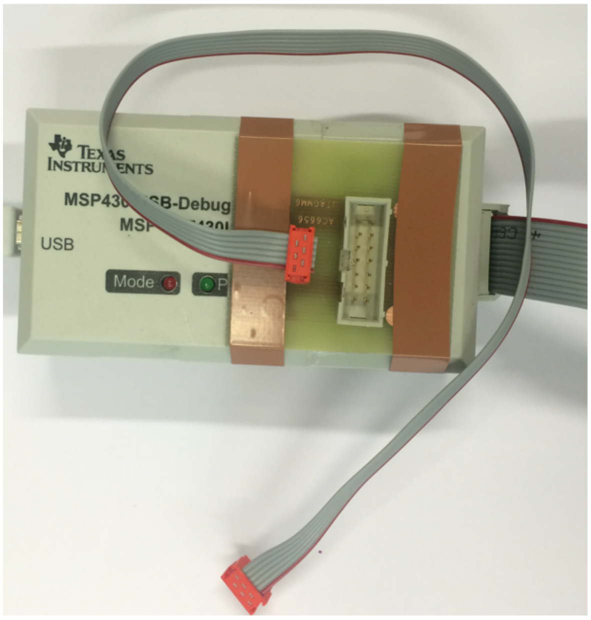
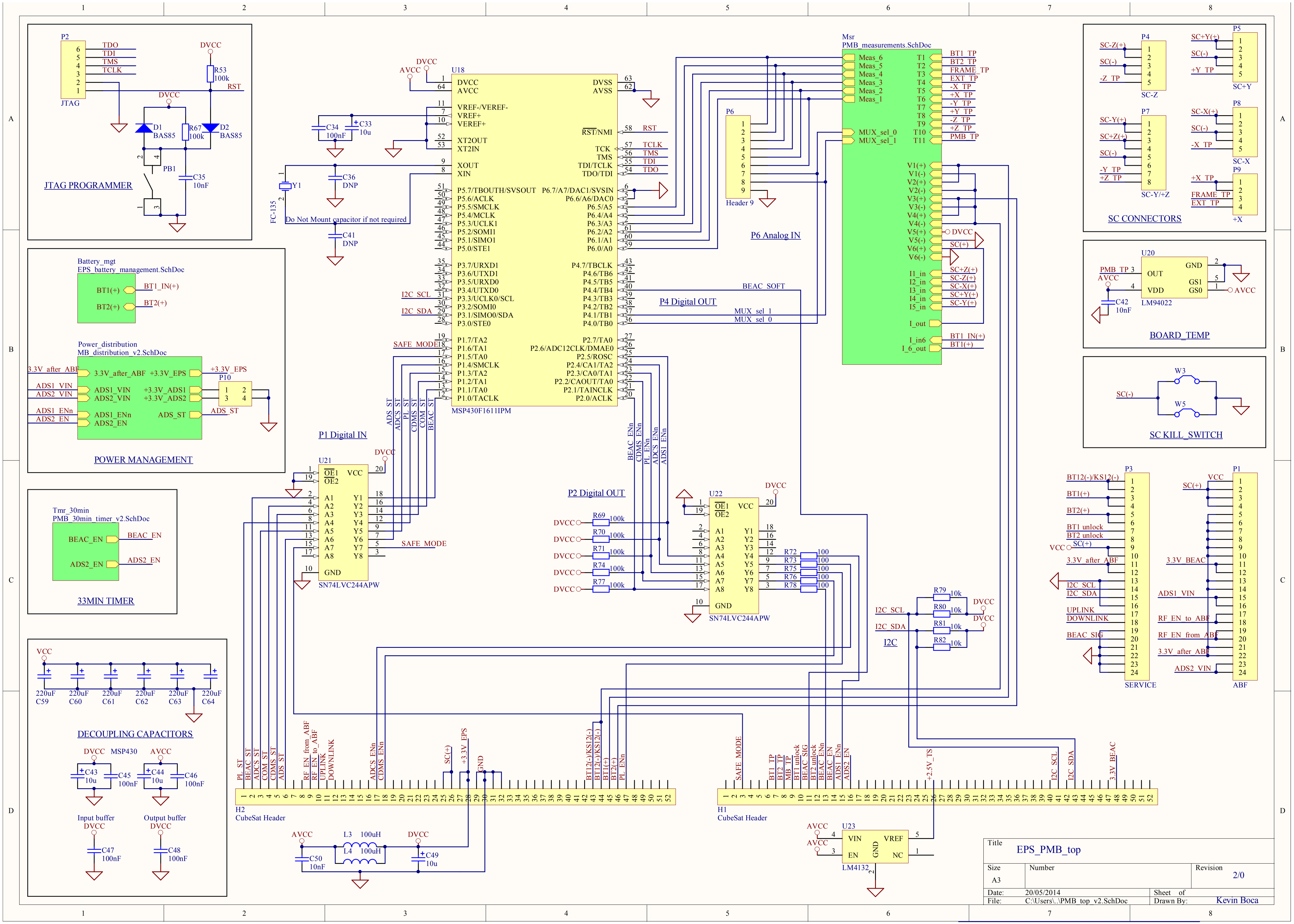


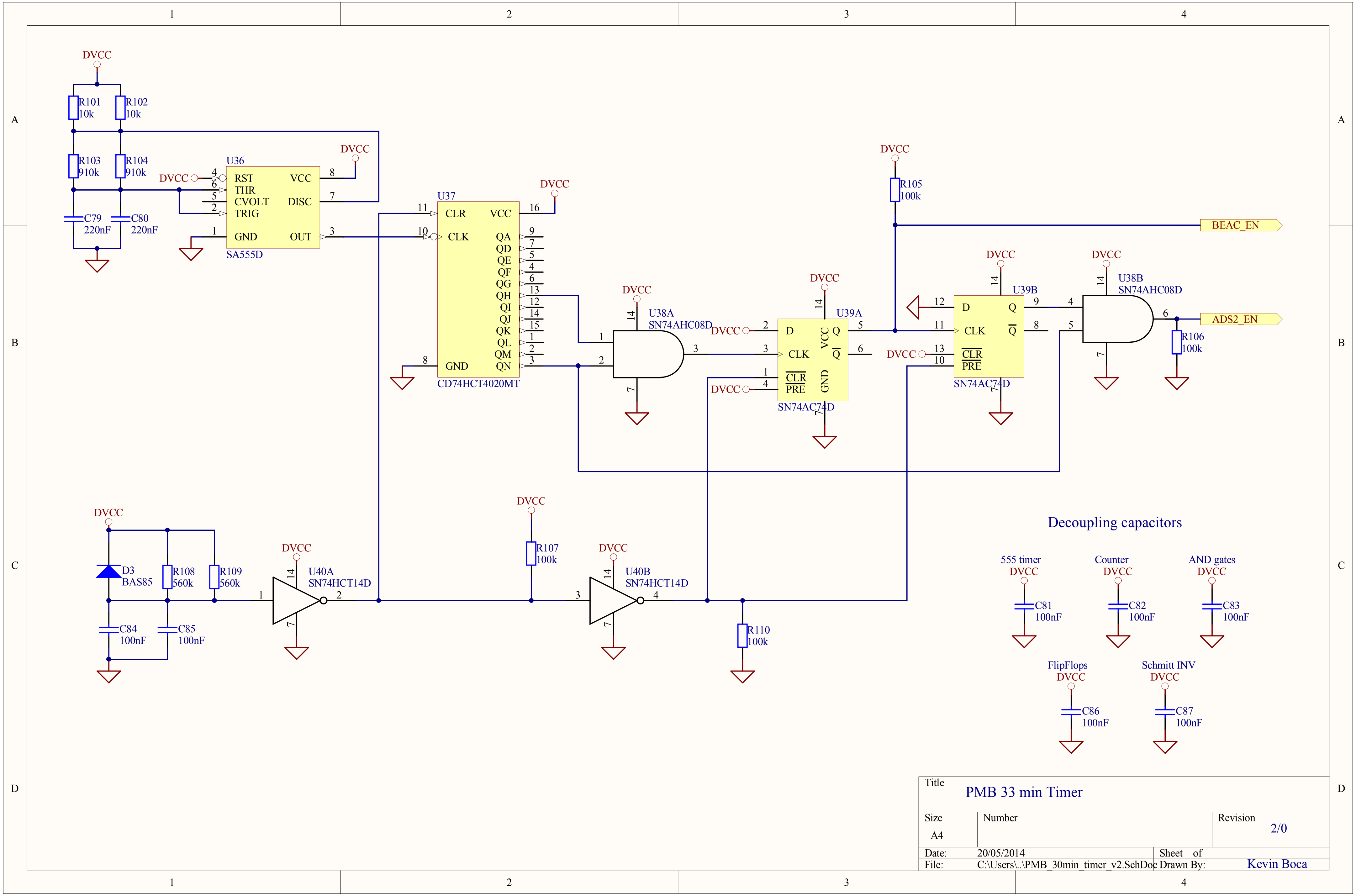
Figure 26: The JTAG-MM6 connector

F EPS PMB-MB corrected electrical diagrams

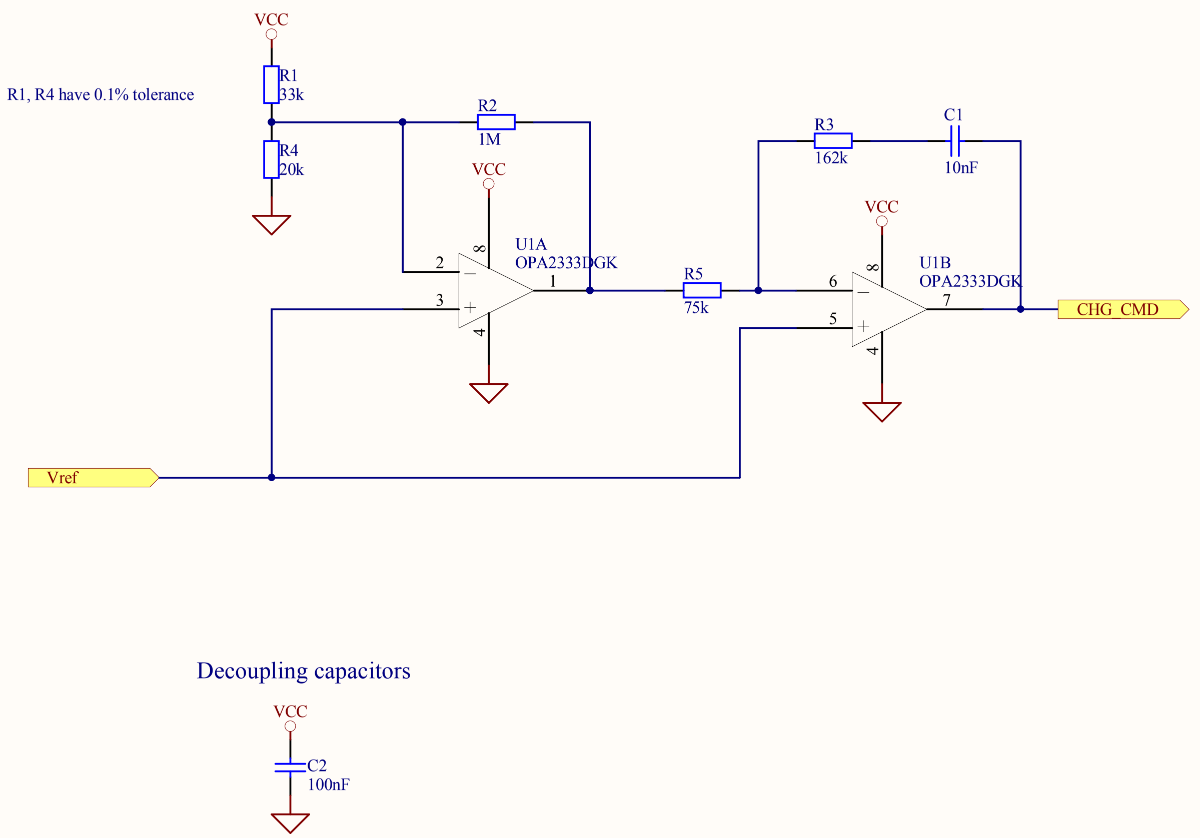
The following diagrams are the ones that should be used from now on for the EPS PMB-MB board, they represent all the corrections that have been made during this paper.



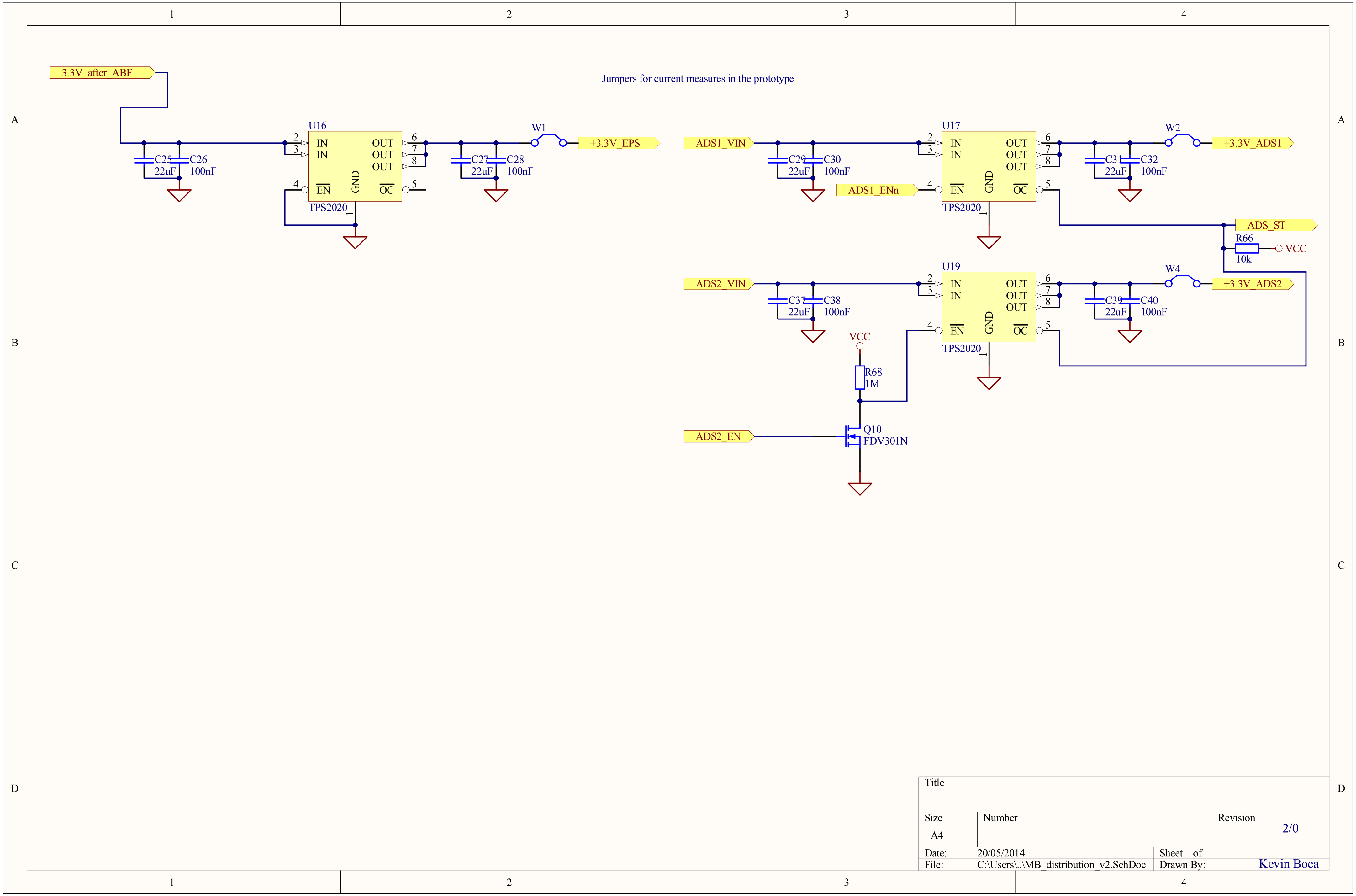
JTAG PROGRAMMER
POWER MANAGEMENT
33MIN TIMER
DECOUPLING CAPACITORS
P1 Digital IN
P2 Digital OUT
P4 Digital OUT
P6 Analog IN
I2C
SC CONNECTORS
BOARD_TEMP
SC KILL_SWITCH
MSP430F1611IPM
SN74LVC244APW
LM94022
LM4132
H1 CubeSat Header
H2 CubeSat Header
Do Not Mount capacitor if not required
Title EPS_PMB_top
Size A3
Revision 2/0
Date: 20/05/2014
File: C:\Users\..\PMB_top_v2.SchDoc
Drawn By: Kevin Boca



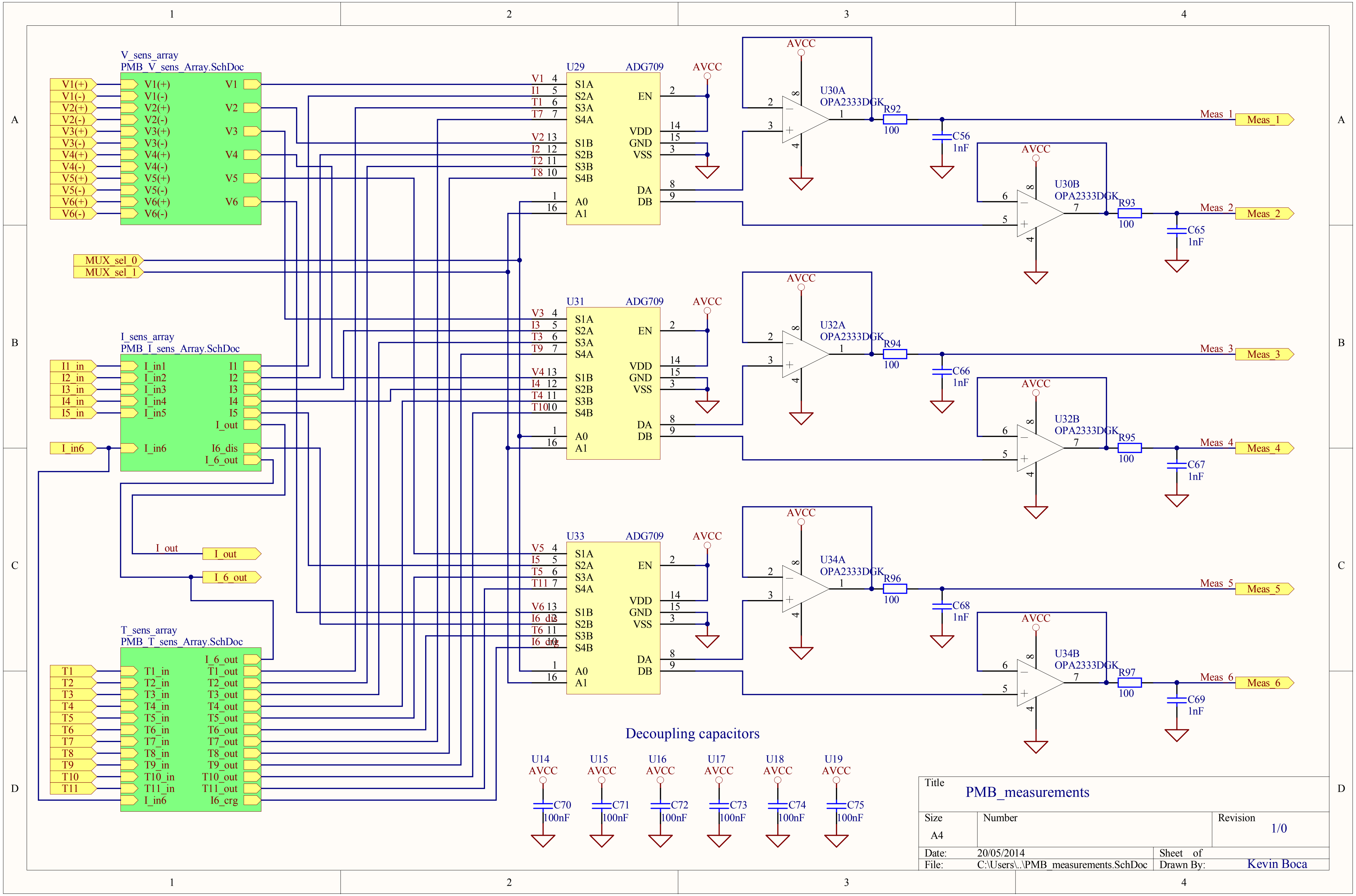
DVCC
R101 10k
R102 10k
R103 910k
R104 910k
C79 220nF
C80 220nF
U36
RST THR CVOLT TRIG GND
VCC DISC OUT
SA555D
U37
CLR CLK GND
VCC QA QD QE QF QG QH QI QJ QK QL QM QN
CD74HCT4020MT
U38A SN74AHC08D
U39A
D CLK CLR PRE VCC GND Q Q
SN74AC74D
U39B
SN74AC74D
U38B SN74AHC08D
R105 100k
R106 100k
BEAC_EN
ADS2_EN
D3 BAS85
R108 560k
R109 560k
C84 100nF
C85 100nF
U40A SN74HCT14D
R107 100k
U40B SN74HCT14D
R110 100k
Decoupling capacitors
555 timer
C81 100nF
Counter
C82 100nF
AND gates
C83 100nF
FlipFlops
C86 100nF
Schmitt INV
C87 100nF
Title
PMB 33 min Timer
Size A4
Number
Revision 2/0
Date: 20/05/2014
Sheet of
File: C:\Users\..\PMB_30min_timer_v2.SchDoc
Drawn By: Kevin Boca



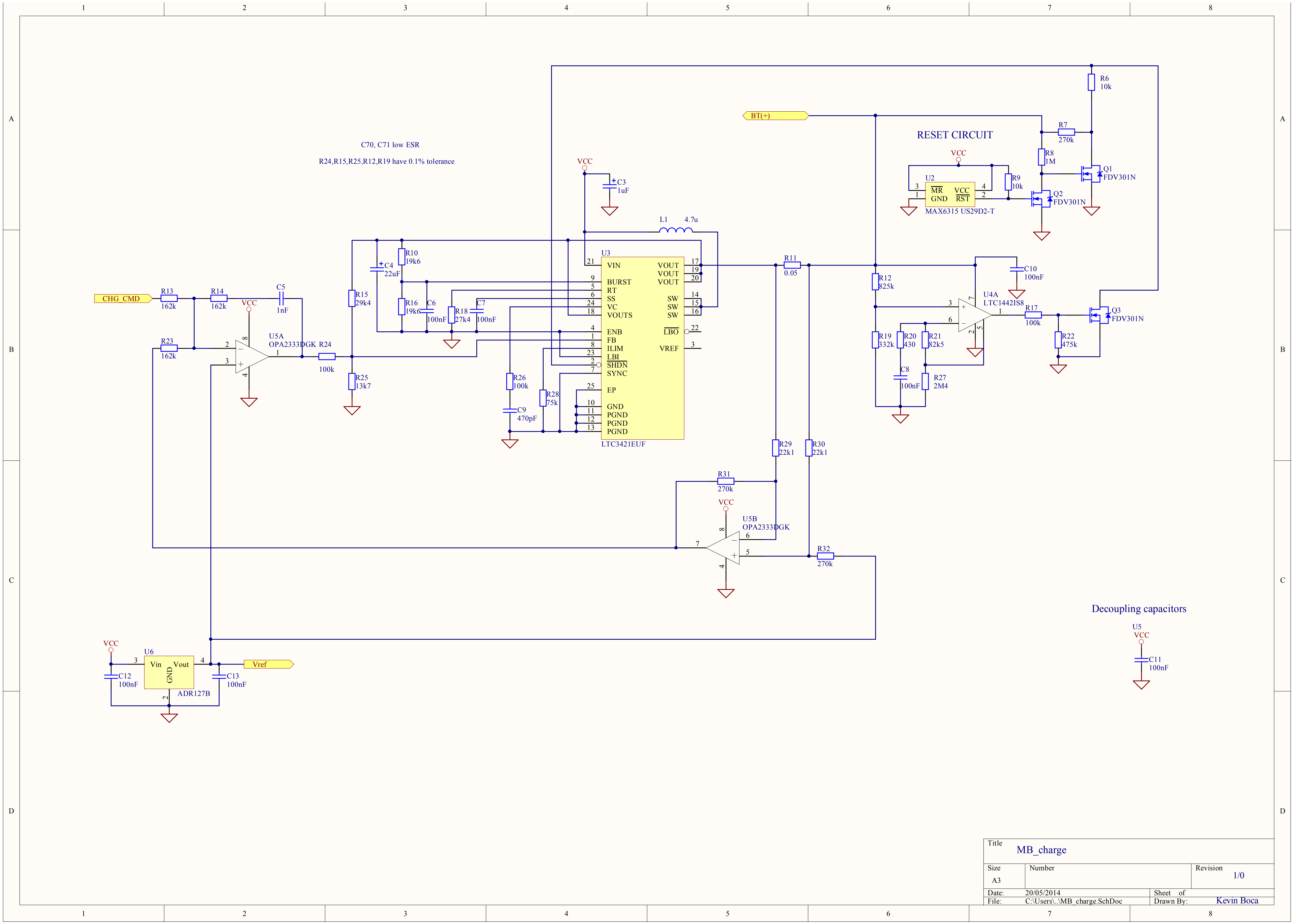
Title	MB_bus_regulation		
Size	Number		Revision
A4			1/0
Date:	20/05/2014	Sheet of	
File:	C:\Users\..\MB_bus_regulation.SchDoc	Drawn By:	Kevin Boca



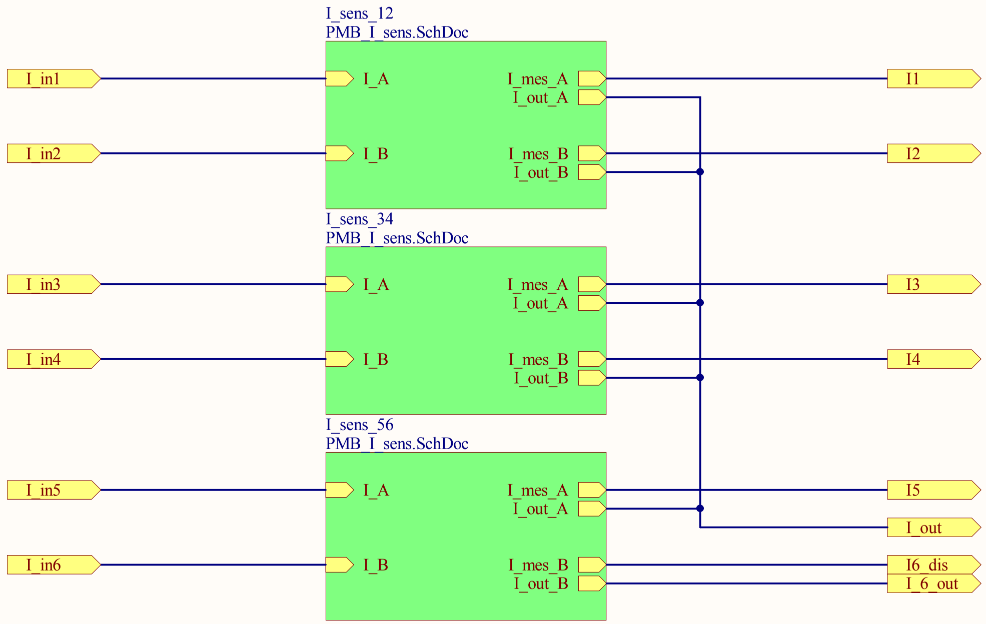
Jumpers for current measures in the prototype
3.3V_after_ABF
U16
TPS2020_
IN
IN
OUT
OUT
OUT
EN
GND
OC
C25
22uF
C26
100nF
C27
22uF
C28
100nF
W1
+3.3V_EPS
ADS1_VIN
C29
22uF
C30
100nF
ADS1_ENn
U17
TPS2020_
C31
22uF
C32
100nF
W2
+3.3V_ADS1
ADS_ST
R66
10k
VCC
ADS2_VIN
C37
22uF
C38
100nF
U19
TPS2020_
C39
22uF
C40
100nF
W4
+3.3V_ADS2
VCC
R68
1M
Q10
FDV301N
ADS2_EN
Title
Size
A4
Number
Revision
2/0
Date:
20/05/2014
Sheet of
File:
C:\Users\..\MB_distribution_v2.SchDoc
Drawn By:
Kevin Boca



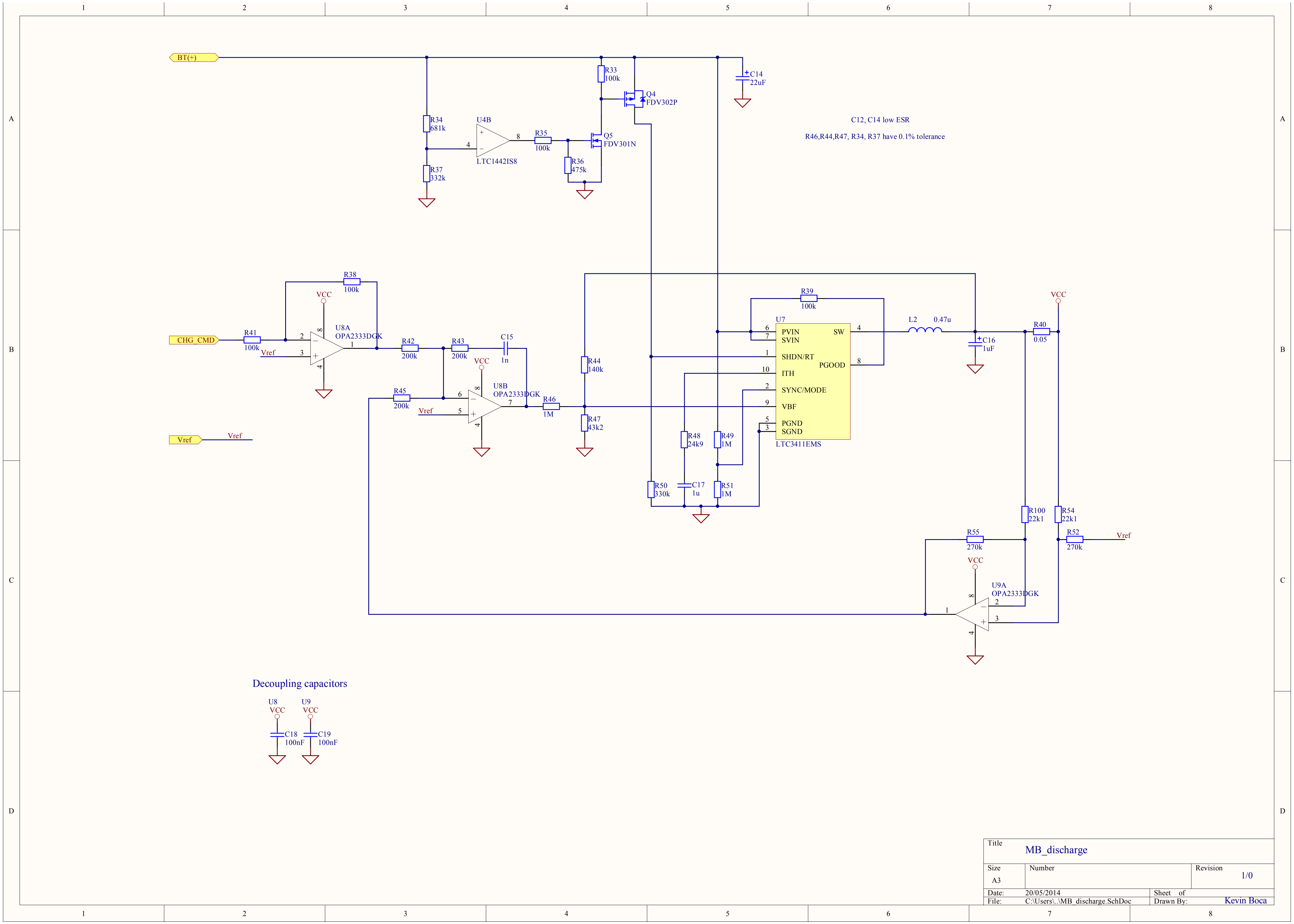
V_sens_array
PMB_V_sens_Array.SchDoc
I_sens_array
PMB_I_sens_Array.SchDoc
T_sens_array
PMB_T_sens_Array.SchDoc
MUX_sel_0
MUX_sel_1
I_out
I_6_out
U29 ADG709
U31 ADG709
U33 ADG709
U30A OPA2333DGK
U30B OPA2333DGK
U32A OPA2333DGK
U32B OPA2333DGK
U34A OPA2333DGK
U34B OPA2333DGK
AVCC
R92 100
R93 100
R94 100
R95 100
R96 100
R97 100
C56 1nF
C65 1nF
C66 1nF
C67 1nF
C68 1nF
C69 1nF
Meas_1
Meas_2
Meas_3
Meas_4
Meas_5
Meas_6
Decoupling capacitors
U14 AVCC C70 100nF
U15 AVCC C71 100nF
U16 AVCC C72 100nF
U17 AVCC C73 100nF
U18 AVCC C74 100nF
U19 AVCC C75 100nF
Title PMB_measurements
Size A4
Number
Revision 1/0
Date: 20/05/2014
File: C:\Users\..\PMB_measurements.SchDoc
Sheet of
Drawn By: Kevin Boca

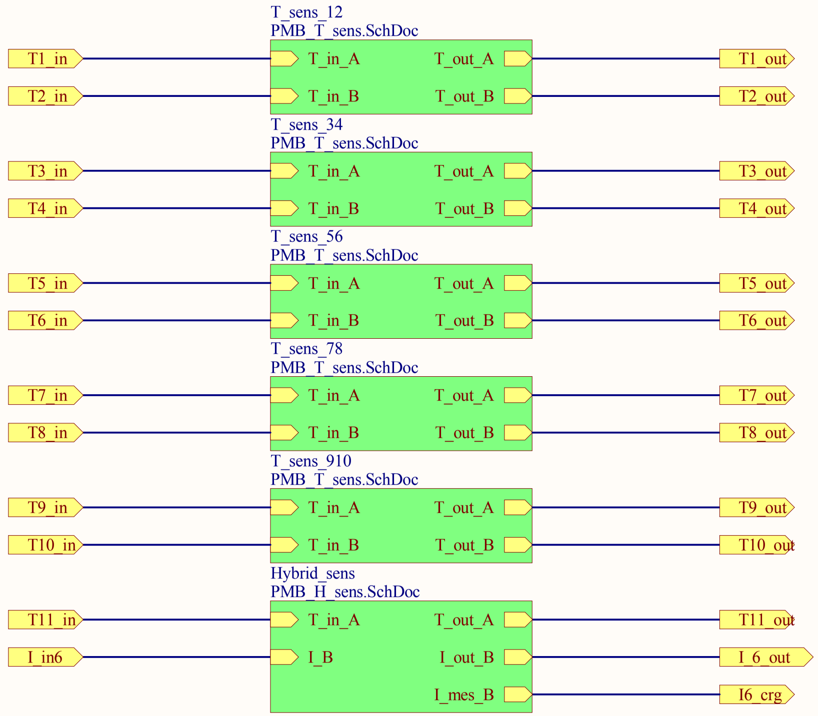


RESET CIRCUIT
C70, C71 low ESR
R24,R15,R25,R12,R19 have 0.1% tolerance
Decoupling capacitors
BT(+)
CHG_CMD
Vref
VCC
U3
LTC3421EUF
VIN
BURST
RT
SS
VC
VOUTS
ENB
FB
ILIM
LBI
SHDN
SYNC
EP
GND
PGND
VOUT
SW
LBO
VREF
L1 4.7u
C3 1uF
C4 22uF
C5 1nF
C6 100nF
C7 100nF
C8 100nF
C9 470pF
C10 100nF
C11 100nF
C12 100nF
C13 100nF
R6 10k
R7 270k
R8 1M
R9 10k
R10 19k6
R11 0.05
R12 825k
R13 162k
R14 162k
R15 29k4
R16 19k6
R17 100k
R18 27k4
R19 332k
R20 430
R21 82k5
R22 475k
R23 162k
R24 100k
R25 13k7
R26 100k
R27 2M4
R28 75k
R29 22k1
R30 22k1
R31 270k
R32 270k
Q1 FDV301N
Q2 FDV301N
Q3 FDV301N
U2
MR
GND
VCC
RST
MAX6315 US29D2-T
U4A
LTC1442IS8
U5A
OPA2333DGK
U5B
OPA2333DGK
U5
U6
Vin
Vout
ADR127B
Title
MB_charge
Size
A3
Number
Revision
1/0
Date:
20/05/2014
File:
C:\Users\..\MB_charge.SchDoc
Sheet of
Drawn By:
Kevin Boca

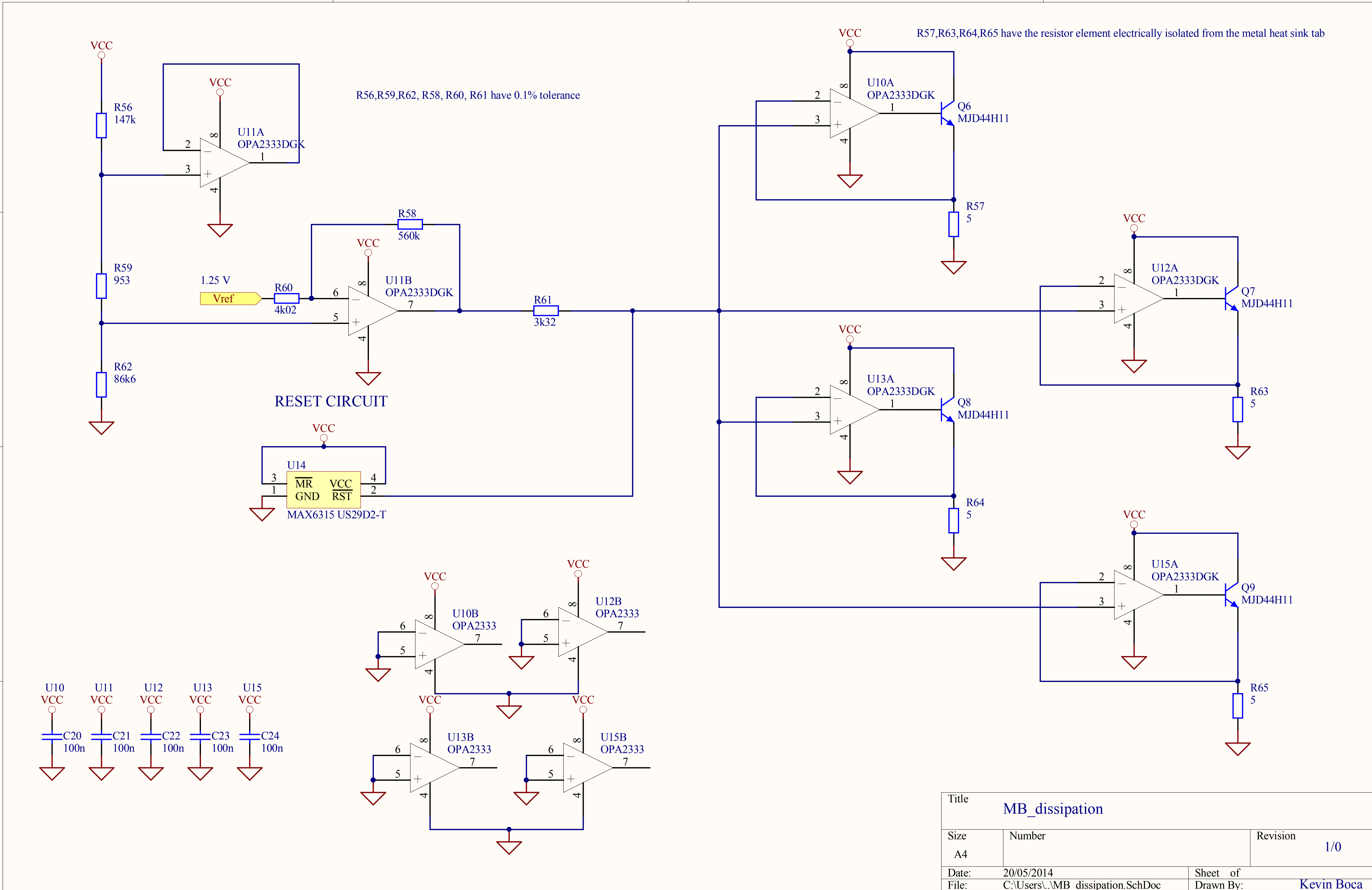


Title	PMB_I_sens_Array		
Size	Number		Revision
A4			1/0
Date:	20/05/2014	Sheet of	
File:	C:\Users\..\PMB_I_sens_Array.SchDoc	Drawn By:	Kevin Boca

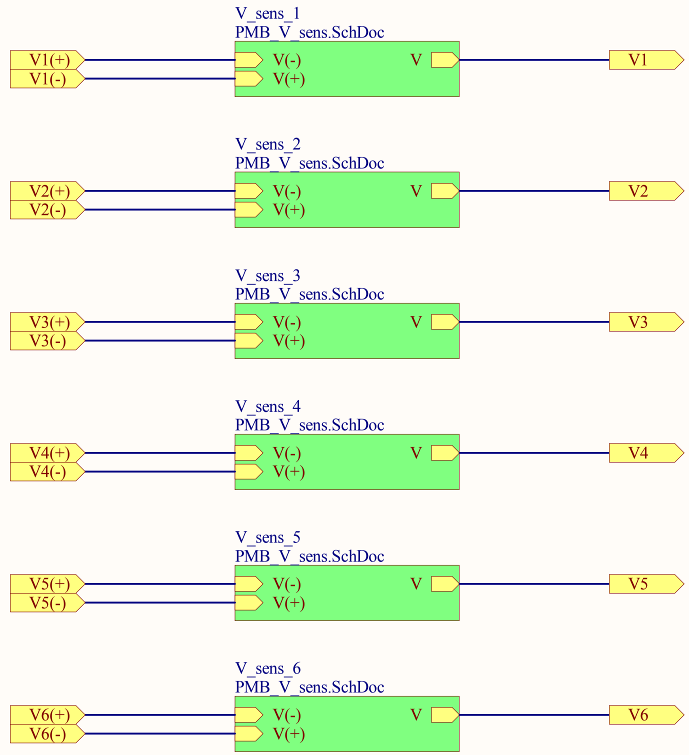

BT(+)
R33
100k
Q4
FDV302P
C14
22uF
R34
681k
U4B
LTC1442IS8
R35
100k
Q5
FDV301N
R36
475k
R37
332k
C12, C14 low ESR
R46,R44,R47, R34, R37 have 0.1% tolerance
R38
100k
VCC
CHG_CMD
R41
100k
Vref
U8A
OPA2333DGK
R42
200k
R43
200k
C15
1n
U8B
OPA2333DGK
R45
200k
R46
1M
R44
140k
R47
43k2
Vref
R39
100k
U7
PVIN
SVIN
SHDN/RT
ITH
SYNC/MODE
VBF
PGND
SGND
SW
PGOOD
LTC3411EMS
L2
0.47u
C16
1uF
R40
0.05
R48
24k9
R49
1M
R50
330k
C17
1u
R51
1M
R100
22k1
R54
22k1
R55
270k
R52
270k
U9A
OPA2333DGK
Decoupling capacitors
U8
U9
C18
100nF
C19
100nF
Title
MB_discharge
Size
A3
Number
Revision
1/0
Date:
20/05/2014
File:
C:\Users\..\MB_discharge.SchDoc
Sheet of
Drawn By:
Kevin Boca



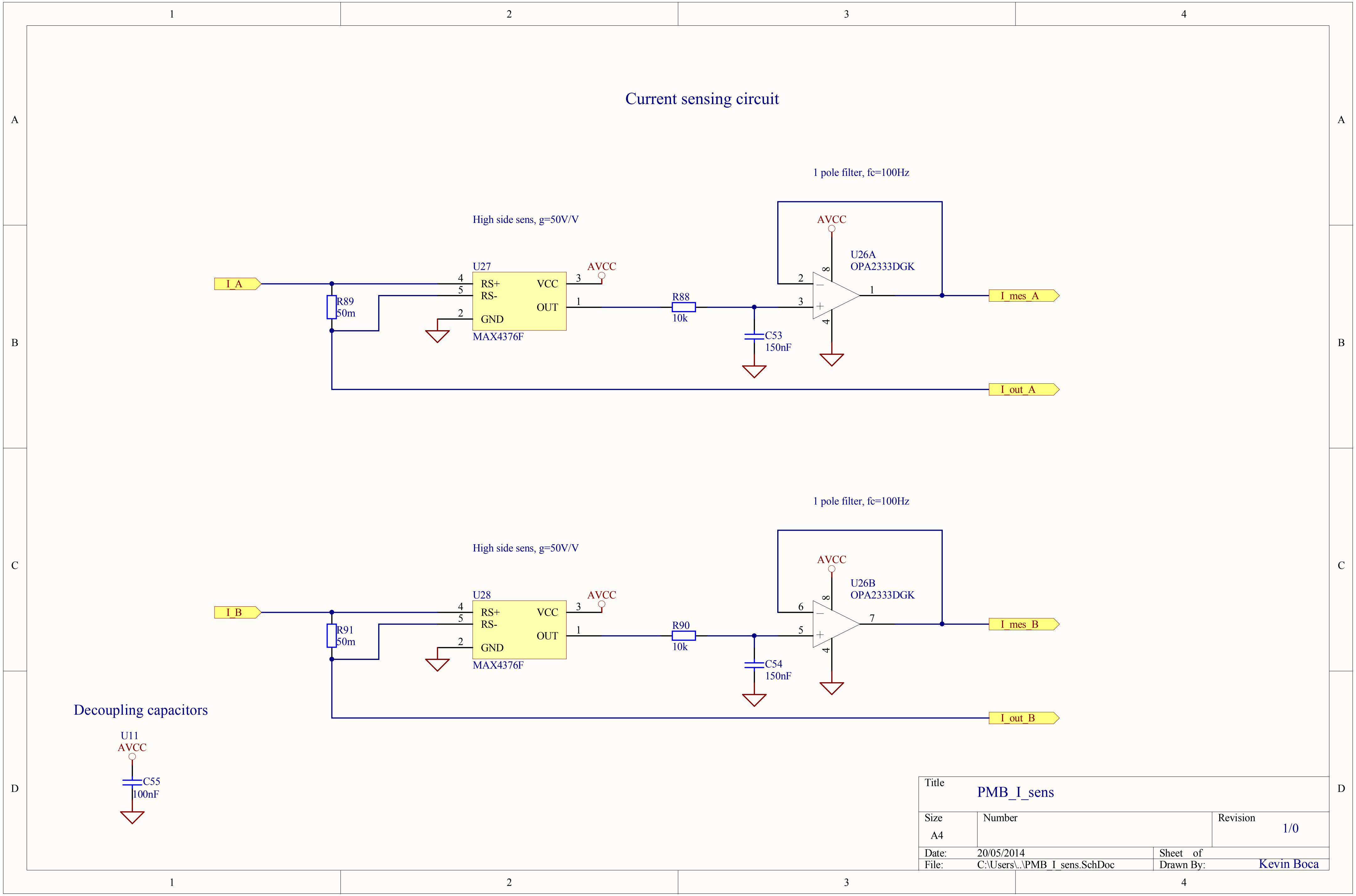
Title	PMB_T_sens_Array	
Size: A4	Number	Revision: 1/0
Date: 20/05/2014		Sheet of
File: C:\Users\..\PMB_T_sens_Array.SchDoc		Drawn By: Kevin Boca



Title	MB_dissipation		
Size	Number		Revision
A4			1/0
Date:	20/05/2014	Sheet of	
File:	C:\Users\..\MB_dissipation.SchDoc	Drawn By:	Kevin Boca

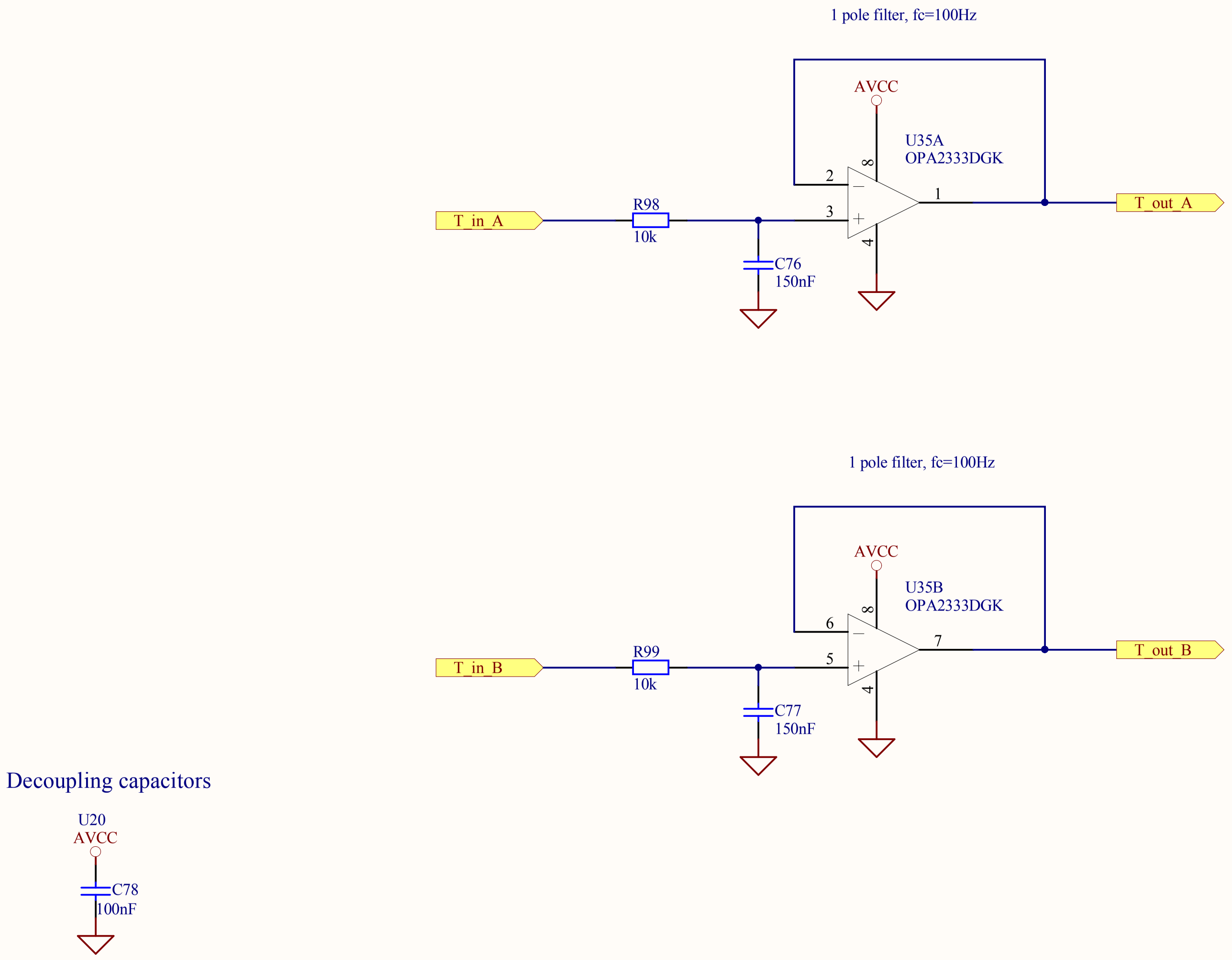


Title	PMB_V_sens_Array		
Size A4	Number		Revision 1/0
Date:	20/05/2014	Sheet of	
File:	C:\Users\..\PMB_V_sens_Array.SchDoc	Drawn By:	Kevin Boca

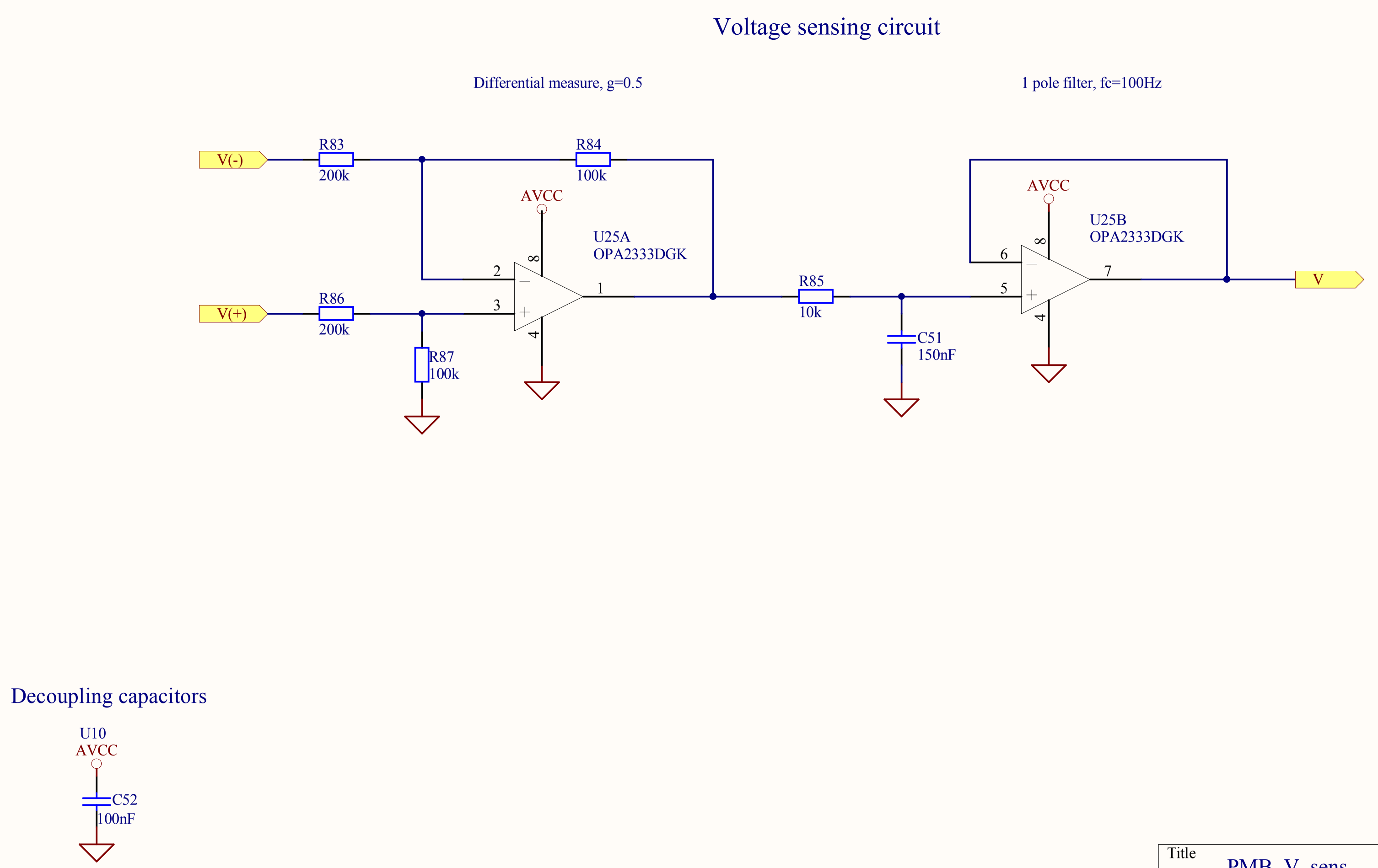


Current sensing circuit
High side sens, g=50V/V
1 pole filter, fc=100Hz
I_A
R89
50m
U27
RS+
RS-
GND
VCC
OUT
MAX4376F
AVCC
R88
10k
C53
150nF
U26A
OPA2333DGK
I_mes_A
I_out_A
High side sens, g=50V/V
1 pole filter, fc=100Hz
I_B
R91
50m
U28
RS+
RS-
GND
VCC
OUT
MAX4376F
AVCC
R90
10k
C54
150nF
U26B
OPA2333DGK
I_mes_B
I_out_B
Decoupling capacitors
U11
AVCC
C55
100nF
Title
PMB_I_sens
Size
A4
Number
Revision
1/0
Date:
20/05/2014
File:
C:\Users\..\PMB_I_sens.SchDoc
Sheet of
Drawn By:
Kevin Boca

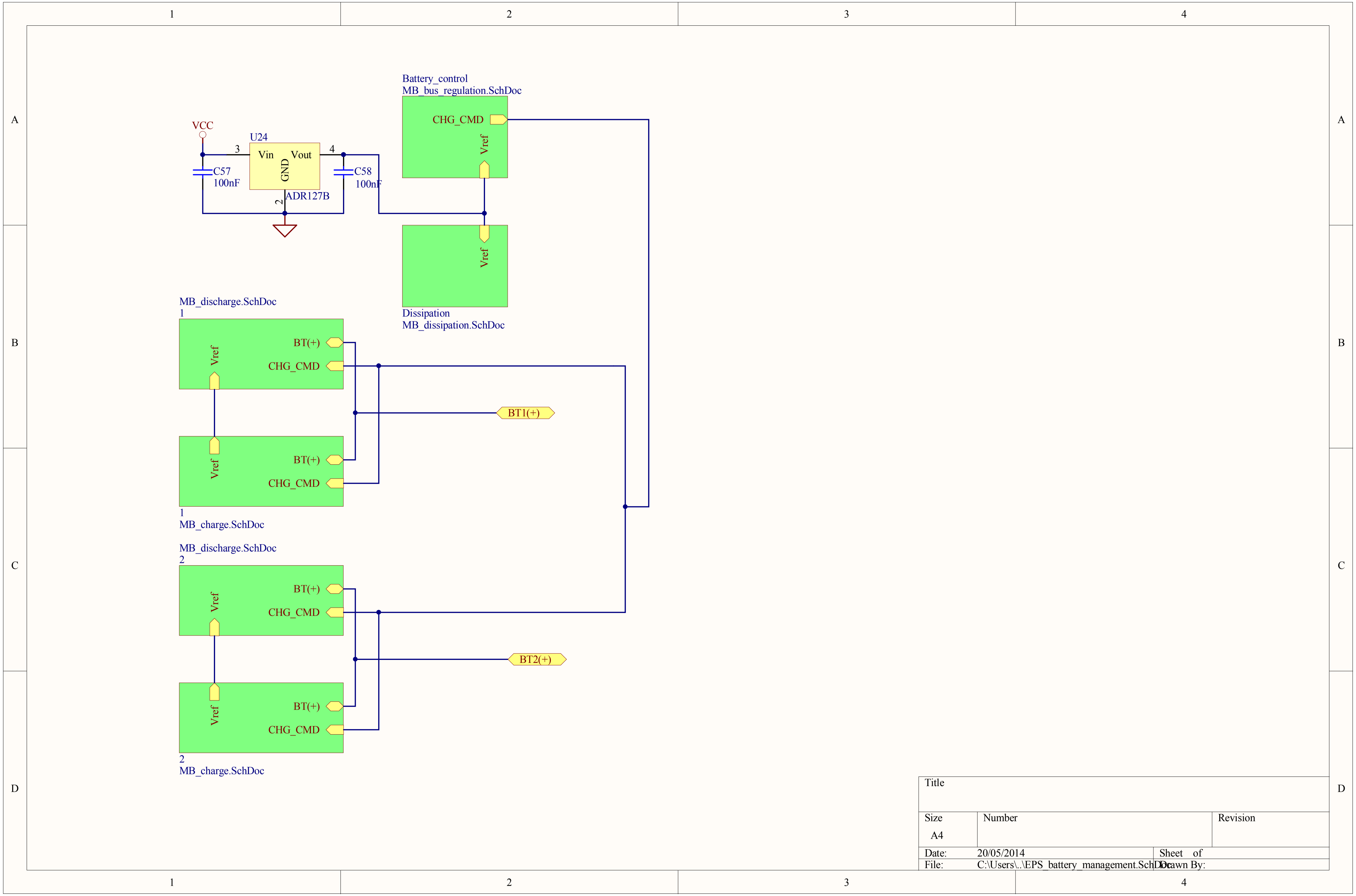
Temperature measure



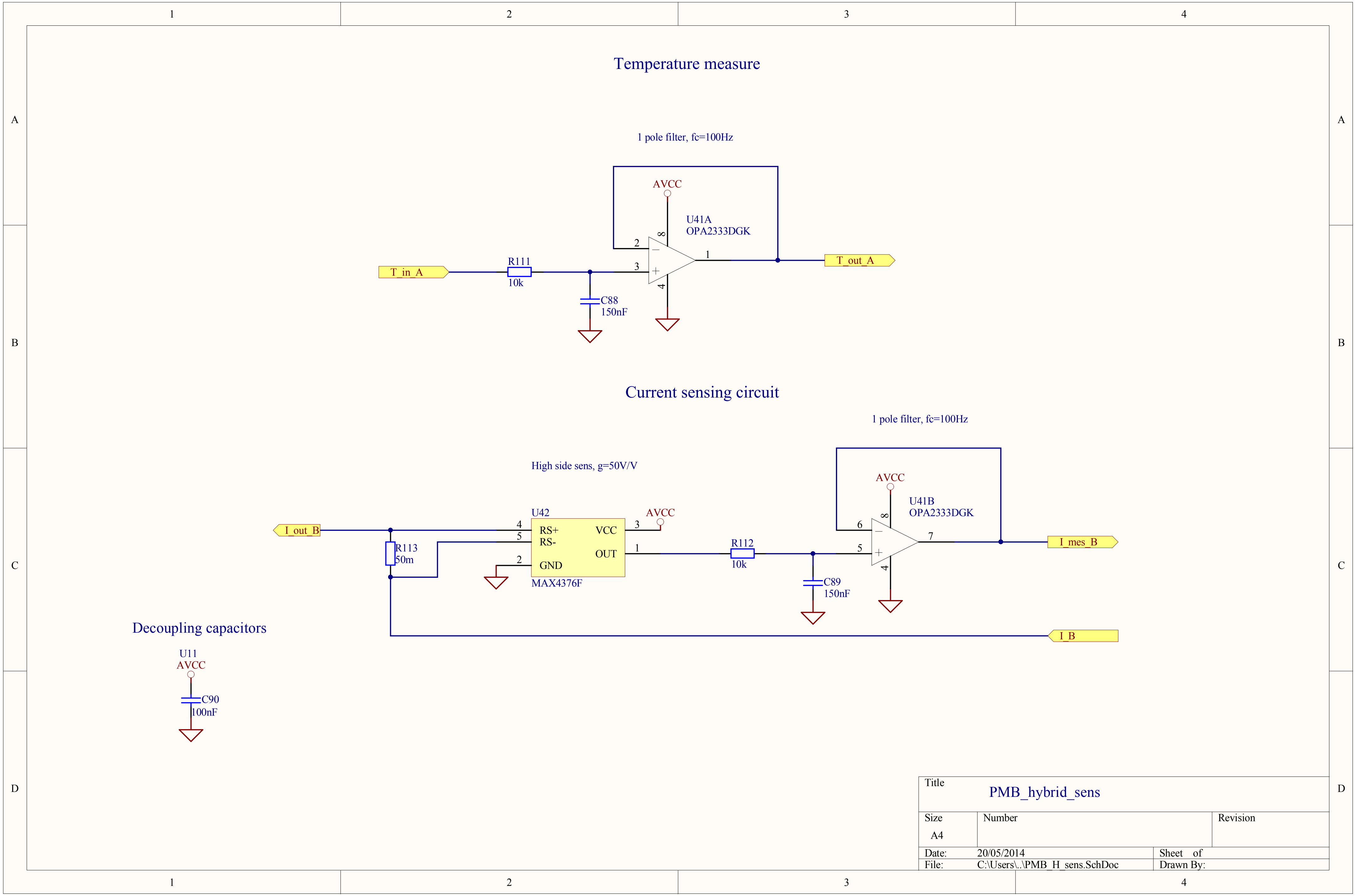
Title	PMB_T_sens		
Size	Number		Revision
A4			1/0
Date:	20/05/2014	Sheet of	
File:	C:\Users\..\PMB_T_sens.SchDoc	Drawn By:	Kevin Boca



Title	PMB_V_sens		
Size	Number		Revision
A4			1/0
Date:	20/05/2014	Sheet of	
File:	C:\Users\..\PMB_V_sens.SchDoc	Drawn By:	Kevin Boca



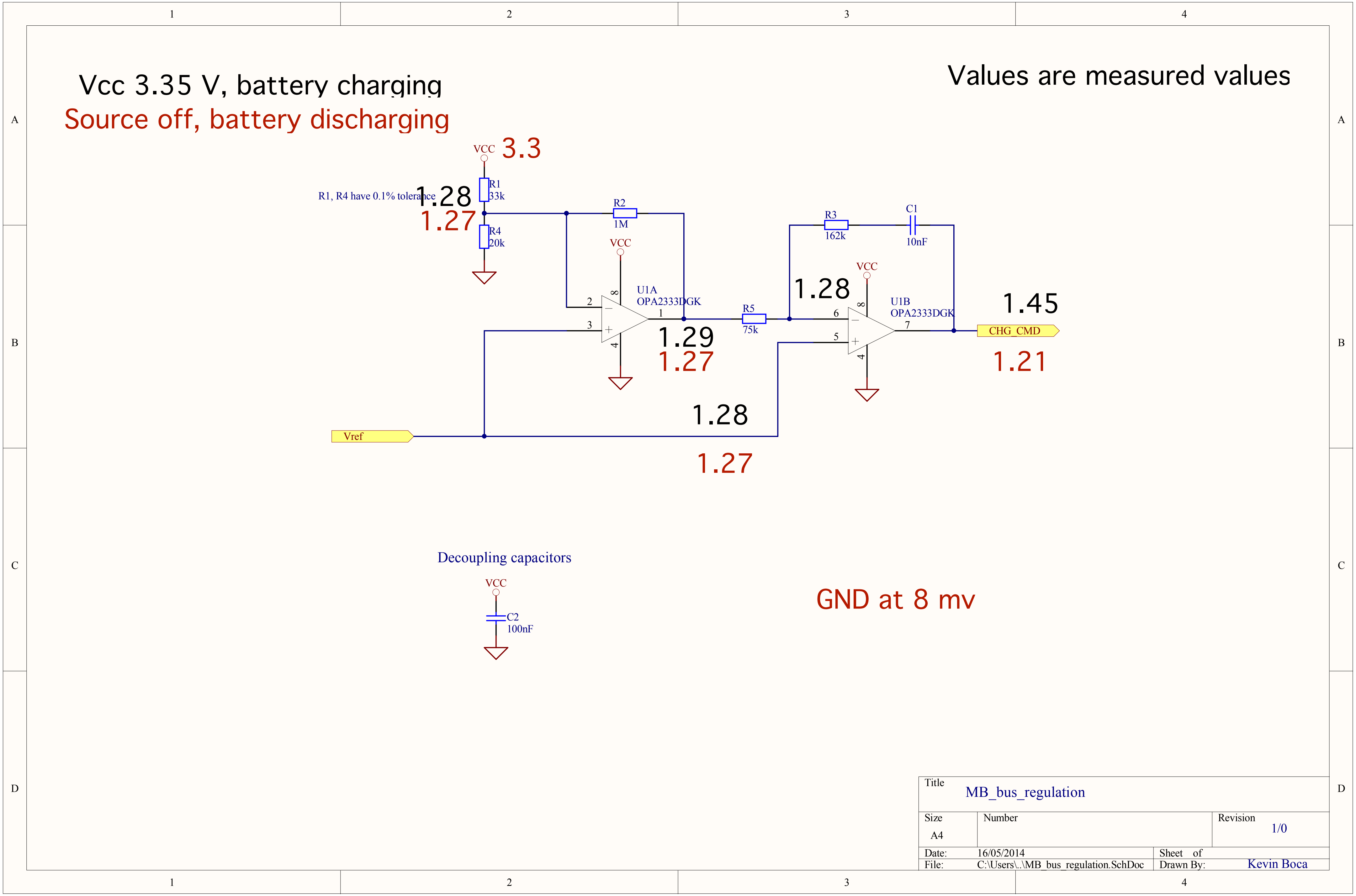
VCC
U24
Vin
Vout
GND
ADR127B
3
4
2
C57
100nF
C58
100nF
Battery_control
MB_bus_regulation.SchDoc
CHG_CMD
Vref
Vref
Dissipation
MB_dissipation.SchDoc
MB_discharge.SchDoc
1
BT(+)
CHG_CMD
Vref
BT1(+)
Vref
BT(+)
CHG_CMD
1
MB_charge.SchDoc
MB_discharge.SchDoc
2
BT(+)
CHG_CMD
Vref
BT2(+)
Vref
BT(+)
CHG_CMD
2
MB_charge.SchDoc
Title
Size
A4
Number
Revision
Date: 20/05/2014
Sheet of
File: C:\Users\..\EPS_battery_management.SchDoc
Drawn By:

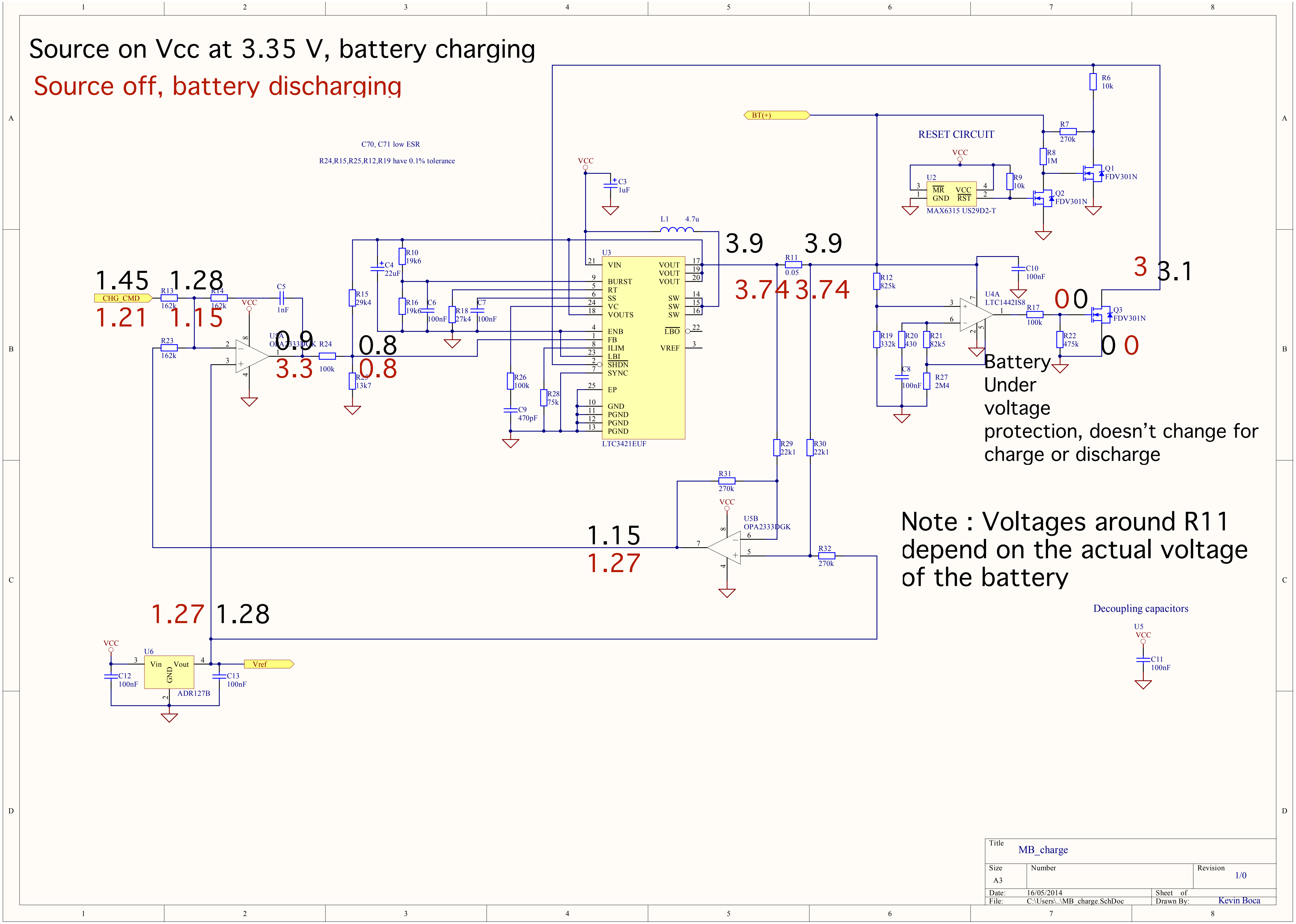


Temperature measure
1 pole filter, fc=100Hz
AVCC
U41A
OPA2333DGK
T_in_A
R111
10k
C88
150nF
T_out_A
Current sensing circuit
1 pole filter, fc=100Hz
High side sens, g=50V/V
U42
RS+
RS-
GND
VCC
OUT
MAX4376F
AVCC
I_out_B
R113
50m
R112
10k
C89
150nF
AVCC
U41B
OPA2333DGK
I_mes_B
I_B
Decoupling capacitors
U11
AVCC
C90
100nF
Title
PMB_hybrid_sens
Size
A4
Number
Revision
Date: 20/05/2014
Sheet of
File: C:\Users\..\PMB_H_sens.SchDoc
Drawn By:

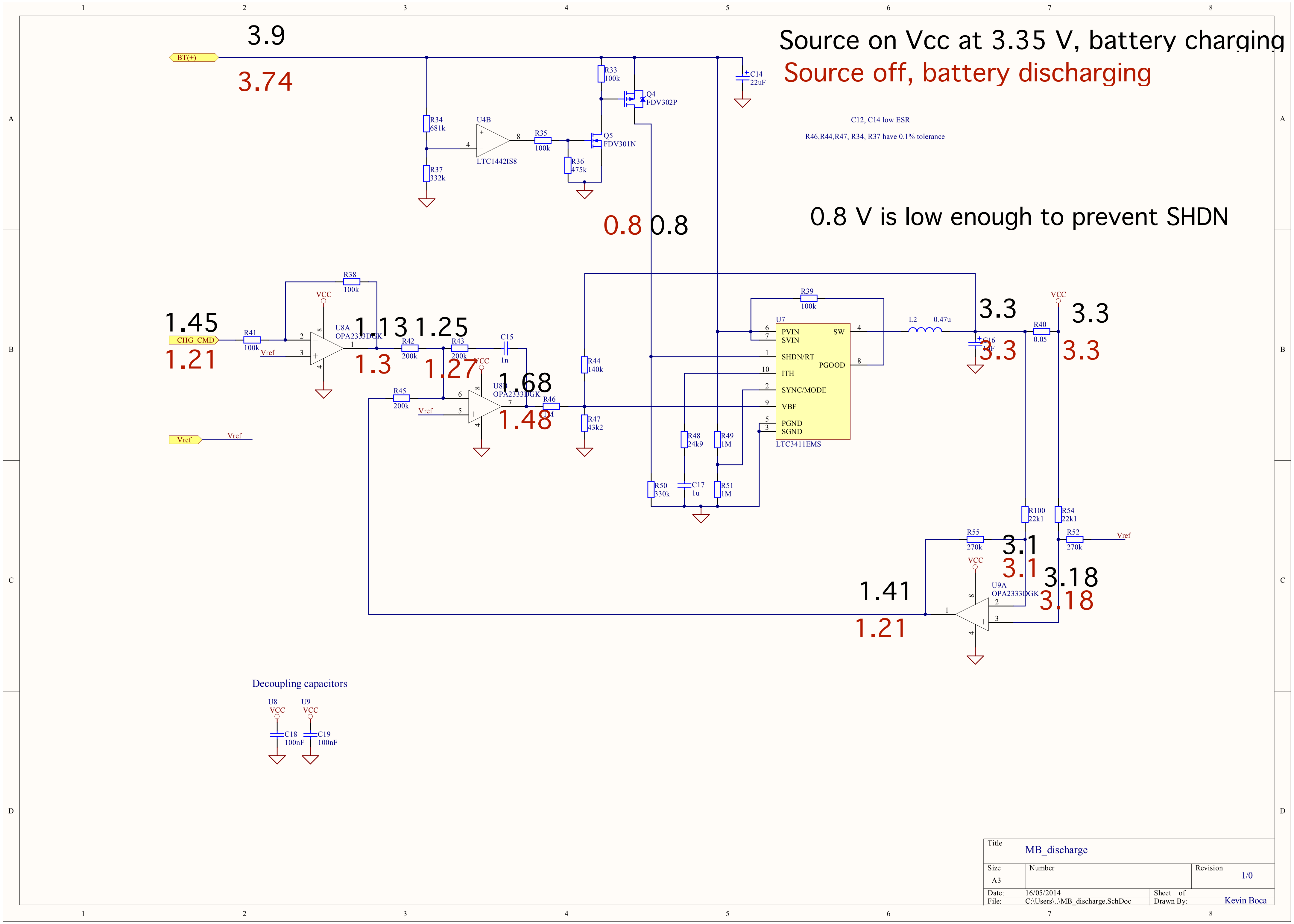
G EPS PMB-MB corrected electrical diagrams with test values

The values written on the following sheets have been obtained during a charge and a discharge test at standard temperature and pressure conditions on the "fixed" PCB. The charge and discharge worked perfectly well, however this values could slightly change with the new PCB that has a corrected routing.


Vcc 3.35 V, battery charging
Source off, battery discharging
Values are measured values
VCC 3.3
R1, R4 have 0.1% tolerance
1.28
1.27
R1
33k
R4
20k
R2
1M
VCC
U1A
OPA2333DGK
1.29
1.27
R5
75k
R3
162k
C1
10nF
VCC
1.28
U1B
OPA2333DGK
1.45
CHG_CMD
1.21
Vref
1.28
1.27
Decoupling capacitors
VCC
C2
100nF
GND at 8 mv
Title MB_bus_regulation
Size A4
Number
Revision 1/0
Date: 16/05/2014
Sheet of
File: C:\Users\..\MB_bus_regulation.SchDoc
Drawn By: Kevin Boca



Source on Vcc at 3.35 V, battery charging
Source off, battery discharging
C70, C71 low ESR
R24,R15,R25,R12,R19 have 0.1% tolerance
RESET CIRCUIT
MAX6315 US29D2-T
LTC3421EUF
OPA2333DGK
LTC1442IS8
ADR127B
FDV301N
BT(+)
CHG_CMD
Vref
VCC
1.45
1.28
1.21
1.15
0.9
3.3
0.8
3.9
3.74
3
3.1
0 0
1.27
Battery Under voltage protection, doesn't change for charge or discharge
Note : Voltages around R11 depend on the actual voltage of the battery
Decoupling capacitors
Title MB_charge
Size A3
Number
Revision 1/0
Date: 16/05/2014
File: C:\Users\..\MB_charge.SchDoc
Sheet of
Drawn By: Kevin Boca



Source on Vcc at 3.35 V, battery charging
Source off, battery discharging
C12, C14 low ESR
R46,R44,R47, R34, R37 have 0.1% tolerance
0.8 V is low enough to prevent SHDN
3.9
3.74
BT(+)
R33 100k
Q4 FDV302P
C14 22uF
R34 681k
U4B
LTC1442IS8
R35 100k
Q5 FDV301N
R36 475k
R37 332k
0.8 0.8
R38 100k
1.45
1.21
CHG_CMD
R41 100k
Vref
U8A OPA2333DGK
1.13 1.25
1.3
1.27
R42 200k
R43 200k
C15 1n
VCC
U8B OPA2333DGK
1.68
1.48
R45 200k
R46 1M
R44 140k
R47 43k2
R39 100k
U7
PVIN
SVIN
SHDN/RT
ITH
SYNC/MODE
VBF
PGND
SGND
SW
PGOOD
LTC3411EMS
L2 0.47u
C16 1uF
3.3
3.3
R40 0.05
VCC
3.3
3.3
R48 24k9
R49 1M
R50 330k
C17 1u
R51 1M
R100 22k1
R54 22k1
R55 270k
R52 270k
Vref
3.1
3.1
3.18
3.18
U9A OPA2333DGK
1.41
1.21
Decoupling capacitors
U8 VCC
U9 VCC
C18 100nF
C19 100nF
Title MB_discharge
Size A3
Number
Revision 1/0
Date: 16/05/2014
Sheet of
File: C:\Users\..\MB_discharge.SchDoc
Drawn By: Kevin Boca