

Instructions:

1. The question paper consists of 5 questions.
2. Mention units with numerical values.
3. Make suitable assumptions, if required.

Constant values (use if not specified in question) - Planck's constant (h) = 6.626×10^{-34} Jule-sec, Boltzmann constant (k) = 1.38×10^{-23} Jule/K, Room Temperature = 300 K, Thermal voltage (V_T) at room temp = 26mV, Speed of light (c) = 3×10^8 m/s, Intrinsic concentration (n_i) at room temperature (cm^{-3}) = 1.5×10^{10} for Si, dielectric constant of vacuum ϵ_0 = $8.85 \times 10^{-14} F \cdot cm^{-1}$, $\epsilon_{Si} = 4\epsilon_0$, $\epsilon_{SiO_2} = 12\epsilon_0$, Mean life time of charge carriers ($\tau = 1$ ns), $\mu_n C_{ox}$ for 180nm CMOS tech node silicon nMOS = $300 \mu A/V^2$, $\mu_p C_{ox}$ for 180 nm CMOS tech node silicon pMOS = $60 \mu A/V^2$. $|V_{th,p}| = V_{th,n} = 0.5V$ (if required), Oxide thickness $t_{ox} = 10 nm$.

1. (a) Calculate the value of the threshold voltage for an NMOS transistor with bulk doping concentration of 10^{17} atoms/ cm^{-3} .
 - (b) If 1.5V has been applied at the gate terminal of the same NMOS transistor, calculate the voltage drop across SiO_2 and Si.
 - (c) For the same condition given in (b), draw the electric field, voltage drop and charge concentration profile across SiO_2 and Si bulk with all numerical values of quantities in the graphs.
- for all above calculations ignore the flat band potential and consider the ideal SiO_2 layer with ideal $Si-SiO_2$ interface and Drain, Source and Body terminal of device are connected to ground potential.

[03+03+03]

Q:- $V_{th} = \frac{\sqrt{2qN_a \epsilon_s \phi_{Si}}}{C_{ox}} + \phi_{Si}$

$$= \sqrt{\frac{2 \times 1.6 \times 10^{-19} F \cdot V \times 10^{17} cm^{-3} \times 4 \times 8.85 \times 10^{-14} F}{10 \times 10^{-7} cm}} \times 0.81 V$$

$$= \frac{12 \times 8.85 \times 10^{-14} F}{10 \times 10^{-7} cm} + 0.81 V$$

$$= \frac{\sqrt{91.76 \times 10^{-16} \frac{F^2 V^2}{cm^{-4}}}}{1.06 \times 10^{-6} \frac{F}{cm^2}} + 0.81 V$$

$$= (0.09 + 0.81) V$$

$V_{th} = 0.9 V$

$$\phi_{Si} = 2 V_T \ln \frac{N_a}{n_i}$$

$\phi_{Si} = 0.81 V$

⑥ \Rightarrow if 1.5V is applied
at the gate
 \rightarrow drop across Si \rightarrow 0.81V

\rightarrow drop across $SiO_2 = 1.5 - 0.81$
 $= 0.69 V$

here 0.81 V across Si will
create depletion charges
& remaining Voltage will
(above 0.9) will generate
inversion charges.

$$\textcircled{C}:- \quad E_{\max. (Si)} = \sqrt{\frac{29 Na \phi_{Si}}{C_{Si}}} = \boxed{2.7 \times 10^5 \frac{V}{cm} = E_{\max. Si}}$$

$$E_{SiO_2} = 3 \cdot E_{\max. (Si)} = 8.1 \times 10^5 \frac{V}{cm}$$

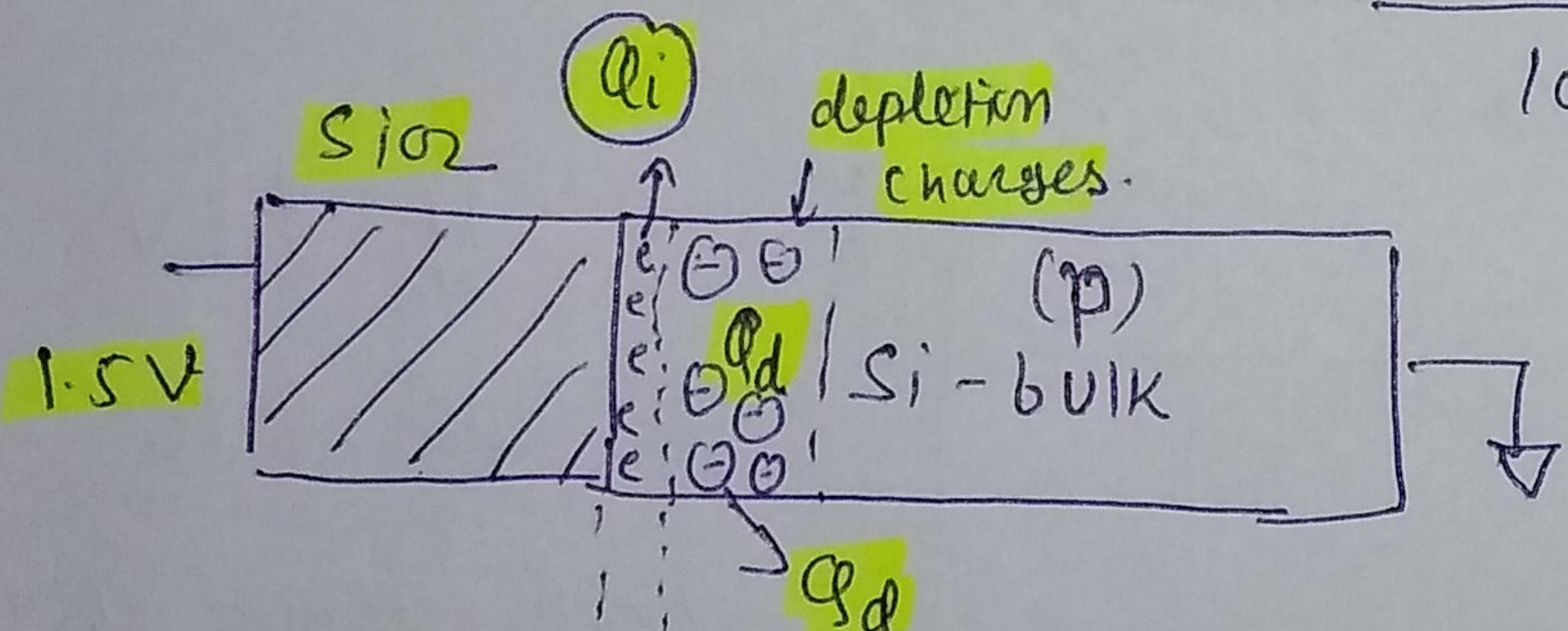
$$\Rightarrow V_G = \underbrace{\frac{\sqrt{29 Na E_{Si} \phi_{Si}}}{C_{ox}}}_{Q_d \over C_{ox}} + \cancel{\frac{Q_i}{C_{ox}}} + \phi_{Si}$$

drop across SiO_2 drop across Si

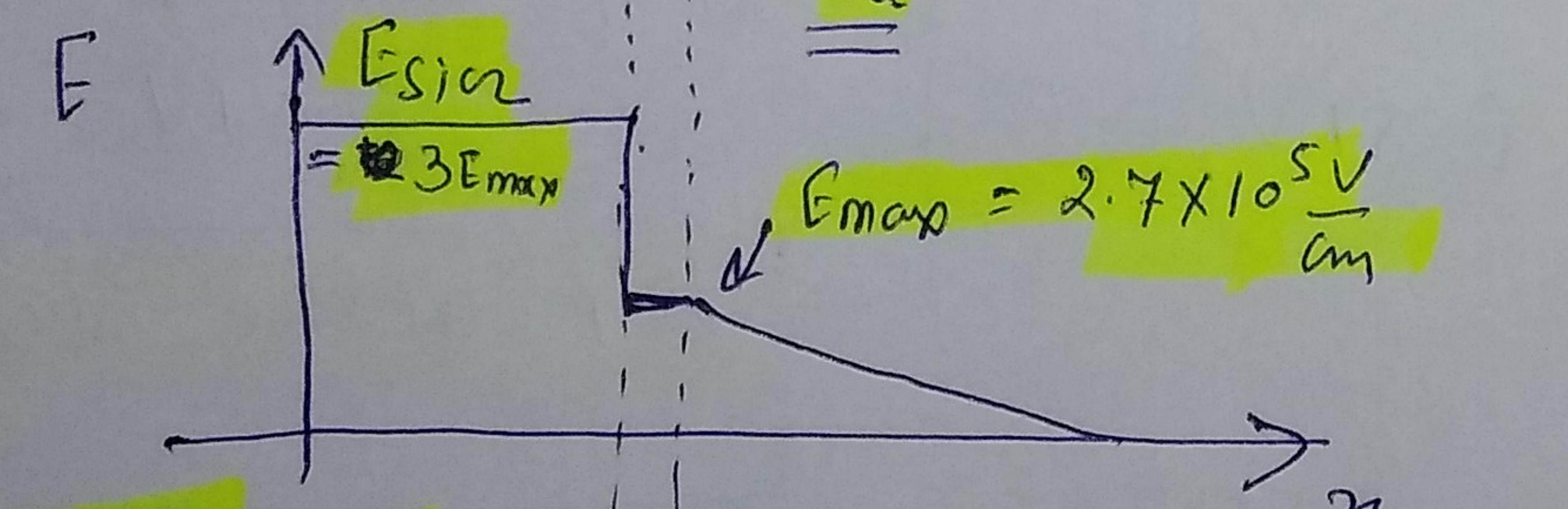
$$1.5 = 0.09 + 0.81 + \frac{Q_i}{C_{ox}}$$

$$Q_i = 0.6 \times C_{ox} = 0.6 \times \frac{E_{SiO_2}}{t_{ox}} = \frac{0.6 \times 12 \times 8.85 \times 10^{-14} \frac{F}{cm}}{10 \times 10^{-7} cm} = 6.3 \times 10^{-7} \frac{Col}{cm^2}$$

Profile -

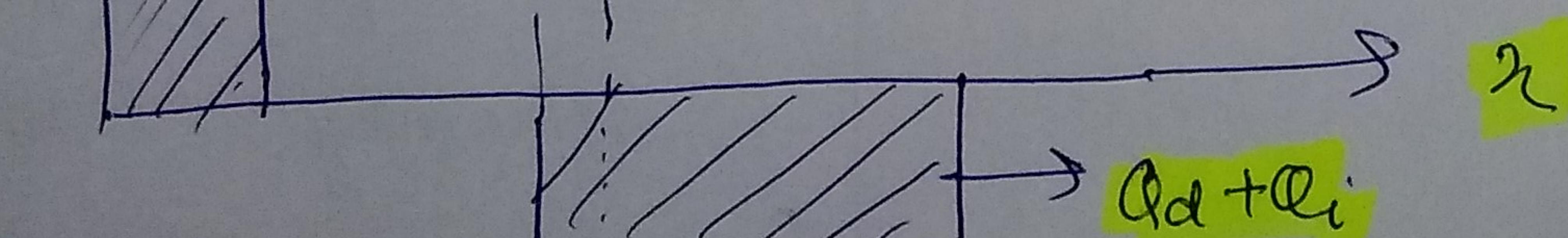


$$Q_i = 6.3 \times 10^{-17} \frac{Col}{cm^2}$$

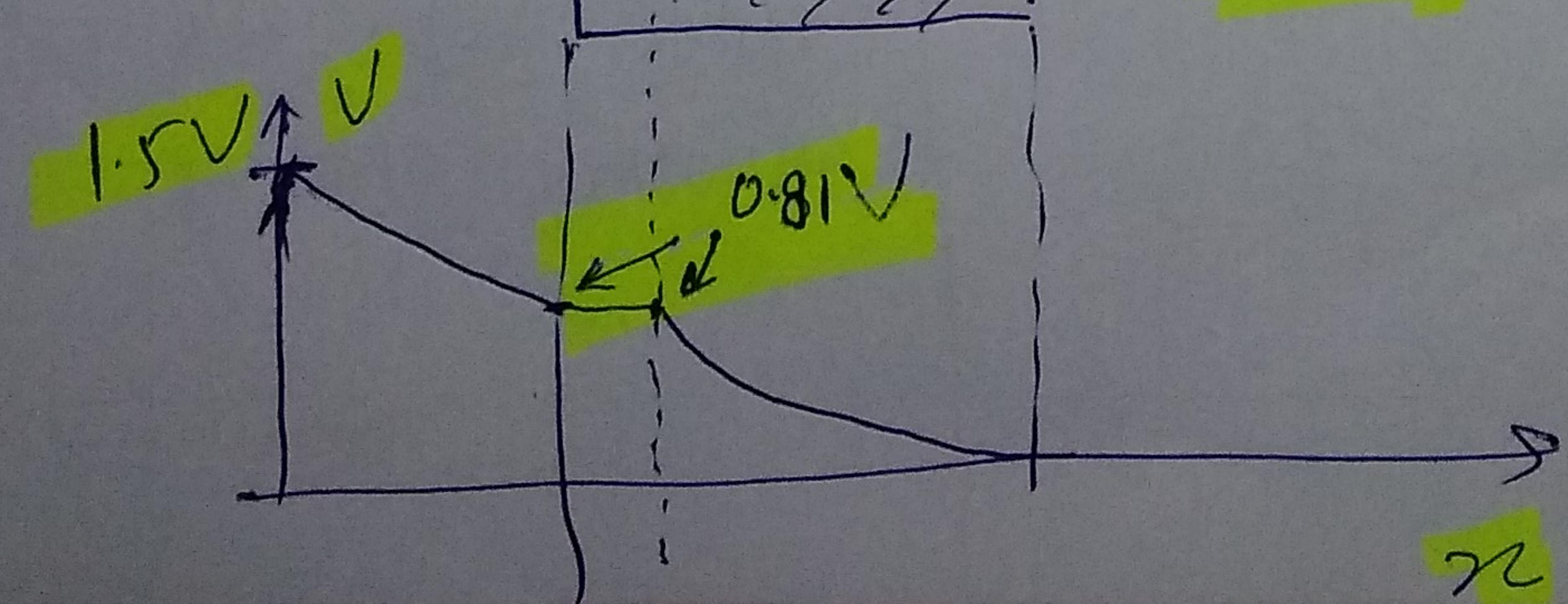


Electric field

Charge profile



Voltage drop



2. (a) For the circuit shown in Fig.1(a) (input is a square wave signal with amplitude = V_{DD} and time period = T), find the following:

- Power stored at V_{OUT} for output = '1'.
- Power dissipation by the circuit.
- Power dissipation by transistor M_1 and M_2 .

- (b) Implement the same logic with minimum transmission gates only, and calculate the power dissipation. [04+03]

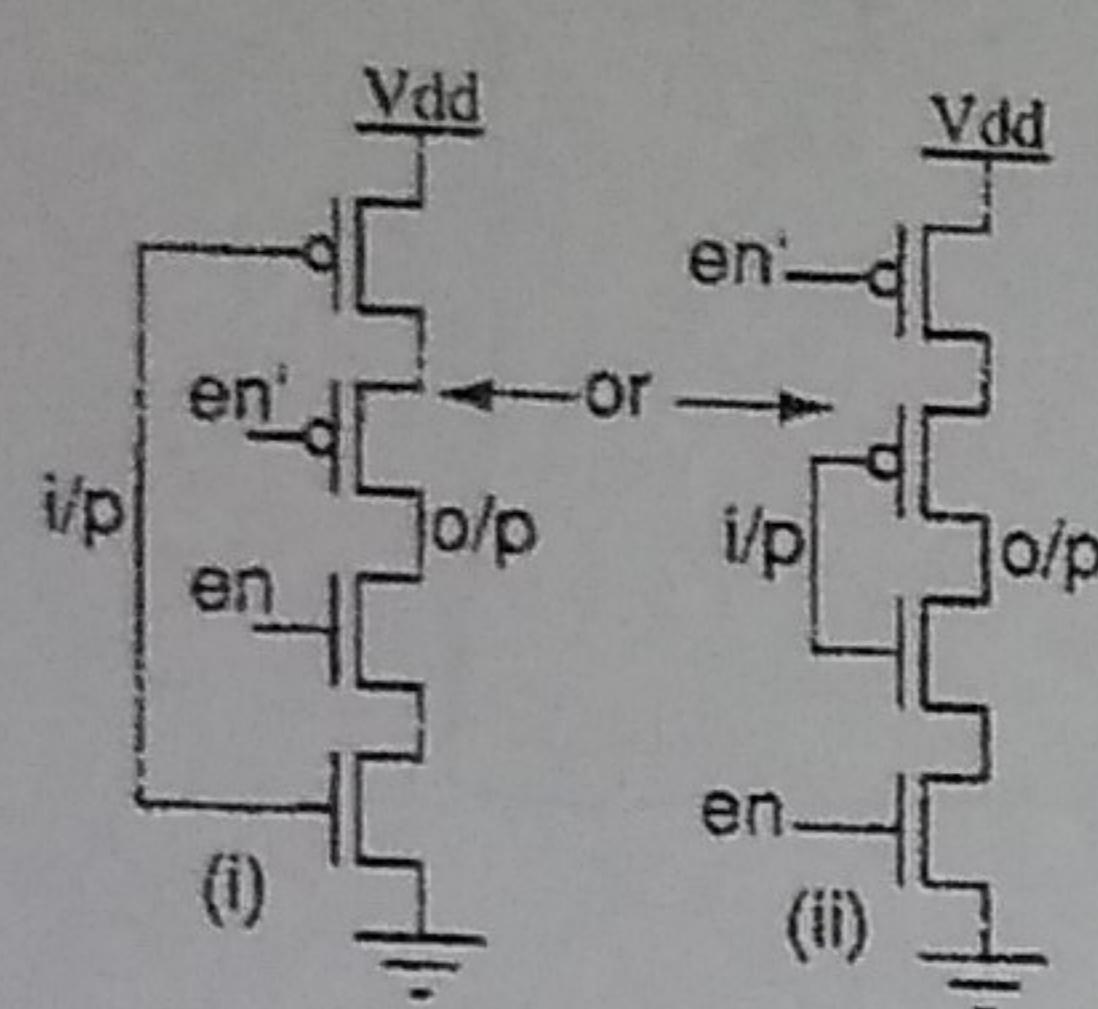
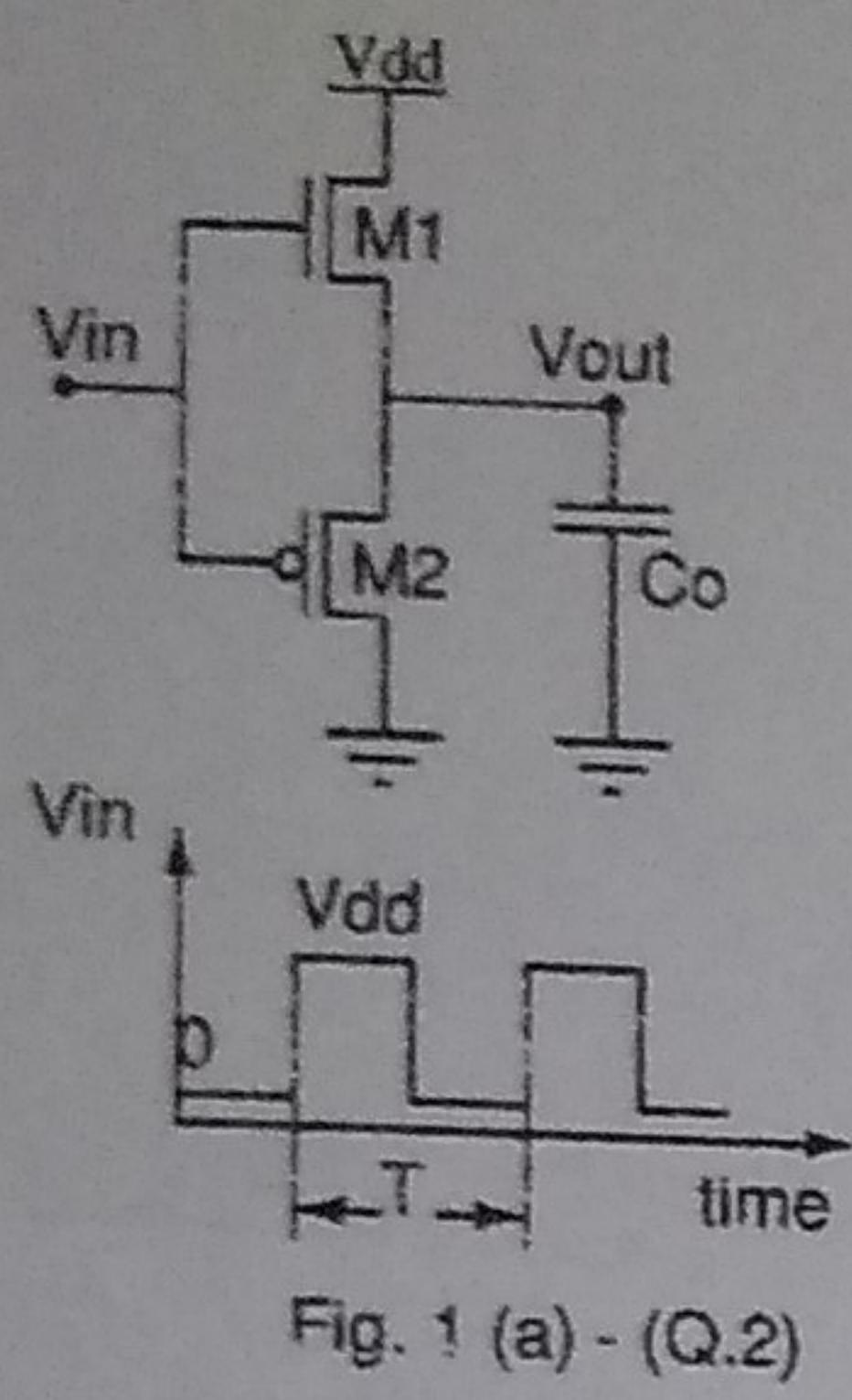
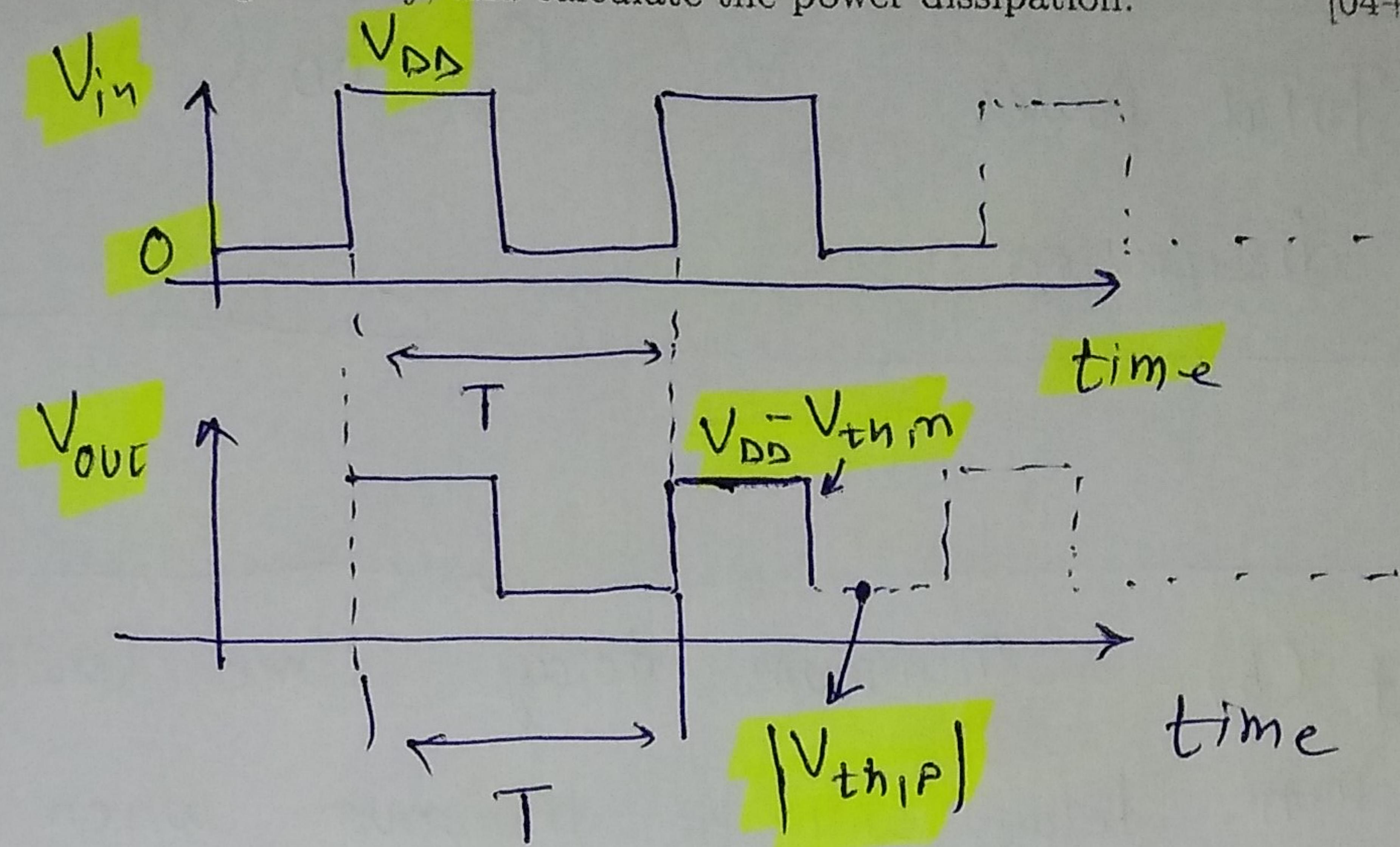


Fig. 1 (b) - (Q.3)



O/P Vol. will swing between $V_{DD} - V_{th,n}$ to $|V_{th,p}|$

ii) \rightarrow Power dissipation by $C_{kt} = \frac{1}{T} \int_{|V_{th,p}|}^{V_{DD} - V_{th,n}} C_0 V_{DD} \left(\frac{dV_{out}}{dt} \right) \cdot dt = \frac{1}{T} \int V_{DD} \cdot I \cdot dt$

if $V_{th,n} = |V_{th,p}| \Rightarrow$
then

$$= \frac{1}{T} C_0 V_{DD} (V_{DD} - 2V_{th})$$

$$= C_0 V_{DD} (V_{DD} - 2V_{th}) \cdot f$$

i) Power stored at V_{OUT} for O/P = '1' (logic '1')

$$= \frac{1}{2} \cdot C_0 V_{DD} (V_{DD} - 2V_{th}) \cdot f$$

iii) Power dissipation by transistor M_1 (during Charging)
(transition from '0' \rightarrow '1') $= \frac{1}{2} C_0 V_{DD} (V_{DD} - 2V_{th}) \cdot f$

Power dissipation by transistor M_2 during discharging =

④

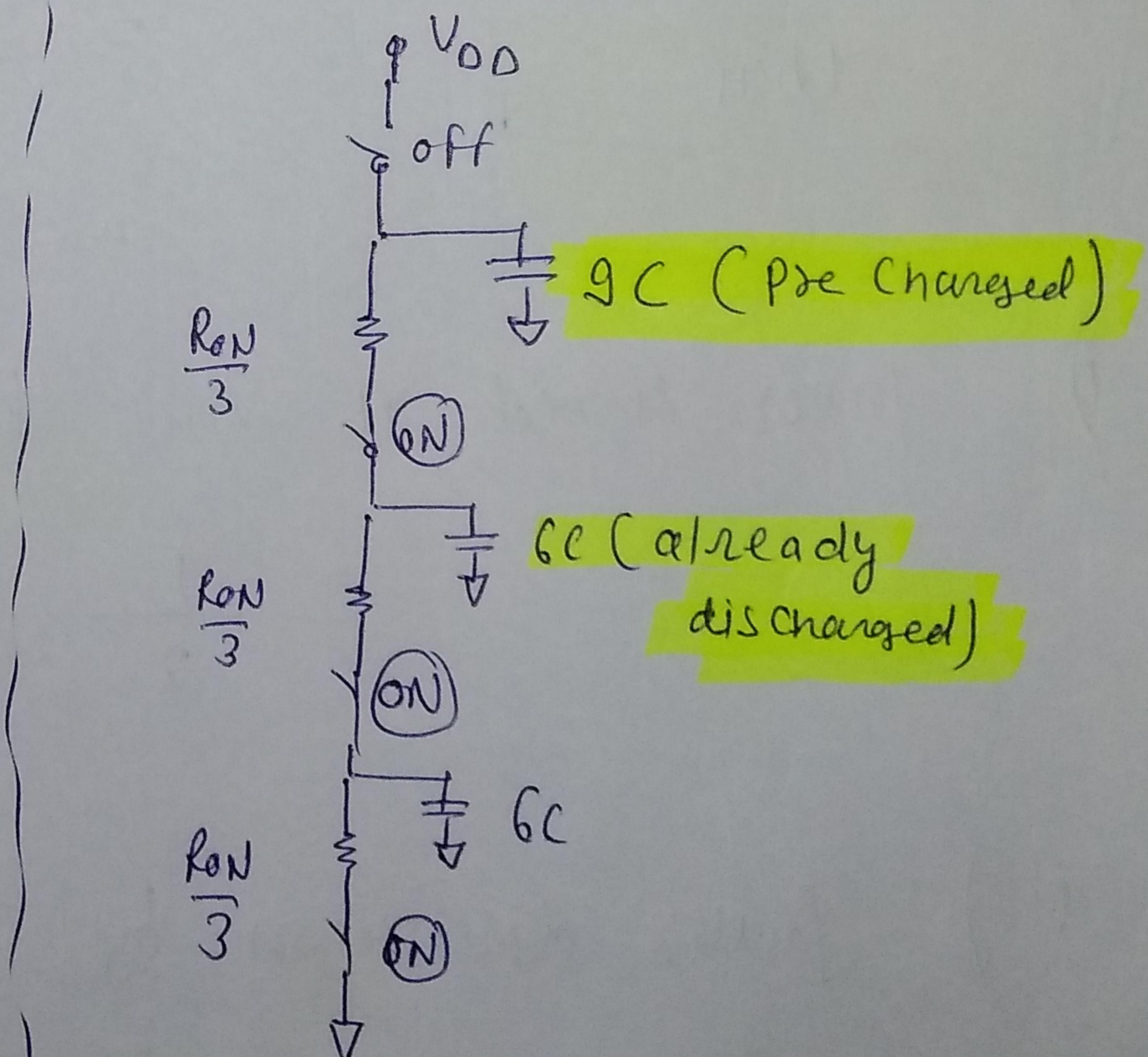
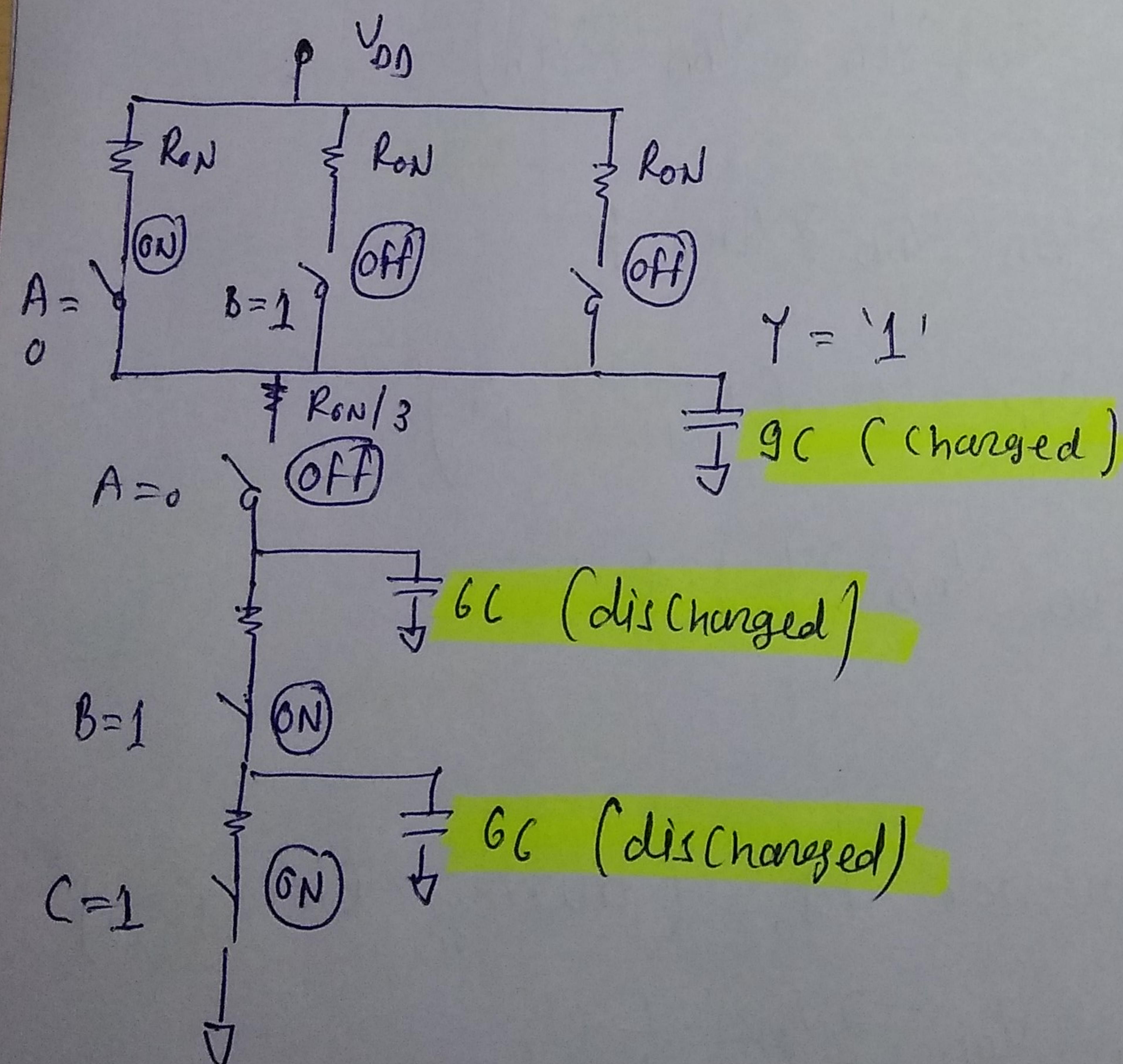
Thus Total power = Power dissipation by M₁
+ Power dissipation by M₂

$$\boxed{\text{Total power} = C_0 V_{DD} (V_{DD} - 2V_{th}) \cdot f}$$

Q. 4 (b) - Minimum delay time constant \rightarrow for o/p $\underline{1} \rightarrow \underline{0}$
 Primary delay will be minimum when intermediate capacitance with
 are already discharged.

Thus minimum delay case will be ~~A = 1~~ A = '0' \rightarrow '1'
 for I/Ps \rightarrow B = '1' \rightarrow '1'
 C = '1' \rightarrow '1'

for A = '0', B = '1' & C = '1'
 O/P = '1' \rightarrow A = '1', B = '1', C = '1'
 O/P \rightarrow '0'



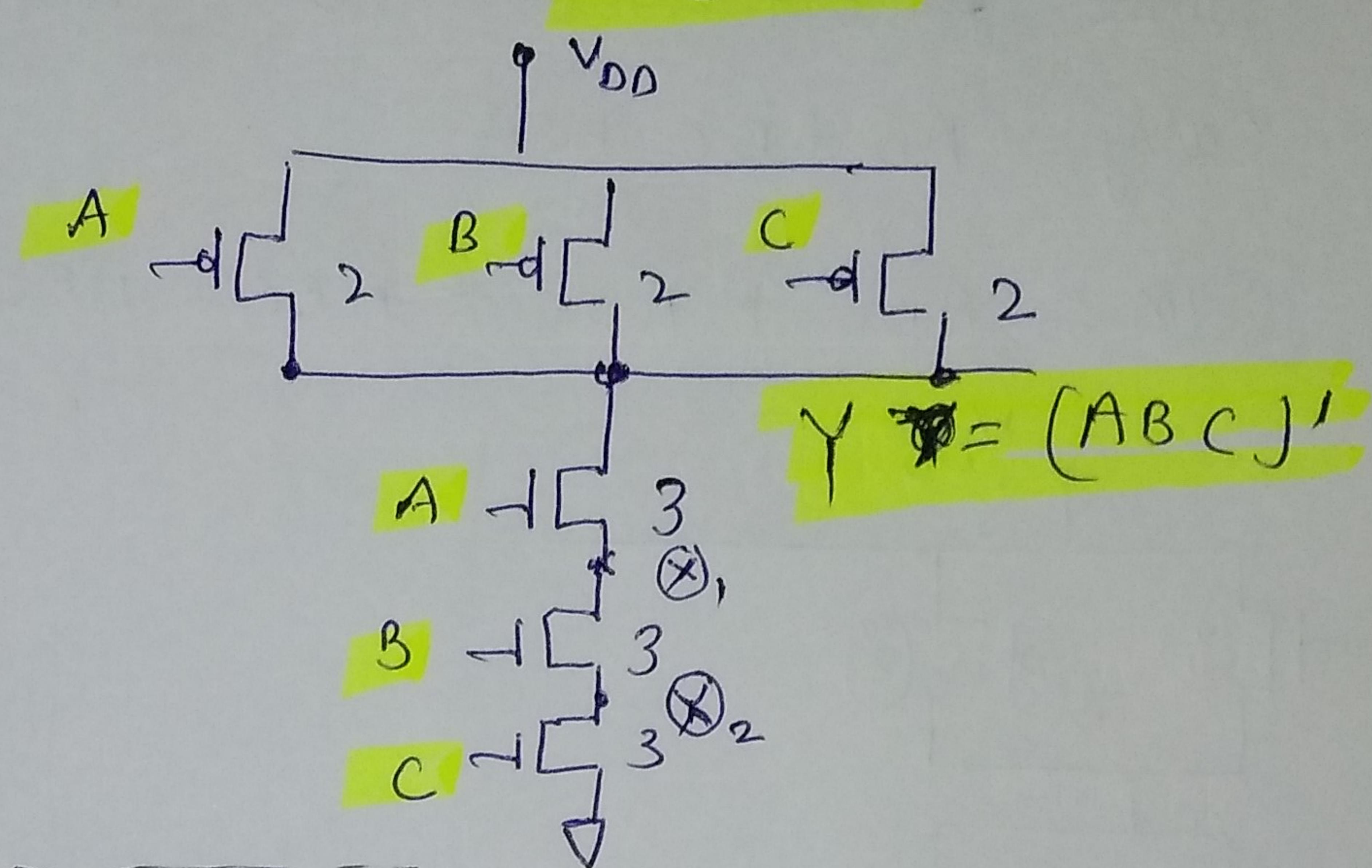
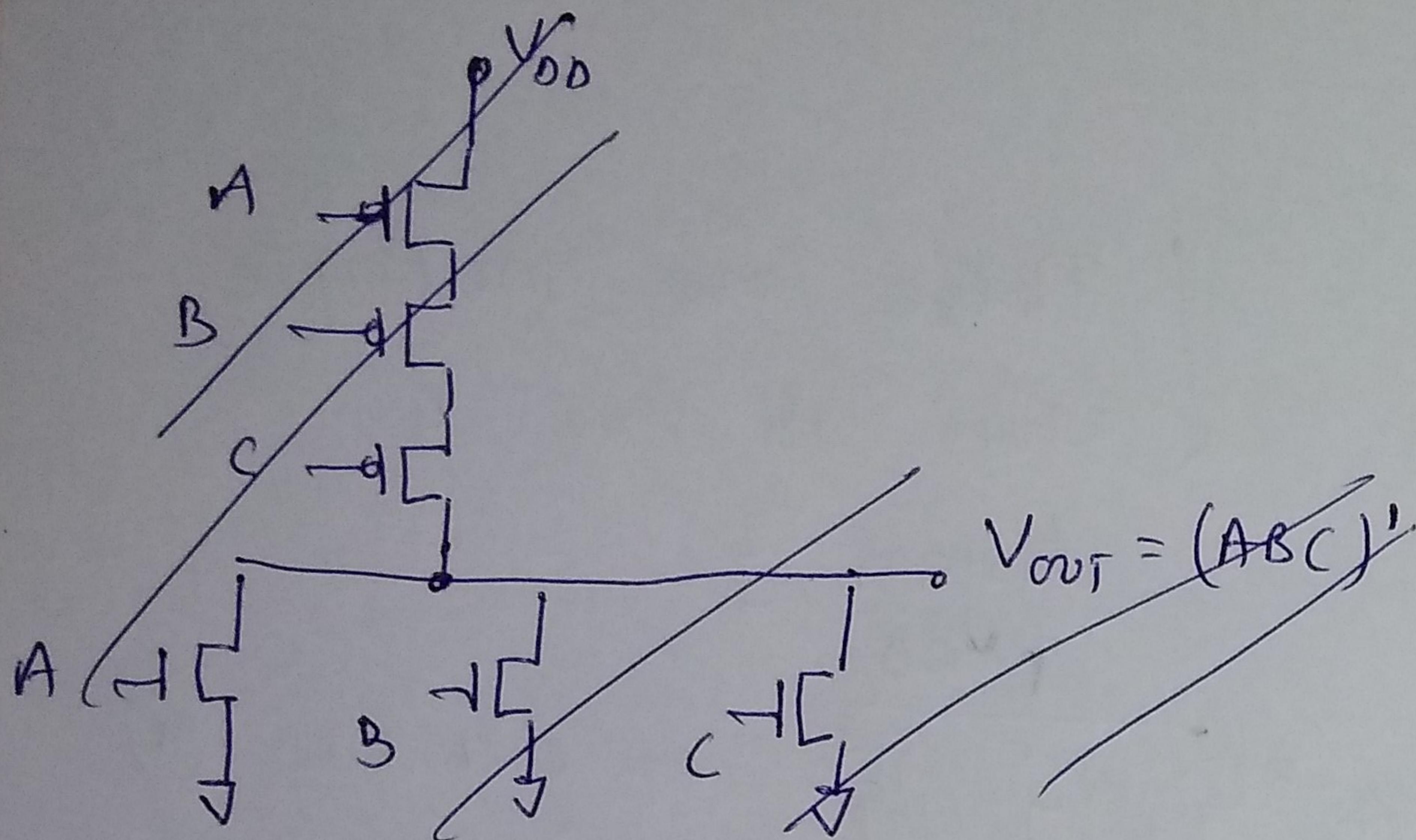
$$T_{1 \rightarrow 0}^{\min} = g_C \left(\frac{R_{on}}{3} + \frac{R_{on}}{3} + \frac{R_{on}}{3} \right)$$

$$= g R_{on} C$$

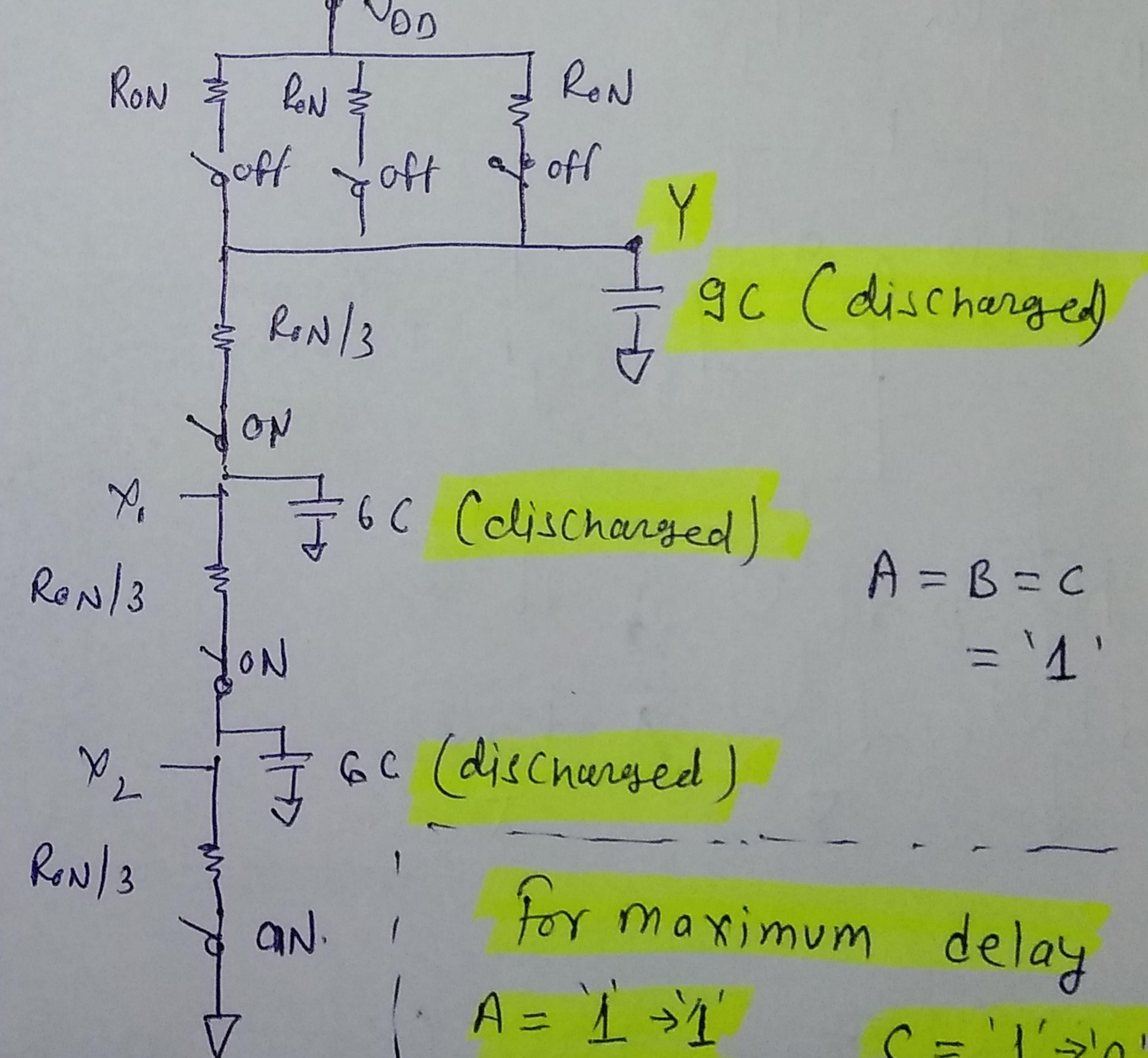
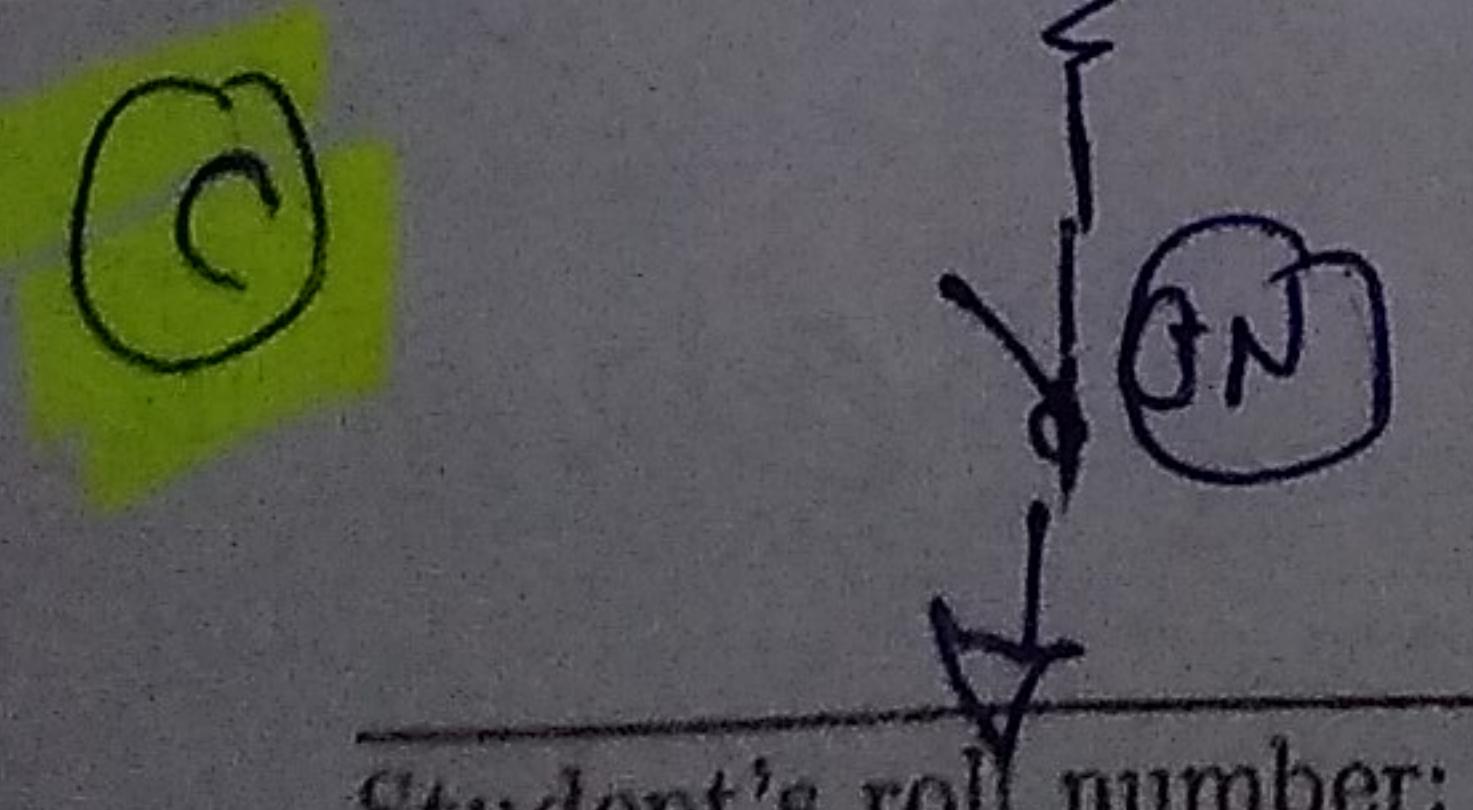
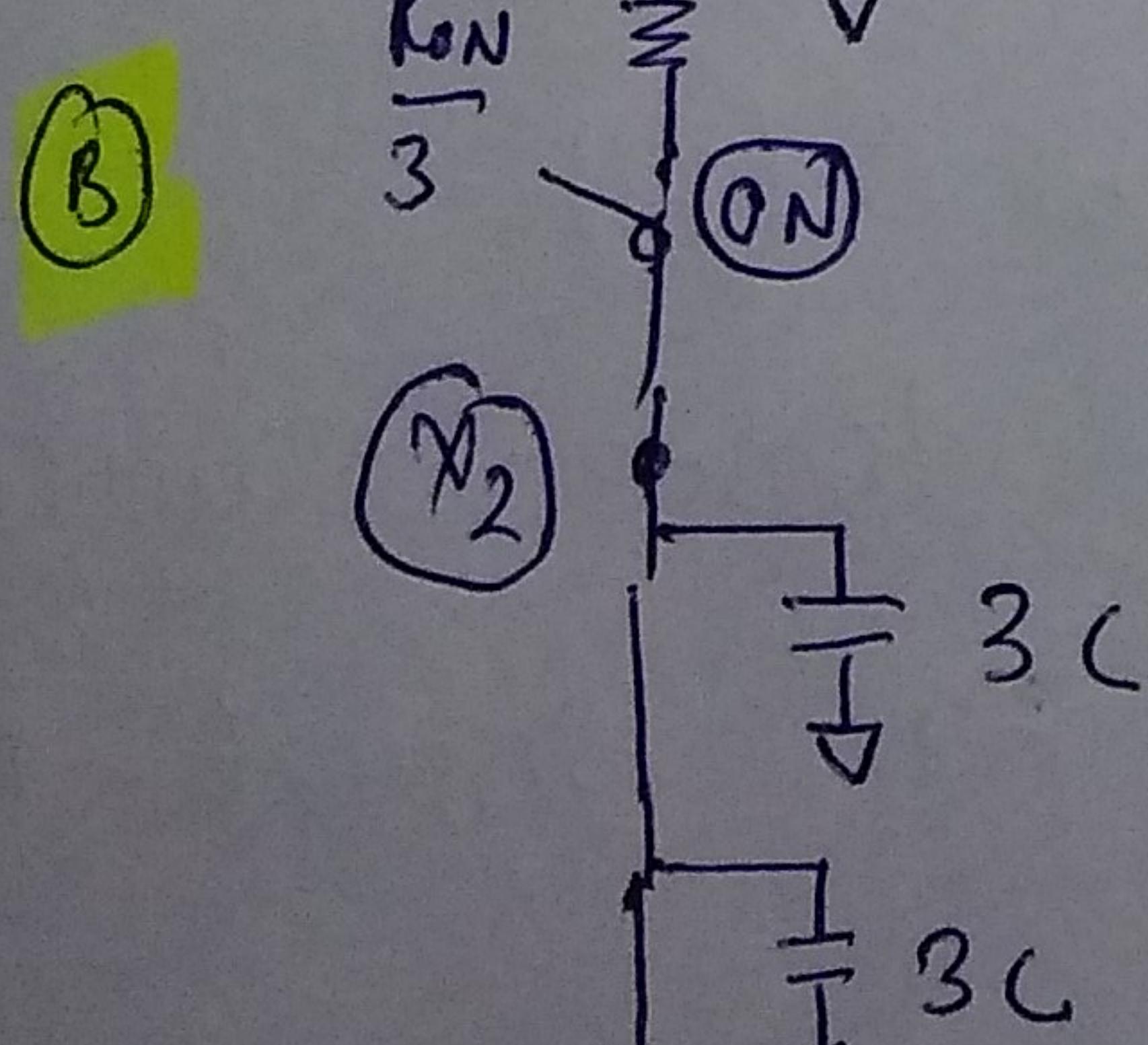
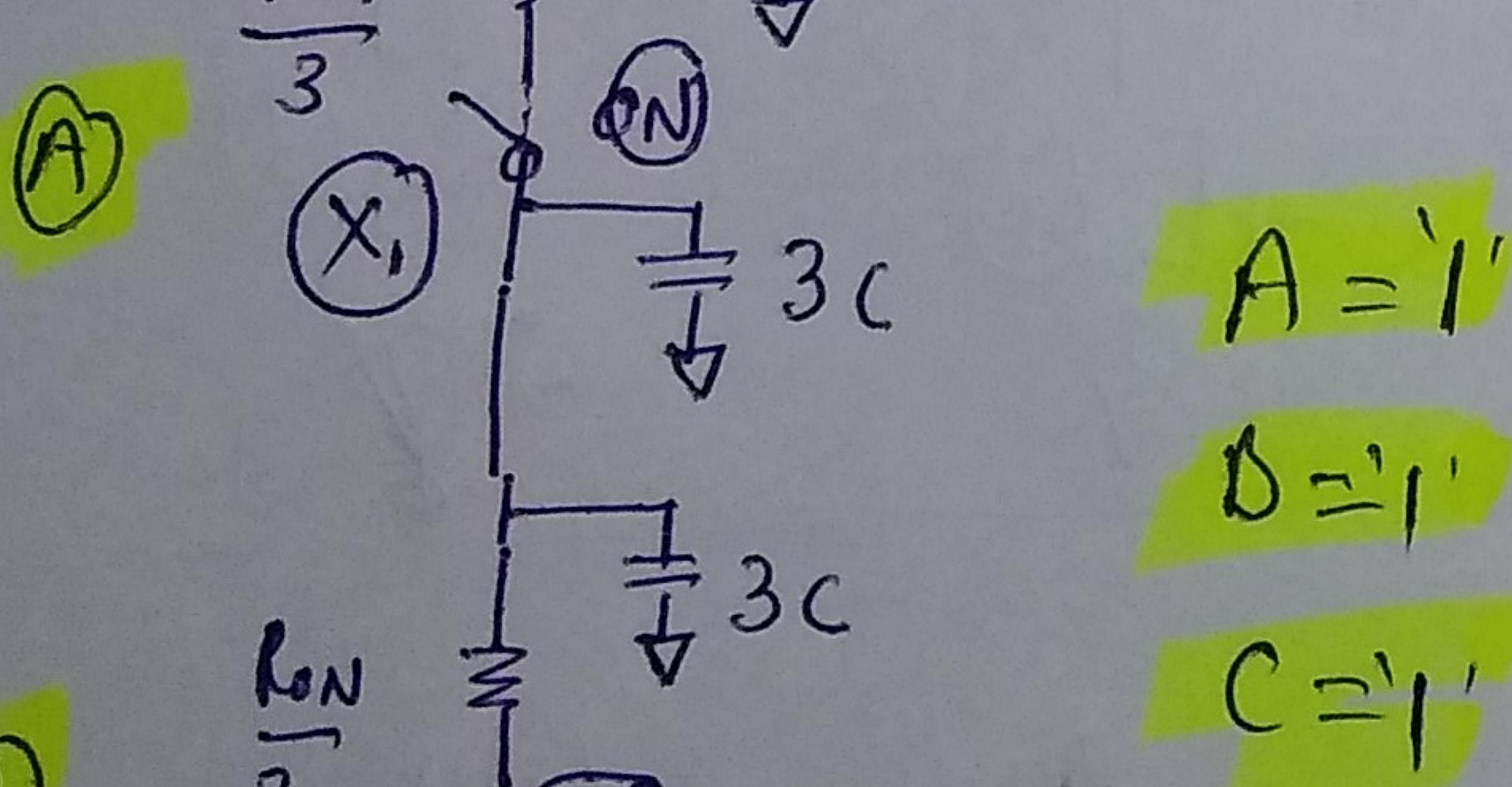
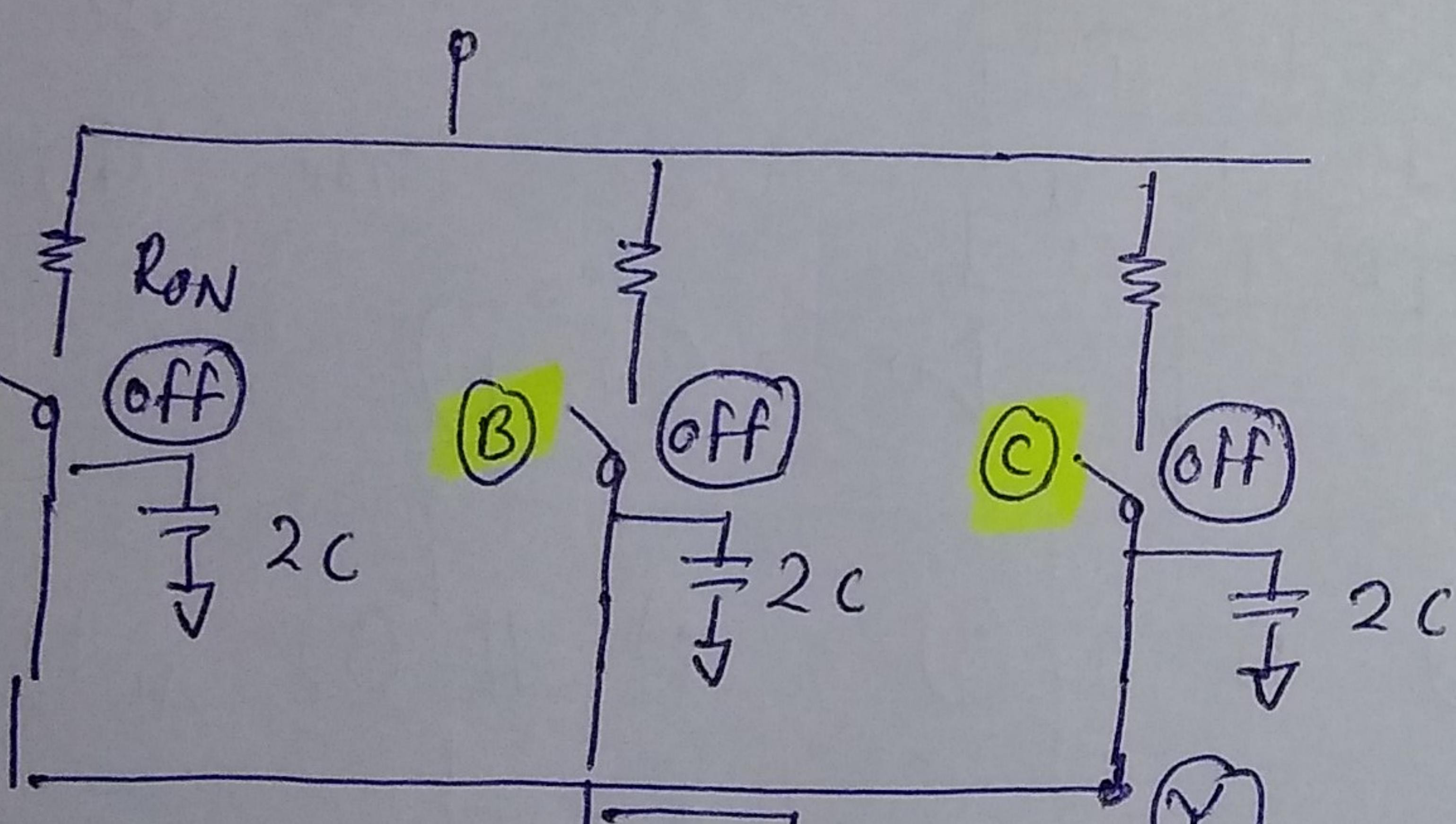
4. Implement the boolean expression $Y = A'B + B' + ABC'$ using static CMOS logic. Find the input values (including switching pattern) and RC time constants for output value transition from

- (a). Maximum delay for output value transition from '0' to '1'.
 (b). Minimum delay for output value transition from '1' to '0'.

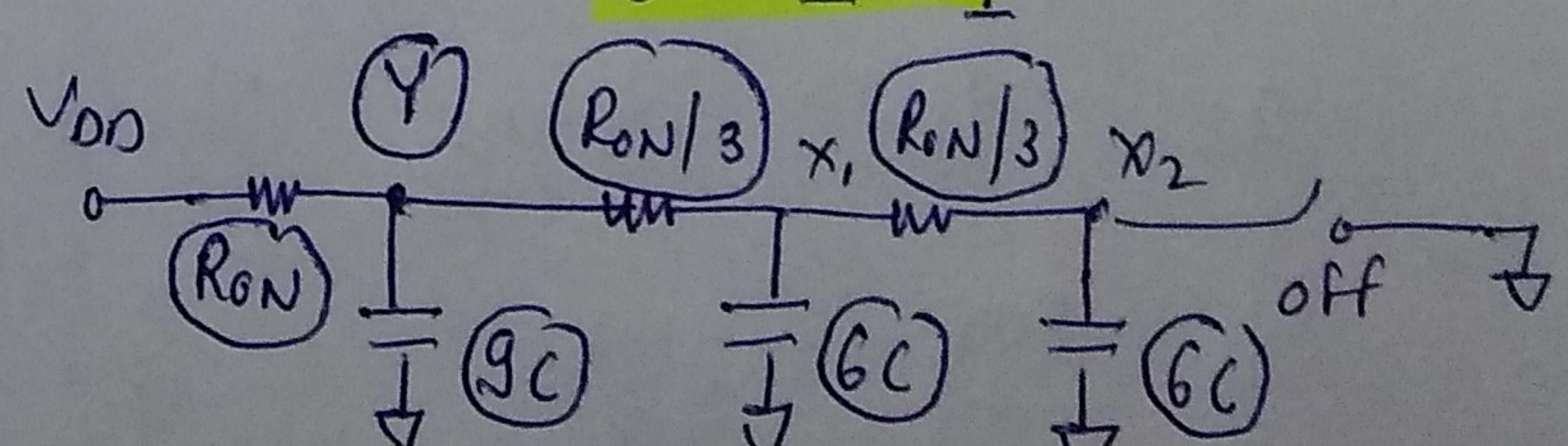
$$Y = A'B + B' + ABC' = A' + B' + ABC' = A' + B' + A' C' = A' + B' + C' = (ABC)'$$



(a) for previous condition of O/P = '0'



$$A = B = C = '1'$$



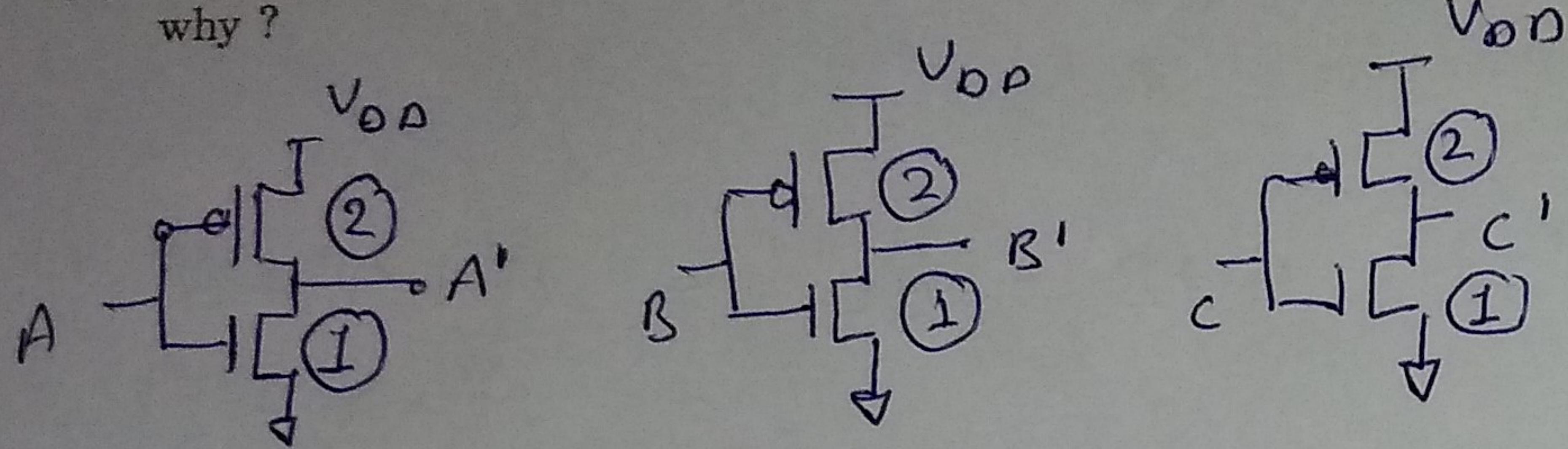
$$T_{0-1} = R_{ON} \cdot 9C + 6C \cdot R_{ON} + 6C \cdot R_{ON}$$

$$T_{0-1} = 21 R_{ON} \cdot C = \text{Max. delay}$$

(6)

3. (a). Implement a full adder circuit with static CMOS logic and size the transistors for equal rise and fall time.
 (b). Fig. 1(b) (i) and (ii) show two architecture to implement a same logic expression. Which design is better and why? [03+02]

(a) →

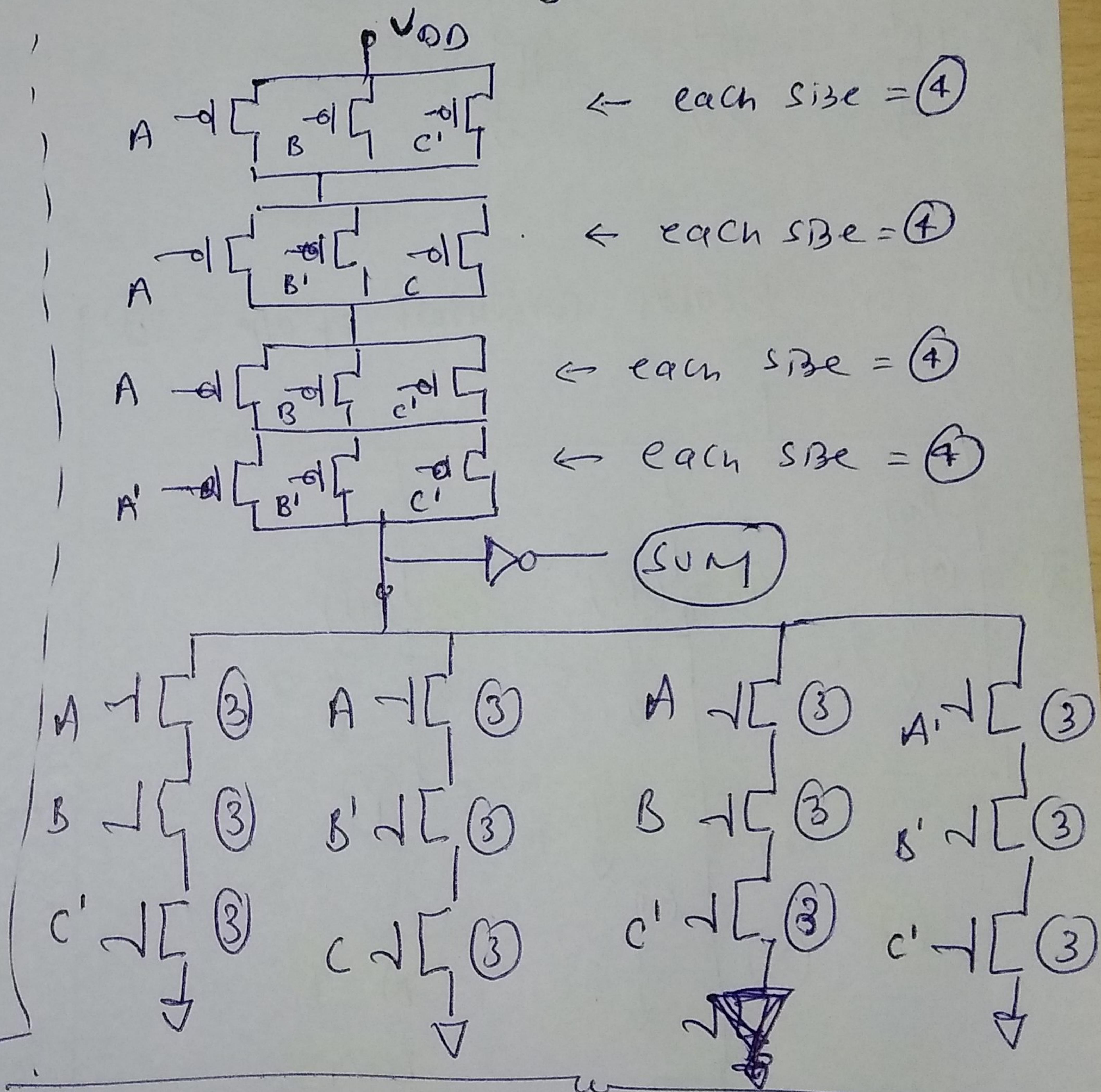
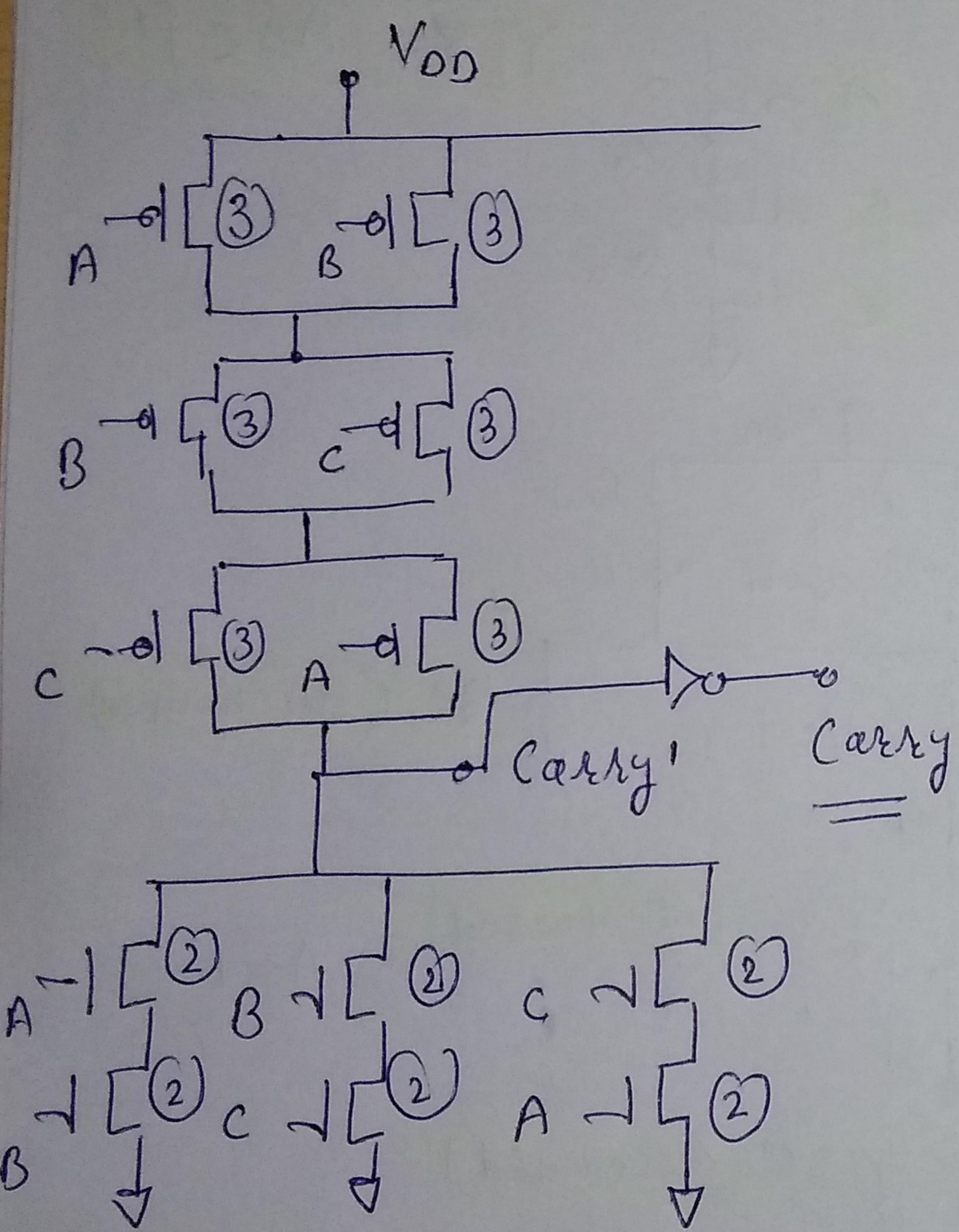


$$\text{Sum} = \cancel{ABC} + \cancel{A'B'C} + \cancel{A'BC'} + \cancel{AB'C'}$$

$$\text{Carry} = AB + BC + CA$$

$$\text{Sum} = ABC' + AB'C + A'BC + A'B'C'$$

There are multiple ways to size & design }



(b) →

Design 1(b) → (ii) is better than 1(b) → (i) as the delay would be lesser for lesser switching of EN signal, & in design (ii) EN signal is closer to VDD & GND which support the argument.

(You can do Calculation by own or refer the Class notes)

5. How does upper and lower noise margins depend (increase or decrease) on the sizing of the transistors in CMOS logic?
Prove your claim with logical reasoning and mathematical analysis. [04]

$$\text{Ans: for } \beta_p = l_{kp} C_{ox} \left(\frac{W}{L} \right)_p$$

$$\text{if } \beta_n = l_{kn} C_{ox} \left(\frac{W}{L} \right)_n$$

Switching Voltage of (inverter - taken as an example to prove)

$$\text{CMOS logic gate} = \frac{V_{DD} - |V_{th,p}| - V_{th,n} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = V_{sw}$$

$$\text{When } V_{DD} \left[|V_{th,p}| = V_{th,n} \right] \Rightarrow$$

$$V_{sw} = \frac{V_{DD}}{2}$$

the curve (i)

$$\Rightarrow \text{when } \beta_n > \beta_p$$

$$V_{sw} < \frac{V_{DD}}{2}$$

→ Curve will shift towards left which shows that lower NM_L decreases & upper noise margin $(NM)_H$ increases.

$$\rightarrow \text{when } \beta_p > \beta_n \Rightarrow V_{sw} > \frac{V_{DD}}{2}$$

then curve (VTC) will shift towards right & thus lower noise margin NM_L increases & upper noise margin $(NM)_H$ decreases.

