LNMIIT
The LNM Institute of Information Technology

The LNM Institute of Information Technology, Jaipur
CSE222: Operating Systems
2021-22 Even semester
Mid Term Exam

Max Marks: 50 **Date: 27th September 2022** **Time: 90 Mins**

Instruction: All the questions are compulsory.
No doubts will be entertained during the exam.
Please make appropriate assumptions if you find any question has any data missing.

Total Questions	Total Marks	CO1	CO2	CO3	CO4	CO5	CO6
10	50	Q5-5, Q7-5	Q4-5, Q8-5, Q9-5	Q1-2, Q2-10	Q3-3, Q6-5, Q10-5		---
CO weightage		**10/50 = 20%**	**15/50 = 30%**	**12/50=24%**	**13/50=26%**		

Section – 1

Q1. Assume the content of Accumulator and Register-B are 03H and 09H respectively. After the SUB B command what will be the contents of Accumulator and different flag bits? **[2 Marks]**

Q2. Briefly explain the following commands and determine the size of each instruction in bytes:

a) DAD B **[2 Marks]**

b) LDAX B **[2 Marks]**

c) STA 9500H **[2 Marks]**

d) JP **[2 Marks]**

e) CNZ **[2 Marks]**

Q3. Briefly explain two important differences between memory mapped IO and peripheral mapped IO techniques. **[3 Marks]**

Section – 2

Q4. What are the different addressing modes available with microprocessor 8085? Along with two instructions of each mode, briefly explain how these instructions are identified in these modes. **[5 Marks]**

Q5. Design a memory mapped IO system, using partial decoding technique, to access 4096 registers in a memory chip using microprocessor 8085. Explain your system and justify the choice of address lines in detail. Draw a neat diagram of your system. **[5 Marks]**

Q6. Design a system to integrate a tri-state buffer (to connect 8 switches) and a latch (to connect 8 LEDs) with microprocessor 8085. Use absolute addressing scheme and memory mapped IO technique to design the system. Draw a neat diagram to represent your design along with the addresses to access the tri-state buffer and LEDs. **[5 Marks]**

Q7. Neatly draw the timing diagram for 8085 microprocessor performing writing operation. Assume the data being written is 3EH at memory address 8085H. Show states of address bus

and data bus, ALE, $IO/\overline{M}$, and $\overline{WR}$ lines at different clock intervals. **[5 Marks]**

Q8. Assume contents of registers A = 08H and B = 03H are to be subtracted. Explain in steps the complete procedure of subtraction performed in microprocessor 8085 for two different cases as given below. **[5 Marks]**

a) **A – B**
b) **B – A**

Q9. Assume a 2MHz crystal oscillator is connected to microprocessor 8085. Explain the program given below and show the steps to calculate the time taken to complete the program. **[5 Marks]**

```
        LXI B, 0010H
Loop:   DCX B
        MOV A, C
        ORA B
        JNZ Loop
        HLT
```

Q10. For the schematic shown in **Figure 1**, determine all possible ranges of addresses and the size of each register in the register bank. **[5 Marks]**

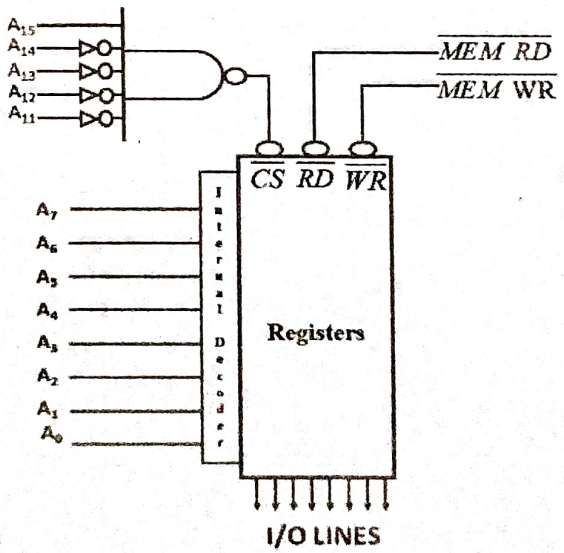

Figure 1