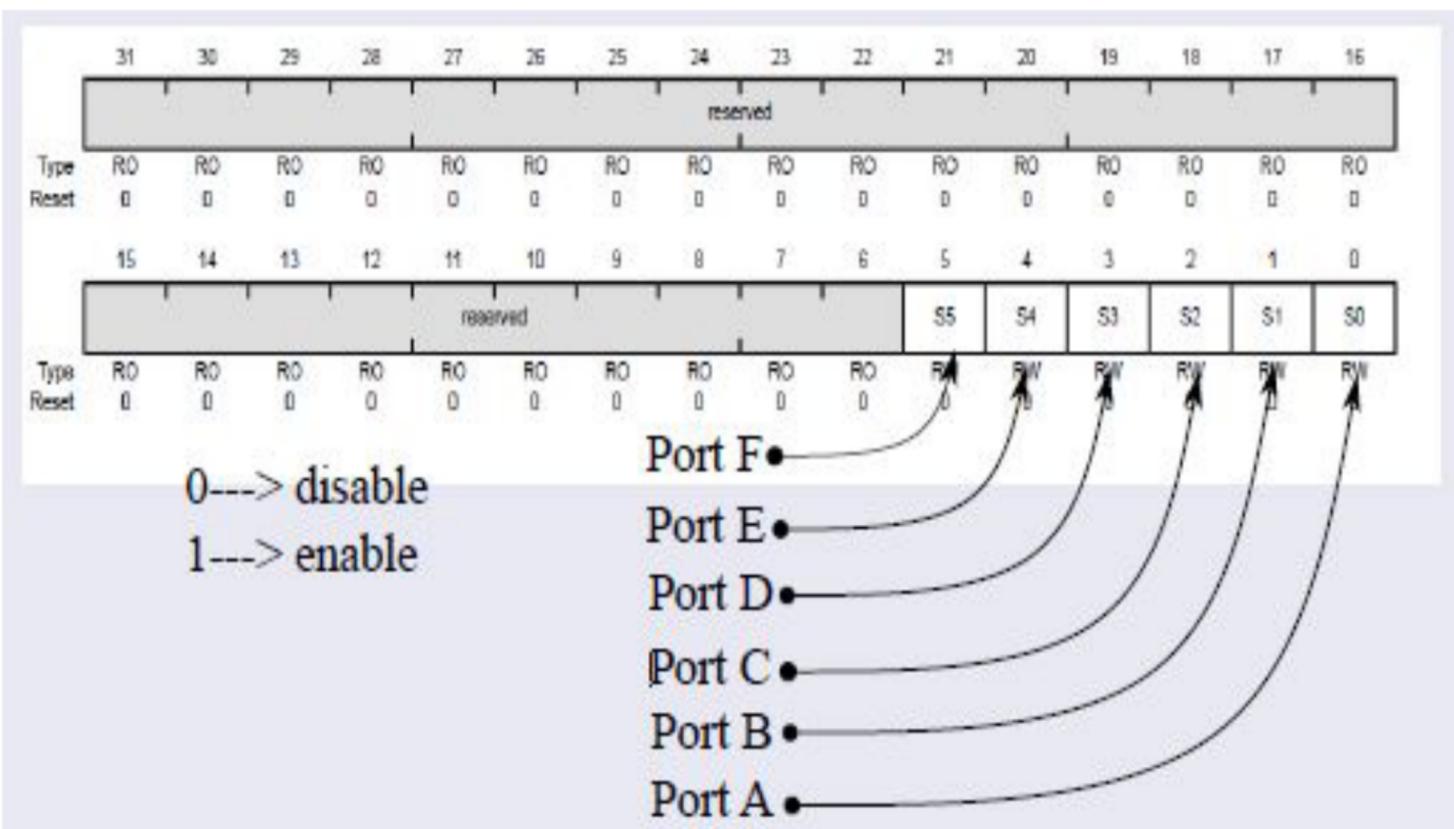


Practice 1

LAB Practice on GPIO Port

Clock Gating Register



Before and After Setting Clock Gating Register

Symbolic Memory					Symbolic Memory				
Location	Data	Variable	Value	Type	Location	Data	Variable	Value	Type
0x400FE5FC	0x00000000				0x400FE5FC	0x00000000			
0x400FE600	0x00000000				0x400FE600	0x00000000			
0x400FE604	0x00000000				0x400FE604	0x00000000			
0x400FE608	0x00000000				0x400FE608	0x00000020			
0x400FE60C	0x00000000				0x400FE60C	0x00000000			
0x400FE610	0x00000000				0x400FE610	0x00000000			
0x400FE614	0x00000001				0x400FE614	0x00000001			

Memory 1									
Go to	0x40025000	Memory	▼	▼	▲	▲	▼	▼	▲
0x40024f90	-----								
0x40024fa0	-----								
0x40024fb0	-----								
0x40024fc0	-----								
0x40024fd0	-----								
0x40024fe0	-----								
0x40024ff0	-----								
0x40025000	-----	-----	-----	-----					
0x40025010	-----								
0x40025020	-----								

Memory 1									
Go to	0x40025000	Memory	▼	▼	▲	▲	▼	▼	▲
0x40024f90	-----								
0x40024fa0	-----								
0x40024fb0	-----								
0x40024fc0	-----								
0x40024fd0	-----								
0x40024fe0	-----								
0x40024ff0	-----								
0x40025000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000					
0x40025010	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000					
0x40025020	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000					

Direction Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
reserved															
Type	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved															
Type	RO	RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0---> Corresponding pin input

1---> Corresponding pin output

0:7 Bits

GPIO Direction (GPIODIR)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
Offset 0x400
Type RW, reset 0x0000.0000

Digital Function Register

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
reserved																
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																
Type	RO	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DIR																

0---> Disable Digital function
1---> Enable Digital function

0:7 Bits

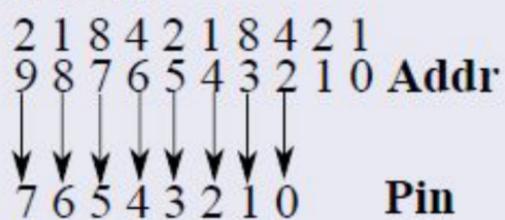
GPIO Digital Enable (GPIODEN)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
Offset 0x51C
Type RW, reset -

Port Data Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
reserved															
Type	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved															
Type	RO	RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0:7 Bits

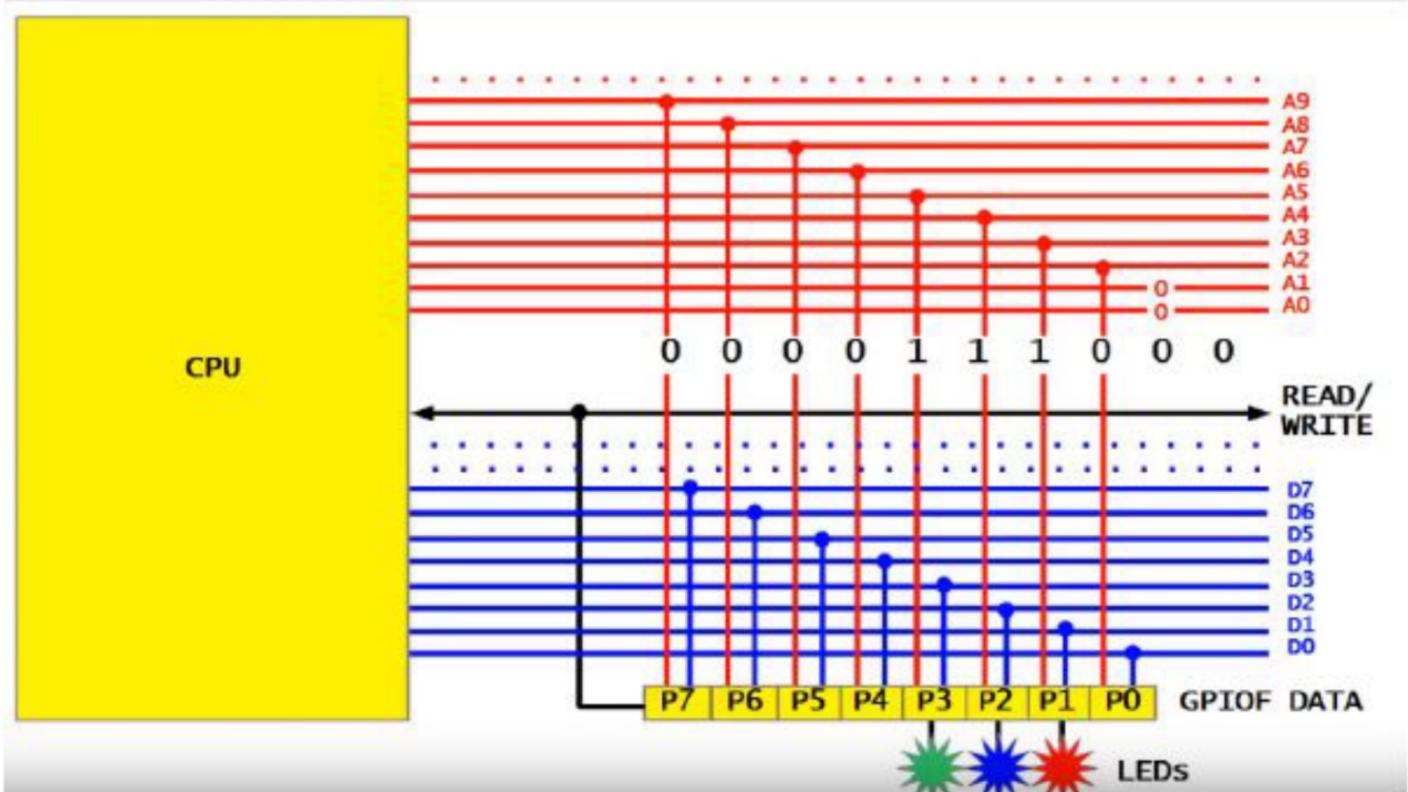


All seven port if want to use
3FC
0x400253FC

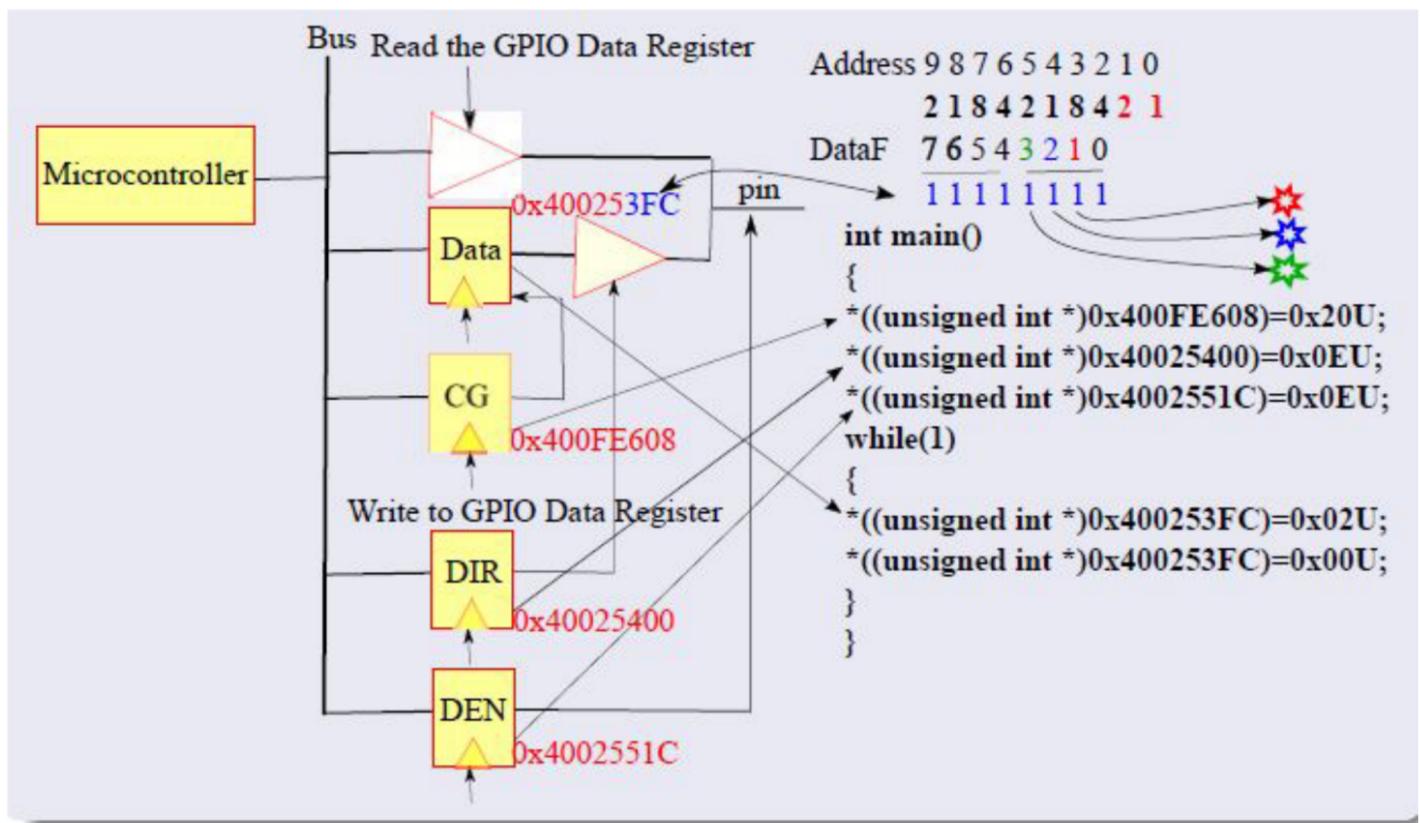
GPIO Data (GPIODATA)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
Offset 0x000
Type RW, reset 0x0000.0000

Addressing Each Bit in Data Register



Final Program with RTL Logic



Practice Problem for Todays Lab

- Write a register level program to calculate each bit address of Port F Data register, where the red, green, blue LEDs are connected. Also light each led with different delay 1 sec, 2sec, 3 sec.

How many cycle do we need to create the delay of 1 sec, 2 sec, and 3 sec. Read the datasheet and identify the clock frequency on the GPIO port.

Upload your practice in Google drive:

https://drive.google.com/drive/folders/17qQZcQr8cAZn7apGTpx_QNbn-r6AkzoO?usp=sharing