Paolo Baesso

Proto DUNE board: pc053a.

6th January 2017

Board pc053a.

Paolo Baesso - 2016
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Contents

SFP: optical serial interface.
MASTER: RJ45 interface. Can do serial and parallel.
SLAVE: RJ45 interface. Can only do parallel.

Chapter 1

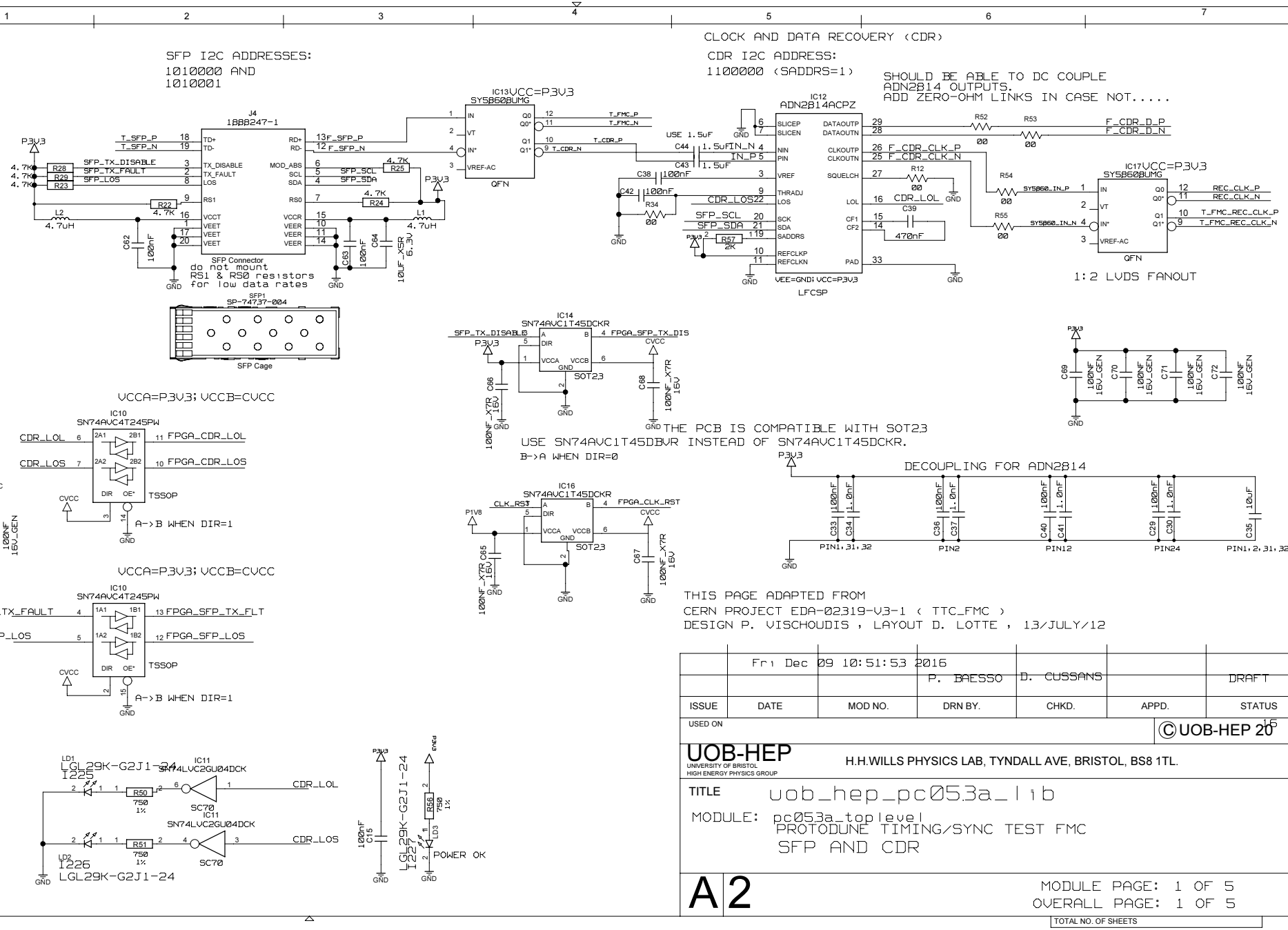
I^{2}C interface

The boards has three independent Inter-Integrated Circuit (I^{2}C) buses, working on separated lines: one bus is connected to the dedicated pins on the Field Programmable Gate Array (FPGA) connector, one is connected to the clock generator and the third one is connected to theSmall Form-factor Pluggable (SFP) transceiver.
The naming used for the I^{2}C buses and the corresponding devices connected are shown in table 1.1

Table 1.1: I^{2}C buses and connected devices.

Component	**Part number**	**Bus**	**FMC pin**	**Note**	**Address**
J4	1888247-1	SFP_SCL SFP_SDA	FMC_LA07_P FMC_LA07_N	SFP transceiver	–
IC12	ADN2B14ACPZ	"		Clock/data recovery	0xC0
IC15	PCA9517DGKR	"		Level translator	–
IC1	PCA9306DCU	CLK_SCL CLK_SDA	FMC_LA11_P FMC_LA11_N	Level translator	–
IC4	SI5344B	"		Clock generator	0x68
IC2	24AA025E48T	FMC_SCL FMC_SDA	C30 C31	EEPROM	0x21

1.1 Schematic



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TITLE uob_hep_pc053a_lib

MODULE: pc053a_toplevel
PROTODUNE TIMING/SYNC TEST FMC
SFP AND CDR

A2

MODULE PAGE: 1 OF 5
OVERALL PAGE: 1 OF 5

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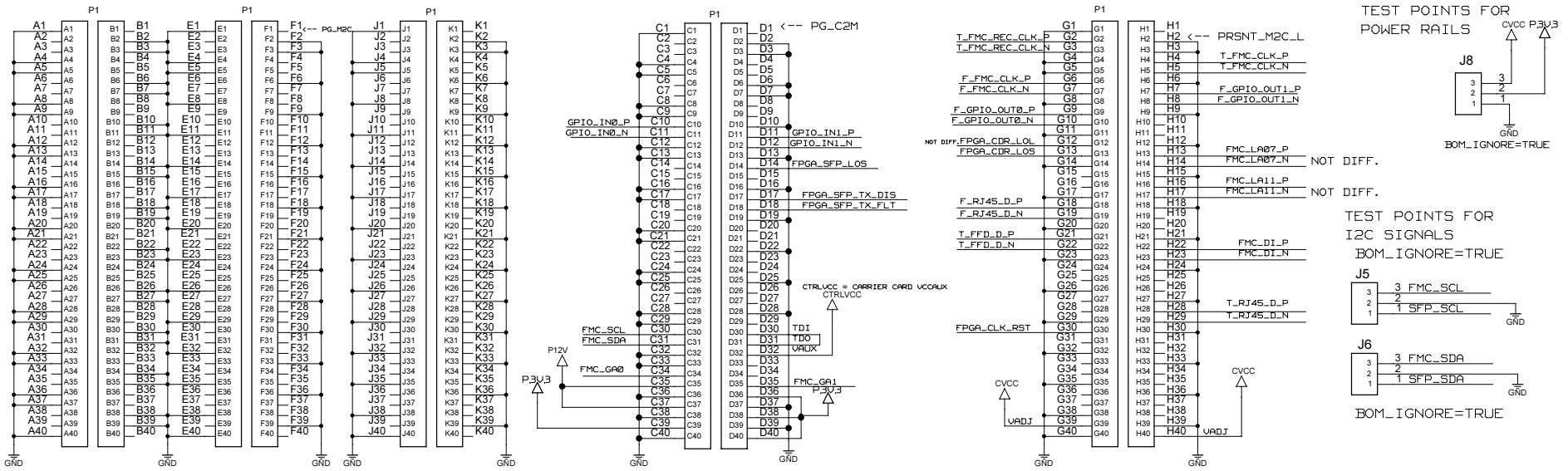


TEST POINTS FOR POWER RAILS

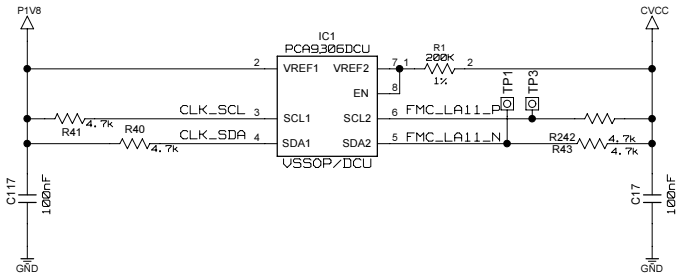
TEST POINTS FOR I2C SIGNALS

BOM_IGNORE=TRUE

BOM_IGNORE=TRUE

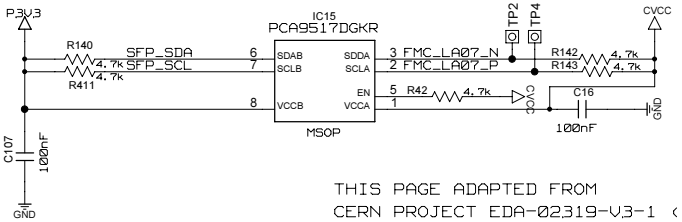
FOR P1 USE SAMTEC MC-LPC-10 OR MC-HPC-10

WHEN USING PCA9306, CVCC MUST BE AT LEAST 1.8V + 0.6V = 2.4V



USE TCA9517DGK INSTEAD

EN PIN INTERNALLY PULLED-UP



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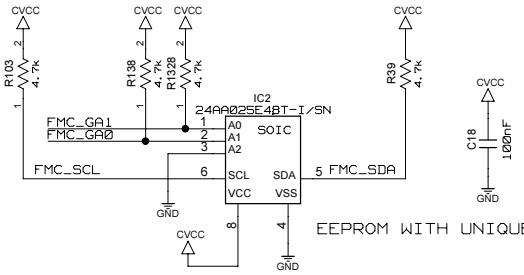
DESIGN P. VISCHOUDIS , LAYOUT D. LOTTE , 13/JULY/12



EEPROM WITH UNIQUE ID

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TITLE uob_hep_pc053a_lib

MODULE: pc053a_toplevel

PROTODUNE TIMING/SYNC TEST FMC
FMC CONNECTOR , EEPROM/UNIQUE-ID

A2

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TOTAL NO. OF SHEETS

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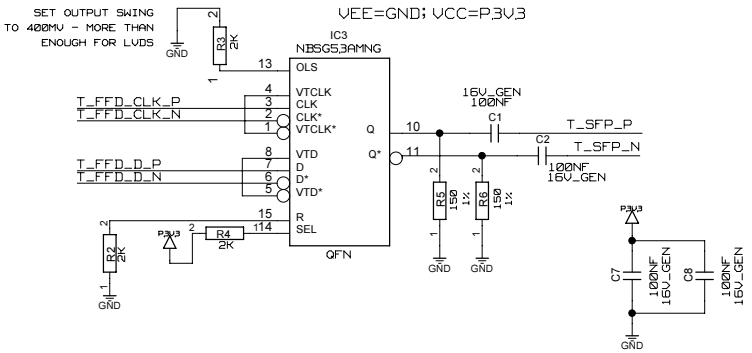
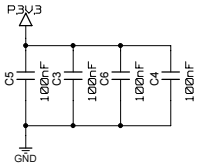
(TO REDUCE JITTER ON ENCODED DATA)





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TITLE uob_hep_pc053a_lib

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PROTODUNE TIMING/SYNC TEST FMC
D-TYPE REGISTER

A2

MODULE PAGE: 3 OF 5
OVERALL PAGE: 3 OF 5

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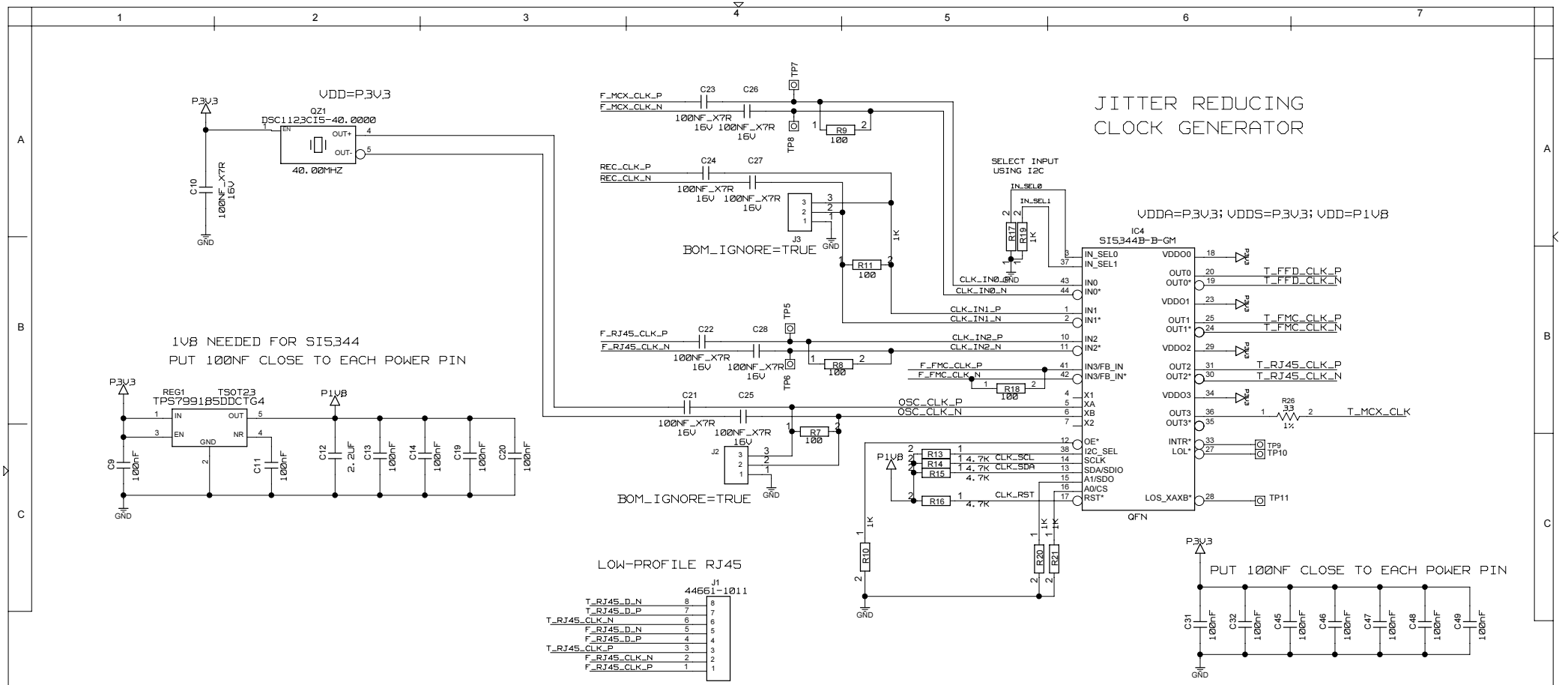

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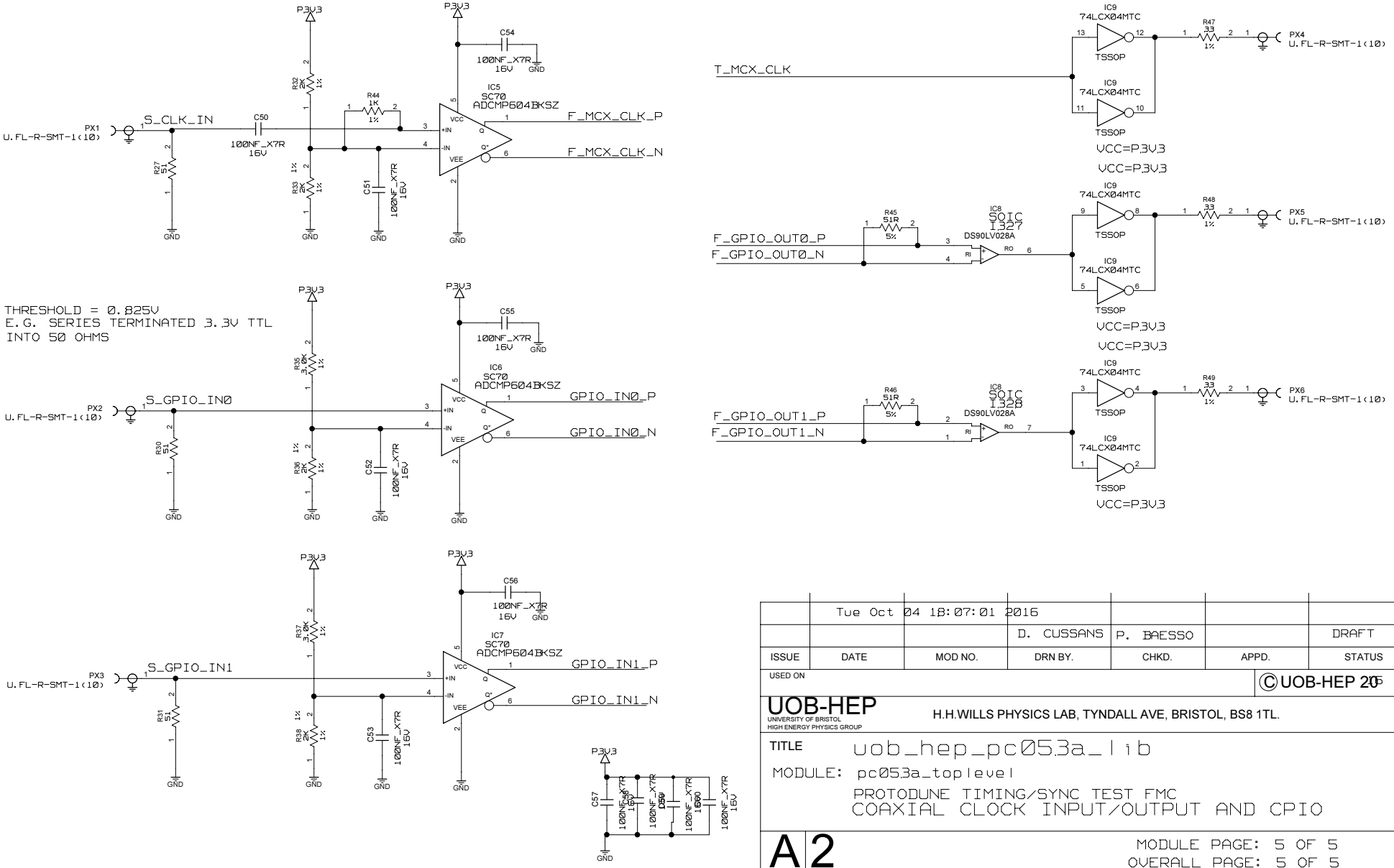
MODULE: pc053a_toplevel

PROTODUNE TIMING/SYNC TEST FMC
CLOCK GENERATOR , RJ45 CONNECTORS

A2



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PROTODUNE TIMING/SYNC TEST FMC
COAXIAL CLOCK INPUT/OUTPUT AND CPIO

A2

MODULE PAGE: 5 OF 5
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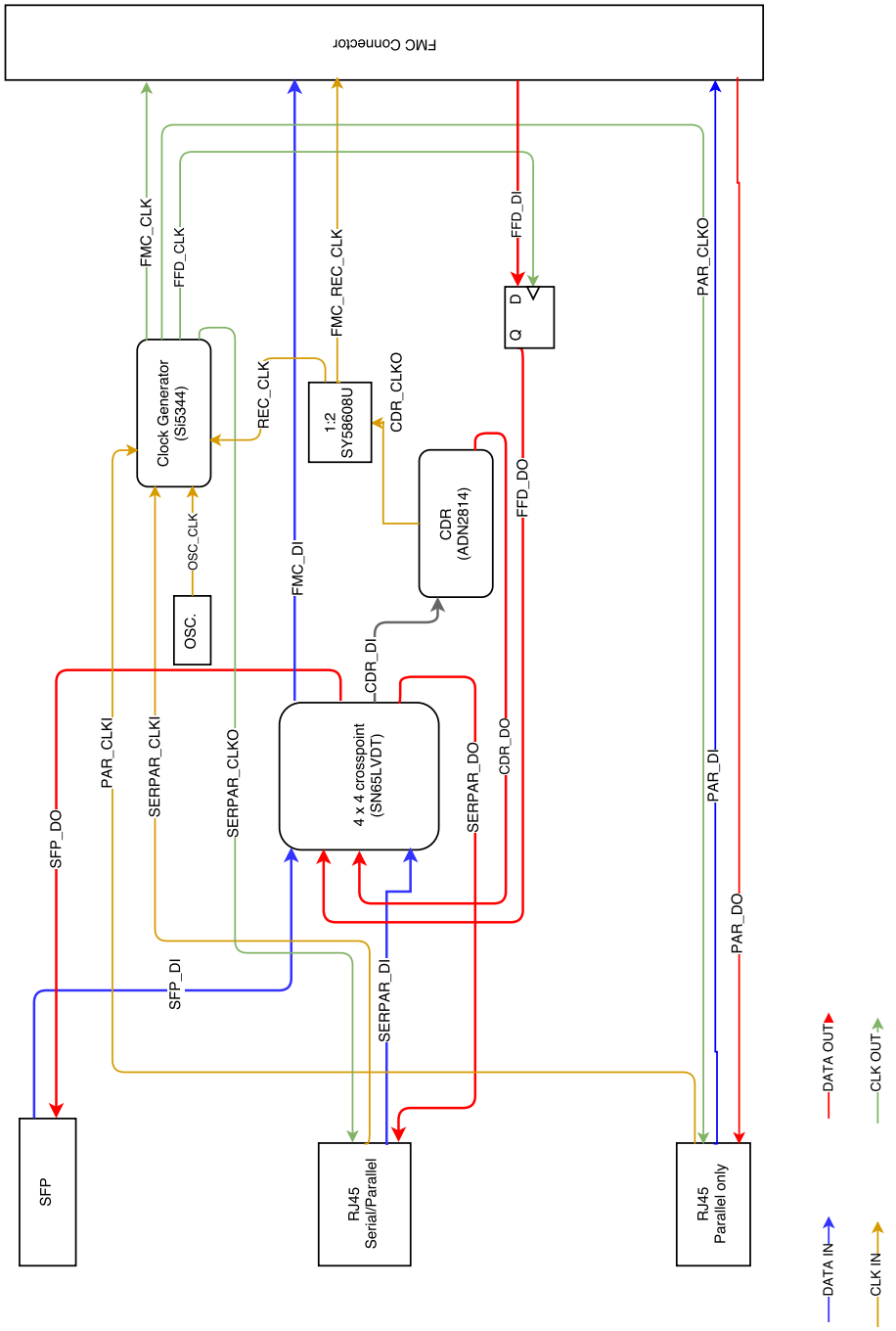

Figure 1.1: Sketch of the connections and signal names between the elements of the board.