YAMAHA LSI

V9958
MSX-VIDEO
TECHNICAL DATA BOOK

YAMAHA

V9958TECHNICAL DATA BOOK
CATALOG No.:249958Y
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This booklet describes those specifications which have been added, modified or deleted on the basis of specifications of V9938. The ones not found here have remained the same as V9938 but note that some, even the same, may be included here due to the conveniance of editing. For specifications of V9938, refer to “V9938 MSX-VIDEO Technical Data Book”.

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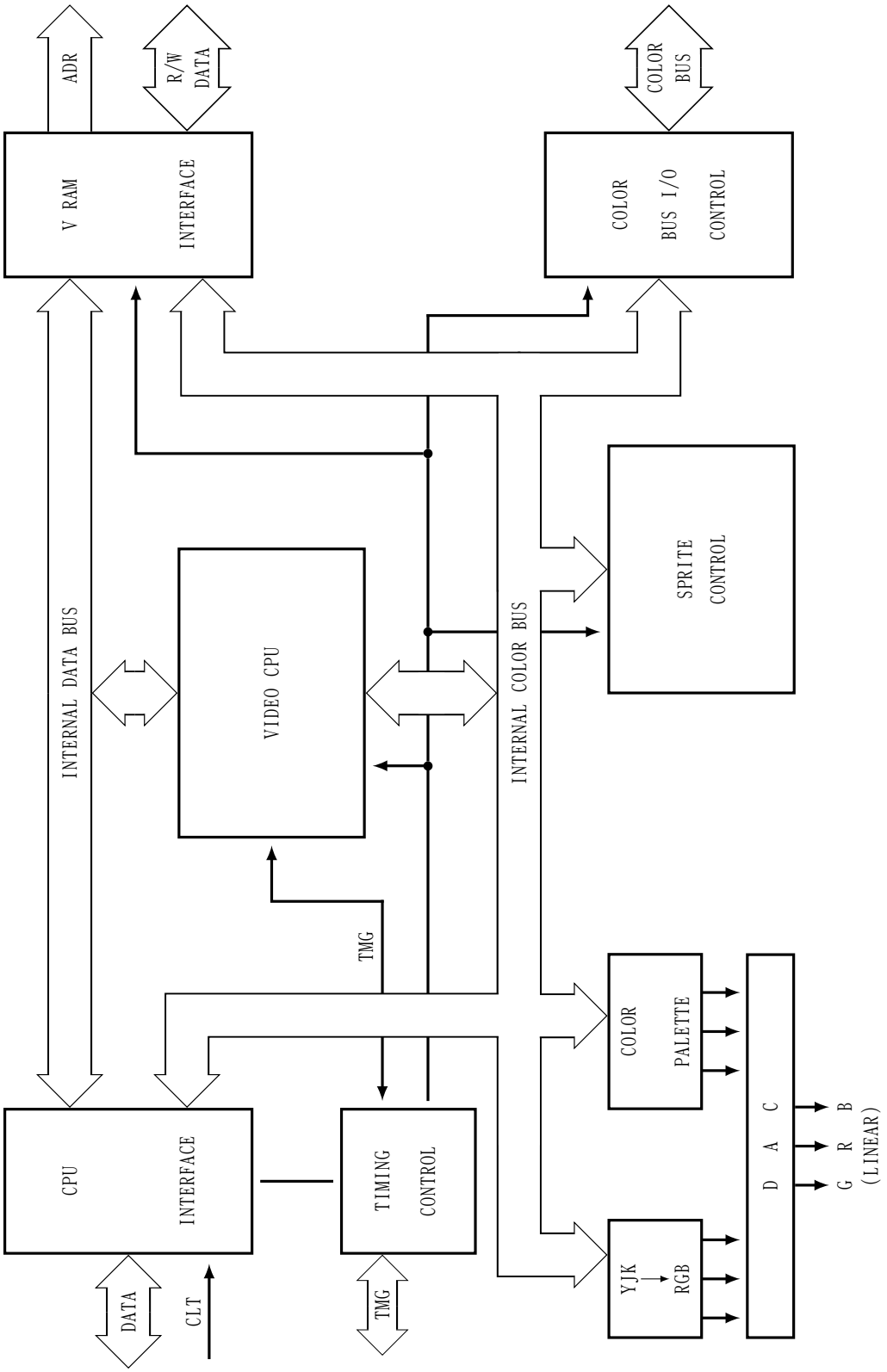
1 GENERAL DESCRIPTION

This LSI is a video display Processor(VDP) which is applicable to new media. It uses an N-channel silicon gate MOS and has a linear RGB output. It is software compatible with TMS9918A and V9938.

2 FEATURES

・5V power supply.
・Outputs linear RGB.
・Built-in color palette for display in up to 512 colors.
・Capable of simultaneous display of 19,268 colors by using YJK system. display.
・Capable of displaying up to 512×424 Pixels and 16 colors.
・Bit mapped graphics.
・Capable of displaying maximum of 256 colors simultaneously.
・16K byte～128K byte useable for display memory.
・16K×1b,16K×4b,64K×1b and 64K×4b DRAMs are useable.
・256 addresses,4ms auto refresh function of DRAM.
・Expansion video memory can be connected.
・Eight sprites can be displayed for each horizontal line.
・Colors for sprites can be specified for each horizontal line.
・Area move, line, search and other commands.
・Command function usable in every display mode.
・Logical operation function.
・Addresses can be specified by coordinates.
・Capable of external synchronization.
・Capable of superimposition.
・Capable of digitization.
・Multi MSX-VIDEO configurations are possible.
・External color palettes can be added by utilizing color bus output.
・Vertical and horizontal scroll function.
・Wait function to CPU.

3 INTERNAL STRUCTURE BLOCK DIAGRAM



4 PIN LAYOUT AND FUNCTIONS

Pin Name	Pin No.	I/O	Function
CD0 LSB	40	I/O	CPU data bus
CD1	39	I/O	”
CD2	38	I/O	”
CD3	37	I/O	”
CD4	36	I/O	”
CD5	35	I/O	”
CD6	34	I/O	”
CD7 MSB	32	I/O	”
MODE 0	29	I	CPU interface mode select
MODE 1	28	I	”
$\overline{CSR}$	31	I	CPU-MSX-VIDEO read strobe
$\overline{CSW}$	30	I	CPU-MSX-VIDEO write strobe
RD0 LSB	41	I/O	VRAM data bus
RD1	42	I/O	”
RD2	43	I/O	”
RD3	44	I/O	”
RD4	45	I/O	”
RD5	46	I/O	”
RD6	47	I/O	”
RD7 MSB	48	I/O	”
AD0 LSB	49	O	VRAM address bus
AD1	50	O	”
AD2	51	O	”
AD3	52	O	”
AD4	53	O	”
AD5	54	O	”
AD6	55	O	”
AD7 MSB	56	O	”
$\overline{RAS}$	62	O	VRAM row address strobe
$\overline{CAS\ 0}$	61	O	VRAM column address strobe 0 (first half of VRAM)
$\overline{CAS\ 1}$	60	O	VRAM column address strobe 1 (last half of VRAM)
$\overline{CAS\ X}$	59	O	VRAM column address strobe X (for expansion VRAM)
R/$\overline{W}$	57	O	VRAM write strobe
G	22	O	Linear RGB signal output
R	23	O	”
B	24	O	”
$\overline{YS}$	10	O	Signal for switching between MSX-VIDEO RGB output and external video signals. (For superimpose) $\overline{YS}$ = High: MSX-VIDEO output is transparent $\overline{YS}$ = Low : MSX-VIDEO output is not transparent
BLEO	7	O	Indicates No. 1 field/No. 2 field blanking with 3-value output. Open drain output High : No. 2 field and active. Middle: No. 1 field and active. Low : Linear erase interval.

Pin Name	Pin No.	I/O	Function
$\overline{\text{HSYNC}}$	5	O	High: Timing other than HSYNC or color burst timing. Low : HSYNC or timing other than color burst.
$\overline{\text{CSYNC}}$	6	O	Composite SYNC output.
CBDR	11	O	Indicates color bus direction. High: Color bus is input Low : Color bus is output
C0 LSB	19	I/O	Color bus.
C1	18	I/O	Normally color code is output. Used as input port when digitizing.
C2	17	I/O	”
C3	16	I/O	”
C4	15	I/O	”
C5	14	I/O	”
C6	13	I/O	”
C7 MSB	12	I/O	”
$\overline{\text{DHCLK}}$	2	O	Dot clock output at high resolution. Approx. 10.74MHz open drain output.
$\overline{\text{DLCLK}}$	3	O	Dot clock output at low resolution. Approx. 5.37MHz open drain output. As input is also possible by using the mode register, it is used for multi MSX-VIDEO.
XTAL 1	63	I	Used for XTAL connection. Also used for input when using an externally generated clock.
XTAL 2	64	I	
CPUCLK/ $\overline{\text{VDS}}$	8	O	1/6 of XTAL frequency is output. VRAM data select $\overline{\text{VDS}}$ = Low : VRAM access for display data. $\overline{\text{VDS}}$ = High: VRAM access for other than the above.
$\overline{\text{INT}}$	25	O	CPU interrupt output, open drain output Low: Generates interrupt.
$\overline{\text{RESET}}$	9	I	Each circuit in MSX-VIDEO is initial reset.
$\overline{\text{VRESET}}$	4	I	VSYNC input.
$\overline{\text{HRESET}}$	27	I	HSYNC input.
$\overline{\text{WAIT}}$	26	O	Wait signal to CPU is output.
V_{DD}	58	I	5V power supply.
GND	1	I	Ground 0V.
GND●DAC	20	I	Ground 0V.
V_{DD}●DAC	21	I	5V power supply.
V_{BB}	33	I	Baseboard voltage.

5 REGISTER DESCRIPTION

5-1 Added Registers

Shown below are the registers newly added to the existing V9938 registers.

	b7	b6	b5	b4	b3	b2	b1	b0
#25		CMD	VDS	YAE	YJK	WTE	MSK	SP2
#26			HO8	HO7	HO6	HO5	HO4	HO3
#27						HO2	HO1	HO0

The above three registers are cleared to "0" by the RESET signal and if used in that state, will function compatibly with V9938.

#25 b7
#26 b6, b7
#27 b3～b7
} Make sure to set "0" for these empty bit positions.

5-1-1 Horizontal Scroll Function.

	b7	b6	b5	b4	b3	b2	b1	b0	
#25							MSK	SP2	
#26			HO8	HO7	HO6	HO5	HO4	HO3	by character units
#27						HO2	HO1	HO0	by dot units

HO8－HO0 Used to set the scroll volume of still pictures in the horizontal direction one dot at a time.
(In G5 and G6 modes, scrolling is in 2-dot units.)

SP2 0 : Sets the horizontal screen size to 1 page. (Initial value)
Scrolling is done within one page and the non-displayed left side of the page is displayed on the right hand side of the screen.

1 : Sets the horizontal screen size to two pages.
Scrolling is done within 2 pages and if the first page is displayed first, then the second page will appear at the scroll operation.

MSK 0 : The left 8 dots are not masked. (Initial value)

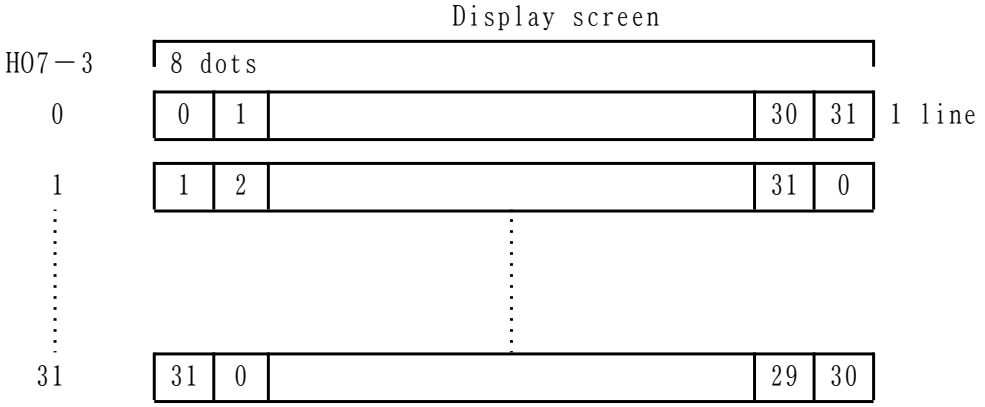
1 : The left 8 dots are masked and the border color is output.
There is no need to mask if the value in #27 is "0".
(In G5 and G6 modes, the number of masked dots is 16.)

During scrolling, once the dots disappear to the left of the screen or once the dots 1 to 7 appear on the screen, their data are not controlled by V9958 and there is no guarantee on what will be displayed.
To ensure proper display on the screen, therefore, masking is necessary.

◎ Screen display for HO8-HO3

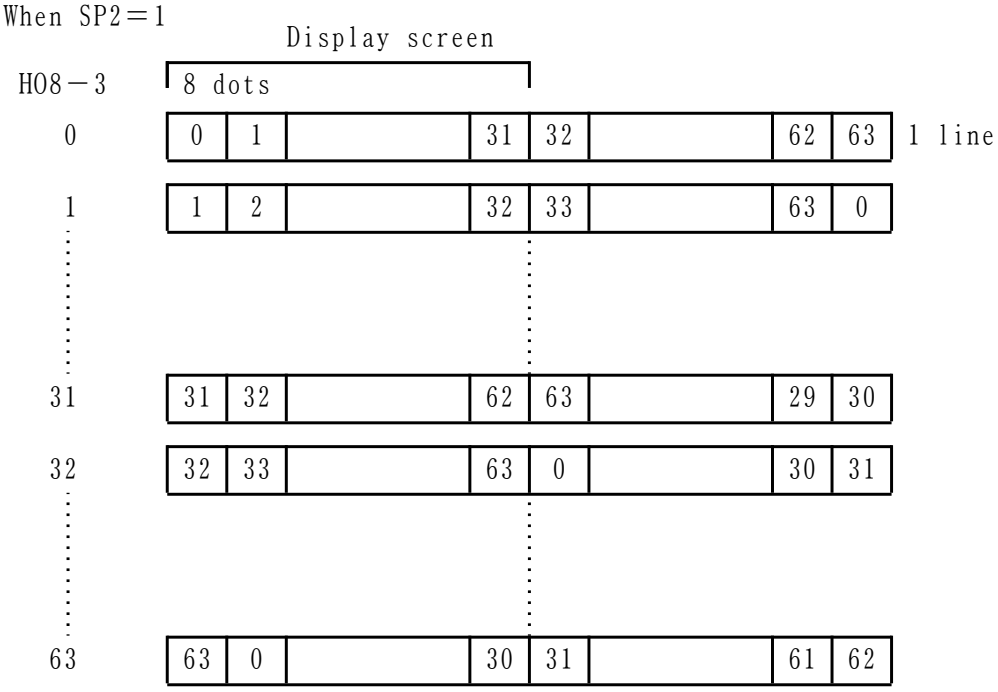
The screen is shifted to the left as specified in 8-dot units (in G5 and G6 modes, the screen is shifted in 16-dot units).

・When SP2＝0



Note) HO8 is ignored

・When SP2＝1



Note) When SP2 ＝1 , bit 5 (A15) of the pattern name table base address register (R#2) should be set to “1”.
The base address of each table will be as follows.

Pattern name table(PNT) : 0 to 31(when A15 is set to “0”)
32 to 63(when A15 is set to “1”)
Pattern generator table (PGT) : The base address remains unchanged even when scroll value is changed.
Color table (CT) : The base address remains unchanged even when scroll value is changed.

◎ Screen display for H02-H00

The screen is shifted to the right as specified in 1-dot unit (in G5 and G6 modes, the screen is shifted in 2-dot units).

(Example) ① When scrolling to the left one dot at a time

	RESET	Initial					
#26	0	1	1	.....	1	2	(Count up)
#27	0	7	6		0	7	(Count down)
		1 dot to the left	2 dots to the left		8 dots to the left	9 dots to the left	

② When scrolling to the right one dot at a time

	RESET	Initial					
#26	0	0	0	.....	31	31	(Count up)
#27	0	1	2		0	1	(Count down)
		1 dot to the right	2 dots to the right		8 dots to the right	9 dots to the right	

5-1-2 Wait Function (to speed up the writing time of data from CPU to VRAM)

	b7	b6	b5	b4	b3	b2	b1	b0
#25						WTE		

WTE 0 : Disables the WAIT function.(Initial value)
Works in the same way as V9938.
1 : Enables the WAIT function.
When the CPU accesses the VRAM, accesses to all ports on V9958 is held in the WAIT state until sccess to the VRAM of V9958 is completed.