# 1. Description

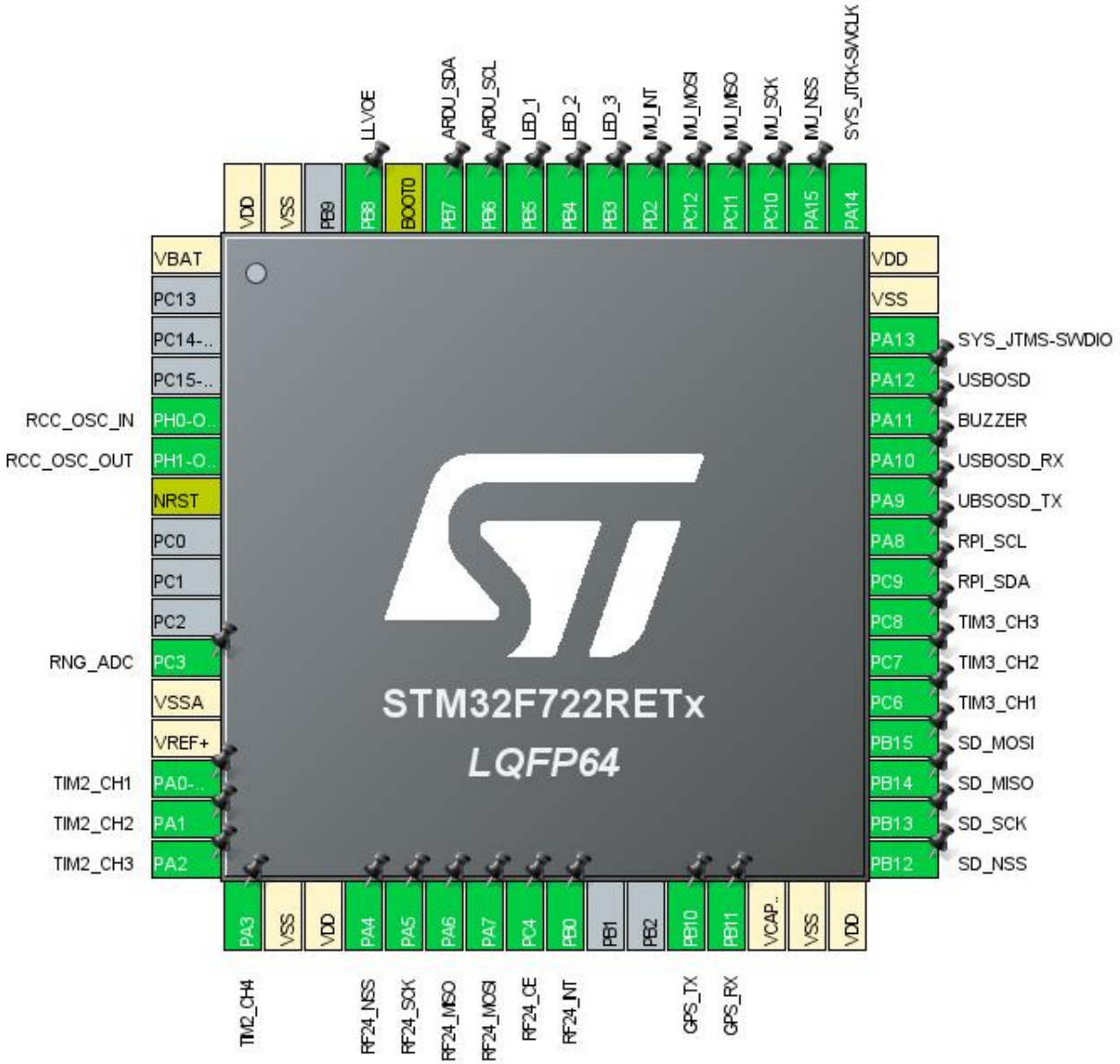
## 1.1. Project

| | |
|---|---|
| Project Name | SHARKSKYFC |
| Board Name | custom |
| Generated with: | STM32CubeMX 5.4.0 |
| Date | 10/26/2019 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F7 |
| MCU Line | STM32F7x2 |
| MCU name | STM32F722RETx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

## 2. Pinout Configuration



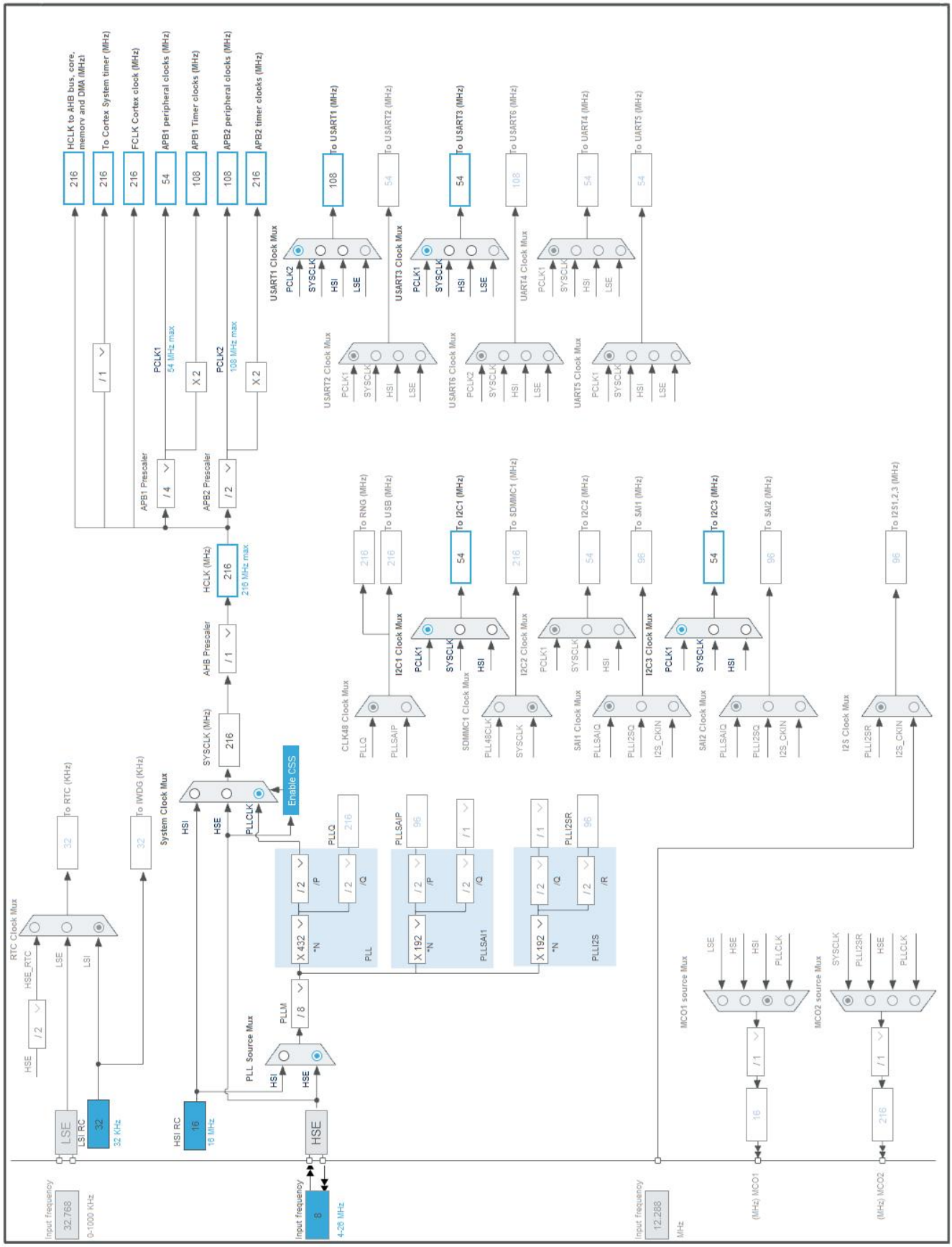
# 3. Pins Configuration

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VBAT | Power | | |
| 5 | PH0-OSC_IN | I/O | RCC_OSC_IN | |
| 6 | PH1-OSC_OUT | I/O | RCC_OSC_OUT | |
| 7 | NRST | Reset | | |
| 11 | PC3 | I/O | ADC1_IN13 | RNG_ADC |
| 12 | VSSA | Power | | |
| 13 | VREF+ | Power | | |
| 14 | PA0-WKUP | I/O | TIM2_CH1 | |
| 15 | PA1 | I/O | TIM2_CH2 | |
| 16 | PA2 | I/O | TIM2_CH3 | |
| 17 | PA3 | I/O | TIM2_CH4 | |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 20 | PA4 | I/O | SPI1_NSS | RF24_NSS |
| 21 | PA5 | I/O | SPI1_SCK | RF24_SCK |
| 22 | PA6 | I/O | SPI1_MISO | RF24_MISO |
| 23 | PA7 | I/O | SPI1_MOSI | RF24_MOSI |
| 24 | PC4 * | I/O | GPIO_Output | RF24_CE |
| 25 | PB0 | I/O | GPIO_EXTI0 | RF24_INT |
| 28 | PB10 | I/O | USART3_TX | GPS_TX |
| 29 | PB11 | I/O | USART3_RX | GPS_RX |
| 30 | VCAP_1 | Power | | |
| 31 | VSS | Power | | |
| 32 | VDD | Power | | |
| 33 | PB12 | I/O | SPI2_NSS | SD_NSS |
| 34 | PB13 | I/O | SPI2_SCK | SD_SCK |
| 35 | PB14 | I/O | SPI2_MISO | SD_MISO |
| 36 | PB15 | I/O | SPI2_MOSI | SD_MOSI |
| 37 | PC6 | I/O | TIM3_CH1 | |
| 38 | PC7 | I/O | TIM3_CH2 | |
| 39 | PC8 | I/O | TIM3_CH3 | |
| 40 | PC9 | I/O | I2C3_SDA | RPI_SDA |
| 41 | PA8 | I/O | I2C3_SCL | RPI_SCL |
| 42 | PA9 | I/O | USART1_TX | UBSOSD_TX |
| 43 | PA10 | I/O | USART1_RX | USBOSD_RX |
| 44 | PA11 * | I/O | GPIO_Output | BUZZER |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 45 | PA12 * | I/O | GPIO_Input | USBOSD |
| 46 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 47 | VSS | Power | | |
| 48 | VDD | Power | | |
| 49 | PA14 | I/O | SYS_JTCK-SWCLK | |
| 50 | PA15 | I/O | SPI3_NSS | IMU_NSS |
| 51 | PC10 | I/O | SPI3_SCK | IMU_SCK |
| 52 | PC11 | I/O | SPI3_MISO | IMU_MISO |
| 53 | PC12 | I/O | SPI3_MOSI | IMU_MOSI |
| 54 | PD2 | I/O | GPIO_EXTI2 | IMU_INT |
| 55 | PB3 * | I/O | GPIO_Output | LED_3 |
| 56 | PB4 * | I/O | GPIO_Output | LED_2 |
| 57 | PB5 * | I/O | GPIO_Output | LED_1 |
| 58 | PB6 | I/O | I2C1_SCL | ARDU_SCL |
| 59 | PB7 | I/O | I2C1_SDA | ARDU_SDA |
| 60 | BOOT0 | Boot | | |
| 61 | PB8 * | I/O | GPIO_Output | LLVOE |
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | SHARKSKYFC |
| Project Folder | C:\Users\Pluscrafter\Documents\SHARKSKY\01_Flightcontroller\Code\SHARKS |
| Toolchain / IDE | STM32CubeIDE |
| Firmware Package Name and Version | STM32Cube FW_F7 V1.15.0 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | Yes |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F7 |
| Line | STM32F7x2 |
| MCU | STM32F722RETx |
| Datasheet | 029808_Rev3 |

6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

# 7. IPs and Middleware Configuration

## 7.1. ADC1

**mode: IN13**

### 7.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 13 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.2. GPIO

## 7.3. I2C1

**I2C: I2C**

### 7.3.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |

| | |
|---|---|
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20404768 *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## *7.4. I2C3*

### I2C: I2C

### 7.4.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20404768 *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## *7.5. RCC*

### High Speed Clock (HSE): Crystal/Ceramic Resonator

### 7.5.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |

| | |
|---|---|
| Flash Latency(WS) | 7 WS (8 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Over Drive | Enabled |
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |

## *7.6. SPI1*

**Mode: Full-Duplex Master**

**Hardware NSS Signal: Hardware NSS Output Signal**

### 7.6.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **54.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Output Hardware |

## *7.7. SPI2*

**Mode: Full-Duplex Master**

**Hardware NSS Signal: Hardware NSS Output Signal**

### 7.7.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |

| | |
|---|---|
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **27.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Output Hardware |

## *7.8. SPI3*

**Mode: Full-Duplex Master**

**Hardware NSS Signal: Hardware NSS Output Signal**

### 7.8.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **27.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Output Hardware |

## *7.9. SYS*

**Debug: Serial Wire**

**Timebase Source: SysTick**

## 7.10. TIM2

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.10.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |

| | |
|---|---|
| CH Polarity | High |

## 7.11. TIM3

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

### 7.11.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## 7.12. TIM5

### mode: Clock Source

### 7.12.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

## 7.13. TIM6

### mode: Activated

### 7.13.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## 7.14. USART1

### Mode: Asynchronous

### 7.14.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

#### Advanced Parameters:

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

#### Advanced Features:

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## *7.15. USART3*

### Mode: Asynchronous

### 7.15.1. Parameter Settings:

#### Basic Parameters:

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

#### Advanced Parameters:

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

#### Advanced Features:

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PC3 | ADC1_IN13 | Analog mode | No pull-up and no pull-down | n/a | RNG_ADC |
| I2C1 | PB6 | I2C1_SCL | Alternate Function Open Drain | Pull-up | **Very High** * | ARDU_SCL |
| | PB7 | I2C1_SDA | Alternate Function Open Drain | Pull-up | **Very High** * | ARDU_SDA |
| I2C3 | PC9 | I2C3_SDA | Alternate Function Open Drain | Pull-up | **Very High** * | RPI_SDA |
| | PA8 | I2C3_SCL | Alternate Function Open Drain | Pull-up | **Very High** * | RPI_SCL |
| RCC | PH0-OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1-OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SPI1 | PA4 | SPI1_NSS | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | RF24_NSS |
| | PA5 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | RF24_SCK |
| | PA6 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | RF24_MISO |
| | PA7 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | RF24_MOSI |
| SPI2 | PB12 | SPI2_NSS | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | SD_NSS |
| | PB13 | SPI2_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | SD_SCK |
| | PB14 | SPI2_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | SD_MISO |
| | PB15 | SPI2_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | SD_MOSI |
| SPI3 | PA15 | SPI3_NSS | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | IMU_NSS |
| | PC10 | SPI3_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | IMU_SCK |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PC11 | SPI3_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | IMU_MISO |
| | PC12 | SPI3_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | IMU_MOSI |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| TIM2 | PA0-WKUP | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA1 | TIM2_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA2 | TIM2_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA3 | TIM2_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM3 | PC6 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC7 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC8 | TIM3_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| USART1 | PA9 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | UBSOSD_TX |
| | PA10 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USBOSD_RX |
| USART3 | PB10 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | GPS_TX |
| | PB11 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | GPS_RX |
| GPIO | PC4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | RF24_CE |
| | PB0 | GPIO_EXTI0 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | RF24_INT |
| | PA11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | BUZZER |
| | PA12 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | USBOSD |
| | PD2 | GPIO_EXTI2 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | IMU_INT |
| | PB3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LED_3 |
| | PB4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LED_2 |
| | PB5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LED_1 |
| | PB8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LLVOE |

## 8.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| SPI1_RX | DMA2_Stream0 | Peripheral To Memory | Low |
| SPI1_TX | DMA2_Stream3 | Memory To Peripheral | Low |
| SPI2_RX | DMA1_Stream3 | Peripheral To Memory | Low |
| SPI2_TX | DMA1_Stream4 | Memory To Peripheral | Low |
| SPI3_RX | DMA1_Stream0 | Peripheral To Memory | Low |
| SPI3_TX | DMA1_Stream7 | Memory To Peripheral | Low |
| I2C1_RX | DMA1_Stream5 | Peripheral To Memory | Low |
| I2C1_TX | DMA1_Stream6 | Memory To Peripheral | Low |
| USART1_RX | DMA2_Stream2 | Peripheral To Memory | Low |
| I2C3_RX | DMA1_Stream2 | Peripheral To Memory | Low |
| USART1_TX | DMA2_Stream7 | Memory To Peripheral | Low |
| USART3_RX | DMA1_Stream1 | Peripheral To Memory | Low |

### *SPI1_RX: DMA2_Stream0 DMA request Settings:*

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

### *SPI1_TX: DMA2_Stream3 DMA request Settings:*

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

### *SPI2_RX: DMA1_Stream3 DMA request Settings:*

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment:

| | |
|---|---|
| | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *SPI2_TX: DMA1_Stream4 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *SPI3_RX: DMA1_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *SPI3_TX: DMA1_Stream7 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *I2C1_RX: DMA1_Stream5 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*I2C1_TX: DMA1_Stream6 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART1_RX: DMA2_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*I2C3_RX: DMA1_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART1_TX: DMA2_Stream7 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART3_RX: DMA1_Stream1 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## 8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| DMA1 stream0 global interrupt | true | 0 | 0 |
| DMA1 stream1 global interrupt | true | 0 | 0 |
| DMA1 stream2 global interrupt | true | 0 | 0 |
| DMA1 stream3 global interrupt | true | 0 | 0 |
| DMA1 stream4 global interrupt | true | 0 | 0 |
| DMA1 stream5 global interrupt | true | 0 | 0 |
| DMA1 stream6 global interrupt | true | 0 | 0 |
| DMA1 stream7 global interrupt | true | 0 | 0 |
| DMA2 stream0 global interrupt | true | 0 | 0 |
| DMA2 stream2 global interrupt | true | 0 | 0 |
| DMA2 stream3 global interrupt | true | 0 | 0 |
| DMA2 stream7 global interrupt | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| EXTI line0 interrupt | unused | | |
| EXTI line2 interrupt | unused | | |
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| I2C1 event interrupt | unused | | |
| I2C1 error interrupt | unused | | |
| SPI1 global interrupt | unused | | |
| SPI2 global interrupt | unused | | |
| USART1 global interrupt | unused | | |
| USART3 global interrupt | unused | | |
| TIM5 global interrupt | unused | | |
| SPI3 global interrupt | unused | | |
| TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts | unused | | |
| | | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| I2C3 event interrupt | unused | | |
| I2C3 error interrupt | unused | | |
| FPU global interrupt | unused | | |

*** User modified value**

# 9. Software Pack Report