Contents

1	PR.	AM	6											
	1.1	Prerequisites	6											
	1.2	Definition	6											
	1.3	How it works	7											
		1.3.1 Computation	7											
		1.3.2 PRAM Classificiation	7											
		1.3.3 Strengths of PRAM	8											
		1.3.4 How to compare PRAM models	8											
	1.4	MVM algorithm	10											
	1.5	SPMD sum	12											
	1.6	MM algorithm	16											
	1.7	PRAM variants and Lemmas	17											
	1.8	PRAM implementation	18											
	1.9	Amdahl's and Gustafson's Laws	20											
_	-													
2		damentals of architecture	23											
	2.1	Introduction	23 23											
		2.1.1 Simplest processor	23 24											
		2.1.2 Superscalar processor	$\frac{24}{25}$											
		2.1.4 Multi-Core Processor	$\frac{25}{25}$											
	2.2	Accessing Memory	$\frac{25}{26}$											
	2.2	2.2.1 What is a memory?	26											
		2.2.2 How to reduce processor stalls	28											
		2.2.2.1 Cache	28											
		2.2.2.2 Multi-threading	28											
		2.2.2.2 Main amounts												
3	Pro	ogramming models 31												
	3.1	Implicit SPMD Program Compiler (ISPC)	31 35											
	3.2	±												
	3.3	Message Passing model of communication	36											
	3.4	Data-Parallel model	37											
4	Dar	allel Programming Models and pthreads	39											
-1	4.1	How to create parallel algorithms and programs	39											
	4.2													
	4.3	Technologies	44											
	4.4	Threads												
		4.4.1 Flynn's taxonomy	47											
		4.4.2 Definition	47											
		4.4.3 pthreads API	49											
		4.4.3.1 Creation	49											
		4.4.3.2 Termination	50											
		4.4.3.3 Joining	51											
		4.4.3.4 Detaching	52											
		4.4.3.5 Joining through Barriers	53											
		4.4.3.6 Mutexes	54											
		4.4.3.7 Condition variables	54											

5	Ope	nMP v5.2	55
	5.1	Introduction	55
	5.2	Basic syntax	57
	5.3	·	60
			60
			65
			67
			68
		9 /	69
			72
	5.4	i	. – 76
	5.5	v	. o 79
	5.6		 87
	5.7	v	90
	5.8		94
	5.9		97
	0.5	DIVID VCCtorization	91
6	\mathbf{GP}	J Architecture 10	
	6.1		00
	6.2		01
	6.3		03
			03
			07
		0 1 ,	09
		6.3.4 Running a CUDA program on a GPU	12
		6.3.5 Implementation of CUDA abstractions	18
		6.3.6 Advanced thread scheduling	21
		6.3.7 Memory and Data Locality in Depth	26
		6.3.8 Tiling Technique	35
		6.3.8.1 Tiled Matrix Multiplication	38
		6.3.8.2 Implementation Tiled Matrix Multiplication 14	43
		6.3.8.3 Any size matrix handling	48
		6.3.9 Optimizing Memory Coalescing	53
7	CU	DA	
	7.1 7.2		
	1.2	CUDA Basics	
		7.2.1 GPGPU Best Practices	
		r r r	70^{-20}
		96 6	72
	- 0		75
	7.3		78
	7.4	• • •	80
	7.5	ů.	82
	7.6	v v	85
	7.7		93
	7.8	±	97
			97
			02
		7.8.3 Memory Management with Multiple GPUs	05

	7.8.4	Batch Processing and Cooperative Patterns with OpenMI	P 211						
	7.8.5	OpenMP for heterogeneous architectures	213						
	7.8.6	MPI-CUDA applications	216						
			220						
8.1									
8.2	Definition								
8.3	Sequer	ntial Consistency Model	225						
8.4	Memo								
	8.4.1	Allowing Reads to Move Ahead of Writes	230						
	8.4.2	Allowing writes to be reordered	232						
	8.4.3	Allowing all reorderings	234						
8.5	Langu	ages Need Memory Models Too	236						
8.6	Impler	nenting Locks	238						
	8.6.1	Introduction	238						
	8.6.2	Test-and-Set based lock	240						
	8.6.3	Test-and-Test-and-Set lock	244						
Hete	erogen	eous Processing	248						
9.1	Energy	y Constrained Computing	250						
9.2	Comp	ute Specialization	251						
9.3	Challe	nges of heterogeneous designs	265						
9.4	Reduc	ing energy consumption	268						
			271						
10.1	Depen	dencies	271						
10.2	Paralle	el Patterns	280						
	10.2.1	Nesting Pattern	281						
	10.2.2	Serial Control Patterns	282						
	10.2.3	Parallel Control Patterns	284						
	10.2.4	Serial Data Management Patterns	289						
	10.2.5	Parallel Data Management Patterns	292						
	10.2.6	Other Parallel Patterns	295						
10.3	Map F	Pattern	297						
	10.3.1	What is a Map?	297						
		10.3.2.2 Code Fusion	300						
		10.3.2.3 Cache Fusion	301						
	10.3.3								
10.4		,							
10.5									
10.0									
		•							
	10.0.4	Onzip	JJ2						
	8.1 8.2 8.3 8.4 8.5 8.6 Het 9.1 9.2 9.3 9.4 Pat 10.1 10.2	7.8.5 7.8.6 Memory C 8.1 Cohere 8.2 Definit 8.3 Sequet 8.4 Memory 8.4.1 8.4.2 8.4.3 8.5 Langu 8.6 Impler 8.6.1 8.6.2 8.6.3 Heterogen 9.1 Energy 9.2 Compt 9.3 Challe 9.4 Reduct Patterns 10.1 Depen 10.2 Paralle 10.2.1 10.2.2 10.2.3 10.2.4 10.2.5 10.2.6 10.3 Map F 10.3.1 10.3.2 10.3.4 10.4 Collect 10.4.1 10.4.2 10.5 Gather 10.5.1 10.5.2 10.5.3	7.8.5 OpenMP for heterogeneous architectures 7.8.6 MPI-CUDA applications Memory Consistency 8.1 Coherence vs Consistency 8.2 Definition 8.3 Sequential Consistency Model 8.4 Memory Models with Relaxed Ordering 8.4.1 Allowing Reads to Move Ahead of Writes 8.4.2 Allowing writes to be reordered 8.4.3 Allowing all reorderings 8.5 Languages Need Memory Models Too 8.6 Implementing Locks 8.6.1 Introduction 8.6.2 Test-and-Set based lock 8.6.3 Test-and-Test-and-Set lock Heterogeneous Processing 9.1 Energy Constrained Computing 9.2 Compute Specialization 9.3 Challenges of heterogeneous designs 9.4 Reducing energy consumption						

	10.6.1	What is a	Scatter?	•	 			 •				333
Index												330

10.6 Scatter Pattern

10.6.1 What is a Scatter?

The Scatter Pattern is a data movement pattern where elements from a source array are distributed (or scattered) to various locations in a destination array based on specified indices. Essentially, it's about writing data to random locations.

* Key Features

In general, the **input** of the scatter pattern is:

- Source data array: value to be written.
- Index array: specifies where each value should be written in the destination.

Each element from the source is written to the position in the target array specified by the corresponding index. The **output** is a **target** array where the data is scattered across the positions.

Gather vs. Scatter

The main differences between gather and scatter are:

- Gather (read focused): Involves random reads where the read locations are provided as input.
- Scatter (write focused): Involves random writes with write locations provided as input, which can lead to race conditions.

X Serial implementation

The following pseudocode shows a serial implementation of the scatter pattern:

```
1 template < typename Data, typename Idx >
  void scatter(
                      // Number of elements
       size t n.
                      // in the output data collection
       size_t m,
                      // Number of elements
                      // in the input data and index collection
       Data a[],
                      // Input data collection (m elements)
       Data A[],
                      // Output data collection (n elements)
       Idx idx[]
                      // Input index collection (m elements)
9
10 ) {
       // Loop through each input element
       for (size_t i = 0; i < m; ++i) {</pre>
12
           // Get the target index from the index array
13
           size_t j = idx[i];
14
           \ensuremath{//} Ensure the index is within output array bounds
15
16
           assert(0 \le j \&\& j \le n);
           // Perform the scatter: write a[i] to A[j]
17
18
           A[j] = a[i];
      }
19
20 }
```

The method is characterized by:

- Loop (for): Iterates through each element in the input array a[] (length m).
- Indexing (j = idx[i]): Determines where to place a[i] in the output array A[].
- Boundary Check (assert): Ensures the index j is valid (avoids outof-bounds errors).
- Write Operation (A[j] = a[i]): Scatters the data from a[i] to A[j].

The possibilities to parallelize the code are interesting, but instead of the gather pattern, here we have a problem with race conditions on write operations. So the code can be parallelized (**parallelize over for loop to perform random write**), but we need to find some strategies to avoid race conditions.

A Race Conditions in Scatter

Unfortunately, the scatter pattern can lead to race conditions because of the way it handles writes to memory. As we know, a race condition occurs when two or more operations try to access and modify the same data at the same time, and the final result depends on the order in which the operations are performed.

In the scatter pattern, we're performing random writes to different locations in memory. The **problem arises when multiple write operations target the same location at the same time**. Because the writes happen in parallel, we can't predict:

- 1. Which write will happen first
- 2. Which value will be stored last

Example 48: Race Condition in Scatter

Consider this:

• Source Data:

$$A = [A, B, C, D, E, F]$$

• Index Array (write locations):

$$idx = [1, 5, 0, 2, 2, 4]$$

This means that the two threads that will handle the 3rd and 4th positions on the index array will suffer from a race condition. Because if they try to write at the same time, the result will depend on which thread finishes last:

- If thread A (writing D) finishes last, position 2 will be equal to D.
- If thread B (writing E) finishes last, position 2 will be equal to E.