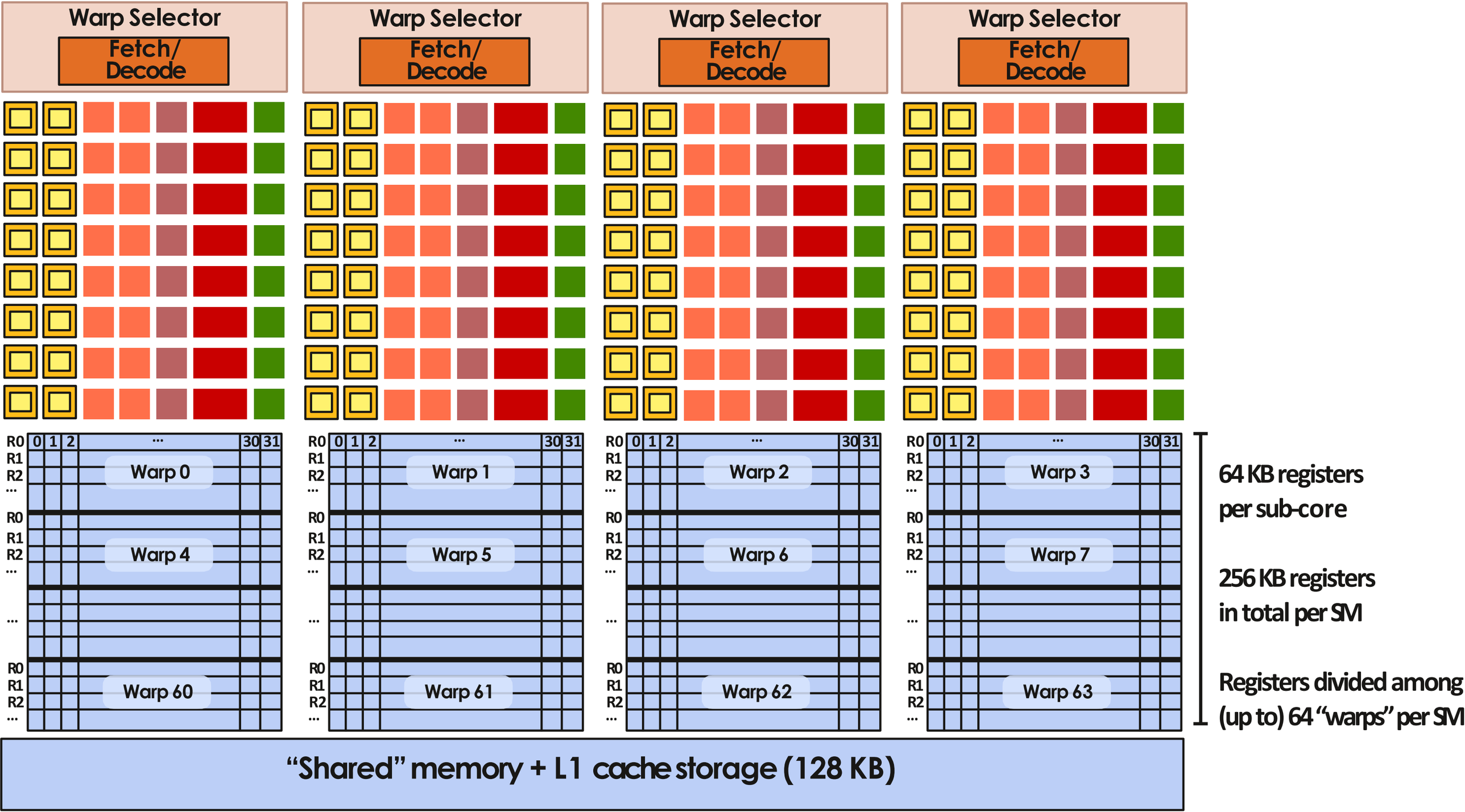
Warp Selector
Fetch/ Decode
Warp Selector
Fetch/ Decode
Warp Selector
Fetch/ Decode
Warp Selector
Fetch/ Decode
R0 R1 R2 ... 0 1 2 ... 30 31
Warp 0
Warp 4
Warp 60
Warp 1
Warp 5
Warp 61
Warp 2
Warp 6
Warp 62
Warp 3
Warp 7
Warp 63
64 KB registers per sub-core
256 KB registers in total per SM
Registers divided among (up to) 64 "warps" per SM
"Shared" memory + L1 cache storage (128 KB)