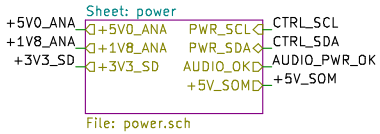
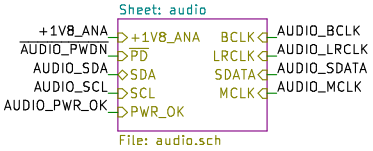
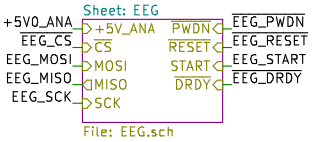
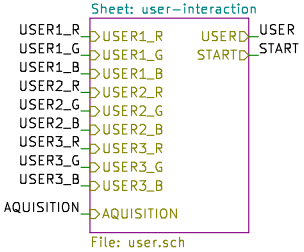
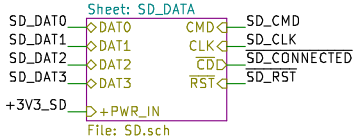


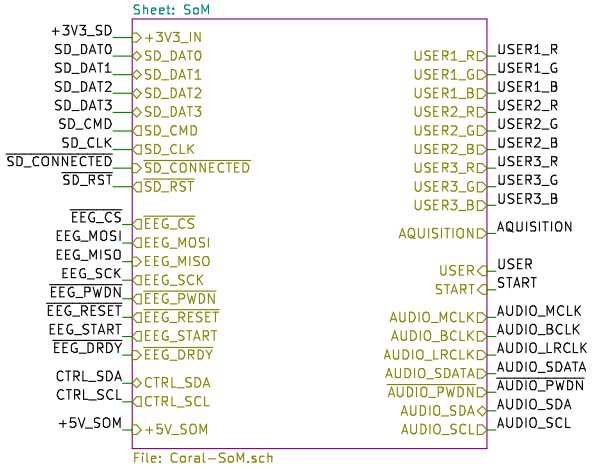




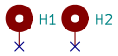
PS I2C addresses:
- **0x5C: HW monitor**







State:
- **Preliminary schematics: done**
- **Layout: to do**
- **Revised schematic: to do**
- **Schematic validation: to do**
- **Layout validation: to do**
- **BOM optimization: to do**
- **Physical testing: to do**



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Sheet: /
File: mist-eeg.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
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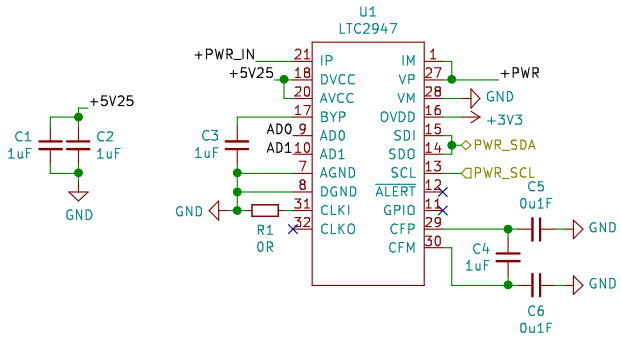
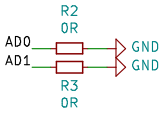


HWMon

HWMon bypass

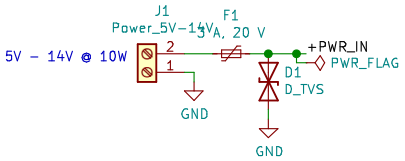


HWMon I2C address

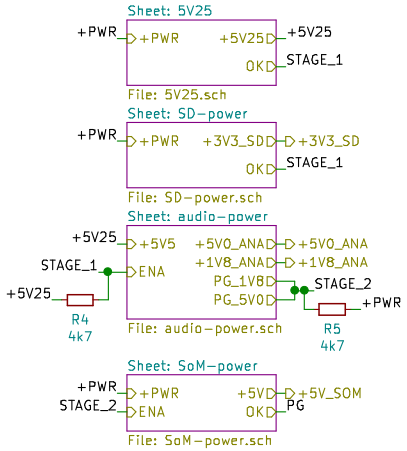
Table 3. I²C Addresses

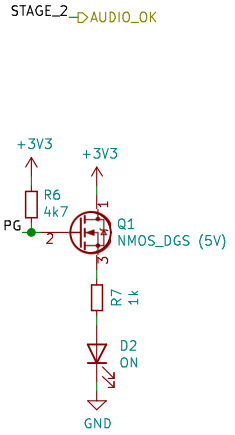
AD0	AD1	8-BIT ADDRESS BYTE WRITE	8-BIT ADDRESS BYTE READ	7-BIT DEVICE ADDRESS	BINARY DEVICE ADDRESS							
				a6:a0	a6	a5	a4	a3	a2	a1	a0	R/$\overline{W}$
L	L	0xB8	0xB9	0x5C	1	0	1	1	1	0	0	1/0
L	H	0xBA	0xBB	0x5D	1	0	1	1	1	0	1	1/0
L	R	0xBC	0xBD	0x5E	1	0	1	1	1	1	0	1/0
R	L	0xC8	0xC9	0x64	1	1	0	0	1	0	0	1/0
R	H	0xCA	0xCB	0x65	1	1	0	0	1	0	1	1/0
R	R	0xCC	0xCD	0x66	1	1	0	0	1	1	0	1/0

Note 10: L: tie to DGND, H: tie to OVDD, R: resistor, connect to DGND with a 100kΩ resistor.



External power port & protection





Rails

3V3 V @ 1.75 A (TPS84A20):
- SD card, 2.88 W max

5V0 (clean) @ 50 mA:
- ADS1299 Analog supply
- LTC2947 supply

1V8 (clean) @ 10 mA
- ADAU1777 Analog supply

Sequencing

ADC supplies:
1 – 5V25 (intermediate)
2 – 5V & 1V8 (clean)

Audio:
1 – 1.8V (clean)
2 – 3.3V

Global:
1 – 3.3V, 5.25V (Intermediate)
2 – 1.8V (Clean), 5V (Clean)
3 – 5V (Board power)

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Sheet: /power/
File: power.sch

Title: Portiloop

Size: USLetter	Date: 2021–06–07	**Rev: 1A**
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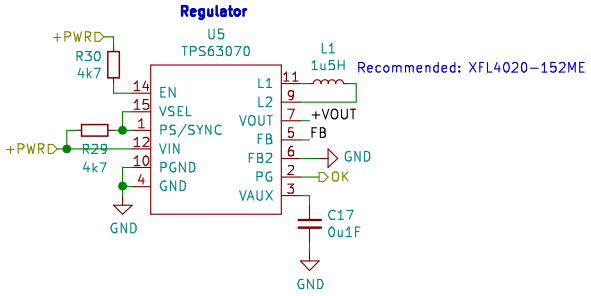

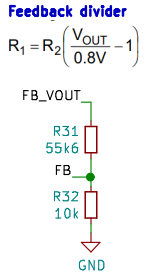

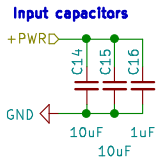

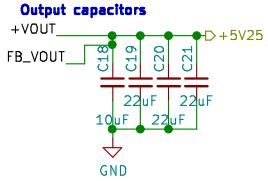

Table 3. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)			
	22	47	68	100
1.0		√	√	√
1.5		√(3)	√	√
2.2			√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
(3) Typical application. Other check marks indicates recommended filter combinations

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Sheet: /power/5V25/
File: 5V25.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
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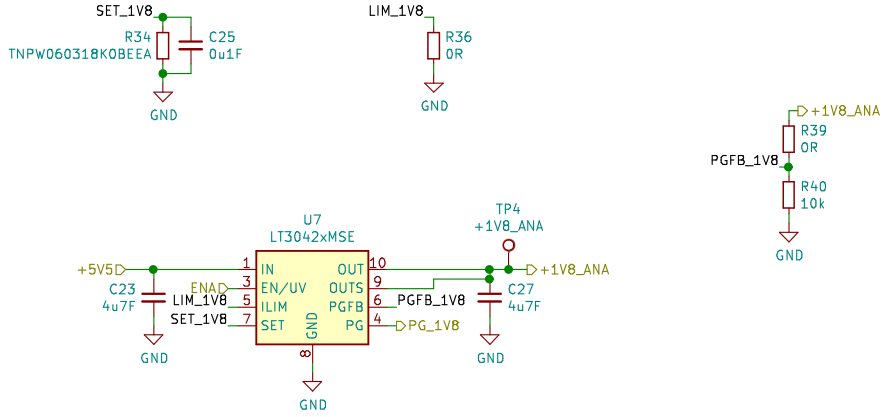
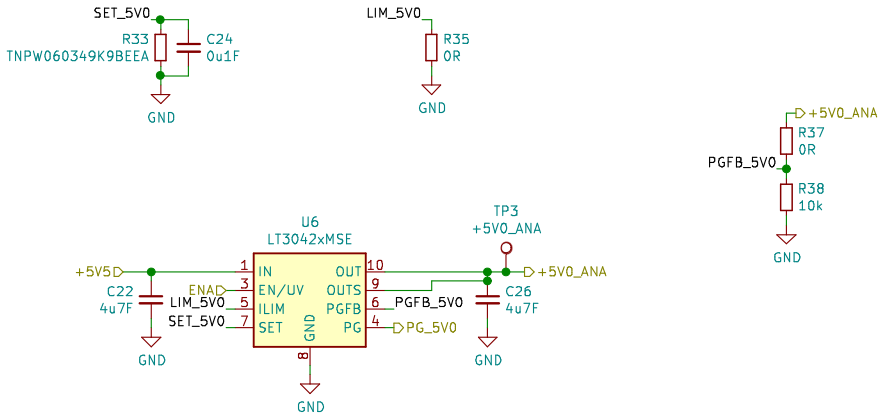
1V8 (clean regulator)



5V0 (clean regulator)



R_set = Vout / 100µA

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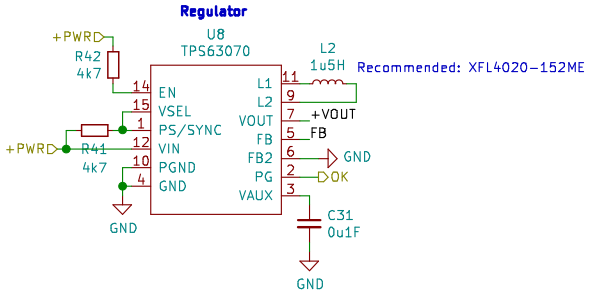
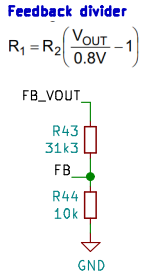
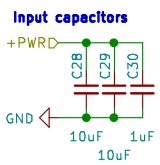
Sheet: /power/audio-power/
File: audio-power.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 4/11







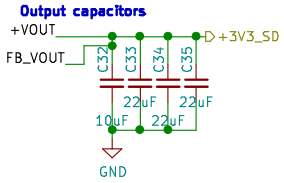


Table 3. Output Filter Selection

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	22	47	68	100
1.0		√	√	√
1.5		√(3)	√	√
2.2			√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
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(3) Typical application. Other check marks indicates recommended filter combinations

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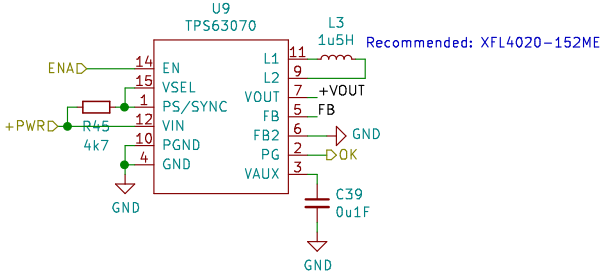
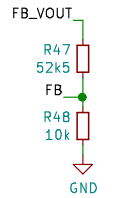
MIST Lab
Sheet: /power/SD-power/
File: SD-power.sch
Title: Portiloop
Size: USLetter | Date: 2021-06-07 | **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 | Id: 5/11

Regulator

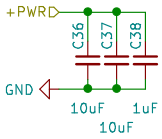


Feedback divider

$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$



Input capacitors



Output capacitors

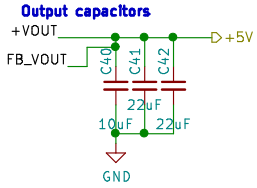


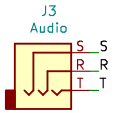
Table 3. Output Filter Selection

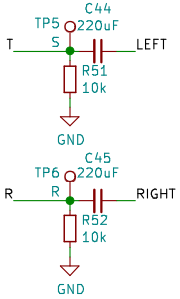
INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)			
	22	47	68	100
1.0		√	√	√
1.5		√(3)	√	√
2.2			√	√

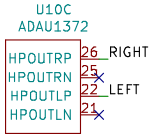
(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
(3) Typical application. Other check marks indicates recommended filter combinations

Sheet: /power/SoM-power/		
File: SoM-power.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.10		Id: 6/11

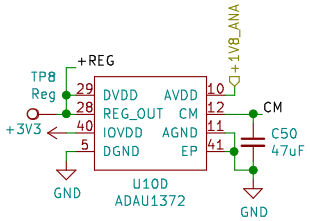
According to wikipedia:
T: Left
R: Right
S: GND

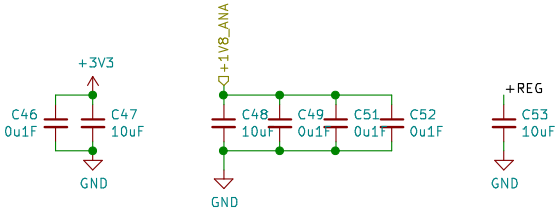




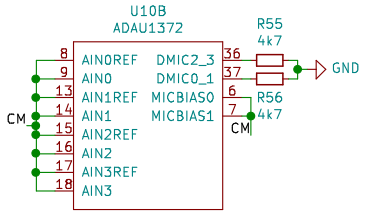


Jack output



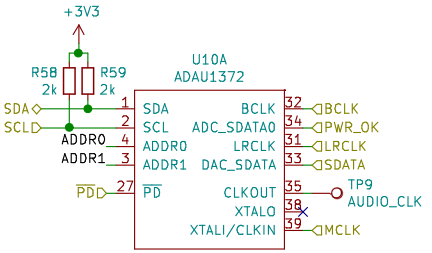


Power & decoupling



Mic Input – Unused

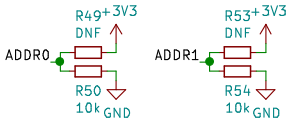
ADC_SDATA0 is connected
to the power good output
Mute the CODEC when it
goes low to avoid pops



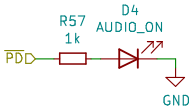
Digital IOs

Table 21. I²C Address Format

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	ADDR1	ADDR0



I2C address



Feedback LED

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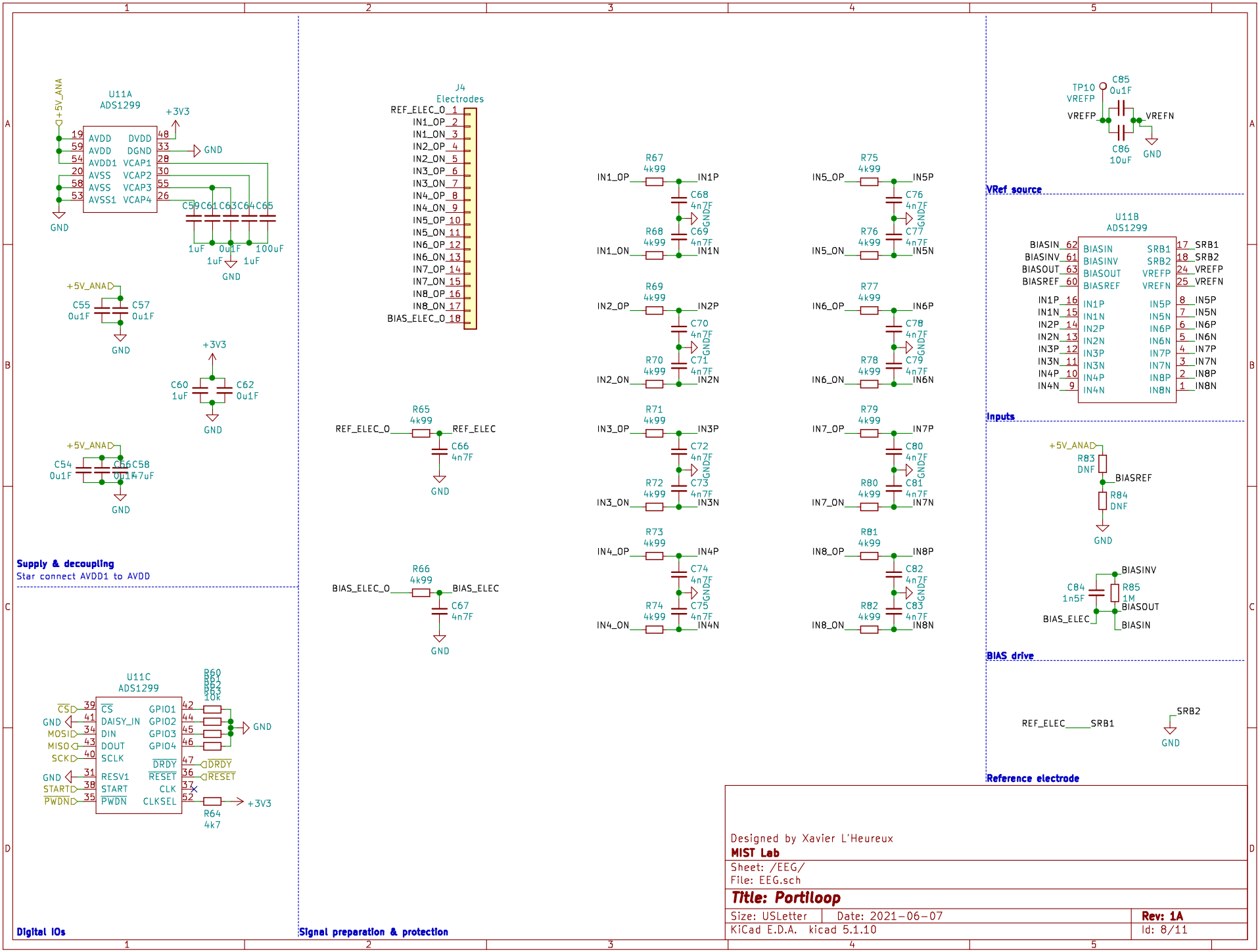
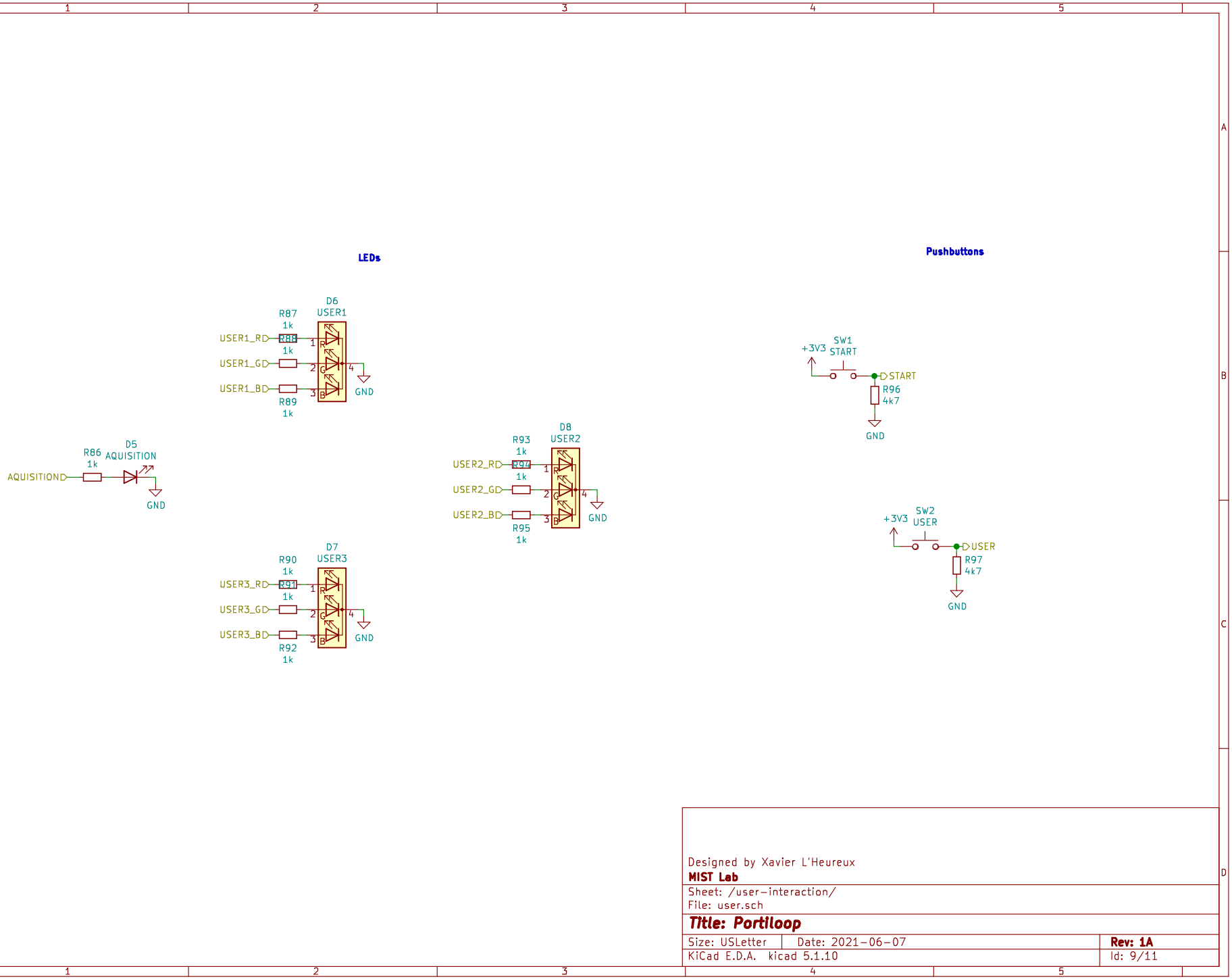
Sheet: /audio/
File: audio.sch

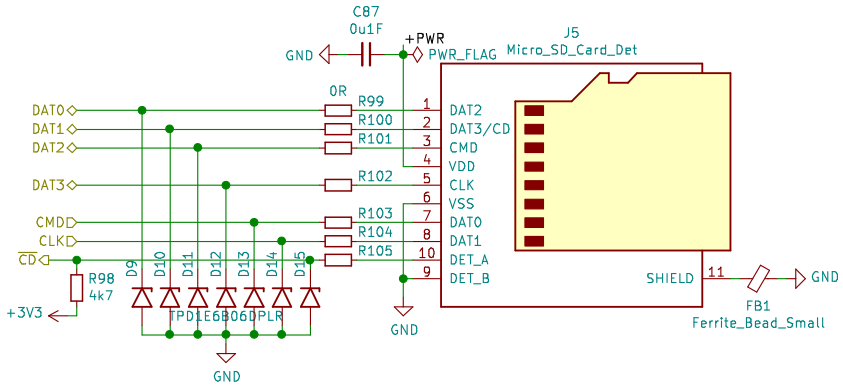
Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 7/11

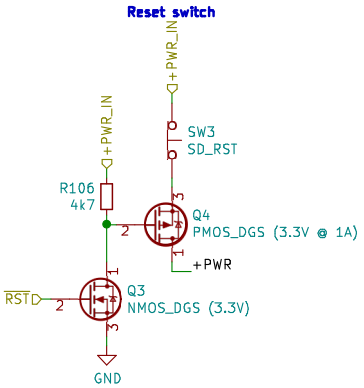

U11A
ADS1299
+5V_ANA
+3V3
GND
AVDD
DVDD
AVDD
DGND
AVDD1
VCAP1
AVSS
VCAP2
AVSS
VCAP3
AVSS1
VCAP4
C59 1uF
C61 0u1F
C63 1uF
C64 1uF
C65 100uF
C55 0u1F
C57 0u1F
C60 1uF
C62 0u1F
C54 0u1F
C66 0u1F
C58 4u7F
Supply & decoupling
Star connect AVDD1 to AVDD
U11C
ADS1299
CS
GND
MOSI
MISO
SCK
GND
START
PWDN
DAISY_IN
DIN
DOUT
SCLK
RESV1
START
PWDN
GPIO1
GPIO2
GPIO3
GPIO4
DRDY
RESET
CLK
CLKSEL
R60
R61
R62
R63
10K
R64
4k7
Digital IOs
J4
Electrodes
REF_ELEC_0
IN1_OP
IN1_ON
IN2_OP
IN2_ON
IN3_OP
IN3_ON
IN4_OP
IN4_ON
IN5_OP
IN5_ON
IN6_OP
IN6_ON
IN7_OP
IN7_ON
IN8_OP
IN8_ON
BIAS_ELEC_0
R65
4k99
REF_ELEC
C66
4n7F
R66
BIAS_ELEC
C67
R67
R68
C68
C69
R69
R70
C70
C71
R71
R72
C72
C73
R73
R74
C74
C75
R75
R76
C76
C77
R77
R78
C78
C79
R79
R80
C80
C81
R81
R82
C82
C83
Signal preparation & protection
TP10
VREFP
C85
0u1F
VREFN
C86
10uF
VRef source
U11B
ADS1299
BIASIN
BIASINV
BIASOUT
BIASREF
IN1P
IN1N
IN2P
IN2N
IN3P
IN3N
IN4P
IN4N
SRB1
SRB2
VREFP
VREFN
IN5P
IN5N
IN6P
IN6N
IN7P
IN7N
IN8P
IN8N
Inputs
R83
DNF
R84
DNF
C84
1n5F
R85
1M
BIAS drive
REF_ELEC
SRB1
SRB2
Reference electrode
Designed by Xavier L'Heureux
MIST Lab
Sheet: /EEG/
File: EEG.sch
Title: Portiloop
Size: USLetter
Date: 2021-06-07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 8/11


LEDs
Pushbuttons
D6
USER1
R87
1k
R88
1k
R89
1k
USER1_RD
USER1_GD
USER1_BD
GND
D5
AQUISITION
R86
1k
AQUISITIOND
GND
D8
USER2
R93
1k
R94
1k
R95
1k
USER2_RD
USER2_GD
USER2_BD
GND
D7
USER3
R90
1k
R91
1k
R92
1k
USER3_RD
USER3_GD
USER3_BD
GND
+3V3
SW1
START
START
R96
4k7
GND
+3V3
SW2
USER
USER
R97
4k7
GND
Designed by Xavier L'Heureux
MIST Lab
Sheet: /user-interaction/
File: user.sch
Title: Portiloop
Size: USLetter
Date: 2021-06-07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 9/11

SD Card module



Resistor array: test points



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Sheet: /SD_DATA/
File: SD.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
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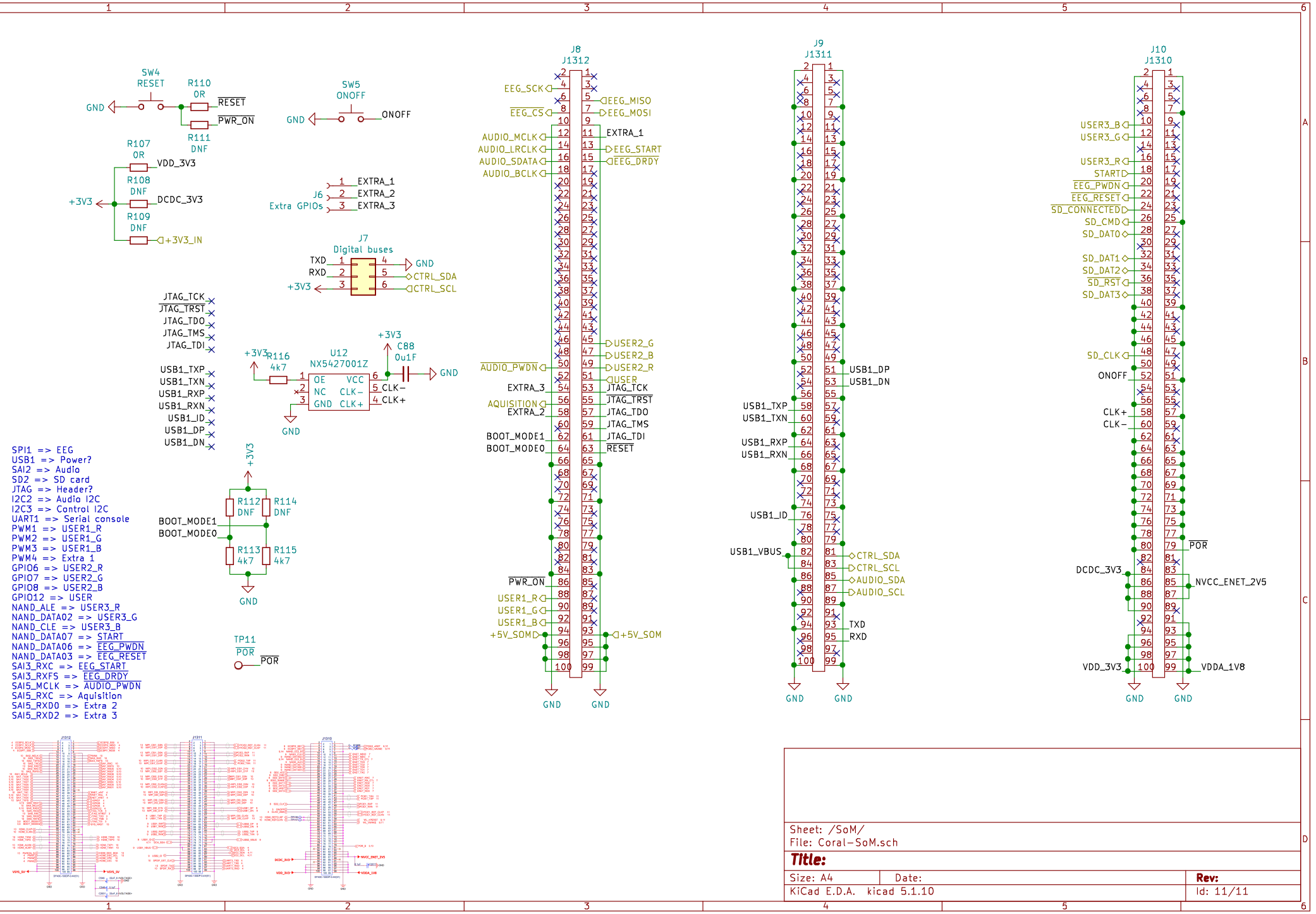

Sheet: /SoM/
File: Coral-SoM.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.10		Id: 11/11