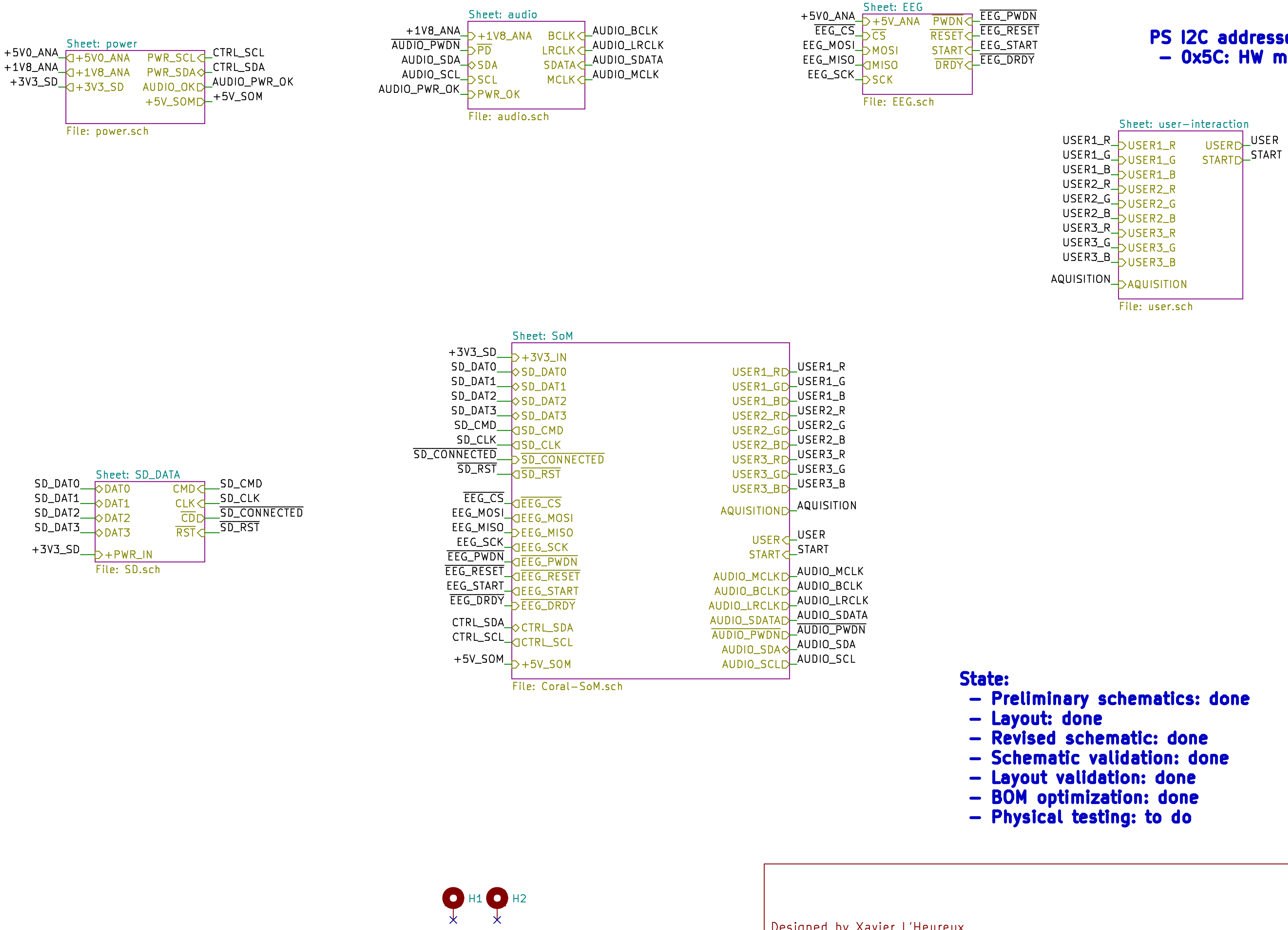
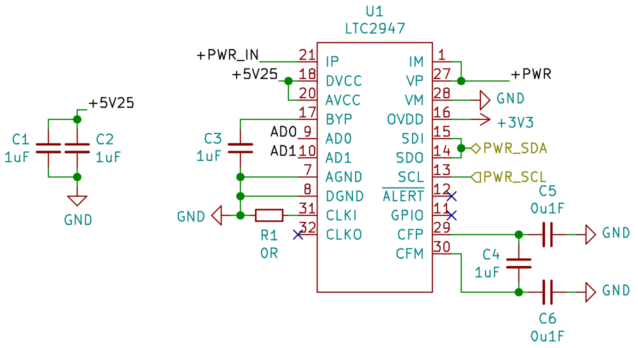
PS I2C addresses:
- **0x5C: HW monitor**



Sheet: power
+5V0_ANA
+1V8_ANA
+3V3_SD
PWR_SCL
PWR_SDA
AUDIO_OK
+5V_SOM
CTRL_SCL
CTRL_SDA
AUDIO_PWR_OK
+5V_SOM
File: power.sch
Sheet: audio
+1V8_ANA
AUDIO_PWDN
AUDIO_SDA
AUDIO_SCL
AUDIO_PWR_OK
+1V8_ANA
PD
SDA
SCL
PWR_OK
BCLK
LRCLK
SDATA
MCLK
AUDIO_BCLK
AUDIO_LRCLK
AUDIO_SDATA
AUDIO_MCLK
File: audio.sch
Sheet: EEG
+5V0_ANA
EEG_CS
EEG_MOSI
EEG_MISO
EEG_SCK
+5V_ANA
CS
MOSI
MISO
SCK
PWDN
RESET
START
DRDY
EEG_PWDN
EEG_RESET
EEG_START
EEG_DRDY
File: EEG.sch
Sheet: user-interaction
USER1_R
USER1_G
USER1_B
USER2_R
USER2_G
USER2_B
USER3_R
USER3_G
USER3_B
AQUISITION
USER
START
File: user.sch
Sheet: SoM
+3V3_SD
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_CONNECTED
SD_RST
EEG_CS
EEG_MOSI
EEG_MISO
EEG_SCK
EEG_PWDN
EEG_RESET
EEG_START
EEG_DRDY
CTRL_SDA
CTRL_SCL
+5V_SOM
+3V3_IN
USER1_R
USER1_G
USER1_B
USER2_R
USER2_G
USER2_B
USER3_R
USER3_G
USER3_B
AQUISITION
USER
START
AUDIO_MCLK
AUDIO_BCLK
AUDIO_LRCLK
AUDIO_SDATA
AUDIO_PWDN
AUDIO_SDA
AUDIO_SCL
File: Coral-SoM.sch
Sheet: SD_DATA
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
+3V3_SD
DAT0
DAT1
DAT2
DAT3
+PWR_IN
CMD
CLK
CD
RST
SD_CMD
SD_CLK
SD_CONNECTED
SD_RST
File: SD.sch
H1
H2

State:
- **Preliminary schematics: done**
- **Layout: done**
- **Revised schematic: done**
- **Schematic validation: done**
- **Layout validation: done**
- **BOM optimization: done**
- **Physical testing: to do**

Designed by Xavier L'Heureux
MIST Lab
Sheet: /
File: mist-eeg.sch
Title: Portiloop
Size: USLetter Date: 2021-06-07 **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 Id: 1/11


U1
LTC2947
+PWR_IN
+5V25
IP
DVCC
AVCC
BYP
AD0
AD1
AGND
DGND
CLKI
CLKO
IM
VP
VM
OVDD
SDI
SDO
SCL
ALERT
GPIO
CFP
CFM
+PWR
GND
+3V3
PWR_SDA
PWR_SCL
C1
1uF
C2
1uF
+5V25
GND
C3
1uF
GND
R1
0R
C4
1uF
C5
0u1F
C6
0u1F
GND
GND

HWMon

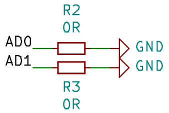
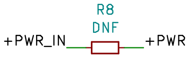

R2
0R
AD0
AD1
GND
GND
R3
0R

Table 3. I^{2}C Addresses

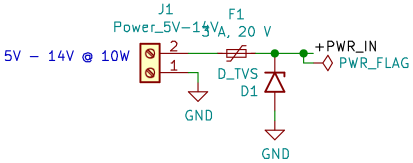
AD0	AD1	8-BIT ADDRESS BYTE WRITE	8-BIT ADDRESS BYTE READ	7-BIT DEVICE ADDRESS	BINARY DEVICE ADDRESS							
				a6:a0	a6	a5	a4	a3	a2	a1	a0	R/$\overline{W}$
L	L	0xB8	0xB9	0x5C	1	0	1	1	1	0	0	1/0
L	H	0xBA	0xBB	0x5D	1	0	1	1	1	0	1	1/0
L	R	0xBC	0xBD	0x5E	1	0	1	1	1	1	0	1/0
R	L	0xC8	0xC9	0x64	1	1	0	0	1	0	0	1/0
R	H	0xCA	0xCB	0x65	1	1	0	0	1	0	1	1/0
R	R	0xCC	0xCD	0x66	1	1	0	0	1	1	0	1/0

Note 10: L: tie to DGND, H: tie to OVDD, R: resistor, connect to DGND with a 100kΩ resistor.

HWMon I2C address


R8
DNF
+PWR_IN
+PWR

HWMon bypass


J1
Power_5V-14V
F1
3A, 20 V
5V – 14V @ 10W
2
1
+PWR_IN
PWR_FLAG
D_TVS
D1
GND
GND

External power port & protection

Rails

3V3 V @ 1.75 A (TPS63070):
- SD card, 2.88 W max

5V0 (clean) @ 50 mA:
- ADS1299 Analog supply
- LTC2947 supply

1V8 (clean) @ 10 mA:
- ADAU1777 Analog supply

5V25 (intermediate) @ 100 mA:
- clean voltage buck-boost

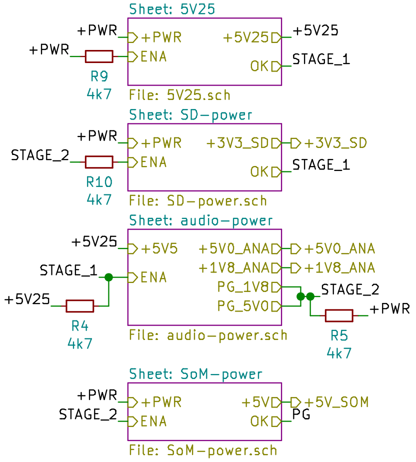
5V @ 1.2 A:
- SoM core voltage

Sequencing

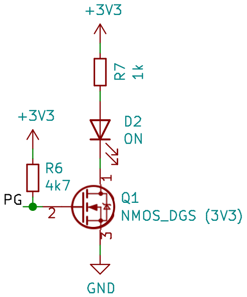
ADC supplies:
1 – 5V25 (intermediate)
2 – 5V & 1V8 (clean)

Audio:
1 – 1.8V (clean)
2 – 3.3V

Global:
1 – 5.25V (Intermediate)
2 – 1.8V (Clean), 5V (Clean)
3 – 3.3V, 5V (Board power)

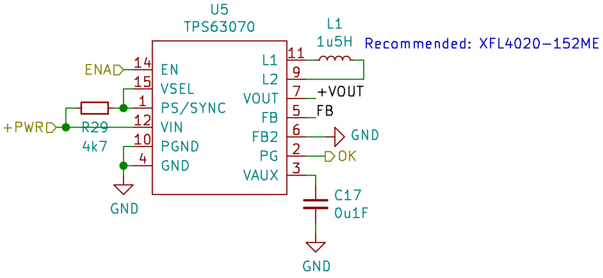

Sheet: 5V25
+PWR
+PWR
ENA
+5V25
OK
+5V25
STAGE_1
R9
4k7
File: 5V25.sch
Sheet: SD–power
+PWR
STAGE_2
+PWR
ENA
+3V3_SD
OK
+3V3_SD
STAGE_1
R10
4k7
File: SD–power.sch
Sheet: audio–power
+5V25
STAGE_1
+5V25
+5V5
ENA
+5V0_ANA
+1V8_ANA
PG_1V8
PG_5V0
+5V0_ANA
+1V8_ANA
STAGE_2
+PWR
R4
4k7
R5
4k7
File: audio–power.sch
Sheet: SoM–power
+PWR
STAGE_2
+PWR
ENA
+5V
OK
+5V_SOM
PG
File: SoM–power.sch

STAGE_2
AUDIO_OK


+3V3
R7
1k
D2
ON
+3V3
R6
4k7
PG
Q1
NMOS_DGS (3V3)
GND

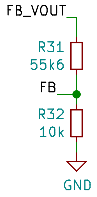
Designed by Xavier L'Heureux
MIST Lab
Sheet: /power/
File: power.sch
Title: Portiloop
Size: USLetter
Date: 2021-06-07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 2/11

Regulator

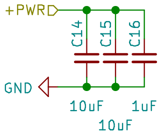

U5
TPS63070
L1
1u5H
Recommended: XFL4020−152ME
ENA
14
EN
15
VSEL
1
PS/SYNC
+PWR
R29
4k7
12
VIN
10
PGND
4
GND
GND
L1
11
L2
9
VOUT
7
+VOUT
FB
5
FB
FB2
6
GND
PG
2
OK
VAUX
3
C17
0u1F
GND

Feedback divider

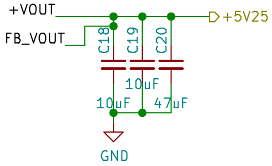
$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$


FB_VOUT
R31
55k6
FB
R32
10k
GND

Input capacitors


+PWR
C14
C15
C16
GND
10uF
1uF
10uF

Output capacitors


+VOUT
FB_VOUT
C18
C19
C20
+5V25
10uF
10uF
47uF
GND

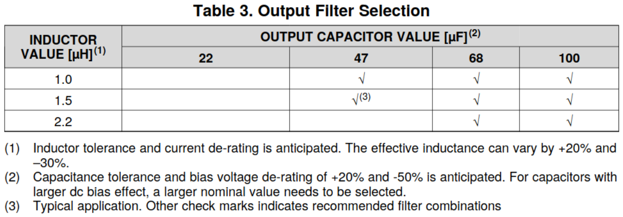


Table 3. Output Filter Selection

INDUCTOR VALUE [μH][(1)]	OUTPUT CAPACITOR VALUE [μF][(2)]			
	22	47	68	100
1.0		√	√	√
1.5		√[(3)]	√	√
2.2			√	√

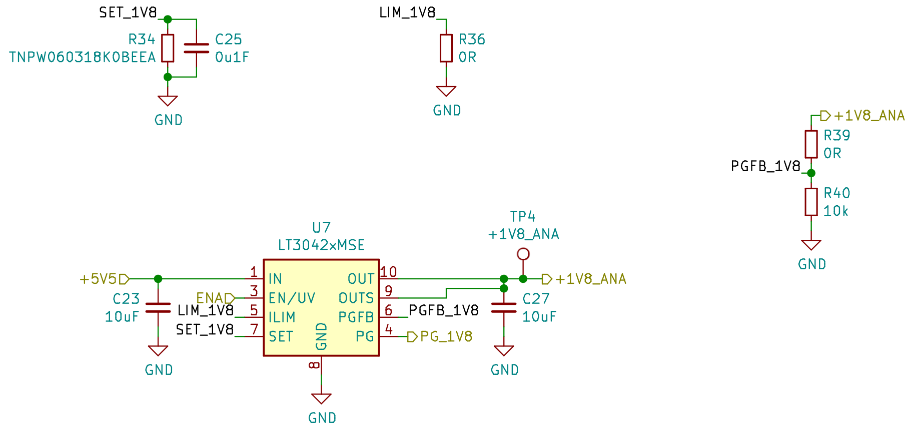
(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.

(2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.

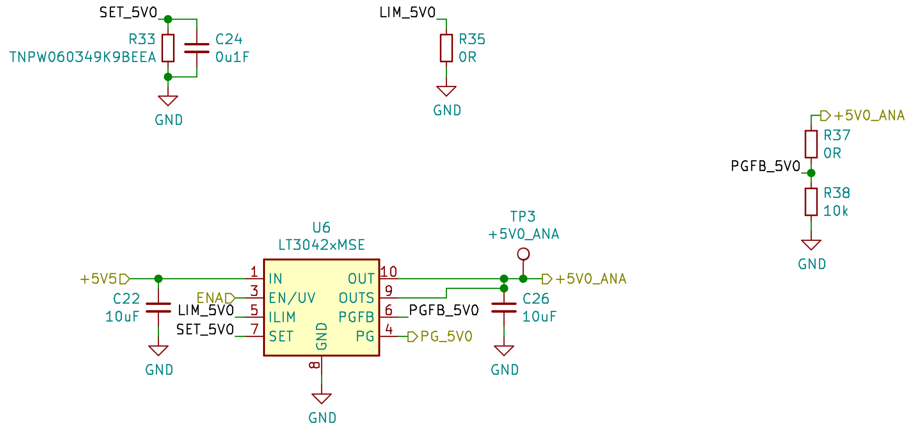
(3) Typical application. Other check marks indicates recommended filter combinations

Designed by Xavier L'Heureux
MIST Lab
Sheet: /power/5V25/
File: 5V25.sch
Title: Portiloop
Size: USLetter Date: 2021−06−07 **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 Id: 3/11

1V8 (clean regulator)


SET_1V8
R34
TNPW060318K0BEEA
C25
0u1F
GND
LIM_1V8
R36
0R
GND
+1V8_ANA
R39
0R
PGFB_1V8
R40
10k
GND
U7
LT3042xMSE
TP4
+1V8_ANA
+5V5
1 IN
3 EN/UV
5 ILIM
7 SET
GND 8
OUT 10
OUTS 9
PGFB 6
PG 4
ENAD
C23
10uF
LIM_1V8
SET_1V8
GND
PGFB_1V8
PG_1V8
+1V8_ANA
C27
10uF
GND
GND

5V0 (clean regulator)


SET_5V0
R33
TNPW060349K9BEEA
C24
0u1F
GND
LIM_5V0
R35
0R
GND
+5V0_ANA
R37
0R
PGFB_5V0
R38
10k
GND
U6
LT3042xMSE
TP3
+5V0_ANA
+5V5
1 IN
3 EN/UV
5 ILIM
7 SET
GND 8
OUT 10
OUTS 9
PGFB 6
PG 4
ENAD
C22
10uF
LIM_5V0
SET_5V0
GND
PGFB_5V0
PG_5V0
+5V0_ANA
C26
10uF
GND
GND

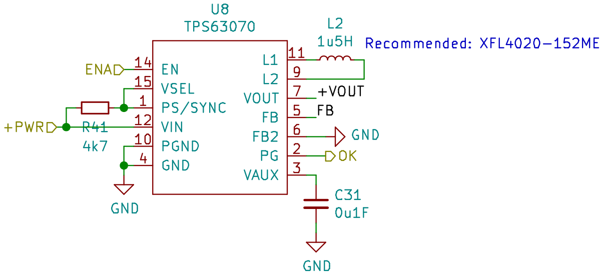
R_set = Vout / 100µA

Designed by Xavier L'Heureux
MIST Lab
Sheet: /power/audio-power/
File: audio-power.sch

Title: Portiloop

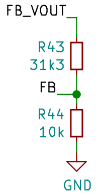
Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 4/11

Regulator

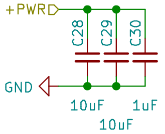

U8
TPS63070
L2
1u5H
Recommended: XFL4020−152ME
ENA
14
EN
15
VSEL
1
PS/SYNC
+PWR
R41
4k7
12
VIN
10
PGND
4
GND
GND
L1
11
L2
9
VOUT
7
+VOUT
FB
5
FB
FB2
6
GND
PG
2
OK
VAUX
3
C31
0u1F
GND

Feedback divider

$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$


FB_VOUT
R43
31k3
FB
R44
10k
GND

Input capacitors


+PWR
C28
C29
C30
GND
10uF
1uF
10uF

Output capacitors

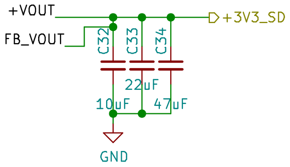
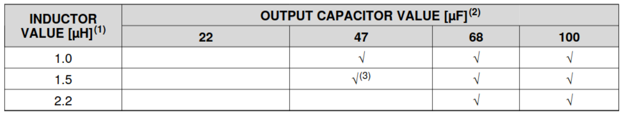

+VOUT
FB_VOUT
C32
C33
C34
+3V3_SD
22uF
10uF
47uF
GND

Table 3. Output Filter Selection



INDUCTOR VALUE [μH][1]	OUTPUT CAPACITOR VALUE [μF][2]			
	22	47	68	100
1.0		√	√	√
1.5		√[3]	√	√
2.2			√	√

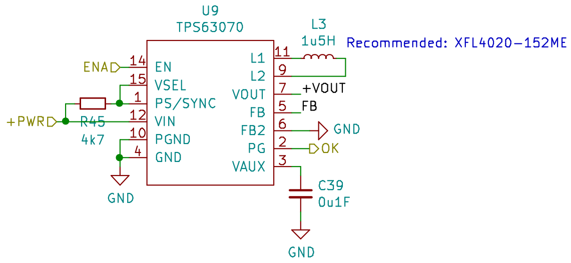
(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.

(2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.

(3) Typical application. Other check marks indicates recommended filter combinations

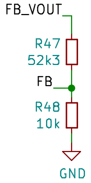
Designed by Xavier L'Heureux
MIST Lab
Sheet: /power/SD−power/
File: SD−power.sch
Title: Portiloop
Size: USLetter Date: 2021−06−07 **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 Id: 5/11

Regulator

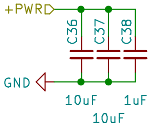

U9
TPS63070
L3
1u5H
Recommended: XFL4020-152ME
ENA
14
EN
15
VSEL
1
PS/SYNC
12
VIN
10
PGND
4
GND
+PWR
R45
4k7
GND
11
L1
9
L2
7
VOUT
+VOUT
5
FB
FB
6
FB2
GND
2
PG
OK
3
VAUX
C39
0u1F
GND

Feedback divider

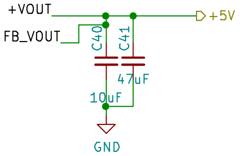
$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$


FB_VOUT
R47
52k3
FB
R48
10k
GND

Input capacitors


+PWR
C36
C37
C38
GND
10uF
1uF
10uF

Output capacitors


+VOUT
+5V
FB_VOUT
C40
C41
47uF
10uF
GND

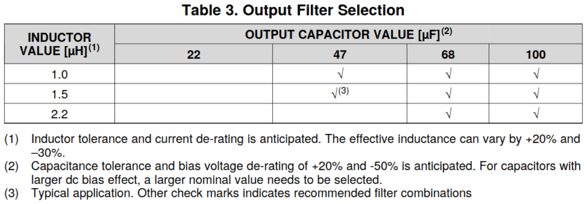


Table 3. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)			
	22	47	68	100
1.0		√	√	√
1.5		√(3)	√	√
2.2			√	√

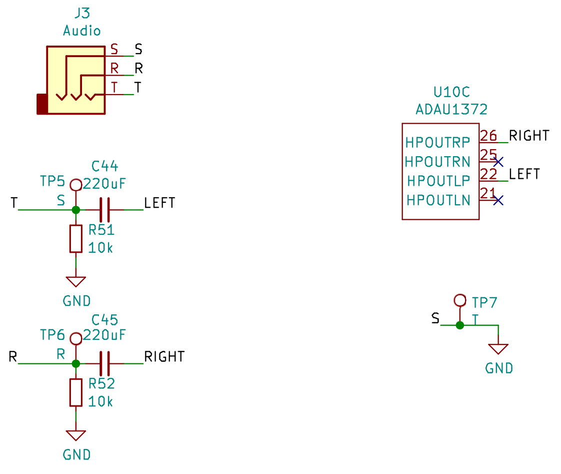
(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
(3) Typical application. Other check marks indicates recommended filter combinations

Sheet: /power/SoM-power/
File: SoM-power.sch

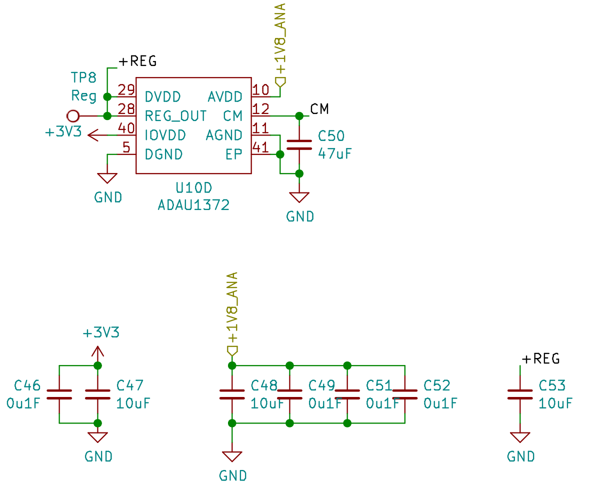
Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. kicad 5.1.10 | Id: 6/11

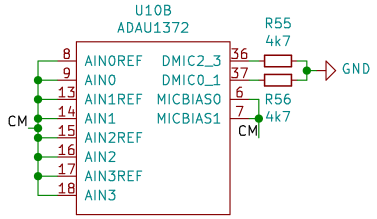
According to wikipedia:
T: Left
R: Right
S: GND


J3
Audio
S
R
T
TP5
C44
220uF
LEFT
R51
10k
GND
TP6
C45
220uF
RIGHT
R52
10k
GND
U10C
ADAU1372
HPOUTRP
HPOUTRN
HPOUTLP
HPOUTLN
26
25
22
21
RIGHT
LEFT
TP7
S
T
GND

Jack output


+1V8_ANA
TP8
Reg
+REG
+3V3
29
28
40
5
DVDD
REG_OUT
IOVDD
DGND
AVDD
CM
AGND
EP
10
12
11
41
CM
C50
47uF
GND
GND
U10D
ADAU1372
+3V3
C46
0u1F
C47
10uF
GND
+1V8_ANA
C48
10uF
C49
0u1F
C51
0u1F
C52
0u1F
GND
+REG
C53
10uF
GND

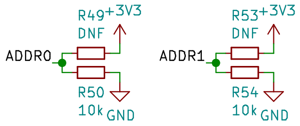
Power & decoupling


U10B
ADAU1372
8
9
13
14
15
16
17
18
AIN0REF
AIN0
AIN1REF
AIN1
AIN2REF
AIN2
AIN3REF
AIN3
CM
DMIC2_3
DMIC0_1
MICBIAS0
MICBIAS1
36
37
6
7
R55
4k7
GND
R56
4k7
CM

Mic input - Unused

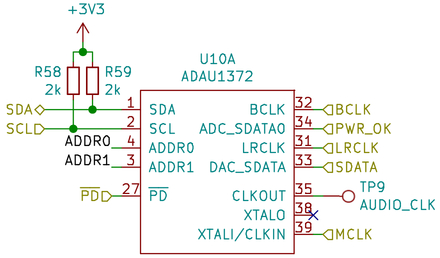
Table 21. I²C Address Format

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	ADDR1	ADDR0

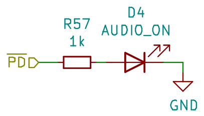

R49
DNF
+3V3
ADDR0
R50
10k
GND
R53
DNF
+3V3
ADDR1
R54
10k
GND

I2C address

ADC_SDATA0 is connected
to the power good output
Mute the CODEC when it
goes low to avoid pops

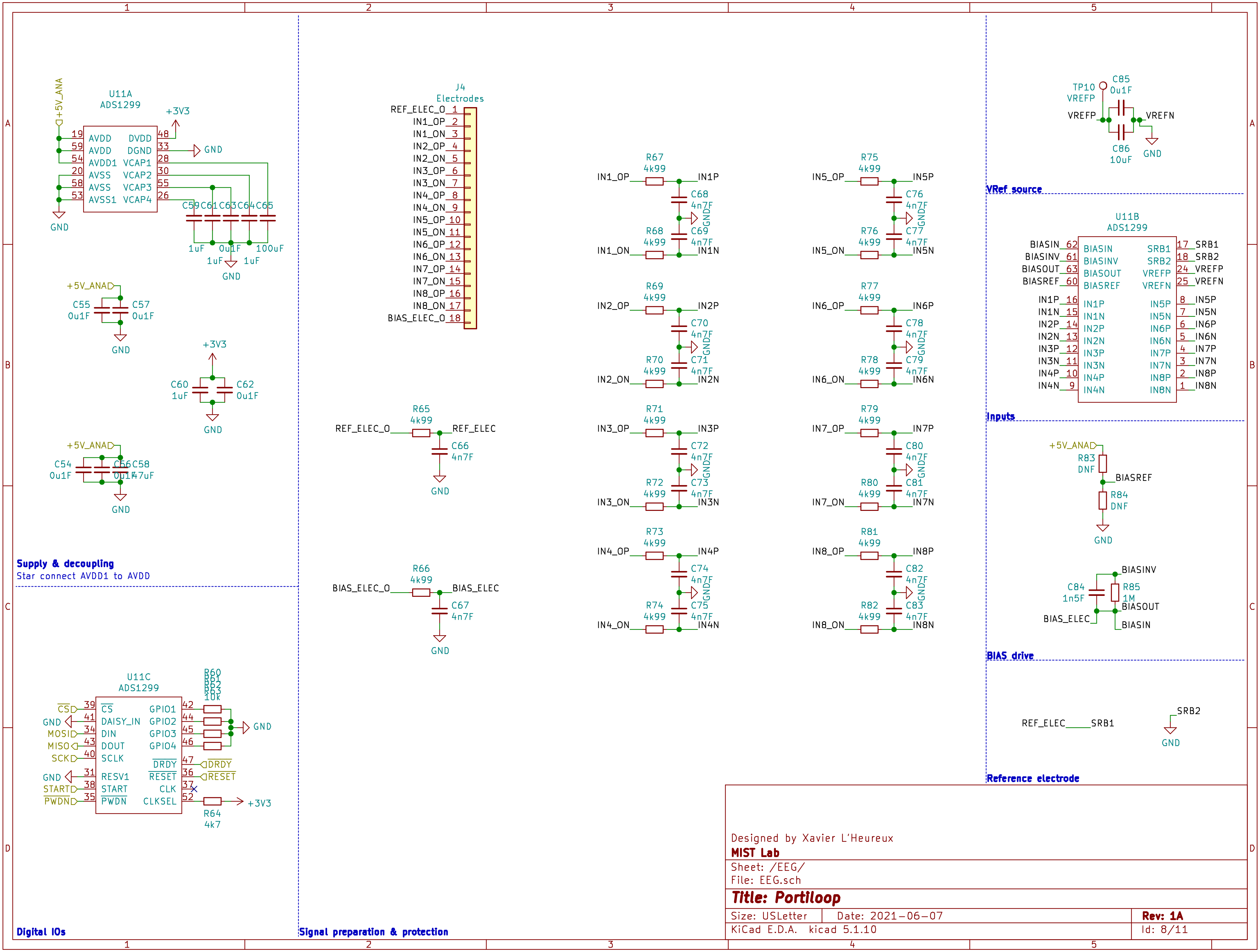

+3V3
R58
2k
R59
2k
U10A
ADAU1372
SDA
SCL
ADDR0
ADDR1
PD
1
2
4
3
27
SDA
SCL
ADDR0
ADDR1
PD
BCLK
ADC_SDATA0
LRCLK
DAC_SDATA
CLKOUT
XTALO
XTALI/CLKIN
32
34
31
33
35
38
39
BCLK
PWR_OK
LRCLK
SDATA
TP9
AUDIO_CLK
MCLK

Digital IOs


PD
R57
1k
D4
AUDIO_ON
GND

Feedback LED

Designed by Xavier L'Heureux
MIST Lab
Sheet: /audio/
File: audio.sch
Title: Portlloop
Size: USLetter Date: 2021-06-07 **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 Id: 7/11


U11A
ADS1299
+5V_ANA
+3V3
AVDD
AVDD
AVDD1
AVSS
AVSS
AVSS1
DVDD
DGND
VCAP1
VCAP2
VCAP3
VCAP4
GND
C59 C61 C63 C64 C65
1uF 0u1F 100uF
1uF 1uF
C55 0u1F
C57 0u1F
C60 1uF
C62 0u1F
C54 0u1F
C56 0u1F
C58 47uF
+5V_ANAD
Supply & decoupling
Star connect AVDD1 to AVDD
U11C
ADS1299
CS
DAISY_IN
DIN
DOUT
SCLK
RESV1
START
PWDN
GPIO1
GPIO2
GPIO3
GPIO4
DRDY
RESET
CLK
CLKSEL
MOSI
MISO
SCK
R60 R61 R62 R63 10k
R64 4k7
Digital IOs
J4
Electrodes
REF_ELEC_O
IN1_OP
IN1_ON
IN2_OP
IN2_ON
IN3_OP
IN3_ON
IN4_OP
IN4_ON
IN5_OP
IN5_ON
IN6_OP
IN6_ON
IN7_OP
IN7_ON
IN8_OP
IN8_ON
BIAS_ELEC_O
R65 4k99
REF_ELEC
C66 4n7F
R66 4k99
BIAS_ELEC
C67 4n7F
R67–R82 4k99
C68–C83 4n7F
IN1P IN1N IN2P IN2N IN3P IN3N IN4P IN4N
IN5P IN5N IN6P IN6N IN7P IN7N IN8P IN8N
Signal preparation & protection
TP10
VREFP
C85 0u1F
C86 10uF
VREFN
VRef source
U11B
ADS1299
BIASIN
BIASINV
BIASOUT
BIASREF
SRB1
SRB2
Inputs
R83 DNF
R84 DNF
C84 1n5F
R85 1M
BIAS drive
Reference electrode

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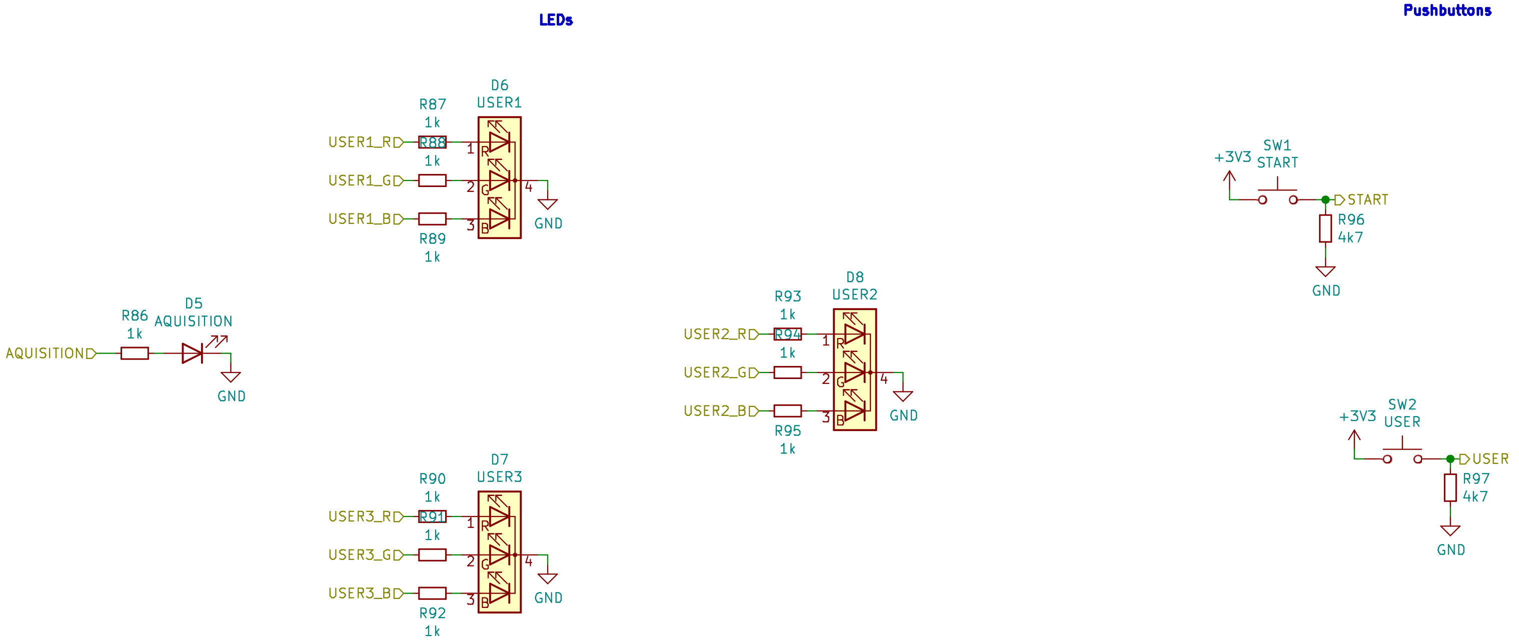
MIST Lab
Sheet: /EEG/
File: EEG.sch

Title: Portiloop

Size: USLetter Date: 2021-06-07 **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 Id: 8/11


LEDs
D6
USER1
R87
1k
R88
1k
USER1_R
USER1_G
USER1_B
R89
1k
GND
R86
1k
D5
AQUISITION
AQUISITION
GND
D8
USER2
R93
1k
R94
1k
USER2_R
USER2_G
USER2_B
R95
1k
GND
D7
USER3
R90
1k
R91
1k
USER3_R
USER3_G
USER3_B
R92
1k
GND
Pushbuttons
+3V3
SW1
START
START
R96
4k7
GND
+3V3
SW2
USER
USER
R97
4k7
GND

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MIST Lab

Sheet: /user-interaction/
File: user.sch

Title: Portiloop

Size: USLetter Date: 2021-06-07 **Rev: 1A**
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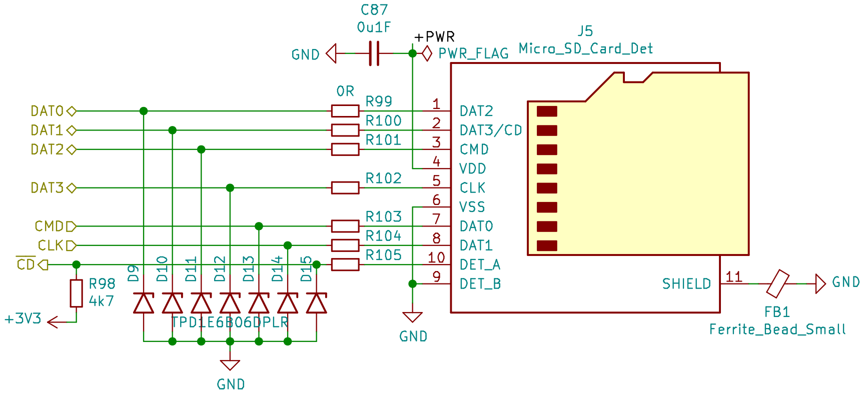
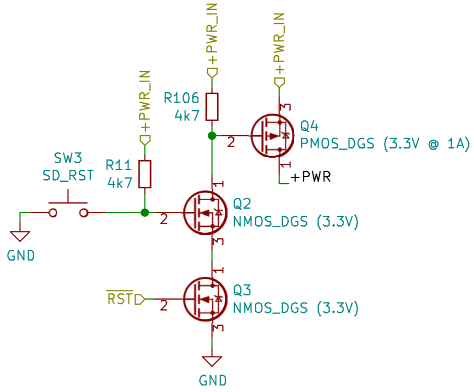
SD Card module


C87
0u1F
GND
+PWR
PWR_FLAG
J5
Micro_SD_Card_Det
0R
R99
R100
R101
R102
R103
R104
R105
DAT0
DAT1
DAT2
DAT3
CMD
CLK
$\overline{CD}$
R98
4k7
+3V3
D9
D10
D11
D12
D13
D14
D15
TPD1E6B06DPLR
GND
1 DAT2
2 DAT3/CD
3 CMD
4 VDD
5 CLK
6 VSS
7 DAT0
8 DAT1
10 DET_A
9 DET_B
SHIELD 11
GND
FB1
Ferrite_Bead_Small
GND

Resistor array: test points

Reset switch


+PWR_IN
+PWR_IN
+PWR_IN
R106
4k7
R11
4k7
SW3
SD_RST
GND
Q4
PMOS_DGS (3.3V @ 1A)
+PWR
Q2
NMOS_DGS (3.3V)
$\overline{RST}$
Q3
NMOS_DGS (3.3V)
GND

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MIST Lab

Sheet: /SD_DATA/

File: SD.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
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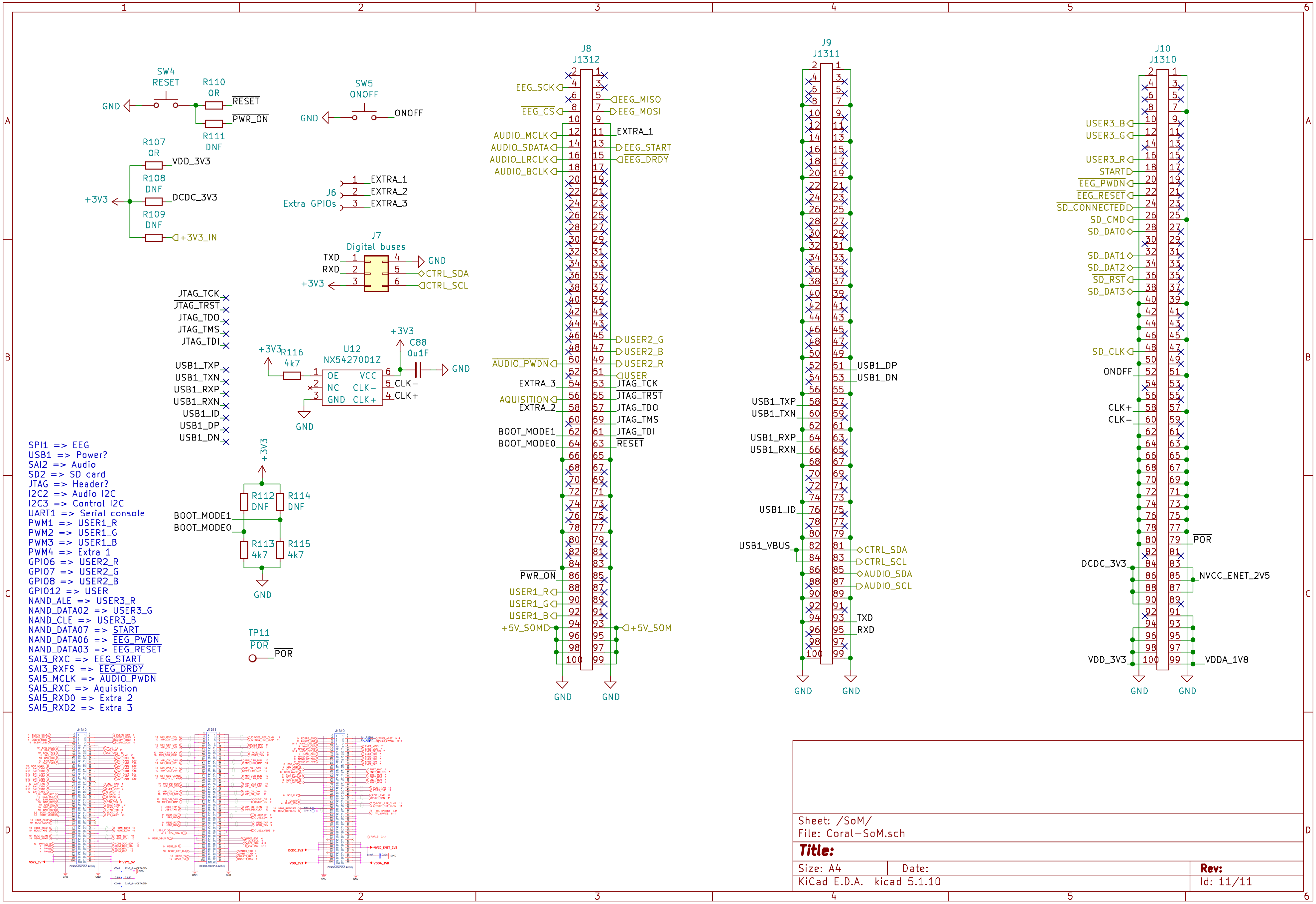
SW4
RESET
GND
R110
0R
RESET
PWR_ON
R111
DNF
SW5
ONOFF
GND
ONOFF
R107
0R
VDD_3V3
R108
DNF
DCDC_3V3
+3V3
R109
DNF
+3V3_IN
J6
Extra GPIOs
EXTRA_1
EXTRA_2
EXTRA_3
J7
Digital buses
TXD
RXD
+3V3
GND
CTRL_SDA
CTRL_SCL
JTAG_TCK
JTAG_TRST
JTAG_TDO
JTAG_TMS
JTAG_TDI
USB1_TXP
USB1_TXN
USB1_RXP
USB1_RXN
USB1_ID
USB1_DP
USB1_DN
+3V3
R116
4k7
U12
NX5427001Z
OE
VCC
NC
CLK−
GND
CLK+
C88
0u1F
GND
+3V3
R112
DNF
R114
DNF
BOOT_MODE1
BOOT_MODE0
R113
4k7
R115
4k7
GND
TP11
POR
POR
J8
J1312
EEG_SCK
EEG_CS
AUDIO_MCLK
AUDIO_SDATA
AUDIO_LRCLK
AUDIO_BCLK
EEG_MISO
EEG_MOSI
EXTRA_1
EEG_START
EEG_DRDY
USER2_G
USER2_B
AUDIO_PWDN
USER2_R
USER
EXTRA_3
JTAG_TCK
AQUISITION
JTAG_TRST
EXTRA_2
JTAG_TDO
JTAG_TMS
BOOT_MODE1
JTAG_TDI
BOOT_MODE0
RESET
PWR_ON
USER1_R
USER1_G
USER1_B
+5V_SOM
+5V_SOM
GND
GND
J9
J1311
USB1_DP
USB1_DN
USB1_TXP
USB1_TXN
USB1_RXP
USB1_RXN
USB1_ID
USB1_VBUS
CTRL_SDA
CTRL_SCL
AUDIO_SDA
AUDIO_SCL
TXD
RXD
GND
GND
J10
J1310
USER3_B
USER3_G
USER3_R
START
EEG_PWDN
EEG_RESET
SD_CONNECTED
SD_CMD
SD_DAT0
SD_DAT1
SD_DAT2
SD_RST
SD_DAT3
SD_CLK
ONOFF
CLK+
CLK−
POR
DCDC_3V3
NVCC_ENET_2V5
VDD_3V3
VDDA_1V8
GND
GND
1
2
3
4
5
6
A
B
C
D

SPI1 => EEG
USB1 => Power?
SAI2 => Audio
SD2 => SD card
JTAG => Header?
I2C2 => Audio I2C
I2C3 => Control I2C
UART1 => Serial console
PWM1 => USER1_R
PWM2 => USER1_G
PWM3 => USER1_B
PWM4 => Extra 1
GPIO6 => USER2_R
GPIO7 => USER2_G
GPIO8 => USER2_B
GPIO12 => USER
NAND_ALE => USER3_R
NAND_DATA02 => USER3_G
NAND_CLE => USER3_B
NAND_DATA07 => START
NAND_DATA06 => EEG_PWDN
NAND_DATA03 => EEG_RESET
SAI3_RXC => EEG_START
SAI3_RXFS => EEG_DRDY
SAI5_MCLK => AUDIO_PWDN
SAI5_RXC => Aquisition
SAI5_RXD0 => Extra 2
SAI5_RXD2 => Extra 3

Sheet: /SoM/
File: Coral−SoM.sch
Title:
Size: A4 Date: **Rev:**
KiCad E.D.A. kicad 5.1.10 Id: 11/11