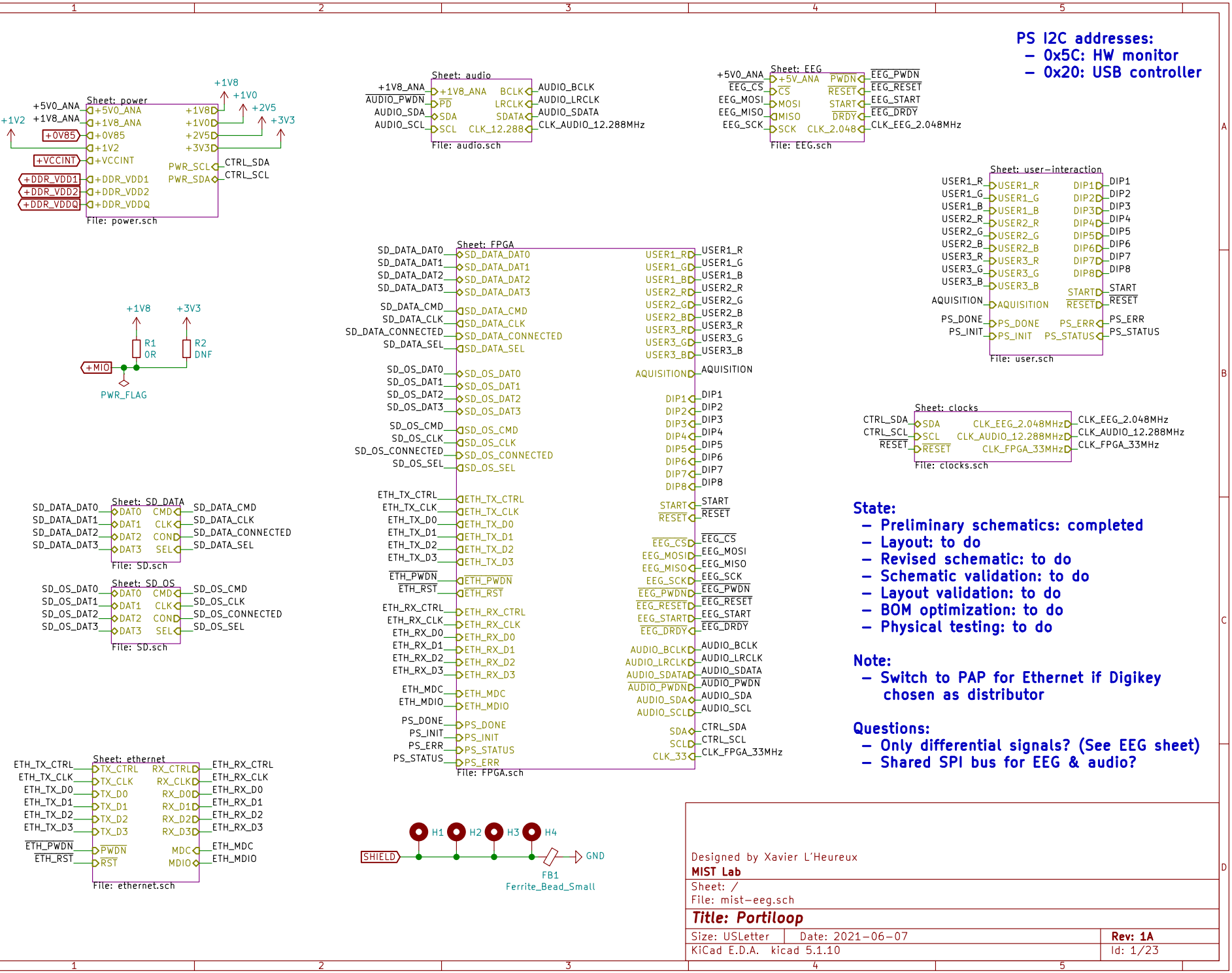
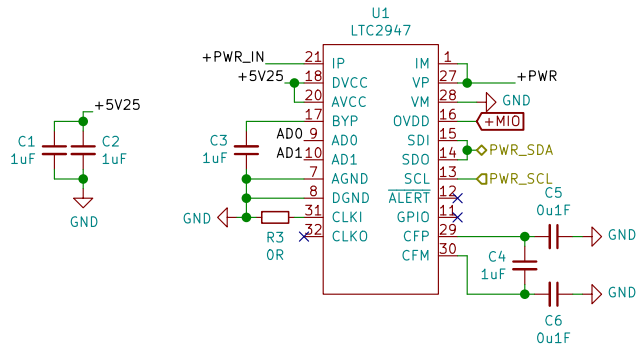

PS I2C addresses:
– 0x5C: HW monitor
– 0x20: USB controller
Sheet: power
File: power.sch
Sheet: audio
File: audio.sch
Sheet: EEG
File: EEG.sch
Sheet: user–interaction
File: user.sch
Sheet: FPGA
File: FPGA.sch
Sheet: clocks
File: clocks.sch
Sheet: SD_DATA
File: SD.sch
Sheet: SD_OS
File: SD.sch
Sheet: ethernet
File: ethernet.sch
PWR_FLAG
State:
– Preliminary schematics: completed
– Layout: to do
– Revised schematic: to do
– Schematic validation: to do
– Layout validation: to do
– BOM optimization: to do
– Physical testing: to do
Note:
– Switch to PAP for Ethernet if Digikey chosen as distributor
Questions:
– Only differential signals? (See EEG sheet)
– Shared SPI bus for EEG & audio?
Designed by Xavier L'Heureux
MIST Lab
Sheet: /
File: mist–eeg.sch
Title: Portiloop
Size: USLetter
Date: 2021–06–07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 1/23



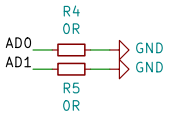


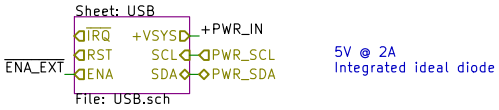
Table 3. I²C Addresses

AD0	AD1	8-BIT ADDRESS BYTE WRITE	8-BIT ADDRESS BYTE READ	7-BIT DEVICE ADDRESS	BINARY DEVICE ADDRESS							
				a6:a0	a6	a5	a4	a3	a2	a1	a0	R/W
L	L	0xB8	0xB9	0x5C	1	0	1	1	1	0	0	1/0
L	H	0xBA	0xBB	0x5D	1	0	1	1	1	0	1	1/0
L	R	0xBC	0xBD	0x5E	1	0	1	1	1	1	0	1/0
R	L	0xC8	0xC9	0x64	1	1	0	0	1	0	0	1/0
R	H	0xCA	0xCB	0x65	1	1	0	0	1	0	1	1/0
R	R	0xCC	0xCD	0x66	1	1	0	0	1	1	0	1/0

Note 10: L: tie to DGND, H: tie to OVDD, R: resistor, connect to DGND with a 100kΩ resistor.

HWMon I2C address

HWMon



5V @ 2A
Integrated ideal diode

USB power

Zynq: (−1 & −2 speed, up to XCZU3EG)

-6 W for max (−2, with GPU, all full speed), -2 W for expected

0.72 V / 0.85 V @ 4 A: (TPS84A20)
- VCCINT (3.090 A)

0.85 V @ 4 A: (TPS84A20)
- VCCINT_IO (0.128 A)
- VCCBRAM (0.069 A)
- VCC_PSINTLP (0.616 A)
- VCC_PSINTFP (1.136 A)
- VCC_PSINTFP_DDR (0.644 A)
- VCC_MGTRAVCC (0.157 A)

1.8V @ 1 A: (TPS84A20)
- VCCAUX (0.091 A)
- VCCAUX_IO (0.108 A)
- VCCO (0.050 A)
- VCCADC (0.008 A)
- VCC_PSAUX (0.122 A)
- VCC_PSADC (0.011 A)
- VCC_PSDDR_PLL (0.026 A)
- VPS_MGTRAVTT (0.034 A)
- SD level shifter x2 (100 mA x2)
- Ethernet PHY (75 mA)
- VDD1 (0.010 A)

1.2V @ 250 mA: (BUCK5)
- VCC_PSPLL (0.002 A)

3V3 V @ 1.75 A (TPS84A20):
- SD card x2, 2.88 W max each

1V0: (TBD)
- Ethernet PHY (108 mA)

2V5: (TBD)
- Ethernet PHY (86 mA)

1V1: (TPS65296)
- VCCO_PSDDR_504 (0.187 A)
- VDD2 (0.322 A)
- VDDQ (0.137 A)

5V0 (clean) @ 50 mA:
- ADS1299 Analog supply
- LTC2947 supply

1V8 (clean) @ 10 mA
- ADAU1777 Analog supply

Unused rails:
VCCINT_VCU => GND
VMGTAVCC, VMGTAVTT, VMGTVCCAUX, VMGTAVTTRCAL => GND

Sequencing

PS:
1 – VCC_PSINTLP
2 – VCC_PSAUX, VCC_PSADC, and VCC_PSPLL
3 – VCCO_PSIO
4 – VCC_PSINTFP and VCC_PSINTFP_DDR
5 – VCC_PSDDR_PLL
6 – VCCO_PSDDR

PL:
1 – VCCINT
2 – VCCINT_IO / VCCBRAM / VCCINT_VCU
3 – VCCAUX / VCCAUX_IO
4 – VCCO

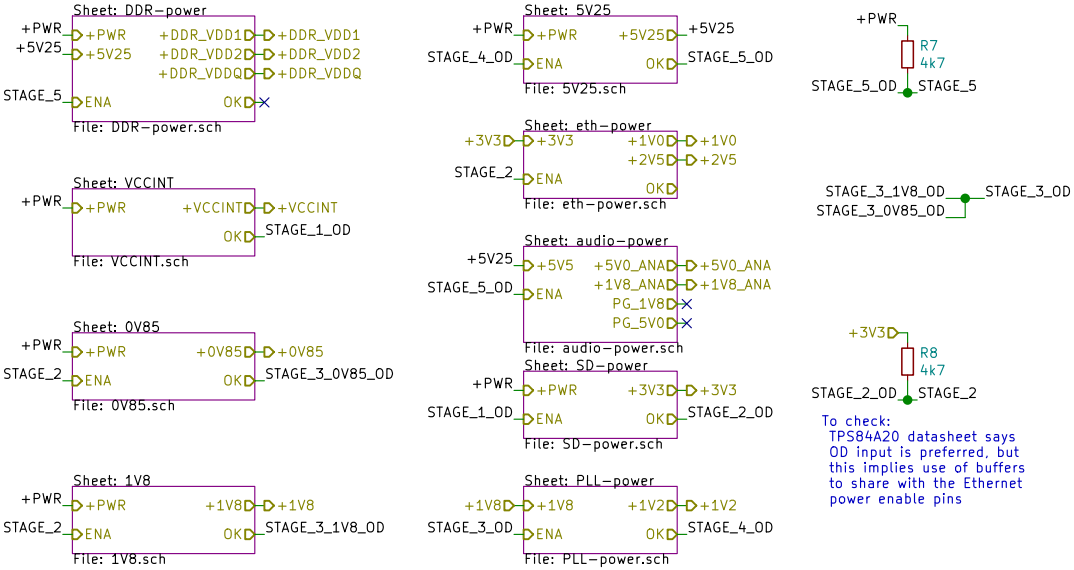
ADC supplies:
1 – 5V25 (intermediate)
2 – 5V & 1V8 (clean)

Ethernet:
1 – 1V8, 1V0 & 2V5

DRAM:
1 – 5V25 (intermediate)
2 – 1V1 & 1V8

Global:
1 – VCCINT
2 – 3.3V
3 – 0.85V, 1.8V (MAIN), 1.0V, 2.5V
4 – 1.2V
5 – 5.25V (intermediate)
6 – 1.8V (clean), 5.0V (clean), 1.1V & 1.8V (DRAM)

External power port & protection



Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/
File: power.sch

Title: Portiloop

Size: USLetter	Date: 2021−06−07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 2/23

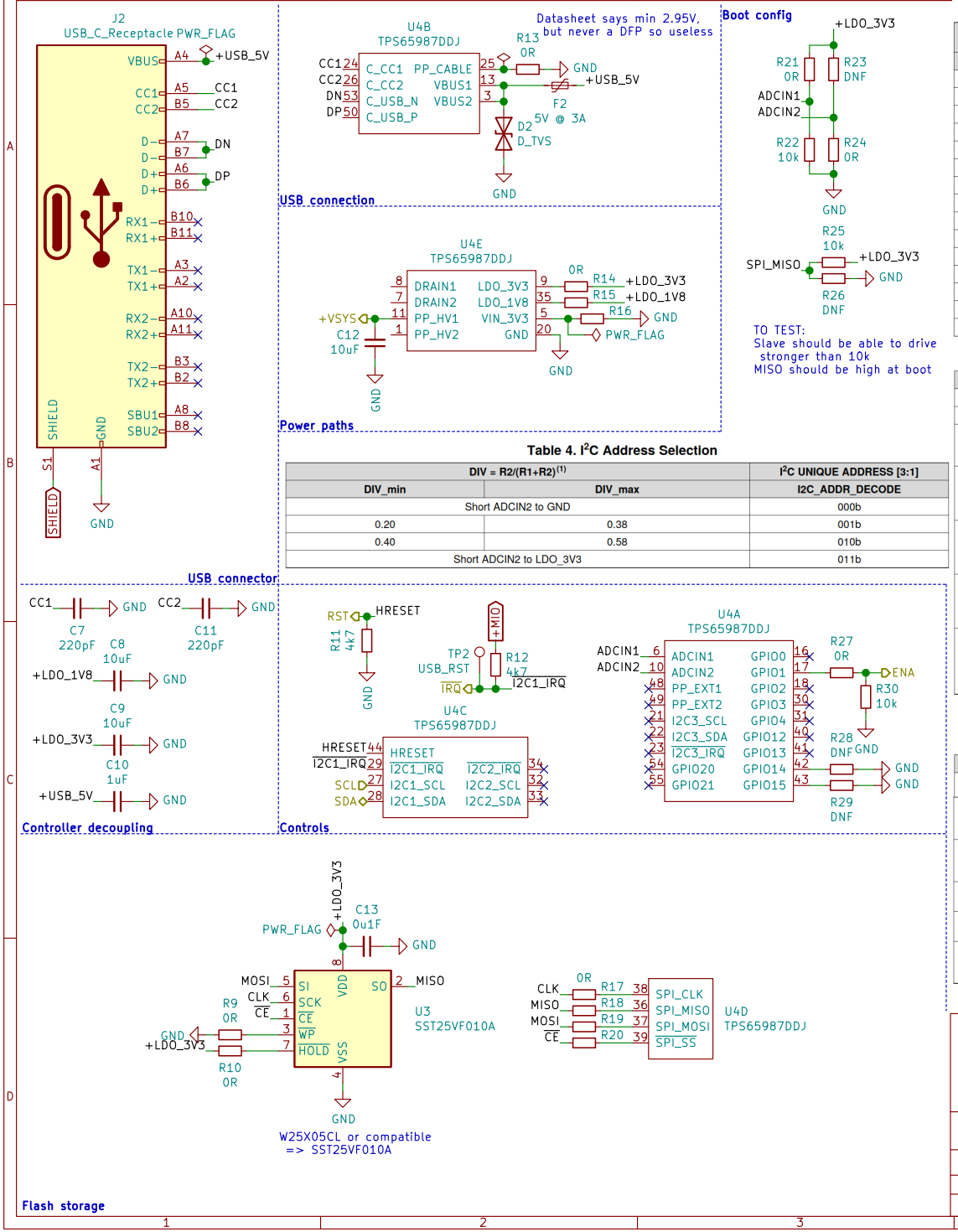


Table 4. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]
DIV_min	DIV_max	I2C_ADDR_DECODE
Short ADCIN2 to GND		000b
0.20	0.38	001b
0.40	0.58	010b
Short ADCIN2 to LDO_3V3		011b

Table 5. Boot Mode Pin Strapping

SPI_MISO	ADCIN1 DIV = R2/(R1+R2)(1)		Dead Battery Mode	Device Configuration
	DIV MIN	DIV MAX		
1	0.00	0.18	BP_NoResponse	Safe Configuration
1	0.20	0.28	BP_WaitFor3V3_Internal	Safe Configuration
1	0.30	0.38	BP_ECWait_Internal	Infinite Wait
1	0.40	0.48	BP_WaitFor3V3_External	Safe Configuration
1	0.50	0.58	BP_ECWait_External	Infinite Wait
1	0.60	1.00	BP_NoWait	Safe Configuration
0	0.10	0.18	BP_NoResponse	Configuration 1
0	0.20	0.28	BP_NoResponse	Configuration 2
0	0.30	0.38	BP_ECWait_Internal	Infinite Wait
0	0.40	0.48	BP_NoWait	Configuration 3
0	0.50	0.58	BP_ECWait_External	Infinite Wait
0	0.60	0.68	BP_NoResponse	Configuration 4
0	0.70	0.78	BP_NoWait	Reserved
0	0.80	0.88	BP_NoResponse	Reserved
0	0.90	1.00	BP_NoWait	Configuration 5

Table 7. Device Default Configurations

Configuration	Description
Safe	Ports disabled, if powered from VBUS operates a legacy sink
Infinite Wait	Device infinitely waits in boot state for configuration information
Configuration 1	DFP only (Internal Switch) 5 V at 3-A Source capability USB Type-C Only (No PD)
Configuration 2	DFP only (Internal Switch) 45-W Source (5/9/15/20-V Output) TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 3	UFP only (Internal Switch) 5-20 V at 0.9 - 3.0-A Sink capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 4	DFP only (Internal Switch) 60-W Source (5/9/15/20-V Output) TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled
Configuration 5	UFP only (External Switch)) 5-20 V at 0.9-3.0-A Sink capability 5 V at 3.0-A Source capability TBT Alternate Modes not enabled DisplayPort Alternate Modes not enabled

Table 6. Dead Battery Configurations

CONFIGURATION	DESCRIPTION
BP_NoResponse	No power switch is enabled and the device does not start-up until VIN_3V3 is present
BP_WaitFor3V3_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.
BP_WaitFor3V3_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.
BP_ECWait_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_ECWait_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device infinitely tries to load configuration.
BP_NoWait	The device continues to start-up and attempts to load configurations while receiving power from VBUS. Once configuration is loaded the appropriate power switch is closed based on the loaded configuration.

Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/USB/
File: USB.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	Rev: 1A
KiCad E.D.A. kicad 5.1.10		Id: 3/23

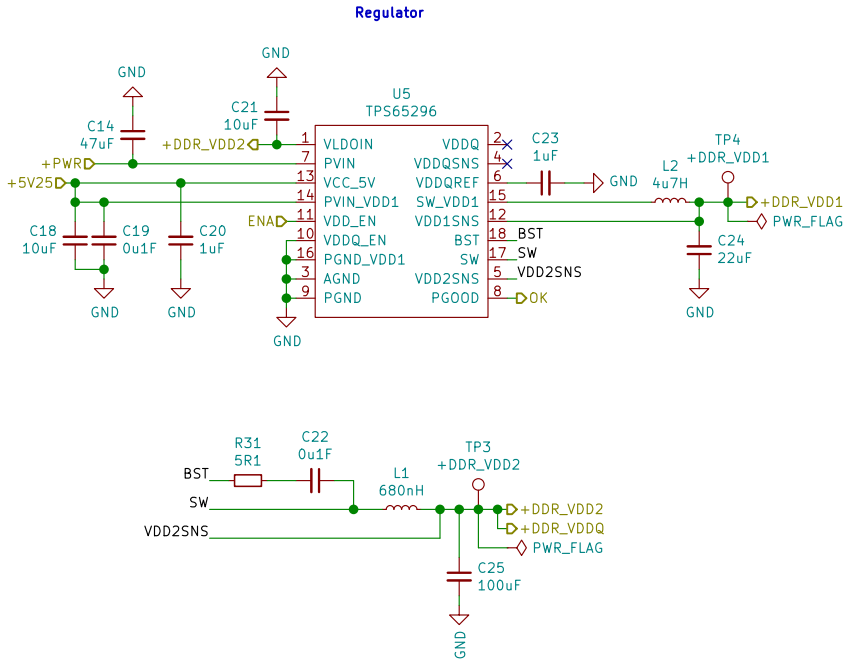
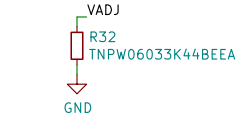


Table 8-3. Recommended Component Values

V_{OUT} (V)	F_{sw} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)
1.1	600	0.68	88	142
	600	0.56	88	142
	600	0.47	88	142
1.8	580	6.8	20	66
	580	4.7	20	66
	580	3.3	20	66

Designed by Xavier L'Heureux
MIST Lab
Sheet: /power/DDR-power/
File: DDR-power.sch
Title: Portiloop
Size: USLetter | Date: 2021-06-07 | **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 | Id: 4/23



$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.6}\right) - 1\right)} \ (k\Omega)$$

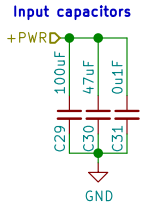
0.72V => 7.15 kΩ
0.85 => 3.432 kΩ

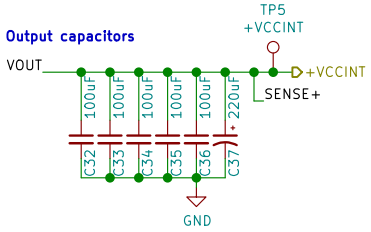
Table 9. Allowable Switching Frequency versus Output Voltage

SWITCHING FREQUENCY (kHz)	PVIN = 12 V			PVIN = 5 V		
	V_{OUT} RANGE (V)			V_{OUT} RANGE (V)		
	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A
200	0.6 - 1.2	0.6 - 1.6	0.6 - 2.0	0.6 - 1.5	0.6 - 2.5	0.6 - 4.3
300	0.8 - 1.9	0.8 - 2.6	0.8 - 3.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
400	1.0 - 2.7	1.0 - 4.0	1.0 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
500	1.3 - 3.8	1.3 - 5.5	1.3 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
600	1.5 - 5.5	1.5 - 5.5	1.5 - 5.5	0.7 - 4.3	0.7 - 4.3	0.7 - 4.3
700	1.8 - 5.5	1.8 - 5.5	1.8 - 5.5	0.8 - 4.3	0.8 - 4.3	0.8 - 4.3
800	2.0 - 5.5	2.0 - 5.5	2.0 - 5.5	0.9 - 4.3	0.9 - 4.3	0.9 - 4.3
900	2.2 - 5.5	2.2 - 5.5	2.2 - 5.5	1.0 - 4.3	1.0 - 4.3	1.0 - 4.3
1000	2.5 - 5.5	2.5 - 5.5	2.5 - 5.5	1.1 - 4.3	1.1 - 4.3	1.1 - 4.3
1100	2.7 - 5.5	2.7 - 5.5	2.7 - 5.5	1.3 - 4.3	1.2 - 4.3	1.2 - 4.3
1200	3.0 - 5.5	3.0 - 5.5	3.0 - 5.5	1.4 - 4.3	1.3 - 4.3	1.3 - 4.3

Voltage output

Clock speed





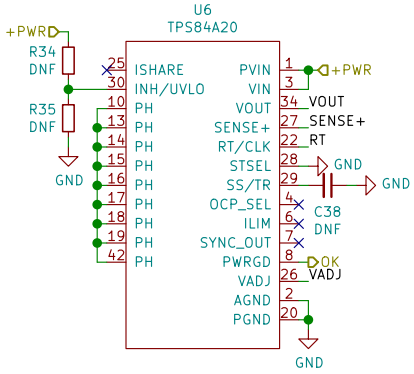


Table 5. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.6	< 0.8	500 µF (1)
0.8	< 1.2	300 µF (1)
1.2	< 3.0	200 µF (1)
3.0	< 4.0	100 µF (1)
4.0	5.5	47 µF ceramic

(1) Minimum required must include at least one 47-µF ceramic capacitor.

Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/VCCINT/
File: VCCINT.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 5/23

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.6}\right) - 1\right)} \ (k\Omega)$$

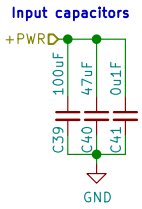
0.85 => 3.432 kΩ

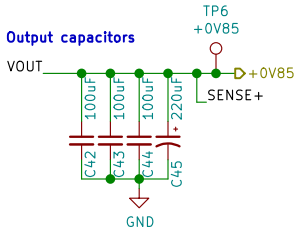
Table 9. Allowable Switching Frequency versus Output Voltage

SWITCHING FREQUENCY (kHz)	PVIN = 12 V			PVIN = 5 V		
	V_{OUT} RANGE (V)			V_{OUT} RANGE (V)		
	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A
200	0.6 - 1.2	0.6 - 1.6	0.6 - 2.0	0.6 - 1.5	0.6 - 2.5	0.6 - 4.3
300	0.8 - 1.9	0.8 - 2.6	0.8 - 3.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
400	1.0 - 2.7	1.0 - 4.0	1.0 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
500	1.3 - 3.8	1.3 - 5.5	1.3 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
600	1.5 - 5.5	1.5 - 5.5	1.5 - 5.5	0.7 - 4.3	0.7 - 4.3	0.7 - 4.3
700	1.8 - 5.5	1.8 - 5.5	1.8 - 5.5	0.8 - 4.3	0.8 - 4.3	0.8 - 4.3
800	2.0 - 5.5	2.0 - 5.5	2.0 - 5.5	0.9 - 4.3	0.9 - 4.3	0.9 - 4.3
900	2.2 - 5.5	2.2 - 5.5	2.2 - 5.5	1.0 - 4.3	1.0 - 4.3	1.0 - 4.3
1000	2.5 - 5.5	2.5 - 5.5	2.5 - 5.5	1.1 - 4.3	1.1 - 4.3	1.1 - 4.3
1100	2.7 - 5.5	2.7 - 5.5	2.7 - 5.5	1.3 - 4.3	1.2 - 4.3	1.2 - 4.3
1200	3.0 - 5.5	3.0 - 5.5	3.0 - 5.5	1.4 - 4.3	1.3 - 4.3	1.3 - 4.3

Voltage output

Clock speed





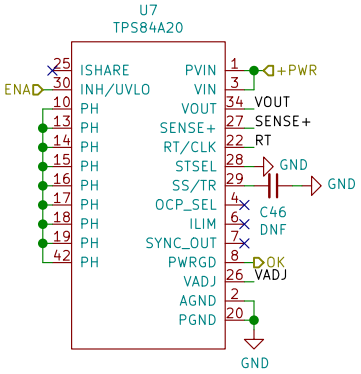


Table 5. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.6	< 0.8	500 µF (1)
0.8	< 1.2	300 µF (1)
1.2	< 3.0	200 µF (1)
3.0	< 4.0	100 µF (1)
4.0	5.5	47 µF ceramic

(1) Minimum required must include at least one 47-µF ceramic capacitor.

Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/0V85/
File: 0V85.sch

Title: Portiloop

Size: USLetter | Date: 2021-06-07 | **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 | Id: 6/23

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.6}\right) - 1\right)} \ (k\Omega)$$

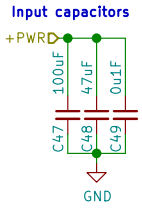
1.8V => 715 Ω

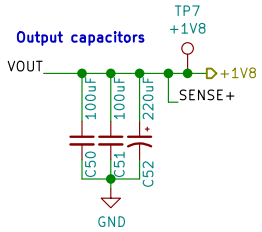
Voltage output

Clock speed

Table 9. Allowable Switching Frequency versus Output Voltage

SWITCHING FREQUENCY (kHz)	PVIN = 12 V			PVIN = 5 V		
	V_{OUT} RANGE (V)			V_{OUT} RANGE (V)		
	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A
200	0.6 - 1.2	0.6 - 1.6	0.6 - 2.0	0.6 - 1.5	0.6 - 2.5	0.6 - 4.3
300	0.8 - 1.9	0.8 - 2.6	0.8 - 3.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
400	1.0 - 2.7	1.0 - 4.0	1.0 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
500	1.3 - 3.8	1.3 - 5.5	1.3 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
600	1.5 - 5.5	1.5 - 5.5	1.5 - 5.5	0.7 - 4.3	0.7 - 4.3	0.7 - 4.3
700	1.8 - 5.5	1.8 - 5.5	1.8 - 5.5	0.8 - 4.3	0.8 - 4.3	0.8 - 4.3
800	2.0 - 5.5	2.0 - 5.5	2.0 - 5.5	0.9 - 4.3	0.9 - 4.3	0.9 - 4.3
900	2.2 - 5.5	2.2 - 5.5	2.2 - 5.5	1.0 - 4.3	1.0 - 4.3	1.0 - 4.3
1000	2.5 - 5.5	2.5 - 5.5	2.5 - 5.5	1.1 - 4.3	1.1 - 4.3	1.1 - 4.3
1100	2.7 - 5.5	2.7 - 5.5	2.7 - 5.5	1.3 - 4.3	1.2 - 4.3	1.2 - 4.3
1200	3.0 - 5.5	3.0 - 5.5	3.0 - 5.5	1.4 - 4.3	1.3 - 4.3	1.3 - 4.3





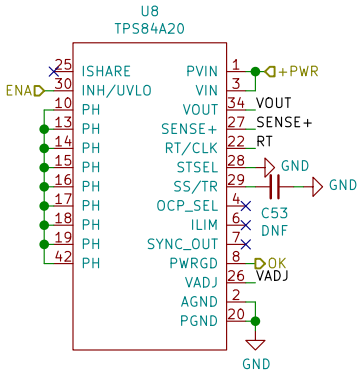


Table 5. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.6	< 0.8	500 µF (1)
0.8	< 1.2	300 µF (1)
1.2	< 3.0	200 µF (1)
3.0	< 4.0	100 µF (1)
4.0	5.5	47 µF ceramic

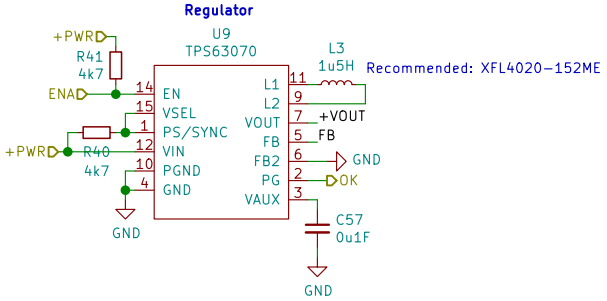
(1) Minimum required must include at least one 47-µF ceramic capacitor.

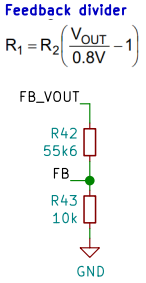
Designed by Xavier L'Heureux
MIST Lab

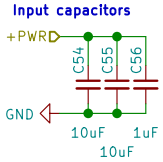
Sheet: /power/1V8/
File: 1V8.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 7/23







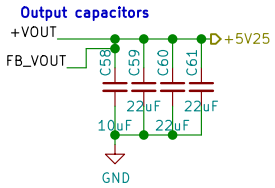


Table 3. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)			
	22	47	68	100
1.0		√	√	√
1.5		√(3)	√	√
2.2			√	√

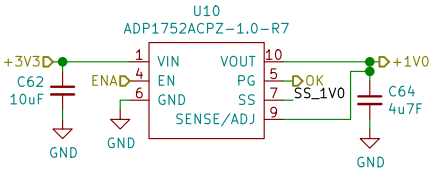
(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
(3) Typical application. Other check marks indicates recommended filter combinations

Designed by Xavier L'Heureux
MIST Lab
Sheet: /power/5V25/
File: 5V25.sch

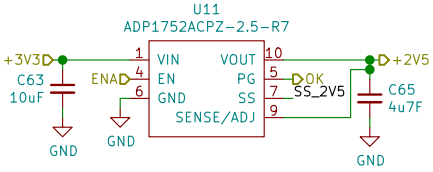
Title: Portiloop

Size: USLetter | Date: 2021-06-07 | **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 | Id: 8/23

1.0V regulator



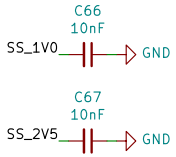
2.5V regulator



Soft-start setting

$$t_{SS} = V_{REF} \times (C_{SS}/I_{SS})$$

where:
t_{SS} is the soft start period.
V_{REF} is the 0.5 V reference voltage.
C_{SS} is the soft start capacitance from SS to GND.
I_{SS} is the current sourced from SS (0.9 µA).



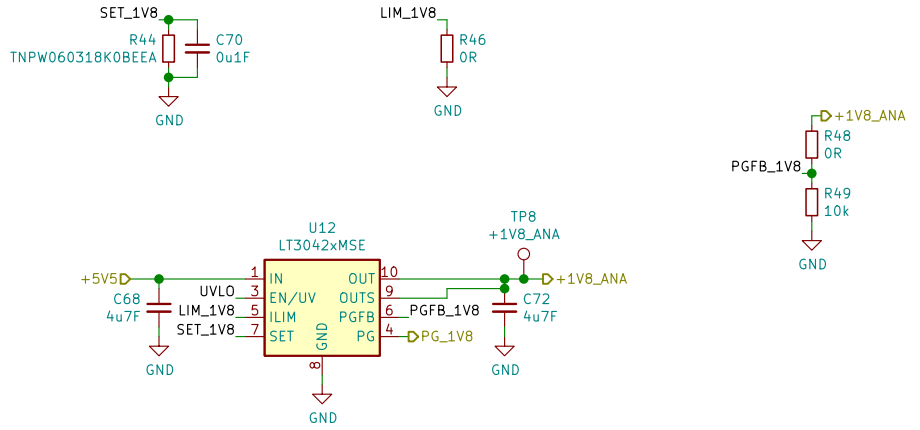
Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/eth-power/
File: eth-power.sch

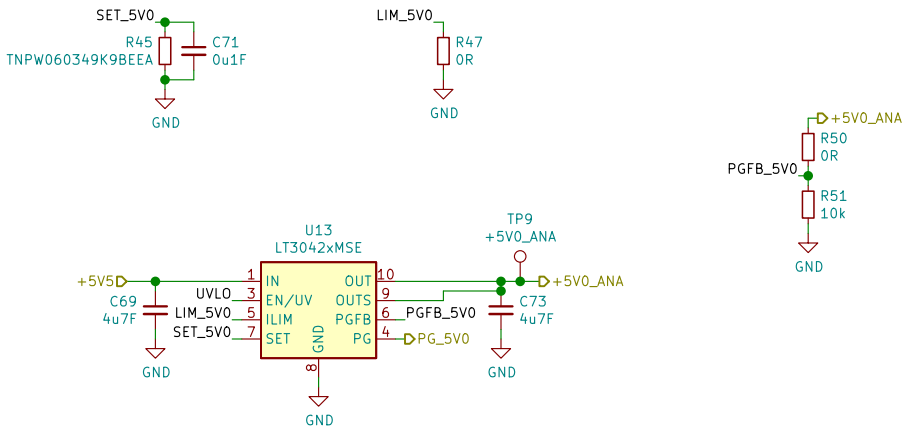
Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 9/23

1V8 (clean regulator)



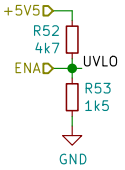
5V0 (clean regulator)



Shared

R_set = Vout / 100µA

ULVO > 1.25V * (R1 / R2 + 1)



Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/audio-power/
File: audio-power.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 10/23

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.6}\right) - 1\right)} \ (k\Omega)$$

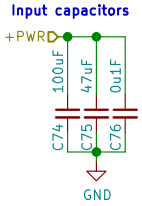
3.3V => 316 Ω

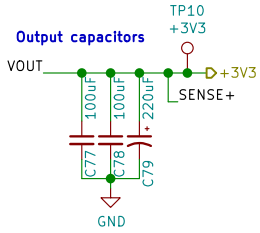
Voltage output

Table 9. Allowable Switching Frequency versus Output Voltage

SWITCHING FREQUENCY (kHz)	PVIN = 12 V			PVIN = 5 V		
	V_{OUT} RANGE (V)			V_{OUT} RANGE (V)		
	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A	$I_{OUT} \le 10$ A	$I_{OUT} \le 9$ A	$I_{OUT} \le 8$ A
200	0.6 - 1.2	0.6 - 1.6	0.6 - 2.0	0.6 - 1.5	0.6 - 2.5	0.6 - 4.3
300	0.8 - 1.9	0.8 - 2.6	0.8 - 3.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
400	1.0 - 2.7	1.0 - 4.0	1.0 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
500	1.3 - 3.8	1.3 - 5.5	1.3 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
600	1.5 - 5.5	1.5 - 5.5	1.5 - 5.5	0.7 - 4.3	0.7 - 4.3	0.7 - 4.3
700	1.8 - 5.5	1.8 - 5.5	1.8 - 5.5	0.8 - 4.3	0.8 - 4.3	0.8 - 4.3
800	2.0 - 5.5	2.0 - 5.5	2.0 - 5.5	0.9 - 4.3	0.9 - 4.3	0.9 - 4.3
900	2.2 - 5.5	2.2 - 5.5	2.2 - 5.5	1.0 - 4.3	1.0 - 4.3	1.0 - 4.3
1000	2.5 - 5.5	2.5 - 5.5	2.5 - 5.5	1.1 - 4.3	1.1 - 4.3	1.1 - 4.3
1100	2.7 - 5.5	2.7 - 5.5	2.7 - 5.5	1.3 - 4.3	1.2 - 4.3	1.2 - 4.3
1200	3.0 - 5.5	3.0 - 5.5	3.0 - 5.5	1.4 - 4.3	1.3 - 4.3	1.3 - 4.3

Clock speed





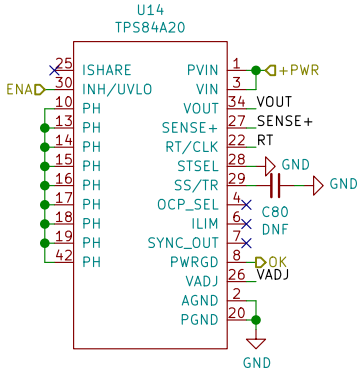


Table 5. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.6	< 0.8	500 µF (1)
0.8	< 1.2	300 µF (1)
1.2	< 3.0	200 µF (1)
3.0	< 4.0	100 µF (1)
4.0	5.5	47 µF ceramic

(1) Minimum required must include at least one 47-µF ceramic capacitor.

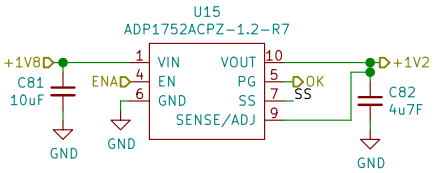
Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/SD-power/
File: SD-power.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 11/23

Regulator

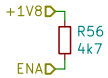


Soft start

$$t_{SS} = V_{REF} \times (C_{SS}/I_{SS})$$

where:
t_{SS} is the soft start period.
V_{REF} is the 0.5 V reference voltage.
C_{SS} is the soft start capacitance from SS to GND.
I_{SS} is the current sourced from SS (0.9 µA).

ENA pullup



Designed by Xavier L'Heureux
MIST Lab

Sheet: /power/PLL-power/
File: PLL-power.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 12/23

SD Card module

http://academy.cba.mit.edu/classes/networking_communications/SD/SD.pdf
https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf#G6.483658

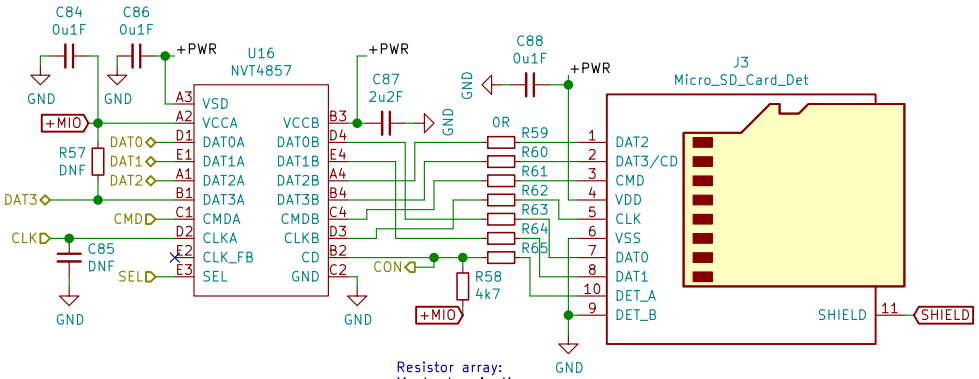
Targetted speed class: UHS-I

Protection against ESD & EMI filter

Needs 1.8V

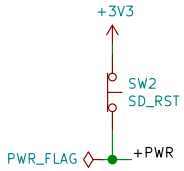
Cases: Push-Push

UHS-I timing diagrams
not available (1000 USD).
try to route under 5 cm
(approx. 300 ps, good enough)



Resistor array:
Maybe termination
resistors required
+ test points

Reset switch



Designed by Xavier L'Heureux
MIST Lab

Sheet: /SD_DATA/
File: SD.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 13/23

SD Card module

http://academy.cba.mit.edu/classes/networking_communications/SD/SD.pdf
https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf#G6.483658

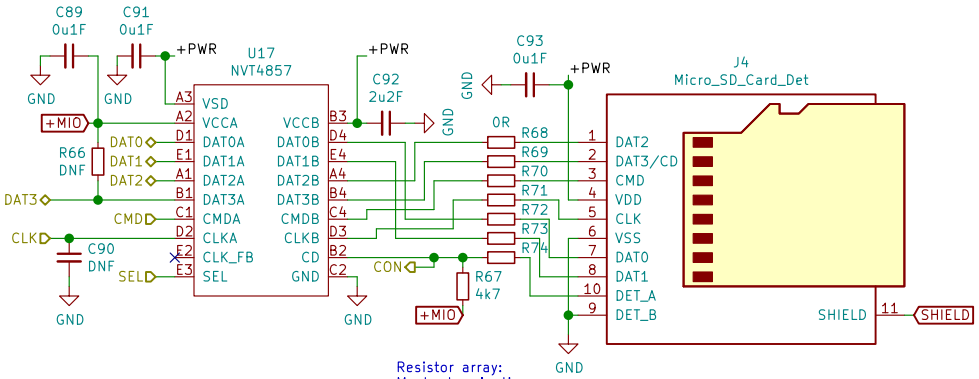
Targetted speed class: UHS-I

Protection against ESD & EMI filter

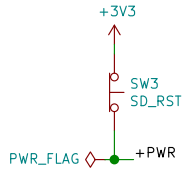
Needs 1.8V

Cases: Push-Push

UHS-I timing diagrams
not available (1000 USD).
try to route under 5 cm
(approx. 300 ps, good enough)



Reset switch

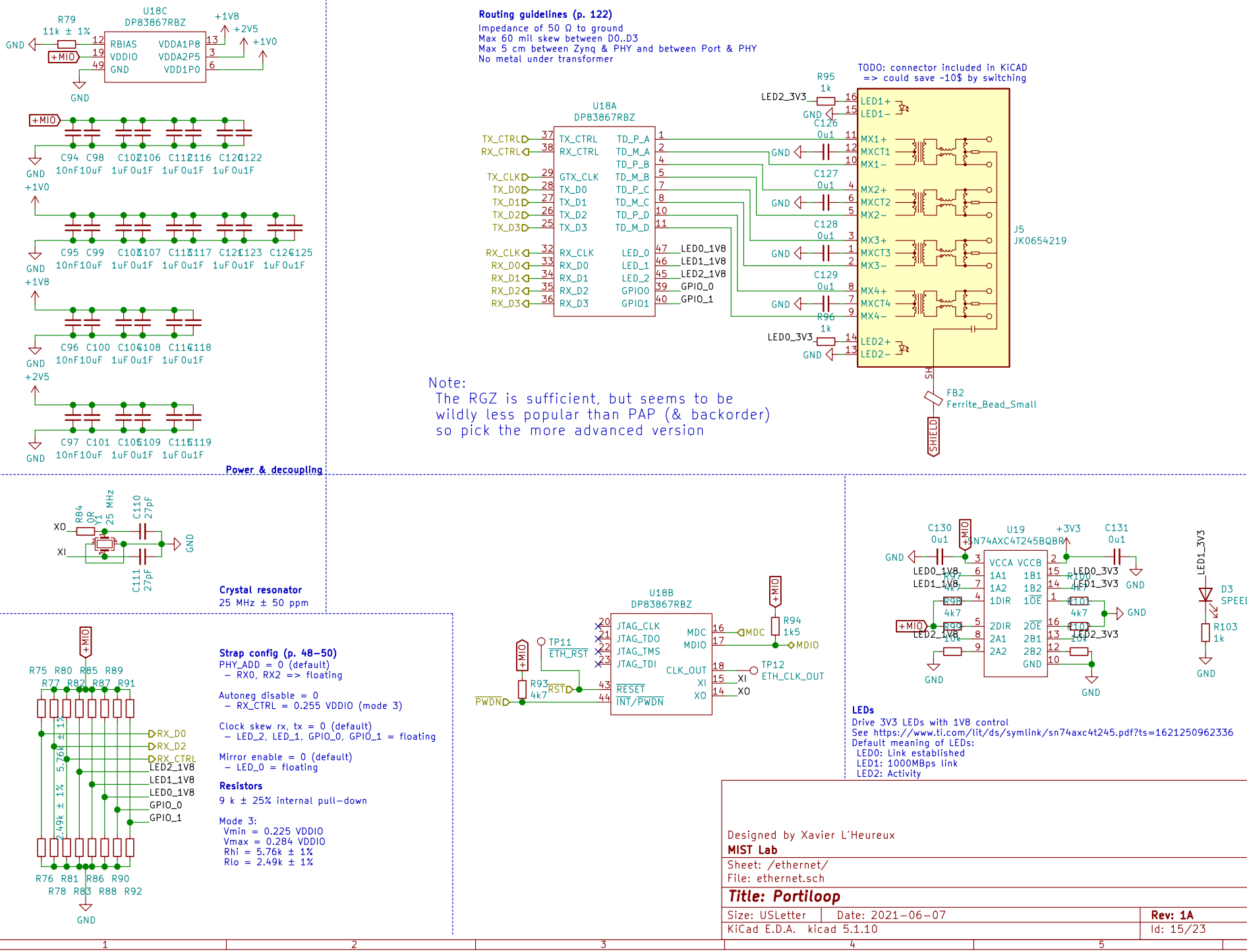


Designed by Xavier L'Heureux
MIST Lab

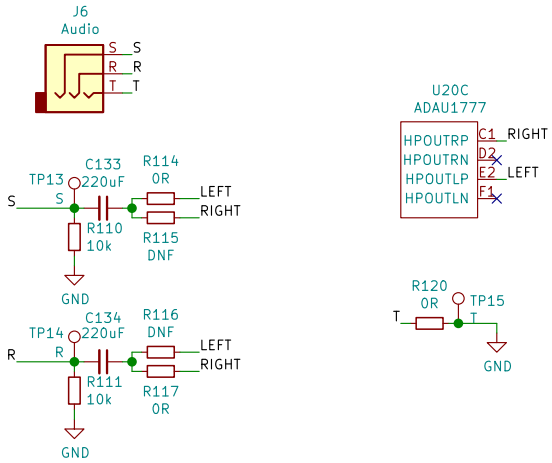
Sheet: /SD_OS/
File: SD.sch

Title: Portiloop

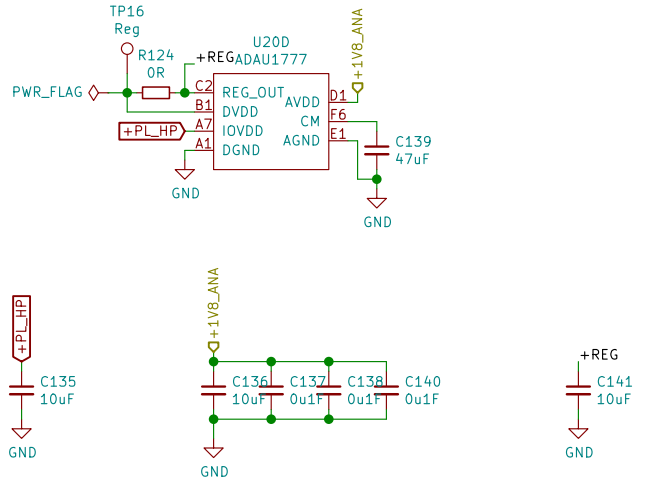
Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 14/23


U18C
DP83867RBZ
R79
11k ± 1%
RBIAS
VDDIO
GND
VDDA1P8
VDDA2P5
VDD1P0
+1V8
+2V5
+1V0
C94 C98 C102 C106 C112 C116 C120 C122
10nF 10uF 1uF 0u1F 1uF 0u1F 1uF 0u1F
C95 C99 C103 C107 C113 C117 C121 C123 C124 C125
C96 C100 C104 C108 C114 C118
C97 C101 C105 C109 C115 C119
Power & decoupling
R84 0R
Y1 25 MHz
C110 27pF
C111 27pF
XO
XI
Crystal resonator
25 MHz ± 50 ppm
U18A
DP83867RBZ
TX_CTRL
RX_CTRL
TX_CLK
TX_D0
TX_D1
TX_D2
TX_D3
RX_CLK
RX_D0
RX_D1
RX_D2
RX_D3
TD_P_A
TD_M_A
TD_P_B
TD_M_B
TD_P_C
TD_M_C
TD_P_D
TD_M_D
GTX_CLK
LED_0
LED_1
LED_2
GPIO0
GPIO1
LED0_1V8
LED1_1V8
LED2_1V8
GPIO_0
GPIO_1
Routing guidelines (p. 122)
Impedance of 50 Ω to ground
Max 60 mil skew between D0..D3
Max 5 cm between Zynq & PHY and between Port & PHY
No metal under transformer
TODO: connector included in KiCAD
=> could save ~10$ by switching
R95 1k
R96 1k
LED2_3V3
LED0_3V3
LED1+
LED1−
LED2+
LED2−
C126 C127 C128 C129 0u1
MX1+
MX1−
MXCT1
MX2+
MX2−
MXCT2
MX3+
MX3−
MXCT3
MX4+
MX4−
MXCT4
J5
JK0654219
SHIELD
FB2
Ferrite_Bead_Small
Note:
The RGZ is sufficient, but seems to be
wildly less popular than PAP (& backorder)
so pick the more advanced version
U18B
DP83867RBZ
JTAG_CLK
JTAG_TDO
JTAG_TMS
JTAG_TDI
RESET
INT/PWDN
MDC
MDIO
CLK_OUT
XI
XO
TP11
ETH_RST
TP12
ETH_CLK_OUT
R93 4k7
R94 1k5
RST
PWDN
+MIO
MDC
MDIO
U19
SN74AXC4T245BQBR
+3V3
C130 C131 0u1
VCCA VCCB
1A1 1B1
1A2 1B2
1DIR 1OE
2DIR 2OE
2A1 2B1
2A2 2B2
R97 R100 R98 R101 R99 R102 4k7
LED0_3V3
LED1_3V3
LED2_3V3
D3
SPEED
R103 1k
LEDs
Drive 3V3 LEDs with 1V8 control
See https://www.ti.com/lit/ds/symlink/sn74axc4t245.pdf?ts=1621250962336
Default meaning of LEDs:
LED0: Link established
LED1: 1000MBps link
LED2: Activity
R75 R80 R85 R89
R77 R82 R87 R91
R76 R81 R86 R90
R78 R83 R88 R92
2.49k ± 1%
5.76k ± 1%
RX_D0
RX_D2
RX_CTRL
LED2_1V8
LED1_1V8
LED0_1V8
GPIO_0
GPIO_1
Strap config (p. 48–50)
PHY_ADD = 0 (default)
– RX0, RX2 => floating
Autoneg disable = 0
– RX_CTRL = 0.255 VDDIO (mode 3)
Clock skew rx, tx = 0 (default)
– LED_2, LED_1, GPIO_0, GPIO_1 = floating
Mirror enable = 0 (default)
– LED_0 = floating
Resistors
9 k ± 25% internal pull-down
Mode 3:
Vmin = 0.225 VDDIO
Vmax = 0.284 VDDIO
Rhi = 5.76k ± 1%
Rlo = 2.49k ± 1%
Designed by Xavier L'Heureux
MIST Lab
Sheet: /ethernet/
File: ethernet.sch
Title: Portiloop
Size: USLetter
Date: 2021-06-07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 15/23

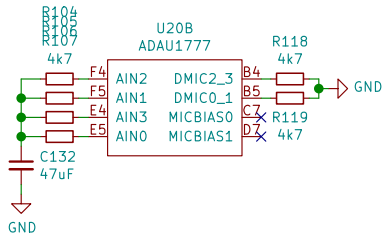
According to wikipedia:
T: Left
R: Right
S: GND



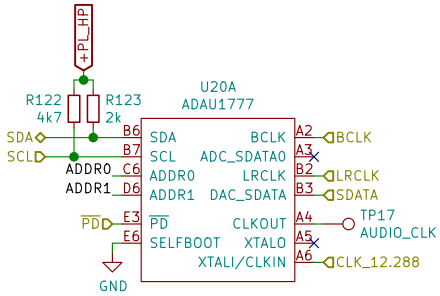
Jack output



Power & decoupling



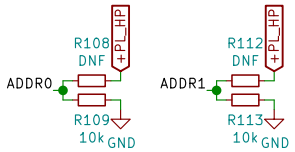
Mic Input – Unused



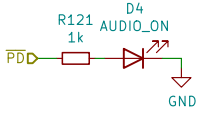
Digital IOs

Table 21. I²C Address Format

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	ADDR1	ADDR0



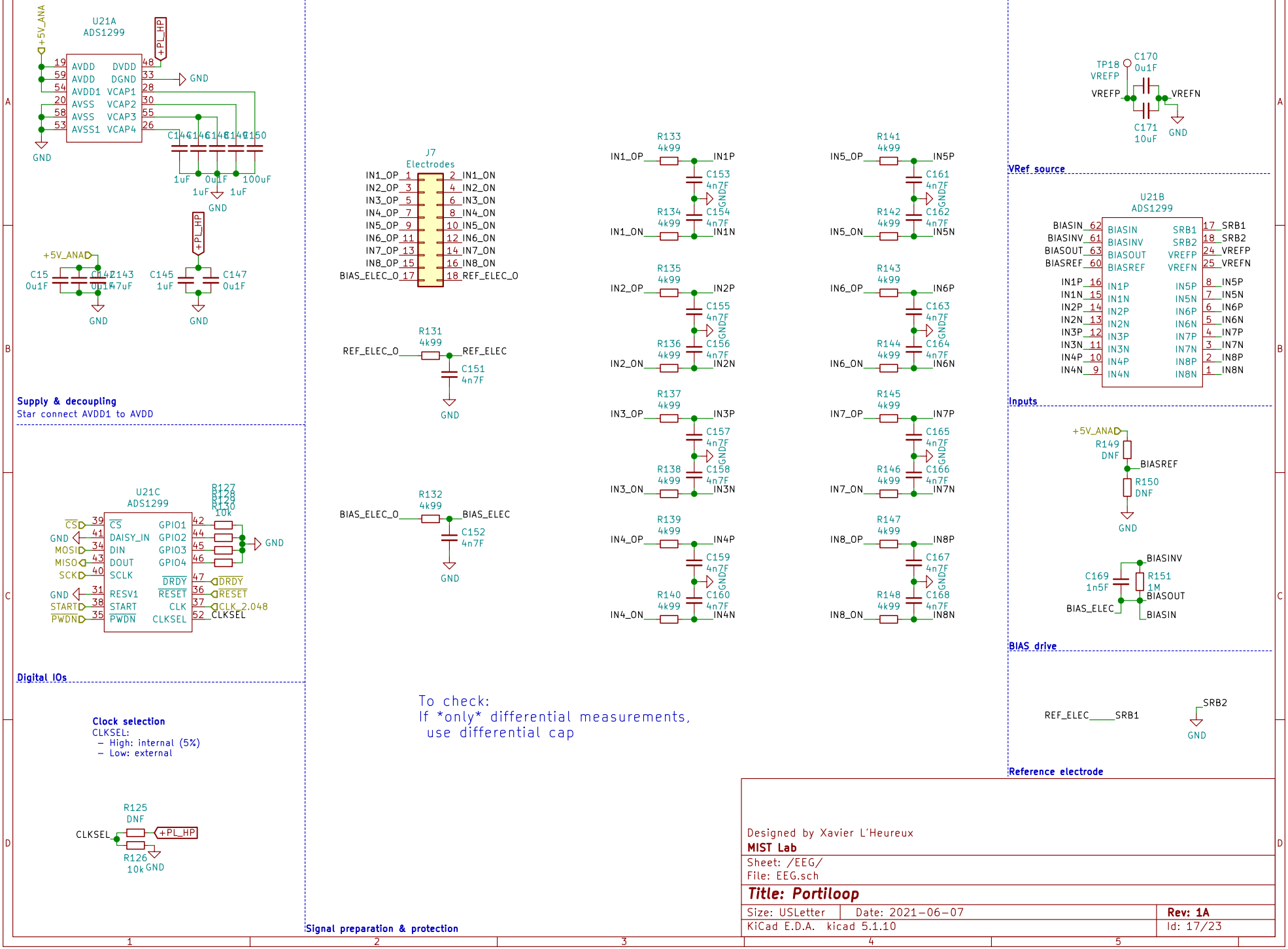
I2C address

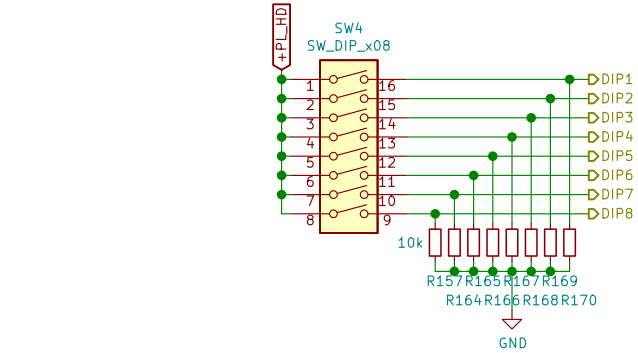


Feedback LED

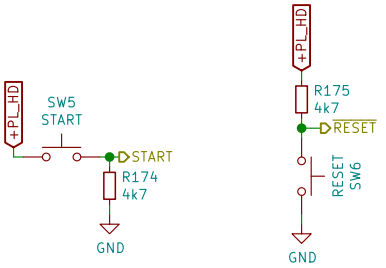
Designed by Xavier L'Heureux
MIST Lab

Sheet: /audio/		
File: audio.sch		
Title: Portiloop		
Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 16/23

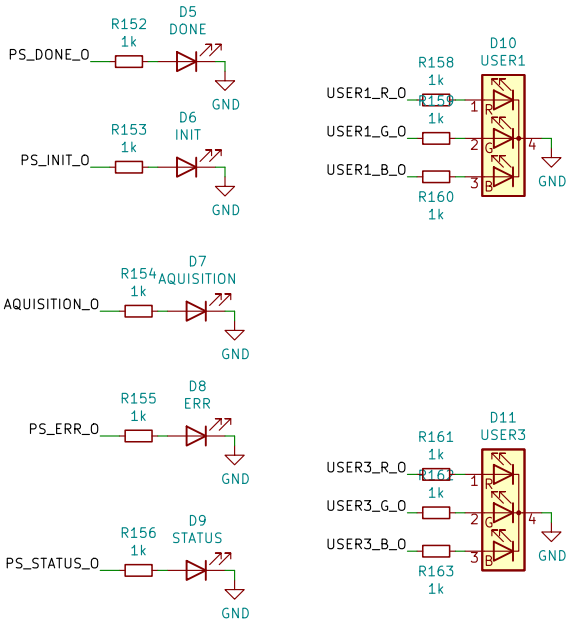

U21A
ADS1299
+5V_ANA
+PL_HP
GND
AVDD
AVDD
AVDD1
AVSS
AVSS
AVSS1
DVDD
DGND
VCAP1
VCAP2
VCAP3
VCAP4
C144 1uF
C146 0u1F
C148 1uF
C149 1uF
C150 100uF
C15 0u1F
C142 0u1F
C143 4u7F
C145 1uF
C147 0u1F
Supply & decoupling
Star connect AVDD1 to AVDD
U21C
ADS1299
R127
R128
R129
R130
10k
CS
DAISY_IN
MOSI
MISO
SCK
RESV1
START
PWDN
GPIO1
GPIO2
GPIO3
GPIO4
DRDY
RESET
CLK
CLKSEL
CLK_2.048
Digital IOs
Clock selection
CLKSEL:
– High: internal (5%)
– Low: external
R125
DNF
R126
10k
J7
Electrodes
IN1_OP
IN2_OP
IN3_OP
IN4_OP
IN5_OP
IN6_OP
IN7_OP
IN8_OP
BIAS_ELEC_O
IN1_ON
IN2_ON
IN3_ON
IN4_ON
IN5_ON
IN6_ON
IN7_ON
IN8_ON
REF_ELEC_O
R131
4k99
REF_ELEC
C151
4n7F
R132
BIAS_ELEC
C152
R133
C153
C154
IN1P
IN1N
R135
C155
C156
IN2P
IN2N
R137
C157
C158
IN3P
IN3N
R139
C159
C160
IN4P
IN4N
R141
C161
C162
IN5P
IN5N
R143
C163
C164
IN6P
IN6N
R145
C165
C166
IN7P
IN7N
R147
C167
C168
IN8P
IN8N
To check:
If *only* differential measurements,
use differential cap
Signal preparation & protection
TP18
VREFP
C170
0u1F
C171
10uF
VREFN
VRef source
U21B
ADS1299
BIASIN
BIASINV
BIASOUT
BIASREF
SRB1
SRB2
VREFP
VREFN
Inputs
R149
DNF
R150
DNF
BIASREF
C169
1n5F
R151
1M
BIASINV
BIASOUT
BIAS_ELEC
BIAS drive
REF_ELEC
SRB1
SRB2
Reference electrode
Designed by Xavier L'Heureux
MIST Lab
Sheet: /EEG/
File: EEG.sch
Title: Portiloop
Size: USLetter
Date: 2021-06-07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 17/23

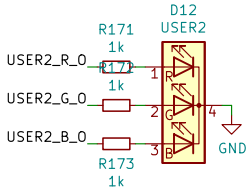


Configuration DIP switches

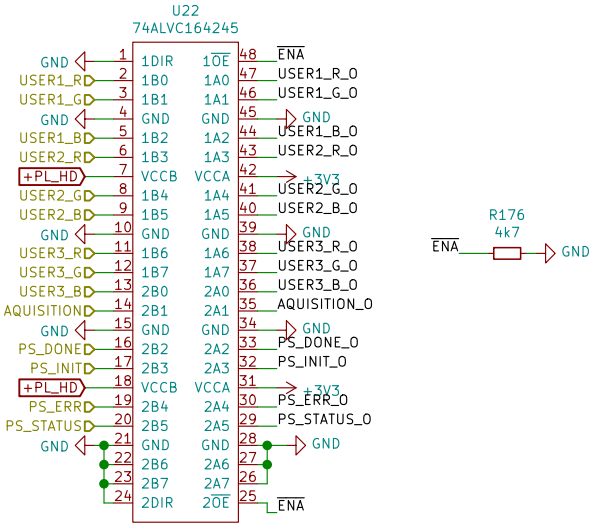


Pushbuttons





LEDs



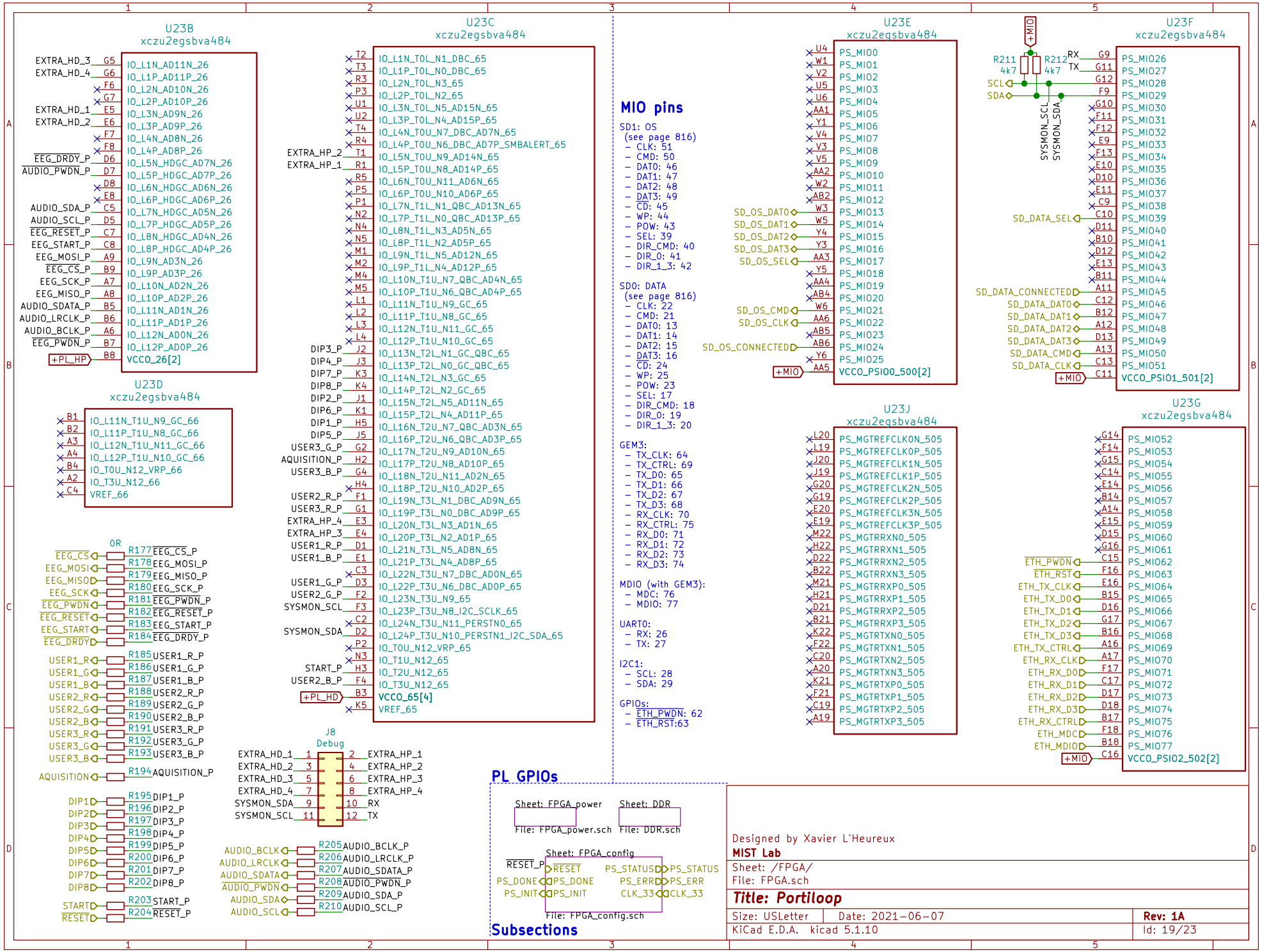
Level shifting (drive LEDs)

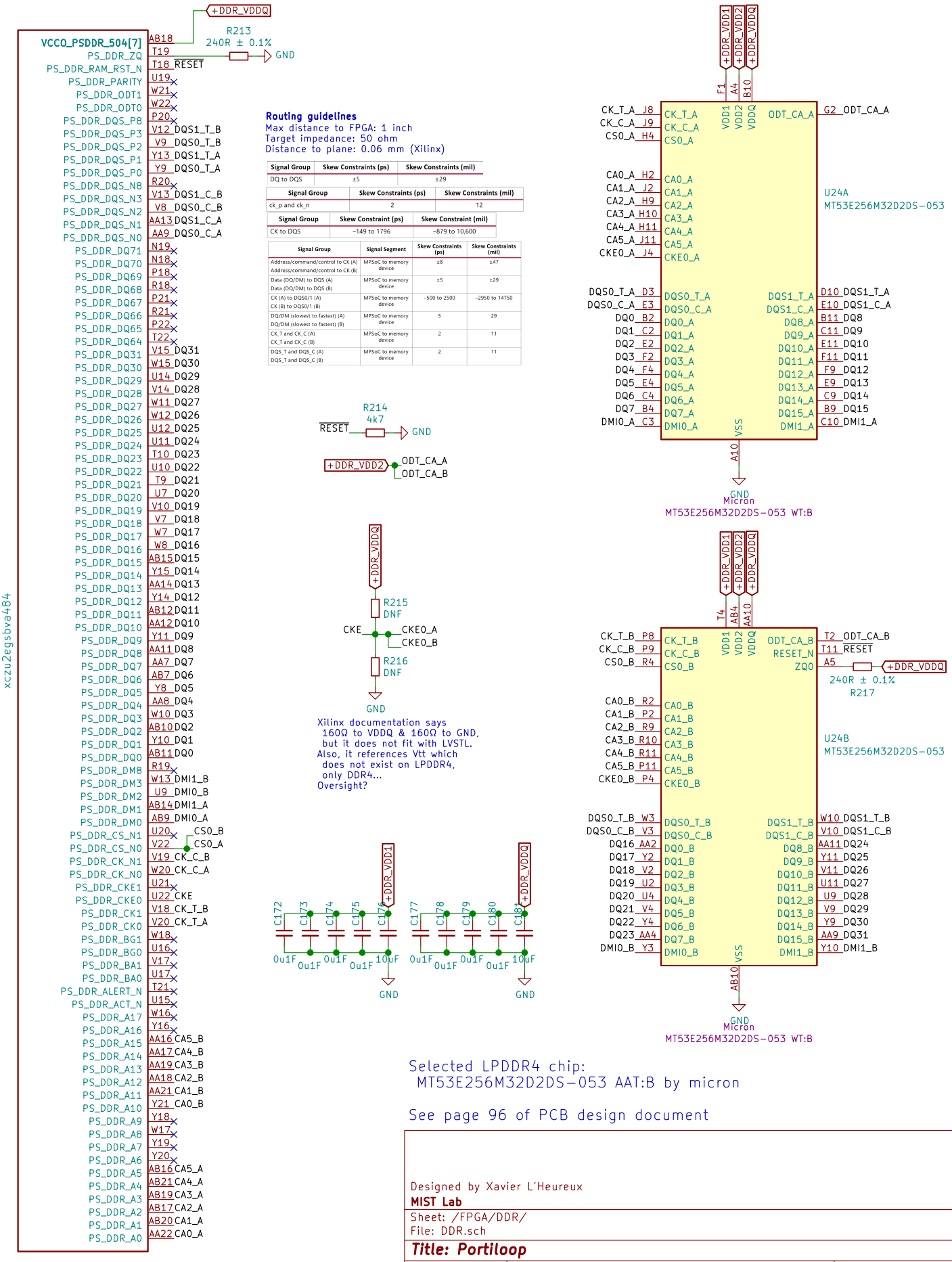
Designed by Xavier L'Heureux
MIST Lab

Sheet: /user-interaction/
File: user.sch

Title: Portiloop

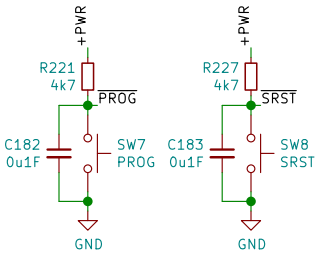
Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 18/23


U23B
xczu2egsbva484
EXTRA_HD_3 G5
EXTRA_HD_4 G6
F6
G7
EXTRA_HD_1 E5
EXTRA_HD_2 E6
F7
F8
EEG_DRDY_P D6
AUDIO_PWDN_P D7
D8
E8
AUDIO_SDA_P C5
AUDIO_SCL_P D5
EEG_RESET_P C7
EEG_START_P C8
EEG_MOSI_P A9
EEG_CS_P B9
EEG_SCK_P A7
EEG_MISO_P A8
AUDIO_SDATA_P B5
AUDIO_LRCLK_P B6
AUDIO_BCLK_P A6
EEG_PWDN_P B7
+PL_HP B8
IO_L1N_AD11N_26
IO_L1P_AD11P_26
IO_L2N_AD10N_26
IO_L2P_AD10P_26
IO_L3N_AD9N_26
IO_L3P_AD9P_26
IO_L4N_AD8N_26
IO_L4P_AD8P_26
IO_L5N_HDGC_AD7N_26
IO_L5P_HDGC_AD7P_26
IO_L6N_HDGC_AD6N_26
IO_L6P_HDGC_AD6P_26
IO_L7N_HDGC_AD5N_26
IO_L7P_HDGC_AD5P_26
IO_L8N_HDGC_AD4N_26
IO_L8P_HDGC_AD4P_26
IO_L9N_AD3N_26
IO_L9P_AD3P_26
IO_L10N_AD2N_26
IO_L10P_AD2P_26
IO_L11N_AD1N_26
IO_L11P_AD1P_26
IO_L12N_AD0N_26
IO_L12P_AD0P_26
VCCO_26[2]
U23D
xczu2egsbva484
B1 IO_L11N_T1U_N9_GC_66
B2 IO_L11P_T1U_N8_GC_66
A3 IO_L12N_T1U_N11_GC_66
A4 IO_L12P_T1U_N10_GC_66
B4 IO_T0U_N12_VRP_66
A2 IO_T3U_N12_66
C4 VREF_66
U23C
xczu2egsbva484
T2 IO_L1N_T0L_N1_DBC_65
T3 IO_L1P_T0L_N0_DBC_65
R3 IO_L2N_T0L_N3_65
P3 IO_L2P_T0L_N2_65
U1 IO_L3N_T0L_N5_AD15N_65
U2 IO_L3P_T0L_N4_AD15P_65
T4 IO_L4N_T0U_N7_DBC_AD7N_65
R4 IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65
EXTRA_HP_2 T1 IO_L5N_T0U_N9_AD14N_65
EXTRA_HP_1 R1 IO_L5P_T0U_N8_AD14P_65
R5 IO_L6N_T0U_N11_AD6N_65
P5 IO_L6P_T0U_N10_AD6P_65
P1 IO_L7N_T1L_N1_QBC_AD13N_65
N2 IO_L7P_T1L_N0_QBC_AD13P_65
N4 IO_L8N_T1L_N3_AD5N_65
N5 IO_L8P_T1L_N2_AD5P_65
M1 IO_L9N_T1L_N5_AD12N_65
M2 IO_L9P_T1L_N4_AD12P_65
M4 IO_L10N_T1U_N7_QBC_AD4N_65
M5 IO_L10P_T1U_N6_QBC_AD4P_65
L1 IO_L11N_T1U_N9_GC_65
L2 IO_L11P_T1U_N8_GC_65
L3 IO_L12N_T1U_N11_GC_65
L4 IO_L12P_T1U_N10_GC_65
DIP3_P J2 IO_L13N_T2L_N1_GC_QBC_65
DIP4_P J3 IO_L13P_T2L_N0_GC_QBC_65
DIP7_P K3 IO_L14N_T2L_N3_GC_65
DIP8_P K4 IO_L14P_T2L_N2_GC_65
DIP2_P J1 IO_L15N_T2L_N5_AD11N_65
DIP6_P K1 IO_L15P_T2L_N4_AD11P_65
DIP1_P H5 IO_L16N_T2U_N7_QBC_AD3N_65
DIP5_P J5 IO_L16P_T2U_N6_QBC_AD3P_65
USER3_G_P G2 IO_L17N_T2U_N9_AD10N_65
AQUISITION_P H2 IO_L17P_T2U_N8_AD10P_65
USER3_B_P G4 IO_L18N_T2U_N11_AD2N_65
H4 IO_L18P_T2U_N10_AD2P_65
USER2_R_P F1 IO_L19N_T3L_N1_DBC_AD9N_65
USER3_R_P G1 IO_L19P_T3L_N0_DBC_AD9P_65
EXTRA_HP_4 E3 IO_L20N_T3L_N3_AD1N_65
EXTRA_HP_3 E4 IO_L20P_T3L_N2_AD1P_65
USER1_R_P D1 IO_L21N_T3L_N5_AD8N_65
USER1_B_P E1 IO_L21P_T3L_N4_AD8P_65
C3 IO_L22N_T3U_N7_DBC_AD0N_65
USER1_G_P D3 IO_L22P_T3U_N6_DBC_AD0P_65
USER2_G_P F2 IO_L23N_T3U_N9_65
SYSMON_SCL F3 IO_L23P_T3U_N8_I2C_SCLK_65
C2 IO_L24N_T3U_N11_PERSTN0_65
SYSMON_SDA D2 IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65
P2 IO_T0U_N12_VRP_65
N3 IO_T1U_N12_65
START_P H3 IO_T2U_N12_65
USER2_B_P F4 IO_T3U_N12_65
+PL_HD B3 VCCO_65[4]
K5 VREF_65
MIO pins
SD1: OS
(see page 816)
– CLK: 51
– CMD: 50
– DAT0: 46
– DAT1: 47
– DAT2: 48
– DAT3: 49
– CD: 45
– WP: 44
– POW: 43
– SEL: 39
– DIR_CMD: 40
– DIR_0: 41
– DIR_1_3: 42
SD0: DATA
(see page 816)
– CLK: 22
– CMD: 21
– DAT0: 13
– DAT1: 14
– DAT2: 15
– DAT3: 16
– CD: 24
– WP: 25
– POW: 23
– SEL: 17
– DIR_CMD: 18
– DIR_0: 19
– DIR_1_3: 20
GEM3:
– TX_CLK: 64
– TX_CTRL: 69
– TX_D0: 65
– TX_D1: 66
– TX_D2: 67
– TX_D3: 68
– RX_CLK: 70
– RX_CTRL: 75
– RX_D0: 71
– RX_D1: 72
– RX_D2: 73
– RX_D3: 74
MDIO (with GEM3):
– MDC: 76
– MDIO: 77
UART0:
– RX: 26
– TX: 27
I2C1:
– SCL: 28
– SDA: 29
GPIOs:
– ETH_PWDN: 62
– ETH_RST:63
U23E
xczu2egsbva484
U4 PS_MIO0
W1 PS_MIO1
V2 PS_MIO2
U5 PS_MIO3
U6 PS_MIO4
AA1 PS_MIO5
Y1 PS_MIO6
V4 PS_MIO7
V3 PS_MIO8
V5 PS_MIO9
AA2 PS_MIO10
W2 PS_MIO11
AB2 PS_MIO12
SD_OS_DAT0 W3 PS_MIO13
SD_OS_DAT1 W5 PS_MIO14
SD_OS_DAT2 Y4 PS_MIO15
SD_OS_DAT3 Y3 PS_MIO16
SD_OS_SEL AA3 PS_MIO17
Y5 PS_MIO18
AA4 PS_MIO19
AB4 PS_MIO20
SD_OS_CMD W6 PS_MIO21
SD_OS_CLK AA6 PS_MIO22
AB5 PS_MIO23
SD_OS_CONNECTED AB6 PS_MIO24
Y6 PS_MIO25
+MIO AA5 VCCO_PSIO0_500[2]
U23J
xczu2egsbva484
L20 PS_MGTREFCLK0N_505
L19 PS_MGTREFCLK0P_505
J20 PS_MGTREFCLK1N_505
J19 PS_MGTREFCLK1P_505
G20 PS_MGTREFCLK2N_505
G19 PS_MGTREFCLK2P_505
E20 PS_MGTREFCLK3N_505
E19 PS_MGTREFCLK3P_505
M22 PS_MGTRRXN0_505
H22 PS_MGTRRXN1_505
D22 PS_MGTRRXN2_505
B22 PS_MGTRRXN3_505
M21 PS_MGTRRXP0_505
H21 PS_MGTRRXP1_505
D21 PS_MGTRRXP2_505
B21 PS_MGTRRXP3_505
K22 PS_MGTRTXN0_505
F22 PS_MGTRTXN1_505
C20 PS_MGTRTXN2_505
A20 PS_MGTRTXN3_505
K21 PS_MGTRTXP0_505
F21 PS_MGTRTXP1_505
C19 PS_MGTRTXP2_505
A19 PS_MGTRTXP3_505
+MIO
R211 4k7
R212 4k7
SCL
SDA
SYSMON_SCL
SYSMON_SDA
RX G9
TX G11
G12
F9
G10 PS_MIO26
F11 PS_MIO27
F12 PS_MIO28
E9 PS_MIO29
F13 PS_MIO30
E10 PS_MIO31
D10 PS_MIO32
E11 PS_MIO33
C9 PS_MIO34
SD_DATA_SEL C10 PS_MIO35
D11 PS_MIO36
B10 PS_MIO37
D12 PS_MIO38
E13 PS_MIO39
B11 PS_MIO40
SD_DATA_CONNECTED A11 PS_MIO41
SD_DATA_DAT0 C12 PS_MIO42
SD_DATA_DAT1 B12 PS_MIO43
SD_DATA_DAT2 A12 PS_MIO44
SD_DATA_DAT3 D13 PS_MIO45
SD_DATA_CMD A13 PS_MIO46
SD_DATA_CLK C13 PS_MIO47
+MIO C11 VCCO_PSIO1_501[2]
U23F
xczu2egsbva484
U23G
xczu2egsbva484
G14 PS_MIO52
F14 PS_MIO53
G15 PS_MIO54
C14 PS_MIO55
E14 PS_MIO56
B14 PS_MIO57
A14 PS_MIO58
E15 PS_MIO59
D15 PS_MIO60
G16 PS_MIO61
ETH_PWDN C15 PS_MIO62
ETH_RST F16 PS_MIO63
ETH_TX_CLK E16 PS_MIO64
ETH_TX_D0 B15 PS_MIO65
ETH_TX_D1 D16 PS_MIO66
ETH_TX_D2 G17 PS_MIO67
ETH_TX_D3 B16 PS_MIO68
ETH_TX_CTRL A16 PS_MIO69
ETH_RX_CLK A17 PS_MIO70
ETH_RX_D0 F17 PS_MIO71
ETH_RX_D1 C17 PS_MIO72
ETH_RX_D2 D17 PS_MIO73
ETH_RX_D3 D18 PS_MIO74
ETH_RX_CTRL B17 PS_MIO75
ETH_MDC F18 PS_MIO76
ETH_MDIO B18 PS_MIO77
+MIO C16 VCCO_PSIO2_502[2]
0R
EEG_CS R177 EEG_CS_P
EEG_MOSI R178 EEG_MOSI_P
EEG_MISO R179 EEG_MISO_P
EEG_SCK R180 EEG_SCK_P
EEG_PWDN R181 EEG_PWDN_P
EEG_RESET R182 EEG_RESET_P
EEG_START R183 EEG_START_P
EEG_DRDY R184 EEG_DRDY_P
USER1_R R185 USER1_R_P
USER1_G R186 USER1_G_P
USER1_B R187 USER1_B_P
USER2_R R188 USER2_R_P
USER2_G R189 USER2_G_P
USER2_B R190 USER2_B_P
USER3_R R191 USER3_R_P
USER3_G R192 USER3_G_P
USER3_B R193 USER3_B_P
AQUISITION R194 AQUISITION_P
DIP1 R195 DIP1_P
DIP2 R196 DIP2_P
DIP3 R197 DIP3_P
DIP4 R198 DIP4_P
DIP5 R199 DIP5_P
DIP6 R200 DIP6_P
DIP7 R201 DIP7_P
DIP8 R202 DIP8_P
START R203 START_P
RESET R204 RESET_P
J8
Debug
EXTRA_HD_1 1 2 EXTRA_HP_1
EXTRA_HD_2 3 4 EXTRA_HP_2
EXTRA_HD_3 5 6 EXTRA_HP_3
EXTRA_HD_4 7 8 EXTRA_HP_4
SYSMON_SDA 9 10 RX
SYSMON_SCL 11 12 TX
AUDIO_BCLK R205 AUDIO_BCLK_P
AUDIO_LRCLK R206 AUDIO_LRCLK_P
AUDIO_SDATA R207 AUDIO_SDATA_P
AUDIO_PWDN R208 AUDIO_PWDN_P
AUDIO_SDA R209 AUDIO_SDA_P
AUDIO_SCL R210 AUDIO_SCL_P
PL GPIOs
Sheet: FPGA_power
File: FPGA_power.sch
Sheet: DDR
File: DDR.sch
Sheet: FPGA_config
RESET_P
RESET
PS_STATUS
PS_DONE
PS_ERR
PS_INIT
CLK_33
File: FPGA_config.sch
Subsections
Designed by Xavier L'Heureux
MIST Lab
Sheet: /FPGA/
File: FPGA.sch
Title: Portiloop
Size: USLetter
Date: 2021-06-07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 19/23

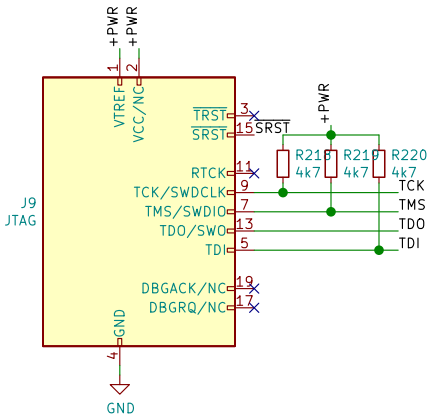

U23I
xczu2egsbva484
VCCO_PSDDR_504[7]
PS_DDR_ZQ
PS_DDR_RAM_RST_N
PS_DDR_PARITY
PS_DDR_ODT1
PS_DDR_ODT0
PS_DDR_DQS_P8
PS_DDR_DQS_P3
PS_DDR_DQS_P2
PS_DDR_DQS_P1
PS_DDR_DQS_P0
PS_DDR_DQS_N8
PS_DDR_DQS_N3
PS_DDR_DQS_N2
PS_DDR_DQS_N1
PS_DDR_DQS_N0
PS_DDR_DQ71
PS_DDR_DQ70
PS_DDR_DQ69
PS_DDR_DQ68
PS_DDR_DQ67
PS_DDR_DQ66
PS_DDR_DQ65
PS_DDR_DQ64
PS_DDR_DQ31
PS_DDR_DQ30
PS_DDR_DQ29
PS_DDR_DQ28
PS_DDR_DQ27
PS_DDR_DQ26
PS_DDR_DQ25
PS_DDR_DQ24
PS_DDR_DQ23
PS_DDR_DQ22
PS_DDR_DQ21
PS_DDR_DQ20
PS_DDR_DQ19
PS_DDR_DQ18
PS_DDR_DQ17
PS_DDR_DQ16
PS_DDR_DQ15
PS_DDR_DQ14
PS_DDR_DQ13
PS_DDR_DQ12
PS_DDR_DQ11
PS_DDR_DQ10
PS_DDR_DQ9
PS_DDR_DQ8
PS_DDR_DQ7
PS_DDR_DQ6
PS_DDR_DQ5
PS_DDR_DQ4
PS_DDR_DQ3
PS_DDR_DQ2
PS_DDR_DQ1
PS_DDR_DQ0
PS_DDR_DM8
PS_DDR_DM3
PS_DDR_DM2
PS_DDR_DM1
PS_DDR_DM0
PS_DDR_CS_N1
PS_DDR_CS_N0
PS_DDR_CK_N1
PS_DDR_CK_N0
PS_DDR_CKE1
PS_DDR_CKE0
PS_DDR_CK1
PS_DDR_CK0
PS_DDR_BG1
PS_DDR_BG0
PS_DDR_BA1
PS_DDR_BA0
PS_DDR_ALERT_N
PS_DDR_ACT_N
PS_DDR_A17
PS_DDR_A16
PS_DDR_A15
PS_DDR_A14
PS_DDR_A13
PS_DDR_A12
PS_DDR_A11
PS_DDR_A10
PS_DDR_A9
PS_DDR_A8
PS_DDR_A7
PS_DDR_A6
PS_DDR_A5
PS_DDR_A4
PS_DDR_A3
PS_DDR_A2
PS_DDR_A1
PS_DDR_A0
+DDR_VDDQ
R213
240R ± 0.1%
GND
RESET
CS0_B
CS0_A
CK_C_B
CK_C_A
CKE
CK_T_B
CK_T_A
CA5_B
CA4_B
CA3_B
CA2_B
CA1_B
CA0_B
CA5_A
CA4_A
CA3_A
CA2_A
CA1_A
CA0_A
Routing guidelines
Max distance to FPGA: 1 inch
Target impedance: 50 ohm
Distance to plane: 0.06 mm (Xilinx)
Signal Group
Skew Constraints (ps)
Skew Constraints (mil)
DQ to DQS
±5
±29
Signal Group
Skew Constraints (ps)
Skew Constraints (mil)
ck_p and ck_n
2
12
Signal Group
Skew Constraint (ps)
Skew Constraint (mil)
CK to DQS
−149 to 1796
−879 to 10,600
Signal Group
Signal Segment
Skew Constraints (ps)
Skew Constraints (mil)
Address/command/control to CK (A)
Address/command/control to CK (B)
MPSoC to memory device
±8
±47
Data (DQ/DM) to DQS (A)
Data (DQ/DM) to DQS (B)
MPSoC to memory device
±5
±29
CK (A) to DQS0/1 (A)
CK (B) to DQS0/1 (B)
MPSoC to memory device
−500 to 2500
−2950 to 14750
DQ/DM (slowest to fastest) (A)
DQ/DM (slowest to fastest) (B)
MPSoC to memory device
5
29
CK_T and CK_C (A)
CK_T and CK_C (B)
MPSoC to memory device
2
11
DQS_T and DQS_C (A)
DQS_T and DQS_C (B)
MPSoC to memory device
2
11
R214
4k7
RESET
GND
+DDR_VDD2
ODT_CA_A
ODT_CA_B
+DDR_VDDQ
R215
DNF
CKE
CKE0_A
CKE0_B
R216
DNF
GND
Xilinx documentation says
160Ω to VDDQ & 160Ω to GND,
but it does not fit with LVSTL.
Also, it references Vtt which
does not exist on LPDDR4,
only DDR4...
Oversight?
+DDR_VDD1
C172
C173
C174
C175
C176
0u1F
10uF
GND
C177
C178
C179
C180
C181
+DDR_VDDQ
U24A
MT53E256M32D2DS-053
CK_T_A
CK_C_A
CS0_A
CA0_A
CA1_A
CA2_A
CA3_A
CA4_A
CA5_A
CKE0_A
DQS0_T_A
DQS0_C_A
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DMI0_A
ODT_CA_A
DQS1_T_A
DQS1_C_A
DQ8_A
DQ9_A
DQ10_A
DQ11_A
DQ12_A
DQ13_A
DQ14_A
DQ15_A
DMI1_A
VDD1
VDD2
VDDQ
VSS
F1
A4
B10
A10
GND
Micron
MT53E256M32D2DS-053 WT:B
U24B
MT53E256M32D2DS-053
CK_T_B
CK_C_B
CS0_B
CA0_B
CA1_B
CA2_B
CA3_B
CA4_B
CA5_B
CKE0_B
DQS0_T_B
DQS0_C_B
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DMI0_B
ODT_CA_B
RESET_N
ZQ0
DQS1_T_B
DQS1_C_B
DQ8_B
DQ9_B
DQ10_B
DQ11_B
DQ12_B
DQ13_B
DQ14_B
DQ15_B
DMI1_B
T4
AB4
AA10
T2
T11
A5
240R ± 0.1%
R217
AB10
Selected LPDDR4 chip:
MT53E256M32D2DS-053 AAT:B by micron
See page 96 of PCB design document
Designed by Xavier L'Heureux
MIST Lab
Sheet: /FPGA/DDR/
File: DDR.sch
Title: Portiloop
Size: USLetter
Date: 2021-06-07
Rev: 1A
KiCad E.D.A. kicad 5.1.10
Id: 20/23

Power selection

Buttons



JTAG connector



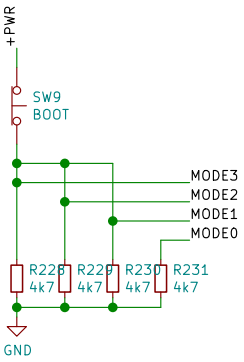
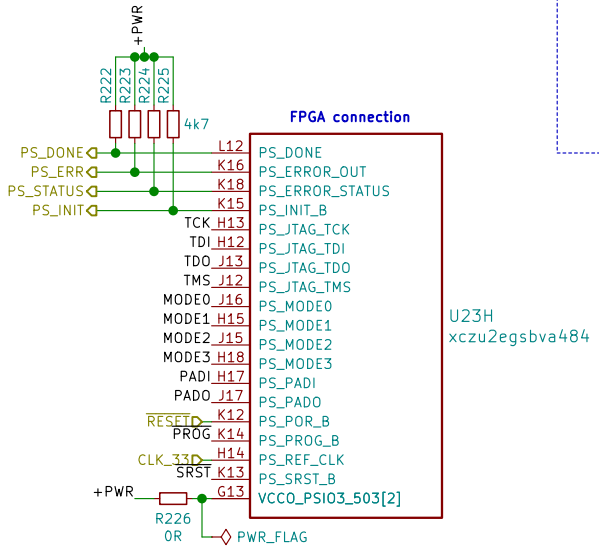
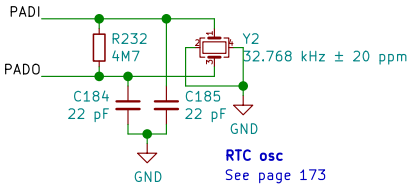


Table 11-1: **Boot Modes**

Boot Mode	Mode Pins [3:0]	Pin Location	CSU Mode	Description
PS JTAG	0000	JTAG	Slave	PSJTAG interface, PS dedicated pins.
Quad-SPI (24b)	0001	MIO[12:0]	Master	24-bit addressing (QSPI24).
Quad-SPI (32b)	0010	MIO[12:0]	Master	32-bit addressing (QSPI32).
SD0 (2.0)	0011	MIO[25:21, 16:13]	Master	SD 2.0.
NAND	0100	MIO[25:09]	Master	Requires 8-bit data bus width.
SD1 (2.0)	0101	MIO[51:43]	Master	SD 2.0.
eMMC (1.8V)	0110	MIO[22:13]	Master	eMMC version 4.5 at 1.8V.
USB0 (2.0)	0111	MIO[52:63]	Slave	USB 2.0 only.
PJTAG (MIO #0)	1000	MIO[29:26]	Slave	PJTAG connection 0 option.
PJTAG (MIO #1)	1001	MIO[15:12]	Slave	PJTAG connection 1 option.
SD1 LS (3.0)	1110	MIO[51:39]	Master	SD 3.0 with a required SD 3.0 compliant voltage level shifter.





Could have chosen Si5340B, but out of stock everywhere

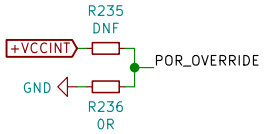
Designed by Xavier L'Heureux
MIST Lab

Sheet: /FPGA/FPGA_config/
File: FPGA_config.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 21/23

POR delay

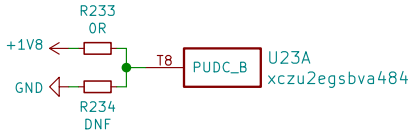


POR delay override.
0 = Standard PL power-on delay time (recommended default).

1= Faster PL power-on delay time.

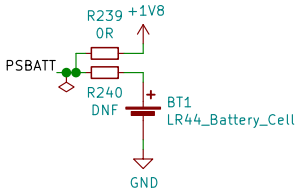
Do not allow this pin to float before and during configuration. This pin must be tied to VCCINT or GND.

Power-up Configuration



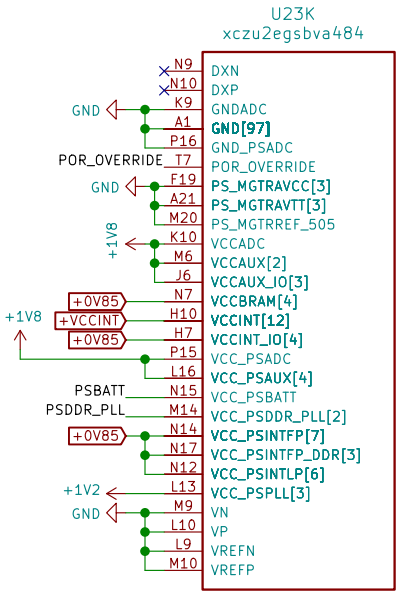
Pull-Up During Configuration (bar) Dedicated input pin. Active-Low input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. Caution! Do not allow this pin to float before and during configuration. Must be tied High or Low. PUDC_B must be tied either directly or via a ≤ 1 k Ω resistor to VCCAUX or GND.

RTC battery



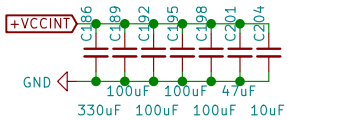
Really not sure about battery
Around 1 year capacity
=> must be able to replace
=> case will be harder to make

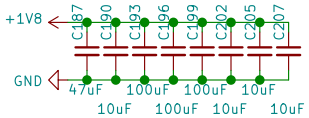
Power bank

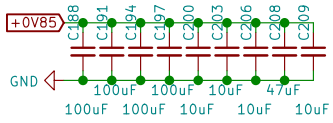


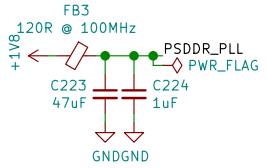
VN & VP determine the SYSMON I2C address at power up
Grounded = 0x32

Decoupling (see page 30)

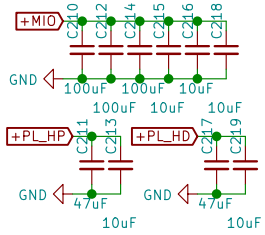








Ferrite bead: Murata BLM18SG121TN1



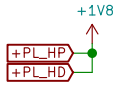


Table 1-11: **Recommended PCB Capacitor Specifications and Placement Guidelines**

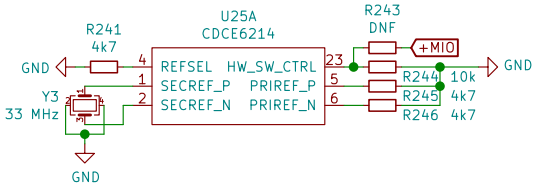
Nominal Value (µF)	Case Size	Temp/Change (%)	Manufacturer	Manufacturer Part Number	Ideal Placement to FPGA/MPSoC[1]
330	1210	X6S	Murata	GRM32EC80E337ME05	1–4"
100	0805	X6S	Murata	GRM21BC80G107ME15	0.5–3"
47	0603	X6S	Murata	GRM188C80E476ME05	0.5–2"
10	0402	X6S	Murata	GRM155C80J106ME11D	0–1"[2]

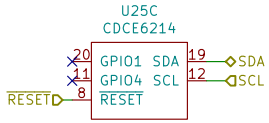
Designed by Xavier L'Heureux
MIST Lab

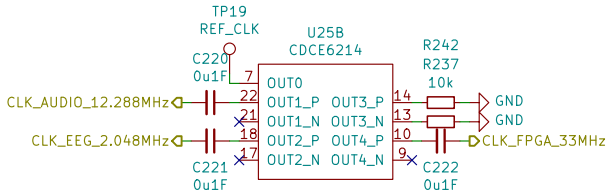
Sheet: /FPGA/FPGA_power/
File: FPGA_power.sch

Title: Portiloop

Size: USLetter | Date: 2021-06-07 | **Rev: 1A**
KiCad E.D.A. kicad 5.1.10 | Id: 22/23







Note
Output capacitors (AC-coupling)
recommended by datasheet.
Not sure about effect, may need
to validate values and/or switch
to 0Ω resistors

Designed by Xavier L'Heureux
MIST Lab

Sheet: /clocks/
File: clocks.sch

Title: Portiloop

Size: USLetter	Date: 2021-06-07	**Rev: 1A**
KiCad E.D.A. kicad 5.1.10		Id: 23/23