TPS650860 Configurable Multirail PMU for Multicore Processors

1 Device Overview

1.1 Features

- Wide V_{IN} Range From 5.6 V to 21 V
- Three Variable-Output Voltage Synchronous Step-Down Controllers With DCAP2™ Topology
  - Scalable Output Current Using External FETs With Selectable Current Limit
  - I^2C DVS Control From 0.41 V to 1.67 V in 10-mV Steps or 1 V to 3.575 V in 25-mV Steps
- Three Variable-Output Voltage Synchronous Step-Down Converters With DCS-Control Topology
  - V_{IN} Range From 4.5 V to 5.5 V
  - Up to 3 A of Output Current
  - I^2C DVS Control From 0.41 V to 1.67 V in 10-mV Steps or 0.425 V to 3.575 V in 25-mV Steps
- Three LDO Regulators With Adjustable Output Voltage
  - LDOA1: I^2C-Selectable Output Voltage From 1.35 V to 3.3 V for up to 200 mA of Output Current
  - LDOA2 and LDOA3: I^2C-Selectable Output Voltage From 0.7 V to 1.5 V for up to 600 mA of Output Current
- VTT LDO for DDR Memory Termination
- Three Load Switches With Slew Rate Control
  - Up to 300 mA of Output Current With Voltage Drop Less Than 1.5% of Nominal Input Voltage
  - R_{DSON} < 96 mΩ at Input Voltage of 1.8 V
- 5-V Fixed-Output Voltage LDO (LDO5)
  - Power Supply for Gate Drivers of SMPS and for LDOA1
  - Automatic Switch to External 5-V Buck for Higher Efficiency
- Built-in Flexibility and Configurability by Factory OTP Programming
  - Six GPI Pins Configurable to Enable (CTL1 to CTL6) or Sleep Mode Entry (CTL3 and CTL6) of Any Selected Rails
  - Four GPO Pins Configurable to Power Good of Any Selected Rails
  - Open-Drain Interrupt Output Pin
- I^2C Interface Supports:
  - Standard Mode (100 kHz)
  - Fast Mode (400 kHz)
  - Fast Mode Plus (1 MHz)

1.2 Applications

- Residential Gateway
- POS Terminals
- Test and Measurement
- Programmable Logic Controllers
- Embedded PCs
- Human to Machine Interfaces

1.3 Description

The TPS650860 device is a single-chip power-management IC designed for multicore processors, FPGAs, and other System-on-Chips (SoCs). The TPS650860 offers an input range of 5.6 V to 21 V, enabling a wide range of applications. The device is well suited for NVDC and non-NVDC power architecture using 2S, 3S, or 4S Li-Ion battery packs. See the *Application Section* for 5-V input supplies. The D-CAP2™ and DCS-Control high-frequency voltage regulators use small inductors and capacitors to achieve a small solution size. The D-CAP2 and DCS-Control topologies have excellent transient response performance, which is great for processor core and system memory rails that have fast load switching. An I^2C interface allows simple control either by an embedded controller (EC) or by an SoC. The PMIC comes in an 8-mm × 8-mm, single-row VQFN package with thermal pad for good thermal dissipation and ease of board routing.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS650860	VQFN (64)	8.00 mm × 8.00 mm

(1) For more information, see the *Mechanical Packaging and Orderable Information* section.

1.4 Functional Block Diagram

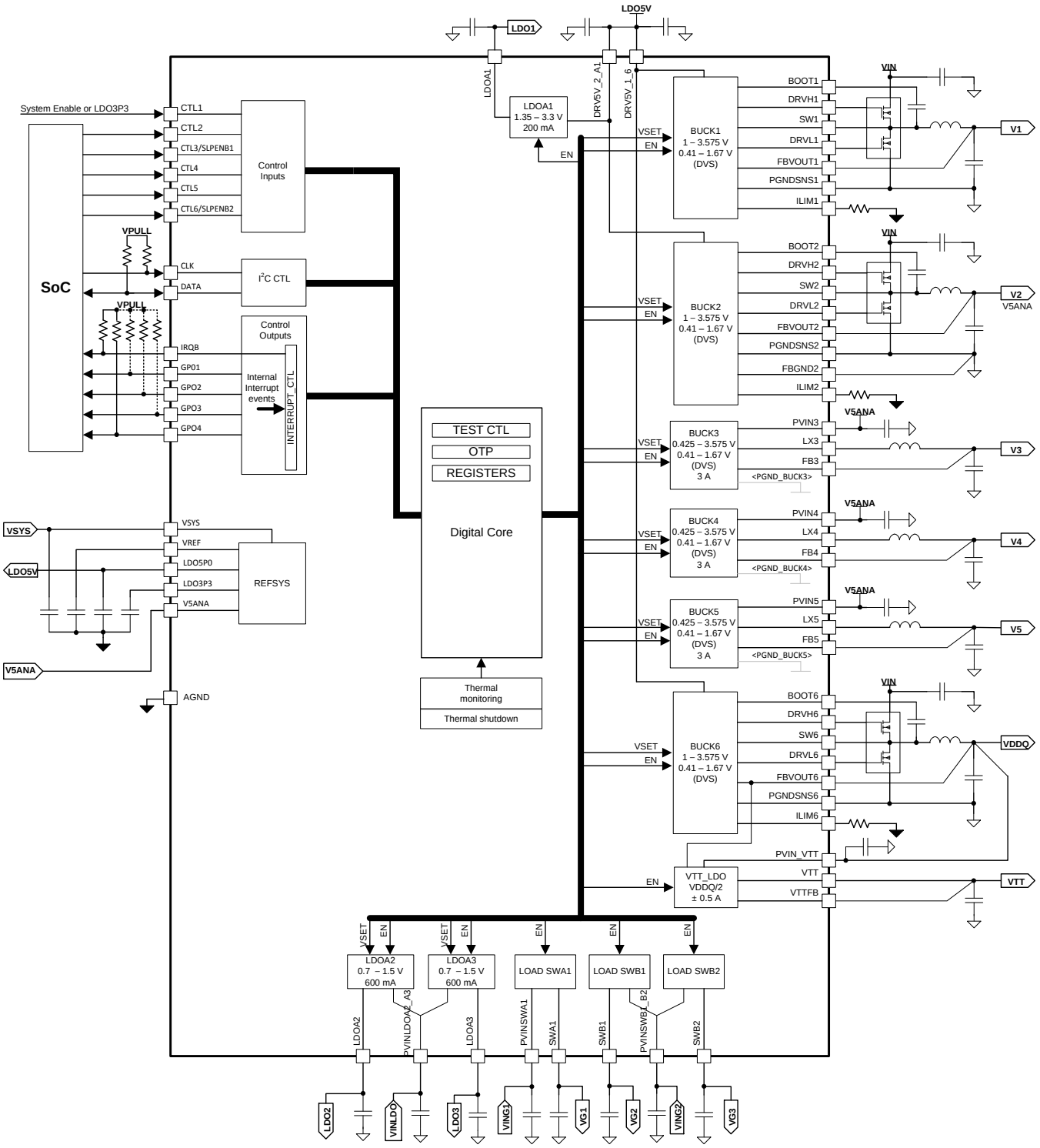

Figure 1-1. PMIC Functional Block Diagram

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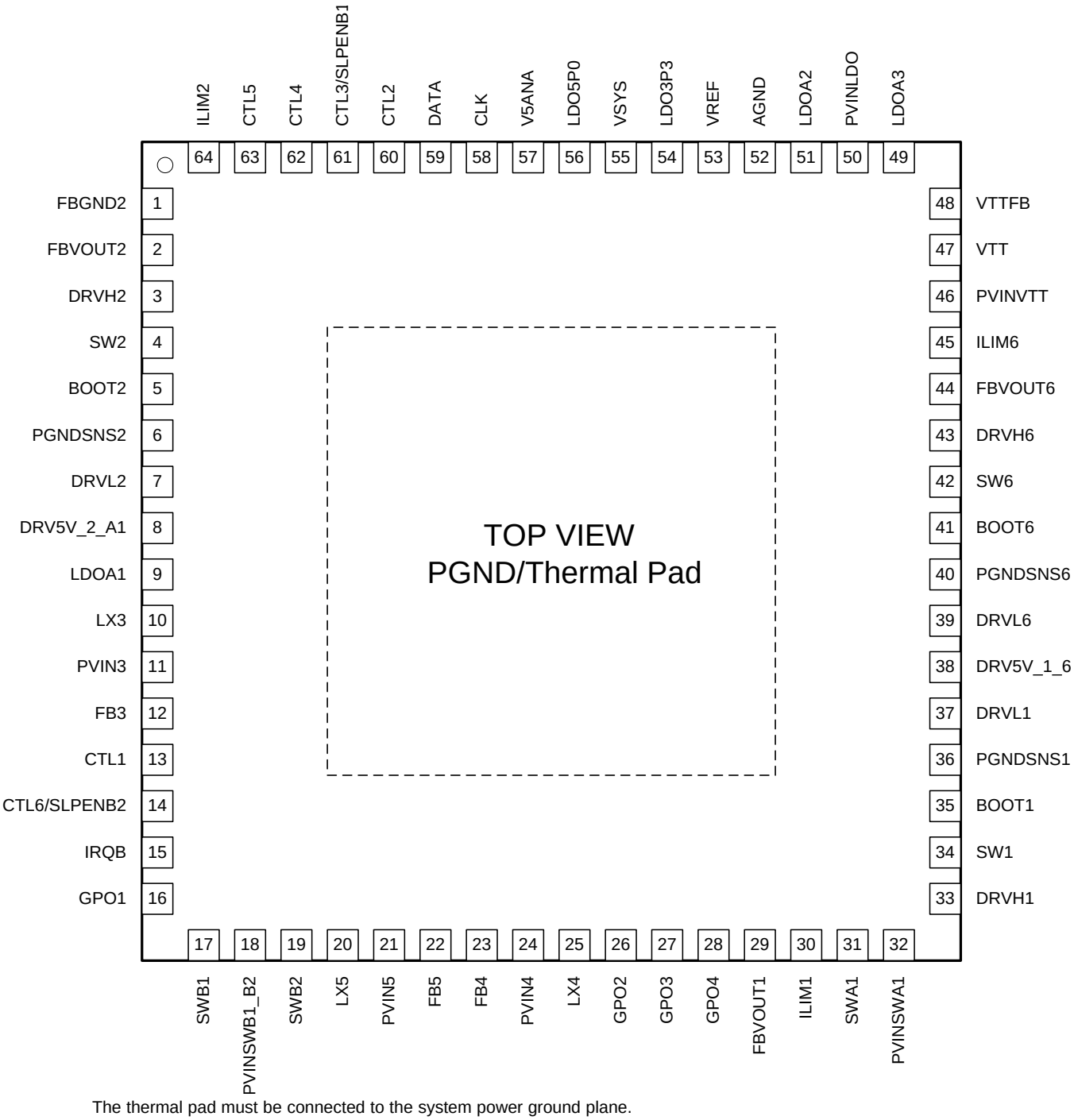
2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2015) to Revision A	Page
• Changed device status from: PRODUCT PREVIEW to: PRODUCTION DATA	1

3 Pin Configuration and Functions



The thermal pad must be connected to the system power ground plane.

Figure 3-1. RSK (VQFN) Pin Map Diagram

Pin Functions

NO.	NAME	I/O	DESCRIPTION
SMPS REGULATORS			
1	FBGND2	I	Remote negative feedback sense for BUCK2 controller. Connect to negative terminal of output capacitor.
2	FBVOUT2	I	Remote positive feedback sense for BUCK2 controller. Connect to positive terminal of output capacitor.
3	DRVH2	O	High-side gate driver output for BUCK2 controller.
4	SW2	I	Switch node connection for BUCK2 controller.
5	BOOT2	I	Bootstrap pin for BUCK2 controller. Connect a 100-nF ceramic capacitor between this pin and SW2 pin.
6	PGNDSNS2	I	Power GND connection for BUCK2. Connect to ground terminal of external low-side FET.
7	DRVL2	O	Low-side gate driver output for BUCK2 controller.
8	DRV5V_2_A1	I	5-V supply to BUCK2 gate driver and LDOA1. Bypass to ground with a 2.2-µF (TYP) ceramic capacitor. Shorted on board to LDO5P0 pin typically.
10	LX3	O	Switch node connection for BUCK3 converter.
11	PVIN3	I	Power input to BUCK3 converter. Bypass to ground with a 10-µF (TYP) ceramic capacitor.
12	FB3	I	Remote feedback sense for BUCK3 converter. Connect to positive terminal of output capacitor.
20	LX5	O	Switch node connection for BUCK5 converter.
21	PVIN5	I	Power input to BUCK5 converter. Bypass to ground with a 10-µF (TYP) ceramic capacitor.
22	FB5	I	Remote feedback sense for BUCK5 converter. Connect to positive terminal of output capacitor.
23	FB4	I	Remote feedback sense for BUCK4 converter. Connect to positive terminal of output capacitor.
24	PVIN4	I	Power input to BUCK4 converter. Bypass to ground with a 10-µF (TYP) ceramic capacitor.
25	LX4	O	Switch node connection for BUCK4 converter.
29	FBVOUT1	I	Remote feedback sense for BUCK1 controller. Connect to positive terminal of output capacitor.
30	ILIM1	I	Current limit set pin for BUCK1 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET.
33	DRVH1	O	High-side gate driver output for BUCK1 controller.
34	SW1	I	Switch node connection for BUCK1 controller.
35	BOOT1	I	Bootstrap pin for BUCK1 controller. Connect a 100-nF ceramic capacitor between this pin and SW1 pin.
36	PGNDSNS1	I	Power GND connection for BUCK1. Connect to ground terminal of external low-side FET.
37	DRVL1	O	Low-side gate driver output for BUCK1 controller.
38	DRV5V_1_6	I	5-V supply to BUCK1 and BUCK6 gate drivers. Bypass to ground with a 2.2-µF (TYP) ceramic capacitor. Shorted on board to LDO5P0 pin typically.
39	DRVL6	O	Low-side gate driver output for BUCK6 controller.
40	PGNDSNS6	I	Power GND connection for BUCK6. Connect to ground terminal of external low-side FET.
41	BOOT6	I	Bootstrap pin for BUCK6 controller. Connect a 100-nF ceramic capacitor between this pin and SW6 pin.
42	SW6	I	Switch node connection for BUCK6 controller.

Pin Functions (continued)

NO.	NAME	I/O	DESCRIPTION
SMPS REGULATORS (continued)			
43	DRVH6	O	High-side gate driver output for BUCK6 controller.
44	FBVOUT6	I	Remote feedback sense for BUCK6 controller. Connect to positive terminal of output capacitor.
45	ILIM6	I	Current limit set pin for BUCK6 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET.
64	ILIM2	I	Current limit set pin for BUCK2 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET.
LDO and LOAD SWITCHES			
9	LDOA1	O	LDOA1 output. Bypass to ground with a 4.7-µF (TYP) ceramic capacitor. Leave floating when not in use.
17	SWB1	O	Output of load switch B1. Bypass to ground with a 0.1-µF (TYP) ceramic capacitor. Leave floating when not in use.
18	PVINSWB1_B2	I	Power supply to load switch B1 and B2. Bypass to ground with a 1-µF (TYP) ceramic capacitor to improve transient performance. Connect to ground when not in use.
19	SWB2	O	Output of load switch B2. Bypass to ground with a 0.1-µF (TYP) ceramic capacitor. Leave floating when not in use.
31	SWA1	O	Output of load switch A1. Bypass to ground with a 0.1-µF (TYP) ceramic capacitor. Leave floating when not in use.
32	PVINSWA1	I	Power supply to load switch A1. Bypass to ground with a 1-µF (TYP) ceramic capacitor to improve transient performance. Connect to ground when not in use.
46	PVINVTT	I	Power supply to VTT LDO. Bypass to ground with a 10-µF (MIN) ceramic capacitor.
47	VTT	O	Output of load VTT LDO. Bypass to ground with 2× 22-µF (MIN) ceramic capacitors.
48	VTTFB	I	Remote feedback sense for VTT LDO. Connect to positive terminal of output capacitor.
49	LDOA3	O	Output of LDOA3. Bypass to ground with a 4.7-µF (TYP) ceramic capacitor. Leave floating when not in use.
50	PVINLDOA2_A3	I	Power supply to LDOA2 and LDOA3. Bypass to ground with a 4.7-µF (TYP) ceramic capacitor. Connect to ground when not in use.
51	LDOA2	O	Output of LDOA2. Bypass to ground with a 4.7-µF (TYP) ceramic capacitor. Leave floating when not in use.
54	LDO3P3	O	Output of 3.3-V internal LDO. Bypass to ground with a 4.7-µF (TYP) ceramic capacitor.
56	LDO5P0	O	Output of 5-V internal LDO or an internal switch that connects this pin to V5ANA. Bypass to ground with a 4.7-µF (TYP) ceramic capacitor.
57	V5ANA	I	External 5-V supply input to internal load switch that connects this pin to LDO5P0 pin. Bypass this pin with an optional ceramic capacitor to improve transient performance.

Pin Functions (continued)

NO.	NAME	I/O	DESCRIPTION
INTERFACE			
13	CTL1	I	Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin.
14	CTL6/SLPENB2	I	Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. Alternatively, when configured to active-low sleep enable, a group of VRs chosen can be entered into (L) or out of (H) sleep state where their output voltages may be different from those in normal state.
15	IRQB	O	Open-drain output interrupt pin. Refer to Section 5.9.3 for definitions.
16	GPO1	O	General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect power good status of VRs of any choice or to be controlled by an I^2C register bit by the user, which then can be used as an enable signal to an external VR.
26	GPO2	O	General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect power good status of VRs of any choice or to be controlled by an I^2C register bit by the user, which then can be used as an enable signal to an external VR.
27	GPO3	O	General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect power good status of VRs of any choice or to be controlled by an I^2C register bit by the user, which then can be used as an enable signal to an external VR.
28	GPO4	O	Open-drain output that can be configured to reflect power good status of VRs of any choice or to be controlled by an I^2C register bit by the user, which then can be used as an enable signal to an external VR.
58	CLK	I	I^2C clock
59	DATA	I/O	I^2C data
60	CTL2	I	Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin.
61	CTL3/SLPENB1	I	Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. Alternatively, when configured to active-low sleep enable, a group of VRs chosen can be entered into (L) or out of (H) sleep state where their output voltages may be different from those in normal state.
62	CTL4	I	Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin.
63	CTL5	I	Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin.
REFERENCE			
53	VREF	O	Band-gap reference output. Stabilize it by connecting a 100-nF (TYP) ceramic capacitor between this pin and quiet ground.
52	AGND	—	Analog ground. Do not connect to the thermal pad ground on top layer. Connect to ground of VREF capacitor.
55	VSYS	I	System voltage detection and input to internal LDOs (3.3 V and 5 V). Bypass to ground with a 1-µF (TYP) ceramic capacitor.
THERMAL PAD			
Thermal pad		—	Connect to PCB ground plane using multiple vias for good thermal and electrical performance.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
ANALOG				
VSYS	Input voltage from battery	–0.3	28	V
PVIN3, PVIN4, PVIN5, LDO5P0, DRV5V_1_6, DRV5V_2_A1, DRVL1, DRVL2, DRVL6		–0.3	7	V
V5ANA		–0.3	6	V
PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2		–0.3	0.3	V
DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6		–0.3	34	V
SW1, SW2, SW6		–2(2)	28	V
LX3, LX4, LX5		–1(3)	7	V
BOOTx to SWx	Differential voltage	–0.3	5.5	V
VREF, LDO3P3, FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5, ILIM1, ILIM2, ILIM6, PVINVTT, VTT, VTTFB, PVINSWA1, SWA1, PVINSWB1_B2, SWB1, SWB2, LDOA1		–0.3	3.6	V
PVINLDOA2_A3, LDOA2, LDOA3		–0.3	3.3	V
DIGITAL IOs				
DATA, CLK, GPO1-GPO3		–0.3	3.6	V
CTL1-CTL6, GPO4, IRQB		–0.3	7	V
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient for less than 5 ns.
(3) Transient for less than 20 ns.

4.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001(1)		±1000	V
		Charged Device Model (CDM), per JESD22-C101(2)	All pins	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
ANALOG				
VSYS	5.6	13	21	V
VREF	–0.3		1.3	V
PVIN3, PVIN4, PVIN5, LDO5P0, V5ANA, DRV5V_1_6, DRV5V_2_A1	–0.3	5	5.5	V
PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2	–0.3		0.3	V
DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6	–0.3		26.5	v
DRVL1, DRVL2, DRVL6	–0.3		5.5	V
SW1, SW2, SW6	–1		21	V
LX3, LX4, LX5	–1		5.5	V
FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5	–0.3		3.6	V
LDO3P3, ILIM1, ILIM2, ILIM6, LDOA1	–0.3		3.3	V
PVINVTT	–0.3	1.2 / 1.35	FBVOUT6	V
VTT, VTTFB	–0.3		FBVOUT6 / 2	V
PVINSWA1, SWA1	–0.3	3.3	3.6	V
PVINSWB1_B2, PVINLDOA2_A3, SWB1, SWB2	–0.3		1.8	V
LDOA2, LDOA3	–0.3		1.5	V
DIGITAL IOs				
DATA, CLK, CTL1–CTL6, GPO1–GPO4, IRQB	–0.3		3.3	V
CHIP				
T_A Operating ambient temperature range	–40	27	85	°C
T_J Operating junction temperature range	–40	27	125	°C

4.4 Thermal Information

THERMAL METRIC(1)		TPS650860 RSK (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.5 Electrical Characteristics: Total Current Consumption

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD}	PMIC shutdown current that includes I_Q for References, LDO5, LDO3P3, and digital core	V_{SYS} = 13 V, all functional output rails are disabled		65		µA

4.6 Electrical Characteristics: Reference and Monitoring System

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{REF}	Bandgap reference Voltage			1.25		V
	Accuracy		–0.5%		0.5%	
C_{VREF}	Bandgap output capacitor		0.047	0.1	0.22	µF
$V_{SYS\_UVLO\_5V}$	VSYS UVLO threshold for LDO5	V_{SYS} falling	5.24	5.4	5.56	V
$V_{SYS\_UVLO\_5V\_HYS}$	VSYS UVLO threshold hysteresis for LDO5	V_{SYS} rising above $V_{SYS\_UVLO\_5V}$		200		mV
$V_{SYS\_UVLO\_3V}$	VSYS UVLO threshold for LDO3P3	V_{SYS} falling	3.45	3.6	3.75	V
$V_{SYS\_UVLO\_3V\_HYS}$	VSYS UVLO threshold hysteresis for LDO3P3	V_{SYS} rising above $V_{SYS\_UVLO\_3V}$		150		mV
T_{CRIT}	Critical threshold of die temperature	T_J rising	130	145	160	°C
T_{CRIT_HYS}	Hysteresis of T_{CRIT}	T_J falling		10		°C
T_{HOT}	Hot threshold of die temperature	T_J rising	110	115	120	°C
T_{HOT_HYS}	Hysteresis of T_{HOT}	T_J falling		10		°C
LDO5						
V_{IN}	Input voltage at V_{SYS} pin		5.6	13	21	V
V_{OUT}	DC output voltage	I_{OUT} = 10 mA	4.9	5	5.1	V
I_{OUT}	DC output current			100	180	mA
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	200			mA
V_{TH_PG}	Power Good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		94%		
$V_{TH\_PG\_HYS}$	Power Good deassertion hysteresis	V_{OUT} rising or falling		4%		
I_Q	Quiescent current	V_{IN} = 13 V, I_{OUT} = 0 A		20		µA
C_{OUT}	External output capacitance		2.7	4.7	10	µF
V5ANA-to-LDO5P0 LOAD SWITCH						
R_{DSON}	On resistance	V_{IN} = 5 V, measured from V5ANA pin to LDO5P0 pin at I_{OUT} = 200 mA			1	Ω
V_{TH_PG}	Power Good threshold for external 5-V supply	V_{V5ANA} rising		4.7		V
$V_{TH\_HYS\_PG}$	Power Good threshold hysteresis for external 5-V supply	V_{V5ANA} falling		100		mV
I_{LKG}	Leakage current	Switch disabled, V_{V5ANA} = 5 V, V_{LDO5} = 0 V			10	µA
LDO3P3						
V_{IN}	Input voltage at V_{SYS} pin		5.6	13	21	V
V_{OUT}	DC output voltage	I_{OUT} = 10 mA		3.3		V
	Accuracy	V_{IN} = 13 V, I_{OUT} = 10 mA	–3%		3%	
I_{OUT}	DC output current				40	mA
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	70			mA
V_{TH_PG}	Power Good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		92%		
$V_{TH\_PG\_HYS}$	Power Good deassertion hysteresis	V_{OUT} falling		3%		
I_Q	Quiescent current	V_{IN} = 13 V, I_{OUT} = 0 A		20		µA
C_{OUT}	External output capacitance		2.2	4.7	10	µF

4.7 Electrical Characteristics: Buck Controllers

over recommended input voltage range, T_A = –40°C to 85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK1, BUCK2, BUCK6						
V_{IN}	Power input voltage for external HSD FET		5.6	13	21	V
V_{OUT}	DC output voltage VID range and options	VID step size = 10 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111	0.41		1.67	V
		VID step size = 25 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111	1 (1)		3.575	V
	BUCK1 output voltage	Set by BUCK1_VID[6:0], 10 mV step size selected		1.05		V
	BUCK2 output voltage	Set by BUCK2_VID[6:0], 25 mV step size selected		3.3		V
	BUCK6 output voltage	Set by BUCK6_VID[6:0], 10 mV step size selected		1.5		V
	DC output voltage accuracy	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 100 mA to 7 A	–2%		2%	
	Total output voltage accuracy (DC + ripple) in DCM	I_{OUT} = 10 mA, V_{OUT} ≤ 1 V	–30		40	mV
SR(V_{OUT})	Output DVS slew rate		2.5	3.125		mV/µs
I_{LIM_LSD}	Low-side output valley current limit accuracy (programmed by external resistor R_{LIM})		–15%		15%	
I_{LIMREF}	Source current out of ILIM1 pin	T = 25°C	45	50	55	µA
V_{LIM}	Voltage at ILIM1 pin	$V_{LIM} = R_{LIM} \times I_{LIMREF}$	0.2		2.25	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 7 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 13 V, V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 0 A to 7 A, referenced to V_{OUT} at $I_{OUT} = I_{OUT\_MAX}$	0%		1%	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising	105.5%	108%	110.5%	
		V_{OUT} falling	89.5%	92%	94.5%	
R_{DSON_DRVH}	Driver DRVH resistance	Source, IDRVH = –50 mA		3		Ω
		Sink, IDRVH = 50 mA		2		Ω
R_{DSON_DRVL}	Driver DRVL resistance	Source, IDRVL = –50 mA		3		Ω
		Sink, IDRVL = 50 mA		0.4		Ω
R_{DIS}	Output auto-discharge resistance	BUCK1_DIS[1:0] = 01		100		Ω
		BUCK1_DIS[1:0] = 10		200		Ω
		BUCK1_DIS[1:0] = 11		500		Ω
C_{BOOT}	Bootstrap capacitance			100		nF
R_{ON_BOOT}	Bootstrap switch ON resistance				20	Ω

(1) BUCKx_VID[6:0] = 0000001 – 0011000

4.8 Electrical Characteristics: Synchronous Buck Converters

over recommended input voltage range, T_A = –40°C to 85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK3, BUCK4, BUCK5						
V_{IN}	Power input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage VID range and options	VID step size = 10 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111	0.41		1.67	V
		VID step size = 12.5 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111	0.4125		1.9875	
		VID step size = 25 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111	0.425		3.575	
	BUCK3 output voltage	Set by BUCK3_VID[6:0], 25-mV step size selected		1.05		V
	BUCK4 output voltage	Set by BUCK4_VID[6:0], 25-mV step size selected		3.3		
	BUCK5 output voltage	Set by BUCK5_VID[6:0], 25-mV step size selected		1.5		
	DC output voltage accuracy	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 1.5 A	–2%		2%	
		V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 100 mA	–2.5%		2.5%	
	Total output voltage accuracy (DC + ripple) in DCM	I_{OUT} = 10 mA, V_{OUT} ≤ 1 V	–30		40	mV
$SR(V_{OUT})$	Output DVS slew rate		2.5	3.125		mV/µs
I_{OUT}	Continuous DC output current				3	A
I_{IND_LIM}	HSD FET current limit		4.3		7	A
I_Q	Quiescent current	V_{IN} = 5 V, V_{OUT} = 1 V		35		µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 1.5 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 5 V, V_{OUT} = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, I_{OUT} = 0 A to 3 A, referenced to V_{OUT} at I_{OUT} = 1.5 A	–0.2%		2%	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		
R_{DIS}	Output auto-discharge resistance	BUCK3_DIS[1:0] = 01		100		Ω
		BUCK3_DIS[1:0] = 10		200		
		BUCK3_DIS[1:0] = 11		500		

4.9 Electrical Characteristics: LDOs

over recommended input voltage range, T_A = –40°C to 85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDOA1						
V_{IN}	Input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage	Set by LDOAx_VID[3:0]		3.3		
	Accuracy	I_{OUT} = 0 to 200 mA	–2%		2%	V
I_{OUT}	DC output current				200	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 40 mA	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 10 mA to 200 mA	–2%		2%	
I_{OCP}	Overcurrent protection	V_{IN} = 5 V, Measured with output shorted to ground	500			mA
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$t_{STARTUP}$	Start-up time	Measured from EN = H to reach 95% of final value, C_{OUT} = 4.7 µF			500	µs
I_Q	Quiescent current	I_{OUT} = 0 A		23		µA
C_{OUT}	External output capacitance		2.7	4.7	10	µF
	ESR				100	mΩ
R_{DIS}	Output auto-discharge resistance	LDOA1_DIS[1:0] = 01		100		Ω
		LDOA1_DIS[1:0] = 10		190		Ω
		LDOA1_DIS[1:0] = 11		450		Ω
LDOA2 and LDOA3						
V_{IN}	Power input voltage		V_{OUT} + V_{DROP} (1)	1.8	1.98	V
V_{OUT}	LDOA2 DC output voltage	Set by LDOAx_VID[3:0]		0.7		V
	LDOA3 DC output voltage	Set by LDOAx_VID[3:0]		1.2		V
	DC output voltage accuracy	I_{OUT} = 0 to 600 mA	–2%		3%	
I_{OUT}	DC output current				600	mA
V_{DROP}	Dropout voltage	V_{OUT} = 0.99 × V_{OUT_NOM}, I_{OUT} = 600 mA			350	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 300 mA	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 10 mA to 600 mA	–2%		2%	
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	0.65	1.25		A
V_{TH_PG}	Power Good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$t_{STARTUP}$	Start-up time	Measured from EN = H to reach 95% of final value, C_{OUT} = 4.7 µF			500	µs
I_Q	Quiescent current	I_{OUT} = 0 A		20		µA

(1) It must be equal to or greater than 1.62 V.

Electrical Characteristics: LDOs *(continued)*

over recommended input voltage range, T_A = –40°C to 85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDOA2 and LDOA3 (continued)						
PSRR	Power supply rejection ratio	f = 1 kHz, V_{IN} = 1.8 V, V_{OUT} = 1.2 V, I_{OUT} = 300 mA, C_{OUT} = 2.2 µF – 4.7 µF		48		dB
		f = 10 kHz, V_{IN} = 1.8 V, V_{OUT} = 1.2 V, I_{OUT} = 300 mA, C_{OUT} = 2.2 µF – 4.7 µF		30		dB
C_{OUT}	External output capacitance		2.2	4.7	10	µF
	ESR				100	mΩ
R_{DIS}	Output auto-discharge resistance	LDOA2_DIS[1:0] = 01		80		Ω
		LDOA2_DIS[1:0] = 10		180		
		LDOA2_DIS[1:0] = 11		475		
VTT LDO						
V_{IN}	Power input voltage			1.2	3.3	V
V_{OUT}	DC output voltage	V_{IN} = 1.2 V, Measured at VTTFB pin		V_{IN} / 2		V
	DC output voltage accuracy	Relative to V_{IN} / 2, I_{OUT} ≤ 10 mA, 1.1 V ≤ V_{IN} ≤ 1.35 V	–10		10	mV
		Relative to V_{IN} / 2, I_{OUT} ≤ 500 mA, 1.1 V ≤ V_{IN} ≤ 1.35 V	–25		25	
I_{OUT}	DC output current	sink(–) and source(+)	–500		500	mA
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	1.1 V ≤ V_{IN} ≤ 1.35 V, I_{OUT} = –500 mA to 500 mA	–4%		4%	
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	0.95			A
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		110%		
		V_{OUT} falling		95%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}			5%		
I_Q	Total ground current	V_{IN} = 1.2 V, I_{OUT} = 0 A			240	µA
I_{LKG}	OFF leakage current	V_{IN} = 1.2 V, disabled			1	µA
C_{IN}	External input capacitance		10			µF
C_{OUT}	External output capacitance		35			µF
R_{DIS}	Output auto-discharge resistance	VTT_DIS = 0	1000			kΩ
		VTT_DIS = 1	60	80	100	Ω

4.10 Electrical Characteristics: Load Switches

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWA1						
V_{IN}	Input voltage range		0.5	1.8	3.3	V
I_{OUT}	DC output current				300	mA
R_{DSON}	ON resistance	V_{IN} = 1.8 V, measured from PVINSWA1 pin to SWA1 pin at I_{OUT} = $I_{OUT,MAX}$		60	93	mΩ
		V_{IN} = 3.3 V, measured from PVINSWA1 pin to SWA1 pin at I_{OUT} = $I_{OUT,MAX}$		100	165	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		2%		
I_{INRUSH}	Inrush current upon turnon	V_{IN} = 3.3 V, C_{OUT} = 0.1 µF			10	mA
I_Q	Quiescent current	V_{IN} = 3.3 V, I_{OUT} = 0 A		10.5		µA
		V_{IN} = 1.8 V, I_{OUT} = 0 A		9		
I_{LKG}	Leakage current	Switch disabled, V_{IN} = 1.8 V		7	370	nA
		Switch disabled, V_{IN} = 3.3 V		10	900	
C_{OUT}	External output capacitance			0.1		µF
R_{DIS}	Output auto-discharge resistance	SWA1_DIS[1:0] = 01		100		Ω
		SWA1_DIS[1:0] = 10		200		
		SWA1_DIS[1:0] = 11		500		
SWB1_2						
V_{IN}	Input voltage range		0.5	1.8	3.3	V
I_{OUT}	DC current per output				400	mA
R_{DSON}	ON resistance	V_{IN} = 1.8 V, measured from PVINSWB1_B2 pin to SWB1/SWB2 pin at I_{OUT} = $I_{OUT,MAX}$		68	92	mΩ
		V_{IN} = 3.3 V, measured from PVINSWB1_B2 pin to SWB1/SWB2 pin at I_{OUT} = $I_{OUT,MAX}$		75	125	mΩ
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		2%		
I_{INRUSH}	Inrush current upon turning on	V_{IN} = 3.3 V, C_{OUT} = 0.1 µF			10	mA
I_Q	Quiescent current	V_{IN} = 3.3 V, I_{OUT} = 0 A		10.5		µA
		V_{IN} = 1.8 V, I_{OUT} = 0 A		9		
I_{LKG}	Leakage current	Switch disabled, V_{IN} = 1.8 V		7	460	nA
		Switch disabled, V_{IN} = 3.3 V		10	1150	
C_{OUT}	External output capacitance			0.1		µF
R_{DIS}	Output auto-discharge resistance	SWBx_DIS[1:0] = 01		100		Ω
		SWBx_DIS[1:0] = 10		200		
		SWBx_DIS[1:0] = 11		500		

4.11 Digital Signals: I²C Interface

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	V_{PULL_UP} = 1.8 V			0.4	V
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
I_{LKG}	Leakage current	V_{PULL_UP} = 1.8 V		0.01	0.3	µA
$R_{PULL-UP}$	Pullup resistance	Standard mode			8.5	kΩ
		Fast mode			2.5	
		Fast mode plus			1	
C_{OUT}	Total load capacitance per pin				50	pF

4.12 Digital Input Signals (CTLx)

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.85			V
V_{IL}	Low-level input voltage				0.4	V

4.13 Digital Output Signals (IRQB, GPOx)

Over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} < 2 mA			0.4	V
I_{LKG}	Leakage current	V_{PULL_UP} = 1.8 V			0.35	µA

4.14 Timing Requirements

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I²C INTERFACE					
f_{CLK}	Clock frequency (standard mode)			100	kHz
	Clock frequency (fast mode)			400	kHz
	Clock frequency (fast mode plus)			1000	kHz
t_r	Rise time (standard mode)			1000	ns
	Rise time (fast mode)			300	ns
	Rise time (fast mode plus)			120	ns
t_f	Rise time (standard mode)			300	ns
	Rise time (fast mode)			300	ns
	Rise time (fast mode plus)			120	ns

4.15 Switching Characteristics

over operating free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK CONTROLLERS						
t_{PG}	Total turnon time	Measured from enable going high to when output reaches 90% of target value.		550	850	µs
$T_{ON,MIN}$	Minimum on-time of DRVH			50		ns
T_{DEAD}	Driver dead-time	DRVH off to DRVL on		15		ns
		DRVL off to DRVH on		30		ns
f_{SW}	Switching frequency	Continuous-conduction mode, V_{IN} = 13 V, V_{OUT} ≥ 1 V		1000		kHz
BUCK CONVERTERS						
t_{PG}	Total turnon time	Measured from enable going high to when output reaches 90% of target value.		250	1000	µs
f_{SW}	Switching frequency	Continuous-conduction mode, V_{OUT} = 1 V, I_{OUT} = 1 A		1.7		MHz
		Continuous-conduction mode, V_{OUT} = 1.05 V, I_{OUT} = 1 A		1.9		MHz
		Continuous-conduction mode, V_{OUT} = 1.8 V, I_{OUT} = 1 A		2.5		MHz
LDOAx						
$t_{STARTUP}$	Start-up time	Measured from enable going high to when output reaches 95% of final value, V_{OUT} = 1.2 V, C_{OUT} = 4.7 µF		180		µs
VTT LDO						
$t_{STARTUP}$	Start-up time	Measured from enable going high to PG assertion, V_{OUT} = 0.675 V, C_{OUT} = 40 µF		22		µs
SWA1						
$t_{TURN-ON}$	Turnon time	Measured from enable going high to reach 95% of final value, V_{IN} = 3.3 V, C_{OUT} = 0.1 µF		0.85		ms
		Measured from enable going high to reach 95% of final value, V_{IN} = 1.8 V, C_{OUT} = 0.1 µF		0.63		ms
SWB1_2						
$t_{TURN-ON}$	Turnon time	Measured from enable going high to reach 95% of final value, V_{IN} = 3.3 V, C_{OUT} = 0.1 µF		1.1		ms
		Measured from enable going high to reach 95% of final value, V_{IN} = 1.8 V, C_{OUT} = 0.1 µF		0.82		ms

4.16 Typical Characteristics

Measurements done at 25°C.

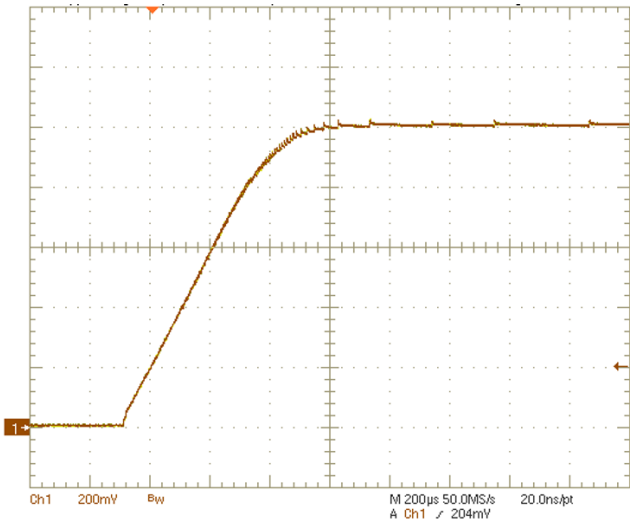


Figure 4-1. BUCK2 Controller Start Up

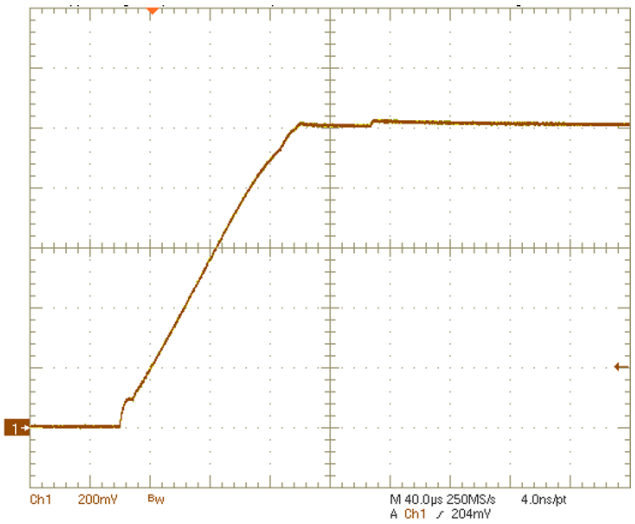


Figure 4-2. BUCK3 Converter Start Up

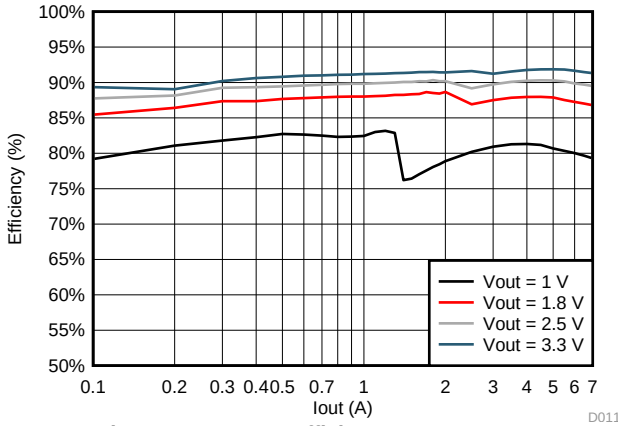


Figure 4-3. BUCK1 Efficiency at V_{IN} = 13 V

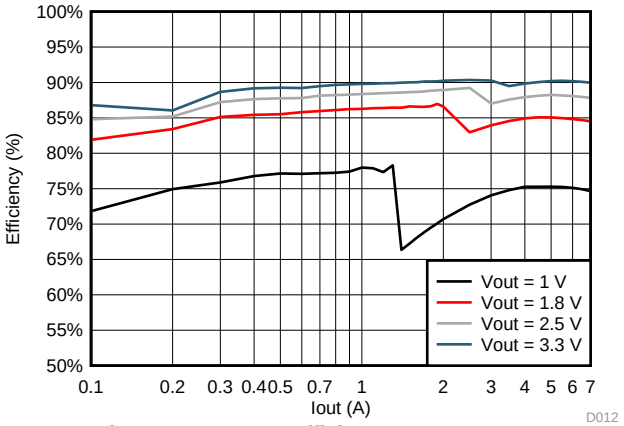


Figure 4-4. BUCK1 Efficiency at V_{IN} = 18 V

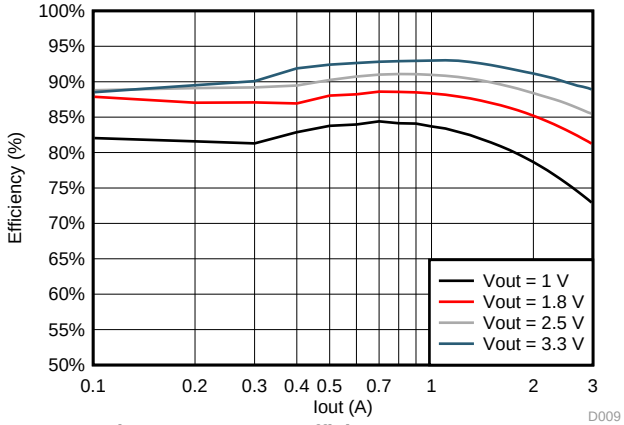


Figure 4-5. BUCK3 Efficiency at V_{IN} = 5 V

5 Detailed Description

5.1 Overview

The TPS650860 power-management integrated circuit (PMIC) provides a highly flexible and configurable power solution that can power a wide array of processors along with DDR3/DDR4 memory and other peripherals. Integrated in the PMIC are three step-down controllers (BUCK1, BUCK2, and BUCK6), three step-down converters (BUCK3, BUCK4, and BUCK5), a sink or source LDO (VTT LDO), three low-voltage V_{IN} LDOs (LDOA1–LDOA3), and three load switches (SWA1, SWB1, and SWB2). With on-chip one-time programmable (OTP) memory, configuration of each rail for default output value, power-up sequence, fault handling, and power good mapping into a GPO pin are all conveniently flexible. All VRs have a built-in discharge resistor, and the value can be changed using the DISCHCNT1–DISCHCNT3 and LDOA1_CTRL registers. When enabling a VR, the PMIC automatically disconnects the discharge resistor for that rail without any I^2C command. Table 5-1 summarizes the key characteristics of the voltage rails.

Table 5-1. Summary of Voltage Regulators

RAIL	TYPE	INPUT VOLTAGE (V)		OUTPUT VOLTAGE RANGE (V)			CURRENT (mA)
		MIN	MAX	MIN	TYP	MAX	
BUCK1	Step-down Controller	4.5	21	0.41	OTP-programmable	3.575	scalable
BUCK2	Step-down Controller	4.5	21	0.41	OTP-programmable	3.575	scalable
BUCK3	Step-down Converter	4.5	5.5	0.41	OTP-programmable	3.575	3000
BUCK4	Step-down Converter	4.5	5.5	0.41	OTP-programmable	3.575	3000
BUCK5	Step-down Converter	4.5	5.5	0.41	OTP-programmable	3.575	3000
BUCK6	Step-down Controller	4.5	21	0.41	OTP-programmable	3.575	scalable
LDOA1	LDO	4.5	5.5	0.7	OTP-programmable	3.3	200 (1)
LDOA2	LDO	1.62	1.98	0.7	OTP-programmable	1.5	600
LDOA3	LDO	1.62	1.98	0.7	OTP-programmable	1.5	600
SWA1	Load Switch	0.5	3.3				300
SWB1/SWB2	Load Switch	0.5	3.3				300
VTT	Sink and Source LDO	BUCK6 output			V_{BUCK6} / 2		500

(1) When powered from a 5-V supply through the DRV5V_2_A1 pin. Otherwise, max current is limited by max I_{OUT} of LDO5.

5.2 Functional Block Diagram

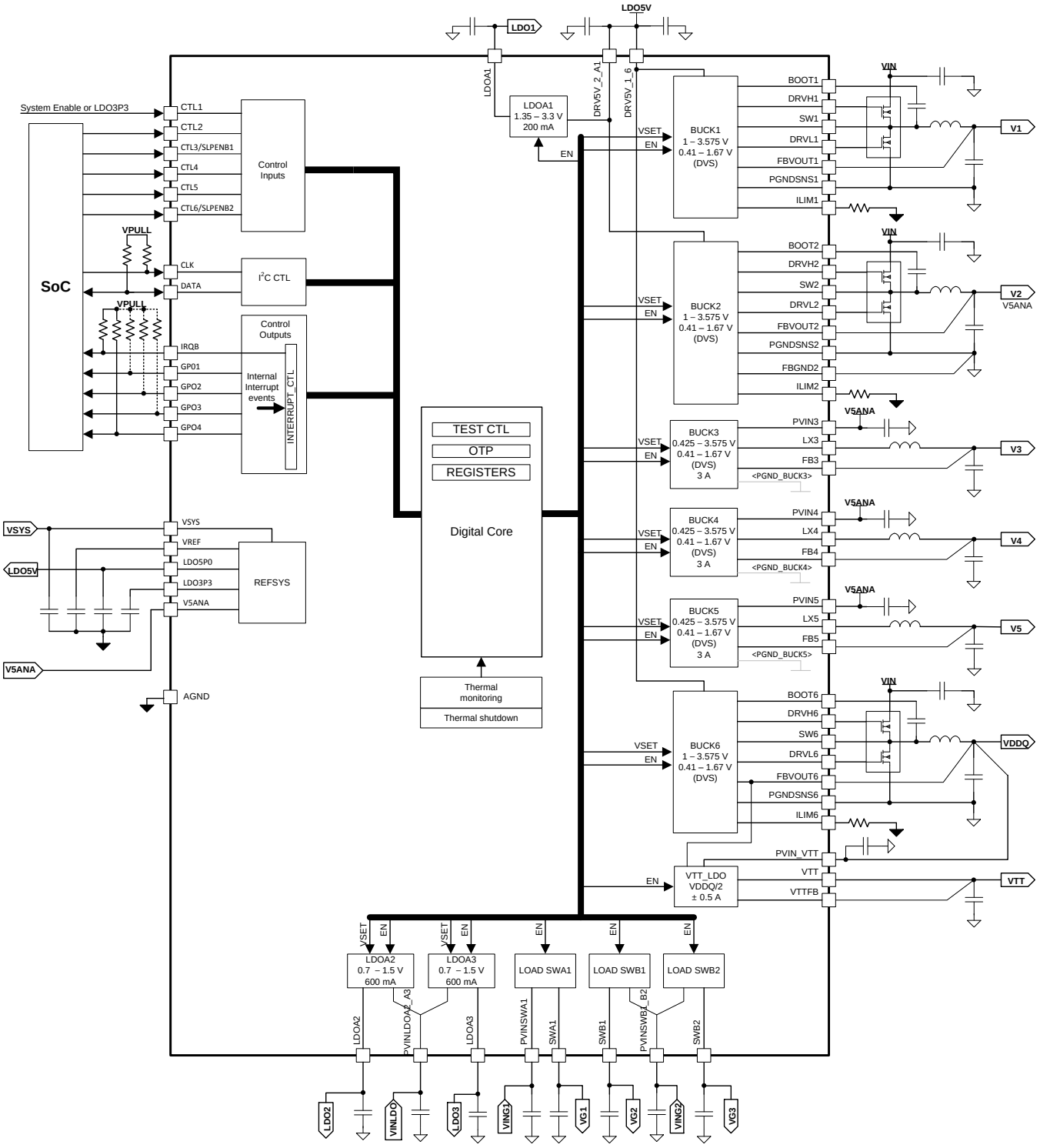


Figure 5-1. PMIC Functional Block Diagram

5.3 SMPS Voltage Regulators

The buck controllers integrate gate drivers for external power stages with programmable current limit (set by an external resistor at ILIMx pin), which allows for optimal selection of external passive components based on the desired system load. The buck converters include integrated power stage and require a minimum number of pins for power input, inductor, and output voltage feedback input. Combined with high-frequency switching, all these features allow use of inductors in small form factor, thus reducing total-system cost and size.

BUCK1–BUCK6 have selectable auto- and forced-PWM mode through the BUCKx_MODE bit in the BUCKxCTRL register. In default auto mode, the VR automatically switches between PWM and PFM depending on the output load to maximize efficiency.

All controllers and converters can be set to default V_{OUT} or dynamically voltage changing at any time. This means that the rails can be programmed for any V_{OUT} by the factory, so the device starts up with the default voltage, or during operation the rail can be programmed to another operating V_{OUT} while the rail is enable or disabled. There are two step sizes or ranges available for V_{OUT} selection: 10-mV and 25-mV steps. The step-size range must be selected prior to use and must be programmed by the factory. It is not subject to programming or change during operation.

For the 10-mV step-size range V_{OUT} options, refer to the Table 5-2. For the 25-mV step-size range V_{OUT} options, refer to the Table 5-3.

Table 5-2. 10-mV Step-Size V_{OUT} Range

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000000	0	0101011	0.83	1010110	1.26
0000001	0.41	0101100	0.84	1010111	1.27
0000010	0.42	0101101	0.85	1011000	1.28
0000011	0.43	0101110	0.86	1011001	1.29
0000100	0.44	0101111	0.87	1011010	1.30
0000101	0.45	0110000	0.88	1011011	1.31
0000110	0.46	0110001	0.89	1011100	1.32
0000111	0.47	0110010	0.90	1011101	1.33
0001000	0.48	0110011	0.91	1011110	1.34
0001001	0.49	0110100	0.92	1011111	1.35
0001010	0.50	0110101	0.93	1100000	1.36
0001011	0.51	0110110	0.94	1100001	1.37
0001100	0.52	0110111	0.95	1100010	1.38
0001101	0.53	0111000	0.96	1100011	1.39
0001110	0.54	0111001	0.97	1100100	1.40
0001111	0.55	0111010	0.98	1100101	1.41
0010000	0.56	0111011	0.99	1100110	1.42
0010001	0.57	0111100	1.00	1100111	1.43
0010010	0.58	0111101	1.01	1101000	1.44
0010011	0.59	0111110	1.02	1101001	1.45
0010100	0.60	0111111	1.03	1101010	1.46
0010101	0.61	1000000	1.04	1101011	1.47
0010110	0.62	1000001	1.05	1101100	1.48
0010111	0.63	1000010	1.06	1101101	1.49
0011000	0.64	1000011	1.07	1101110	1.50
0011001	0.65	1000100	1.08	1101111	1.51
0011010	0.66	1000101	1.09	1110000	1.52
0011011	0.67	1000110	1.10	1110001	1.53
0011100	0.68	1000111	1.11	1110010	1.54
0011101	0.69	1001000	1.12	1110011	1.55
0011110	0.70	1001001	1.13	1110100	1.56
0011111	0.71	1001010	1.14	1110101	1.57
0100000	0.72	1001011	1.15	1110110	1.58
0100001	0.73	1001100	1.16	1110111	1.59
0100010	0.74	1001101	1.17	1111000	1.60
0100011	0.75	1001110	1.18	1111001	1.61
0100100	0.76	1001111	1.19	1111010	1.62
0100101	0.77	1010000	1.20	1111011	1.63
0100110	0.78	1010001	1.21	1111100	1.64
0100111	0.79	1010010	1.22	1111101	1.65
0101000	0.80	1010011	1.23	1111110	1.66
0101001	0.81	1010100	1.24	1111111	1.67
0101010	0.82	1010101	1.25		

Table 5-3. 25-mV Step-Size V_{OUT} Range

VID Bits	V_{OUT} (Converters)	V_{OUT} (Controllers)	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000000	0	1.000	0101011	1.475	1010110	2.550
0000001	0.425	1.000	0101100	1.500	1010111	2.575
0000010	0.450	1.000	0101101	1.525	1011000	2.600
0000011	0.475	1.000	0101110	1.550	1011001	2.625
0000100	0.500	1.000	0101111	1.575	1011010	2.650
0000101	0.525	1.000	0110000	1.600	1011011	2.675
0000110	0.550	1.000	0110001	1.625	1011100	2.700
0000111	0.575	1.000	0110010	1.650	1011101	2.725
0001000	0.600	1.000	0110011	1.675	1011110	2.750
0001001	0.625	1.000	0110100	1.700	1011111	2.775
0001010	0.650	1.000	0110101	1.725	1100000	2.800
0001011	0.675	1.000	0110110	1.750	1100001	2.825
0001100	0.700	1.000	0110111	1.775	1100010	2.850
0001101	0.725	1.000	0111000	1.800	1100011	2.875
0001110	0.750	1.000	0111001	1.825	1100100	2.900
0001111	0.775	1.000	0111010	1.850	1100101	2.925
0010000	0.800	1.000	0111011	1.875	1100110	2.950
0010001	0.825	1.000	0111100	1.900	1100111	2.975
0010010	0.850	1.000	0111101	1.925	1101000	3.000
0010011	0.875	1.000	0111110	1.950	1101001	3.025
0010100	0.900	1.000	0111111	1.975	1101010	3.050
0010101	0.925	1.000	1000000	2.000	1101011	3.075
0010110	0.950	1.000	1000001	2.025	1101100	3.100
0010111	0.975	1.000	1000010	2.050	1101101	3.125
0011000	1.000	1.000	1000011	2.075	1101110	3.150
0011001	1.025	1.025	1000100	2.100	1101111	3.175
0011010	1.050	1.050	1000101	2.125	1110000	3.200
0011011	1.075	1.075	1000110	2.150	1110001	3.225
0011100	1.100	1.100	1000111	2.175	1110010	3.250
0011101	1.125	1.125	1001000	2.200	1110011	3.275
0011110	1.150	1.150	1001001	2.225	1110100	3.300
0011111	1.175	1.175	1001010	2.250	1110101	3.325
0100000	1.200	1.200	1001011	2.275	1110110	3.350
0100001	1.225	1.225	1001100	2.300	1110111	3.375
0100010	1.250	1.250	1001101	2.325	1111000	3.400
0100011	1.275	1.275	1001110	2.350	1111001	3.425
0100100	1.300	1.300	1001111	2.375	1111010	3.450
0100101	1.325	1.325	1010000	2.400	1111011	3.475
0100110	1.350	1.350	1010001	2.425	1111100	3.500
0100111	1.375	1.375	1010010	2.450	1111101	3.525
0101000	1.400	1.400	1010011	2.475	1111110	3.550
0101001	1.425	1.425	1010100	2.500	1111111	3.575
0101010	1.450	1.450	1010101	2.525		

5.3.1 Controller Overview

The controllers are fast-reacting, high-frequency, scalable output power controllers capable of driving two external N-MOSFETs. They are D-CAP2 controller scheme that optimizes transient responses at high load currents for such applications as CORE and DDR supplies. The output voltage is compared with internal reference voltage after divider resistors. The PWM comparator determines the timing to turn on the high-side MOSFET. The PWM comparator response maintains a very small PWM output ripple voltage. Because the device does not have a dedicated oscillator for control loop on board, switching cycle is controlled by the adaptive on-time circuit. The on-time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the on-time one-shot timer.

The D-CAP2 control scheme has an injected ripple from the SW node that is added on to the reference voltage to simulate output ripple, which eliminates the need for ESR-induced output ripple from D-CAP™ mode control. Thus, low-ESR output capacitors (such as low-cost ceramic MLCC capacitors) can be used with the controllers.

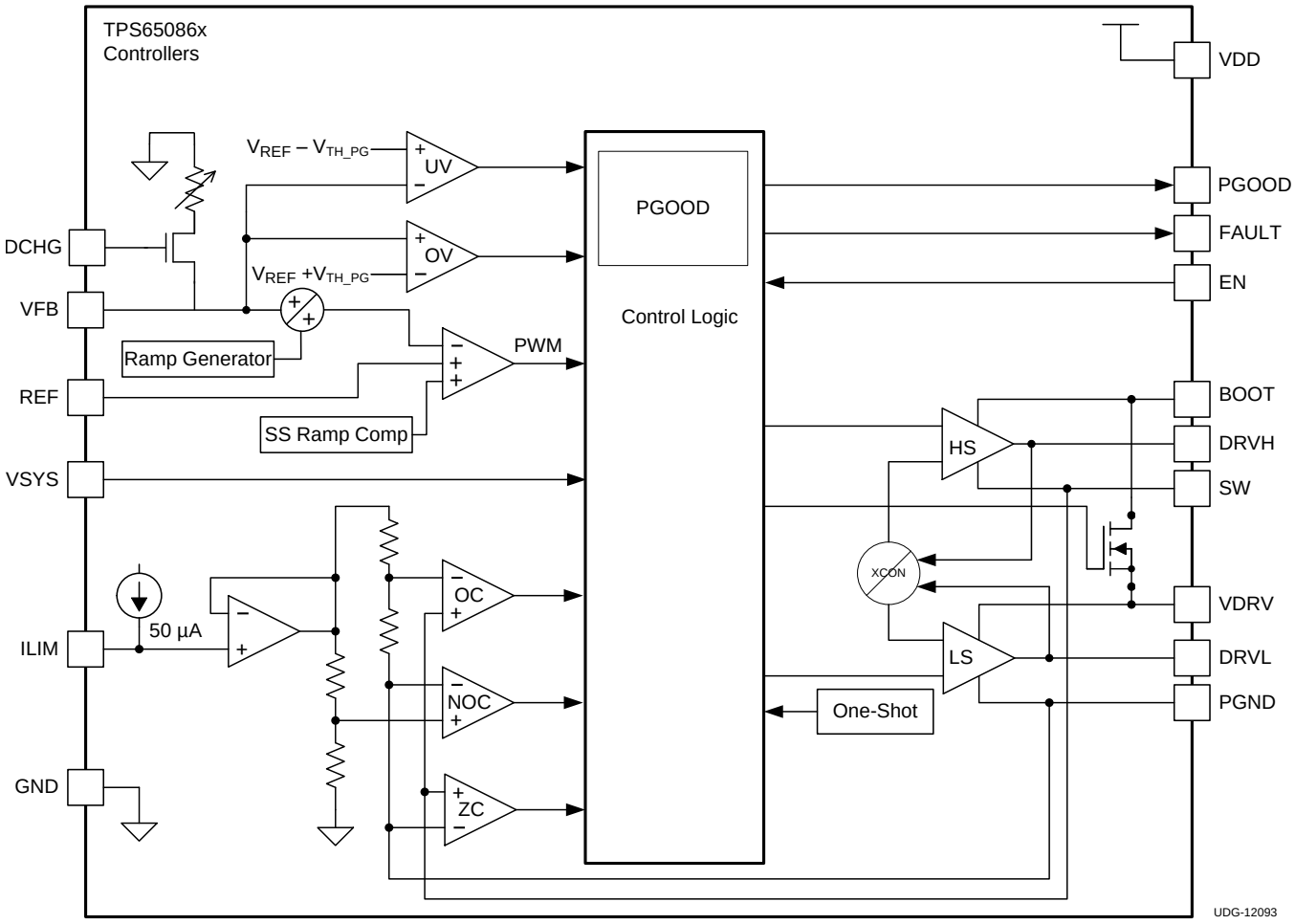


Figure 5-2. Controller Block Diagram

5.3.2 Converter Overview

The PMIC synchronous step-down DCDC converters include a unique hysteretic PWM controller scheme which enables a high switching frequency converter, excellent transient and AC load regulation as well as operation with cost-competitive external components. The controller topology supports forced PWM mode as well as power-save mode operation. Power-save mode operation, or PFM mode, reduces the quiescent current consumption and ensures high conversion efficiency at light loads by skipping switch pulses. In forced PWM mode, the device operates on a quasi-fixed frequency, avoids pulse skipping, and allows filtering of the switch noise by external filter components. The PMIC device offers fixed output voltage options featuring smallest solution size by using only three external components per converter.

A significant advantage of PMIC compared to other hysteretic PWM controller topologies is its excellent AC load transient regulation capability. When the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high-side switch is turned on. It remains turned on until a minimum ON-time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high-side switch current limit. When the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high-side switch turns on again or the inductor current reaches zero. In forced PWM mode operation, negative inductor current is allowed to enable continuous conduction mode even at no load condition.

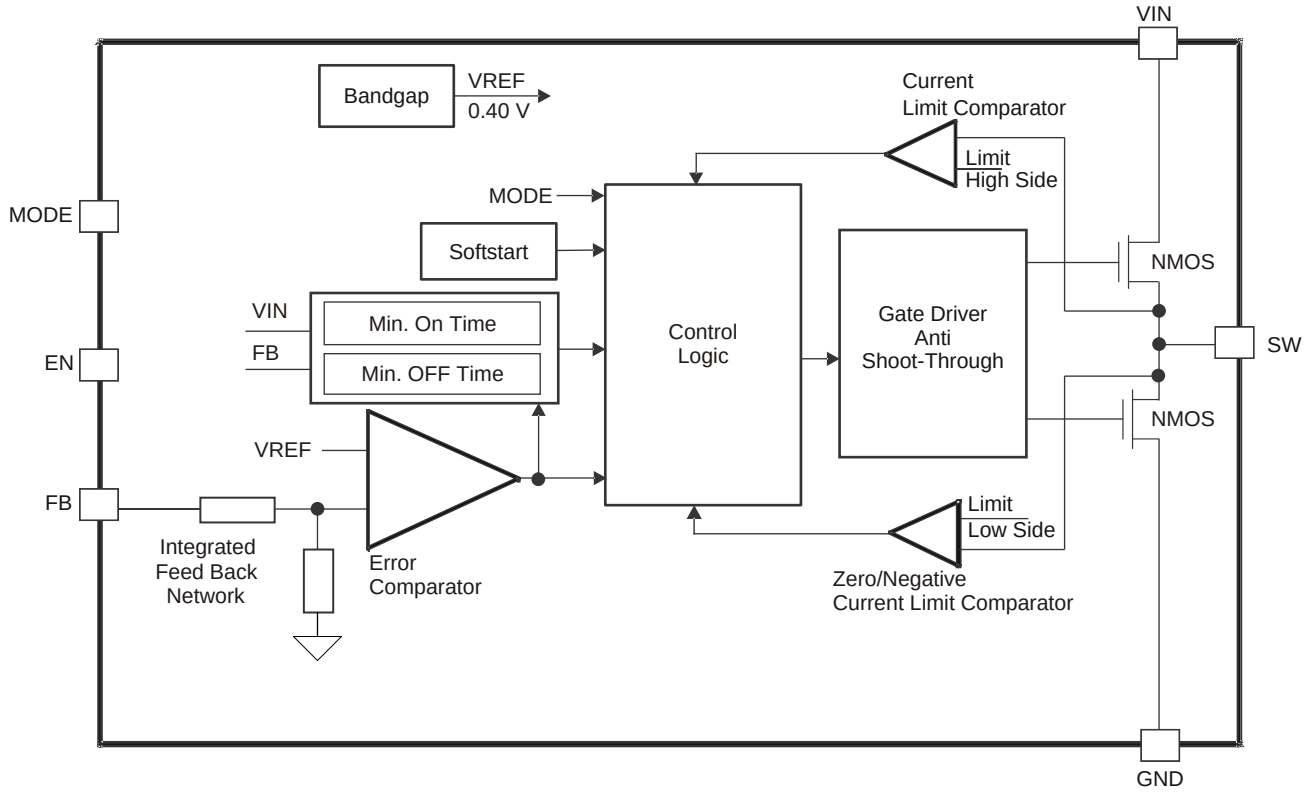


Figure 5-3. Converter Block Diagram

5.3.3 DVS

BUCK1–BUCK6 support dynamic voltage scaling (DVS) for maximum system efficiency. The VR outputs can slew up and down in either 10-mV or 25-mV steps using the 7-bit voltage ID (VID) defined in Section 4.7 and Section 4.8. DVS slew rate is minimum 2.5 mV/µs. In order to meet the minimum slew rate, VID progresses to the next code at 3-µs (nom) interval per 10-mV or at 6-µs interval per 25-mV steps. When DVS is active, the VR is forced into PWM mode, unless BUCKx_DECAY = 1, to ensure the output keeps track of VID code with minimal delay. Additionally, PGOOD is masked when DVS is in progress. An example of slew down and up from one VID to another (step size of 10 mV) is depicted in Figure 5-4.

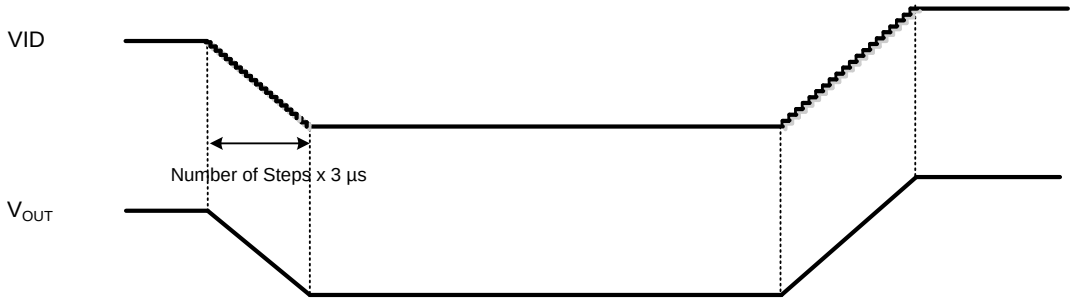


Figure 5-4. DVS Timing Diagram I (BUCKx_DECAY = 0)

As illustrated in Figure 5-5, if a BUCKx_VID[6:0] is set to 7b000 0000, its output voltage will slew down to 0.5 V first, and then will drift down to 0 V as the SMPS stops switching. Subsequently, if a BUCKx_VID[6:0] is set to a value (neither 7b000 0000 nor 7b000 0001) when its output voltage is less than 0.5 V, the VR will ramp up to 0.5 V first with soft-start kicking in, then will slew up to target voltage in the slew rate aforementioned. It must be noted that a fixed 200 µs of soft-start time is reserved for V_{OUT} to reach 0.5 V. In this case, however, the SMPS is not forced into PWM mode as it otherwise could cause V_{OUT} to droop momentarily if V_{OUT} might have been drifting above 0.5 V for any reason.

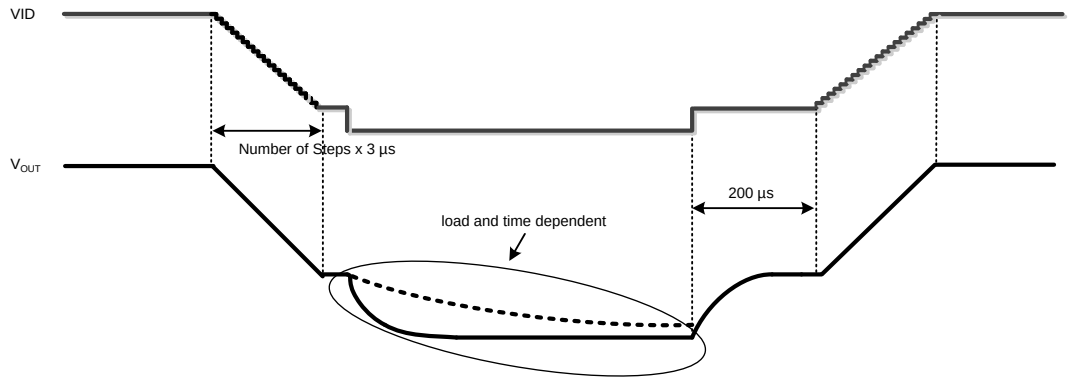


Figure 5-5. DVS Timing Diagram II (BUCKx_DECAY = 0)

5.3.4 Decay

In addition to DVS, BUCK1–BUCK6 can decay down to a lower voltage when BUCKx_DECAY bit in BUCKxCTRL register is set to 1. Decay mode is only used in a downward direction of VID. The VR does not control slew rate. As both high-side and low-side FETs stop switching, the output voltage ramps down naturally, dictated by current drawn from the load and output filtering capacitance. When the VR is in the middle of decay down its PGOOD is masked until V_{OUT} falls below the over-voltage (OV) threshold of the set VID value. Shown in Figure 5-6 are two cases that differ from each other as to whether V_{OUT} has reached the target voltage corresponding to a new VID when the VR is commanded to slew back up to a higher voltage. In case that V_{OUT} has not decayed down below VID as denoted case 2, the VR will wait for VID to catch up, and then V_{OUT} will start ramping up to keep up with the VID ramp.

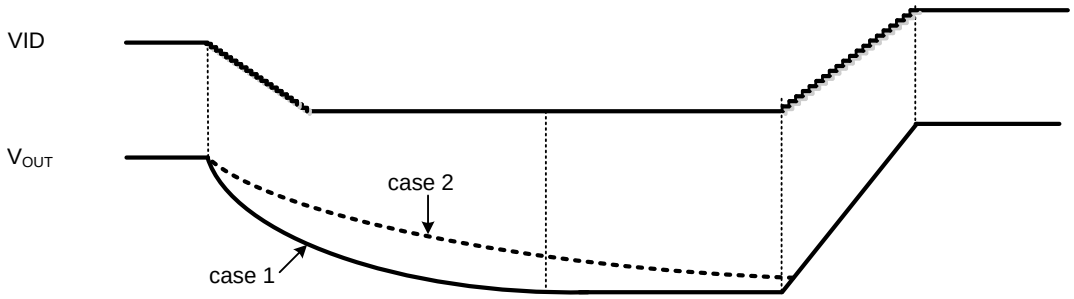


Figure 5-6. Decay Down to a Lower V_{OUT} and Slew Up

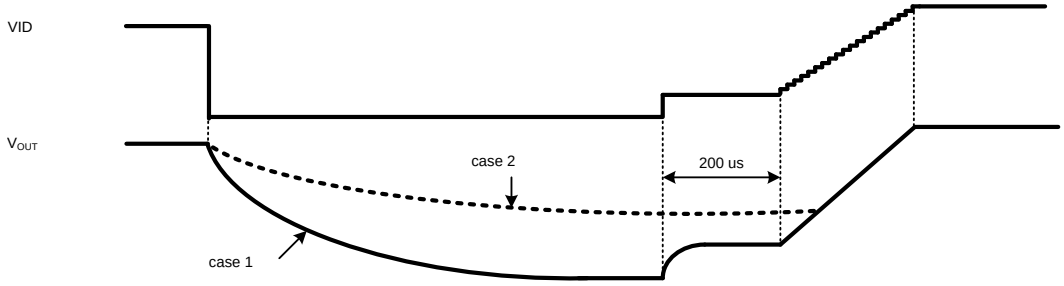


Figure 5-7. Decay Down to 0 V and Slew Up

5.3.5 Current Limit

The buck controllers (BUCK1, BUCK2, and BUCK6) have inductor-valley current-limit architecture and the current limit is programmable by an external resistor at the ILIMx pin. Equation 1 shows the calculation for a desired resistor value, depending on specific application conditions. I_{LIMREF} is the current source out of the ILIMx pin that is typically 50 µA, and R_{DSON} is the maximum channel resistance of the low-side FET. the scaling factor is 1.3 to take into account all errors and temperature variations of R_{DSON}, I_{LIMREF}, and R_{ILIM}. Finally, 8 is another scaling factor associated with I_{LIMREF}.

$$R_{ILIM} = \frac{R_{DSON} \times 8 \times 1.3 \times (I_{LIM} - \frac{I_{ripple,min}}{2})}{I_{LIMREF}} \quad (1)$$

where

- I_{LIM} is the target current limit. An appropriate margin must be allowed when determining I_{LIM} from maximum output DC load current.
- $I_{ripple,min}$ is the minimum peak-to-peak inductor ripple current for a given V_{OUT}.

$$I_{ripple,min} = \frac{V_{out}(v_{in,min} - V_{out})}{L_{max} \times V_{in,min} \times f_{sw,max}} \quad (2)$$

where

- L_{max} is maximum inductance
- $f_{sw,max}$ is maximum switching frequency
- $V_{in,min}$ minimum input voltage to the external power stage

The buck converter limit inductor peak current cycle-by-cycle to I_{IND_LIM} is specified in Section 4.8.

5.4 LDOs and Load Switches

5.4.1 VTT LDO

Powered from the BUCK6 output , VTT LDO tracks V_{BUCK6} by regulating its output to a half of its input. The LDO is capable of sinking and sourcing current up to 500 mA, and it is designed specifically to power DDR memory. The LDO core is a transconductance amplifier with large gain, and it drives a current output stage that either sources or sinks current depending on the deviation of VTTFB pin voltage from the target regulation voltage.

5.4.2 LDOA1–LDOA3

The TPS65086x device integrates three general purpose LDOs. LDOA1 is powered from a 5-V supply through the DRV5V_2_A1 pin and it can be factory configured to be an Always-On rail as long as a valid power supply is available at VSYS. See Table 5-4 for LDOA1 output voltage options. LDOA2 and LDOA3 share a power input pin (PVINLDOA2_A3). The output regulation voltages are set by writing to LDOAx_VID[3:0] bits (Reg 0x9A, 0x9B, and 0xAE). See Table 5-5 for LDOA2 and LDOA3 output voltage options. LDOA1 is controlled by LDOA1CTRL register.

Table 5-4. LDOA1 Output Voltage Options

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000	1.35	0100	1.8	1000	2.3	1100	2.85
0001	1.5	0101	1.9	1001	2.4	1101	3.0
0010	1.6	0110	2.0	1010	2.5	1110	3.3
0011	1.7	0111	2.1	1011	2.6	1111	Not Used

Table 5-5. LDOA2 and LDOA3 Output Voltage Options

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000	0.70	0100	0.90	1000	1.10	1100	1.30
0001	0.75	0101	0.95	1001	1.15	1101	1.35
0010	0.80	0110	1.00	1010	1.20	1110	1.40
0011	0.85	0111	1.05	1011	1.25	1111	1.50

5.4.3 Load Switches

The PMIC features three general purpose load switches. SWA1 has its own power input pin (PVINSWA1), while SWB1 and SWB2 share one power input pin (PVINSWB1_B2). All switches have built-in slew rate control during startup to limit the inrush current.

5.5 Power Goods (PGOOD or PG) and GPOs

The device provides information on status of VRs through four GPO pins along with Power-Good Status registers defined in Section 5.9.49 and Section 5.9.50. Power-good information of any individual VR and load switch can be assigned to be part of the PGOOD tree as defined from Section 5.9.39 to Section 5.9.46. PGOOD assertion delays are programmable from 0 ms to 15 ms for GPO1 and 0 ms to 100 ms for GPO2–GPO4, respectively, as are defined in Section 5.9.20 and Section 5.9.33.

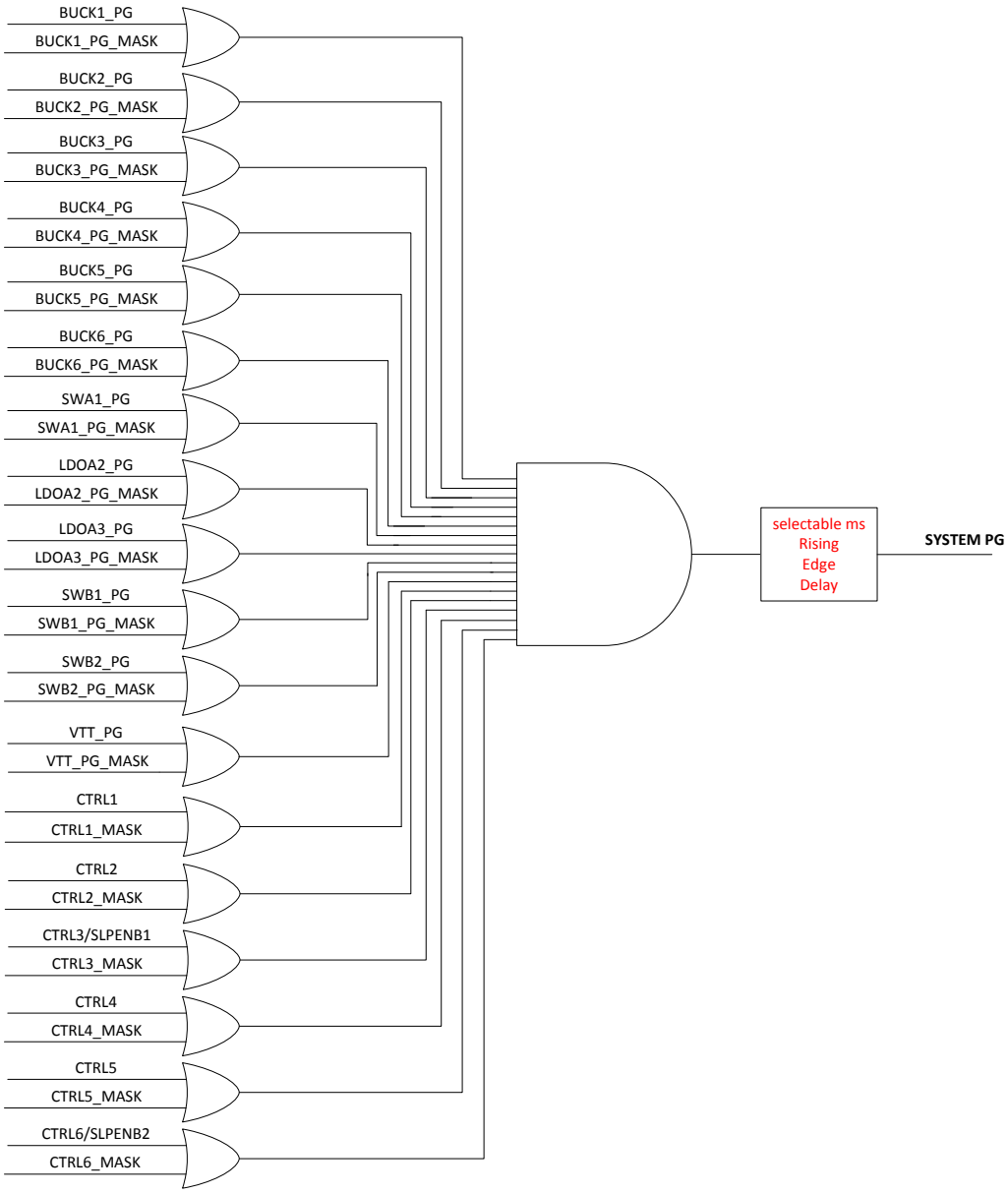


Figure 5-8. Power Good Tree

Alternatively, the GPOs can be used as general purpose outputs controlled by the user via I²C. Refer to the *I2C_RAIL_EN2/GPOCTRL Register Description* for details on controlling the GPOs in I²C control mode.

5.6 Power Sequencing and VR Control

The device has 3 different ways of sequencing the rails during power up and power down:

- Rail enabled by CTLx pin
- Rail enabled by power good, (PG), of prior enabled rail
- Rail enabled by I²C software command

A delay can be added from any CTLx pin or PG to the enable of the subjected enabled rail. This creates a very flexible device capable of many sequence options. If a rail cannot be sequenced automatically, any rail can be enabled or disabled via I^2C command.

5.6.1 CTLx Sequencing

The device has six control-input pins (CTL1–CTL6) to control six SMPS regulators, three LDO regulators, and three load switches. This allows the user to define up to six distinctive groups, to which each VR can be assigned for highly flexible power sequencing. Of the six CTLx pins, CTL3 and CTL6 can be configured alternatively to active-low sleep enable pins. For instance, if a system level SLEEP state is defined such that BUCK1 output regulation voltage is lower than in the normal mode, then BUCK2 SLEEP state can be assigned to CTL3 or CTL6. By being pulled low, either CTL3 or CTL6 can be used to put BUCK1 into SLEEP state, and BUCK1 will regulate its output at a voltage defined by BUCK1_SLP_VID[6:0] in Section 5.9.22. In the example Section 5.6.4, see how the BUCK1 is enabled from CTL1 pin for a demonstration of this feature.

5.6.2 PG Sequencing

Any rail can be sequenced by the power good of a prior rail. This can be combined with the CTLx method to allow for further sequence control and create more distinctive groups of enables than the 6 from CTLx. This also allows some of the CTLx pins to be freed up for other purposes such as logic input gates. In the example Section 5.6.4, see how the BUCK5 is enabled from the BUCK4 PG for a demonstration of this feature.

5.6.3 Enable Delay

A delay can be added to the enable of any rail after the desired CTLx & PGs are met. This allows for the option to create additional timing groups from either CTLx pins or internal PGs. In the example Section 5.6.4, see how the BUCK2 and BUCK6 are enabled after BUCK1 from CTL1 pin for a demonstration of this feature.

5.6.4 Power Up Sequence

When a valid power supply is detected at the VSYS pin as V_{SYS} crosses above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO+5V\_HYS}$, the power-up sequence is initiated by driving one of the control input pins high, followed by the rest of pins in order. Illustrated in Figure 5-9 is an example where CTL1–CTL4 are defined to control four groups of VRs, while GPO1–GPO4 are defined to provide a PGOOD status of each group. The control input pins do not necessarily have to be pulled up in a staggered manner. For instance, if CTL2 is pulled up from the preceding group of VRs before PGOOD has been asserted at GPO1, the BUCK4 enable will be delayed until the PGOOD is asserted.

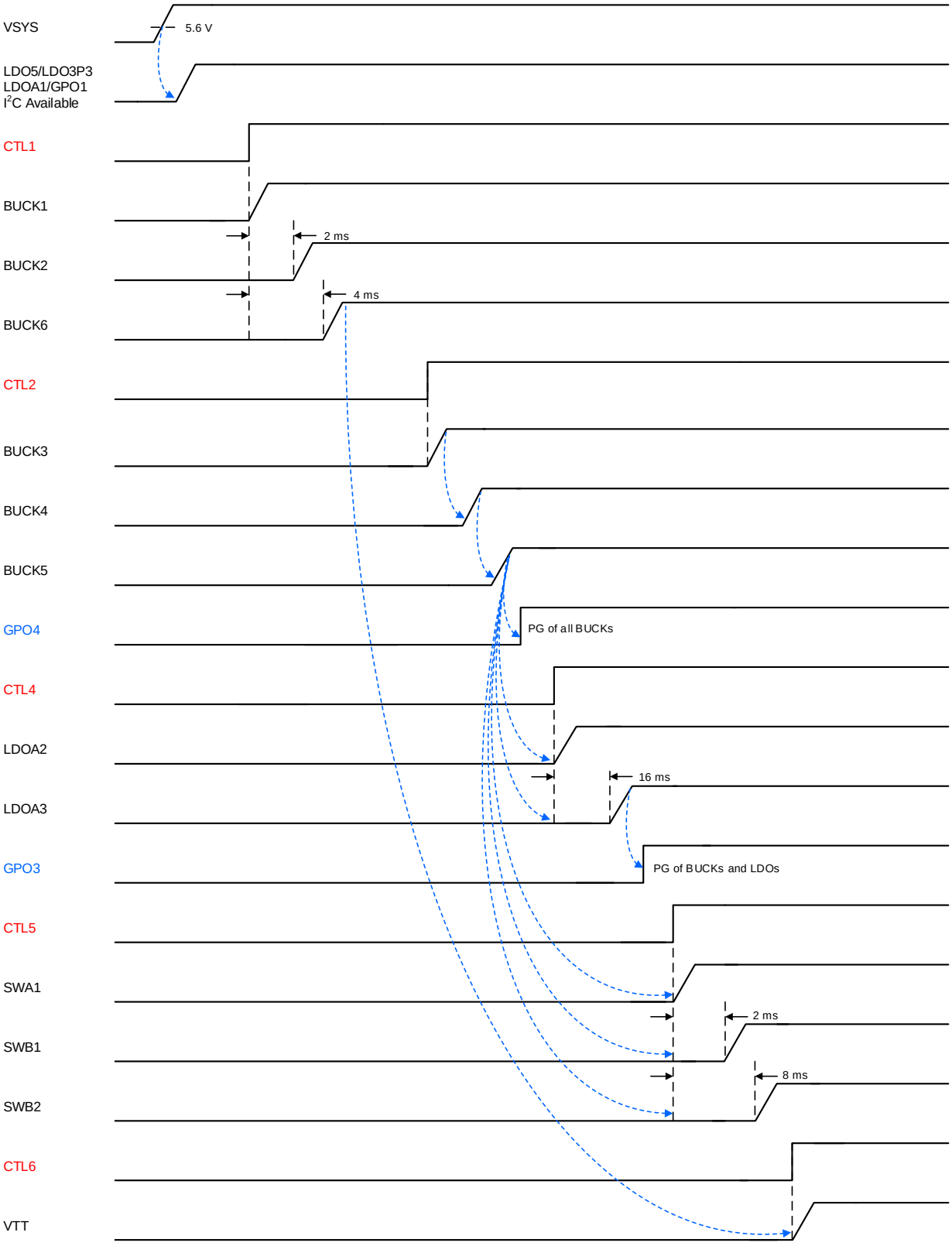


Figure 5-9. TPS650860 Power Up Sequence Example

5.6.5 Power Down Sequence

The power down sequence can follow the CTLx pins, or be controlled with the I²C commands. If the internal PGs are used for sequencing or if some rails need to ramp down before others a delay can be added to the de-assertion low of the internal enable of the subjected rail. This delay can be independent of the power up delay option. Thus, power up and power down sequences can be different of each other or relatively similar to match most applications' sequences.

Refer to Figure 5-10 for an example of a power down sequence demonstrating the delay disable of BUCK1 and BUCK2.

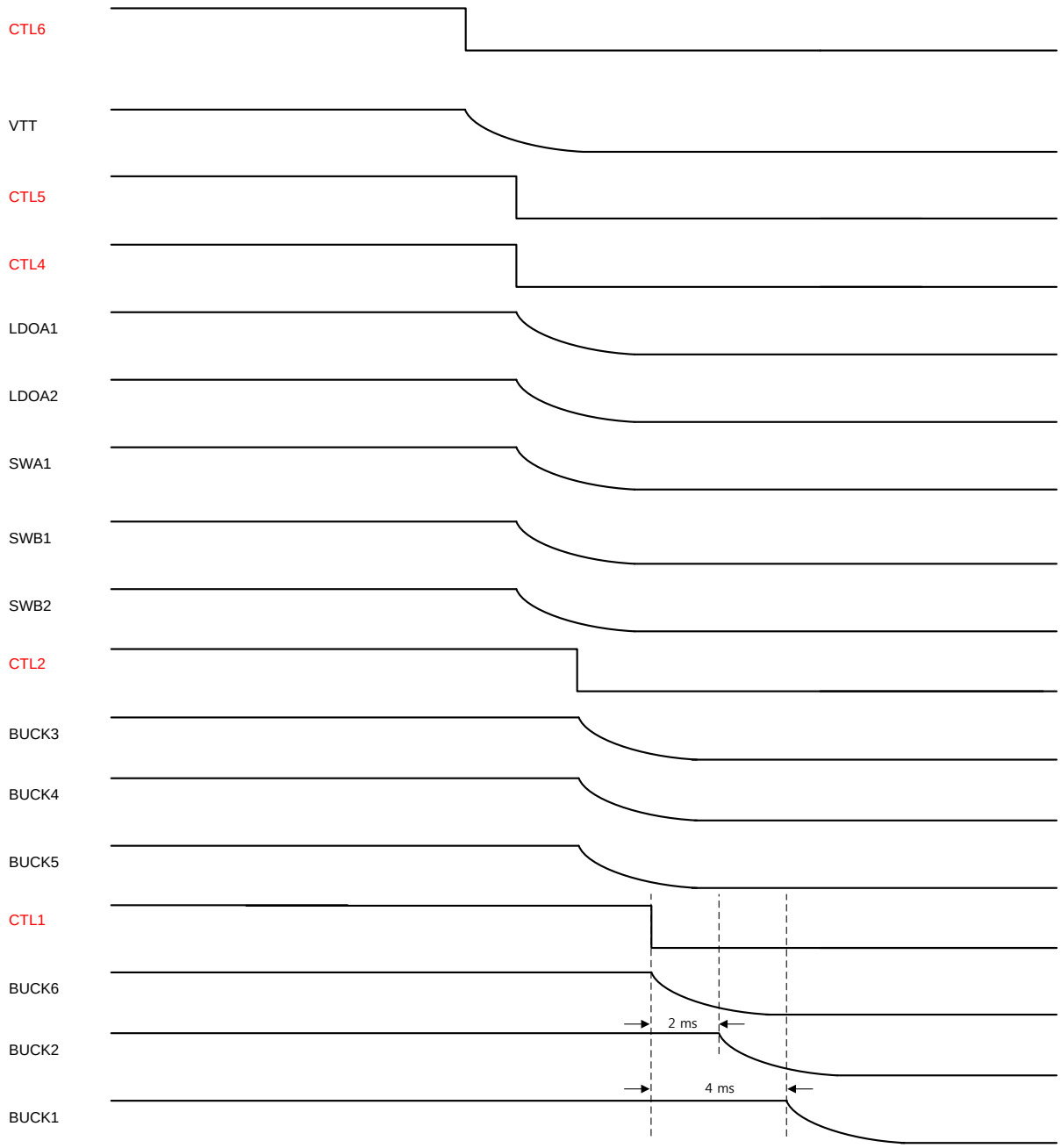


Figure 5-10. TPS650860 Power Down Sequence Example

5.6.6 Sleep State Entry and Exit

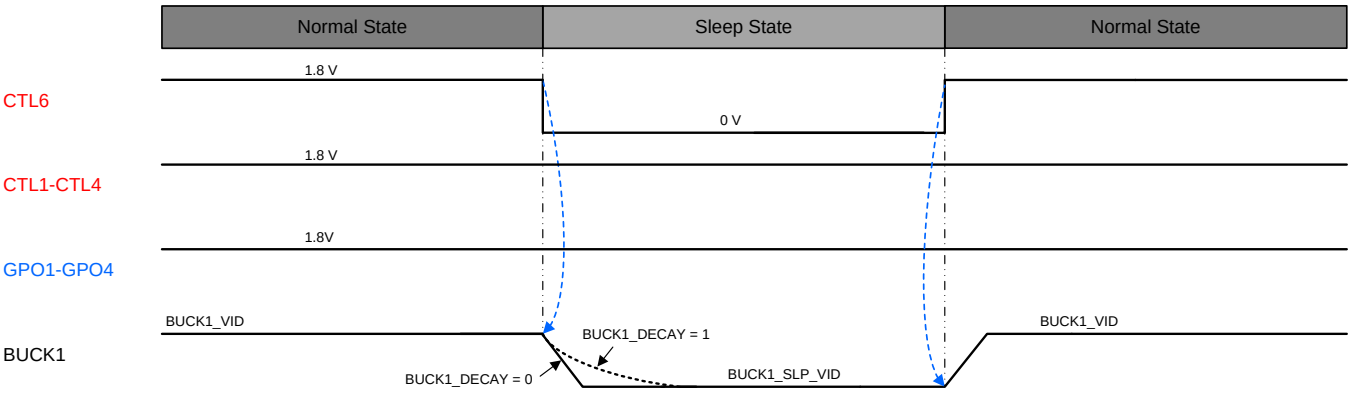


Figure 5-11. Connected Standby Entry and Exit Sequence

Section 5.6.6 illustrates an example where BUCK1 is defined to enter Sleep State in response to CTL6 going low.

NOTE

All PGOODs from GPO1–GPO4 stay asserted during the entry and the exit. Depending on status of the BUCK1_DECAY bit defined in the BUCK1CTRL register, BUCK1 output will either decay or slew down to a new voltage defined in BUCK1_SLP_VID[6:0].

5.6.7 Emergency Shutdown

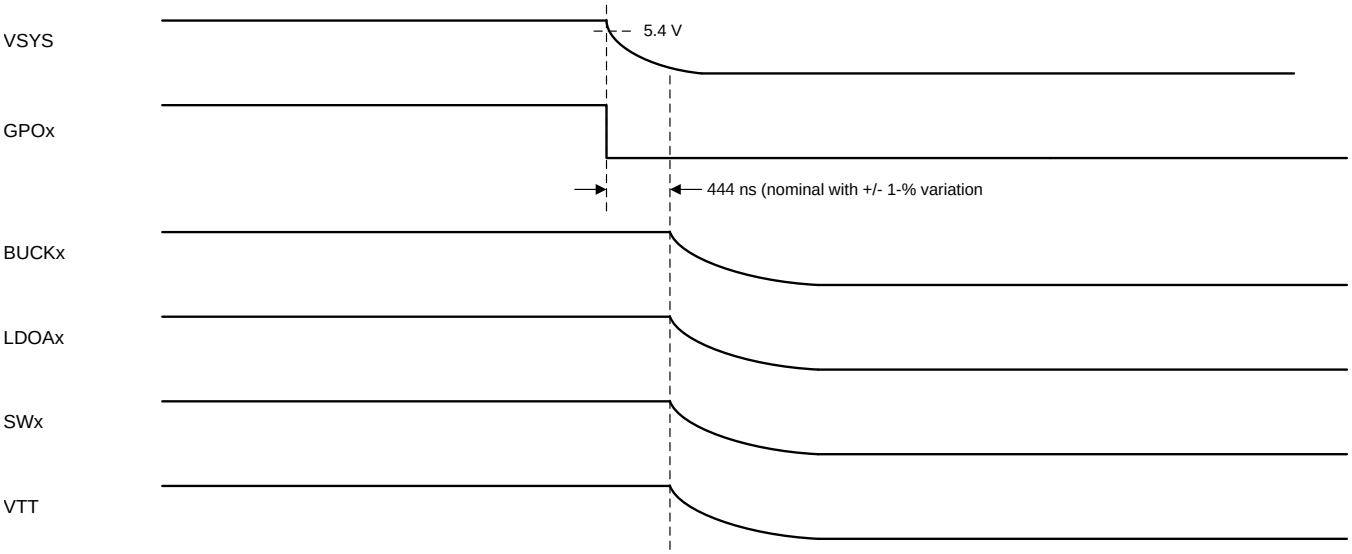


Figure 5-12. Emergency Shutdown Sequence

When V_{SYS} crosses below $V_{SYS\_UVLO\_5V}$, all power good pins will be deasserted, and after 444 ns (nom) of delay all VRs will shut down. Upon shutdown, all internal discharge resistors are set to 100 Ω to ensure timely decay of all VR outputs. Other conditions that will cause emergency shutdown are the die temperature rising above the critical temperature threshold (T_{CRIT}), and de-assertion of power good of any rail (configurable).

5.7 Device Functional Modes

5.7.1 Off Mode

When power supply at the VSYS pin is less than $V_{SYS\_UVLO\_5V}$ (5.4-V nominal) + $V_{SYS\_UVLO\_5V\_HYS}$ (0.2-V nominal), the device is in off mode, where all output rails are disabled. If the supply voltage is greater than $V_{SYS\_UVLO\_3V}$ (3.6-V nominal) + $V_{SYS\_UVLO\_3V\_HYS}$ (0.15-V nominal) while it is still less than $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, then the internal bandgap reference (VREF pin) along with LDO3P3 are enabled and regulated at target values.

5.7.2 Standby Mode

When power supply at the VSYS pin rises above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, the device enters standby mode, where all internal reference and regulators (LDO3P3 and LDO5) are up and running, and I^2C interface and CTL pins are ready to respond. All default registers defined in Section 5.9 should have been loaded from one-time programmable (OTP) memory by now. Quiescent current consumption in standby mode is specified in Section 4.5.

5.7.3 Active Mode

The device proceeds to active mode when any output rail is enabled either via an input pin as discussed in Section 5.6 or by writing to EN bits via I^2C. Output regulation voltage can also be changed by writing to VID bits defined in Section 5.9.

5.8 I^2C Interface

The I^2C interface is a 2-wire serial interface developed by NXP™ (formerly Philips Semiconductor) (see I^2C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, DATA and CLK. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS650860 device works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when V_{SYS} higher than $V_{SYS\_UVLO\_5V}$ is applied to the TPS650860 device. The I^2C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes are exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode.

The TPS650860 device supports 7-bit addressing; however, 10-bit addressing and general call address are not supported. The default device address is 0x5E.

5.8.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high (see Figure 5-13). All I^2C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 5-14). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 5-15), by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 5-13). This releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

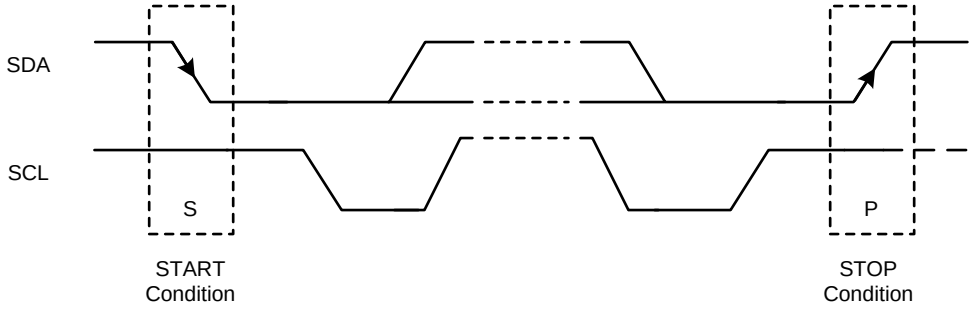


Figure 5-13. START and STOP Conditions

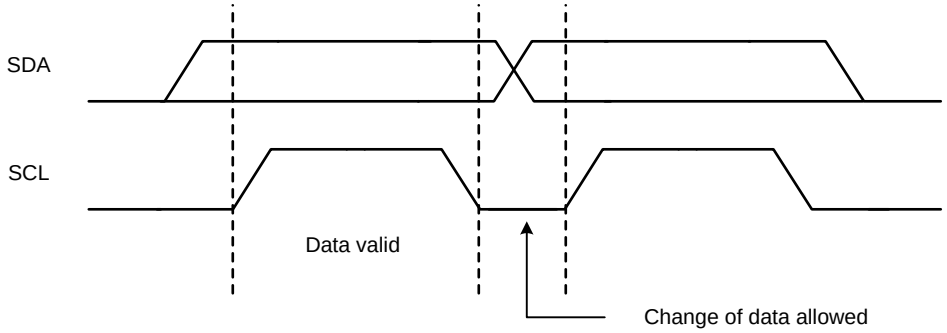


Figure 5-14. Bit Transfer on the I^2C Bus

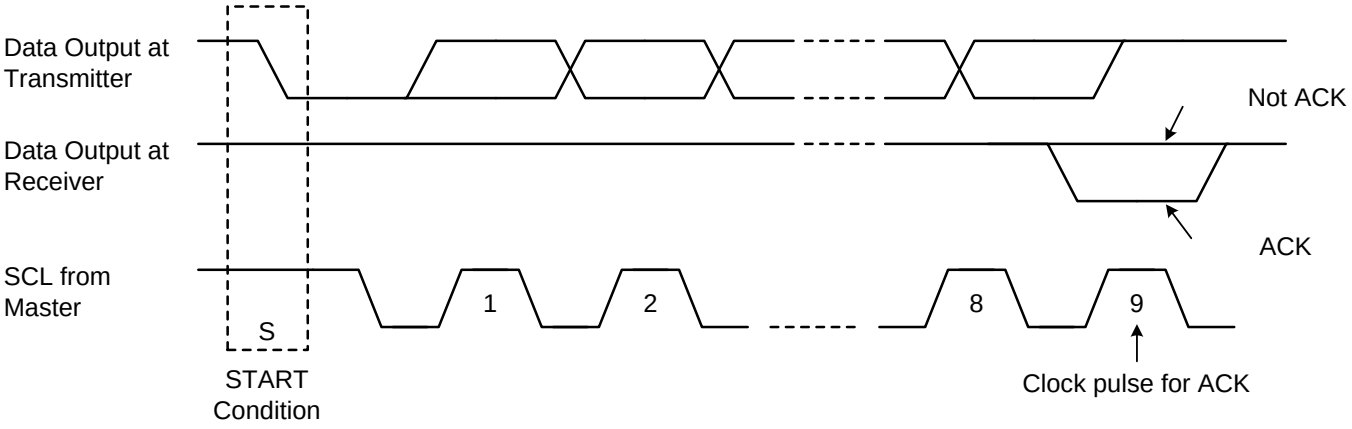


Figure 5-15. Acknowledge on the I²C Bus

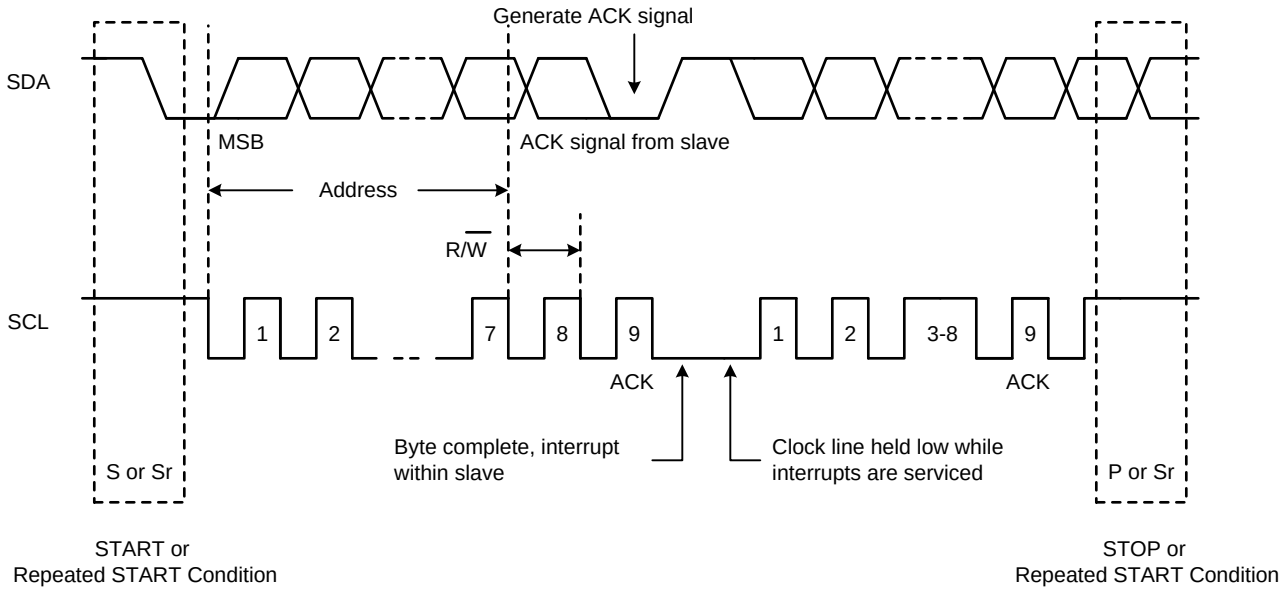


Figure 5-16. I²C Bus Protocol

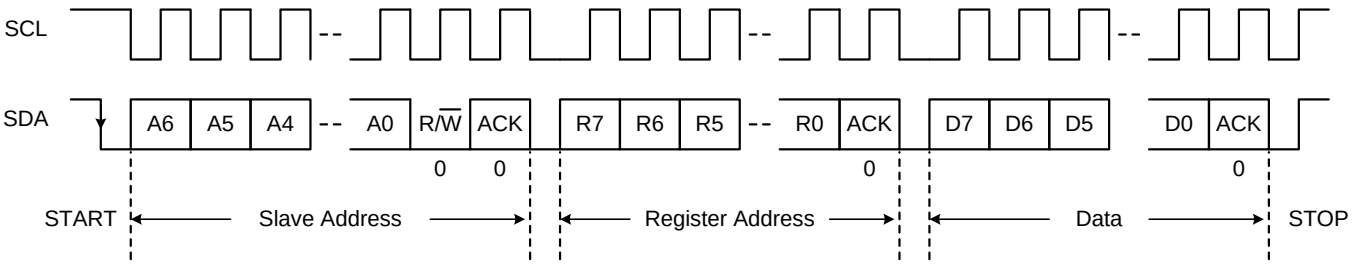


Figure 5-17. I²C Interface WRITE to TPS650860 in F/S Mode

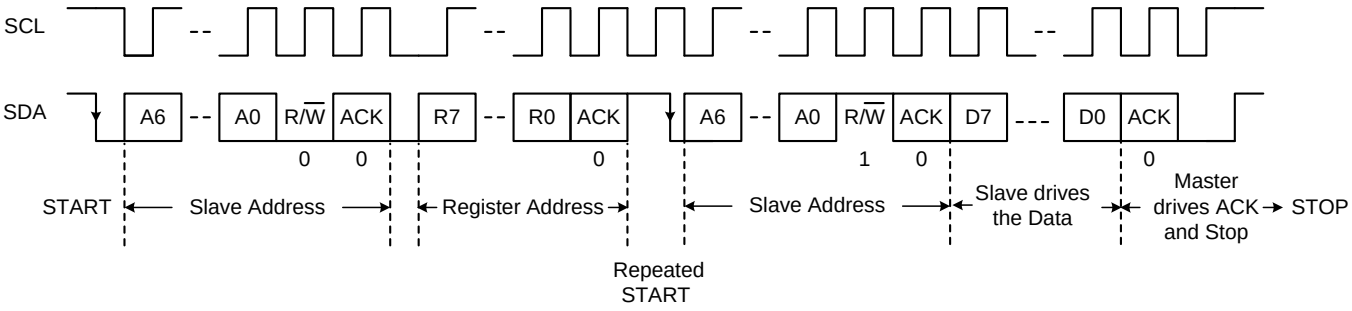


Figure 5-18. I²C Interface READ from TPS650860 in F/S Mode (Only Repeated START is Supported)

5.9 Register Maps

5.9.1 Register Map Summary

Table 5-6. Register Map Summary

Address Hex Value	Name	Short Description
1h	DEVICEID	Device ID code indicating revision
2h	IRQ	Interrupt statuses
3h	IRQ_MASK	Interrupt masking
4h	PMIC_STAT	PMIC temperature indicator
5h	SHUTDNSRC	Shutdown root cause indicator bits
20h	BUCK1CTRL	BUCK1 decay control and voltage select
21h	BUCK2CTRL	BUCK2 decay control and voltage select
22h	BUCK3DECAY	BUCK3 decay control
23h	BUCK3VID	BUCK3 voltage select
24h	BUCK3SLPCTRL	BUCK3 voltage select for sleep state
25h	BUCK4CTRL	BUCK4 control
26h	BUCK5CTRL	BUCK5 control
27h	BUCK6CTRL	BUCK6 control
28h	LDOA2CTRL	LDOA2 control
29h	LDOA3CTRL	LDOA3 control
40h	DISCHCTRL1	Discharge resistors for each rail control
41h	DISCHCTRL2	Discharge resistors for each rail control
42h	DISCHCTRL3	Discharge resistors for each rail control
43h	PG_DELAY1	System power good on GPO3 (*if GPO3 is programmed to be system PG*)
91h	FORCESHUTDN	Software force shutdown
92h	BUCK1SLPCTRL	BUCK1 voltage select for sleep state
93h	BUCK2SLPCTRL	BUCK2 voltage select for sleep state
94h	BUCK4VID	BUCK4 voltage select
95h	BUCK4SLPVID	BUCK4 voltage select for sleep state
96h	BUCK5VID	BUCK5 voltage select
97h	BUCK5SLPVID	BUCK5 voltage select for sleep state
98h	BUCK6VID	BUCK6 voltage select
99h	BUCK6SLPVID	BUCK6 voltage select for sleep state
9Ah	LDOA2VID	LDOA2 voltage select
9Bh	LDOA3VID	LDOA3 voltage select
9Ch	BUCK123CTRL	BUCK1, 2, and 3 disable and PFM/PWM mode control
9Dh	PG_DELAY2	System power good on GPO1, 2, and 4 (*if GPOs is programmed to be system PG*)
9Fh	SWVTT_DIS	SWs & VTT I^2C disable bits
A0h	I2C_RAIL_EN1	I^2C Enable control of individual rails
A1h	I2C_RAIL_EN2/GPOCTRL	I^2C Enable control of individual rails and I^2C controlled GPOs, high or low
A2h	PWR_FAULT_MASK1	Power fault masking for individual rails
A3h	PWR_FAULT_MASK2	Power fault masking for individual rails
A4h	GPO1PG_CTRL1	Power good tree control for GPO1
A5h	GPO1PG_CTRL2	Power good tree control for GPO1
A6h	GPO4PG_CTRL1	Power good tree control for GPO4
A7h	GPO4PG_CTRL2	Power good tree control for GPO4
A8h	GPO2PG_CTRL1	Power good tree control for GPO2

Table 5-6. Register Map Summary (continued)

Address Hex Value	Name	Short Description
A9h	GPO2PG_CTRL2	Power good tree control for GPO2
AAh	GPO3PG_CTRL1	Power good tree control for GPO3
ABh	GPO3PG_CTRL2	Power good tree control for GPO3
ACh	MISCSYSPG	Power good tree control with CTL3 and CTL6 for GPO
AEh	LDOA1CTRL	LDOA1 control for discharge, voltage selection, and enable
B0h	PGSTATUS1	Power good statuses for individual rails
B1h	PGSTATUS2	Power good statuses for individual rails
B2h	PWR_FAULT_STATUS1	Power fault statuses for individual rails
B3h	PWR_FAULT_STATUS2	Power fault statuses for individual rails
B4h	TEMPCRIT	Critical temperature indicators
B5h	TEMPHOT	Hot temperature indicators

The user must not attempt to write a RESERVED R/W bit to the opposite value.

5.9.2 DEVICEID: PMIC Device and Revision ID Register (offset = 1h) [reset = OTP-Programmable]

Figure 5-19. DEVICEID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	REVID[1]	REVID[0]	OTP_ VERSION[1]	OTP_ VERSION[0]	PART_ NUMBER[3]	PART_ NUMBER[2]	PART_ NUMBER[1]	PART_ NUMBER[0]
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-7. DEVICEID Register Descriptions

Bit	Field	Type	Reset	Description
7-6	REVID[1:0]	R	OTP-Programmable	Silicon revision ID
5-4	OTP_VERSION[1:0]	R	OTP-Programmable	OTP variation ID **00**: A **01**: B **10**: C **11**: D
3-0	PART_NUMBER[3:0]	R	OTP-Programmable	Device part number ID **0000**: TPS650860 **0001**: TPS650861 ... **1111**: TPS65086F

5.9.3 IRQ: PMIC Interrupt Register (offset = 2h) [reset = 0000 0000]

Figure 5-20. IRQ Register

Bit	7	6	5	4	3	2	1	0
Bit Name	FAULT	RESERVED	RESERVED	RESERVED	SHUTDN	RESERVED	RESERVED	DIETEMP
TPS650860	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R/W	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-8. IRQ Register Descriptions

Bit	Field	Type	Reset	Description
7	FAULT	R/W	0	Fault interrupt. Asserted when either condition occurs: power fault of any rail, or die temperature crosses over the critical temperature threshold (T_{CRIT}). The user can read ***Reg. 0xB2–0xB6*** to determine what has caused the interrupt. **0**: Not asserted **1**: Asserted. Host to write 1 to clear.
3	SHUTDN	R/W	0	Asserted when PMIC shuts down. To clear indicator, SHUTDNSRC must be cleared first, see Section 5.9.6 **0**: Not asserted. **1**: Asserted. Host to write 1 to clear.
0	DIETEMP	R/W	0	Die temp interrupt. Asserted when PMIC die temperature crosses above the hot temperature threshold (T_{HOT}). **0**: Not asserted. **1**: Asserted. Host to write 1 to clear.

5.9.4 IRQ_MASK: PMIC Interrupt Mask Register (offset = 3h) [reset = 1111 1111]

Figure 5-21. IRQ_MASK Register

Bit	7	6	5	4	3	2	1	0
Bit Name	MFAULT	RESERVED	RESERVED	RESERVED	MSHUTDN	RESERVED	RESERVED	MDIETEMP
TPS650860	1	1	1	1	1	1	1	1
Access	R/W	R	R	R	R/W	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-9. IRQ_MASK Register Descriptions

Bit	Field	Type	Reset	Description
7	MFAULT	R/W	1	FAULT interrupt mask. **0**: Not masked. **1**: Masked.
3	MSHUTDN	R/W	1	PMIC shutdown event interrupt mask **0**: Not masked. **1**: Masked.
0	MDIETEMP	R/W	1	Die temp interrupt mask. **0**: Not masked. **1**: Masked.

5.9.5 PMICSTAT: PMIC Status Register (offset = 4h) [reset = 0000 0000]

Figure 5-22. PMICSTAT Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SDIETEMP
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-10. PMICSTAT Register Descriptions

Bit	Field	Type	Reset	Description
0	SDIETEMP	R	0	PMIC die temperature status. **0**: PMIC die temperature is below T_{HOT}. **1**: PMIC die temperature is above T_{HOT}.

5.9.6 SHUTDNSRC: PMIC Shut-Down Event Register (offset = 5h) [reset = 0000 0000]

Figure 5-23. SHUTDNSRC Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	COLDOFF	UVLO	OCP	CRITTEMP
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-11. SHUTDNSRC Register Descriptions

Bit	Field	Type	Reset	Description
3	COLDOFF	R/W	0	Set by PMIC cleared by host. Host to write 1 to clear. This bit is always 0 for TPS650860. **0** = Cleared **1**= PMIC was shut down by pulling down ***CTL1*** pin.
2	UVLO	R/W	0	Set by PMIC cleared by host. Host to write 1 to clear. **0** = Cleared **1**= PMIC was shut down due to a UVLO event (V_{SYS} crosses below 5.4 V). Assertion of this bit sets the SHUTDN bit in Section 5.9.3.
1	OCP	R/W	0	Set by PMIC cleared by host. Host to write 1 to clear. **0** = Cleared **1**= PMIC was shut down due to an overcurrent event from BUCK1, BUCK2, BUCK6, or VTT LDO. Assertion of this bit sets the SHUTDN bit in Section 5.9.3.
0	CRITTEMP	R/W	0	Set by PMIC cleared by host. Host to write 1 to clear. **0** = Cleared **1**= PMIC was shut down due to the rise of PMIC die temperature above critical temperature threshold (T_{CRIT}). Assertion of this bit sets the SHUTDN bit in Section 5.9.3.

5.9.7 BUCK1CTRL: BUCK1 Control Register (offset = 20h) [reset = OTP-Programmable]

Figure 5-24. BUCK1CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK1_ VID[6]	BUCK1_ VID[5]	BUCK1_ VID[4]	BUCK1_ VID[3]	BUCK1_ VID[2]	BUCK1_ VID[1]	BUCK1_ VID[0]	BUCK1_ DECAY
TPS650860	1	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-12. BUCK1CTRL Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK1_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK1 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK1_DECAY	R/W	OTP-Programmable	Decay Bit **0**: The output slews down to a lower voltage set by the VID bits. **1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

5.9.8 BUCK2CTRL: BUCK2 Control Register (offset = 21h) [reset = OTP-Programmable]

Figure 5-25. BUCK2CTRL Register (offset = 21h) [reset = OTP-Programmable]

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK2_ VID[6]	BUCK2_ VID[5]	BUCK2_ VID[4]	BUCK2_ VID[3]	BUCK2_ VID[2]	BUCK2_ VID[1]	BUCK2_ VID[0]	BUCK2_ DECAY
TPS650860	1	1	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-13. BUCK2CTRL Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK2_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK2 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK2_DECAY	R/W	OTP-Programmable	Decay Bit **0**: The output slews down to a lower voltage set by the VID bits. **1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

5.9.9 BUCK3DECAY: BUCK3 Decay Control Register (offset = 22h) [reset = OTP-Programmable]

Figure 5-26. BUCK3DECAY Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK3_DECAY
TPS650860	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-14. BUCK3DECAY Register Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0	Reserved **X**: Reserved bit are do not care, can be 1 or 0.
0	BUCK3_DECAY	R/W	OTP-Programmable	Decay Bit **0**: The output slews down to a lower voltage set by the VID bits. **1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

5.9.10 BUCK3VID: BUCK3 VID Register (offset = 23h) [reset = OTP-Programmable]

Figure 5-27. BUCK3VID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK3_VID[6]	BUCK3_VID[5]	BUCK3_VID[4]	BUCK3_VID[3]	BUCK3_VID[2]	BUCK3_VID[1]	BUCK3_VID[0]	RESERVED
TPS650860	1	0	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-15. BUCK3VID Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK3_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK3 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.

5.9.11 BUCK3SLPCTRL: BUCK3 Sleep Control VID Register (offset = 24h) [reset = OTP-Programmable]

Figure 5-28. BUCK3SLPCTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK3_SLP_VID[6]	BUCK3_SLP_VID[5]	BUCK3_SLP_VID[4]	BUCK3_SLP_VID[3]	BUCK3_SLP_VID[2]	BUCK3_SLP_VID[1]	BUCK3_SLP_VID[0]	BUCK3_SLP_EN
TPS650860	1	0	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-16. BUCK3SLPCTRL Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK3_SLP_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK3 regulator output regulation voltage in sleep mode. BUCK3_SLP_VID bits are copied to BUCK3_VID bits upon enters sleep mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK3_SLP_EN	R/W	OTP-Programmable	BUCK3 sleep mode enable. For this bit to be effective, BUCK3 must be factory configured to enter sleep mode either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. **0**: Disable. **1**: Enable.

5.9.12 BUCK4CTRL: BUCK4 Control Register (offset = 25h) [reset = OTP-Programmable]

Figure 5-29. BUCK4CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK4_MODE	BUCK4_DIS
TPS650860	0	0	1	1	1	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-17. BUCK4CTRL Register Descriptions

Bit	Field	Type	Reset	Description
5:2	RESERVED	R/W	1111	Reserved bits: Do not write to 0. These bits must stay 1 for sleep control reasons.
1	BUCK4_MODE	R/W	OTP-Programmable	This field sets the BUCK4 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
0	BUCK4_DIS	R/W	OTP-Programmable	BUCK4 Disable Bit. Writing 0 to this bit forces BUCK4 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable **1**: Enable

5.9.13 BUCK5CTRL: BUCK5 Control Register (offset = 26h) [reset = OTP-Programmable]

Figure 5-30. BUCK5CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK5_MODE	BUCK5_DIS
TPS650860	0	0	1	1	1	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-18. BUCK5CTRL Register Descriptions

Bit	Field	Type	Reset	Description
5:2	RESERVED	R/W	1111	Reserved bits: Do not write to 0. These bits must stay 1 for sleep control reasons.
1	BUCK5_MODE	R/W	OTP-Programmable	This field sets the BUCK5 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
0	BUCK5_DIS	R/W	OTP-Programmable	BUCK5 Disable Bit. Writing 0 to this bit forces BUCK5 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable. **1**: Enable.

5.9.14 BUCK6CTRL: BUCK6 Control Register (offset = 27h) [reset = OTP-Programmable]

Figure 5-31. BUCK6CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK6_MODE	BUCK6_DIS
TPS650860	0	0	1	1	1	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-19. BUCK6CTRL Register Descriptions

Bit	Field	Type	Reset	Description
5:2	RESERVED	R/W	1111	Reserved bits: Do not write to 0. These bits must stay 1 for sleep control reasons.
1	BUCK6_MODE	R/W	OTP-Programmable	This field sets the BUCK6 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
0	BUCK6_DIS	R/W	OTP-Programmable	BUCK6 Disable Bit. Writing 0 to this bit forces BUCK6 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable. **1**: Enable.

5.9.15 LDOA2CTRL: LDOA2 Control Register (offset = 28h) [reset = OTP-Programmable]

Figure 5-32. LDOA2CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDOA2_DIS
TPS650860	0	0	1	1	1	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-20. LDOA2CTRL Register Descriptions

Bit	Field	Type	Reset	Description
5:2	RESERVED	R/W	1111	Reserved bits: Do not write to 0. These bits must stay 1 for sleep control reasons.
0	LDOA2_DIS	R/W	OTP-Programmable	LDOA2 Disable Bit. Writing 0 to this bit forces LDOA2 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable. **1**: Enable.

5.9.16 LDOA3CTRL: LDOA3 Control Register (offset = 29h) [reset = OTP-Programmable]

Figure 5-33. LDOA3CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDOA3_DIS
TPS650860	0	0	1	1	1	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-21. LDOA3CTRL Register Descriptions

Bit	Field	Type	Reset	Description
5:2	RESERVED	R/W	1111	Reserved bits: Do not write to 0. These bits must stay 1 for sleep control reasons.
0	LDOA3_DIS	R/W	OTP-Programmable	LDOA3 Disable Bit. Writing 0 to this bit forces LDOA3 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable **1**: Enable

5.9.17 DISCHCTRL1: Discharge Control1 Register (offset = 40h) [reset = OTP-Programmable]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

Figure 5-34. DISCHCTRL1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK4_ DISCHG[1]	BUCK4_ DISCHG[0]	BUCK3_ DISCHG[1]	BUCK3_ DISCHG[0]	BUCK2_ DISCHG[1]	BUCK2_ DISCHG[0]	BUCK1_ DISCHG[1]	BUCK1_ DISCHG[0]
TPS650860	0	1	0	1	0	1	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-22. DISCHCTRL1 Register Descriptions

Bit	Field	Type	Reset	Description
7-6	BUCK4_DISCHG[1:0]	R/W	OTP-Programmable	BUCK4 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5-4	BUCK3_DISCHG[1:0]	R/W	OTP-Programmable	BUCK3 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
3-2	BUCK2_DISCHG[1:0]	R/W	OTP-Programmable	BUCK2 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1-0	BUCK1_DISCHG[1:0]	R/W	OTP-Programmable	BUCK1 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

5.9.18 DISCHCTRL2: Discharge Control2 Register (offset = 41h) [reset = OTP-Programmable]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

Figure 5-35. DISCHCTRL2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_ DISCHG[1]	LDOA2_ DISCHG[0]	SWA1_ DISCHG[1]	SWA1_ DISCHG[0]	BUCK6_ DISCHG[1]	BUCK6_ DISCHG[0]	BUCK5_ DISCHG[1]	BUCK5_ DISCHG[0]
TPS650860	0	1	0	1	0	1	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-23. DISCHCTRL2 Register Descriptions

Bit	Field	Type	Reset	Description
7-6	LDOA2_DISCHG[1:0]	R/W	OTP-Programmable	LDOA2 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5-4	SWA1_DISCHG[1:0]	R/W	OTP-Programmable	SWA1 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
3-2	BUCK6_DISCHG[1:0]	R/W	OTP-Programmable	BUCK6 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1-0	BUCK5_DISCHG[1:0]	R/W	OTP-Programmable	BUCK5 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

5.9.19 DISCHCTRL3: Discharge Control3 Register (offset = 42h) [reset = OTP-Programmable]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

Figure 5-36. DISCHCTRL3 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	SWB2_ DISCHG[1]	SWB2_ DISCHG[0]	SWB1_ DISCHG[1]	SWB1_ DISCHG[0]	LDOA3_ DISCHG[1]	LDOA3_ DISCHG[0]
TPS650860	0	0	0	1	0	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-24. DISCHCTRL3 Register Descriptions

Bit	Field	Type	Reset	Description
5-4	SWB2_DISCHG[1:0]	R/W	OTP-Programmable	SWB2 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
3-2	SWB1_DISCHG[1:0]	R/W	OTP-Programmable	SWB1 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1-0	LDOA3_DISCHG[1:0]	R/W	OTP-Programmable	LDOA3 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

5.9.20 PG_DELAY1: Power Good Delay1 Register (offset = 43h) [reset = OTP-Programmable]

Programmable Power Good delay for GPO3 pin, measured from the moment when all VRs assigned to GPO3 pin reach their regulation range to Power Good assertion. This is an optional register as the PMIC can be programmed for system PG, level shifter or I^2C controller GPO.

Figure 5-37. PG_DELAY1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPO3_PG_ DELAY[2]	GPO3_PG_ DELAY[1]	GPO3_PG_ DELAY[0]
TPS650860	0	0	0	0	0	1	1	1
Access	R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-25. PG_DELAY1 Register Descriptions

Bit	Field	Type	Reset	Description
2-0	GPO3_PG_DELAY[2:0]	R/W	OTP-Programmable	Programmable delay power good or level shifter for GPO3 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10 % variation **000** = 2.5 ms **001** = 5.0 ms **010** = 10 ms **011** = 15 ms **100** = 20 ms **101** = 50 ms **110** = 75 ms **111** = 100 ms **XXX** = Register not used

5.9.21 FORCESHUTDN: Force Emergency Shutdown Control Register (offset = 91h) [reset = 0000 0000]

Figure 5-38. FORCESHUTDN Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SDWN
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-26. FORCESHUTDN Register Descriptions

Bit	Field	Type	Reset	Description
0	SDWN	R/W	0	Forces reset of the PMIC and reset of all registers. The bit is self-clearing. **0** = No action. **1** = PMIC is forced to shut down.

5.9.22 BUCK1SLPCTRL: BUCK1 Sleep Control Register (offset = 92h) [reset = OTP-Programmable]

Figure 5-39. BUCK1SLPCTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK1_ SLP_ VID[6]	BUCK1_ SLP_ VID[5]	BUCK1_ SLP_ VID[4]	BUCK1_ SLP_ VID[3]	BUCK1_ SLP_ VID[2]	BUCK1_ SLP_ VID[1]	BUCK1_ SLP_ VID[0]	BUCK1_ SLP_ EN
TPS650860	1	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-27. BUCK1SLPCTRL Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK1_SLP_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK1 regulator output regulation voltage in sleep mode. Mapping between bits and output voltage is defined as in Section 5.9.7.
0	BUCK1_SLP_EN	R/W	OTP-Programmable	BUCK1 sleep mode enable. For this bit to be effective, BUCK1 must be factory configured to enter sleep mode either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. **0**: Disable. **1**: Enable.

5.9.23 BUCK2SLPCTRL: BUCK2 Sleep Control Register (offset = 93h) [reset = OTP-Programmable]

Figure 5-40. BUCK2SLPCTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK2_SLP_VID[6]	BUCK2_SLP_VID[5]	BUCK2_SLP_VID[4]	BUCK2_SLP_VID[3]	BUCK2_SLP_VID[2]	BUCK2_SLP_VID[1]	BUCK2_SLP_VID[0]	BUCK2_SLP_EN
TPS650860	1	1	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-28. BUCK2SLPCTRL Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK2_SLP_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK2 regulator output regulation voltage in sleep mode. Mapping between bits and output voltage is defined as in Section 5.9.8.
0	BUCK2_SLP_EN	R/W	OTP-Programmable	BUCK2 sleep mode enable. For this bit to be effective, BUCK2 must be factory configured to enter sleep mode either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. **0**: Disable. **1**: Enable.

5.9.24 BUCK4VID: BUCK4 VID Register (offset = 94h) [reset = OTP-Programmable]

Figure 5-41. BUCK4VID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK4_VID[6]	BUCK4_VID[5]	BUCK4_VID[4]	BUCK4_VID[3]	BUCK4_VID[2]	BUCK4_VID[1]	BUCK4_VID[0]	BUCK4_DECAY
TPS650860	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-29. BUCK4VID Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK4_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK4 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK4_DECAY	R/W	OTP-Programmable	Decay Bit **0**: The output slews down to a lower voltage set by the VID bits. **1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

5.9.25 BUCK4SLPVID: BUCK4 Sleep VID Register (offset = 95h) [reset = OTP-Programmable]

Figure 5-42. BUCK4SLPVID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK4_SLP_VID[6]	BUCK4_SLP_VID[5]	BUCK4_SLP_VID[4]	BUCK4_SLP_VID[3]	BUCK4_SLP_VID[2]	BUCK4_SLP_VID[1]	BUCK4_SLP_VID[0]	RESERVED
TPS650860	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-30. BUCK4SLPVID Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK4_SLP_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK4 regulator output regulation voltage in sleep mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.

5.9.26 BUCK5VID: BUCK5 VID Register (offset = 96h) [reset = OTP-Programmable]

Figure 5-43. BUCK5VID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK5_VID[6]	BUCK5_VID[5]	BUCK5_VID[4]	BUCK5_VID[3]	BUCK5_VID[2]	BUCK5_VID[1]	BUCK5_VID[0]	BUCK5_DECAY
TPS650860	0	1	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-31. BUCK5VID Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK5_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK5 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK5_DECAY	R/W	OTP-Programmable	Decay Bit **0**: The output slews down to a lower voltage set by the VID bits. **1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

5.9.27 BUCK5SLPVID: BUCK5 Sleep VID Register (offset = 97h) [reset = OTP-Programmable]

Figure 5-44. BUCK5SLPVID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK5_SLP_VID[6]	BUCK5_SLP_VID[5]	BUCK5_SLP_VID[4]	BUCK5_SLP_VID[3]	BUCK5_SLP_VID[2]	BUCK5_SLP_VID[1]	BUCK5_SLP_VID[0]	RESERVED
TPS650860	0	1	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-32. BUCK5SLPVID Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK5_SLP_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK5 regulator output regulation voltage in sleep mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.

5.9.28 BUCK6VID: BUCK6 VID Register (offset = 98h) [reset = OTP-Programmable]

Figure 5-45. BUCK6VID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK6_VID[6]	BUCK6_VID[5]	BUCK6_VID[4]	BUCK6_VID[3]	BUCK6_VID[2]	BUCK6_VID[1]	BUCK6_VID[0]	BUCK6_DECAY
TPS650860	1	1	0	1	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-33. BUCK6VID Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK6_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK6 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.
0	BUCK6_DECAY	R/W	OTP-Programmable	Decay Bit **0**: The output slews down to a lower voltage set by the VID bits. **1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output.

5.9.29 BUCK6SLPVID: BUCK6 Sleep VID Register (offset = 99h) [reset = OTP-Programmable]

Figure 5-46. BUCK6SLPVID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK6_SLP_VID[6]	BUCK6_SLP_VID[5]	BUCK6_SLP_VID[4]	BUCK6_SLP_VID[3]	BUCK6_SLP_VID[2]	BUCK6_SLP_VID[1]	BUCK6_SLP_VID[0]	RESERVED
TPS650860	1	1	0	1	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-34. BUCK6SLPVID Register Descriptions

Bit	Field	Type	Reset	Description
7:1	BUCK6_SLP_VID[6:0]	R/W	OTP-Programmable	This field sets the BUCK6 regulator output regulation voltage in normal mode. See Table 5-2 and Table 5-3 for 10-mV and 25-mV step ranges for V_{OUT} options.

5.9.30 LDOA2VID: LDOA2 VID Register (offset = 9Ah) [reset = OTP-Programmable]

Figure 5-47. LDOA2VID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_SLP_VID[3]	LDOA2_SLP_VID[2]	LDOA2_SLP_VID[1]	LDOA2_SLP_VID[0]	LDOA2_VID[3]	LDOA2_VID[3]	LDOA2_VID[1]	LDOA2_VID[0]
TPS650860	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-35. LDOA2VID Register Descriptions

Bit	Field	Type	Reset	Description
7-4	LDOA2_SLP_VID[3:0]	R/W	OTP-Programmable	This field sets the LDOA2 regulator output regulation voltage in sleep mode. See Table 5-5 for V_{out} options.
3-0	LDOA2_VID[3:0]	R/W	OTP-Programmable	This field sets the LDOA2 regulator output regulation voltage in normal mode. See Table 5-5 for V_{out} options.

5.9.31 LDOA3VID: LDOA3 VID Register (offset = 9Bh) [reset = OTP-Programmable]

Figure 5-48. LDOA3VID Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA3_SLP_VID[3]	LDOA3_SLP_VID[2]	LDOA3_SLP_VID[1]	LDOA3_SLP_VID[0]	LDOA3_VID[3]	LDOA3_VID[3]	LDOA3_VID[1]	LDOA3_VID[0]
TPS650860	1	0	1	0	1	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-36. LDOA3VID Register Descriptions

Bit	Field	Type	Reset	Description
7-4	LDOA3_SLP_VID[3:0]	R/W	OTP-Programmable	This field sets the LDOA3 regulator output regulation voltage in sleep mode. See Table 5-5 for V_{out} options.
3-0	LDOA3_VID[3:0]	R/W	OTP-Programmable	This field sets the LDOA3 regulator output regulation voltage in normal mode. See Table 5-5 for V_{out} options.

5.9.32 BUCK123CTRL: BUCK1-3 Control Register (offset = 9Ch) [reset = OTP-Programmable]

Figure 5-49. BUCK123CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	BUCK3_MODE	BUCK2_MODE	BUCK1_MODE	BUCK3_DIS	BUCK2_DIS	BUCK1_DIS
TPS650860	0	0	0	0	0	1	1	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-37. BUCK123CTRL Register Descriptions

Bit	Field	Type	Reset	Description
5	BUCK3_MODE	R/W	OTP-Programmable	This field sets the BUCK3 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
4	BUCK2_MODE	R/W	OTP-Programmable	This field sets the BUCK2 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
3	BUCK1_MODE	R/W	OTP-Programmable	This field sets the BUCK1 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
2	BUCK3_DIS	R/W	OTP-Programmable	BUCK3 Disable Bit. Writing 0 to this bit forces BUCK3 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable **1**: Enable
1	BUCK2_DIS	R/W	OTP-Programmable	BUCK2 Disable Bit. Writing 0 to this bit forces BUCK2 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable **1**: Enable
0	BUCK1_DIS	R/W	OTP-Programmable	BUCK1 Disable Bit. Writing 0 to this bit forces BUCK1 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable **1**: Enable

5.9.33 PG_DELAY2: Power Good Delay2 Register (offset = 9Dh) [reset = OTP-Programmable]

Programmable Power Good delay for GPO3 pin, measured from the moment when all VRs assigned to GPO3 pin reach their regulation range to Power Good assertion. This is an optional register as the PMIC can be programmed for system PG, level shifter or I^2C controller GPO.

Figure 5-50. PG_DELAY2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	GPO2_PG_DELAY[2]	GPO2_PG_DELAY[1]	GPO2_PG_DELAY[0]	GPO4_PG_DELAY[2]	GPO4_PG_DELAY[1]	GPO4_PG_DELAY[0]	GPO1_PG_DELAY[1]	GPO1_PG_DELAY[0]
TPS650860	0	0	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-38. PG_DELAY2 Register Descriptions

Bit	Field	Type	Reset	Description
7-5	GPO2_PG_DELAY[2:0]	R/W	OTP-Programmable	Programmable delay power good or level shifter for GPO2 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10 % variation **000** = 2.5 ms **001** = 5.0 ms **010** = 10 ms **011** = 15 ms **100** = 20 ms **101** = 50 ms **110** = 75 ms **111** = 100 ms
4-2	GPO4_PG_DELAY[2:0]	R/W	OTP-Programmable	Programmable delay power good or level shifter for GPO4 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10 % variation **000** = 2.5 ms **001** = 5.0 ms **010** = 10 ms **011** = 15 ms **100** = 20 ms **101** = 50 ms **110** = 75 ms **111** = 100 ms
1-0	GPO1_PG_DELAY[1:0]	R/W	OTP-Programmable	Programmable delay power good or level shifter for GPO1 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10 % variation **00** = 0 ms **01** = 5.0 ms **10** = 10 ms **11** = 15 ms

5.9.34 SWVTT_DIS: SWVTT Disable Register (offset = 9Fh) [reset = OTP-Programmable]

Figure 5-51. SWVTT_DIS Register

Bit	7	6	5	4	3	2	1	0
Bit Name	SWB2_DIS	SWB1_DIS	SWA1_DIS	VTT_DIS	Reserved	Reserved	Reserved	Reserved
TPS650860	1	1	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-39. SWVTT_DIS Register Descriptions

Bit	Field	Type	Reset	Description
7	SWB2_DIS	R/W	OTP-Programmable	SWB2 Disable Bit. Writing 0 to this bit forces SWB2 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable. **1**: Enable.
6	SWB1_DIS	R/W	OTP-Programmable	SWB1 Disable Bit. Writing 0 to this bit forces SWB1 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable. **1**: Enable.
5	SWA1_DIS	R/W	OTP-Programmable	SWA1 Disable Bit. Writing 0 to this bit forces SWA1 to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable. **1**: Enable.
4	VTT_DIS	R/W	OTP-Programmable	VTT Disable Bit. Writing 0 to this bit forces VTT to turn off regardless of any control input pin (CTL1–CTL6) status. **0**: Disable. **1**: Enable.
3	Reserved	R/W	0	Reserved, Keep bit **0** at all times. Do not write to 1.
2	Reserved	R/W	0	Reserved, Keep bit **0** at all times. Do not write to 1.
1	Reserved	R/W	0	Reserved, Keep bit **0** at all times. Do not write to 1.
0	Reserved	R/W	0	Reserved, Keep bit **0** at all times. Do not write to 1.

5.9.35 I2C_RAIL_EN1: VR Pin Enable Override1 Register (offset = A0h) [reset = OTP-Programmable]

Figure 5-52. I2C_RAIL_EN1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_EN	SWA1_EN	BUCK6_EN	BUCK5_EN	BUCK4_EN	BUCK3_EN	BUCK2_EN	BUCK1_EN
TPS650860	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-40. I2C_RAIL_EN1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_EN	R/W	OTP-Programmable	LDOA2 I^2C Enable **0**: LDOA2 is enabled or disabled by one of the control input pins or internal PG signal. **1**: LDOA2 is forced on unless LDOA2_DIS = 0.
6	SWA1_EN	R/W	OTP-Programmable	SWA1 I^2C Enable **0**: SWA1 is enabled or disabled by one of the control input pins or internal PG signal. **1**: SWA1 is forced on unless SWA1_DIS = 0.
5	BUCK6_EN	R/W	OTP-Programmable	BUCK6 I^2C Enable **0**: BUCK6 is enabled or disabled by one of the control input pins or internal PG signal. **1**: BUCK6 is forced on unless BUCK6_DIS = 0.
4	BUCK5_EN	R/W	OTP-Programmable	BUCK5 I^2C Enable **0**: BUCK5 is enabled or disabled by one of the control input pins or internal PG signal. **1**: BUCK5 is forced on unless BUCK5_DIS = 0.
3	BUCK4_EN	R/W	OTP-Programmable	BUCK4 I^2C Enable **0**: BUCK4 is enabled or disabled by one of the control input pins or internal PG signal. **1**: BUCK4 is forced on unless BUCK4_DIS = 0.

Table 5-40. I2C_RAIL_EN1 Register Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BUCK3_EN	R/W	OTP-Programmable	BUCK3 I^2C Enable **0**: BUCK3 is enabled or disabled by one of the control input pins or internal PG signal. **1**: BUCK3 is forced on unless BUCK3_DIS = 0.
1	BUCK2_EN	R/W	OTP-Programmable	BUCK2 I^2C Enable **0**: BUCK2 is enabled or disabled by one of the control input pins or internal PG signal. **1**: BUCK2 is forced on unless BUCK2_DIS = 0.
0	BUCK1_EN	R/W	OTP-Programmable	BUCK1 I^2C Enable **0**: BUCK1 is enabled or disabled by one of the control input pins or internal PG signal. **1**: BUCK1 is forced on unless BUCK1_DIS = 0.

5.9.36 I2C_RAIL_EN2/GPOCTRL: VR Pin Enable Override2/GPO Control Register (offset = A1h) [reset = OTP-Programmable]

Figure 5-53. I2C_RAIL_EN2/GPOCTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	GPO4_LVL	GPO3_LVL	GPO2_LVL	GPO1_LVL	VTT_EN	SWB2_EN	SWB1_EN	LDOA3_EN
TPS650860	X	X	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-41. I2C_RAIL_EN2/GPOCTRL Register Descriptions

Bit	Field	Type	Reset	Description
7	GPO4_LVL	R/W	OTP-Programmable	The field is to set GPO4 pin output if the pin is factory-configured as an open-drain general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high. **X**: Bit not used or is do not care for this version.
6	GPO3_LVL	R/W	OTP-Programmable	The field is to set GPO3 pin output if the pin is factory-configured as either an open-drain or a push-pull general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high. **X**: Bit not used or is do not care for this version.
5	GPO2_LVL	R/W	OTP-Programmable	The field is to set GPO2 pin output if the pin is factory-configured as either an open-drain or a push-pull general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high.
4	GPO1_LVL	R/W	OTP-Programmable	The field is to set GPO1 pin output if the pin is factory-configured as either an open-drain or a push-pull general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high.
3	VTT_EN	R/W	OTP-Programmable	VTT LDO I^2C Enable **0**: VTT LDO is enabled or disabled by one of the control input pins or internal PG signals. **1**: VTT LDO is forced on unless VTT_DIS = 0.
2	SWB2_EN	R/W	OTP-Programmable	SWB2 I^2C Enable **0**: SWB2 is enabled or disabled by one of the control input pins or internal PG signals. **1**: SWB2 is forced on unless SWB2_DIS = 0.
1	SWB1_EN	R/W	OTP-Programmable	SWB1 I^2C Enable **0**: SWB1 is enabled or disabled by one of the control input pins or internal PG signals. **1**: SWB1 is forced on unless SWB1_DIS = 0.

Table 5-41. I2C_RAIL_EN2/GPOCTRL Register Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LDOA3_EN	R/W	OTP-Programmable	LDOA3 I^2C Enable **0**: LDOA3 is enabled or disabled by one of the control input pins or internal PG signals. **1**: LDOA3 is forced on unless LDOA3_DIS = 0.

5.9.37 PWR_FAULT_MASK1: VR Power Fault Mask1 Register (offset = A2h) [reset = OTP-Programmable]

Figure 5-54. PWR_FAULT_MASK1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_ FLTMSK	SWA1_ FLTMSK	BUCK6_ FLTMSK	BUCK5_ FLTMSK	BUCK4_ FLTMSK	BUCK3_ FLTMSK	BUCK2_ FLTMSK	BUCK1_ FLTMSK
TPS650860	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-42. PWR_FAULT_MASK1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_FLTMSK	R/W	OTP-Programmable	LDOA2 Power Fault Mask. When masked, power fault from LDOA2 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
6	SWA1_FLTMSK	R/W	OTP-Programmable	SWA1 Power Fault Mask. When masked, power fault from SWA1 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
5	BUCK6_FLTMSK	R/W	OTP-Programmable	BUCK6 Power Fault Mask. When masked, power fault from BUCK6 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
4	BUCK5_FLTMSK	R/W	OTP-Programmable	BUCK5 Power Fault Mask. When masked, power fault from BUCK5 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
3	BUCK4_FLTMSK	R/W	OTP-Programmable	BUCK4 Power Fault Mask. When masked, power fault from BUCK4 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
2	BUCK3_FLTMSK	R/W	OTP-Programmable	BUCK3 Power Fault Mask. When masked, power fault from BUCK3 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
1	BUCK2_FLTMSK	R/W	OTP-Programmable	BUCK2 Power Fault Mask. When masked, power fault from BUCK2 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
0	BUCK1_FLTMSK	R/W	OTP-Programmable	BUCK1 Power Fault Mask. When masked, power fault from BUCK1 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked

5.9.38 PWR_FAULT_MASK2: VR Power Fault Mask2 Register (offset = A3h) [reset = OTP-Programmable]

Figure 5-55. PWR_FAULT_MASK2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	LDOA1_FLTMSK	VTT_FLTMSK	SWB2_FLTMSK	SWB1_FLTMSK	LDOA3_FLTMSK
TPS650860	0	0	1	0	0	1	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-43. PWR_FAULT_MASK2 Register Descriptions

Bit	Field	Type	Reset	Description
4	LDOA1_FLTMSK	R/W	OTP-Programmable	LDOA1 Power Fault Mask. When masked, power fault from LDOA1 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
3	VTT_FLTMSK	R/W	OTP-Programmable	VTT LDO Power Fault Mask. When masked, power fault from VTT LDO does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
2	SWB2_FLTMSK	R/W	OTP-Programmable	SWB2 Power Fault Mask. When masked, power fault from SWB2 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
1	SWB1_FLTMSK	R/W	OTP-Programmable	SWB1 Power Fault Mask. When masked, power fault from SWB1 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked
0	LDOA3_FLTMSK	R/W	OTP-Programmable	LDOA3 Power Fault Mask. When masked, power fault from LDOA3 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked

5.9.39 GPO1PG_CTRL1: GPO1 PG Control1 Register (offset = A4h) [reset = OTP-Programmable]

Figure 5-56. GPO1PG_CTRL1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_MSK	RESERVED	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
TPS650860	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-44. GPO1PG_CTRL1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	OTP-Programmable	**0**: LDOA2 PG is part of Power Good tree of GPO1 pin. **1**: LDOA2 PG is NOT part of Power Good tree of GPO1 pin and is ignored.
5	BUCK6_MSK	R/W	OTP-Programmable	**0**: BUCK6 PG is part of Power Good tree of GPO1 pin. **1**: BUCK6 PG is NOT part of Power Good tree of GPO1 pin and is ignored.
4	BUCK5_MSK	R/W	OTP-Programmable	**0**: BUCK5 PG is part of Power Good tree of GPO1 pin. **1**: BUCK5 PG is NOT part of Power Good tree of GPO1 pin and is ignored.

Table 5-44. GPO1PG_CTRL1 Register Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BUCK4_MSK	R/W	OTP-Programmable	**0**: BUCK4 PG is part of Power Good tree of GPO1 pin. **1**: BUCK4 PG is NOT part of Power Good tree of GPO1 pin and is ignored.
2	BUCK3_MSK	R/W	OTP-Programmable	**0**: BUCK3 PG is part of Power Good tree of GPO1 pin. **1**: BUCK3 PG is NOT part of Power Good tree of GPO1 pin and is ignored.
1	BUCK2_MSK	R/W	OTP-Programmable	**0**: BUCK2 PG is part of Power Good tree of GPO1 pin. **1**: BUCK2 PG is NOT part of Power Good tree of GPO1 pin and is ignored.
0	BUCK1_MSK	R/W	OTP-Programmable	**0**: BUCK1 PG is part of Power Good tree of GPO1 pin. **1**: BUCK1 PG is NOT part of Power Good tree of GPO1 pin and is ignored.

5.9.40 GPO1PG_CTRL2: GPO1 PG Control2 Register (offset = A5h) [reset = OTP-Programmable]

Figure 5-57. GPO1PG_CTRL2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	RESERVED	RESERVED	LDOA3_MSK
TPS650860	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-45. GPO1PG_CTRL2 Register Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	OTP-Programmable	**0**: CTL5 pin status is part of Power Good tree of GPO1 pin. **1**: CTL5 pin status is NOT part of Power Good tree of GPO1 pin and is ignored.
6	CTL4_MSK	R/W	OTP-Programmable	**0**: CTL4 pin status is part of Power Good tree of GPO1 pin. **1**: CTL4 pin status is NOT part of Power Good tree of GPO1 pin and is ignored.
5	CTL2_MSK	R/W	OTP-Programmable	**0**: CTL2 pin status is part of Power Good tree of GPO1 pin. **1**: CTL2 pin status is NOT part of Power Good tree of GPO1 pin and is ignored.
4	CTL1_MSK	R/W	OTP-Programmable	**0**: CTL1 pin status is part of Power Good tree of GPO1 pin. **1**: CTL1 pin status is NOT part of Power Good tree of GPO1 pin and is ignored.
3	VTT_MSK	R/W	OTP-Programmable	**0**: VTT LDO PG is part of Power Good tree of GPO1 pin. **1**: VTT LDO PG is NOT part of Power Good tree of GPO1 pin and is ignored.
0	LDOA3_MSK	R/W	OTP-Programmable	**0**: LDOA3 PG is part of Power Good tree of GPO1 pin. **1**: LDOA3 PG is NOT part of Power Good tree of GPO1 pin and is ignored.

5.9.41 GPO4PG_CTRL1: GPO4 PG Control1 Register (offset = A6h) [reset = OTP-Programmable]

Figure 5-58. GPO4PG_CTRL1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_MSK	RESERVED	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
TPS650860	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-46. GPO4PG_CTRL1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	OTP-Programmable	**0**: LDOA2 PG is part of Power Good tree of GPO4 pin. **1**: LDOA2 PG is NOT part of Power Good tree of GPO4 pin and is ignored.
5	BUCK6_MSK	R/W	OTP-Programmable	**0**: BUCK6 PG is part of Power Good tree of GPO4 pin. **1**: BUCK6 PG is NOT part of Power Good tree of GPO4 pin and is ignored.
4	BUCK5_MSK	R/W	OTP-Programmable	**0**: BUCK5 PG is part of Power Good tree of GPO4 pin. **1**: BUCK5 PG is NOT part of Power Good tree of GPO4 pin and is ignored.
3	BUCK4_MSK	R/W	OTP-Programmable	**0**: BUCK4 PG is part of Power Good tree of GPO4 pin. **1**: BUCK4 PG is NOT part of Power Good tree of GPO4 pin and is ignored.
2	BUCK3_MSK	R/W	OTP-Programmable	**0**: BUCK3 PG is part of Power Good tree of GPO4 pin. **1**: BUCK3 PG is NOT part of Power Good tree of GPO4 pin and is ignored.
1	BUCK2_MSK	R/W	OTP-Programmable	**0**: BUCK2 PG is part of Power Good tree of GPO4 pin. **1**: BUCK2 PG is NOT part of Power Good tree of GPO4 pin and is ignored.
0	BUCK1_MSK	R/W	OTP-Programmable	**0**: BUCK1 PG is part of Power Good tree of GPO4 pin. **1**: BUCK1 PG is NOT part of Power Good tree of GPO4 pin and is ignored.

5.9.42 GPO4PG_CTRL2: GPO4 PG Control2 Register (offset = A7h) [reset = OTP-Programmable]

Figure 5-59. GPO4PG_CTRL2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	RESERVED	RESERVED	LDOA3_MSK
TPS650860	1	1	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-47. GPO4PG_CTRL2 Register Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	OTP-Programmable	**0**: CTL5 pin status is part of Power Good tree of GPO4 pin. **1**: CTL5 pin status is NOT part of Power Good tree of GPO4 pin and is ignored.
6	CTL4_MSK	R/W	OTP-Programmable	**0**: CTL4 pin status is part of Power Good tree of GPO4 pin. **1**: CTL4 pin status is NOT part of Power Good tree of GPO4 pin and is ignored.
5	CTL2_MSK	R/W	OTP-Programmable	**0**: CTL2 pin status is part of Power Good tree of GPO4 pin. **1**: CTL2 pin status is NOT part of Power Good tree of GPO4 pin and is ignored.
4	CTL1_MSK	R/W	OTP-Programmable	**0**: CTL1 pin status is part of Power Good tree of GPO4 pin. **1**: CTL1 pin status is NOT part of Power Good tree of GPO4 pin and is ignored.
3	VTT_MSK	R/W	OTP-Programmable	**0**: VTT LDO PG is part of Power Good tree of GPO4 pin. **1**: VTT LDO PG is NOT part of Power Good tree of GPO4 pin and is ignored.
0	LDOA3_MSK	R/W	OTP-Programmable	**0**: LDOA3 PG is part of Power Good tree of GPO4 pin. **1**: LDOA3 PG is NOT part of Power Good tree of GPO4 pin and is ignored.

5.9.43 GPO2PG_CTRL1: GPO2 PG Control1 Register (offset = A8h) [reset = OTP-Programmable]

Figure 5-60. GPO2PG_CTRL1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_MSK	RESERVED	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
TPS650860	1	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-48. GPO2PG_CTRL1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	OTP-Programmable	**0**: LDOA2 PG is part of Power Good tree of GPO2 pin. **1**: LDOA2 PG is NOT part of Power Good tree of GPO1 pin and is ignored.
5	BUCK6_MSK	R/W	OTP-Programmable	**0**: BUCK6 PG is part of Power Good tree of GPO2 pin. **1**: BUCK6 PG is NOT part of Power Good tree of GPO2 pin and is ignored.
4	BUCK5_MSK	R/W	OTP-Programmable	**0**: BUCK5 PG is part of Power Good tree of GPO2 pin. **1**: BUCK5 PG is NOT part of Power Good tree of GPO2 pin and is ignored.
3	BUCK4_MSK	R/W	OTP-Programmable	**0**: BUCK4 PG is part of Power Good tree of GPO2 pin. **1**: BUCK4 PG is NOT part of Power Good tree of GPO2 pin and is ignored.
2	BUCK3_MSK	R/W	OTP-Programmable	**0**: BUCK3 PG is part of Power Good tree of GPO2 pin. **1**: BUCK3 PG is NOT part of Power Good tree of GPO2 pin and is ignored.
1	BUCK2_MSK	R/W	OTP-Programmable	**0**: BUCK2 PG is part of Power Good tree of GPO2 pin. **1**: BUCK2 PG is NOT part of Power Good tree of GPO2 pin and is ignored.
0	BUCK1_MSK	R/W	OTP-Programmable	**0**: BUCK1 PG is part of Power Good tree of GPO2 pin. **1**: BUCK1 PG is NOT part of Power Good tree of GPO2 pin and is ignored.

5.9.44 GPO2PG_CTRL2: GPO2 PG Control2 Register (offset = A9h) [reset = OTP-Programmable]

Figure 5-61. GPO2PG_CTRL2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	RESERVED	RESERVED	LDOA3_MSK
TPS650860	1	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-49. GPO2PG_CTRL2 Register Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	OTP-Programmable	**0**: CTL5 pin status is part of Power Good tree of GPO2 pin. **1**: CTL5 pin status is NOT part of Power Good tree of GPO2 pin and is ignored.
6	CTL4_MSK	R/W	OTP-Programmable	**0**: CTL4 pin status is part of Power Good tree of GPO2 pin. **1**: CTL4 pin status is NOT part of Power Good tree of GPO2 pin and is ignored.
5	CTL2_MSK	R/W	OTP-Programmable	**0**: CTL2 pin status is part of Power Good tree of GPO2 pin. **1**: CTL2 pin status is NOT part of Power Good tree of GPO2 pin and is ignored.

Table 5-49. GPO2PG_CTRL2 Register Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CTL1_MSK	R/W	OTP-Programmable	**0**: CTL1 pin status is part of Power Good tree of GPO2 pin. **1**: CTL1 pin status is NOT part of Power Good tree of GPO2 pin and is ignored.
3	VTT_MSK	R/W	OTP-Programmable	**0**: VTT LDO PG is part of Power Good tree of GPO2 pin. **1**: VTT LDO PG is NOT part of Power Good tree of GPO2 pin and is ignored.
0	LDOA3_MSK	R/W	OTP-Programmable	**0**: LDOA3 PG is part of Power Good tree of GPO2 pin. **1**: LDOA3 PG is NOT part of Power Good tree of GPO2 pin and is ignored.

5.9.45 GPO3PG_CTRL1: GPO3 PG Control1 Register (offset = AAh) [reset = OTP-Programmable]

Figure 5-62. GPO3PG_CTRL1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_MSK	RESERVED	BUCK6_MSK	BUCK5_MSK	BUCK4_MSK	BUCK3_MSK	BUCK2_MSK	BUCK1_MSK
TPS650860	0	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-50. GPO3PG_CTRL1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_MSK	R/W	OTP-Programmable	**0**: LDOA2 PG is part of Power Good tree of GPO3 pin. **1**: LDOA2 PG is NOT part of Power Good tree of GPO3 pin and is ignored.
5	BUCK6_MSK	R/W	OTP-Programmable	**0**: BUCK6 PG is part of Power Good tree of GPO3 pin. **1**: BUCK6 PG is NOT part of Power Good tree of GPO3 pin and is ignored.
4	BUCK5_MSK	R/W	OTP-Programmable	**0**: BUCK5 PG is part of Power Good tree of GPO3 pin. **1**: BUCK5 PG is NOT part of Power Good tree of GPO3 pin and is ignored.
3	BUCK4_MSK	R/W	OTP-Programmable	**0**: BUCK4 PG is part of Power Good tree of GPO3 pin. **1**: BUCK4 PG is NOT part of Power Good tree of GPO3 pin and is ignored.
2	BUCK3_MSK	R/W	OTP-Programmable	**0**: BUCK3 PG is part of Power Good tree of GPO3 pin. **1**: BUCK3 PG is NOT part of Power Good tree of GPO3 pin and is ignored.
1	BUCK2_MSK	R/W	OTP-Programmable	**0**: BUCK2 PG is part of Power Good tree of GPO3 pin. **1**: BUCK2 PG is NOT part of Power Good tree of GPO3 pin and is ignored.
0	BUCK1_MSK	R/W	OTP-Programmable	**0**: BUCK1 PG is part of Power Good tree of GPO3 pin. **1**: BUCK1 PG is NOT part of Power Good tree of GPO3 pin and is ignored.

5.9.46 GPO3PG_CTRL2: GPO3 PG Control2 Register (offset = ABh) [reset = OTP-Programmable]

Figure 5-63. GPO3PG_CTRL2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	CTL5_MSK	CTL4_MSK	CTL2_MSK	CTL1_MSK	VTT_MSK	RESERVED	RESERVED	LDOA3_MSK
TPS650860	1	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-51. GPO3PG_CTRL2 Register Descriptions

Bit	Field	Type	Reset	Description
7	CTL5_MSK	R/W	OTP-Programmable	**0**: CTL5 pin status is part of Power Good tree of GPO3 pin. **1**: CTL5 pin status is NOT part of Power Good tree of GPO3 pin and is ignored.
6	CTL4_MSK	R/W	OTP-Programmable	**0**: CTL4 pin status is part of Power Good tree of GPO3 pin. **1**: CTL4 pin status is NOT part of Power Good tree of GPO3 pin and is ignored.
5	CTL2_MSK	R/W	OTP-Programmable	**0**: CTL2 pin status is part of Power Good tree of GPO3 pin. **1**: CTL2 pin status is NOT part of Power Good tree of GPO3 pin and is ignored.
4	CTL1_MSK	R/W	OTP-Programmable	**0**: CTL1 pin status is part of Power Good tree of GPO3 pin. **1**: CTL1 pin status is NOT part of Power Good tree of GPO3 pin and is ignored.
3	VTT_MSK	R/W	OTP-Programmable	**0**: VTT LDO PG is part of Power Good tree of GPO3 pin. **1**: VTT LDO PG is NOT part of Power Good tree of GPO3 pin and is ignored.
0	LDOA3_MSK	R/W	OTP-Programmable	**0**: LDOA3 PG is part of Power Good tree of GPO3 pin. **1**: LDOA3 PG is NOT part of Power Good tree of GPO3 pin and is ignored.

5.9.47 MISCSYSPG Register (offset = ACh) [reset = OTP-Programmable]

Figure 5-64. MISCSYSPG Register

Bit	7	6	5	4	3	2	1	0
Bit Name	GPO1_ CTL3_MSK	GPO1_ CTL6_MSK	GPO4_ CTL3_MSK	GPO4_ CTL6_MSK	GPO2_ CTL3_MSK	GPO2_ CTL6_MSK	GPO3_ CTL3_MSK	GPO3_ CTL6_MSK
TPS650860	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-52. MISCSYSPG Register Descriptions

Bit	Field	Type	Reset	Description
7	GPO1_CTL3_MSK	R/W	OTP-Programmable	**0**: CTL3 pin status is part of Power Good tree of GPO1 pin. **1**: CTL3 pin status is NOT part of Power Good tree of GPO1 pin.
6	GPO1_CTL6_MSK	R/W	OTP-Programmable	**0**: CTL6 pin status is part of Power Good tree of GPO1 pin. **1**: CTL6 pin status is NOT part of Power Good tree of GPO1 pin.
5	GPO4_CTL3_MSK	R/W	OTP-Programmable	**0**: CTL3 pin status is part of Power Good tree of GPO4 pin. **1**: CTL3 pin status is NOT part of Power Good tree of GPO4 pin.
4	GPO4_CTL6_MSK	R/W	OTP-Programmable	**0**: CTL6 pin status is part of Power Good tree of GPO4 pin. **1**: CTL6 pin status is NOT part of Power Good tree of GPO4 pin.
3	GPO2_CTL3_MSK	R/W	OTP-Programmable	**0**: CTL3 pin status is part of Power Good tree of GPO2 pin. **1**: CTL3 pin status is NOT part of Power Good tree of GPO2 pin.
2	GPO2_CTL6_MSK	R/W	OTP-Programmable	**0**: CTL6 pin status is part of Power Good tree of GPO2 pin. **1**: CTL6 pin status is NOT part of Power Good tree of GPO2 pin.
1	GPO3_CTL3_MSK	R/W	OTP-Programmable	**0**: CTL3 pin status is part of Power Good tree of GPO3 pin. **1**: CTL3 pin status is NOT part of Power Good tree of GPO13pin.
0	GPO3_CTL6_MSK	R/W	OTP-Programmable	**0**: CTL6 pin status is part of Power Good tree of GPO3 pin. **1**: CTL6 pin status is NOT part of Power Good tree of GPO3 pin.

5.9.48 LDOA1CTRL: LDOA1 Control Register (offset = AEh) [reset = OTP-Programmable]

Figure 5-65. LDOA1CTRL Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA1_ DISCHG[1]	LDOA1_ DISCHG[0]	LDOA1_SDWN _CONFIG	LDOA1_ VID[3]	LDOA1_ VID[2]	LDOA1_ VID[1]	LDOA1_ VID[0]	LDOA1_ EN
TPS650860	0	1	1	1	1	1	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-53. LDOA1CTRL Register Descriptions

Bit	Field	Type	Reset	Description
7-6	LDOA1_DISCHG[1:0]	R/W	OTP-Programmable	LDOA1 discharge resistance **00**: no discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5	LDOA1_SDWN_CONFIG	R/W	OTP-Programmable	Control for Disabling LDOA1 during Emergency Shutdown **0**: LDOA1 will turn off during Emergency Shutdown for factory-programmable duration of 1 ms, 5 ms, 10 ms, or 100 ms. **1**: LDOA1 is controlled by LDOA1_EN bit only.
4-1	LDOA1_VID[3:0]	R/W	OTP-Programmable	This field sets the LDOA1 regulator output regulation voltage. See Table 5-4 for V_{OUT} options.
0	LDOA1_EN	R/W	OTP-Programmable	LDOA1 Enable Bit. **0**: Disable. **1**: Enable.

5.9.49 PG_STATUS1: Power Good Status1 Register (offset = B0h) [reset = 0000 0000]

Figure 5-66. PG_STATUS1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_ PGOOD	RESERVED	BUCK6_ PGOOD	BUCK5_ PGOOD	BUCK4_ PGOOD	BUCK3_ PGOOD	BUCK2_ PGOOD	BUCK1_ PGOOD
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-54. PG_STATUS1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_PGOOD	R	0	LDOA2 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
5	BUCK6_PGOOD	R	0	BUCK6 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
4	BUCK5_PGOOD	R	0	BUCK5 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
3	BUCK4_PGOOD	R	0	BUCK4 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
2	BUCK3_PGOOD	R	0	BUCK3 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
1	BUCK2_PGOOD	R	0	BUCK2 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.

Table 5-54. PG_STATUS1 Register Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BUCK1_PGOOD	R	0	BUCK1 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.

5.9.50 PG_STATUS2: Power Good Status2 Register (offset = B1h) [reset = 0000 0000]

Figure 5-67. PG_STATUS2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	LDO5 _PGOOD	LDOA1 _PGOOD	VTT _PGOOD	RESERVED	RESERVED	LDOA3 _PGOOD
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-55. PG_STATUS2 Register Descriptions

Bit	Field	Type	Reset	Description
5	LDO5_PGOOD	R	0	LDO5 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
4	LDOA1_PGOOD	R	0	LDOA1 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
3	VTT_PGOOD	R	0	VTT LDO Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
0	LDOA3_PGOOD	R	0	LDOA3 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.

5.9.51 PWR_FAULT_STATUS1: Power Fault Status1 Register (offset = B2h) [reset = 0000 0000]

Figure 5-68. PWR_FAULT_STATUS1 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_ PWRFLT	RESERVED	BUCK6_ PWRFLT	BUCK5_ PWRFLT	BUCK4_ PWRFLT	BUCK3_ PWRFLT	BUCK2_ PWRFLT	BUCK1_ PWRFLT
TPS650860	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-56. PWR_FAULT_STATUS1 Register Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_PWRFLT	R	0	This fields indicates that LDOA2 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
5	BUCK6_PWRFLT	R	0	This fields indicates that BUCK6 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
4	BUCK5_PWRFLT	R	0	This fields indicates that BUCK5 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
3	BUCK4_PWRFLT	R	0	This fields indicates that BUCK4 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.

Table 5-56. PWR_FAULT_STATUS1 Register Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BUCK3_PWRFLT	R	0	This fields indicates that BUCK3 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
1	BUCK2_PWRFLT	R	0	This fields indicates that BUCK2 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
0	BUCK1_PWRFLT	R	0	This fields indicates that BUCK1 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.

5.9.52 PWR_FAULT_STATUS2: Power Fault Status2 Register (offset = B3h) [reset = 0000 0000]

Figure 5-69. PWR_FAULT_STATUS2 Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	LDOA1_ PWRFLT	VTT_ PWRFLT	RESERVED	RESERVED	LDOA3_ PWRFLT
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-57. PWR_FAULT_STATUS2 Register Descriptions

Bit	Field	Type	Reset	Description
4	LDOA1_PWRFLT	R/W	0	This fields indicates that LDOA1 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
3	VTT_PWRFLT	R/W	0	This fields indicates that VTT LDO has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
0	LDOA3_PWRFLT	R/W	0	This fields indicates that LDOA3 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.

5.9.53 TEMPCRIT: Temperature Fault Status Register (offset = B4h) [reset = 0000 0000]

Asserted when an internal temperature sensor detects rise of die temperature above the CRITICAL temperature threshold (T_{CRIT}). There are 5 temperature sensors across the die.

Figure 5-70. TEMPCRIT Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	DIE_CRIT	VTT_CRIT	Top-Right _CRIT	Top-Left _CRIT	Bottom-Right _CRIT
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-58. TEMPCRIT Register Descriptions

Bit	Field	Type	Reset	Description
4	DIE_CRIT	R/W	0	Temperature of rest of die has exceeded T_{CRIT}. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
3	VTT_CRIT	R/W	0	Temperature of VTT LDO has exceeded T_{CRIT}. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
2	Top-Right_CRIT	R/W	0	Temperature of die Top-Right has exceeded T_{CRIT}. Top-Right corner of die from top view given pin1 is in Top-Left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
1	Top-Left_CRIT	R/W	0	Temperature of die Top-Left has exceeded T_{CRIT}.Top-Left corner of die from top view given pin1 is in Top-Left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
0	Bottom-Right_CRIT	R/W	0	Temperature of die Bottom-Right has exceeded T_{CRIT}. Bottom-Right corner of die from top view given pin1 is in Top-Left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.

5.9.54 TEMPHOT: Temperature Hot Status Register (offset = B5h) [reset = 0000 0000]

Asserted when an internal temperature sensor detects rise of die temperature above the HOT temperature threshold (T_{HOT}). There are 5 temperature sensors across the die.

Figure 5-71. TEMPHOT Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	DIE_HOT	VTT_HOT	Top-Right _HOT	Top-Left _HOT	Bottom-Right _HOT
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-59. TEMPHOT Register Descriptions

Bit	Field	Type	Reset	Description
4	DIE_HOT	R/W	0	Temperature of rest of die has exceeded T_{HOT}. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
3	VTT_HOT	R/W	0	Temperature of VTT LDO has exceeded T_{HOT}. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
2	Top-Right_HOT	R/W	0	Temperature of Top-Right has exceeded T_{HOT}. Top-Right corner of die from top view given pin1 is in Top-Left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
1	Top-Left_HOT	R/W	0	Temperature of Top-Left has exceeded THOT. Top-Left corner of die from top view given pin1 is in Top-Left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
0	Bottom-Right_HOT	R/W	0	Temperature of Bottom-Right has exceeded T_{HOT}. Bottom-Right corner of die from top view given pin1 is in Top-Left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.

5.9.55 OC_STATUS: Overcurrent Fault Status Register (offset = B6h) [reset = 0000 0000]

Asserted when overcurrent condition is detected from a LSD FET.

Figure 5-72. OC_STATUS Register

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK6_OC	BUCK2_OC	BUCK1_OC
TPS650860	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-60. OC_STATUS Register Descriptions

Bit	Field	Type	Reset	Description
2	BUCK6_OC	R/W	0	BUCK6 LSD FET overcurrent has been detected. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
1	BUCK2_OC	R/W	0	BUCK2 LSD FET overcurrent has been detected. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
0	BUCK1_OC	R/W	0	BUCK1 LSD FET overcurrent has been detected. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Typical Application

For a detailed description about application usage, refer to the *TPS65086x Design Guide* (SLVUAJ9) and to the *TPS65086x Schematic and Layout Checklist* (SLVA734). The TPS650860 can be used in several different applications from computing, industrial interfacing and much more. This section describes the general application information and provides a more detailed description on the TPS650860 device that powers a generic multicore-processor application. An example system block diagram for the device powering an SoC and the rest of platform is shown in Figure 6-1. The functional block diagram from Figure 5-1 outlines the typical external components necessary for proper device functionality.

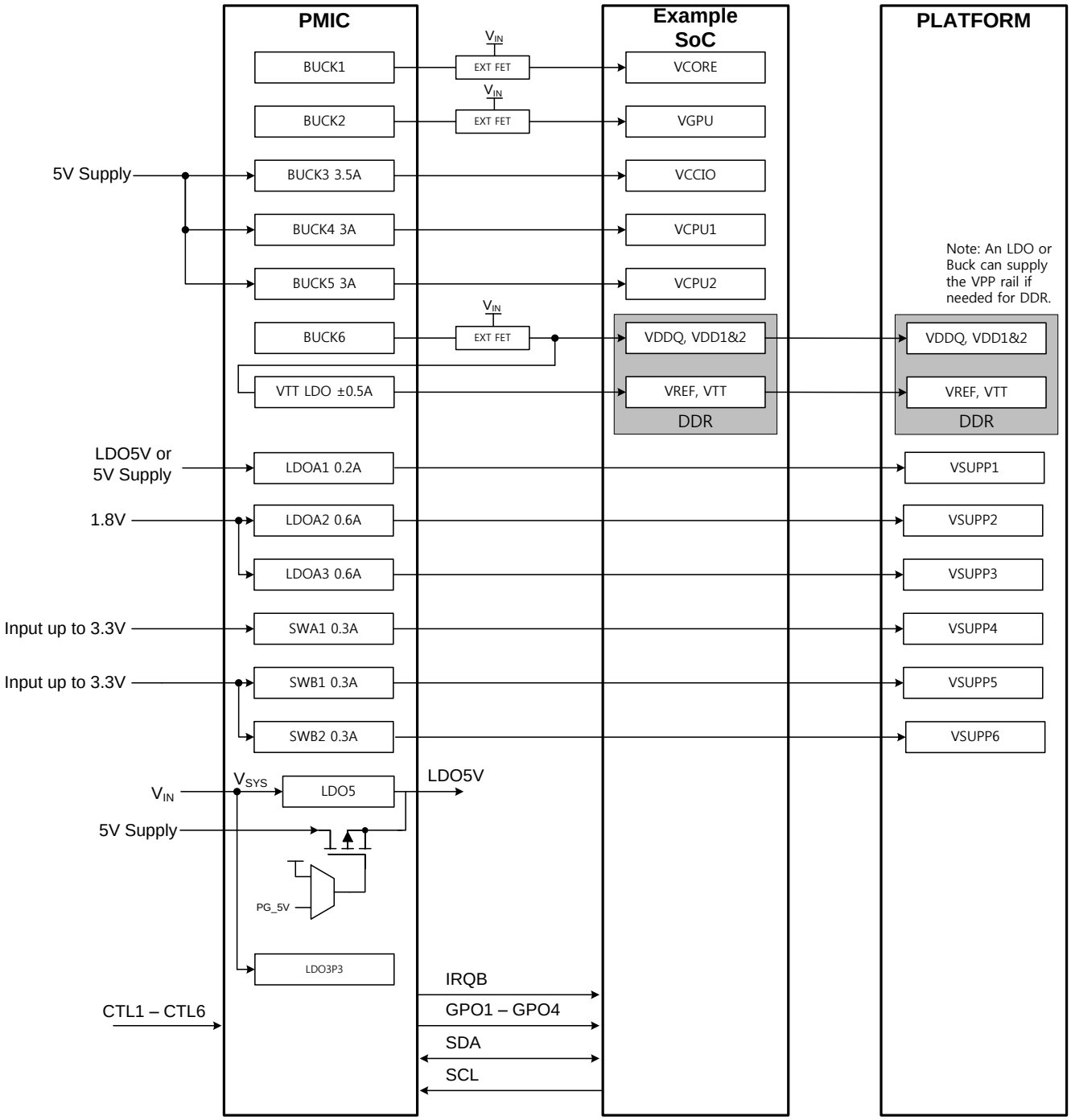


Figure 6-1. Typical Application Example

6.1.1.1 Design Requirements

The TPS650860 requires decoupling caps on the supply pins. Follow the values for recommended capacitance on these supplies given in the *Specifications* section. The controllers, converter, LDOs, and some other features can be adjusted to meet specific application needs. Section 6.1.1.2 describes how to design and adjust the external components to achieve desired performance.

6.1.1.2 Detailed Design Procedure

6.1.1.2.1 Controller Design Procedure

Designing the controller can be broken down into the following steps:

1. Design the output filter
2. Select the FETs
3. Select the bootstrap capacitor
4. Select the input capacitors
5. Set the current limits

Controllers BUCK1, BUCK2, and BUCK6 require a 5-V supply and capacitors at their corresponding DRV5V_x_x pins. For most applications, the DRV5V_x_x input must come from the LDO5P0 pin to ensure uninterrupted supply voltage; a 2.2-µF, X5R, 20%, 10-V, or similar capacitor must be used for decoupling.

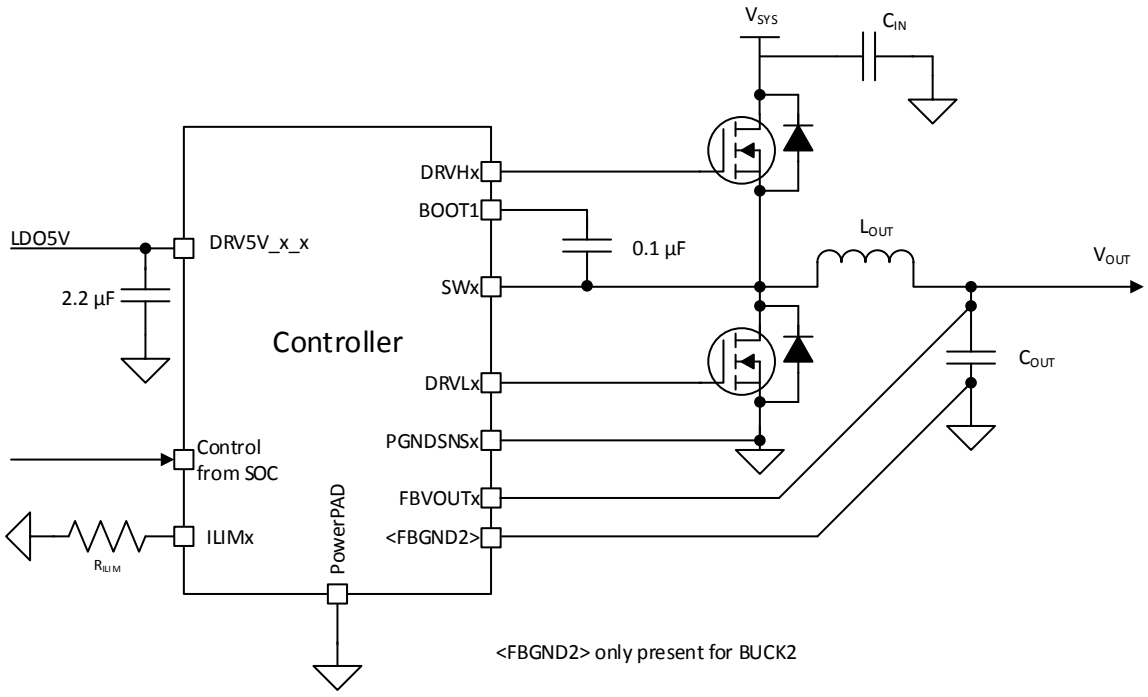


Figure 6-2. Controller Diagram

6.1.1.2.1.1 Selecting the Inductor

Placement of an inductor is required between the external FETs and the output capacitors. Together, the inductor and output capacitors make the double-pole that contributes to stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases, the ripple current decreases, which typically results in an increased efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

Equation 3 shows the calculation for the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}} \quad (3)$$

where

- V_{OUT} is the typical output voltage
- V_{IN} is the typical input voltage
- f_{SW} is the typical switching frequency
- $Iout_{MAX}$ is the maximum load current
- K_{IND} is the ratio of $I_{Lripple}$ to the $I_{out(max)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4.

With the chosen inductance value, the peak current for the inductor in steady state operation, $I_{L(max)}$, can be calculated using Equation 4. The rated saturation current of the inductor must be higher than the $I_{L(max)}$ current.

$$I_{LMAX} = Iout_{MAX} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \quad (4)$$

Following the previous equations, the preferred inductor selected for the controllers are listed Table 6-1.

Table 6-1. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIME031B	0.47 µH–1 µH	3.3 mm × 3.7 mm	1.2 mm
Cyntec	PIMB041B	0.33 µH–2.2 µH	4.45 mm × 4.75 mm	1.2 mm
Cyntec	PIMB051B	1 µH–3.3 µH	5.4 mm × 5.75 mm	1.2 mm
Cyntec	PIME051E	0.33 µH–4.7 µH	5.4 mm × 5.75 mm	1.5 mm
Cyntec	PIMB051H	0.47 µH–4.7 µH	5.4 mm × 5.75 mm	1.8 mm
Cyntec	PIME061B	0.56 µH–3.3 µH	6.8 mm × 7.3 mm	1.2 mm
Cyntec	PIME061E	0.33 µH–4.7 µH	6.8 mm × 7.3 mm	1.5 mm
Cyntec	PIMB061H	0.1 µH–4.7 µH	6.8 mm × 7.3 mm	1.8 mm
Cyntec	PIMB062D	0.1 µH–6.8 µH	6.8 mm × 7.3 mm	2.4 mm

6.1.1.2.1.2 Selecting the Output Capacitors

TI recommends using ceramic capacitors with low ESR values to provide the lowest output voltage ripple. The output capacitor requires an X7R or an X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the controller operates in PFM mode, and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

TI recommends the use of small ceramic capacitors placed between the inductor and load with many vias to the PGND plane for the output capacitors of the BUCK controllers. This solution typically provides the smallest and lowest cost solution available for DCAP2 controllers.

The selection of the output capacitor is typically driven by the output transient response. Equation 5 provides a rough estimate of the minimum required capacitance to ensure proper transient response. Because the transient response is significantly affected by the board layout, some experimentation is expected in order to confirm that values derived in this section are applicable to any particular use case. Equation 5 is not meant to be an absolute requirement, but rather a rough starting point. Alternatively, some known combination values from which to begin are provided in Table 6-2.

$$C_{OUT} > \frac{I_{TRAN(max)}^{2} \times L}{(V_{IN} - V_{OUT}) \times V_{OVER}} \quad (5)$$

where

- $I_{TRAN(max)}$ is the maximum load current step
- L is the chosen inductance
- V_{OUT} is the minimum programmed output voltage
- V_{IN} is the maximum input voltage
- V_{OVER} is the maximum allowable overshoot from programmed voltage

In cases where the transient current change is very low, the DC stability may become important. Equation 6 approximates the amount of capacitance necessary to maintain DC stability. Again, this is provided as a starting point; actual values will vary on a board-to-board case.

$$C_{OUT} > \frac{V_{OUT} \times 50\ \mu s}{V_{IN} \times f_{SW} \times L} \quad (6)$$

where

- V_{OUT} is the maximum programmed output voltage
- 50 µs is based on internal ramp setup
- V_{IN} is the minimum input voltage
- f_{SW} is the typical switching frequency
- L is the chosen inductance

It is necessary to choose the maximum valuable between Equation 5 and Equation 6.

Table 6-2. Known LC Combinations

$I_{TRAN(max)}$ (A)	L (µH)	V_{OUT} (V)	V_{OVER} (V)	C_{OUT}(µF)
3.5	0.47	1	0.05	220
4	0.47	1	0.05	440
5	0.47	1.35	0.068	440
8	0.33	1	0.06	640
20	0.22	1	0.16	550

6.1.1.2.1.3 Selecting the FETs

This controller is designed to drive two NMOS FETs. Typically, lower R_{DSON} values are better for improving the overall efficiency of the controller, however higher gate charge thresholds will result in lower efficiency so the two need to be balanced for optimal performance. As the R_{DSON} for the low-side FET decreases, the minimum current limit increases; therefore, ensure selection of the appropriate values for the FETs, inductor, output capacitors, and current limit resistor. The Texas Instruments' CSD87331Q3D, CSD87381P and CSD87588N devices are recommended for the controllers, depending on the required maximum current.

6.1.1.2.1.4 Bootstrap Capacitor

To ensure the internal high-side gate drivers are supplied with a stable low-noise supply voltage, a capacitor must be connected between the SWx pins and the respective BOOTx pins. TI recommends placing ceramic capacitors with the value of 0.1 µF for the controllers. During testing, a 0.1-µF, size 0402, 10-V capacitor is used for the controllers.

TI recommends reserving a small resistor in series with the bootstrap capacitor in case the turnon and turnoff of the FETs must be slowed to reduce voltage ringing on the switch node, which is a common practice for controller design.

6.1.1.2.1.5 Setting the Current Limit

The current-limiting resistor value must be chosen based on Equation 1.

6.1.1.2.1.6 Selecting the Input Capacitors

Due to the nature of the switching controller with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and also for minimizing the interference with other circuits caused by high input-voltage spikes. For the controller, a typical 2.2-µF capacitor can be used for the DRV5V_x_x pin to handle the transients on the driver. For the FET input, 10 µF of input capacitance (after derating) is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

NOTE

Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

TI recommends placing a ceramic capacitor as close as possible to the FET across the respective VSYS and PGND pins of the FETs. The preferred capacitors for the controllers are two Murata GRM21BR61E226ME44: 22-µF, 0805, 25-V, ±20%, or similar capacitors.

6.1.1.2.2 Converter Design Procedure

Designing the converter has only two steps: design the output filter and select the input capacitors.

The converter must be supplied by a 5-V source. Figure 6-3 shows a diagram of the converter.

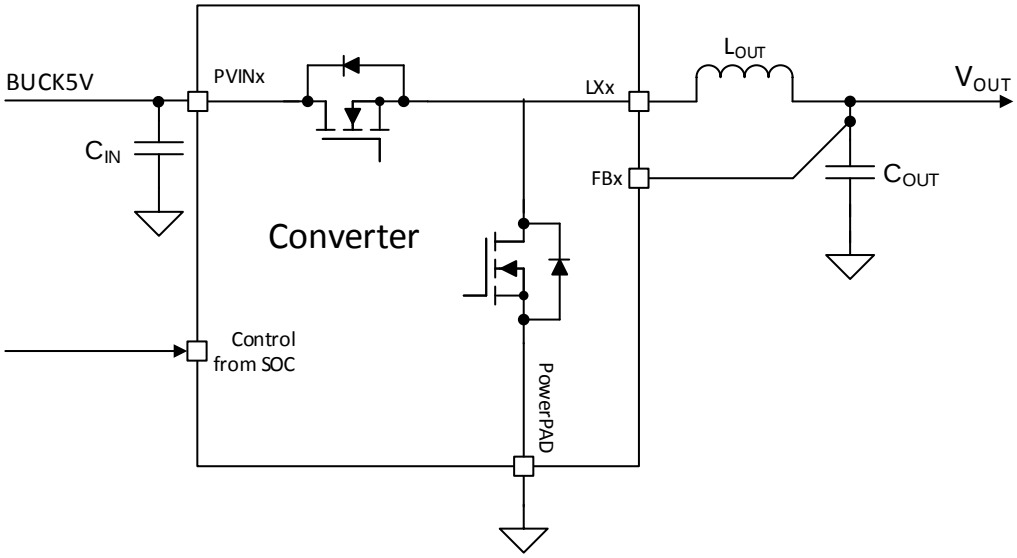


Figure 6-3. Converter Diagram

6.1.1.2.2.1 Selecting the Inductor

It is required that an inductor be placed between the external FETs and the output capacitors. Together, the inductor and output capacitors form a double pole in the control loop that contributes to stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases, the ripple current decreases, which typically results in an increase in efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

NOTE

Internal parameters for the converters are optimized for a 0.47 µH inductor, however it is possible to use other inductor values as long as they are chosen carefully and thoroughly tested.

Equation 7 shows the calculation for the recommended inductance for the converter.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}} \quad (7)$$

where

- V_{OUT} is the typical output voltage
- V_{IN} is the typical input voltage
- f_{SW} is the typical switching frequency
- $Iout_{MAX}$ is the maximum load current
- K_{IND} is the ratio of $I_{Lripple}$ to the $I_{out(max)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4.

With the chosen inductance value and the peak current for the inductor in steady state operation, $I_{L(MAX)}$ can be calculated using Equation 8. The rated saturation current of the inductor must be higher than the $I_{L(MAX)}$ current.

$$I_{LMAX} = Iout_{MAX} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \quad (8)$$

Following these equations, the preferred inductor selected for the converters is listed in Table 6-3.

Table 6-3. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIFE32251B-R47MS	0.47 µH	3.2 mm × 2.5 mm	1.2 mm

6.1.1.2.2.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values are recommended because they provide the lowest output voltage ripple. The output capacitor requires either an X7R or X5R rating. Y5V and Z5U capacitors, aside from the wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in PFM mode and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC-bias voltage.

For the output capacitors of the BUCK converters, TI recommends placing small ceramic capacitors between the inductor and load with many vias to the PGND plane. This solution typically provides the smallest and lowest-cost solution available for DCAP2 controllers.

The output capacitance must equal or exceed the minimum capacitance listed for BUCK3, BUCK4, and BUCK5 (assuming quality layout techniques are followed).

6.1.1.2.2.3 Selecting the Input Capacitors

Due to the nature of the switching converter with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For the PVINx pin, 2.5 µF of input capacitance (after derating) is required for most applications. A ceramic capacitor is recommended to achieve the low ESR requirement. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. The input capacitor can be increased without any limit for better input-voltage filtering.

NOTE

Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

The preferred capacitor for the converters is one Samsung CL05A106MP5NUNC: 10-µF, 0402, 10-V, ±20%, or similar capacitor.

6.1.1.2.3 LDO Design Procedure

The VTT LDO must handle the fast load transients from the DDR memory for termination. Therefore, it is recommended to use ceramic capacitors to maintain a high amount of capacitance with low ESR on the VTT LDO outputs and inputs. The preferred output capacitors for the VTT LDO are the GRM188R60J226MEA0 from Murata (22 µF, 0603, 6.3 V, ±20%, or similar capacitors). The preferred input capacitor for the VTT LDO is the CL05A106MP5NUNC from Samsung (10-µF, 0402, 10-V, ±20%, or similar capacitor).

The remaining LDOs must have input and output capacitors chosen based on the values in Section 4.9.

6.1.1.3 Application Curves

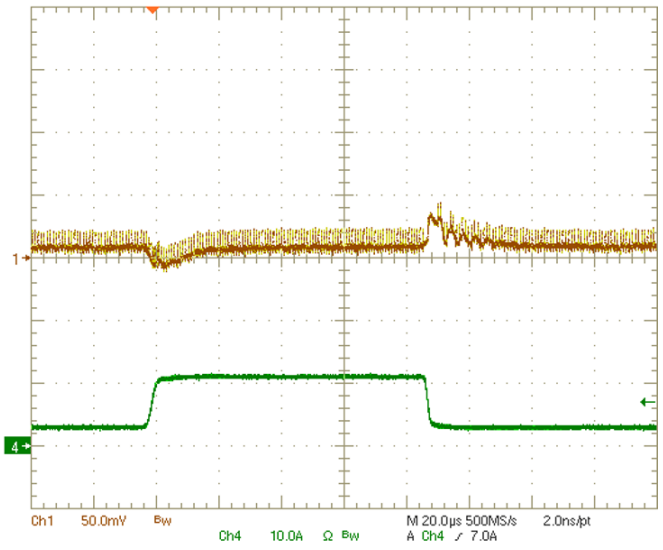


Figure 6-4. BUCK2 Controller Load Transient

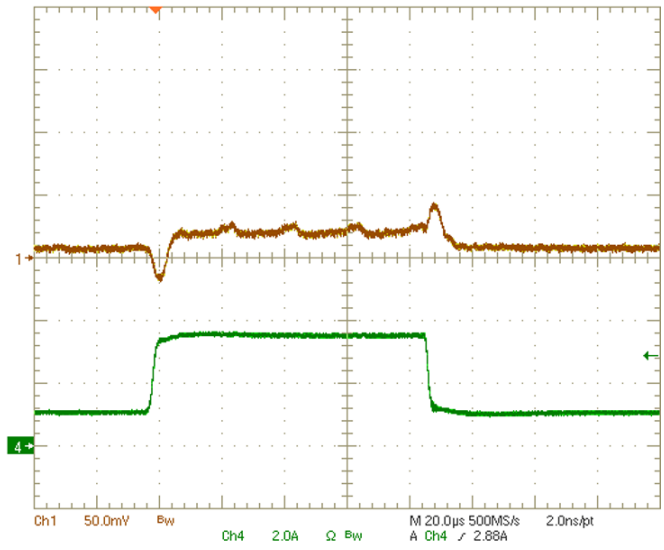


Figure 6-5. BUCK3 Controller Load Transient

6.2 VIN 5-V Application

The PMIC can be operated by a 5-V input voltage to the system because the power path of the controller does not go through the device itself. The concept is simple: supply the controller VINs with the 5-V input, and supply the VSYS with a 5.8-V step-up of the 5 V with a boost or charge pump. The 5.8 V is recommended because the UVLO of the internal LDO5 is at 5.6 V and the device measures the voltage at VSYS and determines the optimum internal compensation and controller settings thus, it is ideal the VSYS be close to the VIN of the controllers.

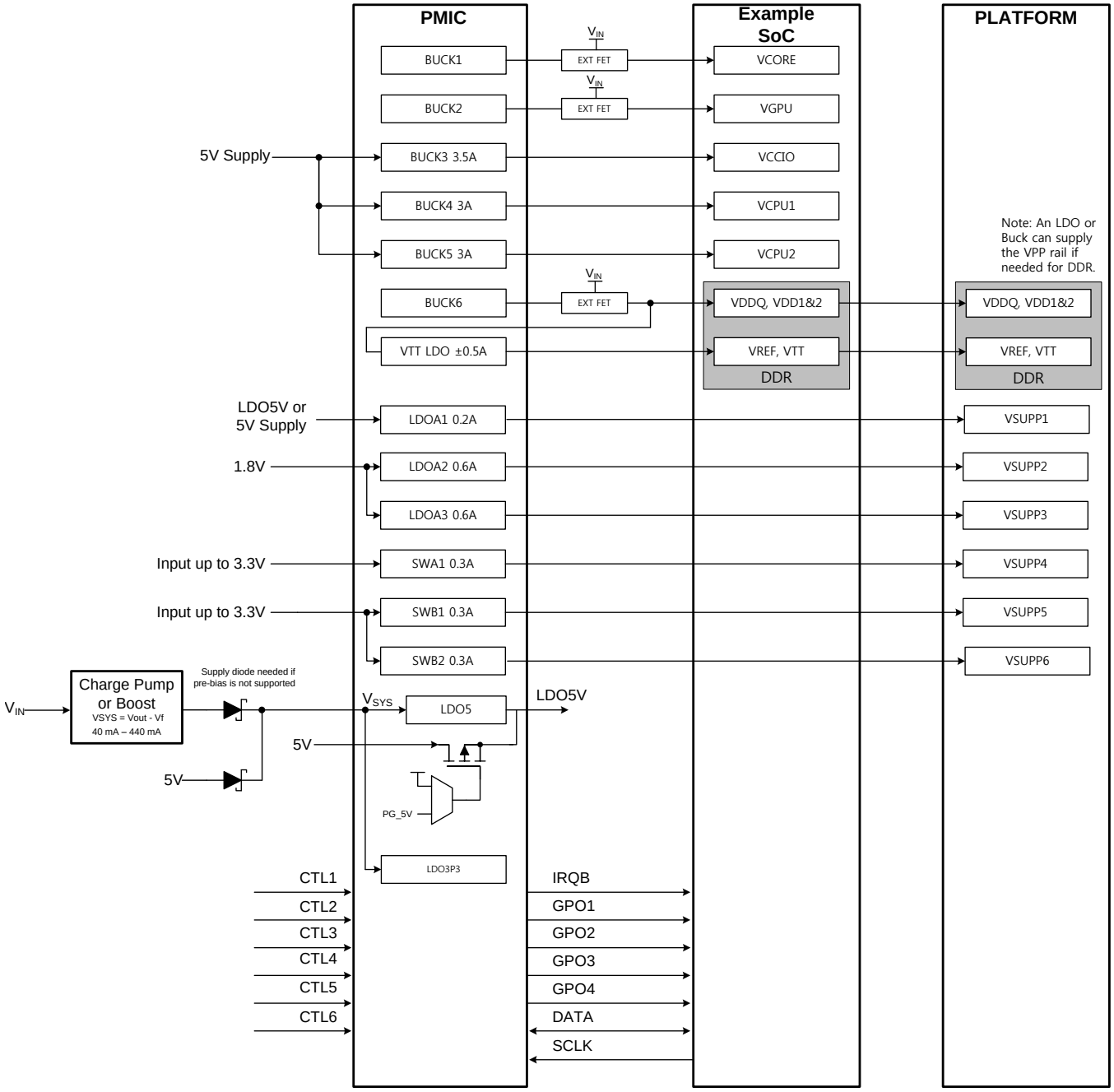


Figure 6-6. VIN 5-V Application

6.2.1 Design Requirements

The PMIC requires a step-up voltage from the 5-V input to 5.8 V for the VSYS supply. TI recommends keeping the VSYS near 5.8 V for optimization of the controllers.

Depending on the application use cases, the supply current to the VSYS can require from 40 mA with the drivers being supplied by the 5-V input to 440 mA with the drivers being supplied by the LDO5 and the LDOA1 being operated at max loading. This means that a charge pump may be used in some applications like the 5-V input but in others, a small boost may be required.

A Schottky diode from the 5-V input to the VSYS is recommended to ensure the VSYS is biased and the internal reference LDOs are on before the step-up regulator is enabled or fully ramped up. If the step-up cannot tolerate pre-bias condition then, 2 diodes may be needed to prevent the initial 5-V supply biasing the output of the step-up.

6.2.2 Design Procedure

To design a 5-V input application, first provide a step-up voltage from the 5-V input to the VSYS. Design the step-up to output a voltage near 5.8 V. Next, route the 5-V input to the controller and converter VINs. Thus, all power paths (*all high currents*) are routed through the controllers or directly to the converters. None of the high currents are required from the step-up supply. After the input stage is complete, the rest of the system can be designed as normal following the typical application procedure. Only the controller design is affected by the input voltage change.

6.2.2.1 Controller Design Procedure

Designing the controller can be broken down into the following steps:

1. Design the output filter.
2. Select the FETs.
3. Select the bootstrap capacitor, same procedure as Section 6.1.1.2.1.4
4. Select the input capacitors.
5. Set the current limits. Will be very different values but, same procedure as Section 6.1.1.2.1.5

Controllers BUCK1, BUCK2, and BUCK6 require a 5-V supply and capacitors at their corresponding DRV5V_x_x pins. For most applications, the DRV5V_x_x input must come from the LDO5P0 pin to ensure uninterrupted supply voltage; a 2.2-µF, X5R, 20%, 10-V, or similar capacitor must be used for decoupling.

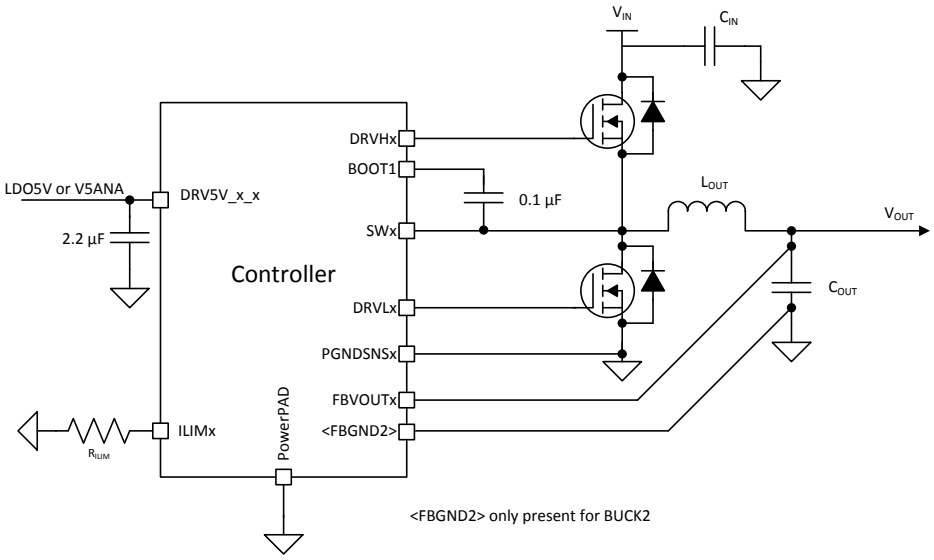


Figure 6-7. 5-V Input Controller Diagram

6.2.2.1.1 Selecting the LC Output Filter

Selecting the inductor is the same as the typical application. Refer to Section 6.1.1.2.1.1 for desired inductor calculations.

Selection of the output capacitance is also the same as the typical design procedure, but due to the reduced V_{IN}, the likely required minimum C_{OUT} will be larger. This is because the V_L, or $V_{IN} – V_{OUT}$, is much smaller. Refer to Section 6.1.1.2.1.2 for output capacitance selection calculations.

6.2.2.1.2 Selecting the FETs

For lower current and lower input voltage applications, smaller lower-cost FETs can be selected with the trade off of R_{DSON} and max VDS because the output power is reduced. The CSD85301Q2 is recommended for lower current applications. The CSD87381P is recommended for mid-range current applications.

6.2.2.1.3 Setting the Current Limit

The current-limiting resistor value must be chosen based on Equation 1.

6.2.2.1.4 Selecting the Input Capacitors

Due to the nature of the switching controller with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and also for minimizing the interference with other circuits caused by high input-voltage spikes. For the controller, a typical 2.2-µF capacitor can be used for the DRV5V_x_x pin to handle the transients on the driver. For the FET input, 10 µF of input capacitance (after derating) is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

NOTE

Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

TI recommends placing a ceramic capacitor as close as possible to the FET across the respective VIN and PGND pins of the FETs. The preferred capacitors for the controllers are two Murata GRM188R61A226ME15 (22-µF, 0603, 10-V, ±20%) or similar capacitors.

6.2.3 Application Curve

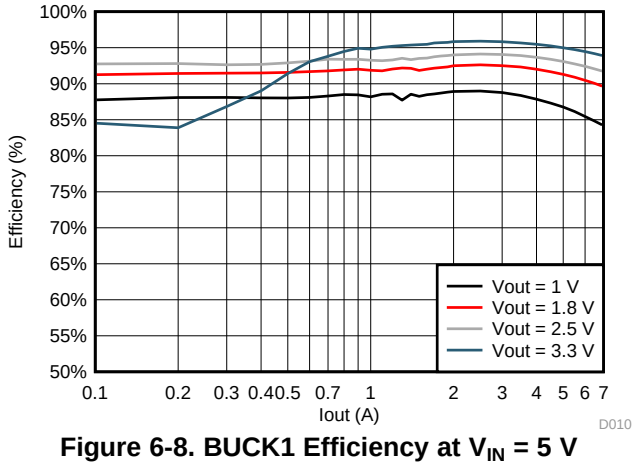


Figure 6-8. BUCK1 Efficiency at V_{IN} = 5 V

6.3 Do's and Don'ts

- Connect the LDO5V output to the DRV5V_x_x inputs for situations where an external 5-V supply is not initially available or is not available the entire time PMIC is on. If the external 5-V supply is always present, then DRV5V_x_x can be directly connected to remove the V5ANA-to-LDO5P0 load switch R_{DSON}.
- Ensure that none of the control pins are potentially floating.
- Include 0-Ω resistors on the DRVH and BOOT pins of controllers on prototype boards, which allows for slowing the controllers if the system is unable to handle the noise generated by the large switching or if switching voltage is too large due to layout.
- Do **not** connect the V5ANA power input to a different source other than PVINx. A mismatch here causes reference circuits to regulate incorrectly.
- Do **not** supply the V5ANA power input before the VSYS. Reference biasing of the internal FETs may turn on the HS FET passing the input to the output until VSYS is biased.

7 Power Supply Coupling and Bulk Capacitors

This device is designed to work with several different input voltages. The minimum voltage on the VSYS pin is 5.6 V for the device to start up; however, this is a low power rail. The input to the FETs must be between 4.5 V to 21 V as long as the proper BOM choices are made. Input to the converters must be 5 V. For the device to output maximum power, the input power must be sufficient. For the controllers, VIN must be able to supply sufficient input current for the application's output power. For the converters, PVINx must be able to supply 2 A typically.

A best practice here is to determine power usage by the system and back-calculate the necessary power input based on expected efficiency values.

8 Layout

8.1 Layout Guidelines

For a detailed description regarding layout recommendations, refer to the *TPS65086x Design Guide* (SLVUAJ9) and to the *TPS650860 Schematic and Layout Check List* (SLVA734). For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can have stability problems and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the IC. Use a common-ground node for power ground and use a different, isolated node for control ground to minimize the effects of ground noise. Connect these ground nodes close to the AGND pin by one or two vias. Use of the design guide is highly encouraged in addition to the following list of other basic requirements:

- Do **not** allow the AGND, PGNDSNSx, or FBGND2 to connect to the thermal pad on the top layer.
- To ensure proper sensing based on FET R_{DSON}, PGNDSNSx must not connect to PGND until very close to the PGND pin of the FET.
- All inductors, input/output caps, and FETs for the converters and controller must be on the same board layer as the IC.
- To achieve the best regulation performance, place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible.
- Bootstrap capacitors must be placed close to the IC.
- The internal reference regulators must have their input and output caps placed close to the IC pins.
- Route DRVHx and SWx as a differential pair. Ensure that there is a PGND path routed in parallel with DRVLx, which provides optimal driver loops.

8.2 Layout Example

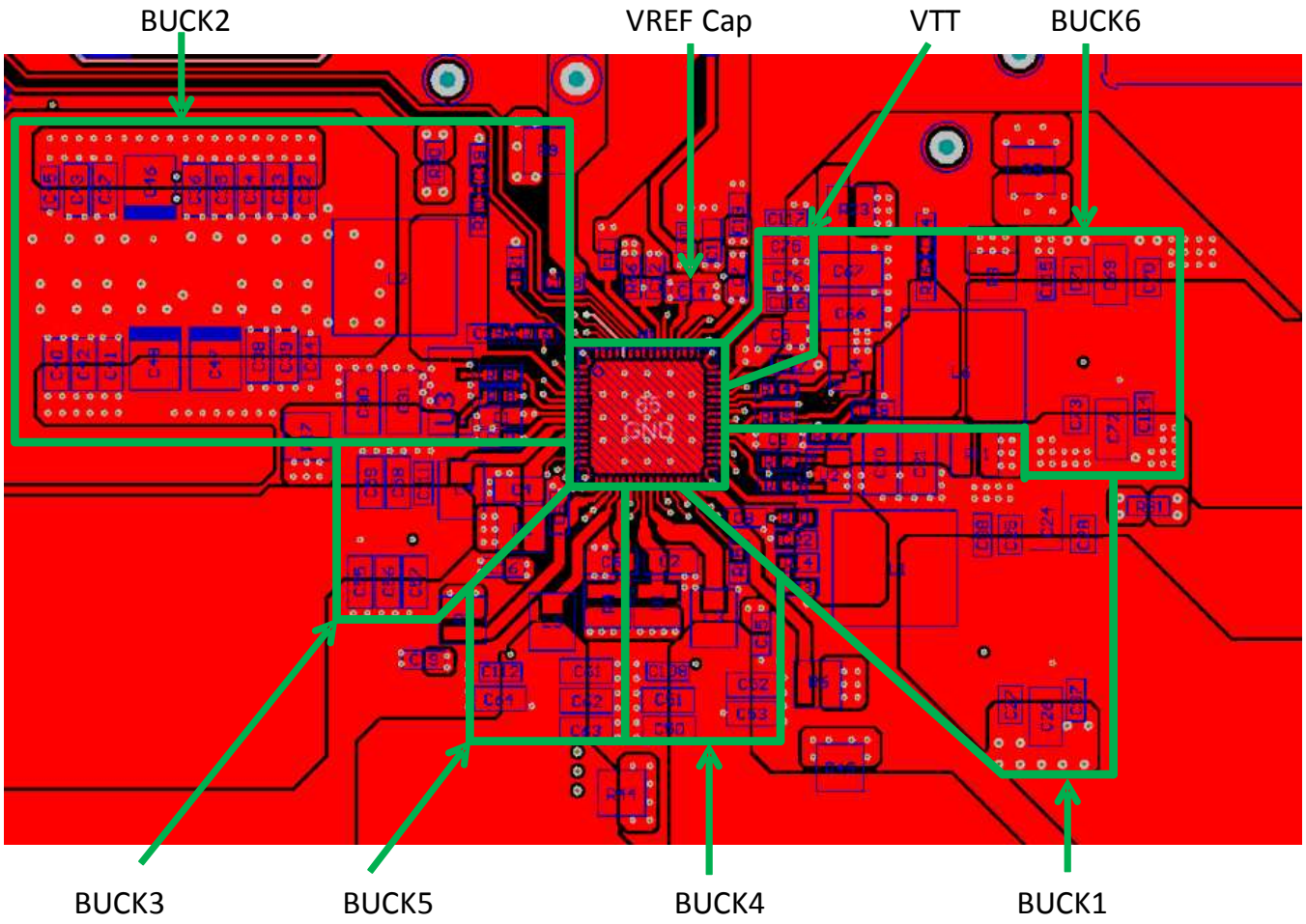


Figure 8-1. EVM Layout Example With All Components on the Top Layer

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.1.2 Development Support

SLVA734 *TPS65086x Schematic and Layout Checklist*

SLVUAJ9 *TPS650860 Design Guide*

9.2 Documentation Support

9.2.1 Related Documentation

SLVUAH2 *TPS65086x Evaluation Module*

SLYY077 *Power management integrated buck controllers for distant point-of-load applications*

9.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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All other trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS650860A0RSKR	ACTIVE	VQFN	RSK	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	T650860A0 PG1.0	Samples
TPS650860A0RSKT	ACTIVE	VQFN	RSK	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	T650860A0 PG1.0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

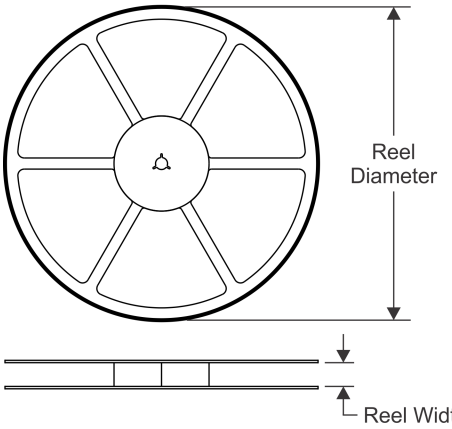
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

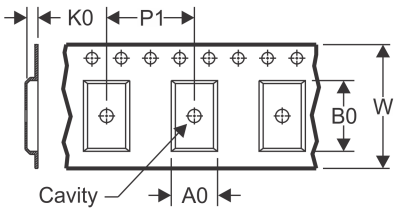
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

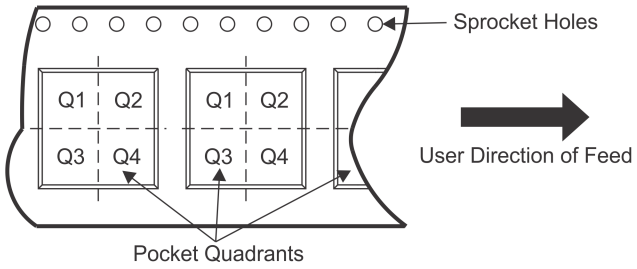


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

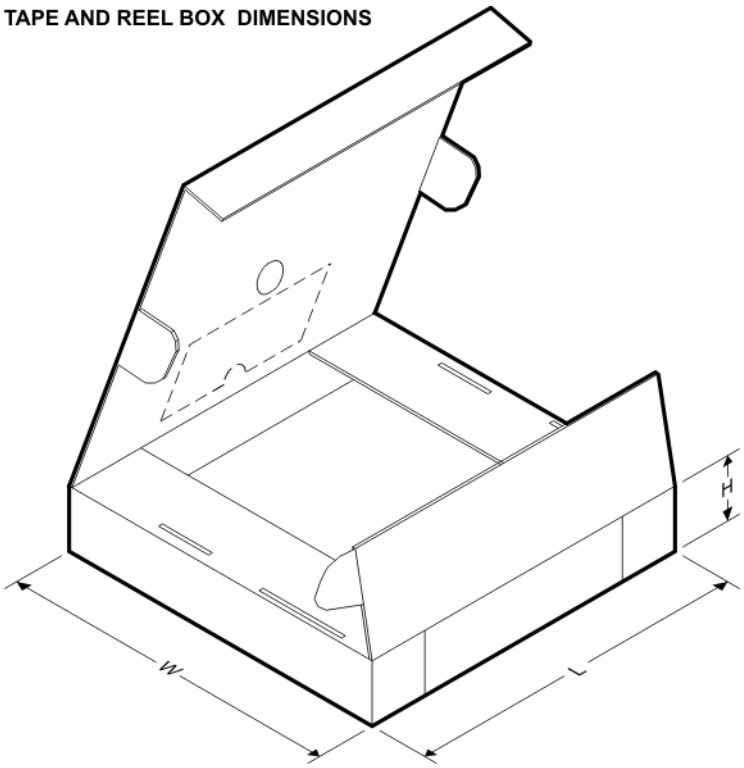
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650860A0RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650860A0RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

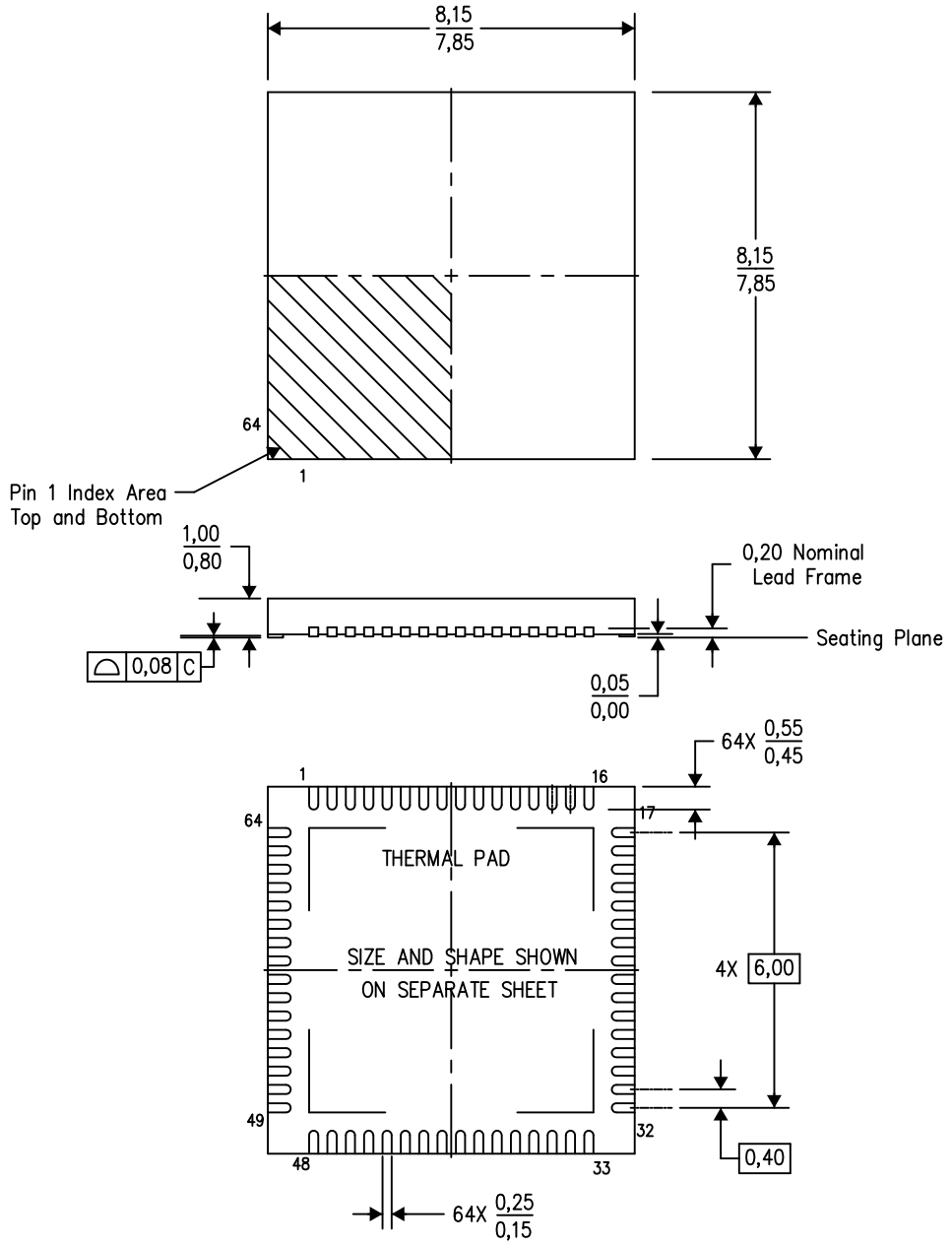
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650860A0RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS650860A0RSKT	VQFN	RSK	64	250	210.0	185.0	35.0

RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4207547/C 04/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

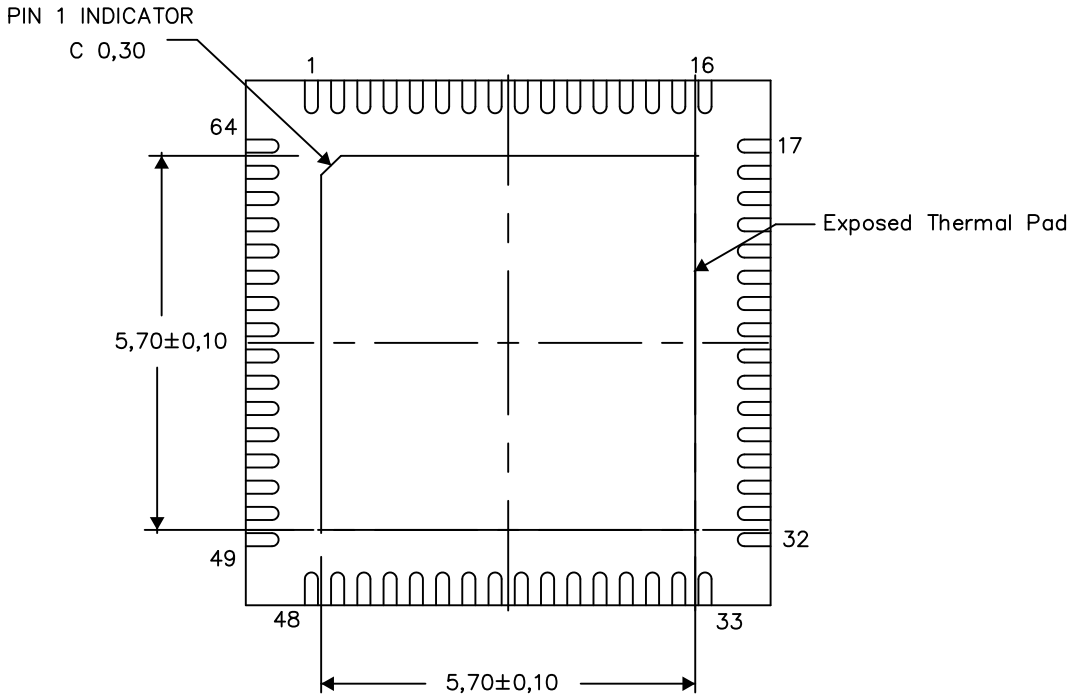
RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



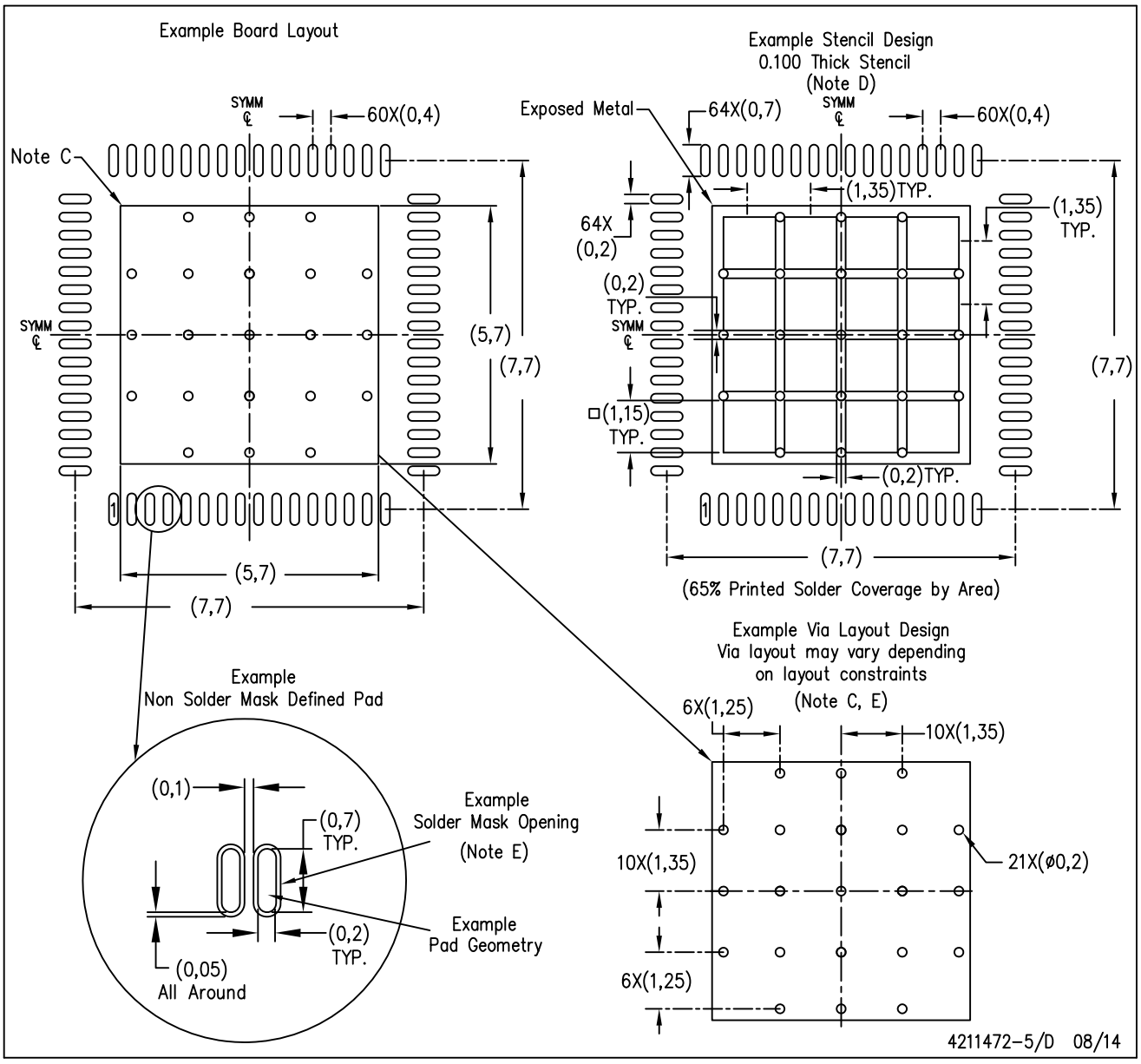
Bottom View

Exposed Thermal Pad Dimensions

4208001–5/H 08/14

NOTE: A. All linear dimensions are in millimeters

RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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