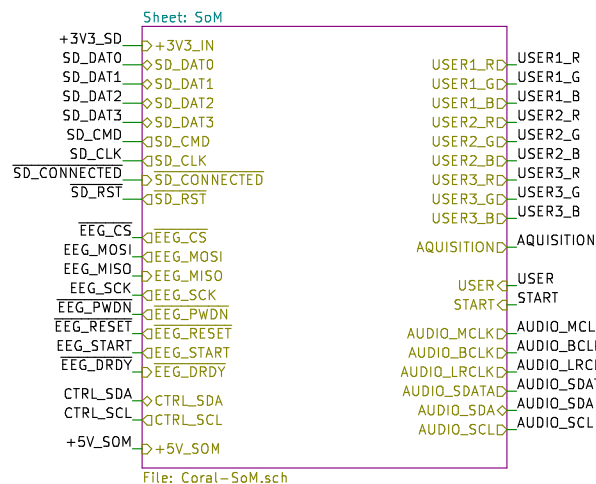
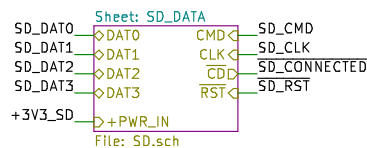
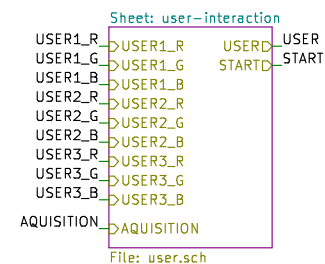
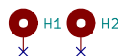


PS I2C addresses:
 - 0x5C: HW monitor
 Audio I2C address: 0x0A



State:

- Preliminary schematics: done
- Layout: done
- Revised schematic: done
- Schematic validation: done
- Layout validation: done
- BOM optimization: done
- Physical testing: to do



Designed by Xavier L'Heureux

MIST Lab

Sheet: /

File: mist-eeg.sch

Title: Portiloop

Size: USLetter Date: 2021-08-03

KiCad E.D.A. kicad 5.1.10

Rev: 1D

Id: 1/11

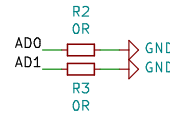
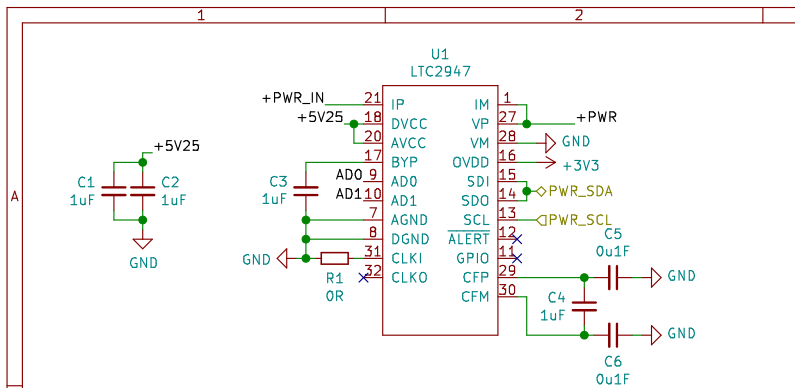
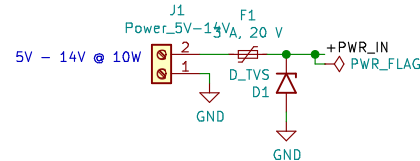


Table 3. I²C Addresses

ADD	AD1	8-BIT ADDRESS BYTE WRITE	8-BIT ADDRESS BYTE READ	7-BIT DEVICE ADDRESS	BINARY DEVICE ADDRESS							
				a6:a0	a6	a5	a4	a3	a2	a1	a0	R/W
L	L	0xB8	0xB9	0x5C	1	0	1	1	1	0	0	1/0
L	H	0xBA	0xBB	0x5D	1	0	1	1	1	0	1	1/0
L	R	0xBC	0xBD	0x5E	1	0	1	1	1	1	0	1/0
R	L	0xC8	0xC9	0x64	1	1	0	0	1	0	0	1/0
R	H	0xCA	0xCB	0x65	1	1	0	0	1	0	1	1/0
R	R	0xCC	0xCD	0x66	1	1	0	0	1	1	0	1/0

Note 10: L: tie to DGND, H: tie to OVDD, R: resistor, connect to DGND with a 100k Ω resistor.

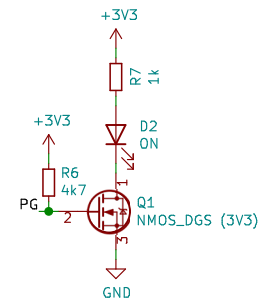
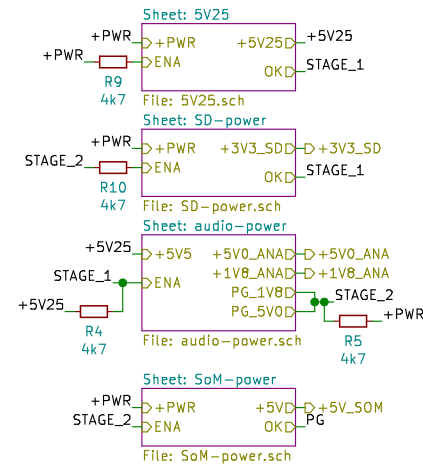


HWMon



HWMon bypass

External power port & protection



Rails

3V3 V @ 1.75 A (TPS63070):
– SD card, 2.88 W max

5V0 (clean) @ 50 mA:
 - ADS1299 Analog supply
 - LTC2947 supply

1V8 (clean) @ 10 mA:
- ADAU1777 Analog supply

5V25 (intermediate) @ 100 mA:
– clean voltage buck-boost

- 5V @ 1.2 A:
 - SoM core voltage

Sequencing

ADC supplies:
1 - 5V25 (intermediate)
2 - 5V & 1V8 (clean)

Audio:
1 - 1.8V (clean)
2 - 3.3V

Global:
1 - 5.25V (Intermediate)
2 - 1.8V (Clean), 5V (Clean)
3 - 3.3V, 5V (Board power)

Designed by Xavier L'Heureux

MIST Lab

Sheet: /power/

File: power.sch

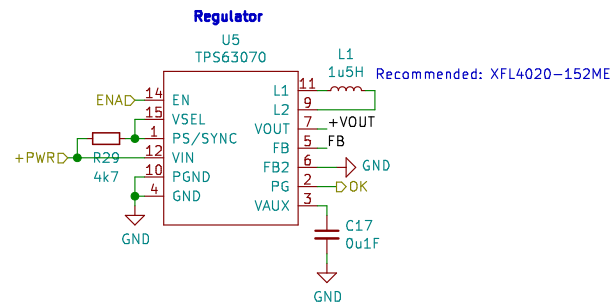
Title: Portiloop

Size: USLetter	Date: 2021-08-03
----------------	------------------

Size: 65Kb	Date: 2019-01-10
KiCad E.D.A.	kicad 5.1.10

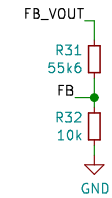
Rev: 1D

Id: 2/11

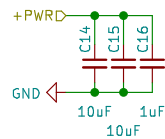


Feedback divider

$$R_1 = R_2 \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$



Input capacitors



Output capacitors

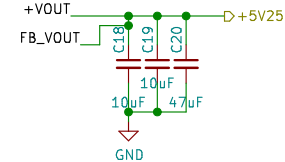


Table 3. Output Filter Selection

INDUCTOR VALUE [μH] ⁽¹⁾	OUTPUT CAPACITOR VALUE [μF] ⁽²⁾			
	22	47	68	100
1.0		√	√	√
1.5		√ ⁽³⁾	√	√
2.2			√	√

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
- (2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
- (3) Typical application. Other check marks indicates recommended filter combinations

Designed by Xavier L'Heureux

MIST Lab

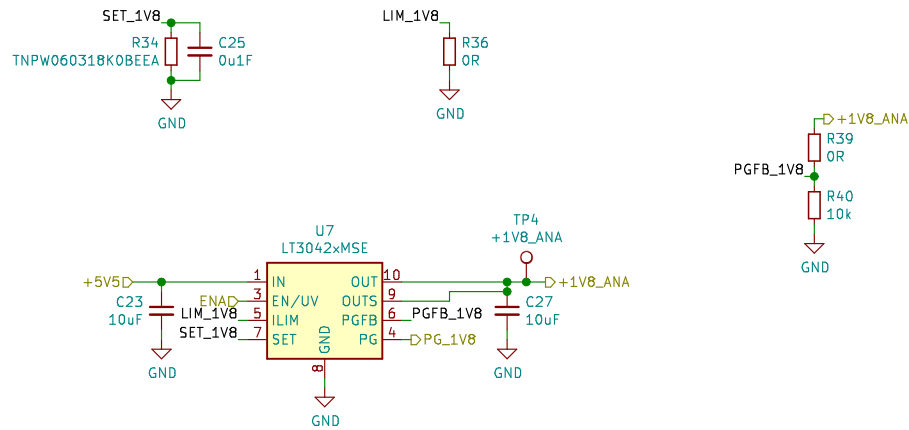
Sheet: /power/5V25/
File: 5V25.sch

Title: Portiloop

Size: USLetter Date: 2021-08-03
KiCad E.D.A. kicad 5.1.10

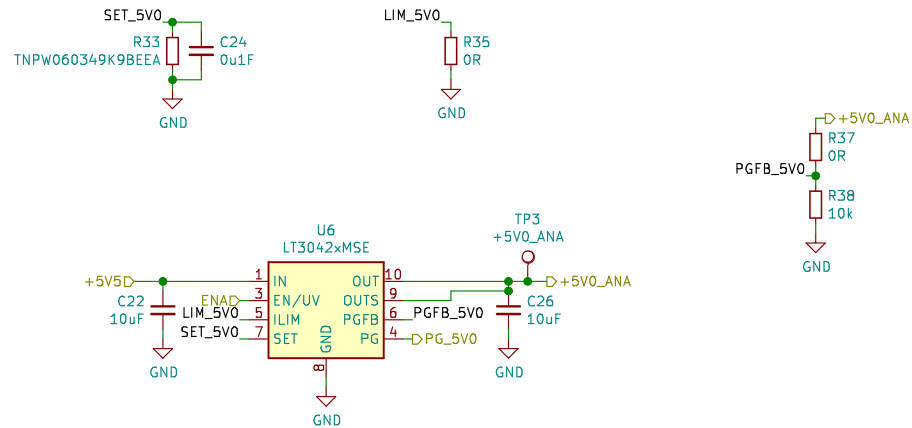
Rev: 1D
Id: 3/11

1V8 (clean regulator)



$$R_{set} = V_{out} / 100\mu A$$

5V0 (clean regulator)



Designed by Xavier L'Heureux

MIST Lab

Sheet: /power/audio-power/

File: audio-power.sch

Title: Portiloop

Size: USLetter Date: 2021-08-03

KiCad E.D.A. kicad 5.1.10

Rev: 1D

Id: 4/11

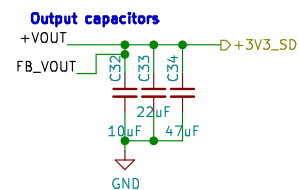
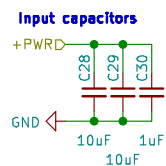
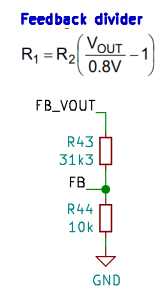
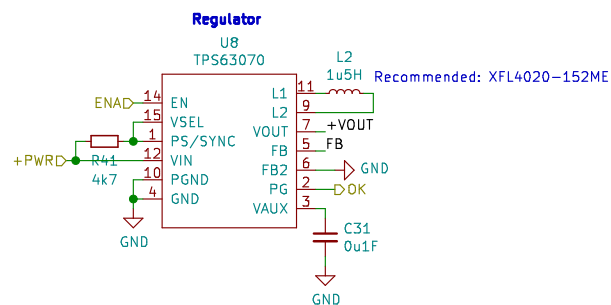


Table 3. Output Filter Selection

INDUCTOR VALUE [μH] ⁽¹⁾	OUTPUT CAPACITOR VALUE [μF] ⁽²⁾			
	22	47	68	100
1.0		√	√	√
1.5		√ ⁽³⁾	√	√
2.2			√	√

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
- (2) Capacitance tolerance and bias voltage de-rating of -20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
- (3) Typical application. Other check marks indicates recommended filter combinations

Designed by Xavier L'Heureux

MIST Lab

Sheet: /power/SD-power/
File: SD-power.sch

Title: Portiloop

Size: USLetter Date: 2021-08-03

KiCad E.D.A. kicad 5.1.10

Rev: 1D

Id: 5/11

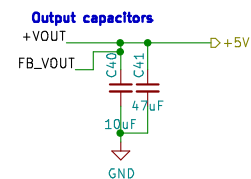
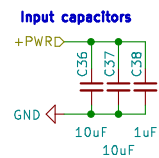
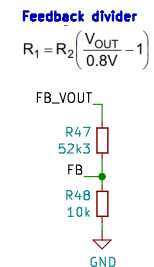
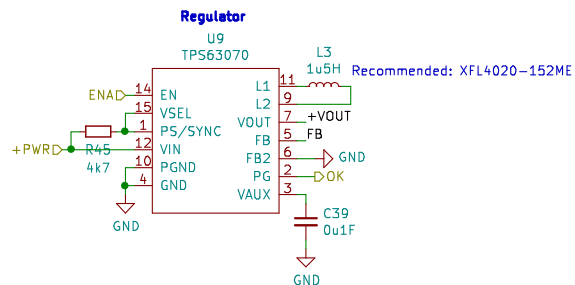


Table 3. Output Filter Selection

INDUCTOR VALUE [μH] ⁽¹⁾	OUTPUT CAPACITOR VALUE [μF] ⁽²⁾			
	22	47	68	100
1.0		√	√	√
1.5		√ ⁽³⁾	√	√
2.2			√	√

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
- (2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
- (3) Typical application. Other check marks indicates recommended filter combinations

Sheet: /power/SoM-power/
File: SoM-power.sch

Title:

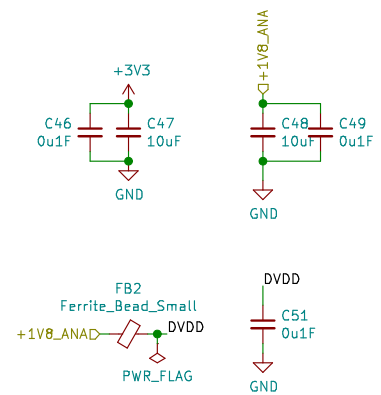
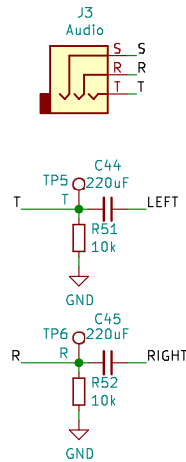
Size: A4 Date: 2021-08-03

KICad E.D.A. kicad 5.1.10

Rev: 1D

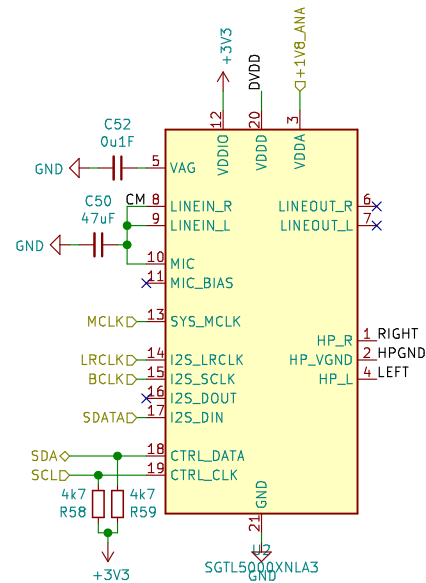
Id: 6/11

According to wikipedia:
T: Left
R: Right
S: GND



Jack output

Power & decoupling



R58, R59 => 4k7
TP9 => deleted
R49, R50, R54, R53 => deleted
R57, D4 => deleted
C52, C53 => deleted
R55, R56 => deleted
FB2 => added

CODEC

Designed by Xavier L'Heureux

MIST Lab

Sheet: /audio/

File: audio.sch

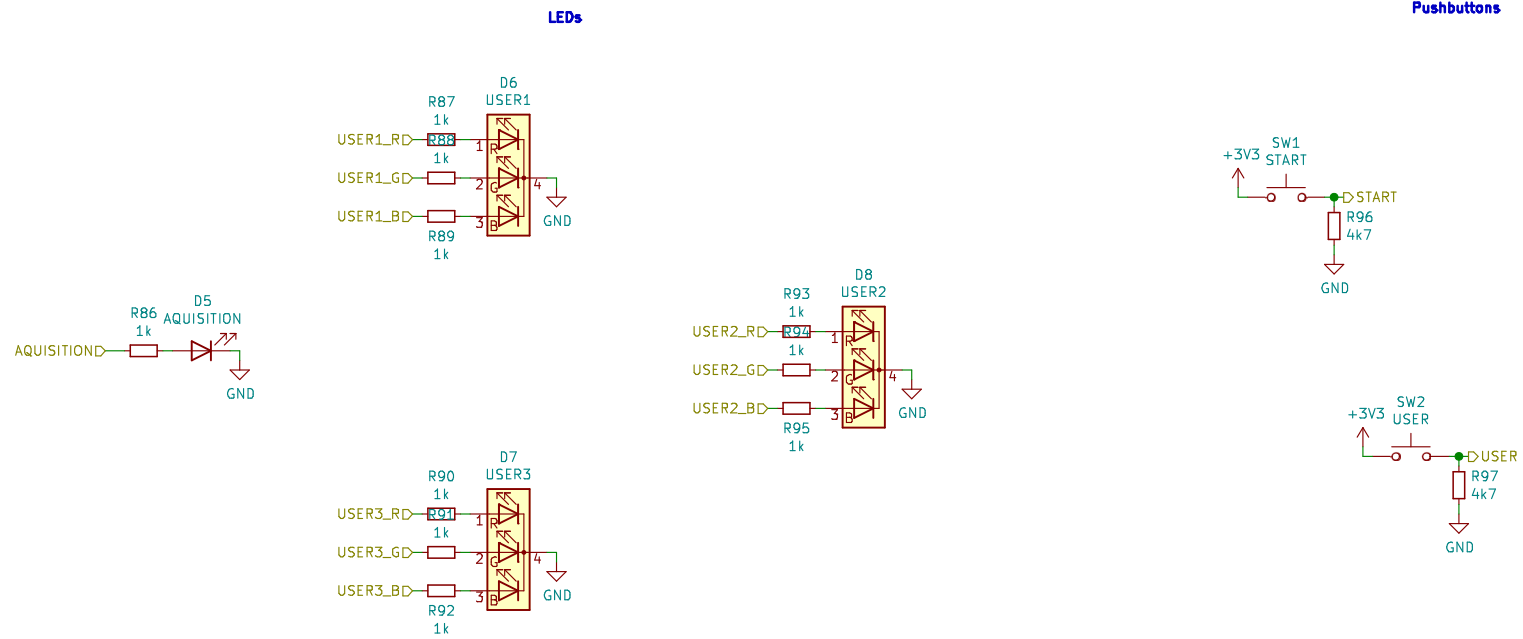
Title: Portiloop

Size: USLetter Date: 2021-08-03

KiCad E.D.A. kicad 5.1.10

Rev: 1D

Id: 7/11



Designed by Xavier L'Heureux

MIST Lab

Sheet: /user-interaction/

File: user.sch

Title: Portiloop

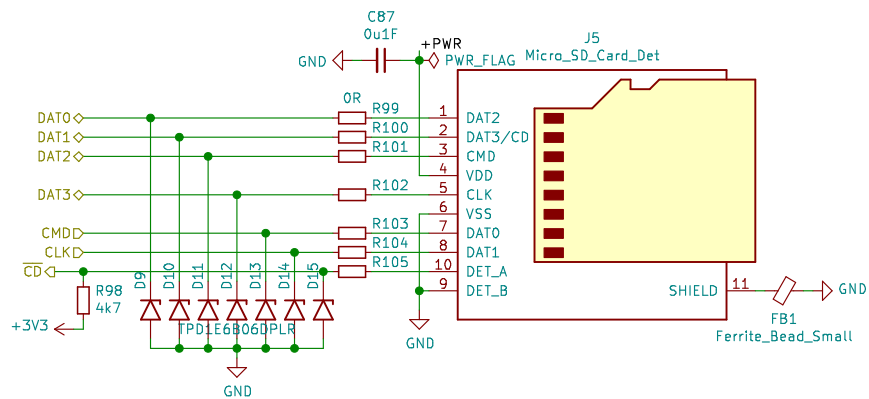
Size: USLetter Date: 2021-08-03

KiCad E.D.A. kicad 5.1.10

Rev: 1D

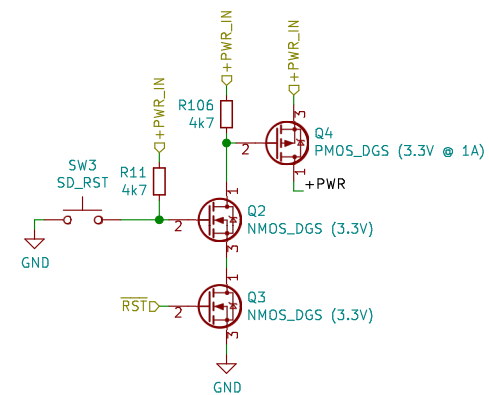
Id: 9/11

SD Card module



Resistor array: test points

Reset switch



Designed by Xavier L'Heureux

MIST Lab

Sheet: /SD_DATA/

File: SD.sch

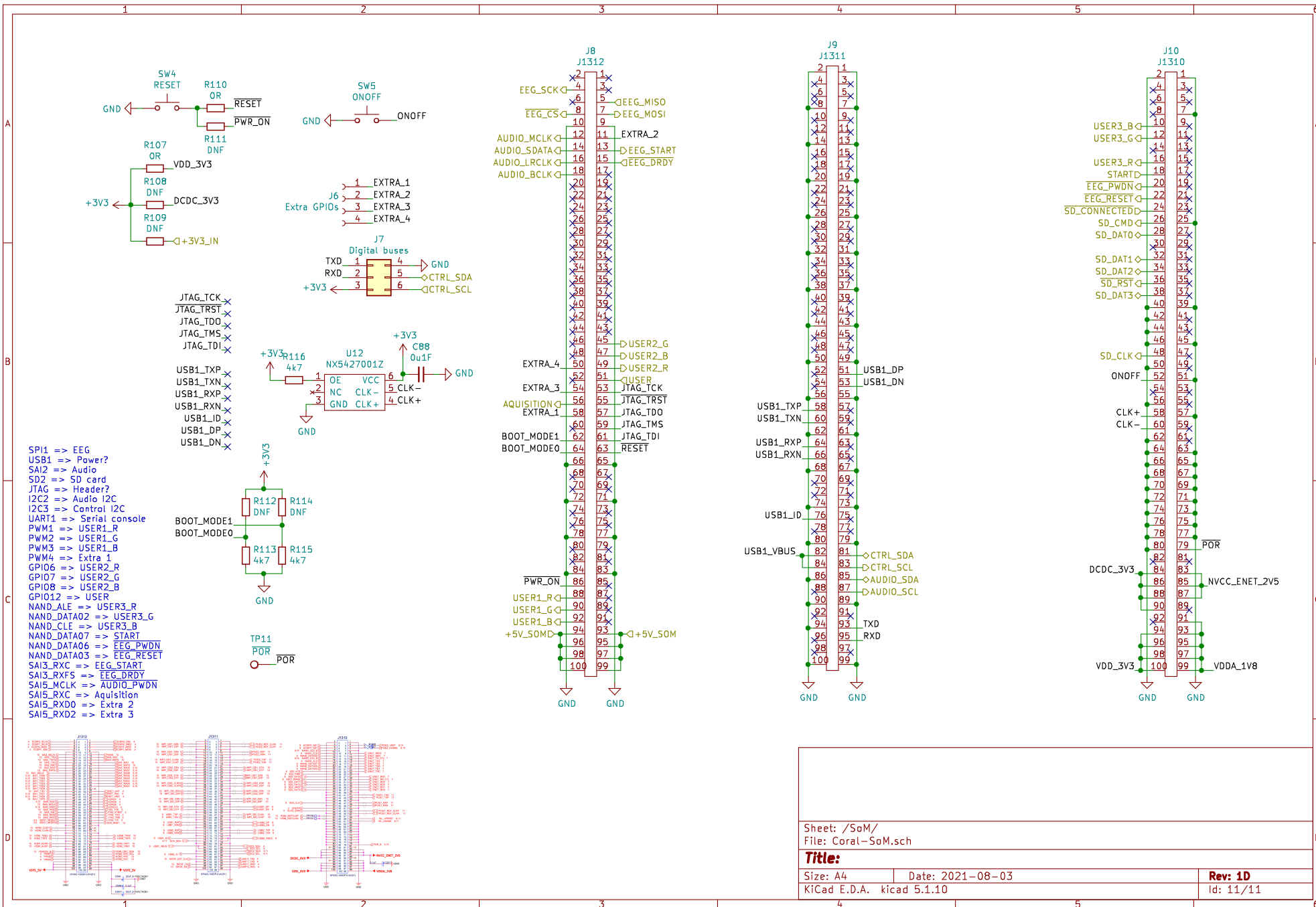
Title: Portiloop

Size: USLetter Date: 2021-08-03

KiCad E.D.A. kicad 5.1.10

Rev: 1D

Id: 10/11



Sheet: /SoM/ File: Coral-SoM.sch		
Title:		
Size: A4	Date: 2021-08-03	Rev: 1D
KiCad E.D.A. kicad 5.1.10		Id: 11/11