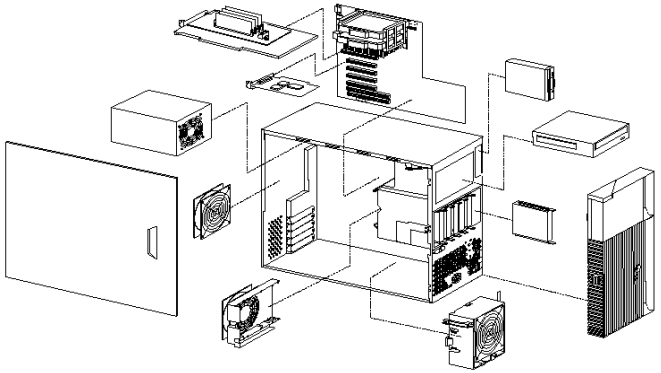
Department of Computer Science and Engineering
School of Science, Engineering & Technology



CSE 317: Computer Organization & Architecture

Wahidul Alam, Lecturer, CSE, SoSET, EDU

Topic 4 – Interrupts

- Interrupts
- Instruction Cycle with Interrupts
- Multiple Interrupts
- Time Sequence of Multiple Interrupts

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Interrupts

Mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing

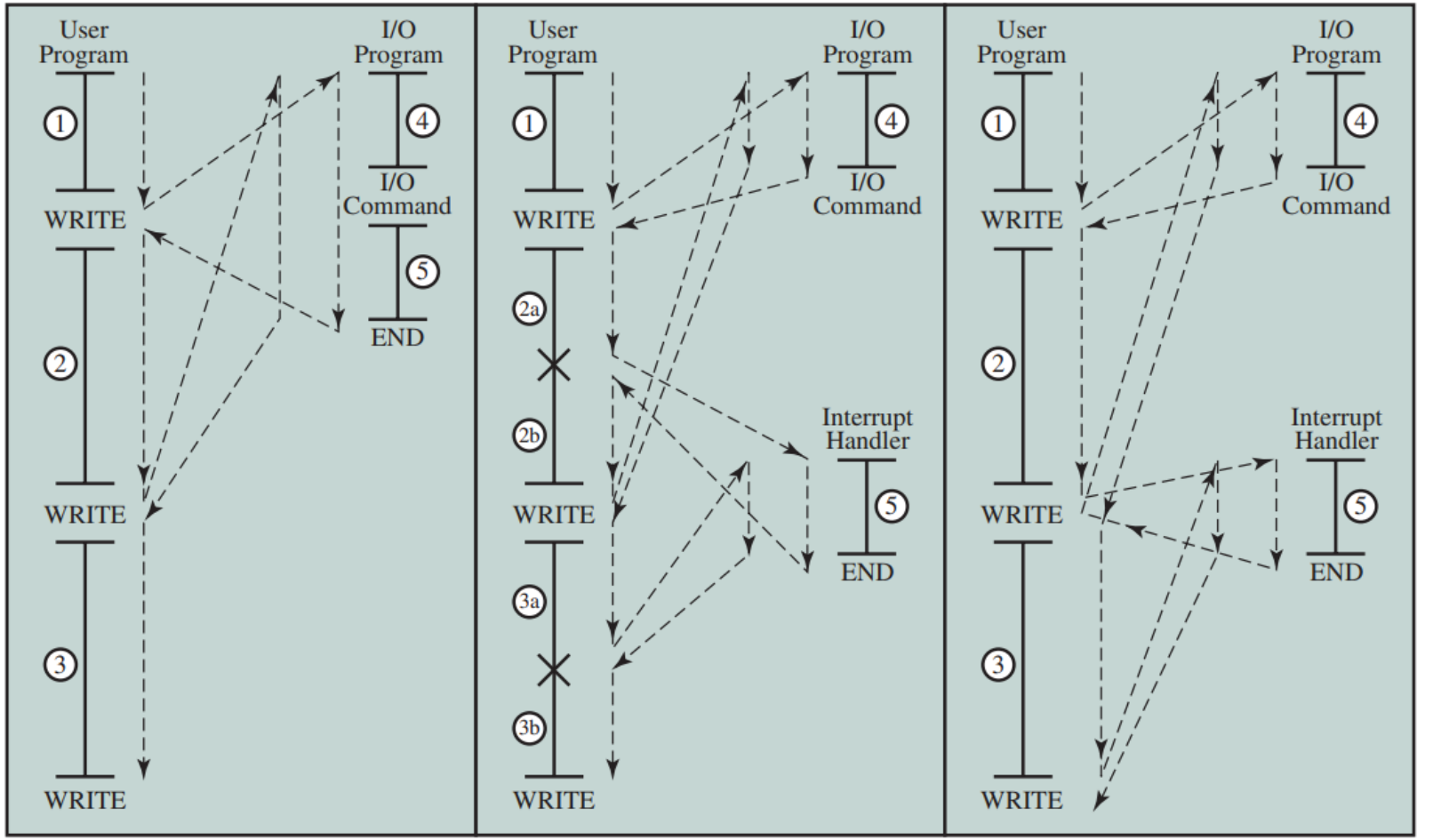
Program
- e.g. overflow, division by zero

Timer
- Generated by internal processor timer
- Used in pre-emptive multi-tasking

I/O
- from I/O controller

Hardware failure
- e.g. memory parity error

Program Flow Control



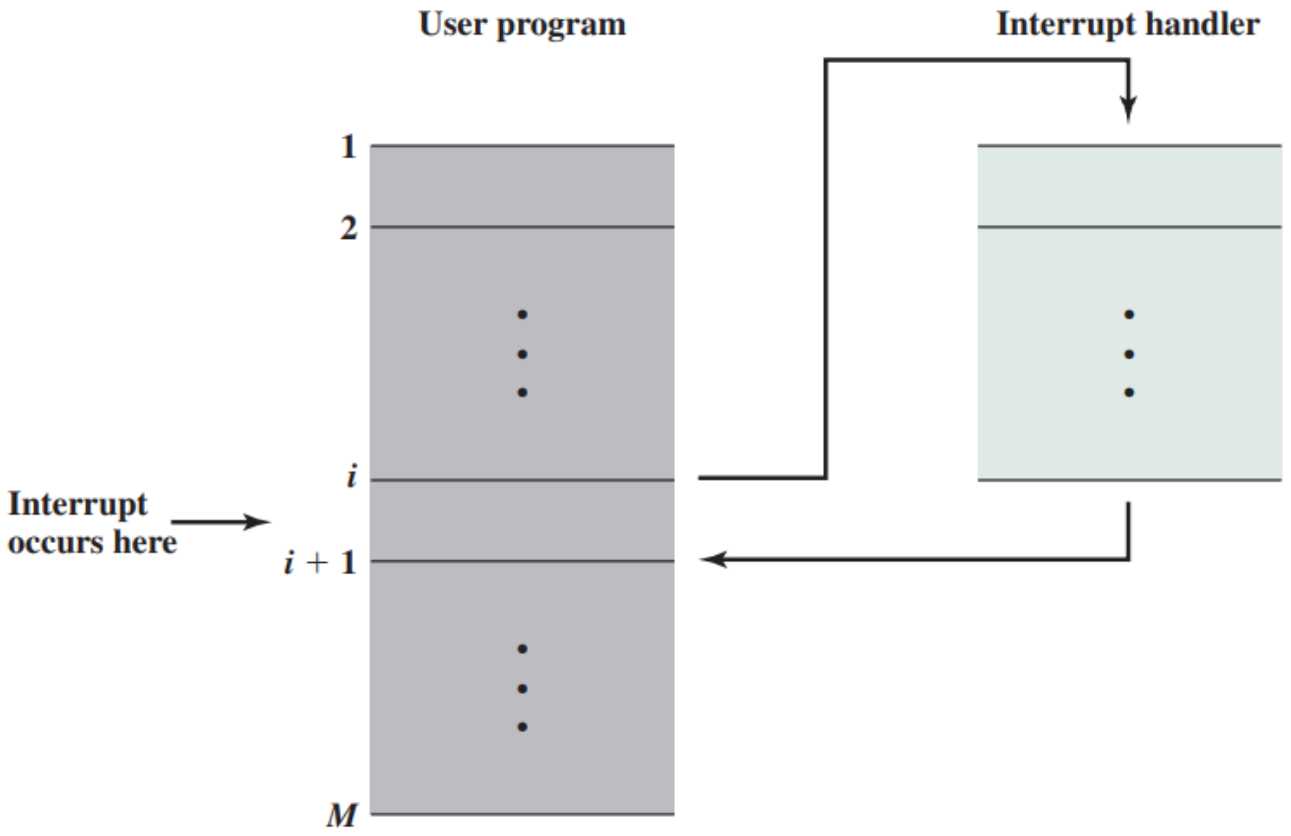
(a) No interrupts (b) Interrupts; short I/O wait (c) Interrupts; long I/O wait

= interrupt occurs during course of execution of user program

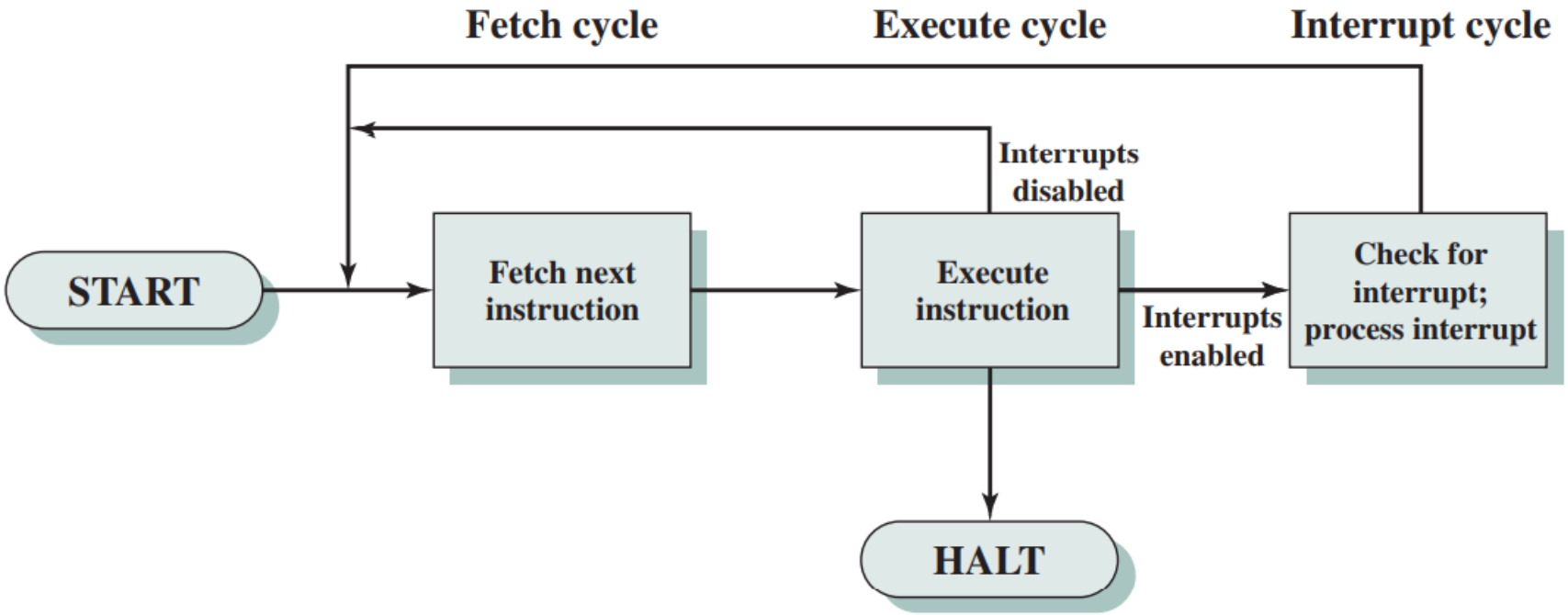
Interrupt Cycle

- Added to instruction cycle
- Processor checks for interrupt
  - Indicated by an interrupt signal
- If no interrupt, fetch next instruction
- If interrupt pending:
  - Suspend execution of current program
  - Save context
  - Set PC to start address of interrupt handler routine
  - Process interrupt
  - Restore context and continue interrupted program

Transfer of Control via Interrupts



Instruction Cycle with Interrupts



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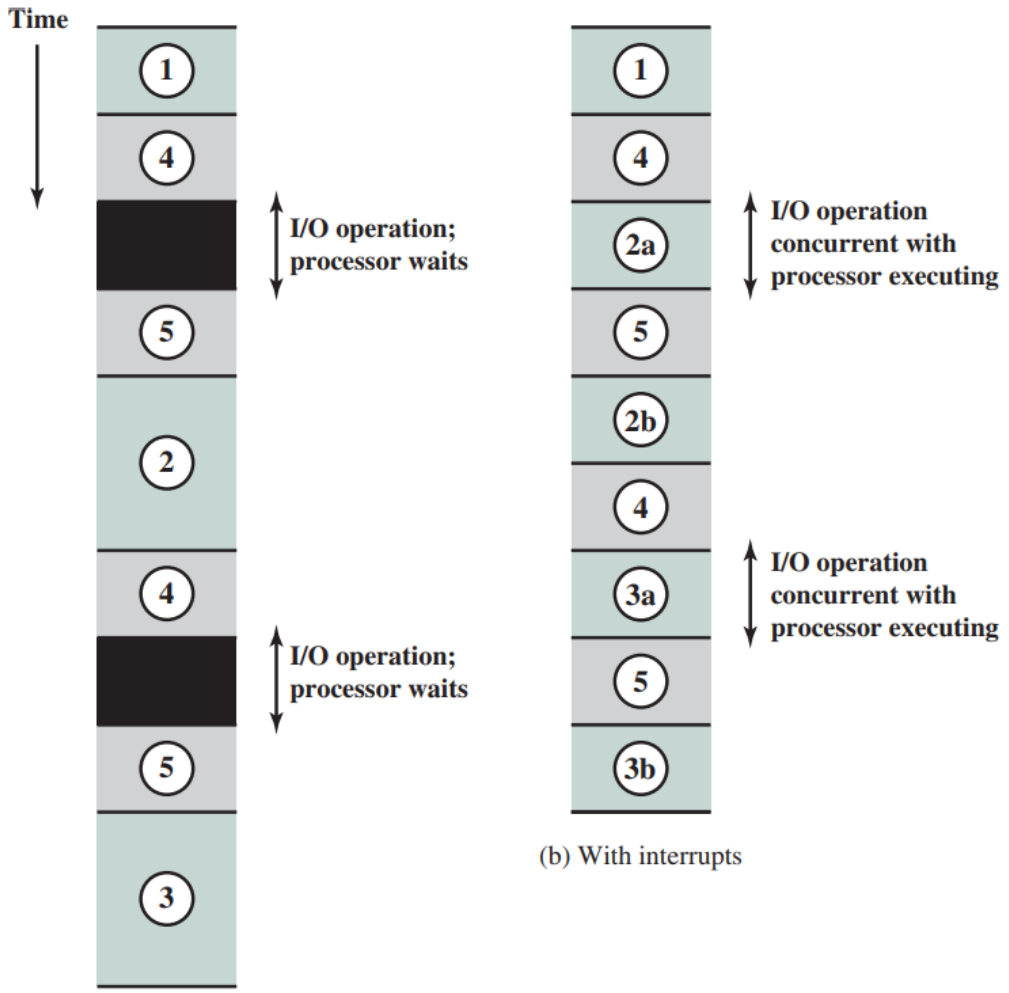
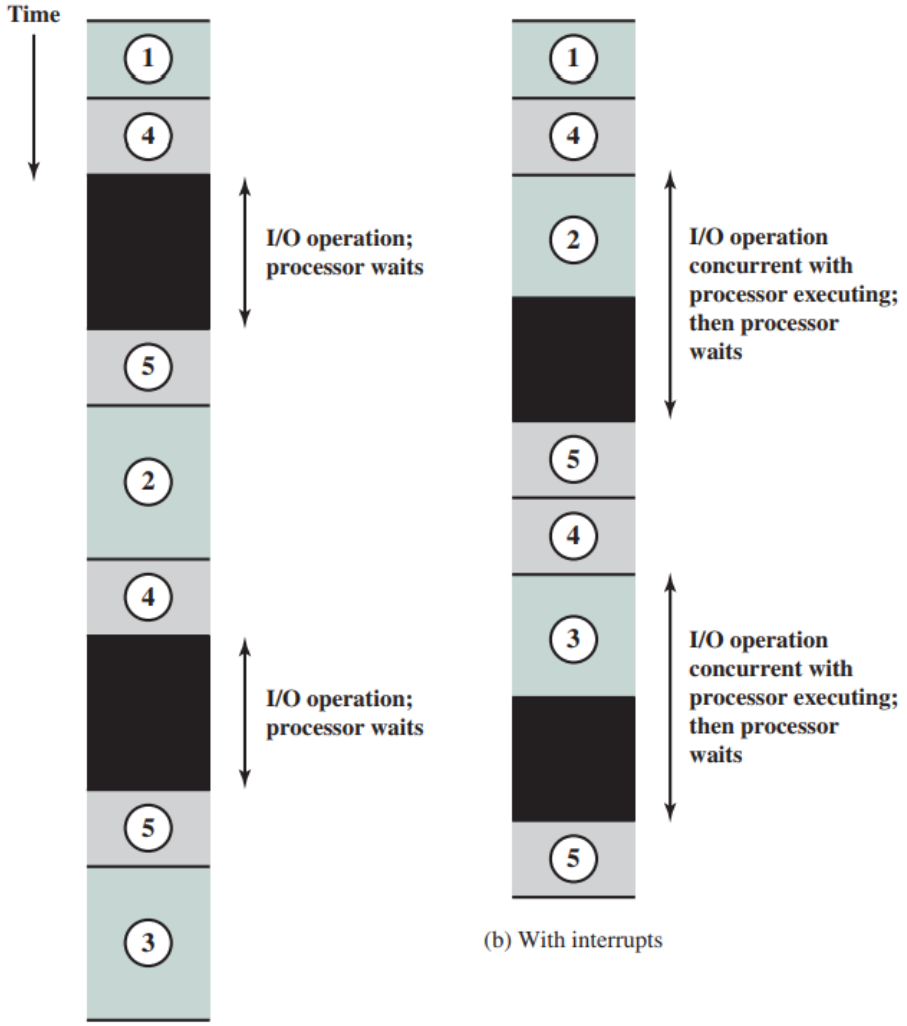
Program Timing Short I/O Wait



(a) Without interrupts

(b) With interrupts

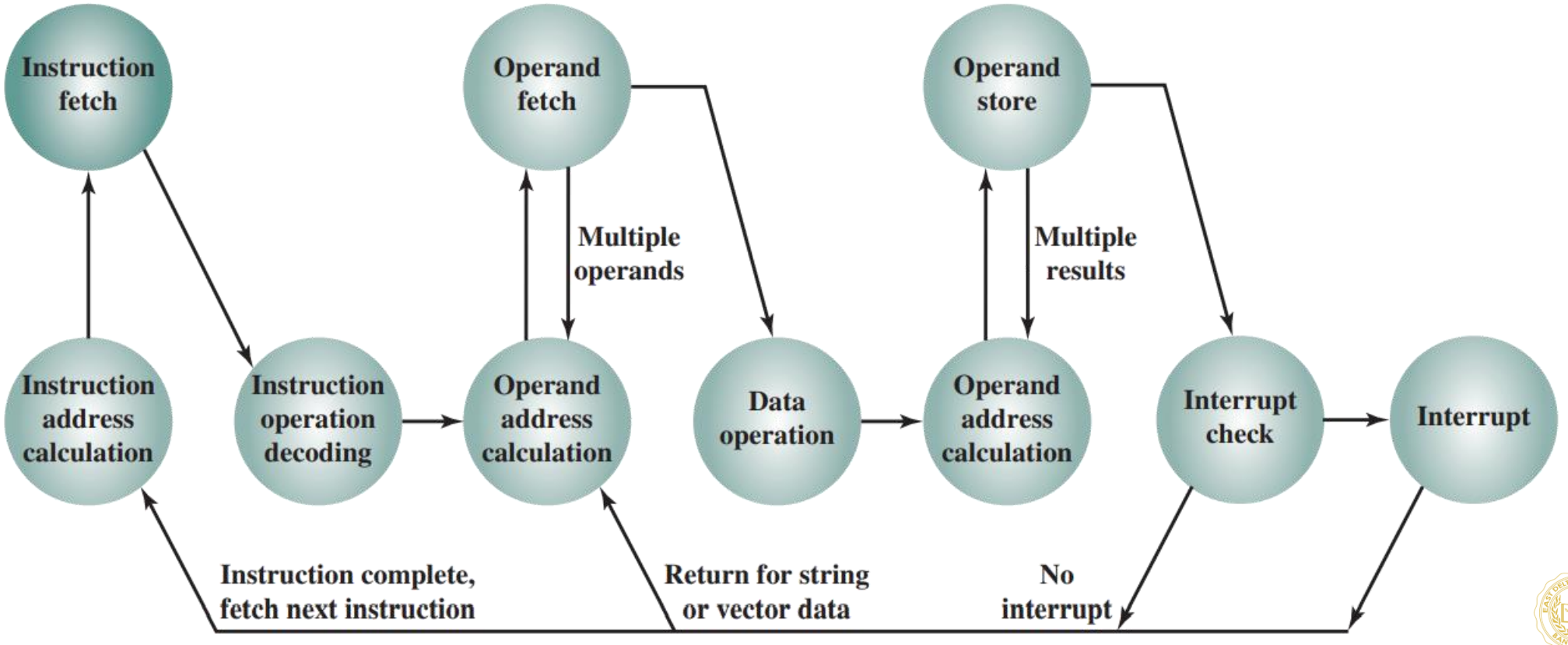
Program Timing Long I/O Wait



(a) Without interrupts

(b) With interrupts

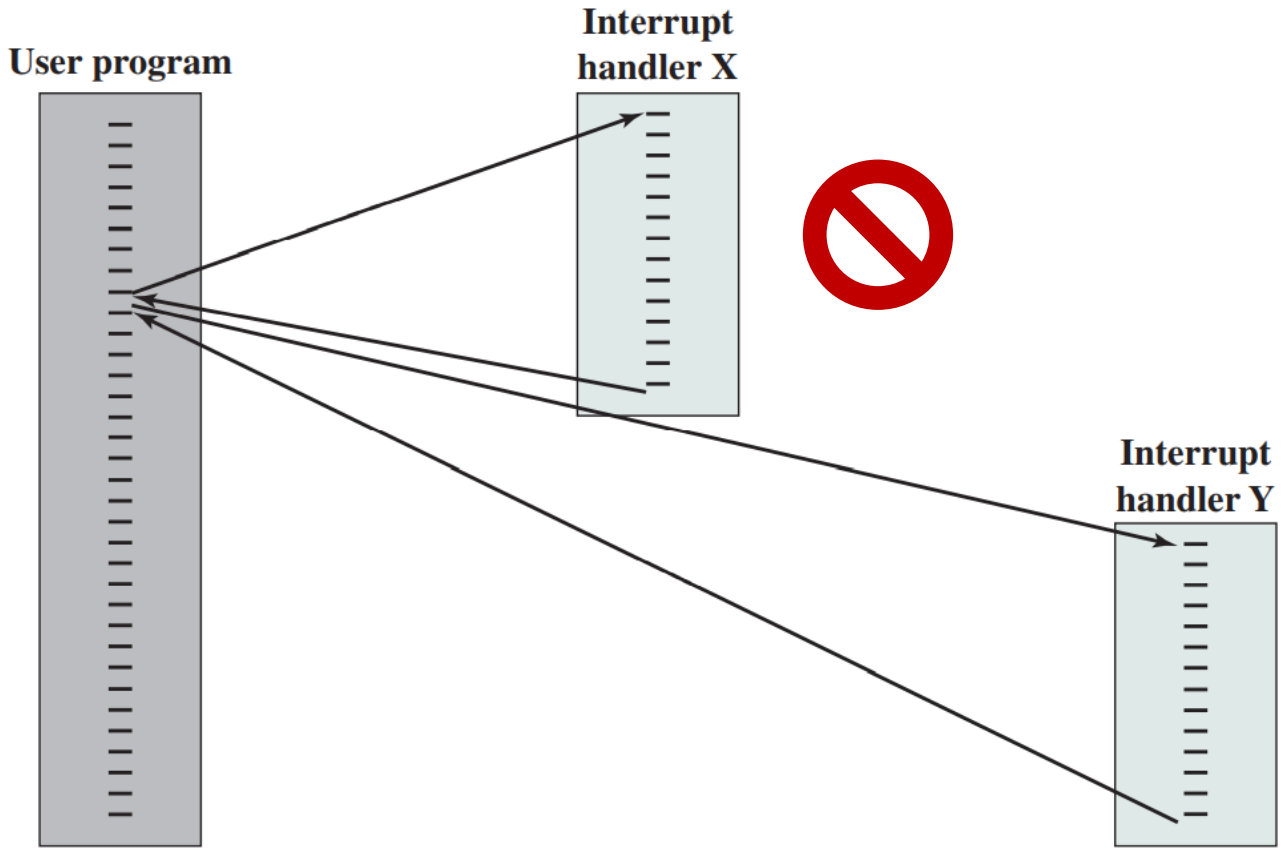
Instruction Cycle (with Interrupts) - State Diagram



Multiple Interrupts

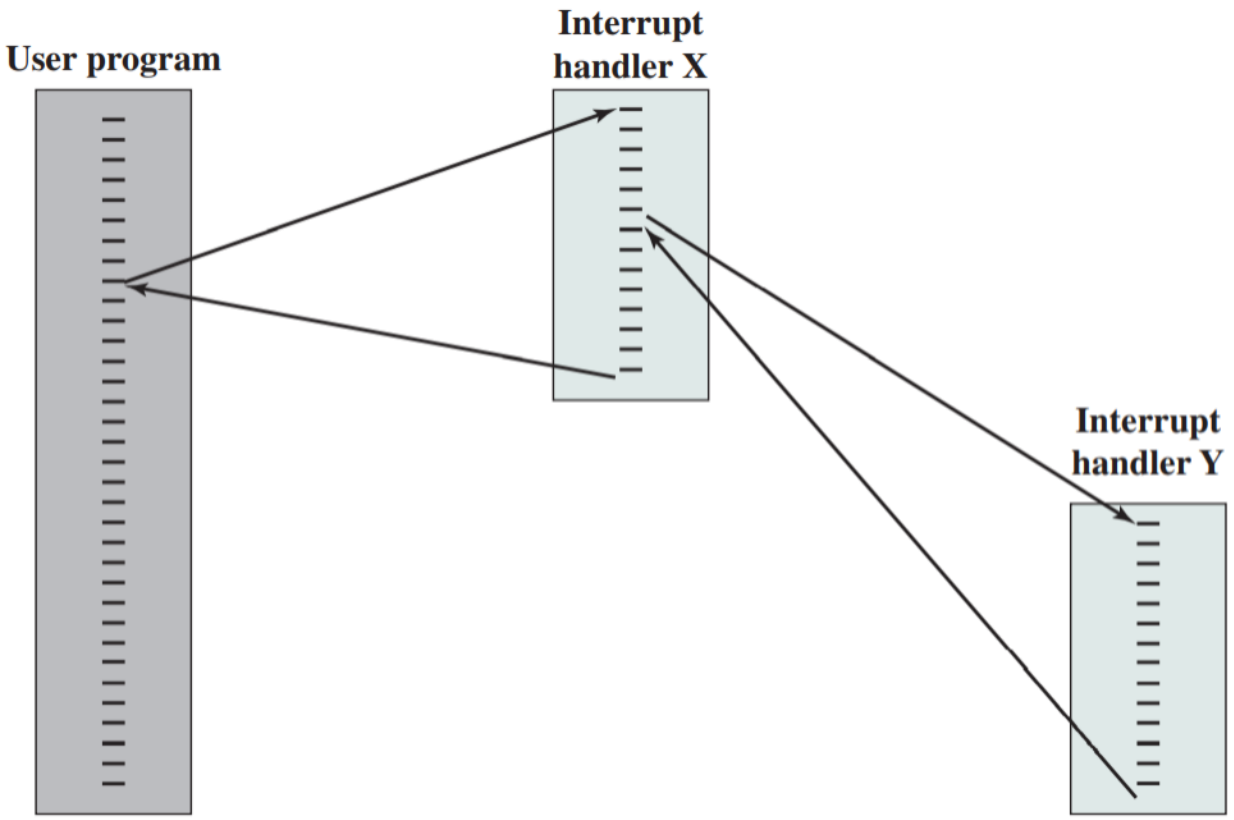
- Disable interrupts
  - Processor will ignore further interrupts whilst processing one interrupt
  - Interrupts remain pending and are checked after first interrupt has been processed
  - Interrupts handled in sequence as they occur
- Define priorities
  - Low priority interrupts can be interrupted by higher priority interrupts
  - When higher priority interrupt has been processed, processor returns to previous interrupt

Multiple Interrupts - Sequential



(a) Sequential interrupt processing

Multiple Interrupts – Nested



(b) Nested interrupt processing

Time Sequence of Multiple Interrupts