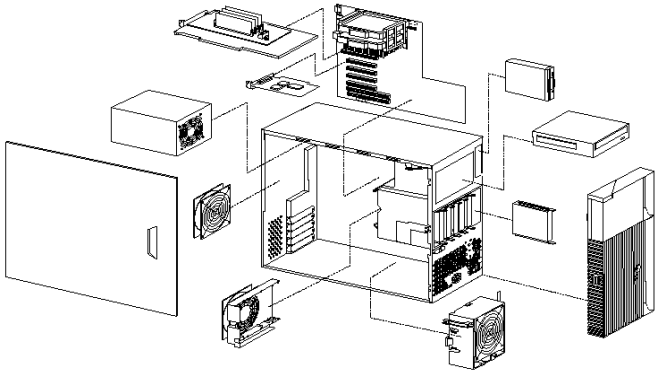
Department of Computer Science and Engineering
School of Science, Engineering & Technology



CSE 317: Computer Organization & Architecture

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Topic 7 – Internal Memory

- Memory Cell Operation
- Dynamic RAM (DRAM)
- Static RAM Structure (SRAM)
- Flash Memory

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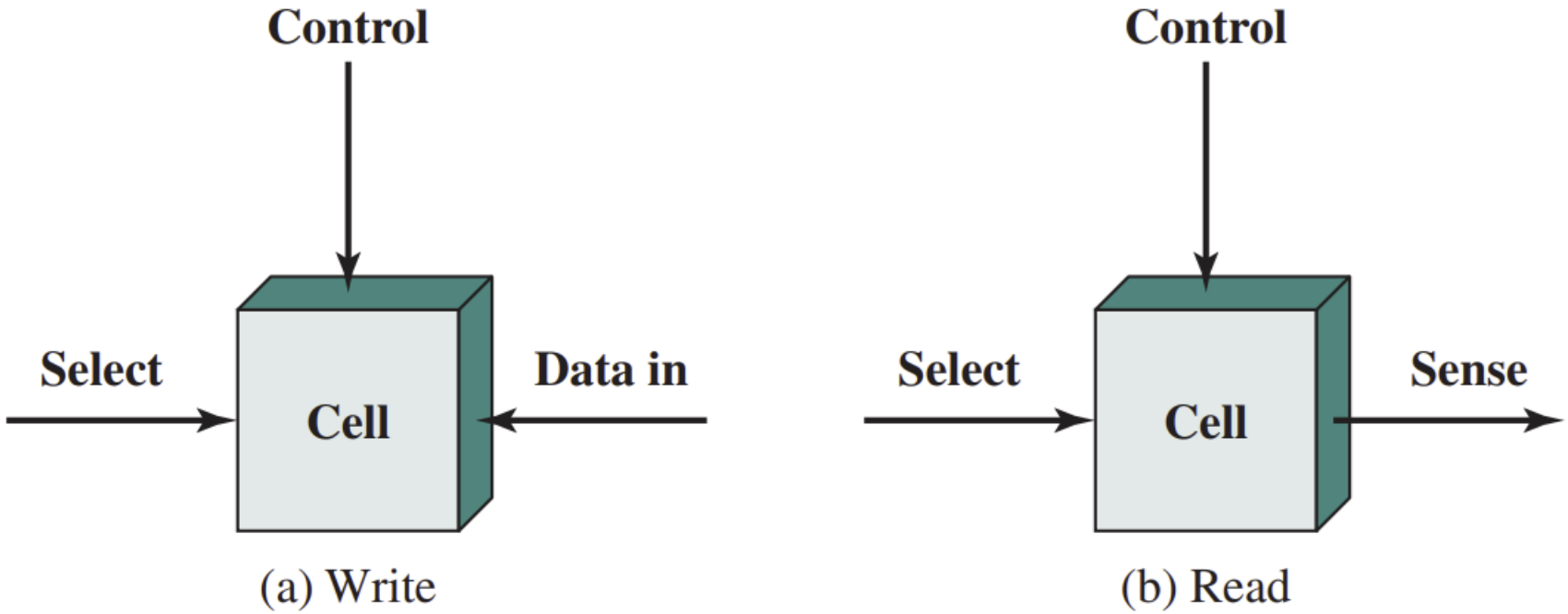
Memory Cell Operation



Semiconductor Memory Types

Topics

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

RAM Technology

RAM technology is divided into two technologies:

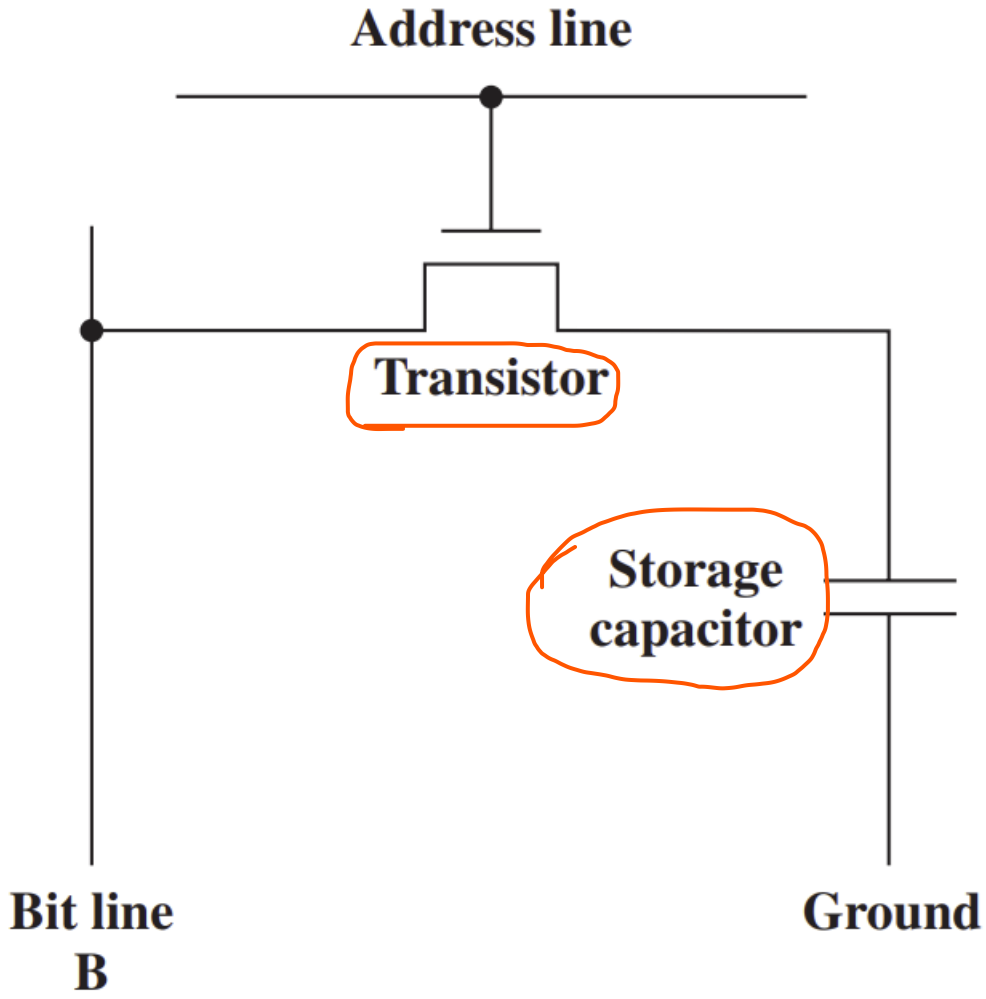
- Dynamic RAM (DRAM)
- Static RAM (SRAM)

* RAM is volatile memory, which means that the information temporarily stored in the module is erased when you restart or shut down your computer.

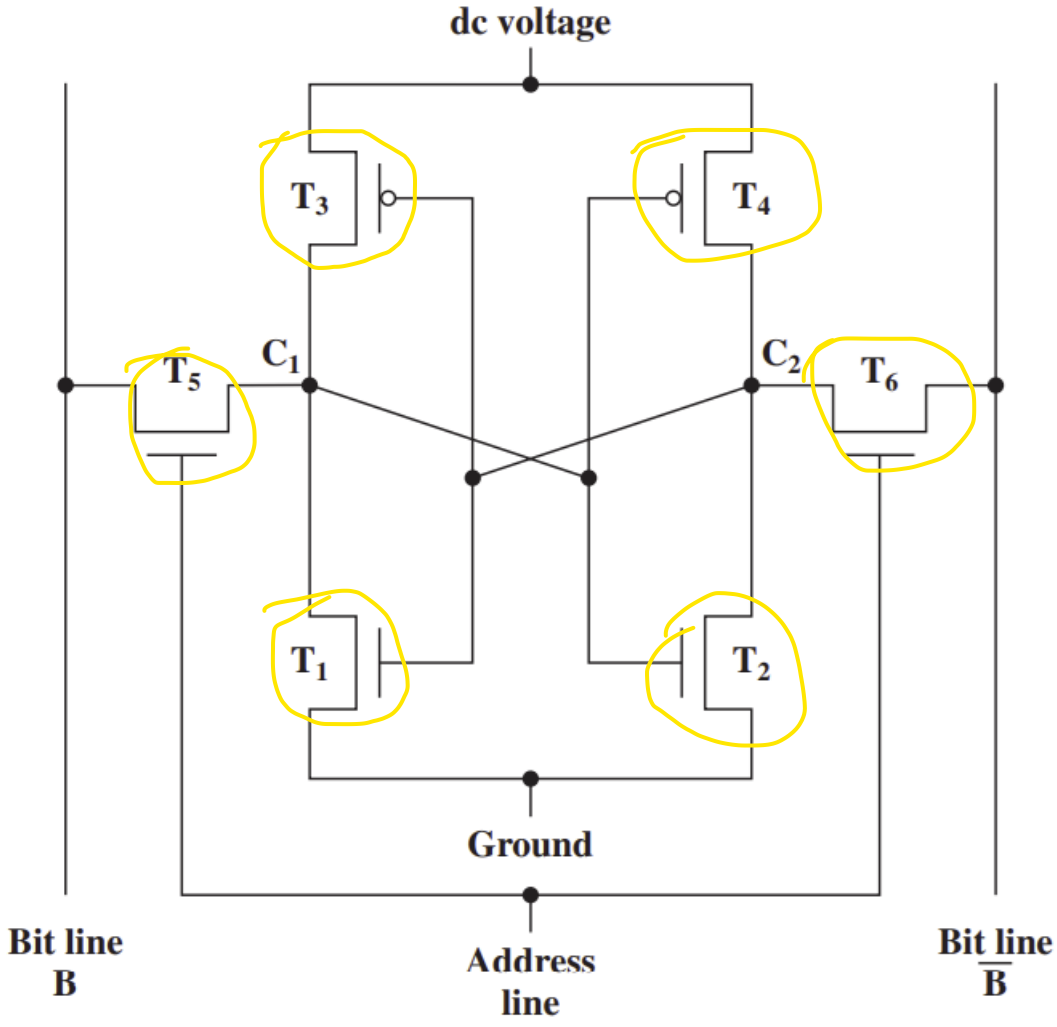
Dynamic RAM (DRAM)

- Made with cells that store data as charge on capacitors
- Presence or absence of charge in a capacitor is interpreted as a binary 1 or 0
- Requires periodic charge refreshing to maintain data storage
- The term dynamic refers to tendency of the stored charge to leak away, even with power continuously applied

Dynamic RAM Structure



Static RAM Structure



C1 – High
T2, T3: Active
T1, T4: Deactive

C2 – High
T2, T3: Deactive
T1, T4: Active

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SRAM versus DRAM

Both volatile

- Power must be continuously supplied to the memory to preserve the bit values

Dynamic cell

- Simpler to build, smaller
- More dense (smaller cells = more cells per unit area)
- 1 transistors for storing 1 bit
- Less expensive
- Requires the supporting refresh circuitry
- Tend to be favored for large memory requirements
- Used for main memory

Static

- Faster
- 6 transistors for storing 1 bit
- Used for cache memory (both on and off chip)

Read Only Memory (ROM)

* Non-Volatile

- Contains a permanent pattern of data that cannot be changed or added to
- No power source is required to maintain the bit values in memory
- Data or program is permanently in main memory and never needs to be loaded from a secondary storage device
- Data is actually wired into the chip as part of the fabrication process.
- No room for error, if one bit is wrong the whole batch of ROMs must be thrown out.
- Data insertion step includes a relatively large fixed cost.

ROM (read-only memory) is a non-volatile memory type. This means it receives data and permanently writes it on a chip, and it lasts even after you turn off your computer.

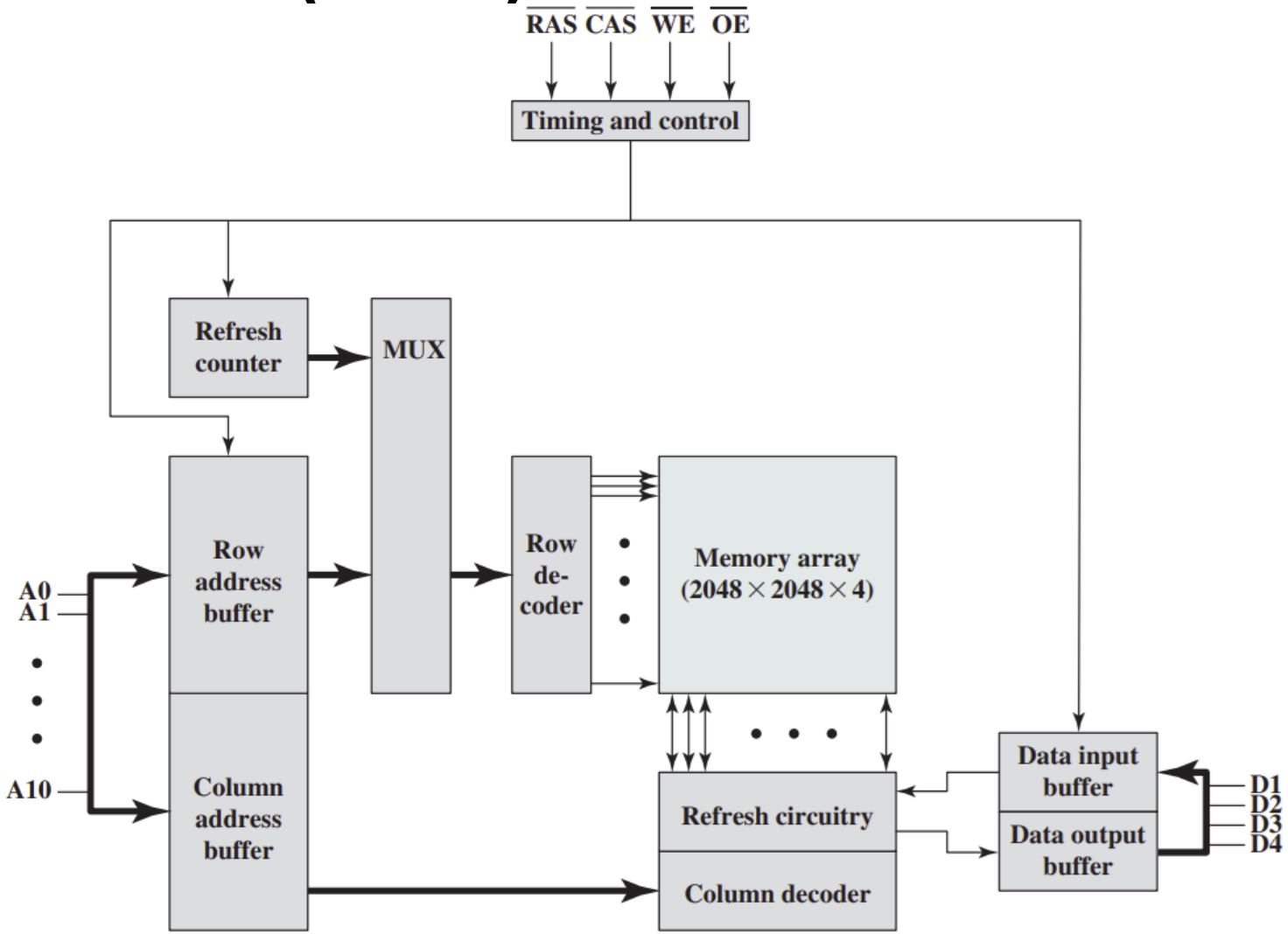
Programmable ROM (PROM)

- Less expensive alternative.
- Nonvolatile and may be written into only once.
- Writing process is performed electrically and may be performed by supplier or customer at a time later than the original chip fabrication.
- Special equipment is required for the writing process.
- Provides flexibility and convenience.
- Attractive for high volume production runs.

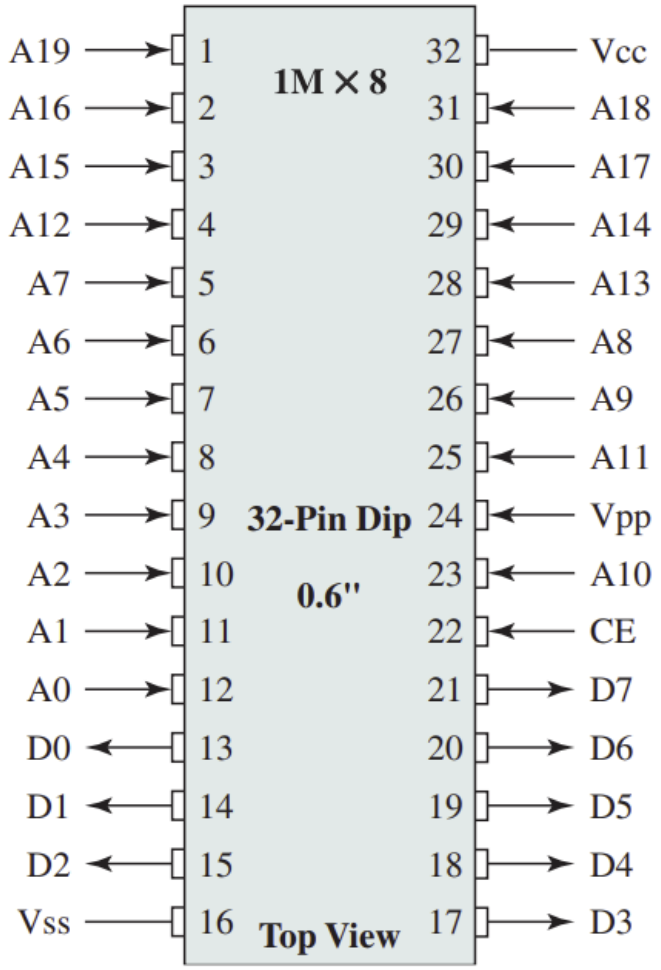
Read-Mostly Memory

EPROM	EEPROM	Flash Memory
Erasable programmable read-only memory	Electrically erasable programmable read-only memory	Intermediate between EPROM and EEPROM in both cost and functionality
Erasure process can be performed repeatedly	Can be written into at any time without erasing prior contents	Uses an electrical erasing technology, does not provide byte-level erasure
More expensive than PROM but it has the advantage of the multiple update capability	Combines the advantage of non-volatility with the flexibility of being updatable in place	Microchip is organized so that a section of memory cells are erased in a single action or “flash”
	More expensive than EPROM	

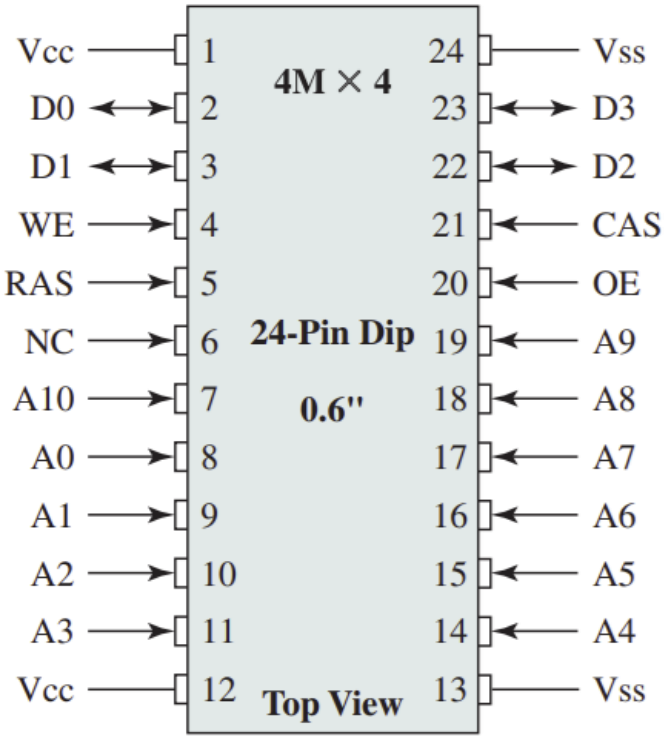
Typical 16 Mb DRAM (4M x 4)



Chip Packaging



(a) 8-Mbit EPROM



(b) 16-Mbit DRAM

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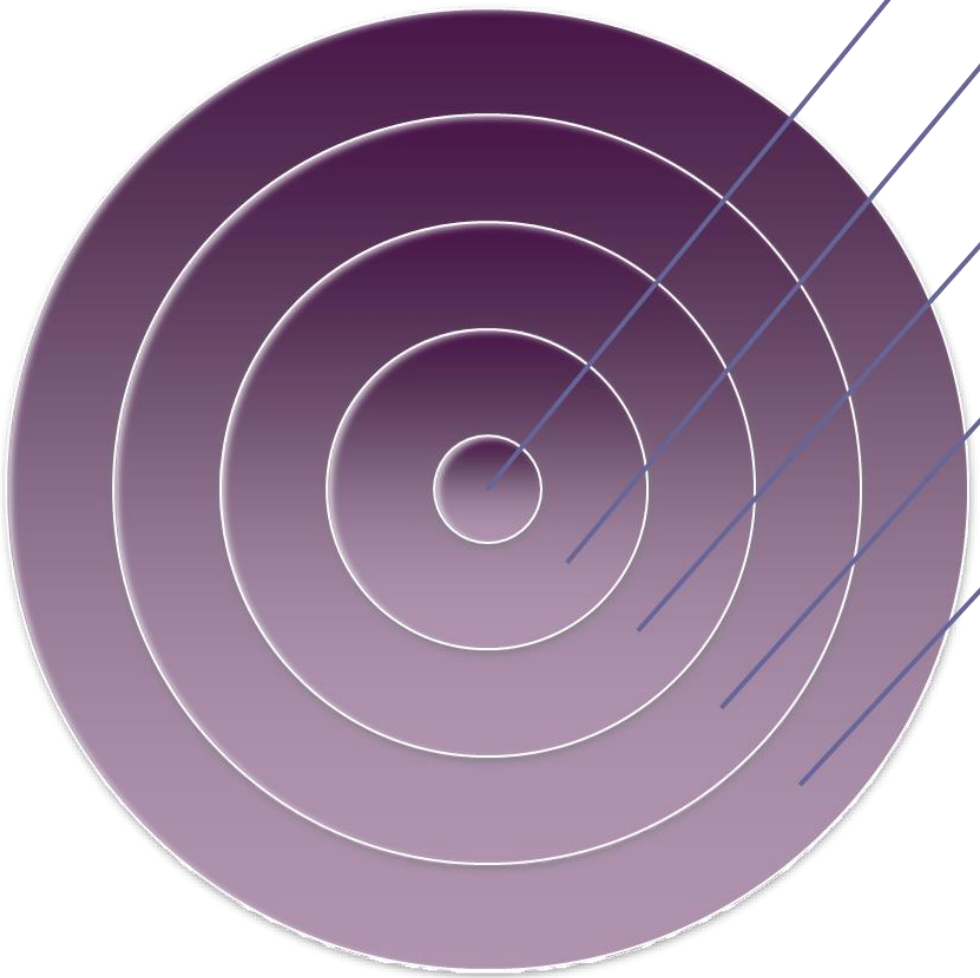
Interleaved Memory



Composed of a collection of DRAM chips

Grouped together to form a *memory bank*

Each bank is independently able to service a memory read or write request

K banks can service *K* requests simultaneously, increasing memory read or write rates by a factor of *K*

If consecutive words of memory are stored in different banks, the transfer of a block of memory is speeded up

Let’s Watch :

https://www.youtube.com/watch?v=0rNEtAz3wJQ

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Error Correction

Hard Failure

- Permanent physical defect
- Memory cell or cells affected cannot reliably store data but become
- stuck at 0 or 1 or switch erratically between 0 and 1
- Can be caused by:
- Harsh environmental abuse
- Manufacturing defects
- Wear

Soft Error

- Random, non-destructive event that alters the contents of one or more memory cells
- No permanent damage to memory
- Can be caused by:
- Power supply problems
- Alpha particles

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Error Correction

- When data are to be written into memory, a calculation, depicted as a function f, is performed on the data to produce a code. Both the code and the data are stored.

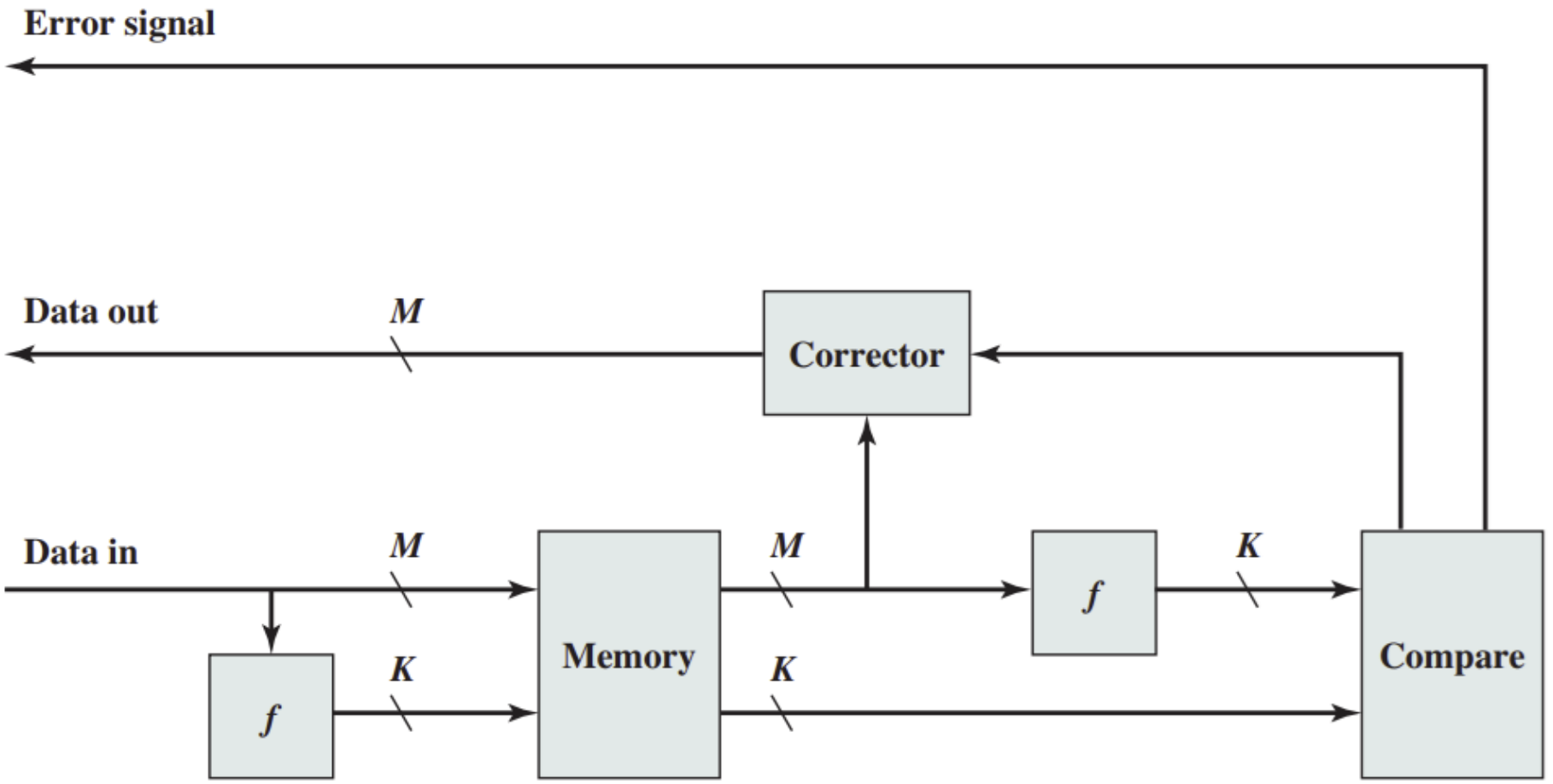
- Thus, if an M-bit word of data is to be stored and the code is of length K bits, then the actual size of the stored word is M + K bits.

- When the previously stored word is read out, the code is used to detect and possibly correct errors.

- A new set of K code bits is generated from the M data bits and compared with the fetched code bits. The comparison yields one of three results:

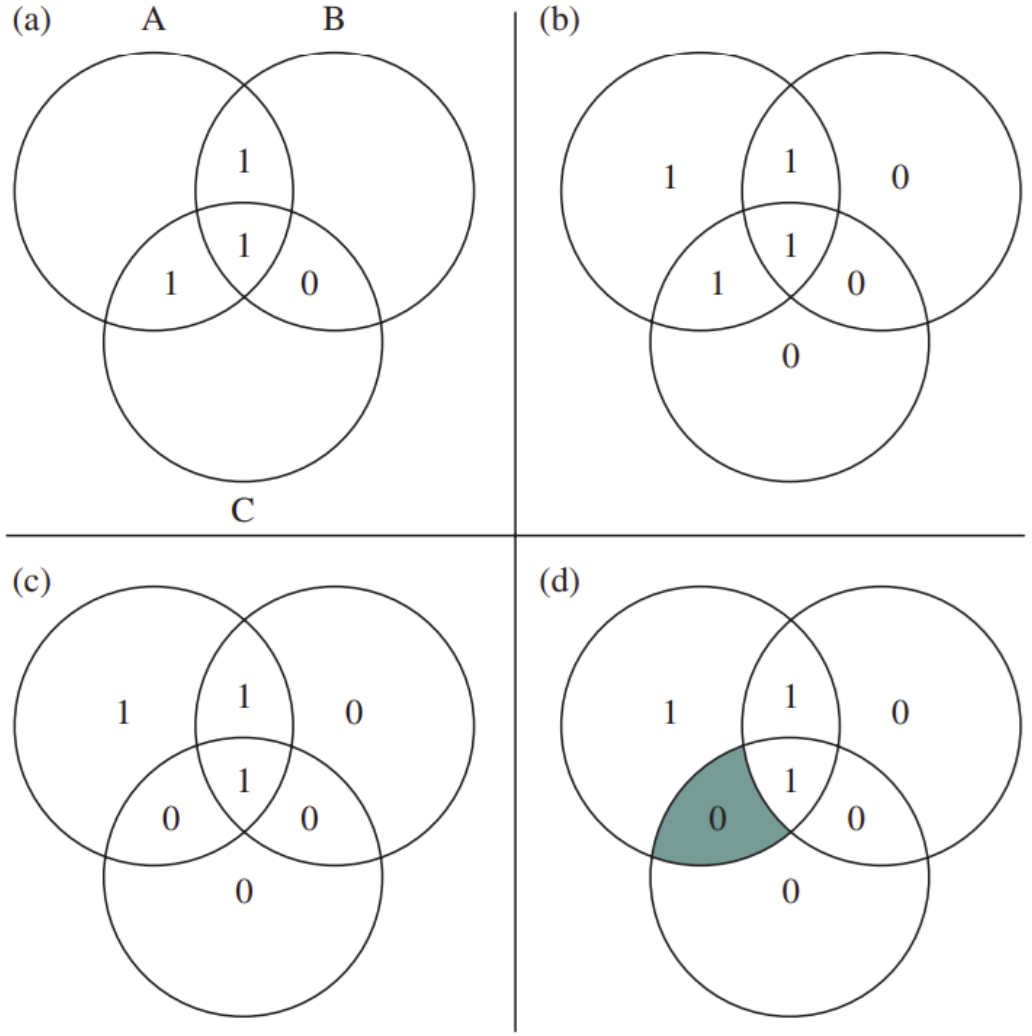
  - No errors are detected. The fetched data bits are sent out.
  - An error is detected, and it is possible to correct the error. The data bits plus error correction bits are fed into a corrector, which produces a corrected set of M bits to be sent out.
  - An error is detected, but it is not possible to correct it. This condition is reported

Error Correcting Code Function



Hamming Error Correcting Code

* Van Diagram



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Layout of Data Bits and Check Bits

Bit position	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check bit					C8				C4		C2	C1

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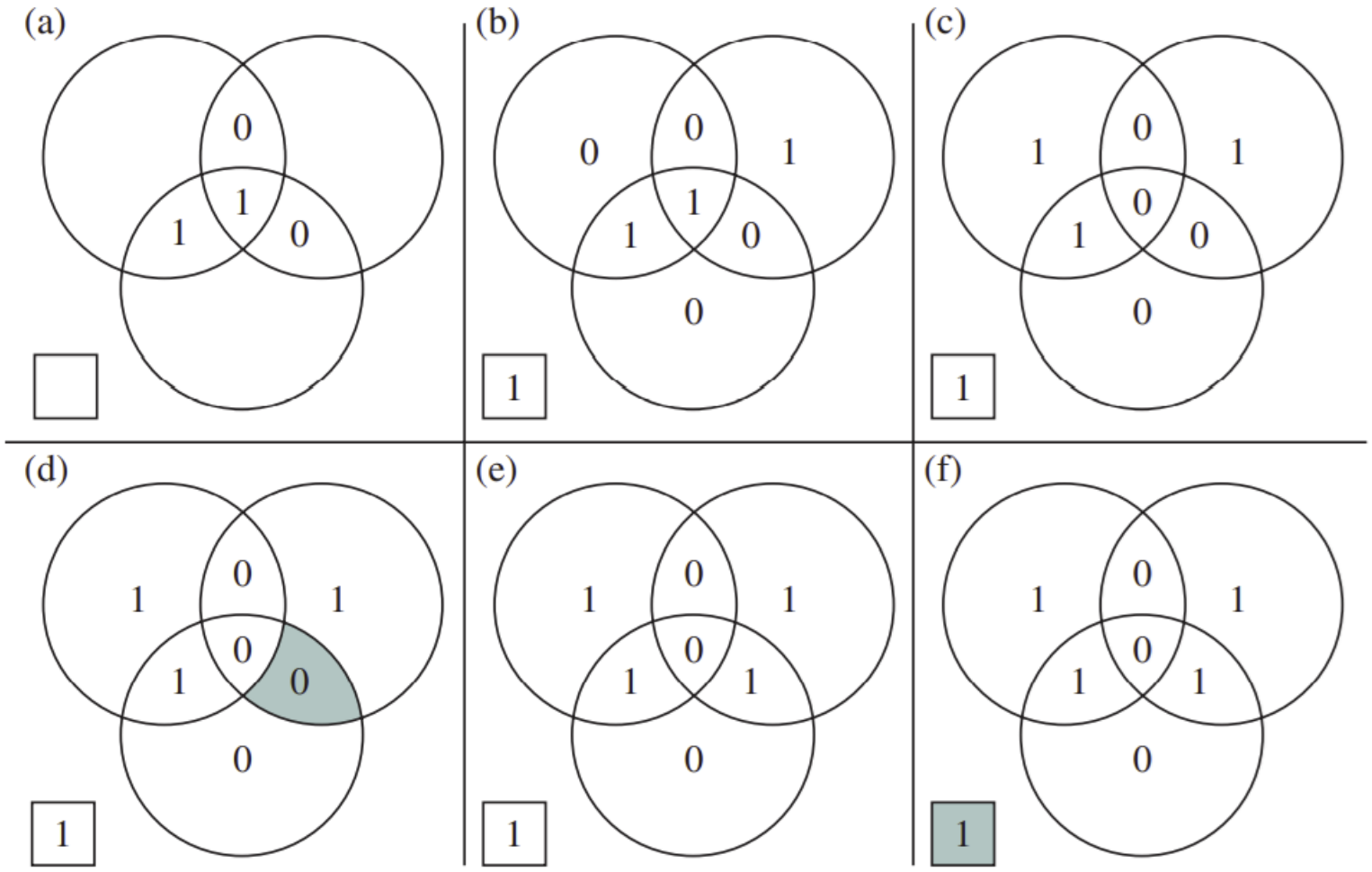
Hamming SEC-DED Code



Advanced DRAM Organization

- One of the most critical system bottlenecks when using high-performance processors is the interface to main internal memory.

- The traditional DRAM chip is constrained both by its internal architecture and by its interface to the processor's memory bus.

- A number of enhancements to the basic DRAM architecture have been explored:

	Clock Frequency (MHz)	Transfer Rate (GB/s)	Access Time (ns)	Pin Count
SDRAM	166	1.3	18	168
DDR	200	3.2	12.5	184
RDRAM	600	4.8	12	162

Synchronous DRAM (SDRAM)

One of the most widely used forms of DRAM

⬇

Exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states

⬇

With synchronous access the DRAM moves data in and out under control of the system clock. The processor or other master issues the instruction and address information which is latched by the DRAM. The DRAM then responds after a set number of clock cycles. Meanwhile the master can safely do other tasks while the SDRAM is processing.

Flash Memory

- Another form of semiconductor memory is flash memory.
- Flash memory is used both for internal memory and external memory applications.
- An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM. In addition, it is possible to erase just blocks of memory rather than an entire chip.

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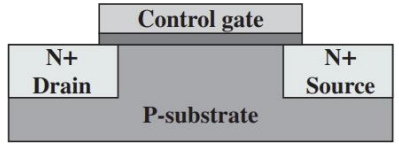
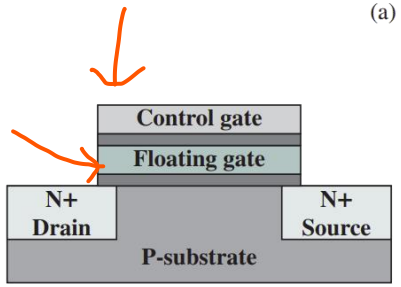
Flash Memory

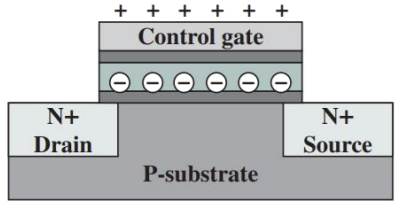
- In a flash memory cell, a second gate—called a floating gate, because it is insulated by a thin oxide layer—is added to the transistor.
- Initially, the floating gate does not interfere with the operation of the transistor (Figure b).
- In this state, the cell is deemed to represent binary 1. Applying a large voltage across the oxide layer causes electrons to tunnel through it and become trapped on the floating gate, where they remain even if the power is disconnected (Figure c).
- In this state, the cell is deemed to represent binary 0. The state of the cell can be read by using external circuitry to test whether the transistor is working or not. Applying a large voltage in the opposite direction removes the electrons from the floating gate, returning to a state of binary 1.



(a) Transistor structure



(b) Flash memory cell in one state



(c) Flash memory cell in zero state