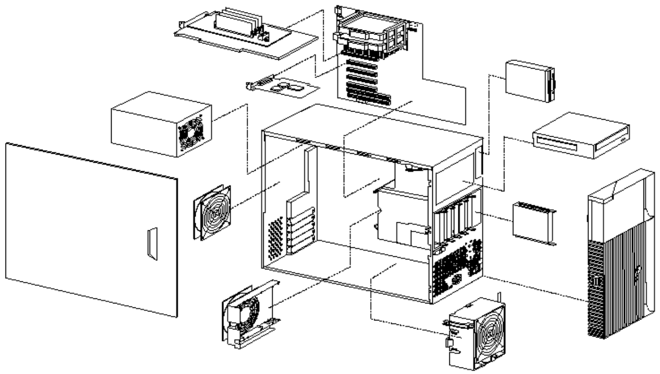
EDU
EAST DELTA UNIVERSITY

Department of Computer Science and Engineering
School of Science, Engineering & Technology



CSE 317: Computer Organization & Architecture

Wahidul Alam, Lecturer, CSE, SoSET, EDU

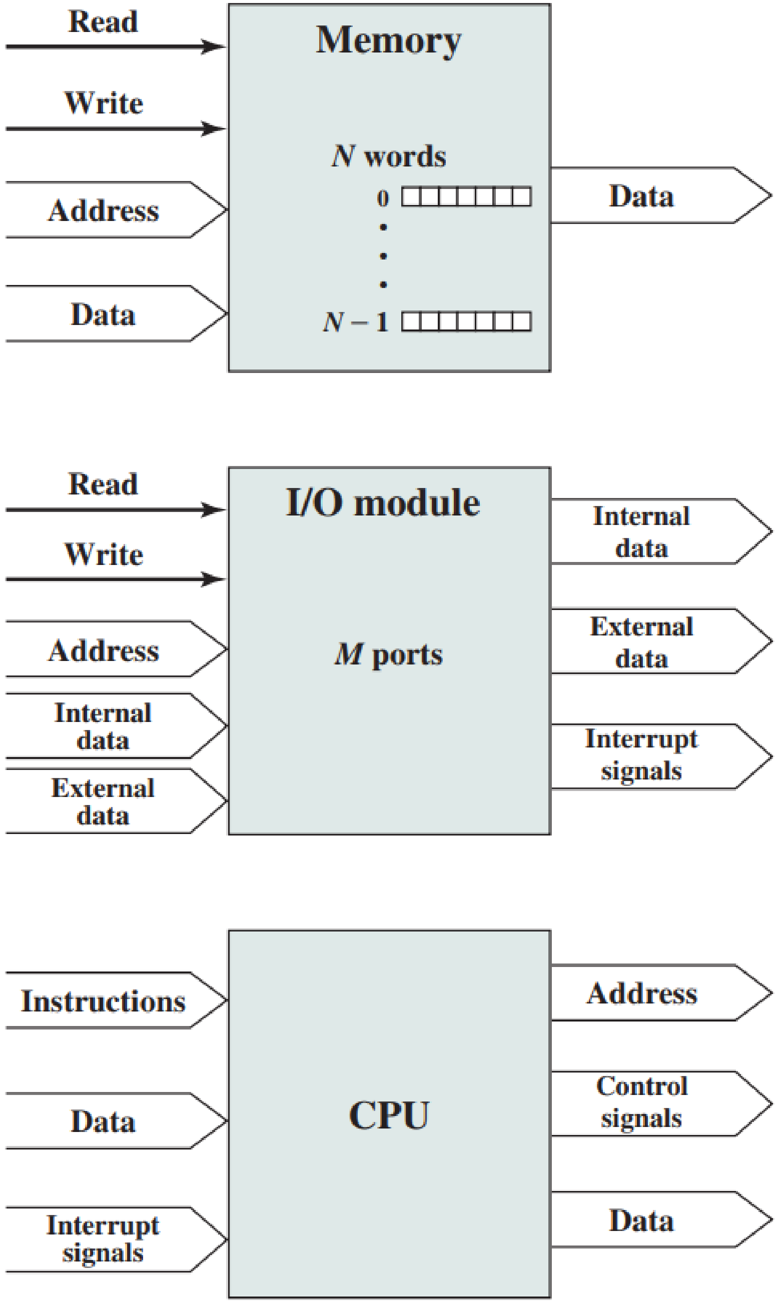
Topic 5 – Bus

- Bus
- Data, Address, Control Buses
- Quick Path Interconnect (QPI)
- Peripheral Component Interconnect (PCI)

Connecting

- All the units must be connected
- Different type of connection for different type of unit
    - Memory
    - Input/Output
    - CPU

Computer Modules



Memory Connection

- Typically, a memory module will consist of *N words of equal length.*

- Each word is assigned a unique numerical address (0, 1, …, *N - 1).*

- *A word of* data can be read from or written into the memory. The nature of the operation is indicated by read and write control signals. The location for the operation is specified by an address.

Input/Output Connection

- From an internal (to the computer system) point of view, I/O is functionally similar to memory. There are two operations, read and write.

- Further, an I/O module may control more than one external device. We can refer to each of the interfaces to an external device as a *port and give each* a unique address (e.g., 0, 1, ..., *M - 1).*

- *In addition, there are external data* paths for the input and output of data with an external device.

CPU Connection

The processor reads in instructions and data, writes out data after processing, and uses control signals to control the overall operation of the system. It also receives interrupt signals.

The interconnection structure must support the following types of transfers:

- **Memory to processor:** The processor reads an instruction or a unit of data from memory.
- **Processor to memory:** The processor writes a unit of data to memory.
- **I/O to processor:** The processor reads data from an I/O device via an I/O module.
- **Processor to I/O:** The processor sends data to the I/O device.
- **I/O to or from memory:** For these two cases, an I/O module is allowed to exchange data directly with memory, without going through the processor, using direct memory access (DMA).

Buses

- There are a number of possible interconnection systems.
- Single and multiple BUS structures are most common –
  - e.g. Control/Address/Data bus (PC)
  - e.g. Unibus (DEC-PDP)

Concepts of Buses:
- A Collection of Wires through which data is transmitted from one part of a Computer to another is known as Bus.
- A bus as a highway on which data travels within a computer.
- It connects all the internal Computer components to CPU and main memory.

* Three types of Bus:
1) Data Bus
2) Address Bus
3) Control Bus

What is a Bus?

- A communication pathway connecting two or more devices
- Usually broadcast
- Often grouped
  - A number of channels in one bus
  - e.g. 32 bit data bus is 32 separate single bit channels

1

Data Bus

- The data lines provide a path for moving data among system modules. These lines, collectively, are called the data bus.

- The data bus may consist of 32, 64, 128, or even more separate lines, the number of lines being referred to as the *width of the* data bus. Because each line can carry only 1 bit at a time, the number of lines determines how many bits can be transferred at a time.

- The width of the data bus is a key factor in determining overall system performance. For example, if the data bus is 32 bits wide and each instruction is 64 bits long, then the processor must access the memory module twice during each instruction cycle.

2

Address bus

- The address lines are used to designate the source or destination of the data on the data bus. For example, if the processor wishes to read a word (8, 16, or 32 bits) of data from memory, it puts the address of the desired word on the address lines.

- Furthermore, the address lines are generally also used to address I/O ports. Typically, the higher-order bits are used to select a particular module on the bus, and the lower-order bits select a memory location or I/O port within the module. For example, on an 8-bit address bus, address 01111111 and below might reference locations in a memory module (module 0) with 128 words of memory, and address 10000000 and above refer to devices attached to an I/O module (module 1).

3 Control Bus

- The control lines are used to control the access to and the use of the data and address lines.

- As the data and address lines are shared by all components, there must be a means of controlling their use. Control signals transmit both command and timing information among system modules.

- Timing signals indicate the validity of data and address information.

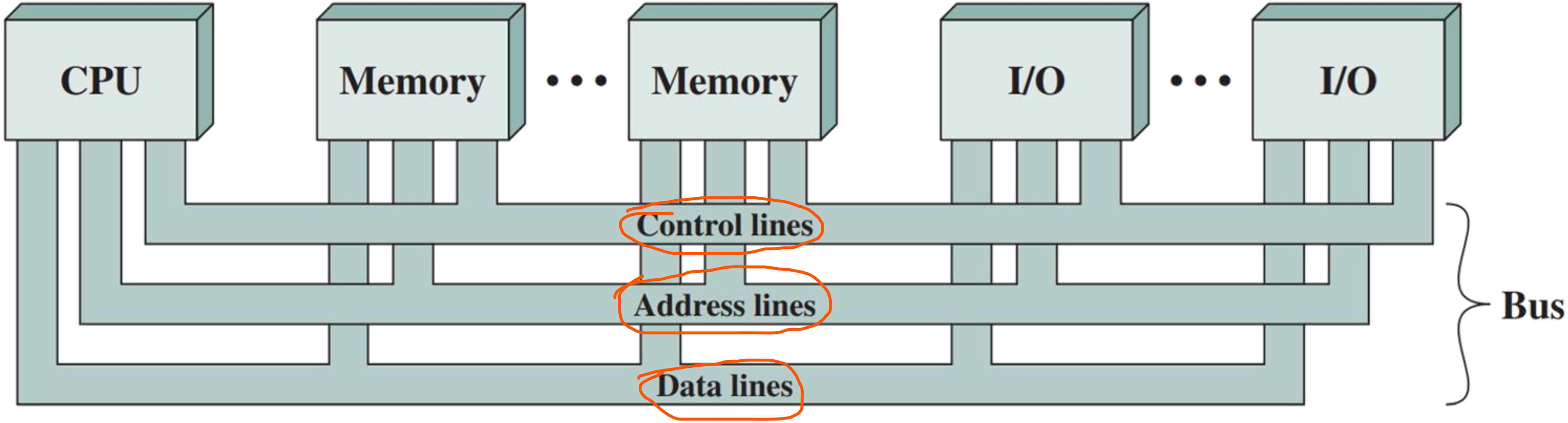
- Command signals specify operations to be performed.

Control Bus

Typical control lines include:

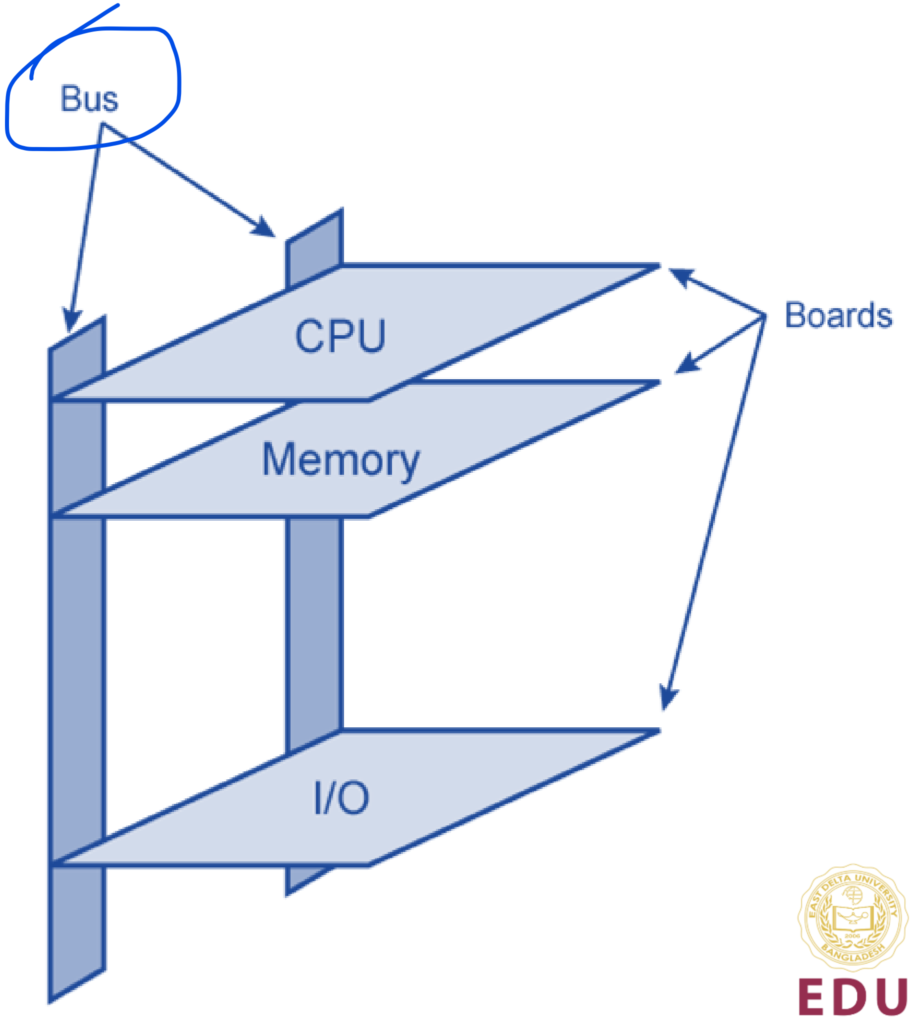
- Memory write: causes data on the bus to be written into the addressed location
- Memory read: causes data from the addressed location to be placed on the bus
- I/O write: causes data on the bus to be output to the addressed I/O port
- I/O read: causes data from the addressed I/O port to be placed on the bus
- Transfer ACK: indicates that data have been accepted from or placed on the bus
- Bus request: indicates that a module needs to gain control of the bus
- Bus grant: indicates that a requesting module has been granted control of the bus
- Interrupt request: indicates that an interrupt is pending
- Interrupt ACK: acknowledges that the pending interrupt has been recognized
- Clock: is used to synchronize operations
- Reset: initializes all modules.

Bus Interconnection Scheme



Physical Realization of Bus Architecture

- What do buses look like?
  - Parallel lines on circuit boards
  - Ribbon cables
  - Strip connectors on mother boards
    - e.g. PCI
  - Sets of wires



Single Bus Problems

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
    - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

Point to Point Interconnect

- Contemporary systems rely on point-to-point interconnection rather than shared buses.
- The principal reason driving the change from bus to point-to-point interconnect was the electrical constraints encountered with increasing the frequency of wide synchronous buses.
- At higher and higher data rates, it becomes increasingly difficult to perform the synchronization and arbitration functions in a timely fashion.
- Further, with the advent of multicore chips, with multiple processors and significant memory on a single chip, it was found that the use of a conventional shared bus on the same chip magnified the difficulties of increasing bus data rate and reducing bus latency to keep up with the processors.
- Compared to the shared bus, the point to point interconnect has lower latency, higher data rate, and better scalability.

Quick Path Interconnect (QPI)

Example of the point-to-point interconnect approach: Intel's Quick Path Interconnect (QPI), which was introduced in 2008. The following are significant characteristics of QPI and other point-to-point interconnect schemes:

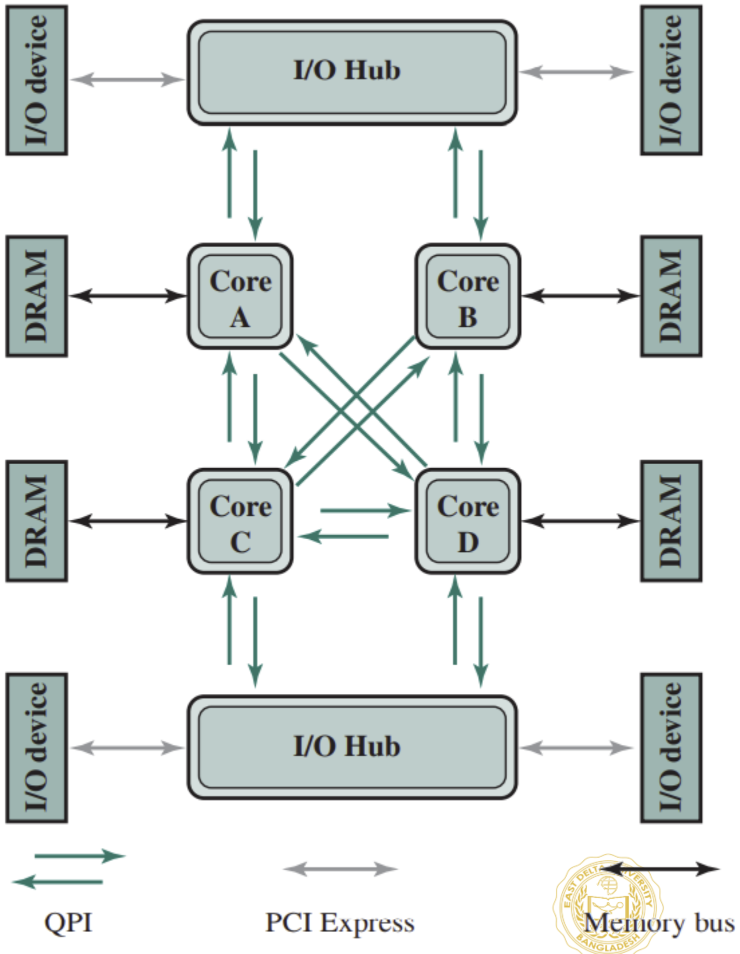
- **Multiple direct connections:** Multiple components within the system enjoy direct pairwise connections to other components. This eliminates the need for arbitration found in shared transmission systems.

- **Layered protocol architecture:** As found in network environments, such as TCP/IP-based data networks, these processor-level interconnects use a layered protocol architecture, rather than the simple use of control signals found in shared bus arrangements.

- **Packetized data transfer:** Data are not sent as a raw bit stream. Rather, data are sent as a sequence of packets, each of which includes control headers and error control codes.

Typical Use of QPI On A Multicore Computer

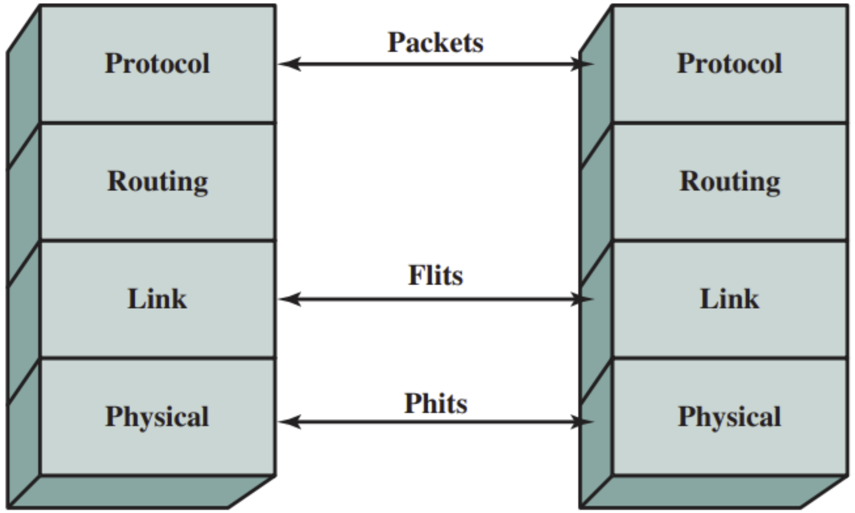
- The QPI links form a switching fabric that enables data to move throughout the network.
- Direct QPI connections can be established between each pair of core processors.
- If core A needs to access the memory controller in core D, it sends its request through either cores B or C, which must in turn forward that request on to the memory controller in core D.
- In addition, QPI is used to connect to an I/O module, called an I/O hub (IOH).
- The IOH acts as a switch directing traffic to and from I/O devices.
- A core also links to a main memory module (typically the memory uses dynamic access random memory (DRAM) technology) using a dedicated memory bus.



QPI Layers

QPI is defined as a four-layer protocol architecture

- **Physical:** Consists of the actual wires carrying the signals, as well as circuitry and logic to support features required in the transmission and receipt of the 1s and 0s. The unit of transfer at the Physical layer is 20 bits, which is called a Phit (physical unit).
- **Link:** Responsible for reliable transmission and flow control. The Link layer’s unit of transfer is an 80-bit Flit (flow control unit).
- **Routing:** Provides the framework for directing packets through the fabric.
- **Protocol:** The high-level set of rules for exchanging packets of data between devices. A packet is comprised of an integral number of Flits.



Peripheral Component Interconnect (PCI)

- The peripheral component interconnect (PCI) is a popular high-bandwidth, processor-independent bus that can function as a peripheral bus.

- Compared with other common bus specifications, PCI delivers better system performance for high-speed I/O subsystems (e.g., graphic display adapters, network interface controllers, and disk controllers).

- The bus-based PCI scheme has not been able to keep pace with the data rate demands of attached devices. Accordingly, a new version, known as PCI Express (PCIe) has been developed.

- A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices, such as Gigabit Ethernet. Another requirement deals with the need to support time-dependent data streams.

PCI Physical and Logical Architecture

- A root complex device, also referred to as a chipset or a host bridge, connects the processor and memory subsystem to the PCI Express switch fabric comprising one or more PCIe and PCIe switch devices.

- The root complex acts as a buffering device, to deal with difference in data rates between I/O controllers and memory and processor components.

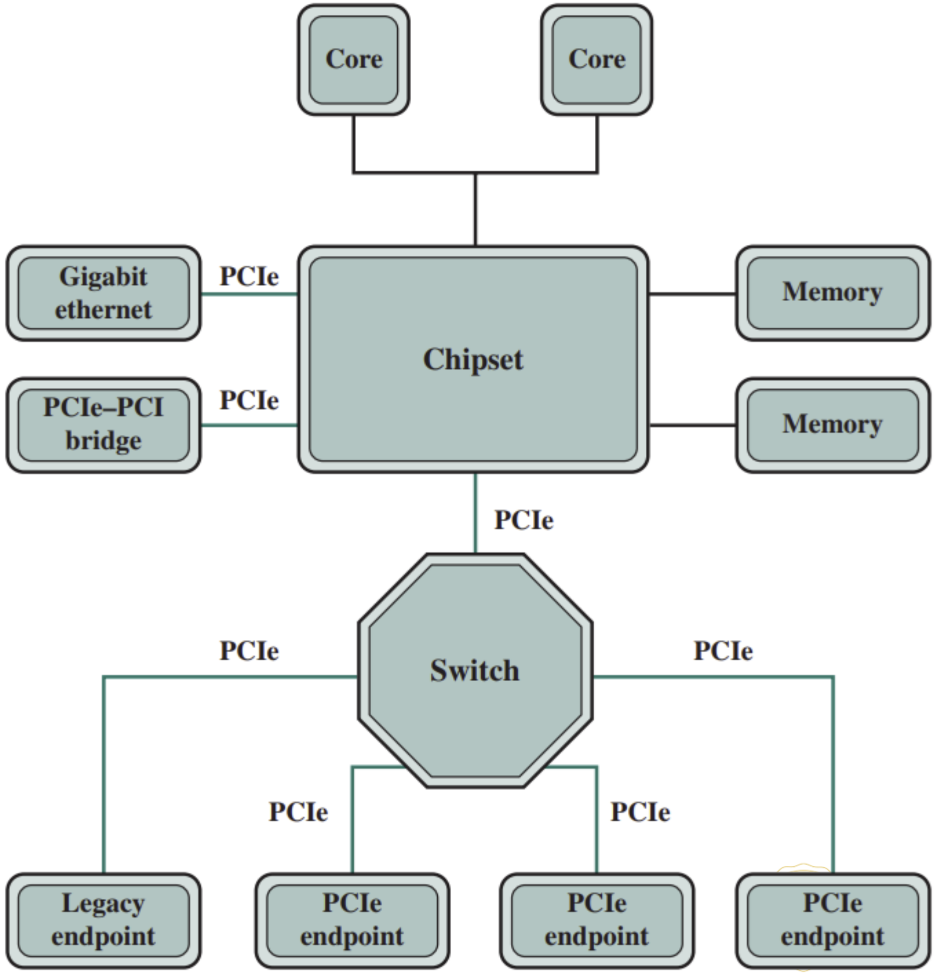
- The root complex also translates between PCIe transaction formats and the processor and memory signal and control requirements.

- The chipset will typically support multiple PCIe ports, some of which attach directly to a PCIe device, and one or more that attach to a switch that manages multiple PCIe streams.

PCI Physical and Logical Architecture

PCIe links from the chipset may attach to the following kinds of devices that implement PCIe:

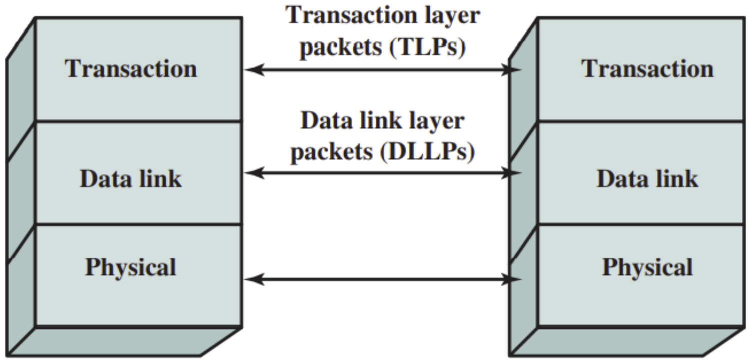
- **Switch:** The switch manages multiple PCIe streams.
- **PCIe endpoint:** An I/O device or controller that implements PCIe, such as a Gigabit ethernet switch, a graphics or video controller, disk interface, or a communications controller.
- **Legacy endpoint:** Legacy endpoint category is intended for existing designs that have been migrated to PCI Express, and it allows legacy behaviors such as use of I/O space and locked transactions. PCI Express endpoints are not permitted to require the use of I/O space at runtime and must not use locked transactions. By distinguishing these categories, it is possible for a system designer to restrict or eliminate legacy behaviors that have negative impacts on system performance and robustness.
- **PCIe/PCI bridge:** Allows older PCI devices to be connected to PCIe-based systems. As with QPI, PCIe interactions are defined using a protocol architecture.



PCI Physical and Logical Architecture

The PCIe protocol architecture encompasses the following layers:

- **Physical:** Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s and 0s.
- **Data link:** Is responsible for reliable transmission and flow control. Data packets generated and consumed by the DLL are called Data Link Layer Packets (DLLPs).
- **Transaction:** Generates and consumes data packets used to implement load/store data transfer mechanisms and also manages the flow control of those packets between the two components on a link. Data packets generated and consumed by the TL are called Transaction Layer Packets (TLPs).


Transaction
Transaction layer packets (TLPs)
Transaction
Data link
Data link layer packets (DLLPs)
Data link
Physical
Physical

Above the TL are software layers that generate read and write requests that are transported by the transaction layer to the I/O devices using a packet-based transaction protocol.