Chapter 1

Introduction to Microprocessors

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- A processor is the logic circuitry that responds to and processes the basic instructions that drive a computer.
- The term processor has generally replaced the term central processing unit (CPU)

Microprocessor

- CPU housed in a single silicon chip called microprocessor.
- Incorporate function of CPU in a single IC
- Set of circuit which connect the CPU with the rest of the computer.
- Consists of CPU, I/O ckt and memory access ckt

Mechanical Computing

- The abacus circa 500 B.C. – the first calculator
- Blaise Pascal – the first modern mechanical adder
- Charles Babbage – the first true computer
- Herman Hollerith – the punched card system and founder of IBM

Early electronic computers

- **Konrad Zuse – Z3 (relay logic at 5.33 Hz)**

– 1936-39, German used for aircraft and missile design during World War II.

- **Alan Turing – Colossus**

– 1943, vacuum tube, British military for decoding German codes in World War II.

• **University of Pennsylvania – ENIAC, 1946**

– The first general-purpose, programmable electronic computer.

– 1946, 17000 vacuum tubes, 500 miles of wires, weight 30 tons.

Early milestones

- 1948 – the transistor at Bell Labs
- 1958 – the integrated circuit
- 1961 – RTL digital logic
- 1971 – the microprocessor (4004)

Early programming

- Countess of Lovelace (1823) wrote programs for the Analytical Engine
- Machine Language then Assembly Language
- Grace Hopper (1957) develops FLOW-MATIC
- FORTRAN, ALGOL, and RPG
- COBOL

Modern programming

- Visual BASIC (most common business)
- Visual C/C++ (most common technical)
- JAVA (most common web)
- ADA and PASCAL
- C# (gaining on web)

Terms

- KIP – Kilo of Instructions per Second
- MIP – Millions of Instructions per Second
- Bit - a binary digit with a value of 1 or 0
- Nibble – 4-bit-wide binary number
- Byte – 8-bit-wide binary number Word (16 bits)
- Doubleword (32 bits) Quadword (64 bits)
- Octalword (128 bits)
- K – 1024, 1M – 1024K, 1G – 1024M

Early Microprocessors

- 4004 the first microprocessor (4-bit) 16K RAM
- 8008 (8-bit)
- 8080 (8-bit) 64K RAM, 2Mhz clock
- 8086 (16-bit) 1M RAM, 5MHz clock
- 80286 (16-bit) 16M RAM, 16MHz clock

32-bit Microprocessors

- 80386, 4G RAM, 33 MHz clock
- 80486, 4G RAM, 66 MHz clock
- Pentium, 4G RAM, 66 MHz clock
- Pentium Pro, 64G RAM, 133 MHz clock
- Pentium II, 64G RAM, 233 MHz clock
- Pentium III, 64G RAM, 500 MHz clock
- Pentium 4, 64G RAM, 1.5 GHz clock

The P nomenclature

- P1 – 8086/8088 class
- P2 – 80286 class
- P3 – 80386 class
- P4 – 80486 class
- P5 – Pentium class
- P6 – Pentium Pro/Pentium II, Pentium III, and Pentium 4 class

80x86 Evolution

4004:

- 4-bit microprocessor.
- 4KB main memory.
- 45 instructions.
- PMOS technology.
- 50 KIPS

8008: (1971)

- **8-bit** version of 4004.
- **16KB** main memory.
- 48 instructions.
- NMOS technology.

8080: (1973)

- 8-bit microprocessor.
- **64KB** main memory.
- 2 microseconds clock cycle time; 500,000 instructions/sec.
- 10X faster than 8008.

80x86 Evolution

8085: (1977)

- 8-bit microprocessor - upgraded version of the 8080.
- 64KB main memory.
- **1.3 microseconds** clock cycle time; 769,230 instructions/sec.
- 246 instructions.
- Intel sold 100 million copies of this 8-bit microprocessor.

8086: (1978) 8088 (1979)

- **16-bit** microprocessor.
- **1MB** main memory.
- 2.5 MIPS (400 ns).
- 4- or 6-byte instruction cache.
- Other improvements included more registers and additional instructions.

80286: (1983)

- 16-bit microprocessor very similar in instruction set to the 8086.
- **16MB** main memory.
- 4.0 MIPS (250 ns/8MHz).

80x86 Evolution

80386: (1986)

- **32-bit** microprocessor.
- **4GB** main memory.
- 12-33MHz.
- Memory management unit added.
- Variations: DX, EX, SL, SLC (cache) and SX.

  80386SX: 16MB through a 16-bit data bus and 24 bit address bus.

80486: (1989)

- 32-bit microprocessor, 32-bit data bus and 32-bit address bus.
- 4GB main memory.
- 20-50MHz. Later at 66 and 100MHz
- Incorporated an 80386-like microprocessor, 80387-like floating point co cessor and an 8K byte cache on one package.
- About half of the instructions executed in 1 clock instead of 2 on the 38
- Variations: SX, DX2, DX4.

  DX2: Double clocked version:

  66MHz clock cycle time with memory transfers at 33MHz

80x86 Evolution

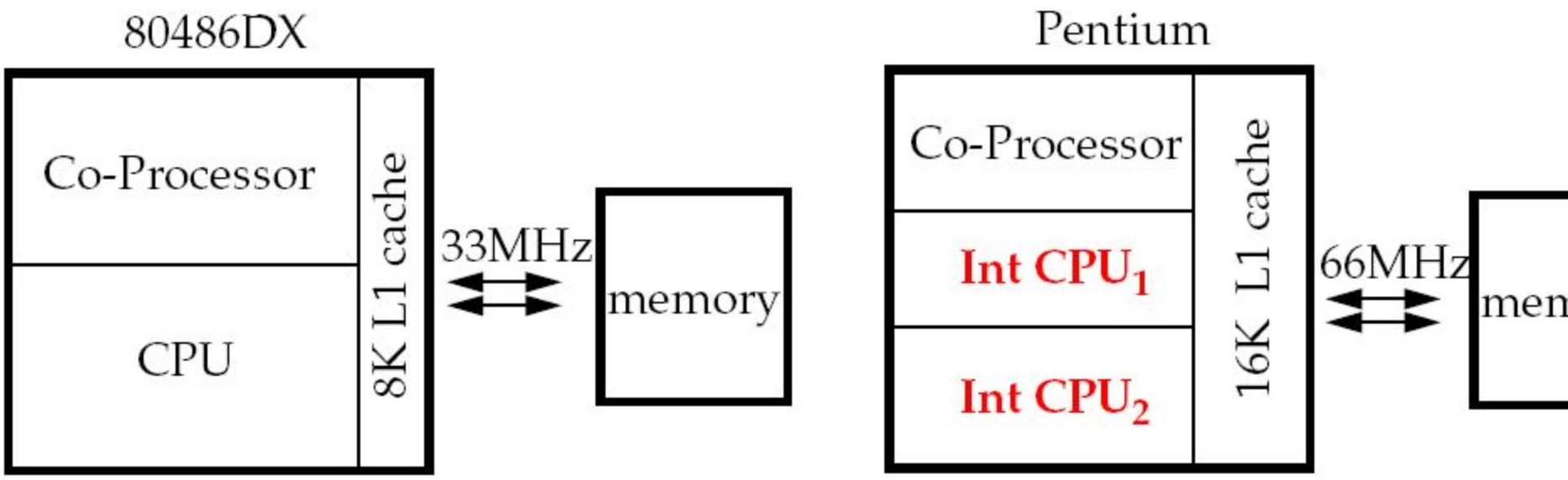
Pentium: (1993)

- 32-bit microprocessor, 64-bit data bus and 32-bit address bus.
- 4GB main memory.
- 60, 66, 90MHz.

  1-and-1/2 100MHz version.

  Double clocked 120 and 133MHz versions.

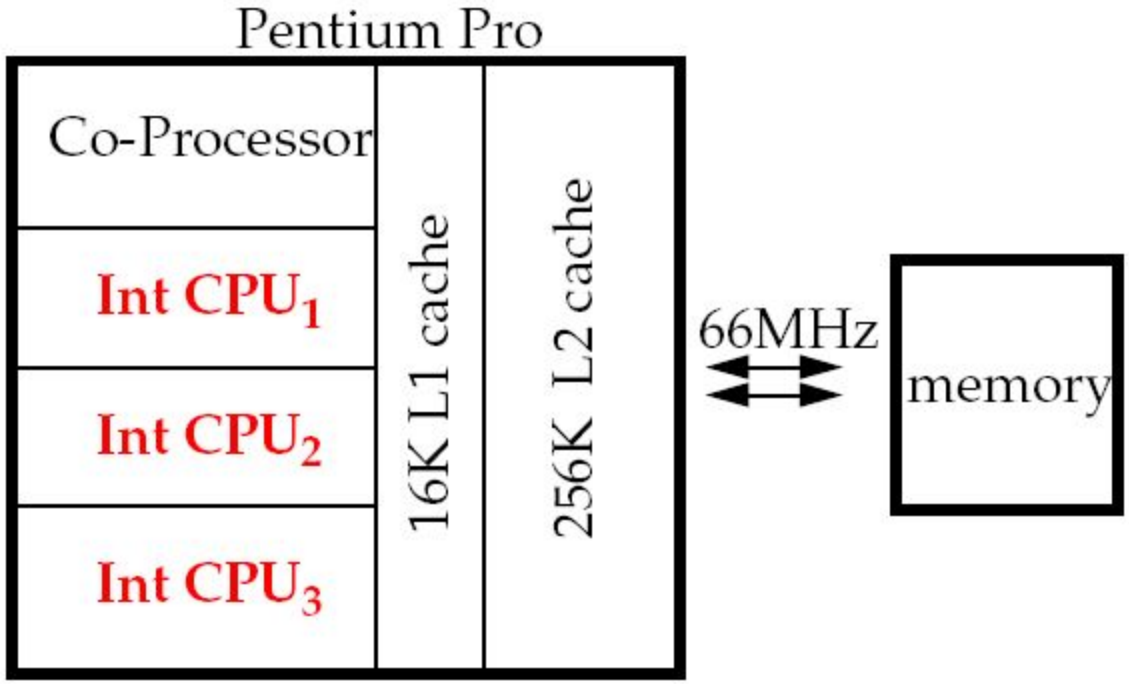
  Fastest version is the 233MHz (3-and-1/2 clocked version).
- **16KB L1 cache (split instruction/data: 8KB each).**
- Memory transfers at **66MHz** (instead of 33MHz).
- **Dual integer processors.**



80x86 Evolution

Pentium Pro: (1995)

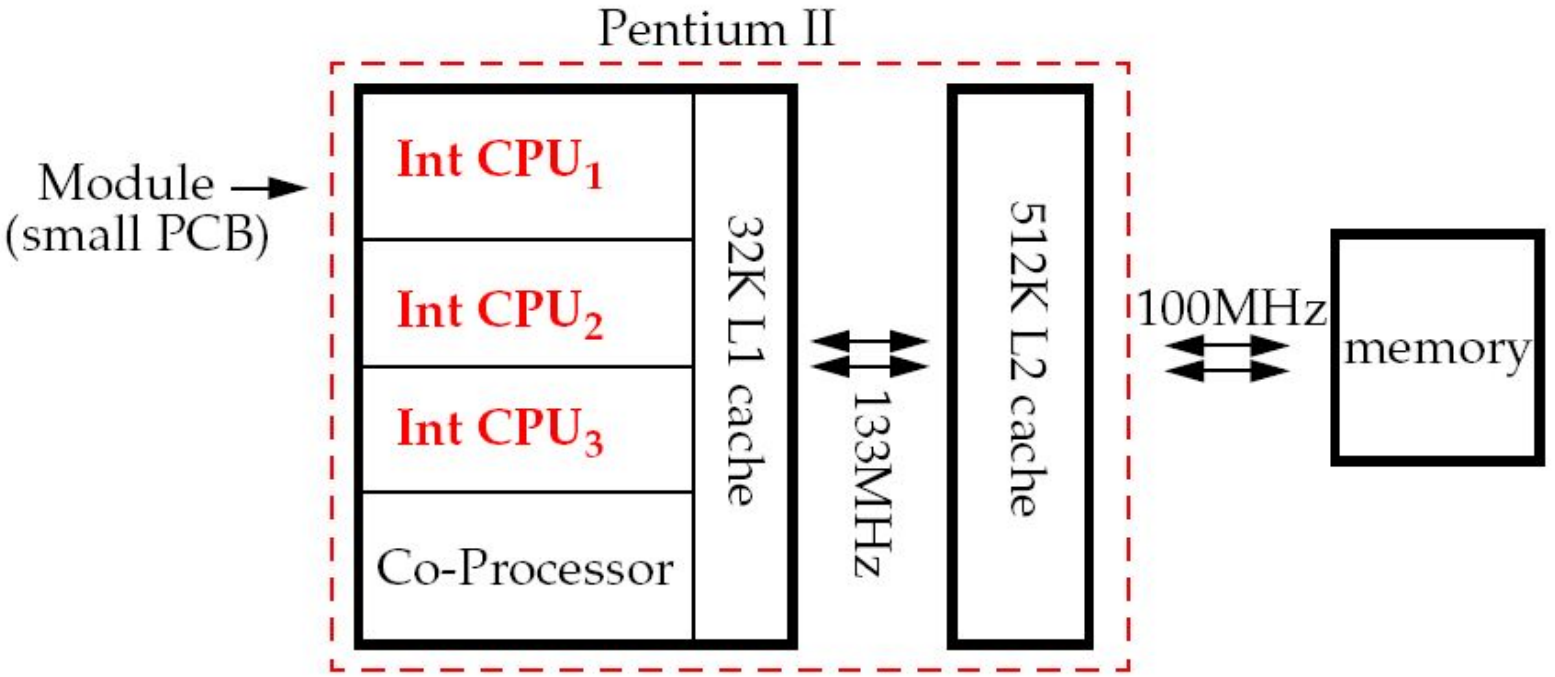
- 32-bit microprocessor, 64-bit data bus and 36-bit address bus.
- **64GB** main memory.
- Starts at 150MHz.
- 16KB L1 cache (split instruction/data: 8KB each).
- **256KB L2 cache.**
- Memory transfers at 66MHz.
- **3 integer processors.**



80x86 Evolution

Pentium II: (1997)

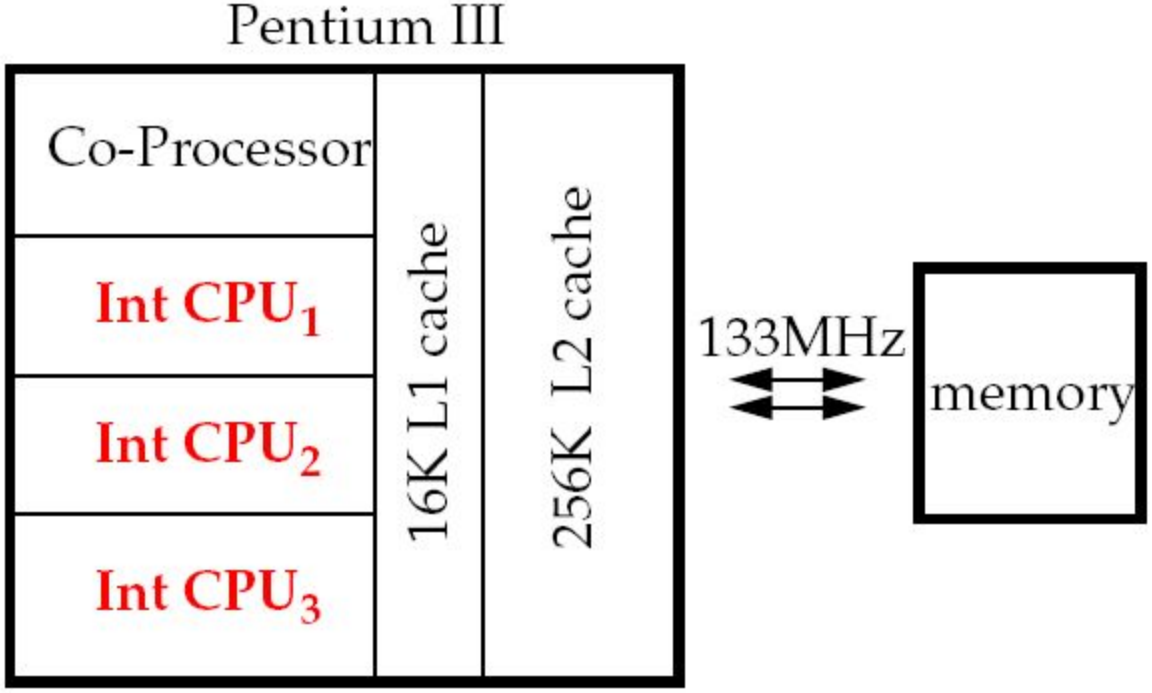
- 32-bit microprocessor, 64-bit data bus and 36-bit address bus.
- 64GB main memory.
- Starts at 266MHz.
- **32KB** split instruction/data L1 caches (16KB each).
- **Module integrated 512KB L2 cache (133MHz).**
- Memory transfers at 66MHz to **100MHz** (1998).



80x86 Evolution

Pentium III: (1999)

- 32-bit microprocessor, 64-bit data bus and 36-bit address bus.
- 64GB main memory.
- Up to 800MHz.
- 32KB split instruction/data L1 caches (16KB each).
- **On-chip 256KB L2 cache (at-speed).**
- Memory transfers 100MHz to **133MHz.**
- **Dual Independent Bus (simultaneous L2 and system memory access**



80x86 Evolution

Pentium IV: (2002)

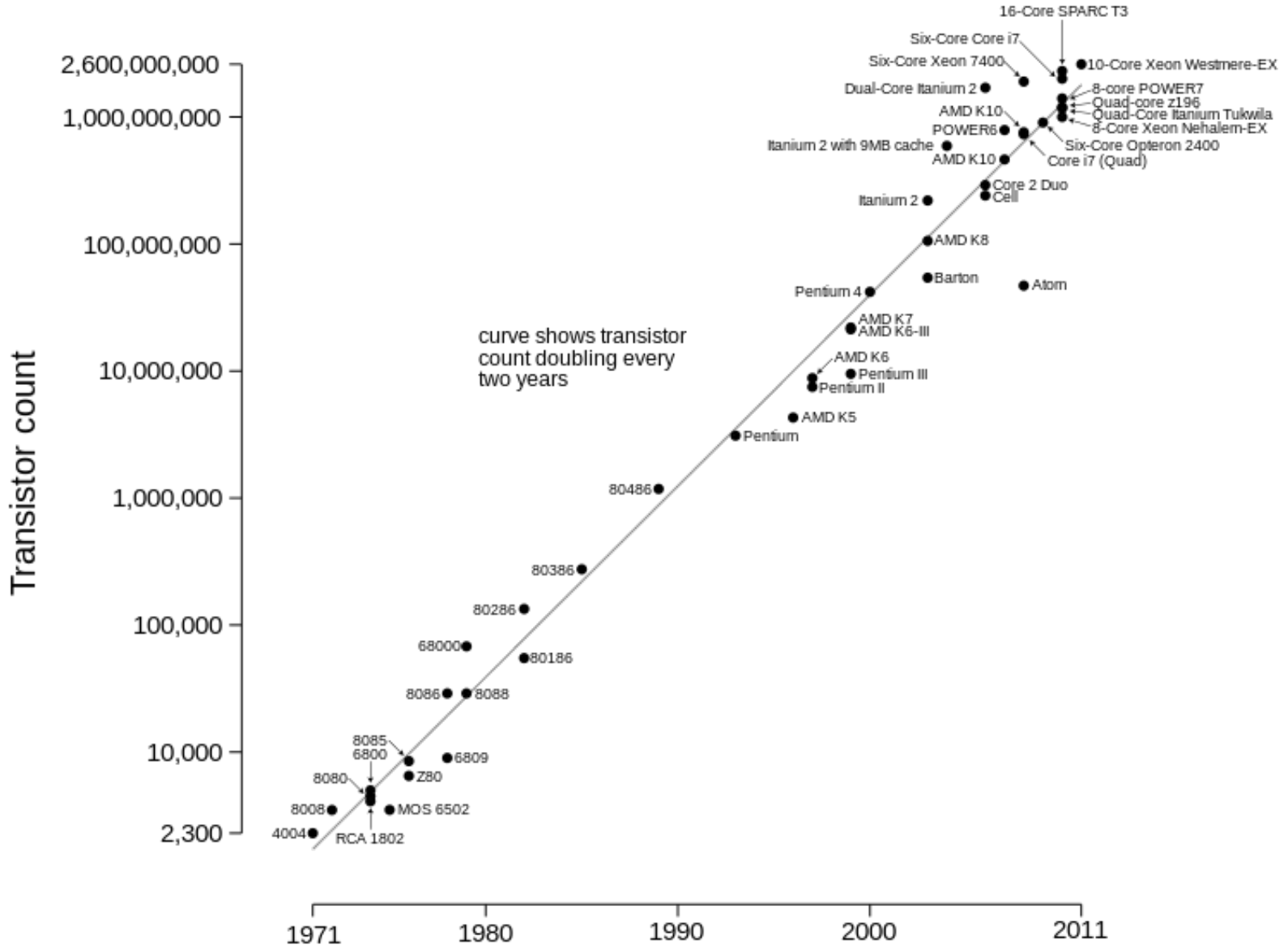
- 1.4 to 1.9GHz and the latest at 2.2 GHz!
- 512KB L2 cache.
- 400 MHz system bus (quad pumping a 100MHz bus) (3.2 GB/sec).
- Specialized for streaming video, game and DVD apps (144 new SIMD instructions).
- Support for 200/266MHz DDR (Double Data Rate) SDRAM (Synchron DRAM).
- 0.13um, 55 million transistors, 60nm transistors.

Moore’s law

- **Moore's law** is the observation that the number of transistors in a dense integrated circuit doubles approximately every two years. The observation is named after Gordon MooreMoore, the co-founder of IntelMoore, the co-founder of Intel and Fairchild SemiconductorMoore, the co-founder of Intel and Fairchild Semiconductor, whose 1965 paper described a doubling every year in the number of components per integrated circuit and projected this rate of growth would continue for at least another decade.

Microprocessor Transistor Counts 1971-2011 & Moore's Law

Diagram



- Moore's law is an observationMoore's law is an observation or projectionMoore's law is an observation or projection and not a physicalMoore's law is an observation or projection and not a physical or natural lawMoore's law is an observation or projection and not a physical or natural law. Although the rate held steady from 1975 until around 2012, the rate was faster during the first decade. In general, it is not logically sound to extrapolate from the historical growth rate into the indefinite future. For example, the 2010 update to the International Technology Roadmap for Semiconductors, predicted that growth would slow around 2013,[18] and Gordon Moore in 2015 foresaw that the rate ofprogress and Gordon Moore in 2015 foresaw that the rate ofprogress would reach saturation: "I see Moore's law dying here in the next decade or so."
- Intel stated in 2015 that the pace of advancement has slowed, starting at the 22 nmIntel stated in 2015 that the pace of advancement has slowed, starting at the 22 nm feature width around 2012, and continuing at 14 nmIntel stated in 2015 that the pace of advancement has slowed, starting at the 22 nm feature width around 2012, and continuing at 14 nm. Brian KrzanichIntel stated in 2015 that the pace of advancement has slowed, starting at the 22 nm feature width around 2012, and continuing at 14 nm. Brian Krzanich, CEO of Intel, announced that "our cadence today is closer to two and a half years than two." This is scheduled to hold through the 10 nm width in late 2017. He cited Moore's 1975 revision as a precedent for the current deceleration, which results from technical challenges and is "a natural part of the history of Moore's law."[

Tasks

- **µP performs 3 main tasks:**

– **Data transfer -** µP and the memory or I/O systems.

– **Arithmetic and logic operations.**

– **Program flow via simple decisions**

Power of µP

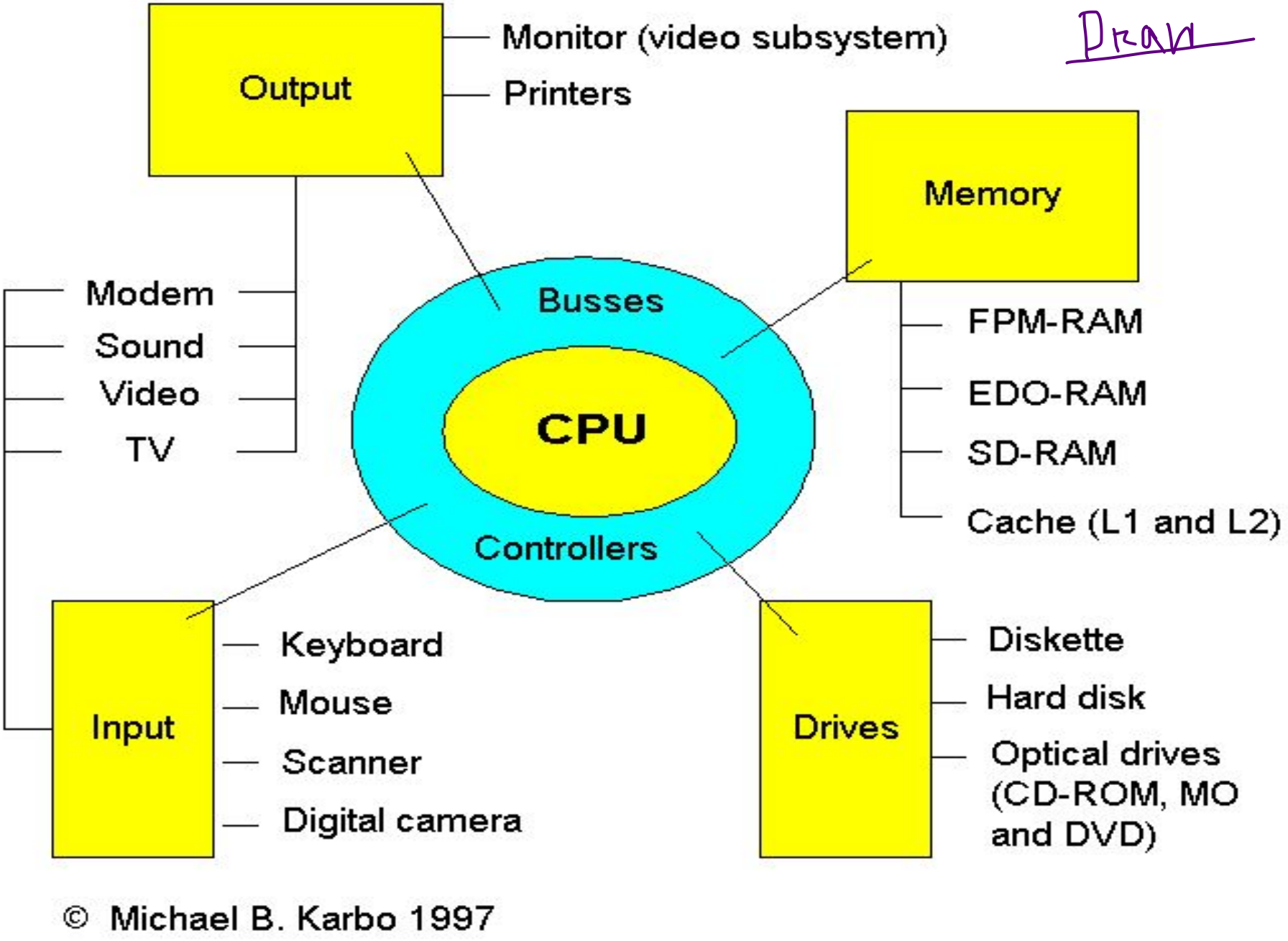
- • **Capable of executing billions of millions of**
- **instructions per second from a program or software**
- **stored in the memory system**

- µP-based PC Systems

- • Memory system
- • I/O system
- • µP

Von Neumann Model

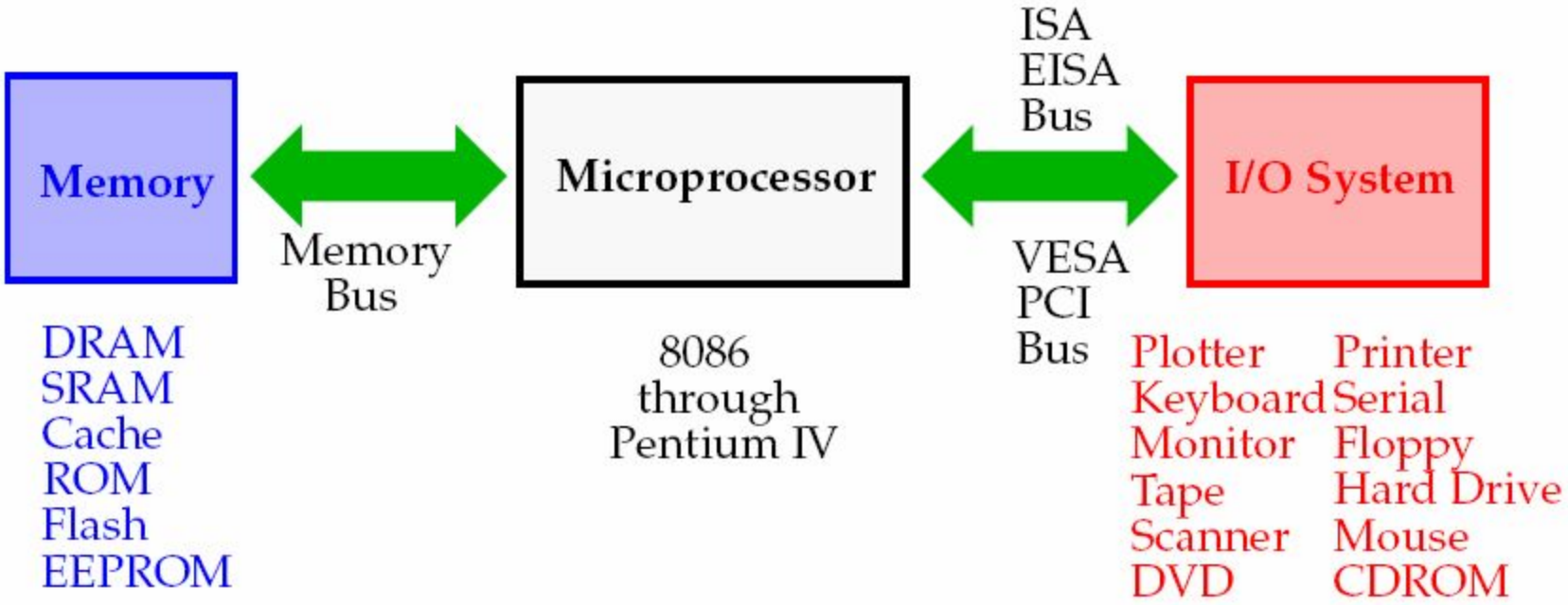
- Roots of the modern PC go back to the 1940's
- • John Von Neumann proposed this design:
- – CPU
- – Input
- – Output
- – Working Memory
- – Permanent Memory



Basic Architecture

Basic components

Draw



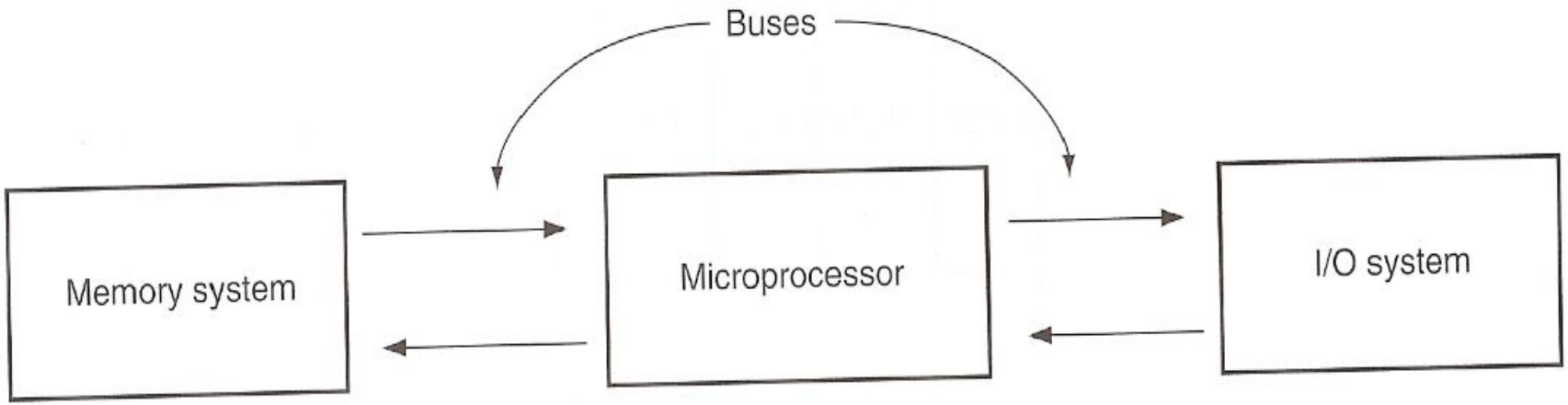
Cache Memory

- A temporary high speed memory that buffers the slower DRAM from the higher speed microprocessor.
- Usages in bursts of 4 memory-sized chunks of data (today 4, 64-bit numbers)
- Level 1 (small cache for local high-speed storage)
- Level 2 (larger cache for local high-speed storage.
- Level 3 (large cache on Pentium 4 chip)

Memory Organization

- Memory is organized in byte-sized (wide) chunks of data
- Memory is numbered in bytes
- Memory is number in hexadecimal addresses or locations
- Modern memory is 64-bits wide containing 8 bytes per memory physical location.
- Buffering and double clock edge transfers can speed memory access times to about 25 MHz

Computer Block Diagram



Dynamic RAM (DRAM)
Static RAM (SRAM)
Cache
Read-only (ROM)
Flash memory
EEPROM
SDRAM
RAMBVS
DDR DRAM

8086
8088
80186
80188
80286
80386
80486
Pentium
Pentium Pro
Pentium II
Pentium III
Pentium 4

Printer
Serial communications
Floppy disk drive
Hard disk drive
Mouse
CD-ROM drive
Plotter
Keyboard
Monitor
Tape backup
Scanner
DVD

Computer System Functions

- CPU (microprocessor) – performs
  - arithmetic and logic operations (table 1-4)
  - data transfers (to memory or i/o)
  - program flow via simple decisions (table 1-5)
- Memory – stores program and data
- I/O – communicates to humans and machines (figure 1-11)

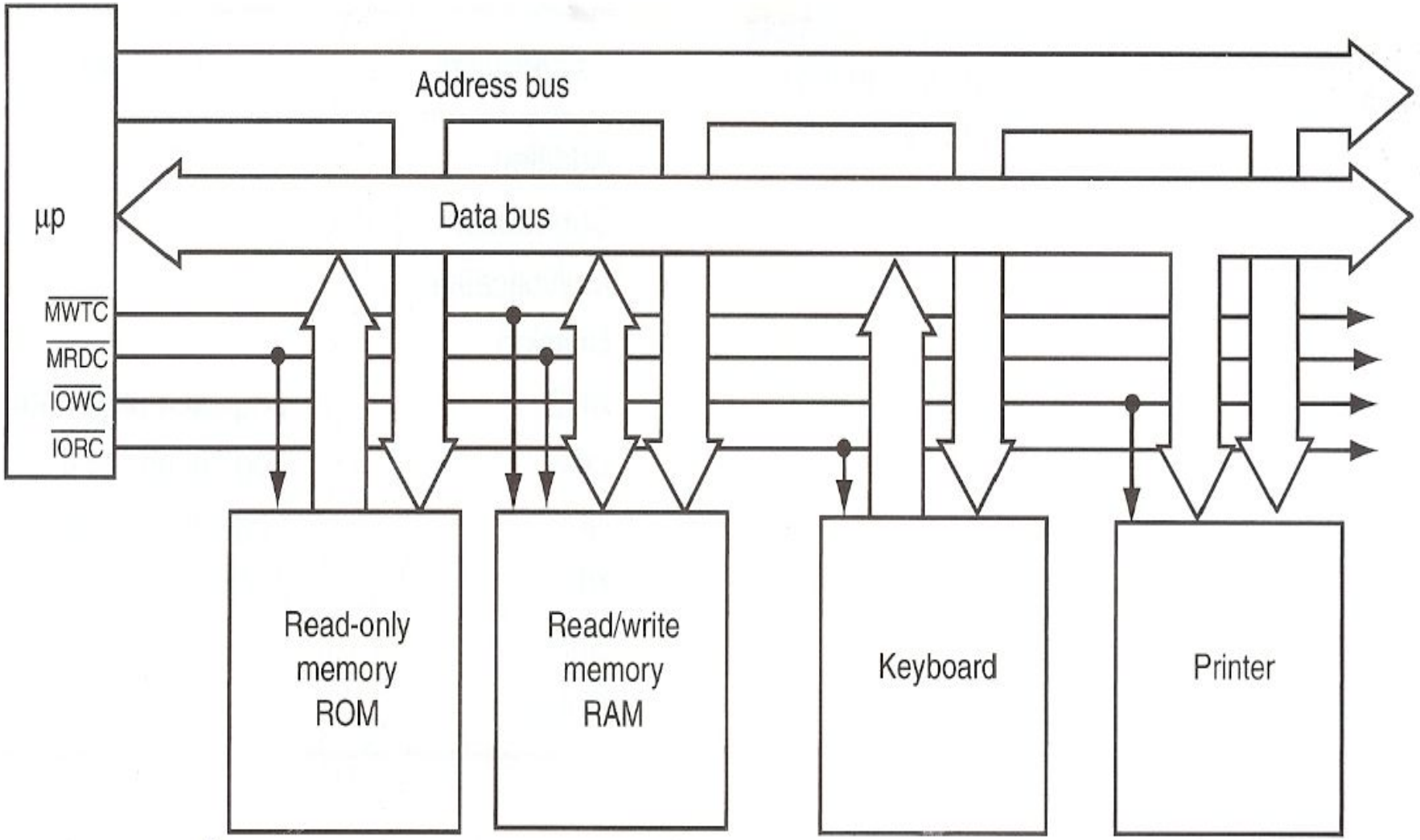
PCI

- PCI (Peripheral Component Interconnect) is an interconnection system between a microprocessor and attached devices in which expansion slots are spaced closely for high speed operation. Using PCI, a computer can support both new PCI cards while continuing to support Industry Standard Architecture (ISA) expansion cards, an older standard. Designed by Intel, the original PCI was similar to the VESA Local Bus.

I/O Space

- Port 0000H to ffffH (64K 8-bit i/o devices)
- Two major sections
  - System devices (motherboard, etc)
  - Reserved for expansion
- Various I/O devices that control the system are not directly addressed. System BIOS Rom addresses these devices.
- Access made through OS or BIOS function calls to maintain compatibility from one computer system to another

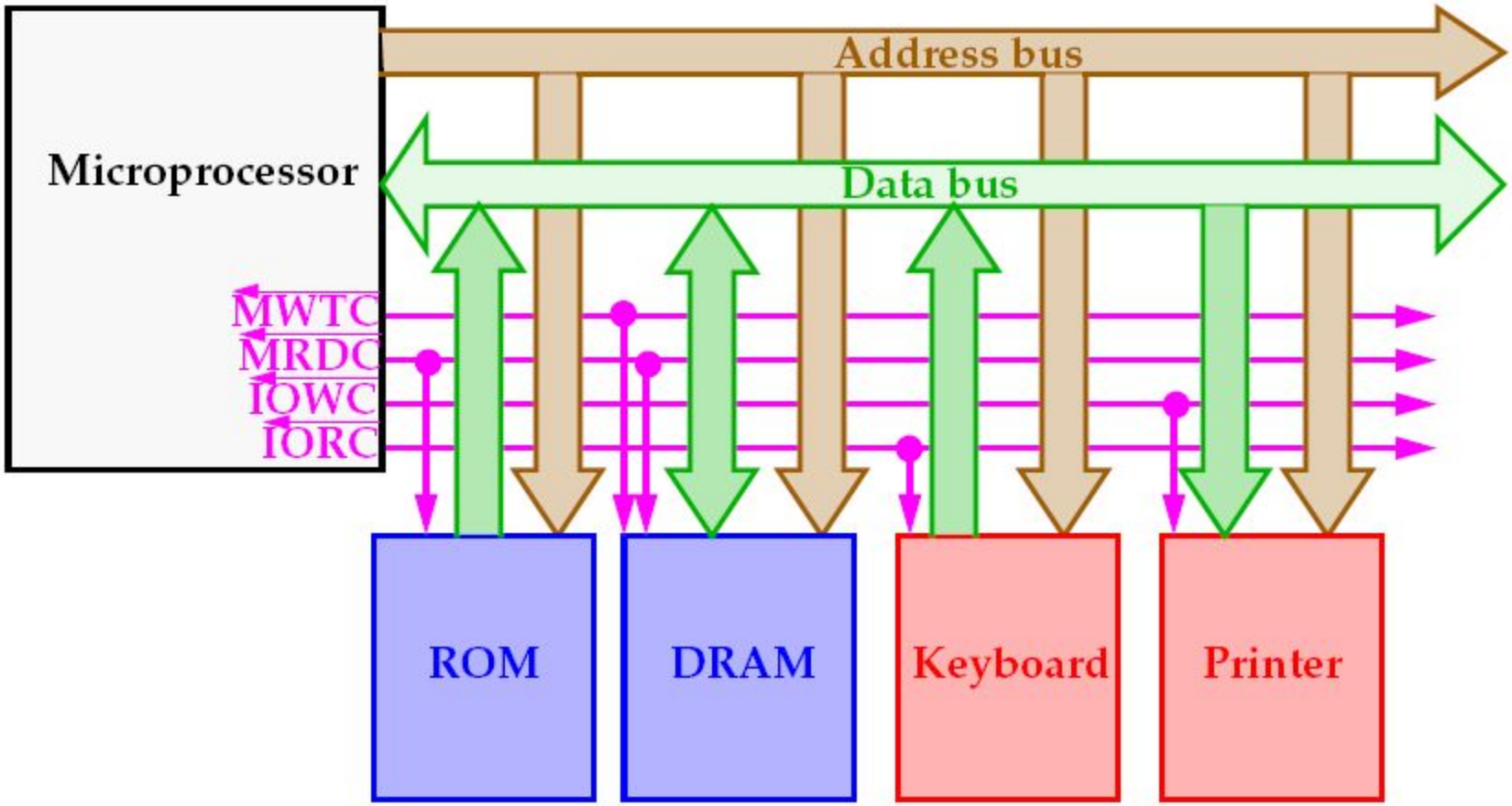
Computer Structure



Basic Architecture

Bus Architecture:

Dram



The Pentium bus architecture is not this simple.

We will elaborate on this later.

Buses

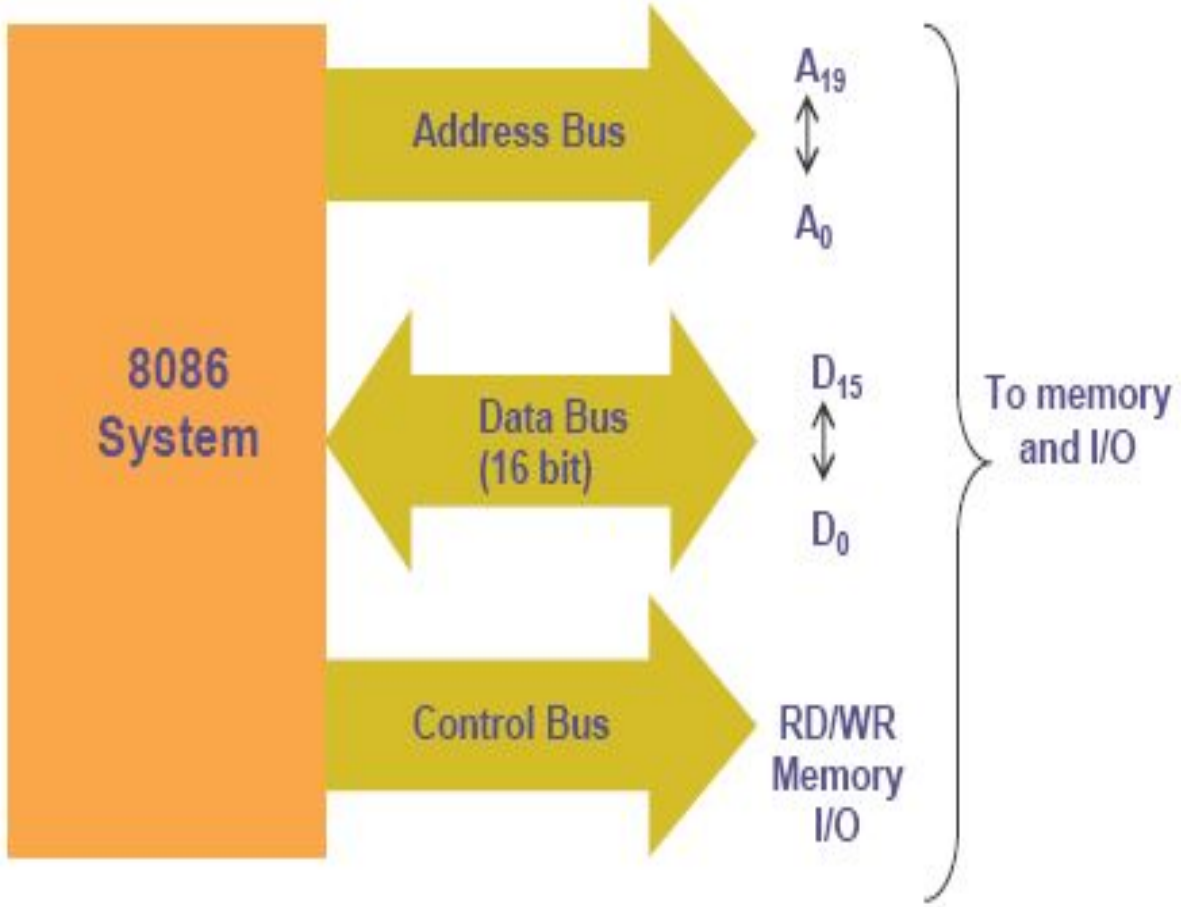
- **Address Bus** – selects a location in the memory or a specific I/O device
- **Data Bus** – transfers data between the microprocessor and the memory or I/O
- **Control Bus** – selects I/O or memory and causes a read or a write
- See Table 1-6 for Bus widths and memory sizes

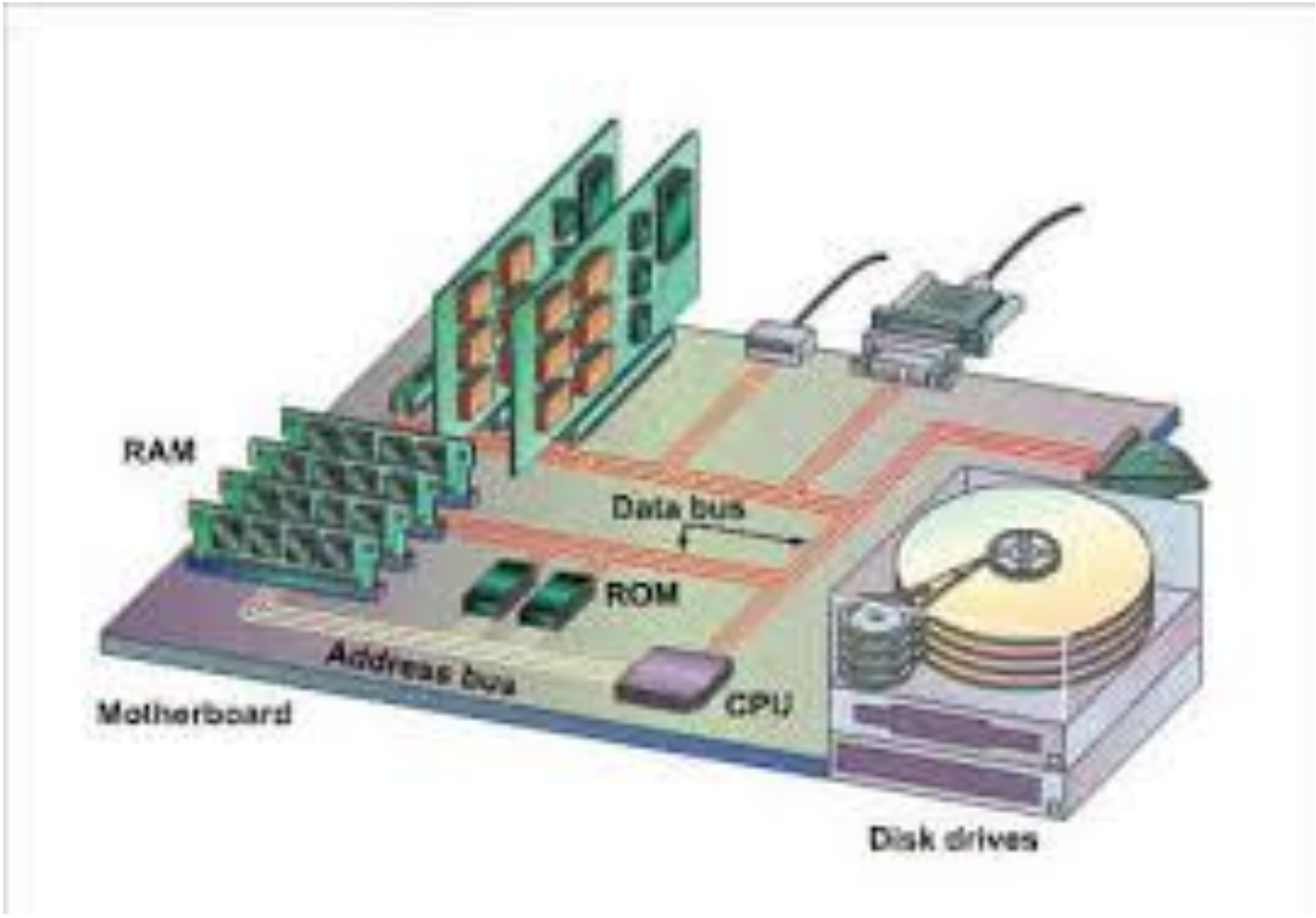
Buses: A common group of wires that interconnect components in a computer system.

***Address** Bus* provides a memory address to the system memory and I/O address to the system I/O devices

Data Bus transfers data between the microprocessor and the memory and I/O attached to the system

Control Bus provides control signals that cause the memory or I/O to perform a read or write operation





Intel µP Buses

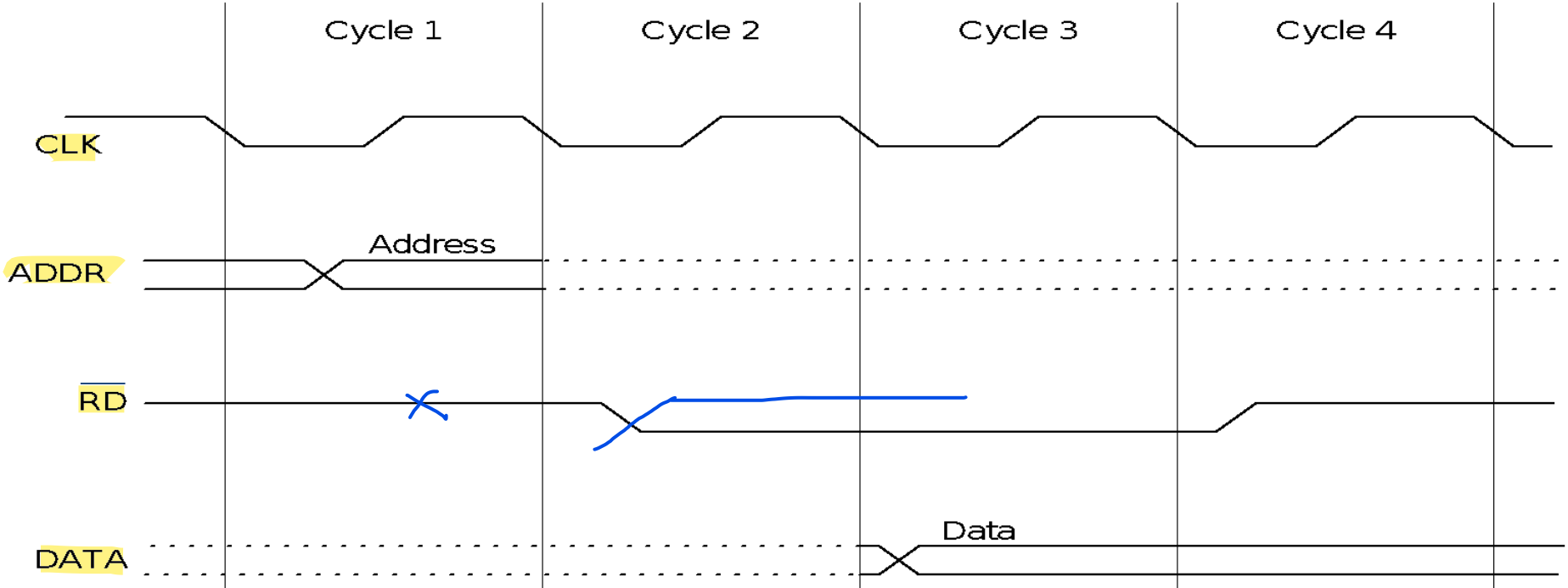
Processor	Data Bus	Address Bus	Max Addressable Memory	
8088	8	20	1,048,576	(1Mb)
8086	16	20	1,048,576	(1Mb)
80286	16	24	16,777,21	(16Mb)
80386dx	32	32	4,294,976,296	(4Gb)
80486	32	32	4,294,976,296	(4Gb)
80586/Pentium (Pro)	64	32	4,294,976,296	(4Gb)

Reading from Memory

Draw

Multiple machine cycles are required when reading from memory, because it responds much more slowly than the CPU. The steps are:

- address placed on address bus
- Read Line (RD) set low
- CPU waits one cycle for memory to respond
- Read Line (RD) goes to 1, indicating that the data is on the data bus



Basic Bus Architecture

Bus Architecture: Three buses:

- *Address:*

  If I/O, a value between 0000H and FFFFH is issued.

  If memory, it depends on the architecture:

  20-bits (8086/8088)

  24-bits (80286/80386SX)

  25-bits (80386SL/SLC/EX)

  32-bits (80386DX/80486/Pentium)

  36-bits (Pentium Pro/II/III)

- *Data:*

  8-bits (8088)

  16-bits (8086/80286/80386SX/SL/SLC/EX)

  32-bits (80386DX/80486/Pentium)

  64-bits (Pentium/Pro/II/III)

- *Control:*

  Most systems have at least 4 control bus connections (active low).

  $\overline{\textbf{MRDC}}$ (Memory ReaD Control), $\overline{\textbf{MWRC}}$, $\overline{\textbf{IORC}}$ (I/O Read Control), $\overline{\textbf{IOWC}}$.

Basic Bus Architecture

Bus Standards:

- **ISA** (Industry Standard Architecture): 8 MHz
  - 8-bit (8086/8088)
  - 16-bit (80286-Pentium)

- **EISA**: 8 MHz
  - 32-bit (older 386 and 486 machines).

- **PCI** (Peripheral Component Interconnect): 33 MHz
  - 32-bit or 64-bit (Pentiums)

- **VESA** (Video Electronic Standards Association): Runs at processor speed.
  - 32-bit or 64-bit (Pentiums)
  - Only disk and video. Competes with the PCI but is not popular.

Basic Bus Architecture

Bus Standards:

- **USB** (Universal Serial Bus): 10 Mbps (extensions to 100Mbps)

  Newest systems.

  Serial connection to microprocessor.

  For keyboards, the mouse, modems and sound cards.

  - To reduce system cost through fewer wires.

- **AGP** (Advanced Graphics Port): 66MHz

  Newest systems.

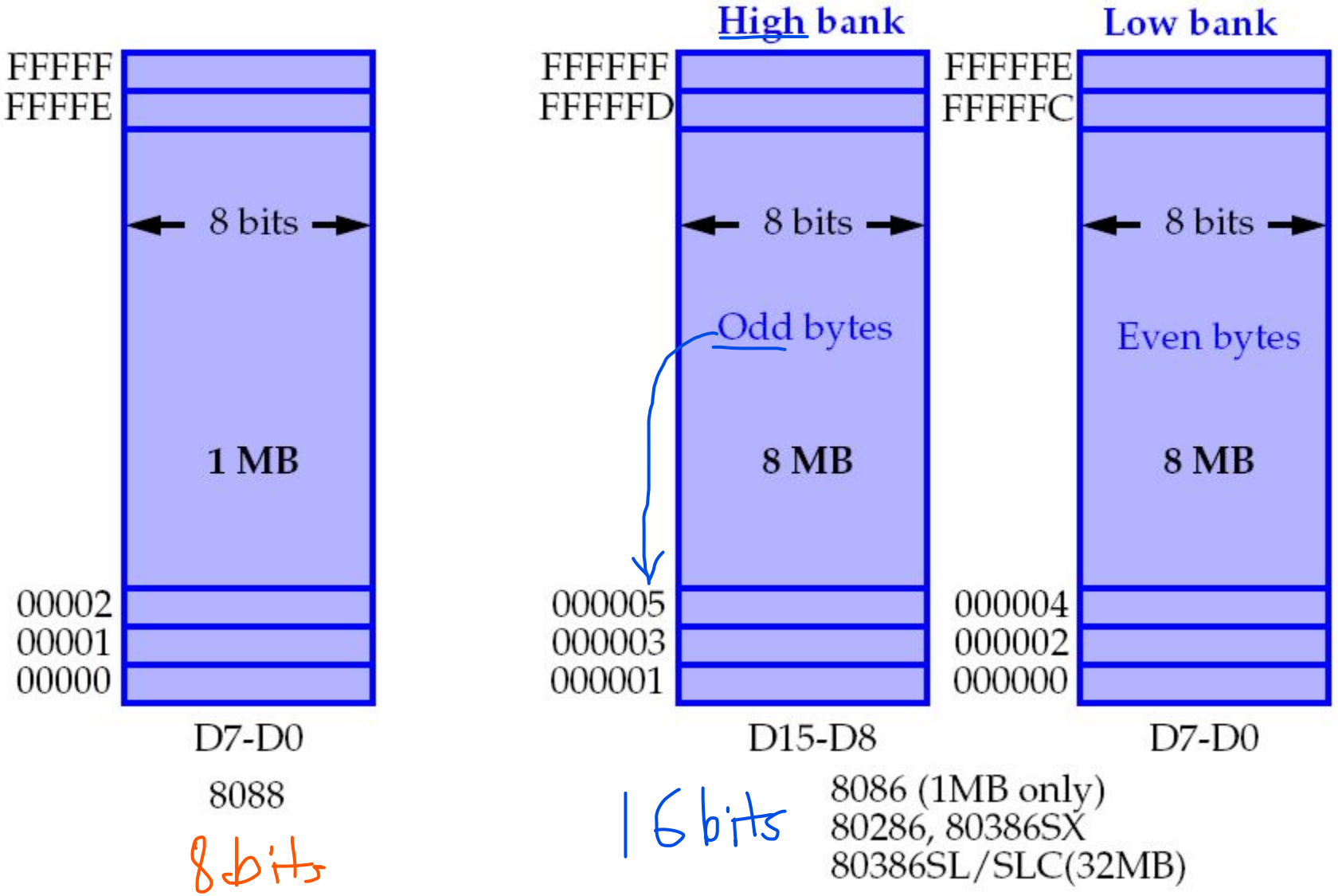
  Fast parallel connection: Across 64-bits for 533MB/sec.

  For video cards.

  - To accommodate the new **DVD** (Digital Versatile Disk) players.

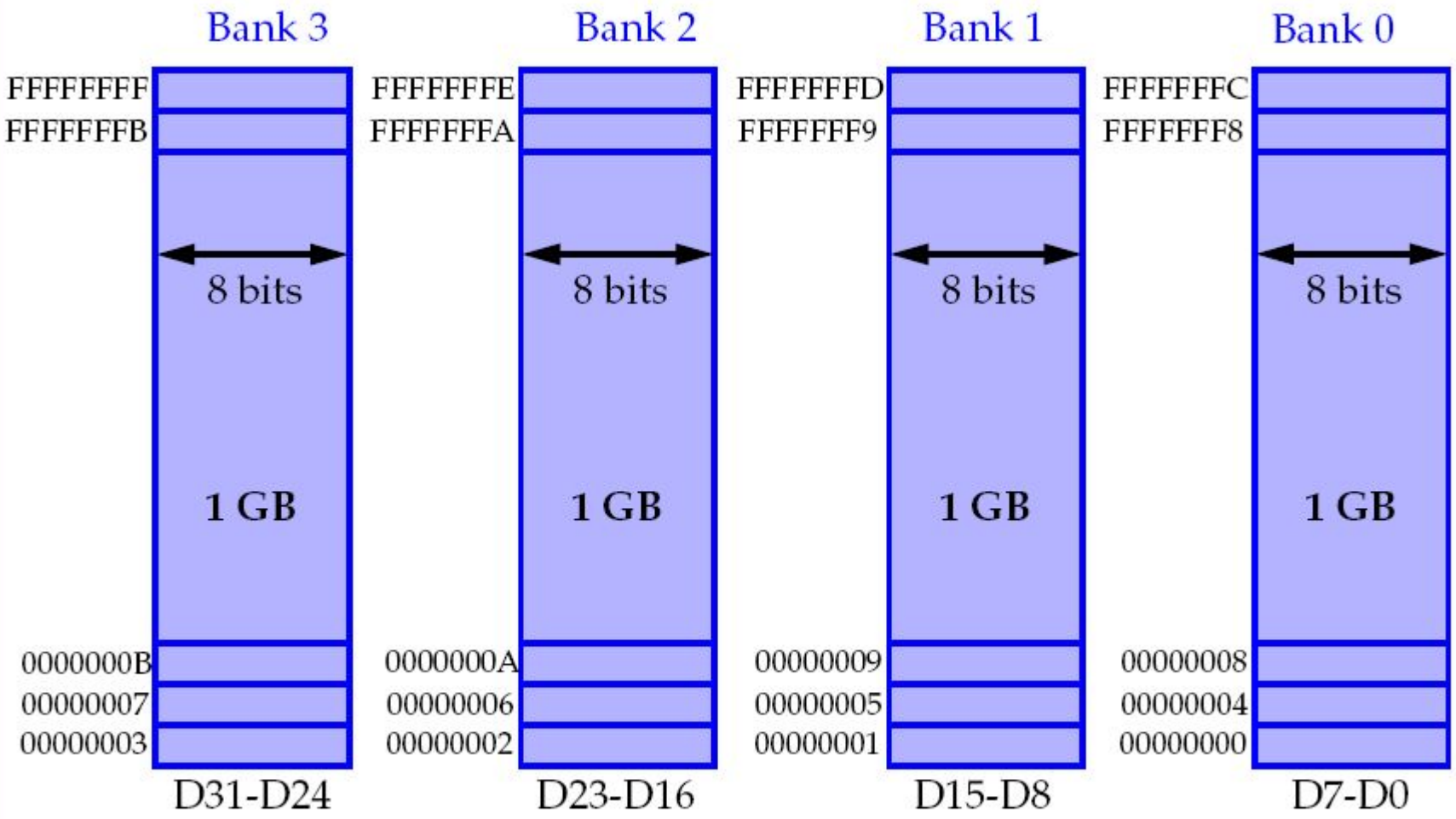
Basic Memory Architecture

Bank layout

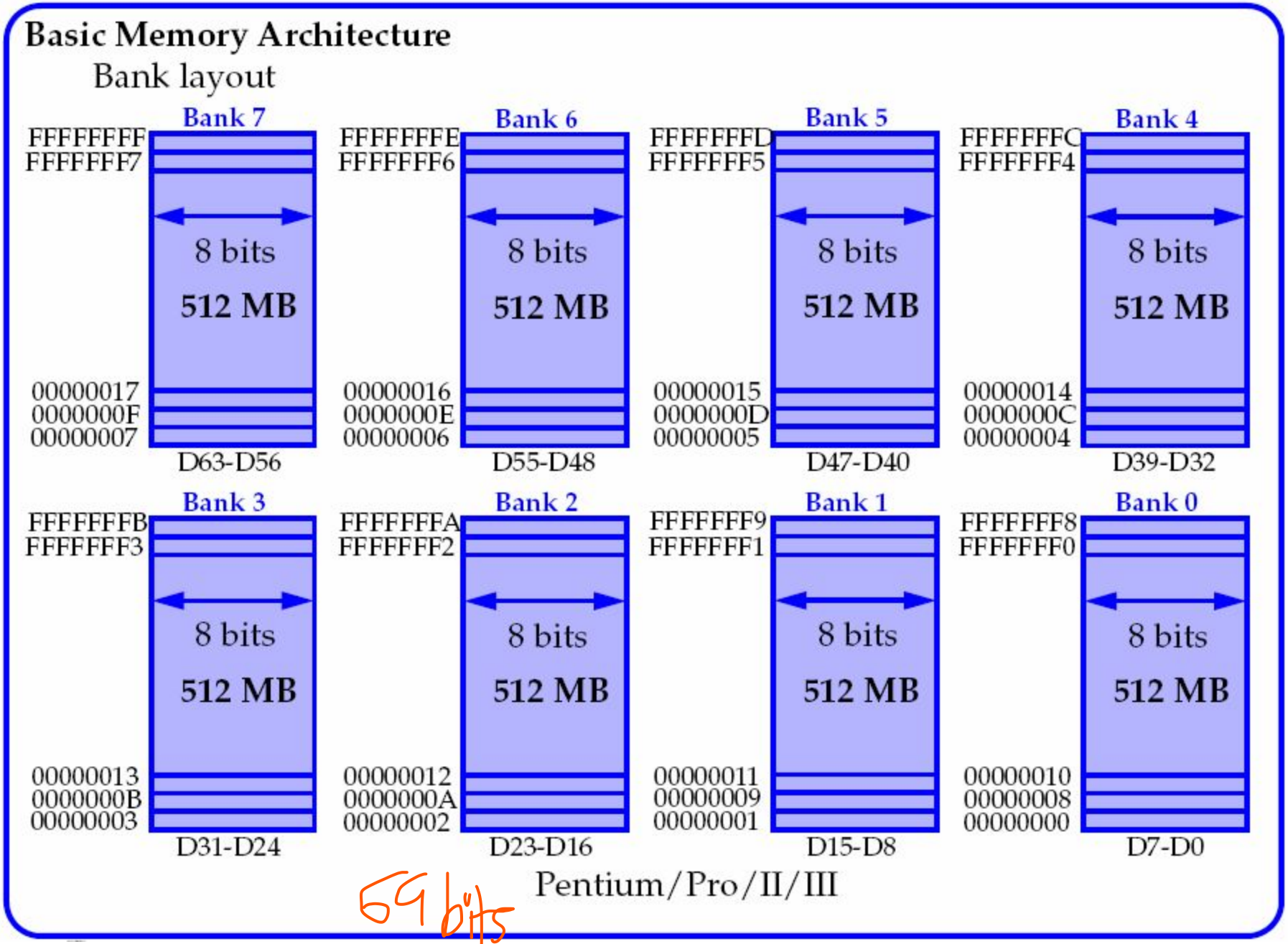


Basic Memory Architecture

Bank layout



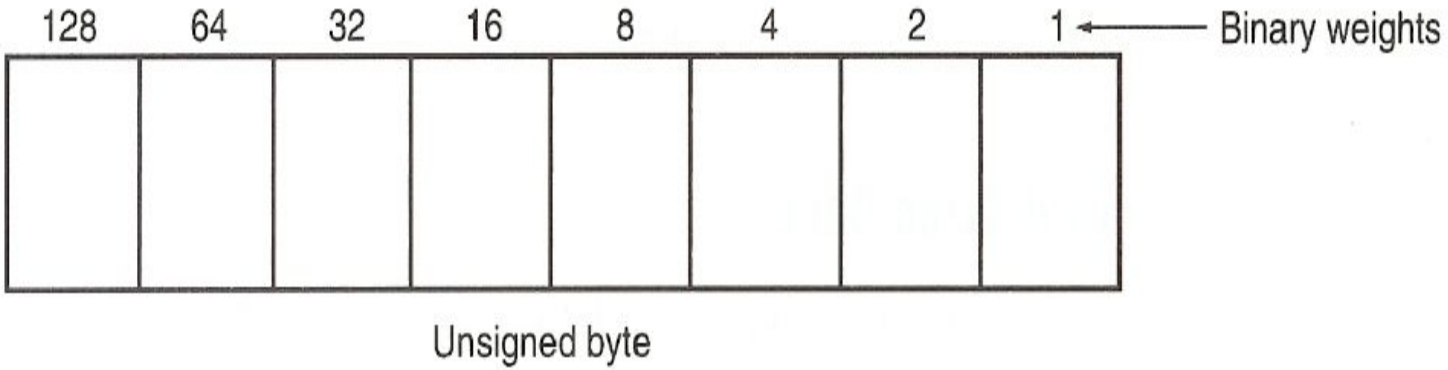
32 bits 80386DX, 80486



Memory Organization

- 8086/8088 – 8- or 16-bits in width
- 80286 – 16-bits in width
- 80386/80486 – 32-bits in width
- Pentium/Pentium 4 – 64-bits in width

8-bit Data



8-bit Data Formats

- In the assembler use:

```
DATA1  DB   10H
```

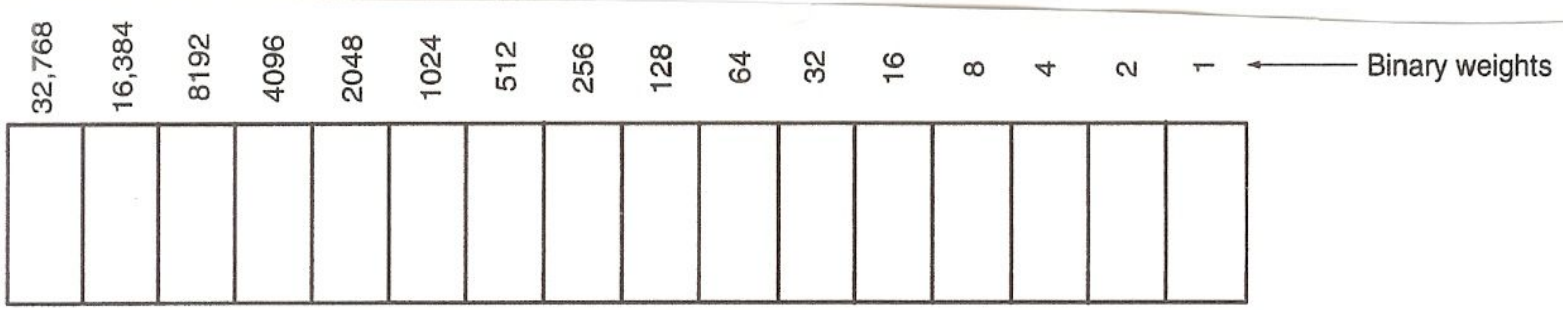
- In C++

```
char Data1 = 0x10;
```

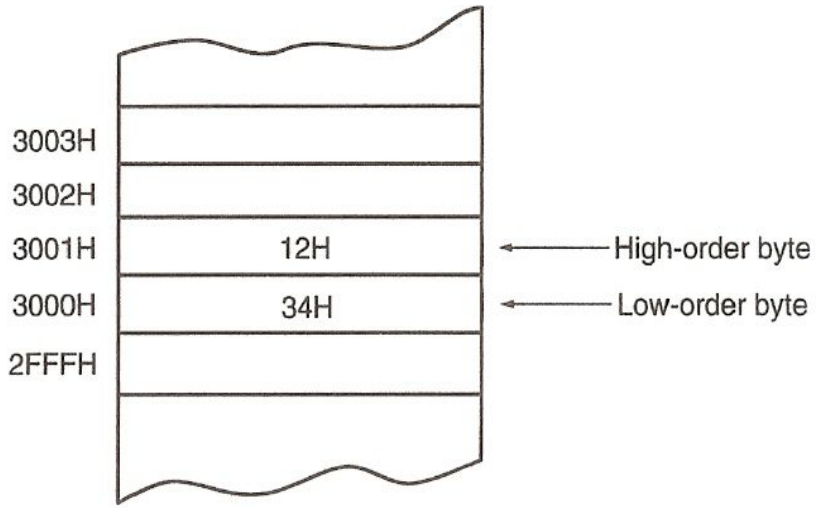
or

```
unsigned char Data2 = 3;
```

16-bit Data



(a) Unsigned word



(b) The contents of memory location 3000H and 3001H are the word 1234H.

16-bit Data Formats

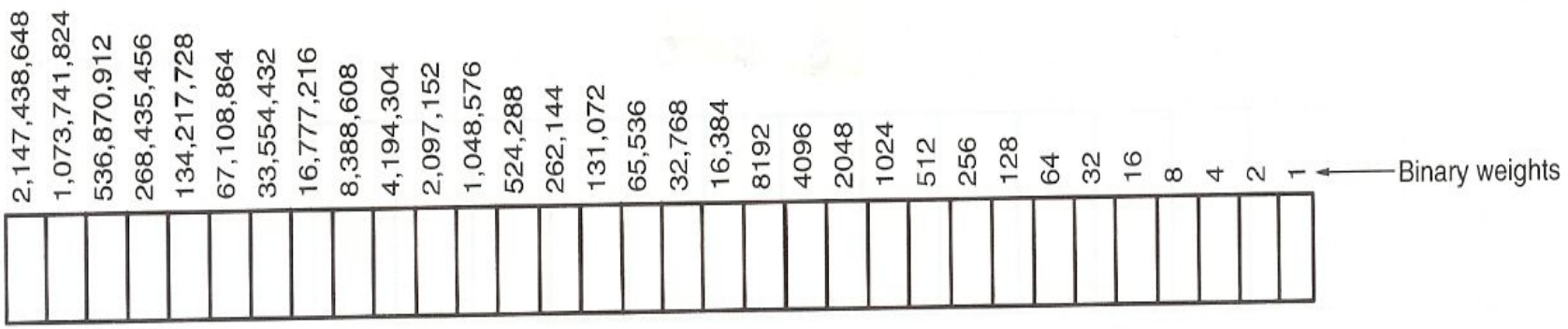
- In the assembler

```
Data3   DW   1000H
```

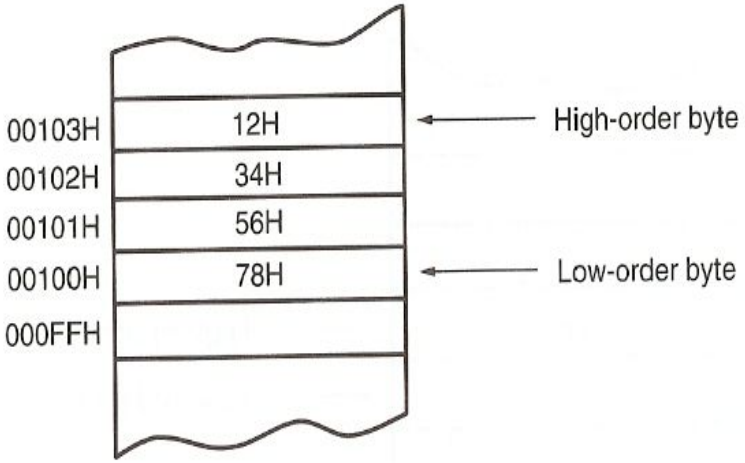
- In C++

```
short  Data3 = 0x1000;
    or
_int16 Data4 = 23;
    or
unsigned short Data5 = 4;
```

32-bit Data



(a) Unsigned doubleword



(b) The contents of memory location 00100H –00103H are the doubleword 12345678H.

32-bit Data Formats

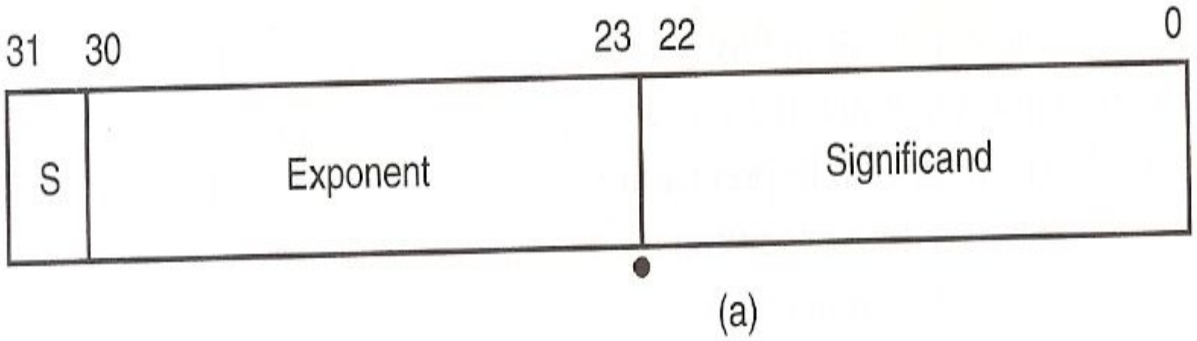
- In the assembler

```
DATA6    DD  10002345H
```

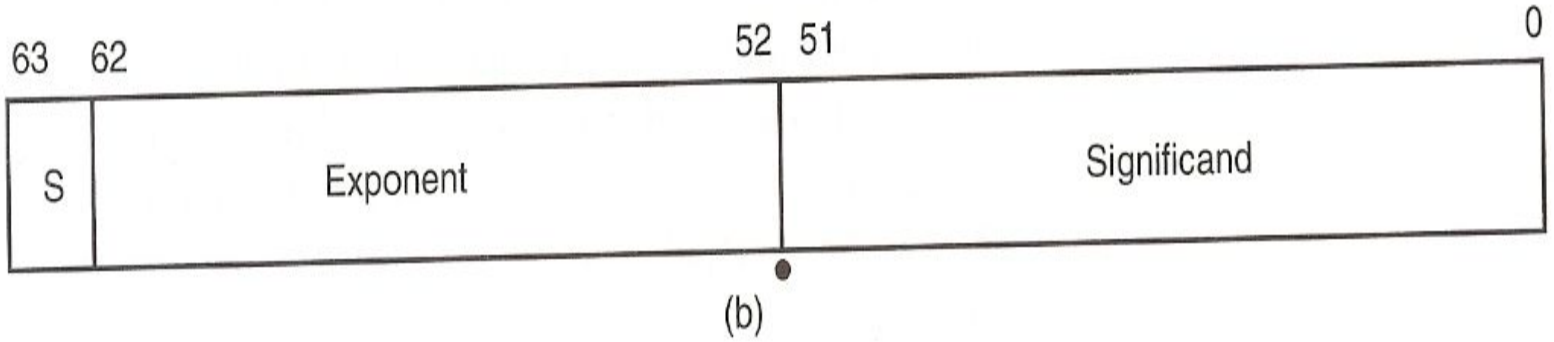
- In C++

```
int Data6 = 0x10002345;
        or
unsigned int Data7 = 34566;
        or
UINT Data8 = 344;
```

Floating-point Data



(a)



(b)

Floating-Point Formats

- In the assembler

```
DATAA   DD  23.4
DATAB   DQ  -345.0
DATAR   DQ  3.5E2
```

- In C++

```
float DataC = 23.4;
double DataD = -345;
double DataE = 3.5e2;
```

Complements

- Twos complements are used to store negative data in modern computers
- To twos complement a number invert all the bits and ten add 1 to the result

Hexadecimal-coded Binary

- Binary numbers are often coded in groups of 4 bits to represent hexadecimal numbers.
- 0100 0001 1010 = $41A_{16}$
- $3C45_{16}$ = 0011 1100 0100 0101