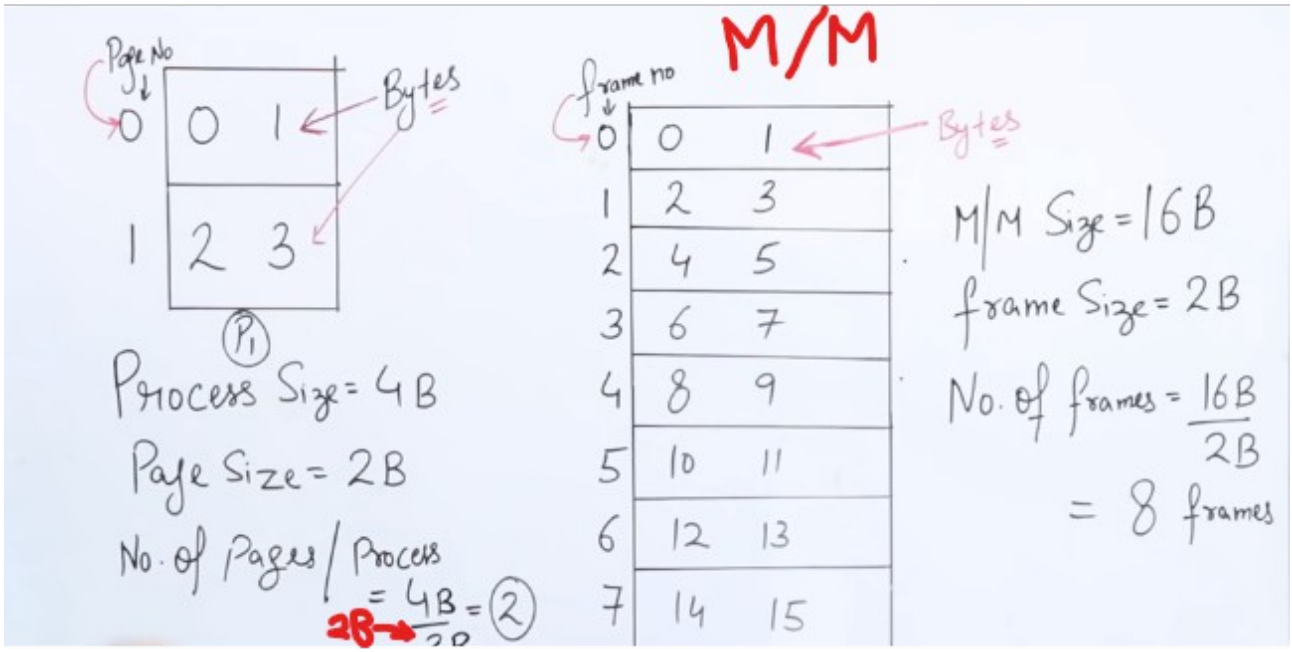

Figure 1:

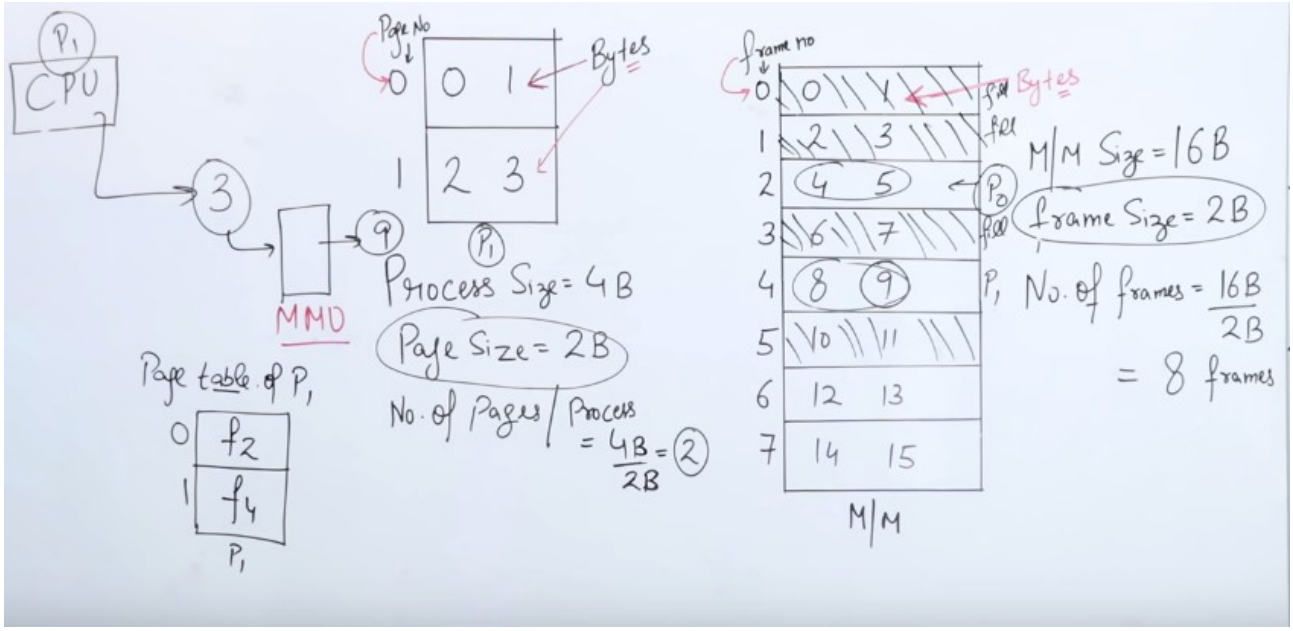

Figure 2:

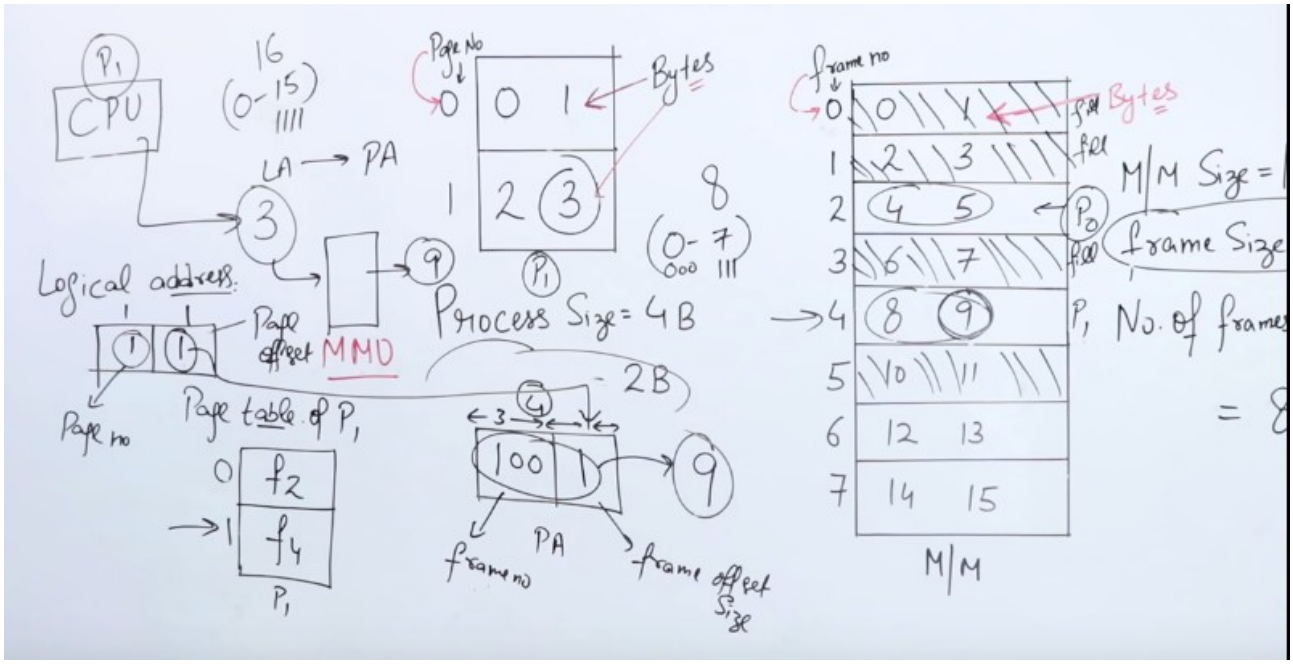

***Figure 3**:*

Always Remember:

- Memory is byte-addressable.
- No. of page = process size/page size; No. of frames = M/M size/frame size
- CPU generates Logical Memory Address(LA) and it is converted into Physical Memory Address(PA) which resides in M/M.

LA:

Page No.	Page Offset(Size)

PA:

Frame No.	Frame Offset(Size)

- Page Size = Frame Size
- CPU has no idea about page or frame. It will just request for the byte of a process from M/M.
- Page table is important to map pages into frames for MMU. Every process will have it's own page table.

  Example, Page table of P1 process from the earlier representation:

Page No.	**Frame No.**
0	f_2
1	f_4