## **Enrollment no:**

## KADI SARVA VISHWAVIDYALAYA LADRP INSTITUTE OF TECHNOLOGY AND RESEARCH GANDINAGAR DEPARTMENT OF ELECTRONICS AND COMMUNICATION B.E. 3<sup>RD</sup> SEMESTER

## MID SEMESTER EXAMINATION AUGUST-2014

Branch: EC Subject Code: EC-304 Subject Name: Digital Logic Design **Total Marks: 30** Time: 12.00 PM to 1.30 PM Date: 27/08/2014 **Instructions:**-All questions are compulsory. -Figures to the right indicate full marks. -Make suitable assumption, wherever necessary. Que.1 Answer the followings. Convert the decimal number 250.5 to base 3, base 8 and base 16. (03)(A) Implement function F=xyz+x'y+xyz' with only OR and NOT gates. (03)(B) Answer the following questions. Que.2 Perform the subtraction of 3570-2100 using 10's complement and 9's (06)(A) complement. Find out simplified expression of function in sum of products using k-map (06)(B) method. F = xy'z + xyz' + x'yz + xyzOR Perform the subtraction of following binary number using 2's complement and (06)(A) 1's complement. 11010-1101. (06)Simplify the following Boolean function by means of the tabulation method. (B)  $F(A,B,C,D,E,F,G) = \sum (20,28,38,39,52,60,102,103,127)$ Answer the following questions. Que.3 Explain full adder circuit with neat diagram. (04)(A) Write short note on JK flip-flop. (04)(B) Design a combinational circuit that accepts a three bit number and generates an (04)(C)output binary number equal to the square of the input number. Implement a full subtractor with two half subtractor and an OR gate. (04)(A) (04)Write short note on D flip-flop. (B) (04)(C)Show that NAND and NOR gates are universal gates.