# KADI SARVA VISHWAVIDHYALAYA

## B.E. Semester IV

**Subject Code: - EE-405** **Subject Name: - Digital Electronics**

**Date: - 29/10/2015** **Time: - 10:30a.m to 1:30 p.m** **Total Marks: - 70**

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**Instructions:**

1. Answer each section in separate Answer Sheet.
2. Use of scientific calculator is permitted.
3. All questions are **Compulsory.**
4. Indicate **clearly,** the options you attempt along with it's with respective question number.
5. Use the last page of main supplementary of **rough work.**

## Section – I

**Q.1** **(A)** Explain BCD to Seven Segment Decoder with logic Diagram and Truth Table. 5

**(B)** Explain Half Subtractor and Full Subtractor with logic diagram and Truth Table. 5

**(C)** Explain Master-Salve J-K Flip Flop with logic diagram and Truth Table. 5

**OR**

**(C)** Explain operation of Transistor Transistor Logic (TTL) with necessary diagram. 5

**Q.2** **(A)** Reduce the expression $\Sigma m\ (1, 5, 6, 12, 13, 14) + d\ (2, 4)$ and implement it in NOR logic. 5

**(B)** Do as directed: 5

1. $(1101.101)_2 + (111.011)_2$
2. $(5497)_{10}$ to $(\_\_\_\_\_)_2$
3. $(2A7C.30D)_{16} + (8D9.E8B)_{16}$
4. Multiply $(2A8)_{16}$ by $(B6)_{16}$
5. $(1011011101101110)_2$ to $(\_\_\_\_\_)_{10}$

**OR**

**(A)** Give application of decoders, multiplexer and de-multiplexer. 5

**(B)** What is the basic difference between synchronous and asynchronous counter? Explain four bit synchronous up counter. 5

**Q.3** **(A)** Explain 4-Input multiplexer with logic diagram and Truth Table. 5

**(B)** Explain X-OR and X-NOR gate with logic Symbol and truth table. 5

**OR**

**(A)** With suitable example explain binary addition, subtraction, and multiplication. 5

**(B)** Write short note on D-flip-flop. 5

## Section – II

**Q.4** **(A)** Define: **5**

(1) Propagation Delay Time
(2) Set-up Time
(3) Hold Time
(4) Maximum Clock Frequency
(5) Pulse Widths

**(B)** Explain 1-line to 8-line Demultiplexer with logic diagram and Truth Table. **5**

**(C)** Explain NOR gate as Universal Gate. **5**

**OR**

**(C)** What are SOP and POS forms of Boolean expressions? Explain three variables K-MAP **5**

**Q.5** **(A)** Explain Octal to Binary Encoder with logic diagram and Truth Table **5**

**(B)** State and Prove De Morgan's Theorems. **5**

**OR**

**(A)** Discuss the applications of flip-flops. **5**

**(B)** Classify the various modes of operation of shift registers. Explain the serial in parallel out Operation of shift register. **5**

**Q.6** **(A)** Explain Master-Salve S-R Flip Flop with logic diagram and Truth Table **5**

**(B)** Reduce the following using K-map: **5**

a. $\Sigma m$ (5,6,7,9,10,11,13,14,15)
b. $\Pi M$ (1,2,3,5,6,7,8,9,12,13)

**OR**

**(A)** Compare the CMOS and TTL logic. **5**

**(B)** Discuss 4-bit buffer register using D-flip flop. **5**

# KADI SARVA VISHWAVIDHYALAYA

## B.E. Semester IV

**Subject Code: - EE-405** **Subject Name: - Digital Electronics**

**Date: - 15/05/2014** **Time:- 10:30 to 1:30** **Total Marks:- 70**

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**Instructions:**

1. Answer each section in separate Answer Sheet.
2. Use of scientific calculator is permitted.
3. All questions are **Compulsory.**
4. Indicate **clearly,** the options you attempt along with it's with respective question number.
5. Use the last page of main supplementary of **rough work.**

## Section – I

**Q.1** **(A)** Write short note on Master-Salve S-R Flip Flop. **5**

**(B)** Explain Half Subtractor and Full Subtractor. **5**

**(C)** What is Decoder? Draw truth table and logic diagram of 3 to 8 line Decoder **5**

**OR**

**(C)** What are SOP and POS forms of Boolean expressions? Explain three variables K-MAP. **5**

**Q.2** **(A)** Explain binary addition, subtraction, and multiplication with example. **5**

**(B)** Define: **5**

(1)Propagation Delay Time
(2) Set-up Time
(3) Hold Time
(4) Maximum Clock Frequency
(5) Pulse Widths

**OR**

**(A)** Realize Exclusive OR gate using NAND logic and NOR logic. **5**

**(B)** State and explain the triggering methods for a J-K flip flop. **5**

**Q.3** **(A)** Discuss multiplexers with suitable diagram. **5**

**(B)** Reduce the expression $\sum m(1,5,6,12,13,14) + d(2,4)$ and implement it in NOR logic. **5**

**OR**

**(A)** Explain the Universal Gate and build up AND, OR and NOT using NAND and NOR gate. **5**

**(B)** Discuss the applications of flip-flops. **5**

## Section – II

Q.4 (A) Write short note on half adder and full adder. 5

(B) State and Prove De Morgan's Theorems. 5

(C) Explain Octal to Binary Encoder. 5

**OR**

(C) Classify the various modes of operation of shift registers. Explain the serial in parallel out operation of shift register. 5

Q.5 (A) Explain operation of JK flip flop using necessary schematic diagram and truth table. 5

(B) Write Short note On S-R Flip Flop. 5

**OR**

(A) Write short notes on Parallel in Serial out shift register. 5

(B) Explain operation of Transistor Transistor Logic (TTL) with necessary diagram 5

Q.6 (A) Explain BCD to Seven Segment Decoder with logic Diagram and Truth Table. 5

(B) Explain 1-line to 8-line Demultiplexer with logic diagram and Truth Table. 5

**OR**

(A) Compare the CMOS and TTL logic. . 5

(B) What is the basic difference between synchronous and asynchronous counter? Explain four bit synchronous up counter. 5

# KADI SARVA VISHWAVIDHYALAYA

## B.E. Semester IV

**Subject Code:- EE-405** **Subject Name: - Digital Electronics**

**Date:- 08/11/2014** **Time:- 10:30 to 1:30** **Total Marks:- 70**

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**Instructions:**

1. Answer each section in separate Answer Sheet.
2. Use of scientific calculator is permitted.
3. All questions are **Compulsory.**
4. Indicate **clearly,** the options you attempt along with it's with respective question number.
5. Use the last page of main supplementary of **rough work.**

## Section – I

**Q.1** **(A)** State and Prove De Morgan's Theorems. **5**

**(B)** Explain Half Subtractor and Full Subtractor with logic diagram and Truth Table **5**

**(C)** Write short note on Master-Salve S-R Flip Flop. **5**

**OR**

**(C)** Explain 4-Input multiplexer with logic diagram and Truth Table **5**

**Q.2** **(A)** Explain binary addition, subtraction, and multiplication with example. **5**

**(B)** What are SOP and POS forms of Boolean expressions? Explain three variables K-MAP. **5**

**OR**

**(A)** Explain X-OR and X-NOR gate with logic Symbol and truth table. **5**

**(B)** Draw the logic diagram and construct the truth table for each of the following expression. **5**

1. X= A+B+$\overline{CD}$
2. Y= (AB)($\overline{A+B}$)+ $\overline{EF}$

**Q.3** **(A)** Reduce the following Expression. **5**

1. (B+BC)(B+$\bar{B}$C)(B+D)
2. ($\overline{A+\overline{BC}}$)(A$\bar{B}$+ABC)

**(B)** Reduce the expression $\sum m(1,5,6,12,13,14) + d(2,4)$ and implement it in NOR logic. **5**

**OR**

**(A)** Show that X-OR gate is equivalent to A$\bar{B}$+$\bar{A}$B and construct the corresponding logic diagrams. **5**

**(B)** Discuss the applications of flip-flops. **5**

## Section – II

**Q.4** **(A)** Write Short note On S-R Flip Flop. **5**

**(B)** Do as directed: **5**

1. $(1101.101)_2 + (111.011)_2$
2. $(5497)_{10}$ to $(\_\_\_\_\_)_2$
3. $(2A7C.30D)_{16}+(8D9.E8B)_{16}$
4. Multiply $(2A8)_{16}$ by $(B6)_{16}$
5. $(1011011101101110)_2$ to $(\_\_\_\_\_)_{10}$

**(C)** Compare the CMOS and TTL logic. **5**

**OR**

**(C)** What is the basic difference between synchronous and asynchronous counter? Explain four bit synchronous up counter. **5**

**Q.5** **(A)** Explain Master-Salve J-K Flip Flop with logic diagram and Truth Table. **5**

**(B)** Define: **5**

(1)Propagation Delay Time
(2) Set-up Time
(3) Hold Time
(4) Maximum Clock Frequency
(5) Pulse Widths

**OR**

**(A)** Explain Octal to Binary Encoder with logic diagram and Truth Table **5**

**(B)** Explain 3-line to 8-line Decoder with logic diagram and Truth Table. **5**

**Q.6** **(A)** Explain BCD to Seven Segment Decoder with logic Diagram and Truth Table. **5**

**(B)** Explain operation of Transistor Transistor Logic (TTL) with necessary diagram. **5**

**OR**

**(A)** Explain 1-line to 8-line Demultiplexer with logic diagram and Truth Table. **5**

**(B)** Classify the various modes of operation of shift registers. Explain the serial in parallel out operation of shift register. **5**

# KADI SARVA VISHWAVIDHYALAYA

## B.E. SEMESTER IV EXAMINATION (MAY-2015)

**Subject Code: - EE-405** **Subject Name: - Digital Electronics**

**Date: - 07/05/2015** **Time: - 10:30 am to 1:30 pm** **Total Marks: - 70**

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**Instructions:**

1. Answer each section in separate Answer Sheet.
2. Use of scientific calculator is permitted.
3. All questions are **Compulsory.**
4. Indicate **clearly,** the options you attempt along with it's with respective question number.
5. Use the last page of main supplementary of **rough work.**

### Section – I

**Q.1** **(A)** Write short note on R-S Flip Flop. **5**

**(B)** Explain Half adder and Full Subtractor. **5**

**(C)** Draw truth table and logic diagram of 3 to 8 line Decoder. Give difference between Decoder And De-multiplexer. **5**

**OR**

**(C)** What are SOP and POS forms of Boolean expressions? Explain three variables K-MAP. **5**

**Q.2** **(A)** Explain binary addition, subtraction, and multiplication with example. **5**

**(B)** Prove that: **5**

1) $A + \bar{A}B = A + B$
2) $AB + \overline{AC} + A\bar{B}C(AB + C) = 1$
3) $ABCD + AB(\overline{CD}) + (\overline{AB})CD = AB + CD$
4) $A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$
5) Transposition Theorem

**OR**

**(A)** Implement Boolean expression for 2 input AND gate using NAND and NOR gate. **5**

**(B)** State and explain the triggering methods for a J-K flip flop. **5**

**Q.3** **(A)** Discuss multiplexers with suitable diagram. **5**

**(B)** Reduce the expression $\sum m(1,5,6,12,13,14) + d(2,4)$ and implement it in NOR logic. **5**

**OR**

**(A)** Using K-Map realize the following expression using minimum number of gates $Y = \bar{A}\,\bar{B}\,\bar{C}\,D + \bar{A}\,\bar{B}\,C\,D + \bar{A}\,B\,\bar{C}\,\bar{D} + \bar{A}\,B\,\bar{C}\,D + A\,\bar{B}\,\bar{C}\,D + \bar{A}\,B\,C\,D + A\,\bar{B}\,C\,D + A\,B\,\bar{C}\,D + A\,B\,C\,D$ **5**

**(B)** Write short note on D-flip-flop. **5**

## Section – II

Q.4 (A) Write short note on half subtractor and full adder. 5

(B) Explain the De-Morgan Theorem with necessary truth table. 5

(C) Explain Octal to Binary Encoder. 5

**OR**

(C) What is the basic difference between synchronous and asynchronous counter? Explain four bit synchronous up counter. 5

Q.5 (A) Explain operation of JK flip flop using necessary schematic diagram and truth table. 5

(B) Explain 1-line to 8-line De-multiplexer with logic diagram and Truth Table 5

**OR**

(A) Convert following decimal to binary 5

(1) 145 (2) 160

(B) Explain operation of Transistor Transistor Logic (TTL) with necessary diagram 5

Q.6 (A) Explain BCD to Seven Segment Decoder with logic Diagram and Truth Table. 5

(B) Write Short note On master slave S-R Flip Flop. 5

**OR**

(A) Compare the CMOS and TTL logic. 5

(B) State and explain the triggering methods for a T- Flip Flop. 5

**----------ALL THE BEST----------**