KADI SARVA VISHWAVIDYALAYA

B.E SEMESTER IV EXAMINATION (October - 2015)

SUBJECT CODE : CE/IT 403 SUBJECT NAME : Computer Organization and Architecture

DATE: 27/10/2015 TIME: 10.30 A.M. to 1.30 P.M. TOTAL MARKS: 70

Instructions:

1. Answer each section in separate Answer sheet.
2. Use of scientific Calculator is permitted.
3. Al Indicate **clearly**, the options you attempted along with its respective question number
4. Use the last page of main supplementary for rough work

SECTION 1

Q:1 (All Compulsory)

(A) Simplify the following Boolean Functions: 05

(a) $F(x,y,z) = \Sigma(0,2,4,5,6)$

(b) $F(x,y,z) = \Sigma(3,4,6,7)$

(B) Simplify the following Boolean function. 05

(a) x'z+x'y+xy'z+yz

(C) Explain full adder in detail. 05

OR

(C) Explain NAND and NOR as universal gates. 05

Q:2 (A) Simplify the Boolean Function by using the tabulation method

$F(A,B,C,D,E,F,G) = \Sigma(20,28,52,60)$ 05

(B) Explain RS Flip-Flop in Detail. 05

OR

(A) Simplify the Following Boolean Function: 05

(a) $F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10)$

(B) Explain De-Morgan's theorem in Detail. 05

Q:3 (A) With logic diagram explain the function of D flip-flop. 05

(B) What is high impedance state in three-state buffer? Explain Bus line with three – state buffer. 05

OR

(A) Reduce the number of states in the following state table and tabulate the reduced state table 05

Present state	Next state		output	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

Starting from State a of the reduced state table ,find the output sequence generated with an input sequence 01110010011.

(B) Draw and Explain Flow chart for interrupt cycle. 05

SECTION 2

Q:4 (All Compulsory)

(A) Explain Shift Micro-operations. 05

(B) Explain 4-bit Binary adder with necessary diagram. 05

(C) What is an instruction cycle? Draw its Flow chart. 05

OR

(C) List memory reference instructions and explain any one with example. 05

Q:5 (A) Explain the Common Bus System with its Diagram. 05

(B) Explain different types of addressing modes in detail. 05

OR

(A) Explain the first pass of assembler. 05

(B) Explain Instruction Pipeline in Detail. 05

Q:6 (A) Explain register stack and memory stack with block diagram. 05

(B) Define the following terms : 05

1. Program counter
2. Accumulator
3. Register Transfer Language
4. Micro operation
5. Opcode

OR

(A) List and explain functionalities of the basic computer registers and memory. 05

(B) Give the Comparisons between RISC and CISC. 05

KADI SARVA VISHWAVIDHYALAYA

B.E. (C.E./I.T.) SEMESTER-IV EXAMINATION (MAY/2014)

SUBJECT CODE: **CE/IT 403** SUBJECT NAME: **Computer Organization And Architecture**

DATE: 13/05/2014 **TIME: 10:30 a.m. to 1:30 p.m.** **TOTAL MARKS: 70**

Instructions:

1. Answer each section in separate Answer Sheet.
2. Use of scientific Calculator is permitted.
3. All questions are compulsory.
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of main supplementary for rough work.

SECTION-1

Q:1

(A) Explain with figures how NAND and NOR gate can be used as universal gate. [5]
(B) Give classification of logic families and compare CMOS and TTL families. [5]
(C) Design a 4 bit binary to BCD code converter. [5]

OR

(C) Draw the logic symbol and construct the truth table for each of the following gates. [5]

[1] 2-input NAND gate
[2] 3-input OR gate
[3] 3-input EX-NOR gate
[4] NOT gate

Q:2

(A) Simplify following Boolean function using K-Map . [5]
$F(w,x,y,z) = \sum (1,3,7,11, 15)$
$d(w,x,y,z) = \sum (0,2,5)$
(B) Simplify following Boolean function using tabulation method and draw the logic Diagram . [5]
$F(w,x,y,z) = \sum (0,1,2,8,10,11,14,15)$

OR

(A) Design the Combinational circuit for Binary to Gray code conversion [5]
(B) Design a Combinational circuit for a full adder. [5]

Q:3

(A) Design a combinational circuit whose input is 4 bit number and whose output is 2's complement of the input number. [5]
(B) Explain working of Master Slave J K flip-flop. [5]

P.T.O.

OR

(A) Simplify following Boolean functions to a minimum number of literals. [5]
(1) xyz + x'y + xyz'
(2) (A+B)'(A'+B')'
(B) Explain 4 bit binary Ripple Counters. [5]

SECTION-2

Q:4

(A) Explain common bus system with neat diagram. [5]
(B) Explain following instructions. [5]
BSA, CIR, SZE, SZA, LDA
(C) Explain different addressing modes with suitable example. [5]

OR

(C) Explain instruction pipelining with example. [5]

Q:5

(A) Define following terms. [5]
(1) Effective address
(2) Immediate Instruction
(3) Register Transfer Language
(4) Computer Organization
(5) Pseudo instruction
(B) Explain 4 bit incrementer with necessary diagram. [5]

OR

(A) Write a note on Subroutine. [5]
(B) Explain direct and indirect addressing mode. [5]

Q:6

(A) Explain the first pass of an Assembler with a flowchart. [5]
(B) Explain register stack and memory stack with suitable example. [5]

OR

(A) List important characteristics of RISC architecture and explain the use of overlapped Register window. [5]
(B) List and explain different types of shift micro operations. [5]

----------**ALL THE BEST**----------

KADI SARVA VISHVA VIDHYALAYA

B.E. (C.E./I.T.) SEMESTER-IV EXAMINATION (NOVEMBER/2014)

SUBJECT CODE: **CE/IT 403** SUBJECT NAME: **Computer Organization and Architecture**

DATE: 5/11/2014 **TIME: 10:30 TO 1:30** **TOTAL MARKS:70**

Instructions:

1. Answer each section in separate Answer Sheet.
2. Use of scientific Calculator is permitted.
3. All questions are compulsory.
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of main supplementary for rough work.

SECTION-1

Q:1

(A) Simplify the following Boolean functions to a minimum numbers of literals. (a) xyz+xy+xyz' and (b) (A+B)'(A'+B')' [5]

(B) Obtain the truth table of the function F= xy+xy'+y'z [5]

(C) Design a 4 bit BCD to binary code converter. [5]

OR

(C) Draw the logic symbol and construct the truth table for each of the following gates. [5]

[1] 2-input NAND gate
[2] 3-input OR gate
[3] 3-input EX-NOR gate
[4] NOT gate

Q:2

(A) Using K-map find the Boolean function and its complement for the following: $F(A,B,C,D) = \sum(1,2,3,4,6,8,9,10,11,12,14)$ [5]

(B) Derive Boolean function using Tabulation Method for the following: $F(P,Q,R,S) = \sum(0,1,3,4,5,7,10,13,14,15)$ [5]

OR

(A) Write a note on Master-Slave Flip-Flop. [5]

(B) Design a combination circuits for a full adder. [5]

Q:3

(A) Explain NAND and NOR as an universal gates [5]

(B) Design a combinational circuit whose input is four bit binary number and output is the 2's complement of the input binary number. [5]

P.T.O.

OR

(A) Simplify the Boolean function:

(1) F = A'B'C'+B'CD'+A'BCD'+AB'C'

(2) F =A'B'D'+A'CD+A'BC

(3) d=A'BC'D+ACD+AB'D' Where "d " indicates Don't care conditions. [5]

(B) Attempt following:

1. Covert into Sum-of-Minterms : A' + B + CA
2. Covert into Product-of-Maxtems : A(A'+B)(C') [5]

SECTION-2

Q:1

(A) Design and Explain Common bus system using Multiplexer [5]

(B) Draw and explain first pass assembler. [5]

(C) Write short note on subroutines [5]

OR

(C) Draw and explain the 4-bit binary adder-subtractor circuit. [5]

Q:2

(A) Define register transfer language. Draw and explain the block diagram for transfer of data from R1 to R2 when control p = 1. [5]

(B) Explain 4 bit incrementer with necessary diagram. [5]

OR

(A) List memory reference instructions and explain any one with example. [5]

(B) Explain direct and indirect addressing mode. [5]

Q:3

(A) Define following terms. Any five. 1.RTL 2.Micro-operation 3.Accumulator 4.Interrupt 5.Parallel processing 6.Assembler. [5]

(B) Explain Stack Organization of a computer system. Explain push and pop operations on register stack. [5]

OR

(A) Differentiate RISC and CISC [5]

(B) List and explain different types of shift micro operations. [5]

----------ALL THE BEST----------

KADI SARVA VISHWAVIDHYALAYA

B.E. Semester IV Examination – April – 2015

CE 403 / IT 403 – COMPUTER ORGANIZATION AND ARCHITECTURE

DATE: 2/05/2015 **TIME: 10.30 AM to 1.30 PM** **TOTAL MARKS: 70**

Instructions:

1. Answer each section in separate answer sheet.
2. Use of scientific calculator is permitted.
3. All questions are **Compulsory**.
4. Indicate **clearly**, the options you attempt along with its respective question number.
5. Use the last page of main supplementary for **rough work**.

SECTION – I

Q-1 A Answer the following in short. 10

1 Draw the logic diagram for following Boolean function using NOR gates only.
F=AB'+B'C'+A'C'

2 Explain the Full Adder using circuit diagram and truth table.

Q-1 B Simplify the following Boolean function using K-Map and also draw the circuit diagram for the simplified expression. 5
F= XYZ+X'Y'Z+X'Y'Z', DON'T CARES XY'Z+XYZ'.

OR

Q-1 B Simplify the following Boolean function using K-Map and also draw the circuit diagram for the simplified expression. 5
F= XY'Z'+X'Y'Z', DON'T CARES X'YZ'+XYZ'.

Q-2 A Explain Half Subtractor. 5

Q-2 B Explain basic RS flip-flop and derive its characteristics. 5

OR

Q-2 A Simplify the following Boolean function using K-Map: 5
F(A,B,C,D)=∑(0,2,6,7,10,11,12,14)

Q-2 B Explain state table and state diagram with an example. 5

Q-3 A Draw and explain flow chart for memory reference instruction. 5

Q-3 B Express the Boolean function F=A+B'C in a Sum of Minterms and Product of Maxterms. 5

OR

Q-3 A Justify the following : 5
(i) $(A \oplus B)' = (A \odot B)$ (ii) (A+B+C)'=A'B'C'

Q-3 B Design BCD counter using D flip-flop. 5

SECTION – II

Q-4 A	Answer the following in short.	10
1	Differentiate RISC and CISC.	
2	Explain register stack and memory stack with block diagram.	
Q-4 B	Design 3 bit binary synchronous down counter using JK flip flops.	5
	OR	
Q-4 B	Design 2 bit binary synchronous up counter using RS flip flops.	5
Q-5 A	Simplify the following Boolean function by using the tabulation method: $F= \sum(0,1,2,8,10,11,14,15)$	5
Q-5 B	Explain Bus system for four register.	5
	OR	
Q-5 A	List out different Logic and Shift micro operations with an example.	5
Q-5 B	Explain RISC Pipelining.	5
Q-6 A	Explain different Instruction formats.	5
Q-6 B	Explain functionality of assembler in detail.	5
	OR	
Q-6 A	Explain 2 stage Instruction Pipeline with diagram.	5
Q-6 B	Explain Accumulator.	5