Enrolment No:

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LDRP INSTITUTE OF TECHNOLOGY AND RESEARCH, GANDHINAGAR
DEPARTMENT OF ELECTRONICS AND COMMUNICATION
B.E. 5th SEMESTER
MID SEMESTER EXAMINATION AUGUST-2014

Subject Code: EC-506 **Branch: EC**
Subject : VLSI Technology and Design **Total Marks: 30**
Date : 30th August 2014 **Time: 08.30 to 10.00 AM**

Instructions: - All questions are compulsory.
- Figures to the right indicate full marks.
- Make suitable assumption, wherever necessary.

Que. 1 **Answer the following questions.** **(06)**

A) Write a Program in VHDL
1) Design a Full Adder using Half Adder. (Using **Structural** Modeling).
2) Design All Logic Gates using selection line. (Using **Behavioral** Modeling).

Que. 2 **Answer the following questions.** **(12)**

A) Discuss VLSI design flow in detail.
B) Draw lithography steps to fabricate N- MOS in detail.

OR

Que. 2 **Answer the following questions.** **(12)**

A) Justify Modularity, Locality and Regularity with example.
B) Draw DC model of MOSFET capacitance and explain oxide-related capacitances.

Que. 3 **Answer the following questions.** **(12)**

A) Calculate the threshold voltage for a polysilicon gate nMOS transistor with the following parameters: $N_A = 2 \times 10^{16}$ cm^{-3}, $N_D = 2 \times 10^{19}$ cm^{-3}, $t_{ox} = 300 \times 10^{-8}$ cm, and $N_{ox} = 10^{10}$ cm^{-2}. Take kT/q = 26 mV, $n_i = 1.45 \times 10^{10}$ cm^{-3}, q = 1.6×10^{-19} C, $\varepsilon_{ox} = 3.97 \times 8.85 \times 10^{-14}$ F/cm, $\varepsilon_{si} = 11.7 \times 8.85 \times 10^{-14}$ F/cm.
B) Explain Band Diagram of the MOS structure, at surface Inversion. Derive the expression of Threshold Voltage.

OR

Que. 3 **Answer the following questions.** **(12)**

A) With neat sketch explain gradual channel approximation and derive the equation for drain current in linear region mode.
B) Comparison between Constant-Field Scaling and Constant-Voltage Scaling.

*****Best of Luck*****