KADI SARVA VISHWAVIDHYALAYA

BE Semester V Electronics & Communication Dept.

Examination – 2016

Sub code: EC 506 **Sub Name: VLSI Technology**
Date: 22/11/2016 **Time: 10:30am to 01:30pm**
Total Marks: 70

Instructions:

1. Answer Each Section in Separate Answer sheet.
2. Use of Scientific Calculator is permitted. .
3. All questions are separate
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1 (a)	Explain Full custom and semi custom in detail.	[05]
(b)	Explain VLSI design flow in detail.	[05]
(c)	Explain the concepts of Regularity and Locality with example.	[05]
	OR	
(c)	Explain Gate Array in detail.	[05]
Q.2 (a)	What is Lithography? Explain all the steps of lithography for n-MOSFET.	[05]
(b)	Draw and explain energy band diagram of the combined MOS system.	[05]
	OR	
Q.2 (a)	What is scaling? Explain any one type of scaling in detail.	[05]
(b)	Explain LOCOS technique in detail.	[05]
Q-3 (a)	Explain Gradual channel Approximation.	[05]
(b)	Define Noise Immunity and Noise Margins.	[05]
	OR	
Q-3 (a)	Explain operation of MOSFET with current equations.	[05]
(b)	Draw and explain VI characteristic of CMOS inverter with all regions.	[05]

SECTION II

Q.4 (a)	Define : 1. Transmission gate 2. CPL	**[05]**
(b)	Explain FPGA in detail.	**[05]**
(c)	Write a program of Full Adder with structural style using VHDL.	**[05]**
	OR	
(c)	Write program of NAND gate using structural style using VHDL.	**[05]**
Q.5 (a)	Consider a resistive – load inverter circuit with VDD = 5V,k'n=20μA/V^2 ,Vto=0.8V,R_L= 200kΩ,and W/L=2.Calculate the critical voltages V_{OL},V_{OH},V_{IL},V_{IH}.	**[05]**
(b)	Explain stick diagram with advantage of Euler path.	**[05]**
	OR	
Q.5 (a)	Calculate the equivalent W/L ratio of nMOS and pMOS with (W/L)n=10 and (W/L)p=15 for the Z=((D+E+A)(B+C))'.	**[05]**
(b)	Explain two input CMOS NOR gate in detail with $(W/L)_{eq}$ equation for n inputs.	**[05]**
Q-6 (a)	Explain CMOS D Latch in detail.	**[05]**
(b)	Write a program of 1 bit comparator using VHDL.	**[05]**
	OR	
Q-6(a)	Explain clocked SR Latch in detail.	**[05]**
(b)	Write a program of 4 × 1 MUX using VHDL.	**[05]**

KADI SARVA VISHWAVIDHYALAYA

BE 5th Semester Electronics & Communication Dept.

Examination –November 2015

Sub code: EC- 506 **Sub Name: VLSI Technology and Design**

Date: 30 /11/2015 **Time: 10:30am to 01:30pm** **Total Marks:70**

Instructions:

1. Answer Each Section in Separate Answer sheet.
2. Use of Scientific Calculator is permitted.
3. All questions are separate
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1	(a)	Explain following terms: (i) Yield (ii) Manufacturability (iii) Standard Cell based Design	[05]
	(b)	Discuss VLSI design flow in brief. (Y – chart)	[05]
	(c)	Discuss different device isolation techniques for MOS Transistor.	[05]
		OR	
	(c)	Explain Channel Length Modulation.	[05]
Q.2	(a)	Explain design and analysis of CMOS two input NOR Gate.	[05]
	(b)	Explain CMOS Transmission Gate in Detail.	[05]
		OR	
Q.2	(a)	Explain Concept of Regularity, Modularity and Locality.	[05]
	(b)	Discuss Scan based Techniques for Testing.	[05]
Q-3	(a)	Discuss Layout Design Rules.	[05]
	(b)	Explain the working of MOS system under external Bias.	[05]
		OR	
Q-3	(a)	Draw and explain transistor level implementation of clocked NOR based SR latch circuit.	[05]
	(b)	Explain design procedure steps for fabrications of n-MOS transistor	[05]

SECTION II

Q.4 (a)	List the important concern for the IC packaging technology. Also Explain different packaging technologies.	[05]
(b)	Explain the functioning of depletion load nMOS inverter and derive critical voltage points VOH, VOL, VIL and VIH.	[05]
(c)	Write a short note on Built In Self Test (BIST).	[05]
	OR	
(c)	Discuss basic steps of the LOCOS Process.	[05]
Q.5 (a)	Explain concurrent and non-concurrent statement in VHDL with suitable examples.	[05]
(b)	Write a 4*1 multiplexer programme using structural modelling.	[05]
	OR	
Q.5 (a)	Write a programme a for D flip flop and D latch using process block.	[05]
(b)	Explain PLA and PAL architecture in details.	[05]
Q-6 (a)	Explain details architecture of CPLD.	[05]
(b)	Write a programme for traffic control using FSM(finite state machine).	[05]
	OR	
Q-6(a)	Write a programme for a ripple counter using behavior modeling.	[05]
(b)	Write a programme for and gate using data flow modeling and also write a test bench for the programme.	[05]

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KADI SARVA VISHWAVIDYALAYA
B.E.SEMESTER 5TH EXAMINATION NOVEMBER-2014

SUBJECT CODE: EC - 506
SUBJECT NAME : VLSI Technology & Design
DATE: 24/11/2014 TIME: 10.30 AM To 01.30 PM TOTAL MARKS: 70

Instructions:
1. Answer Each Section in Separate Answer sheet.
2. Use of Scientific Calculator is permitted.
3. All questions are compulsory.
4. Indicate **clearly**, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION-1

Q – 1(A)	Explain Y – chart of design flow in detail.	(7)
(B)	Explain concept of regularity, modularity and locality.	(3)
(C)	Explain LOCOS in detail.	(5)
	OR	
(C)	Explain layout design rules.	(5)
Q – 2(A)	Explain MOS system under external bias with energy band diagram	(7)
(B)	Explain operation of MOSFET in brief.	(3)
	OR	
Q – 2(A)	Explain gradual channel approximation method.	(7)
(B)	Explain constant field scaling in brief.	(3)
Q – 3(A)	Explain resistive load inverter with calculation of V_{OH}, V_{OL}, V_{IL} and V_{IH}.	(7)
(B)	Explain short channel effect in brief.	(3)
	OR	
Q – 3(A)	Explain CMOSinverter with calculation of V_{IH}, V_{IL},and V_{TH}.	(7)
(B)	Explain CMOS ring oscillator circuit in brief.	(3)

SECTION-2

Q – 4(A)	Draw and explain circuit of NAND2 gate using CMOS.	(7)
(B)	Explain pseudo – nMOS logic with example.	(3)
(C)	Explain clocked JK latch circuit in circuit.	(5)
	OR	
(C)	Draw and explain CMOS SR latch in detail.	(5)
Q – 5(A)	Explain Behavioral style of modeling with example.	(7)
(B)	Short note on finite state machine.	(3)
	OR	
Q – 5(A)	Explain structural style of modeling with example.	(7)
(B)	Difference between concurrent and sequential method.	(3)
Q –6(A)	Explain structure of FPGA in Detail.	(7)
(B)	Write down VHDL program for half adder using data flow method.	(3)
	OR	
Q – 6(A)	Explain structure of CPLD in detail.	(7)
(B)	Write down VHDL program for 2*1 mux using data flow method.	(3)

----------ALL THE BEST ---------

KADI SARVA VISHWAVIDYALAYA
B.E. SEMESTER 5TH EXAMINATION APRIL-2015

SUBJECT CODE: EC-506 **SUBJECT NAME : VLSI Technology & Design**
DATE: 25/04/2015 **TIME: 10.30 AM To 01.30 PM** **TOTAL MARKS: 70**

Instructions:

1. Answer each section in separate Answer Sheet.
2. Use of Scientific Calculator is permitted.
3. All questions are compulsory.
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of main supplementary for rough work.

SECTION-I

Q.1	(A)	Explain a Metal Oxide Semiconductor (MOS) structure in detail.	[05]
	(B)	Draw VLSI design flow and explain.	[05]
	(C)	Explain Junction Capacitances.	[05]
		OR	
	(C)	Explain Oxide related Capacitances.	[05]
Q.2	(A)	What is threshold voltage? Draw band diagram of MOS Structure at surface inversion.	[05]
	(B)	Explain Layout Design rules in detail.	[05]
		OR	
Q.2	(A)	Derive the expression of Threshold Voltage.	[05]
	(B)	Discuss process flow for the fabrication of an n-type MOSFET on p-type silicon.	[05]
Q-3	(A)	Consider a CMOS Inverter circuit with the following parameters: V_{DD}=3.3V, $V_{TO,n}$=0.6V, $V_{TO,p}$= - 0.7V, k_n=200 μA/V², k_p=80 μA/V² Calculate the noise margin of the circuit.	[07]
	(B)	Justify Regularity, Modularity and Locality.	[03]
		OR	
Q-3	(A)	Draw circuit of CMOS inverter and explain its function.	[05]
	(B)	Comparison between Enhancement type MOSFET and Depletion type MOSFET.	[05]

SECTION-II

Q.4	(A)	Difference between Structural and Behavioral modeling.	[05]
	(B)	Explain types of programmable logic device.	[05]
	(C)	Explain Data flow modeling with example.	[05]
		OR	
	(C)	Explain the features of Hardware Description Language.	[05]

Q.5	**(A)**	What is latch? Explain CMOS D-latch.	**[05]**
	(B)	Implement following Boolean functions using transmission gates.	**[05]**

$F= \overline{B}C+\overline{B}A+B\overline{C}A$

OR

Q.5	**(A)**	Explain SR latch circuit in detail.	**[05]**
	(B)	Draw circuit of Resistive load Inverter.	**[05]**
Q-6	**(A)**	Design 8:1 Multiplexer using VHDL.(Using Data Flow modeling)	**[05]**
	(B)	Explain CMOS Transmission Gates (TGs).	**[05]**

OR

Q-6	**(A)**	Design 4-bit Comparator using VHDL	**[05]**
	(B)	Comparison between FPGA and CPLD.	**[05]**

-----All The Best-----