



## 1. Description

### 1.1. Project

Project Name	ui
Board Name	custom
Generated with:	STM32CubeMX 6.8.0
Date	11/26/2024

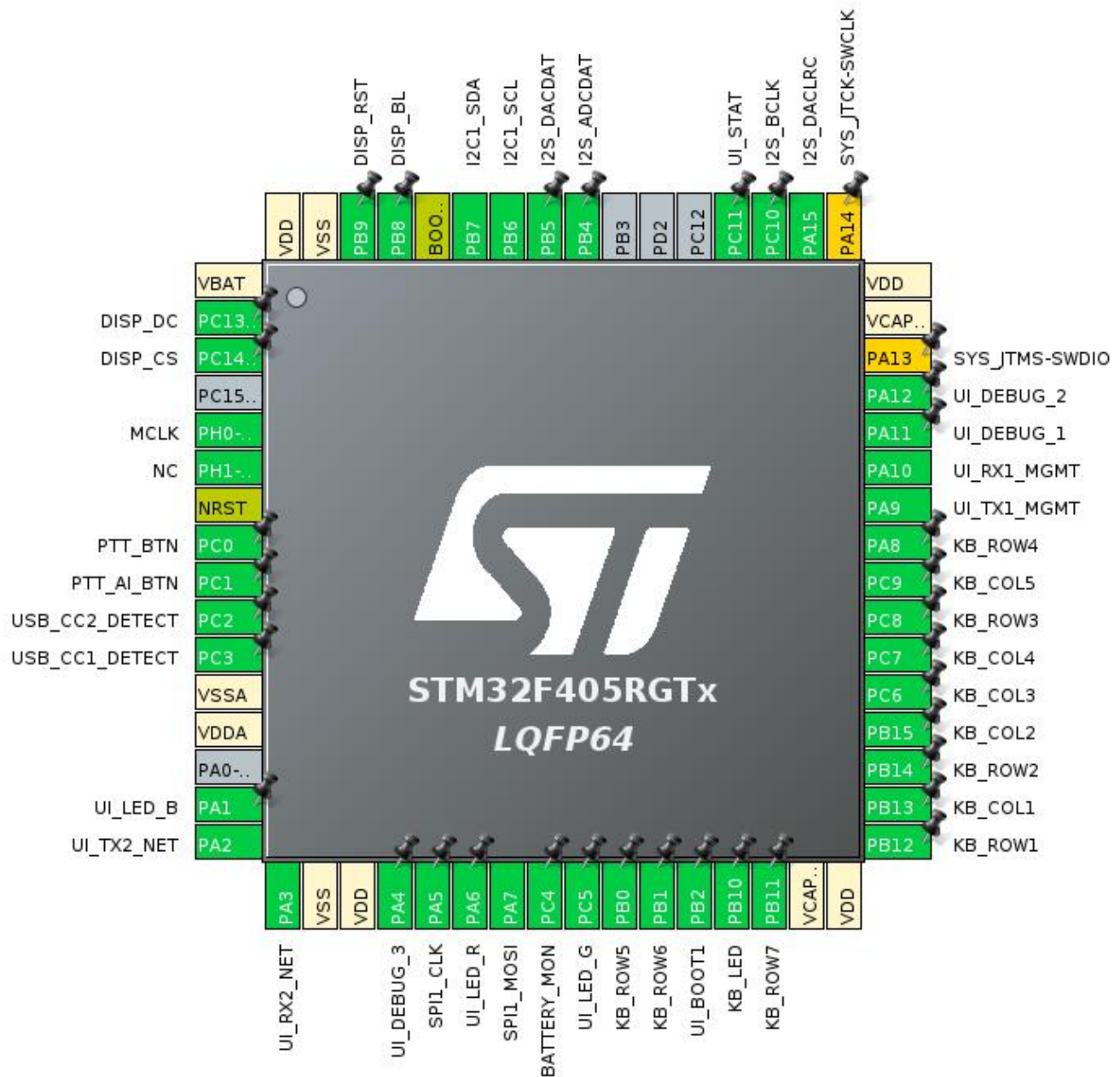
### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



### 3. Pins Configuration

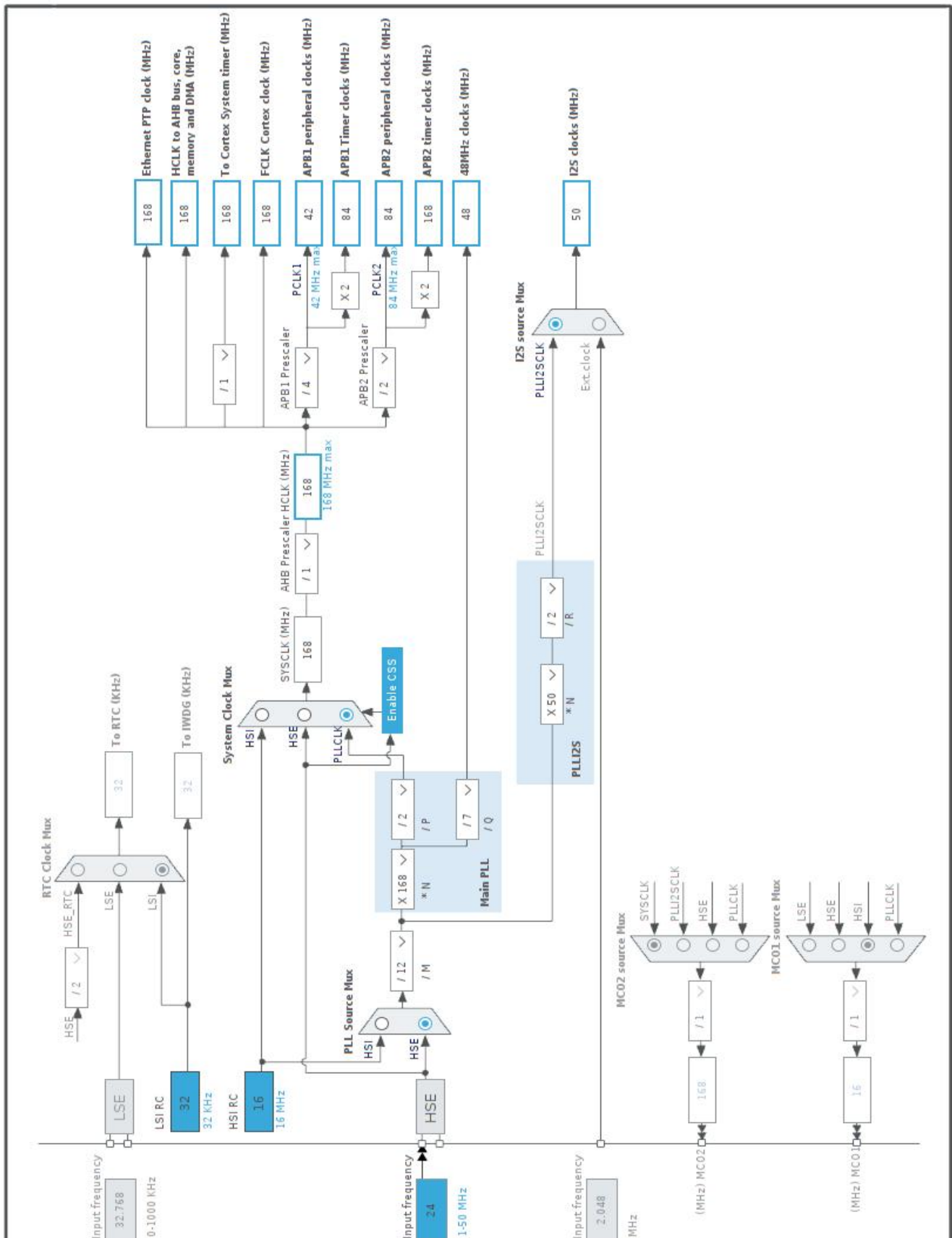
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP *	I/O	GPIO_Output	DISP_DC
3	PC14-OSC32_IN *	I/O	GPIO_Output	DISP_CS
5	PH0-OSC_IN	I/O	RCC_OSC_IN	MCLK
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	NC
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	PTT_BTN
9	PC1 *	I/O	GPIO_Input	PTT_AI_BTN
10	PC2	I/O	ADC1_IN12	USB_CC2_DETECT
11	PC3	I/O	ADC1_IN13	USB_CC1_DETECT
12	VSSA	Power		
13	VDDA	Power		
15	PA1 *	I/O	GPIO_Output	UI_LED_B
16	PA2	I/O	USART2_TX	UI_TX2_NET
17	PA3	I/O	USART2_RX	UI_RX2_NET
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	UI_DEBUG_3
21	PA5	I/O	SPI1_SCK	SPI1_CLK
22	PA6 *	I/O	GPIO_Output	UI_LED_R
23	PA7	I/O	SPI1_MOSI	SPI1_MOSI
24	PC4	I/O	ADC1_IN14	BATTERY_MON
25	PC5 *	I/O	GPIO_Output	UI_LED_G
26	PB0 *	I/O	GPIO_Input	KB_ROW5
27	PB1 *	I/O	GPIO_Input	KB_ROW6
28	PB2 *	I/O	GPIO_Input	UI_BOOT1
29	PB10 *	I/O	GPIO_Output	KB_LED
30	PB11 *	I/O	GPIO_Input	KB_ROW7
31	VCAP_1	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Input	KB_ROW1
34	PB13 *	I/O	GPIO_Output	KB_COL1
35	PB14 *	I/O	GPIO_Input	KB_ROW2
36	PB15 *	I/O	GPIO_Output	KB_COL2
37	PC6 *	I/O	GPIO_Output	KB_COL3
38	PC7 *	I/O	GPIO_Output	KB_COL4

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PC8 *	I/O	GPIO_Input	KB_ROW3
40	PC9 *	I/O	GPIO_Output	KB_COL5
41	PA8 *	I/O	GPIO_Input	KB_ROW4
42	PA9	I/O	USART1_TX	UI_TX1_MGMT
43	PA10	I/O	USART1_RX	UI_RX1_MGMT
44	PA11 *	I/O	GPIO_Output	UI_DEBUG_1
45	PA12 *	I/O	GPIO_Output	UI_DEBUG_2
46	PA13 **	I/O	SYS_JTMS-SWDIO	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14 **	I/O	SYS_JTCK-SWCLK	
50	PA15	I/O	I2S3_WS	I2S_DACLRC
51	PC10	I/O	I2S3_CK	I2S_BCLK
52	PC11 *	I/O	GPIO_Input	UI_STAT
56	PB4	I/O	I2S3_ext_SD	I2S_ADCDAT
57	PB5	I/O	I2S3_SD	I2S_DACDAT
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	I2C1_SDA	
60	BOOT0	Boot		
61	PB8 *	I/O	GPIO_Output	DISP_BL
62	PB9 *	I/O	GPIO_Output	DISP_RST
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

\*\* The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	ui
Project Folder	/media/brett/cisco/code/hactar/firmware/ui
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_I2C1_Init	I2C1
6	MX_I2S3_Init	I2S3
7	MX_SPI1_Init	SPI1
8	MX_USART1_UART_Init	USART1
9	MX_USART2_UART_Init	USART2
10	MX_TIM2_Init	TIM2
11	MX_RNG_Init	RNG

Rank	Function Name	Peripheral Instance Name
12	MX_CRC_Init	CRC
13	MX_TIM3_Init	TIM3



## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	DS8626_Rev8

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

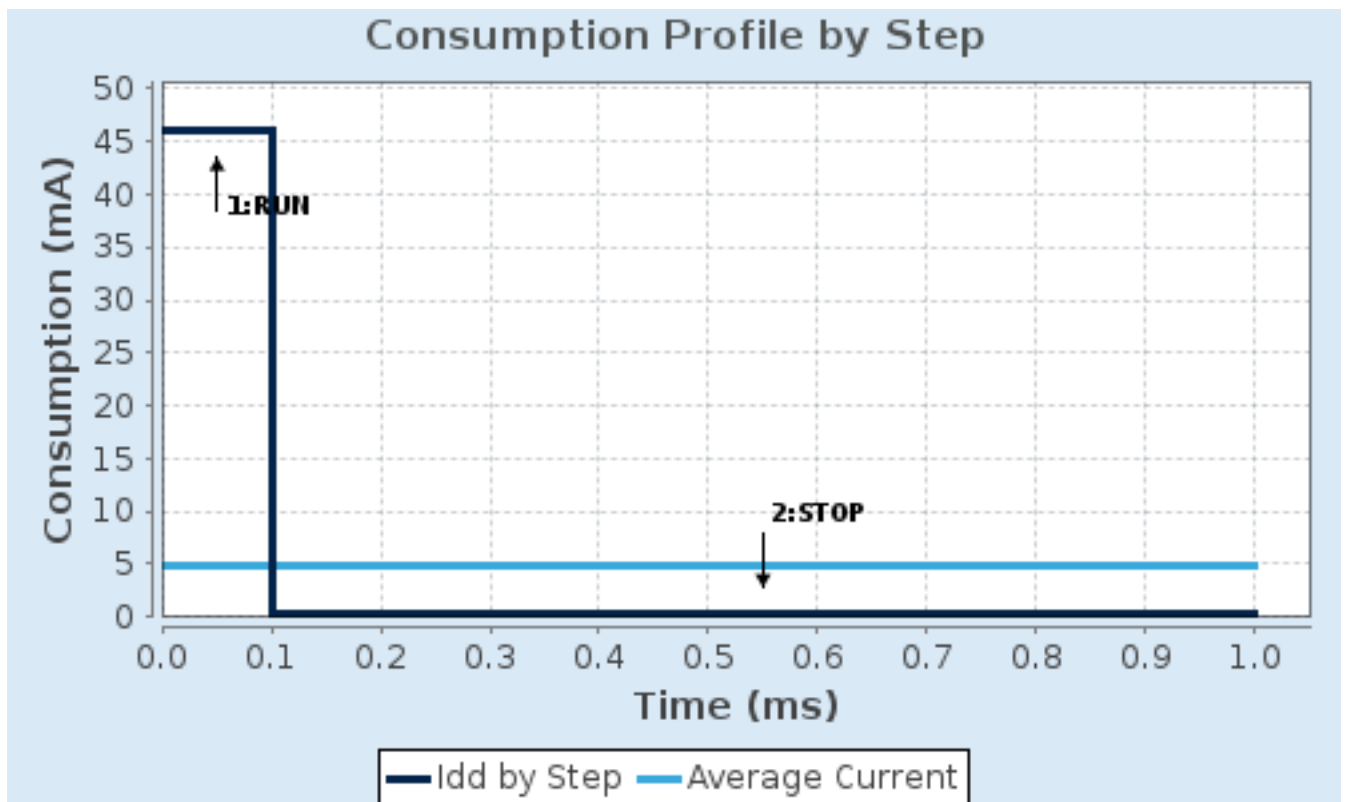
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	168 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	46 mA	280 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	210.0	0.0
<b>Ta Max</b>	98.02	104.96
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

#### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

mode: IN12

mode: IN13

mode: IN14

#### 7.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode	Independent mode
<b>ADC_Settings:</b>	
Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

##### **ADC\_Regular\_ConversionMode:**

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 12
Sampling Time	3 Cycles

##### **ADC\_Injected\_ConversionMode:**

Number Of Conversions	0
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##### **WatchDog:**

Enable Analog WatchDog Mode	false
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### 7.2. CRC

mode: Activated

### 7.3. I2C1

I2C: I2C

#### 7.3.1. Parameter Settings:

**Master Features:**

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

**Slave Features:**

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

## 7.4. I2S3

**Mode: Full-Duplex Slave****7.4.1. Parameter Settings:****Generic Parameters:**

Transmission Mode	Mode Slave Transmit
Communication Standard	I2S Philips
Data and Frame Format	<b>16 Bits Data on 32 Bits Frame *</b>
Selected Audio Frequency	<b>16 KHz *</b>
Real Audio Frequency	<b>15.943 KHz *</b>
Error between Selected and Real	<b>-0.35 % *</b>

**Clock Parameters:**

Clock Source	I2S PLL Clock
Clock Polarity	Low

## 7.5. RCC

**High Speed Clock (HSE): BYPASS Clock Source****7.5.1. Parameter Settings:****System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

**Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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**7.6. RNG**

**mode: Activated**

**7.7. SPI1**

**Mode: Half-Duplex Master**

**7.7.1. Parameter Settings:****Basic Parameters:**

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>42.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSS Signal Type	Software

**7.8. SYS**

**Timebase Source: SysTick**

**7.9. TIM2**

**Clock Source : Internal Clock**

**7.9.1. Parameter Settings:****Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>1600 *</b>
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Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	<b>100 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
<b>Trigger Output (TRGO) Parameters:</b>	
Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

## 7.10. TIM3

### Clock Source : Internal Clock

#### 7.10.1. Parameter Settings:

<b>Counter Settings:</b>	
Prescaler (PSC - 16 bits value)	<b>16 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>999 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
<b>Trigger Output (TRGO) Parameters:</b>	
Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

## 7.11. USART1

### Mode: Asynchronous

#### 7.11.1. Parameter Settings:

<b>Basic Parameters:</b>	
Baud Rate	115200
Word Length	<b>9 Bits (including Parity) *</b>
Parity	<b>Even *</b>
Stop Bits	1
<b>Advanced Parameters:</b>	
Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.12. USART2

**Mode: Asynchronous**

### 7.12.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	<b>921600 *</b>
Word Length	<b>9 Bits (including Parity) *</b>
Parity	<b>Even *</b>
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

**\* User modified value**



## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	USB_CC2_DETECT
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	USB_CC1_DETECT
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	BATTERY_MON
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
I2S3	PA15	I2S3_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S_DACLRC
	PC10	I2S3_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S_BCLK
	PB4	I2S3_ext_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S_ADCDAT
	PB5	I2S3_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S_DACDAT
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCLK
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	NC
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPI1_CLK
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPI1_MOSI
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	UI_TX1_MGMT
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	UI_RX1_MGMT
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	UI_TX2_NET
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	UI_RX2_NET
Single Mapped Signals	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
GPIO	PC13-ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_DC
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_CS
	PC0	GPIO_Input	Input mode	Pull-up *	n/a	PTT_BTN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC1	GPIO_Input	Input mode	<b>Pull-up *</b>	n/a	PTT_AI_BTN
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_LED_B
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_DEBUG_3
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_LED_R
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_LED_G
	PB0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KB_ROW5
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KB_ROW6
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UI_BOOT1
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KB_LED
	PB11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KB_ROW7
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KB_ROW1
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KB_COL1
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KB_ROW2
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KB_COL2
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KB_COL3
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KB_COL4
	PC8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KB_ROW3
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KB_COL5
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KB_ROW4
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_DEBUG_1
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_DEBUG_2
	PC11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UI_STAT
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_BL
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_RST

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_RX	DMA1_Stream5	Peripheral To Memory	<b>Very High *</b>
USART2_TX	DMA1_Stream6	Memory To Peripheral	<b>Very High *</b>
USART1_RX	DMA2_Stream5	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
SPI1_TX	DMA2_Stream3	Memory To Peripheral	Low
SPI3_TX	DMA1_Stream7	Memory To Peripheral	<b>Very High *</b>
I2S3_EXT_RX	DMA1_Stream0	Peripheral To Memory	<b>Very High *</b>

### USART2\_RX: DMA1\_Stream5 DMA request Settings:

Mode: **Circular \***  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Byte  
 Memory Data Width: Byte

### USART2\_TX: DMA1\_Stream6 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Byte  
 Memory Data Width: Byte

### USART1\_RX: DMA2\_Stream5 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Byte  
 Memory Data Width: Byte

USART1\_TX: DMA2\_Stream7 DMA request Settings:

Mode: Normal  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

SPI1\_TX: DMA2\_Stream3 DMA request Settings:

Mode: Normal  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

SPI3\_TX: DMA1\_Stream7 DMA request Settings:

Mode: **Circular \***  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: **Half Word \***  
Memory Data Width: **Half Word \***

I2S3\_EXT\_RX: DMA1\_Stream0 DMA request Settings:

Mode: **Circular \***  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: **Half Word \***  
Memory Data Width: **Half Word \***

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
RCC global interrupt	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	1	0
DMA1 stream6 global interrupt	true	1	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	10	0
SPI1 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	0	0
SPI3 global interrupt	true	0	0
DMA2 stream3 global interrupt	true	0	0
DMA2 stream5 global interrupt	true	1	0
DMA2 stream7 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
RCC global interrupt	false	true	false
DMA1 stream0 global interrupt	false	true	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
SPI1 global interrupt	false	true	true
USART1 global interrupt	false	true	true
USART2 global interrupt	false	true	true
DMA1 stream7 global interrupt	false	true	true
SPI3 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true
DMA2 stream5 global interrupt	false	true	true
DMA2 stream7 global interrupt	false	true	true

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓	ADC1 ✓	TIM2 ✓	I2C1 ✓	I2S3 ✓	RNG ✓	CRC ✓
GPIO ⚠		TIM3 ✓	SPI1 ✓			
NVIC ✓			USART1 ✓			
RCC ✓			USART2 ✓			
SYS ✓						

## 10. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32f4_svd.zip">https://www.st.com/resource/en/svd/stm32f4_svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstmcsuite.pdf">https://www.st.com/resource/en/flyer/flstmcsuite.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
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