

The following pins must be stable at boot:

- PA9/PA10: input/output usart2
- PB6/PB7: input/output for I2C
- PA11/PA12: input/output for USB

The schematic diagram illustrates the connection of a WM8960CEFL/RV audio codec to a Raspberry Pi 3B+. The codec is represented by a yellow-shaded component with pins numbered 1 through 28. The Raspberry Pi's pins are shown on the left, with their functions and pin numbers indicated. The power supply section at the top shows the +3.3V and GND connections, with decoupling capacitors C21, C23, C25, C26, and C28. The audio output section on the right shows the HP_L and HP_R outputs connected to a 100k resistor (R32) and a 100k resistor (R33), which are then connected to the HP_L and HP_R pins of the codec. The microphone input section at the bottom shows the MIC_P and MIC_N pins connected to a 10k resistor (R31) and a 10k resistor (R32), which are then connected to the MIC_P and MIC_N pins of the codec. The ground connections are shown at the bottom, with the GND pin of the codec connected to the GND pin of the Raspberry Pi.

Pin Connections:

- Power:**
 - Pin 1 (GND) to GND
 - Pin 2 (DCVDD) to +3.3V
 - Pin 3 (DBVDD) to +3.3V
 - Pin 4 (AVDD) to +3.3V
 - Pin 5 (SPK_VDD) to +3.3V
 - Pin 6 (SPK_VDD) to +3.3V
 - Pin 7 (SPK_VDD) to +3.3V
 - Pin 8 (SPK_VDD) to +3.3V
 - Pin 9 (SPK_VDD) to +3.3V
 - Pin 10 (SPK_VDD) to +3.3V
 - Pin 11 (SPK_VDD) to +3.3V
 - Pin 12 (SPK_VDD) to +3.3V
 - Pin 13 (SPK_VDD) to +3.3V
 - Pin 14 (SPK_VDD) to +3.3V
 - Pin 15 (SPK_VDD) to +3.3V
 - Pin 16 (SPK_VDD) to +3.3V
 - Pin 17 (SPK_VDD) to +3.3V
 - Pin 18 (SPK_VDD) to +3.3V
 - Pin 19 (SPK_VDD) to +3.3V
 - Pin 20 (SPK_VDD) to +3.3V
 - Pin 21 (SPK_VDD) to +3.3V
 - Pin 22 (SPK_VDD) to +3.3V
 - Pin 23 (SPK_VDD) to +3.3V
 - Pin 24 (SPK_VDD) to +3.3V
 - Pin 25 (SPK_VDD) to +3.3V
 - Pin 26 (SPK_VDD) to +3.3V
 - Pin 27 (SPK_VDD) to +3.3V
 - Pin 28 (SPK_VDD) to +3.3V
- Audio:**
 - Pin 1 (HP_L) to HP_L
 - Pin 2 (HP_R) to HP_R
 - Pin 3 (MIC_P) to MIC_P
 - Pin 4 (MIC_N) to MIC_N
- Control:**
 - Pin 5 (SCL) to SCL
 - Pin 6 (SDA) to SDA
 - Pin 7 (MCLK) to MCLK
 - Pin 8 (BCLK) to BCLK
 - Pin 9 (DACLR) to DACLR
 - Pin 10 (DACDR) to DACDR
 - Pin 11 (ADCL) to ADCL
 - Pin 12 (ADCR) to ADCR

BM148(0.8) - 24DS - 0.4V(53)

[illegible]

- H1 MountingHole
- H2 MountingHole
- H3 MountingHole
- H4 MountingHole

Display - 0.3mm FPC

+3.3V

18 X

17

16 DISP_BL

15 SPI1_CLK

14 SPI1_MISO

13

12 DISP_DC

11 DISP_RST

10 DISP_CS

9

8

7

6

5

4

3

2

1

J4

Conn_01x10_MountingPin

UI_ST-LINK - 2MM R

+3.3V

1 UI_NRST

2 UI_SWDIO

3 UI_BOOT03

4

5

6 UI_SWCLK

7

8

9

10

J5

Conn_02x03_Gdd_Even

GND

Net_JTAG Connector

+3.3V

1 CN1

2 NET_MTMS

3

4 NET_MTCK

5

6 NET_MTDO

7

8 NET_MTDI

9

10

GND

Conn_005x02_Female

SERIAL DEBUG

Pin	Signal
1	10USB_RX1_MGMT
2	9 UL_RX1_MGMT
3	8 UL_TX1_MGMT
4	7 NET_RX1_MGMT
5	6 NET_TX1_MGMT

+3.3V
GND

Conn_02x05_Counter_Clockwise

I2S + I2C DEBUG

Pin	Signal
1	10 U1_SDA1
2	9 U1_SCL1
3	7 I2S_DACDAT
4	6 I2S_ADCCAT

+3.3V
GND

R69 R67 R68 R66 R67 k7 k7

MCLK R64 R66 R67

Conn_02x05_Counter_Clockwise

GPIO DEBUG

Pin	Signal
1	MGMT_DEBUG_1
2	MGMT_DEBUG_2
3	k40NET_DEBUG_3
4	k40NET_DEBUG_2
5	k40NET_DEBUG_1

GND

U1_DEBUG_1 R74 k40-2 U1_CS1_MGMT U1_RST1_MGMT

Conn_02x05_Counter_Clockwise

NET_SERIAL_UPLOADER + MGMT ST LINK

Pin	Signal
1	MGMT_SWCLK
2	MGMT_SWIO
3	MGMT_NRST
4	MGMT_BOOT

+3.3V
GND

Conn_02x04_Odd_Even

EV14 layer build up:
top: High Speed
second: GND
third: 3.3V
bottom: Low Speed

CISCO SYSTEMS INC		
Sheet: /		
File: ev15.kicad_sch		
Title: EV15 FINN BERG & BRETT REGNIER		
Size: A2	Date: 2025-07-25	Rev: EV15
KiCad E.D.A. 9.0.6		Id: 1/1