

# 1. Description

# 1.1. Project

Project Name	mgmt
Board Name	custom
Generated with:	STM32CubeMX 6.8.0
Date	05/07/2023

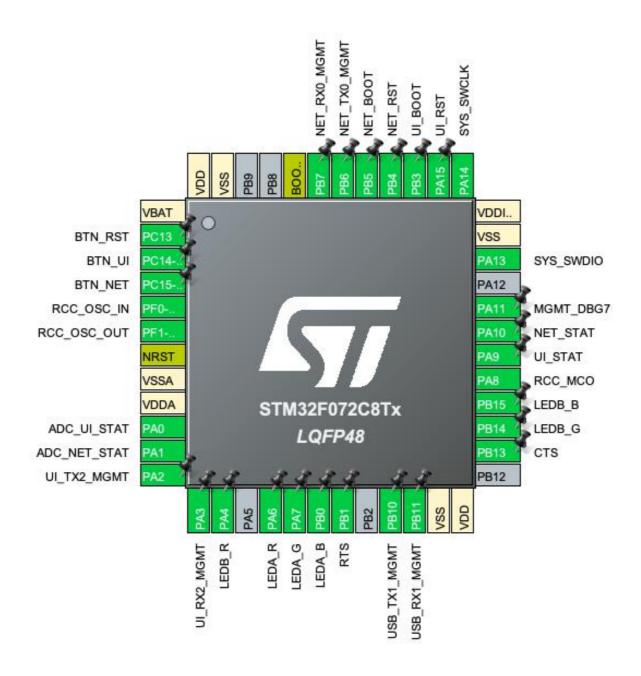
## 1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x2
MCU name	STM32F072C8Tx
MCU Package	LQFP48
MCU Pin number	48

# 1.3. Core(s) information

Core(s)	Arm Cortex-M0

# 2. Pinout Configuration



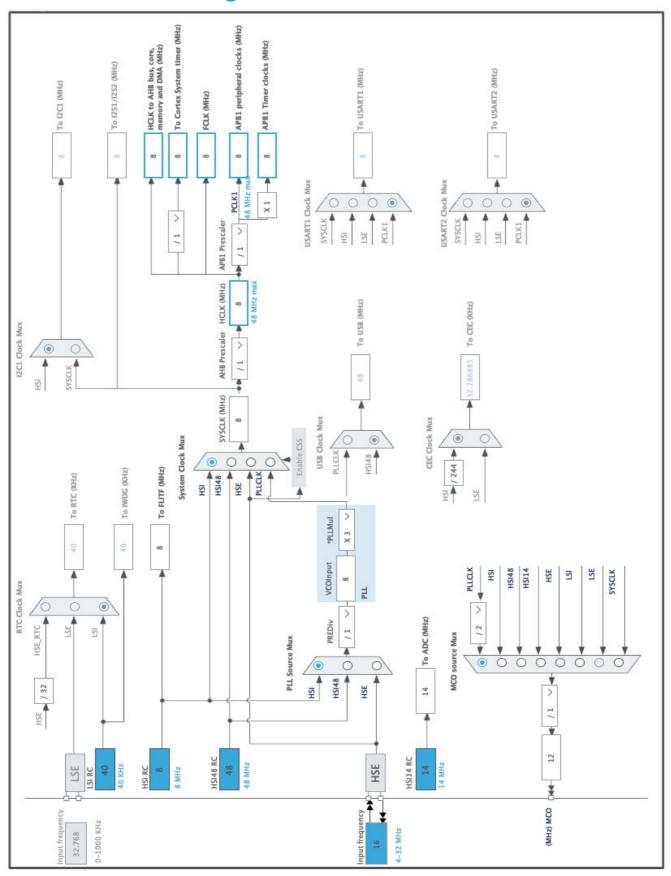
# 3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP48	(function after		Function(s)	
	reset)		(-)	
1	VBAT	Power		
2	PC13 *	1/0	GPIO_Input	BTN_RST
3	PC14-OSC32_IN *	I/O	GPIO_Input	BTN_UI
4	PC15-OSC32_OUT *	I/O	GPIO_Input	BTN_NET
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0	I/O	ADC_IN0	ADC_UI_STAT
11	PA1	I/O	ADC_IN1	ADC_NET_STAT
12	PA2 *	I/O	GPIO_Input	UI_TX2_MGMT
13	PA3 *	I/O	GPIO_Output	UI_RX2_MGMT
14	PA4 *	I/O	GPIO_Output	LEDB_R
16	PA6 *	I/O	GPIO_Output	LEDA_R
17	PA7 *	I/O	GPIO_Output	LEDA_G
18	PB0 *	I/O	GPIO_Output	LEDA_B
19	PB1 *	I/O	GPIO_Input	RTS
21	PB10 *	I/O	GPIO_Input	USB_TX1_MGMT
22	PB11 *	I/O	GPIO_Output	USB_RX1_MGMT
23	VSS	Power		
24	VDD	Power		
26	PB13 *	I/O	GPIO_Input	CTS
27	PB14 *	I/O	GPIO_Input	LEDB_G
28	PB15 *	I/O	GPIO_Input	LEDB_B
29	PA8	I/O	RCC_MCO	
30	PA9 *	I/O	GPIO_Input	UI_STAT
31	PA10 *	I/O	GPIO_Input	NET_STAT
32	PA11 *	I/O	GPIO_Output	MGMT_DBG7
34	PA13	I/O	SYS_SWDIO	
35	VSS	Power		
36	VDDIO2	Power		
37	PA14	I/O	SYS_SWCLK	
38	PA15 *	I/O	GPIO_Output	UI_RST
39	PB3 *	I/O	GPIO_Output	UI_BOOT
40	PB4 *	I/O	GPIO_Output	NET_RST

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	PB5 *	I/O	GPIO_Output	NET_BOOT
42	PB6 *	I/O	GPIO_Input	NET_TX0_MGMT
43	PB7 *	I/O	GPIO_Output	NET_RX0_MGMT
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

Name	Value
Project Name	mgmt
Project Folder	/Users/fluffy/src/hactar/firmware/mgmt
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F0 V1.11.4
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

## 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC_Init	ADC
4	MX_TIM3_Init	TIM3

# 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x2
MCU	STM32F072C8Tx
Datasheet	DS9826_Rev5

### 6.2. Parameter Selection

Temperature	25
Vdd	3.6

## 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

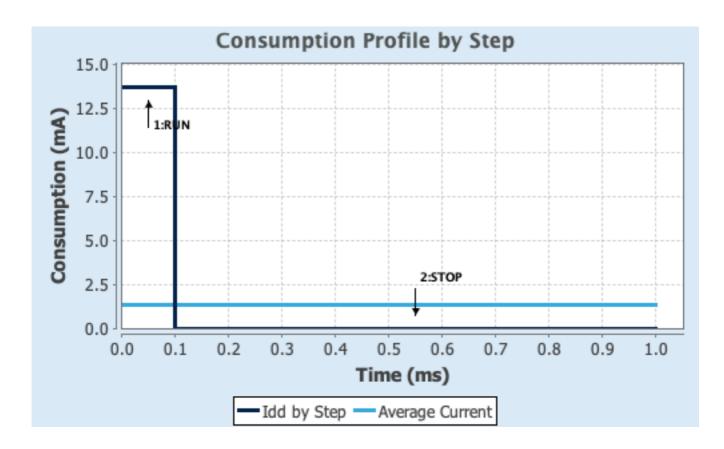
# 6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	48 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	13.66 mA	6.5 μA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Ta Max	102.34	105
Category	In DS Table	In DS Table

### 6.5. Results

Sequence Time	1 ms	Average Current	1.37 mA
Battery Life	3 months, 11	Average DMIPS	0.0 DMIPS
	days, 17 hours		

## 6.6. Chart



# 7. Peripherals and Middlewares Configuration

Disabled

7.1. ADC mode: IN0

mode: IN1

### 7.1.1. Parameter Settings:

Discontinuous Conversion Mode

#### ADC\_Settings:

Clock Prescaler

Resolution

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

ADC 12-bit resolution

Right alignment

Forward

Disabled

DMA Continuous Requests

Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled
Low Power Auto Power Off Disabled

#### ADC\_Regular\_ConversionMode:

Sampling Time 1.5 Cycles

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

WatchDog:

Enable Analog WatchDog Mode false
Low Threshold 0

#### 7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

mode: Master Clock Output

#### 7.2.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16
HSI14 Calibration Value 16

HSE Startup Timout Value (ms) 100 LSE Startup Timout Value (ms) 5000

#### 7.3. SYS

mode: Debug Serial Wire Timebase Source: SysTick

#### 7.4. TIM3

Trigger Source: ITR0

### 7.4.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value ) 48000 \*

Internal Clock Division (CKD) No Division auto-reload preload Disable

Slave Mode Controller Slave mode disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

#### \* User modified value

# 8. System Configuration

# 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PA0	ADC_IN0	Analog mode	No pull-up and no pull-down	n/a	ADC_UI_STAT
	PA1	ADC_IN1	Analog mode	No pull-up and no pull-down	n/a	ADC_NET_STAT
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
GPIO	PC13	GPIO_Input	Input mode	Pull-up *	n/a	BTN_RST
	PC14- OSC32_IN	GPIO_Input	Input mode	Pull-up *	n/a	BTN_UI
	PC15- OSC32_OU T	GPIO_Input	Input mode	Pull-up *	n/a	BTN_NET
	PA2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UI_TX2_MGMT
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	UI_RX2_MGMT
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDB_R
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDA_R
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDA_G
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDA_B
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RTS
	PB10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_TX1_MGMT
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	USB_RX1_MGMT
	PB13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CTS
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LEDB_G
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LEDB_B
	PA9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	UI_STAT
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NET_STAT
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MGMT_DBG7
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_RST
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UI_BOOT
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NET_RST
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NET_BOOT
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NET_TX0_MGMT
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	NET_RX0_MGMT

# 8.2. DMA configuration

nothing configured in DMA service

# 8.3. NVIC configuration

# 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	3	0
PVD and VDDIO2 supply comparator interrupts through EXTI lines 16 and 31	unused		
Flash global interrupt	unused		
RCC and CRS global interrupts	unused		
ADC and COMP interrupts (COMP interrupts through EXTI lines 21 and 22)	pts unused		
TIM3 global interrupt		unused	

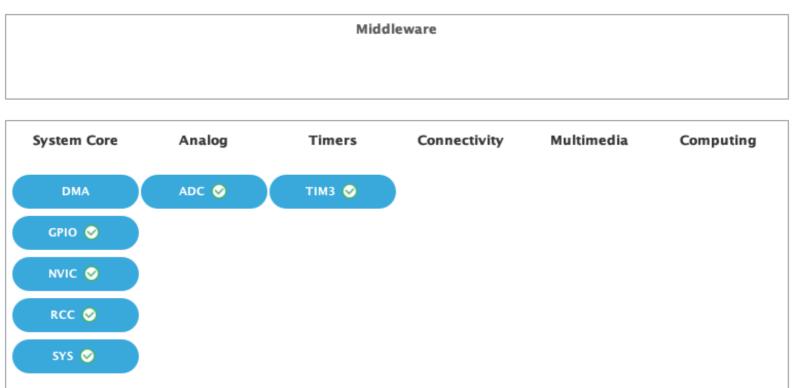
# 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

<sup>\*</sup> User modified value

# 9. System Views

- 9.1. Category view
- 9.1.1. Current



### 10. Docs & Resources

Type Link

IBIS models https://www.st.com/resource/en/ibis\_model/stm32f0\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f0\_svd.zip

Description

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