IS RISC-V READY FOR HIGH PERFORMANCE COMPUTING? AN EVALUATION OF THE SOPHON SG2044

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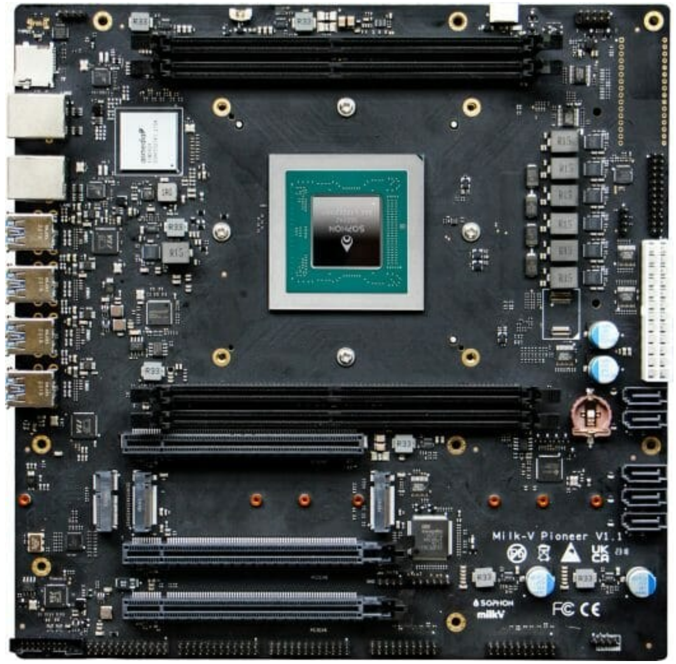
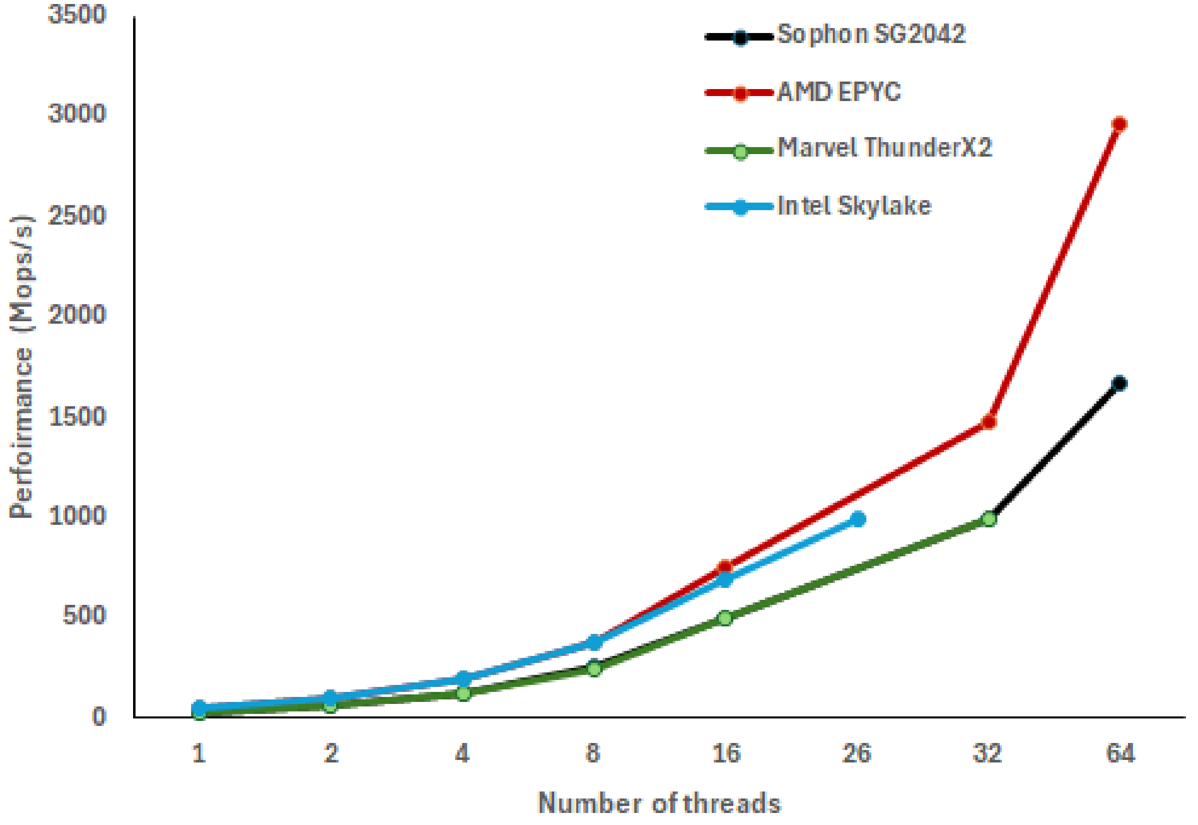
Motivation: SG2042

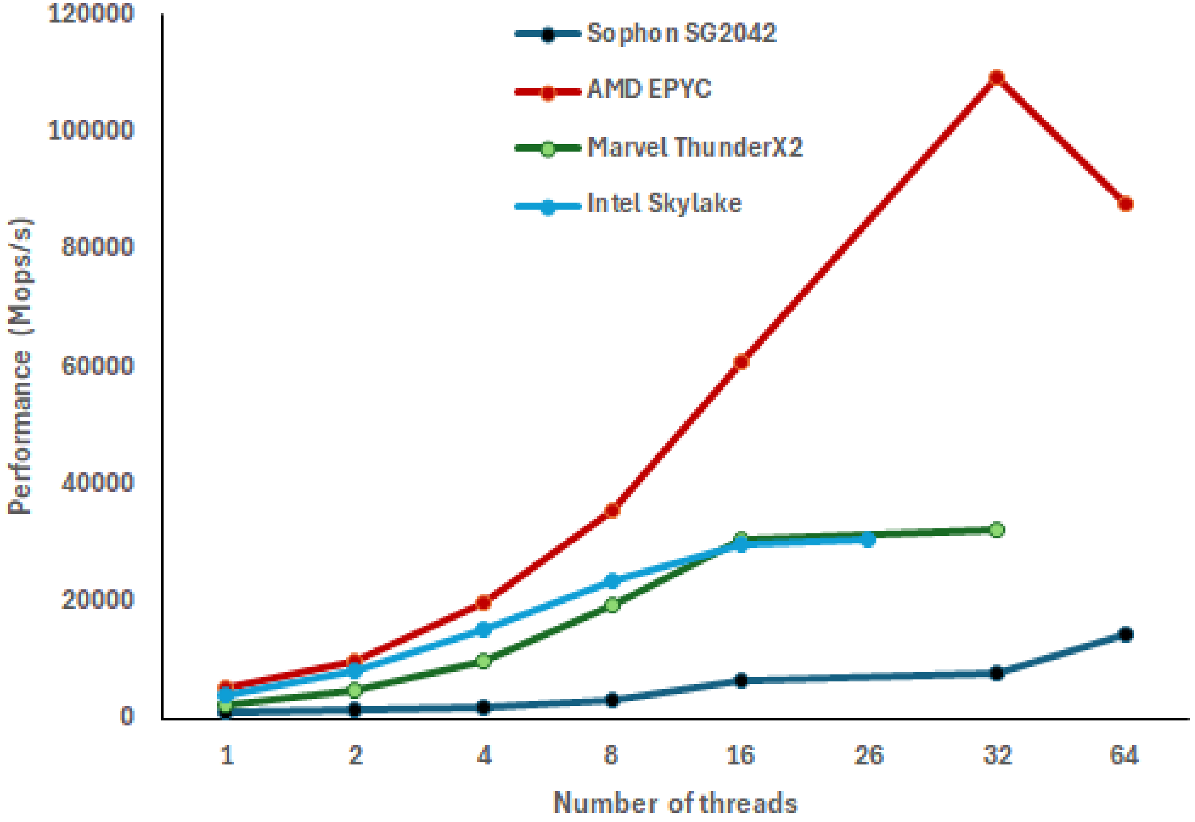


- Comprises 64 XuanTie C920v1 cores
  - 12-stage out-of-order multiple issue superscalar pipeline design
  - RV64GCV instruction set, the C920v1 has three decode, four rename/dispatch, eight issue/execute and two load/store execution units
  - RVV v0.7.1 is supported with a vector width of 128 bits.
  - Each core contains 64KB of L1 instruction (I) and data (D) cache, 1MB of L2 cache which is shared between the cluster of four cores, and 64MB of L3 system cache which is shared by all cores in the package.
- The SG2042 also provides four DDR4-3200 memory controllers, and 32 lanes of PCIe gen4.

Motivation: SG2042



EP NAS benchmark class C (compute bound)



MG NAS benchmark class C (mem bandwidth bound)

Fundamentally, the SG2042 is limited in memory performance which has a major impact in overall code performance that one can obtain

The next generation SG2044

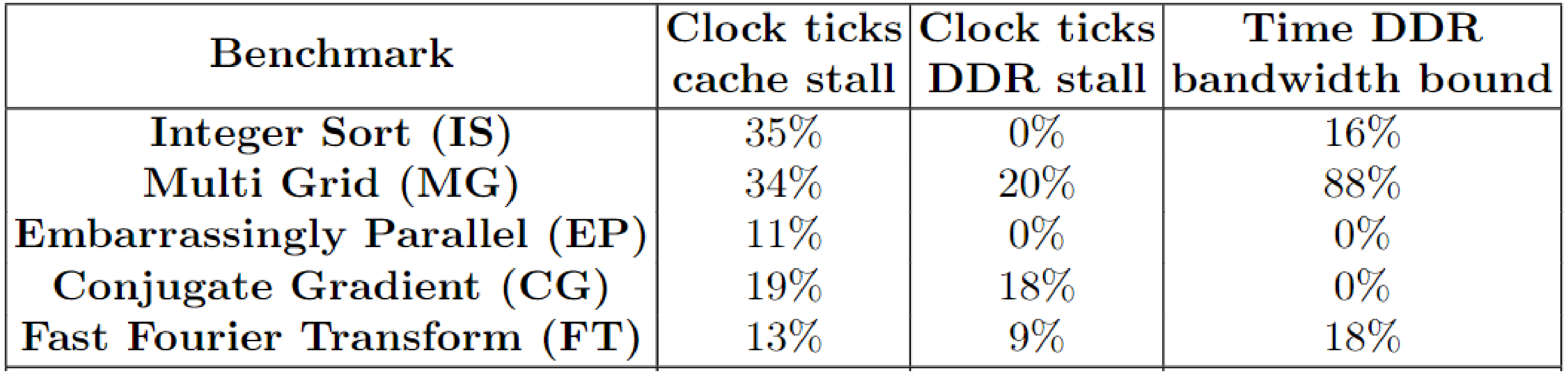
- Evolution of the SG2042, 64-core XuanTie C920v2
  - 128-bit wide vector unit implements RVV v1.0
  - As per C920v1, there is a 12 stage out-of-order multiple issue superscalar pipeline design. Providing the RV64GCV instruction set, the C920v2 has three decode, four rename/dispatch, eight issue/execute and two load/ store execution units
  - 2.6 GHz clock frequency, compared to 2 GHz in SG2042
  - All cores are in a single NUMA region, with 32 memory controllers and 32 memory channels
  - Each core contains 64KB of L1 instruction (I) and data (D) cache like SG2042, but 2MB of L2 cache shared between a cluster of four cores (double the SG2042), and 64MB of L3 system cache shared by all cores in the package.
  - Support for PCIe Gen5 and DDR5

Geekbench results published:

- Impressive against SG2042, but different versions of benchmark being compared.
- Another evaluation used the same benchmark version, single core performance similar and for multi-core SG2044 is around 1.3 times faster.

NAS Parallel Benchmarks (NPBs)

- Suite developed by NASA's Advanced Supercomputing (NAS) division
  - Aim is to characterise HPC systems, especially for CFD applications
  - We focus on the five original kernels, and three pseudo-applications
  - Driven by a variety of problem size classes

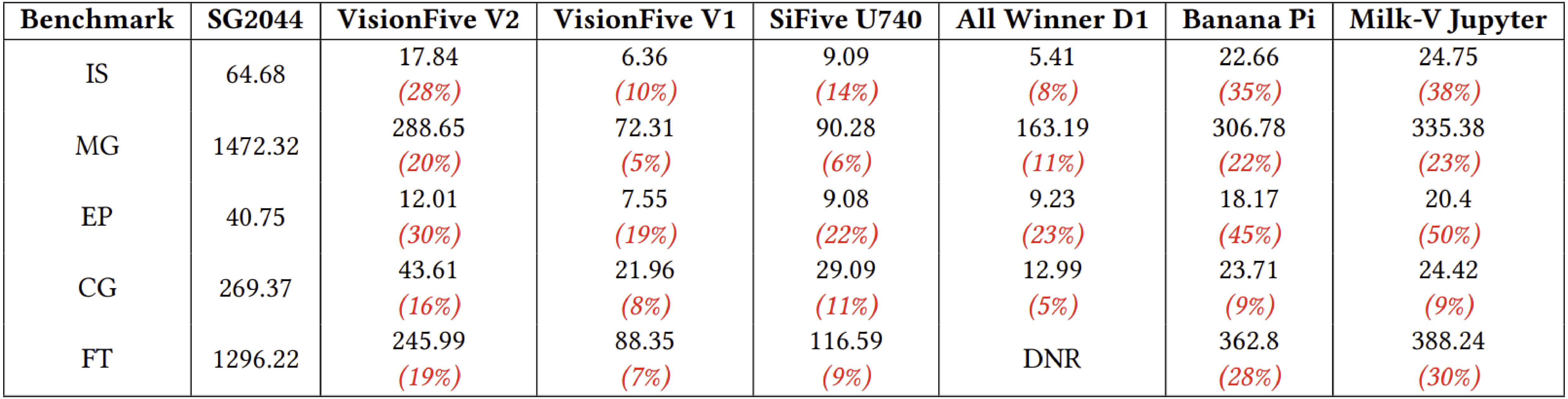


Benchmark	Clock ticks cache stall	Clock ticks DDR stall	Time DDR bandwidth bound
Integer Sort (IS)	35%	0%	16%
Multi Grid (MG)	34%	20%	88%
Embarrassingly Parallel (EP)	11%	0%	0%
Conjugate Gradient (CG)	19%	18%	0%
Fast Fourier Transform (FT)	13%	9%	18%

Profiling with Vtune on a Xeon 8170 via OpenMP over all 26 cores

- IS: Indirect, random memory access & integer performance
- MG: Memory bound
- EP: Tests floating point computer performance
- CG: Irregular memory access and nearest neighbour interactions
- FT: All to All neighbour interactions

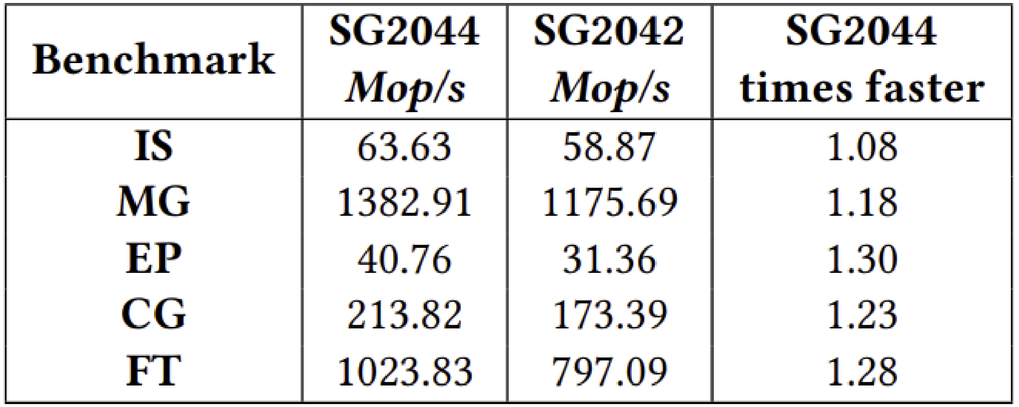
Single core C920v2 against other RISC-V



	C920v2	JH7200	JH7100	U74	C906	SpacemiT K1 (1.6Ghz)	SpacemiT M1 (1.8Ghz)
Benchmark	**SG2044**	**VisionFive V2**	**VisionFive V1**	**SiFive U740**	**All Winner D1**	**Banana Pi**	**Milk-V Jupyter**
IS	64.68	17.84 *(28%)*	6.36 *(10%)*	9.09 *(14%)*	5.41 *(8%)*	22.66 *(35%)*	24.75 *(38%)*
MG	1472.32	288.65 *(20%)*	72.31 *(5%)*	90.28 *(6%)*	163.19 *(11%)*	306.78 *(22%)*	335.38 *(23%)*
EP	40.75	12.01 *(30%)*	7.55 *(19%)*	9.08 *(22%)*	9.23 *(23%)*	18.17 *(45%)*	20.4 *(50%)*
CG	269.37	43.61 *(16%)*	21.96 *(8%)*	29.09 *(11%)*	12.99 *(5%)*	23.71 *(9%)*	24.42 *(9%)*
FT	1296.22	245.99 *(19%)*	88.35 *(7%)*	116.59 *(9%)*	DNR	362.8 *(28%)*	388.24 *(30%)*

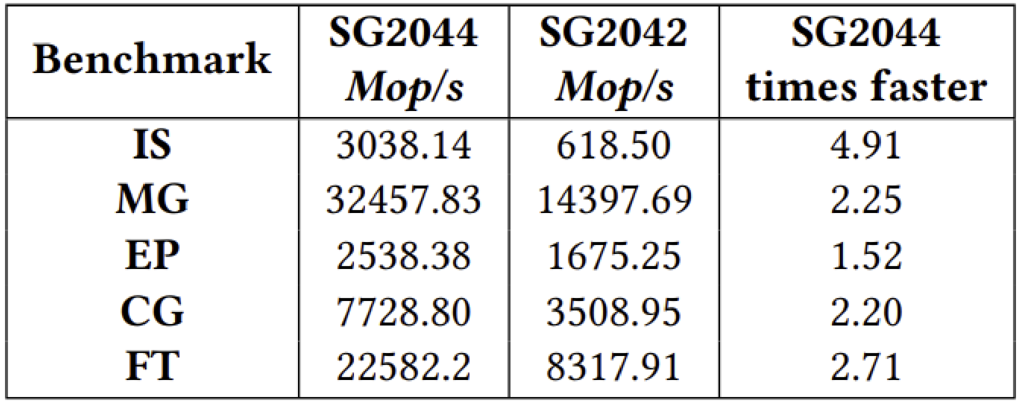
For NAS benchmark kernels (class B), the black number is million ops/second (higher is better), red is percentage of performance obtained by a C920v2 core in the SG2044

SG2044 vs SG2042



Benchmark	SG2044 *Mop/s*	SG2042 *Mop/s*	SG2044 times faster
IS	63.63	58.87	1.08
MG	1382.91	1175.69	1.18
EP	40.76	31.36	1.30
CG	213.82	173.39	1.23
FT	1023.83	797.09	1.28

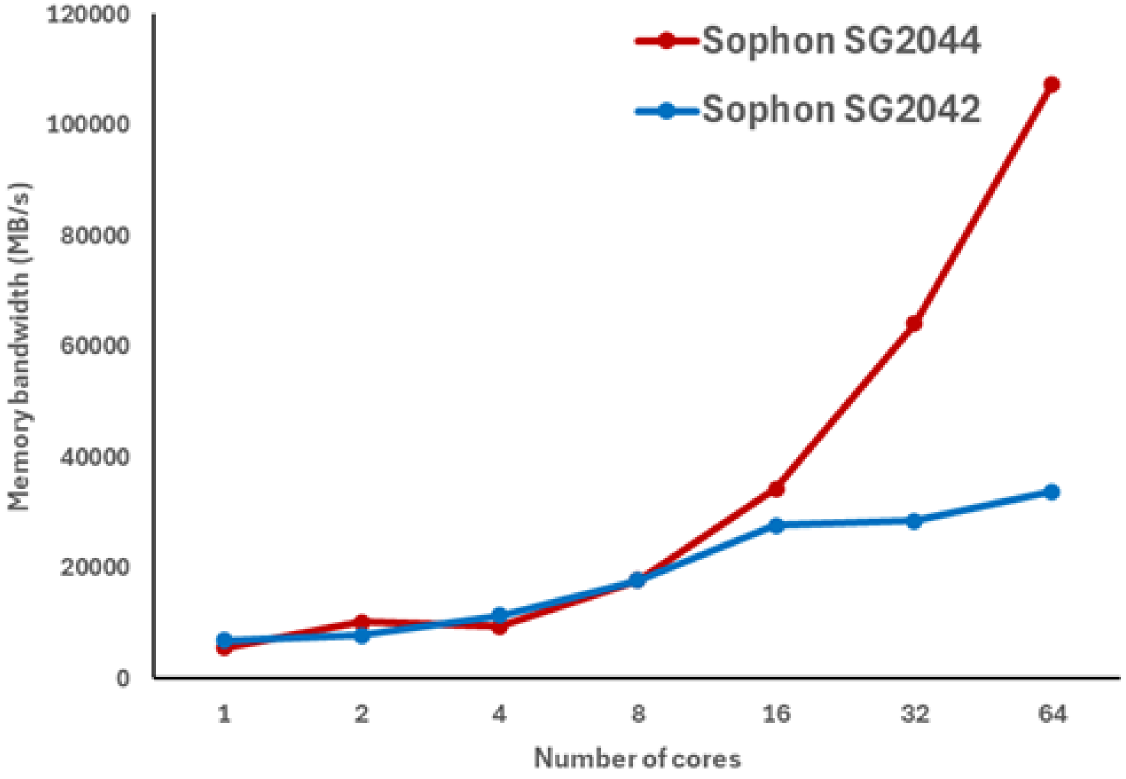
Single core performance comparison (class C, higher is better)



Benchmark	SG2044 *Mop/s*	SG2042 *Mop/s*	SG2044 times faster
IS	3038.14	618.50	4.91
MG	32457.83	14397.69	2.25
EP	2538.38	1675.25	1.52
CG	7728.80	3508.95	2.20
FT	22582.2	8317.91	2.71

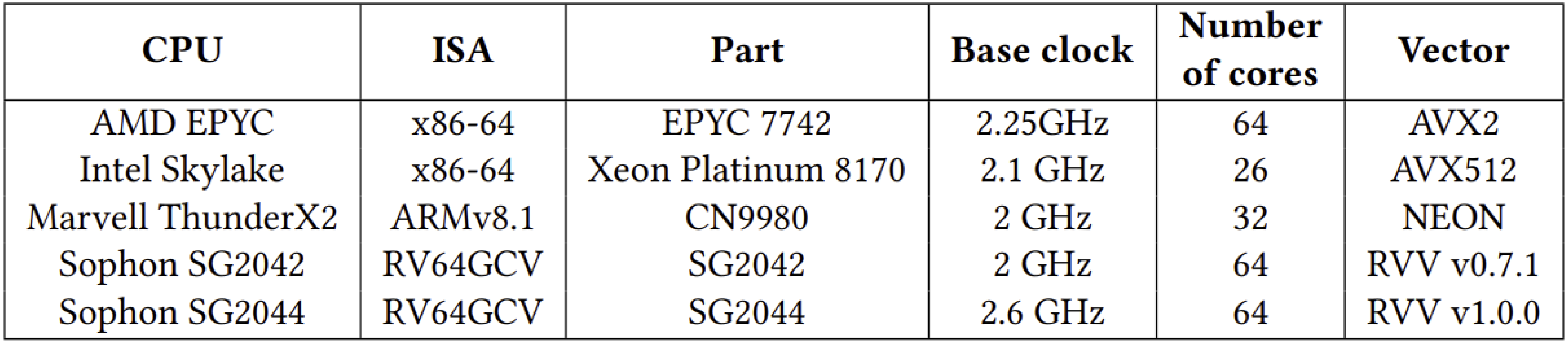
Multi-core (64) performance comparison (class C, higher is better)

- T-Head's fork of GCCv8.4 (XuanTie GCC) consistently provided best performance on SG2042
- GCC v15.2 was used for the SG2044



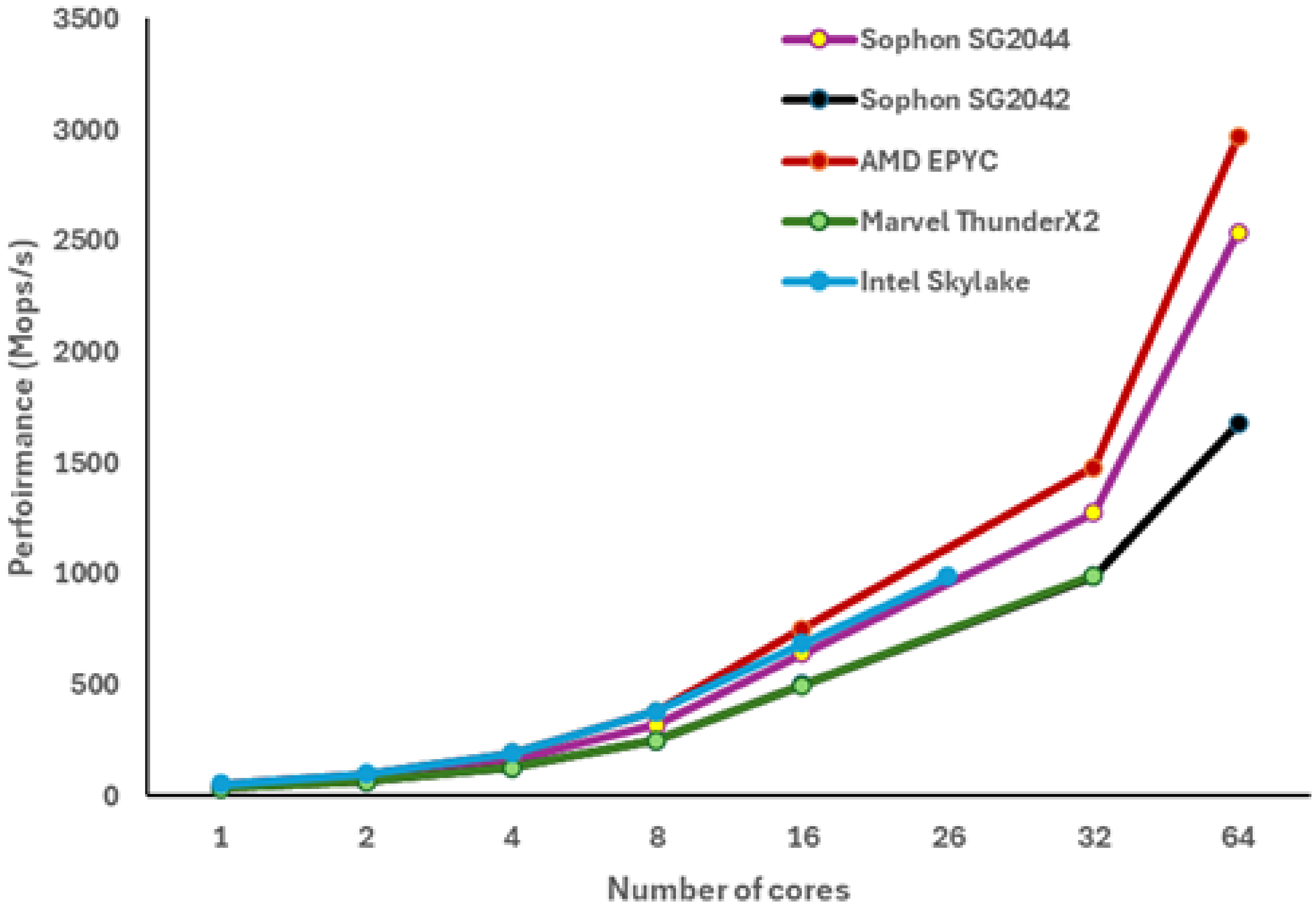
Memory bandwidth reported by STREAM benchmark (higher is better)

Comparing with other architectures for NAS Class C



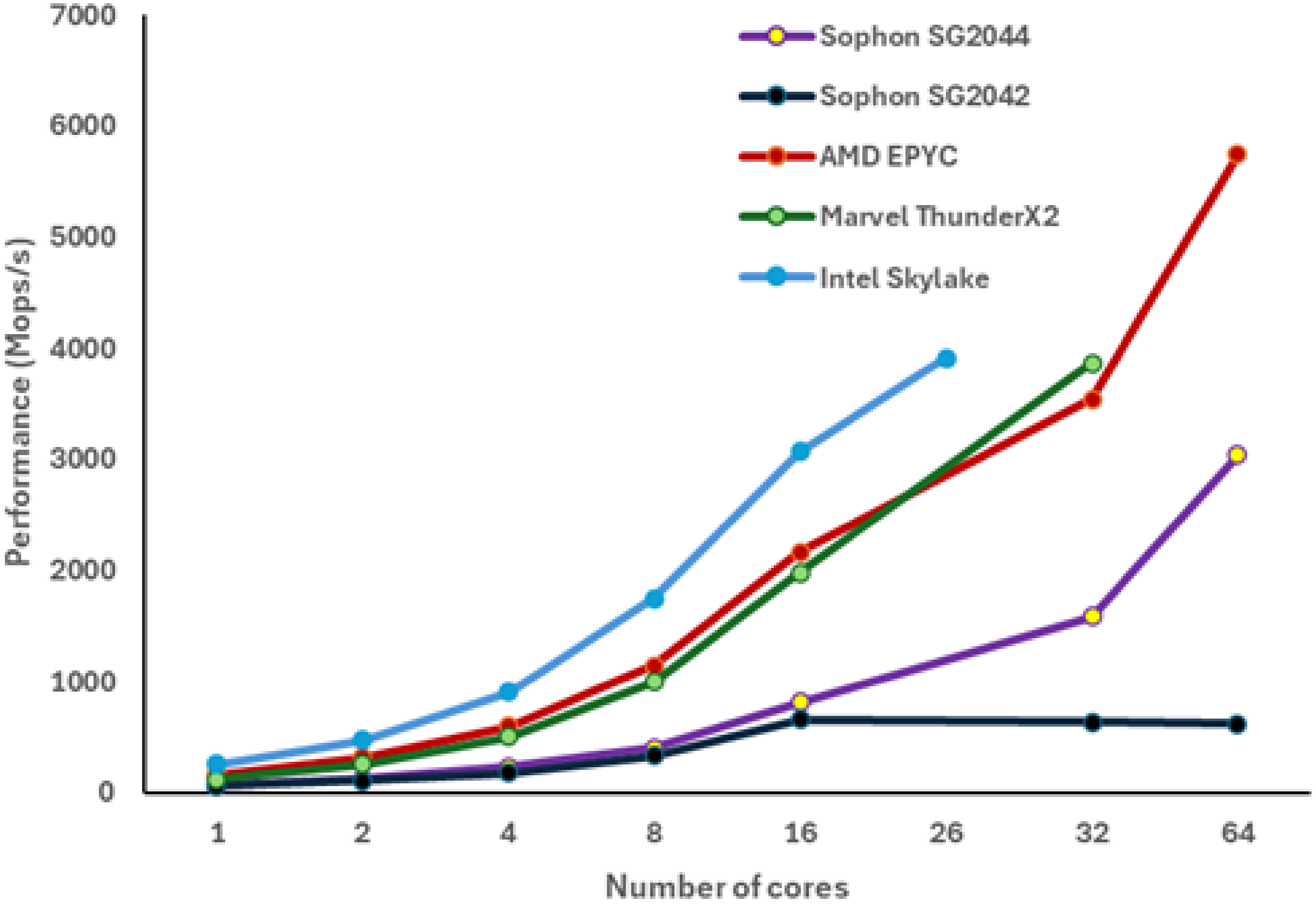
CPU	ISA	Part	Base clock	Number of cores	Vector
AMD EPYC	x86-64	EPYC 7742	2.25GHz	64	AVX2
Intel Skylake	x86-64	Xeon Platinum 8170	2.1 GHz	26	AVX512
Marvell ThunderX2	ARMv8.1	CN9980	2 GHz	32	NEON
Sophon SG2042	RV64GCV	SG2042	2 GHz	64	RVV v0.7.1
Sophon SG2044	RV64GCV	SG2044	2.6 GHz	64	RVV v1.0.0

Embarrassingly Parallel (EP) benchmark



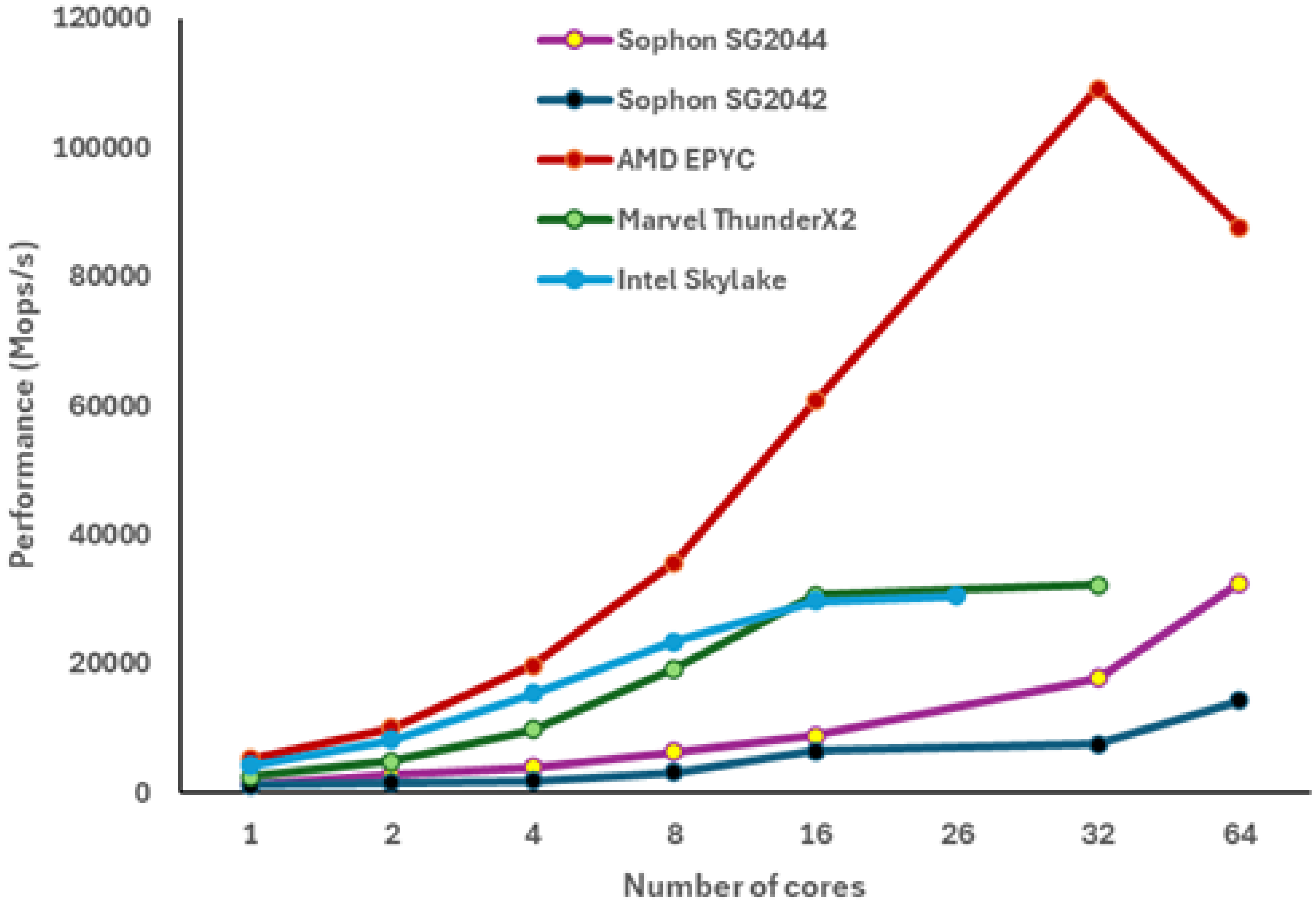
- Focus on compute performance
  - Three groups of performance here
- SG2042 and ThunderX2 are both 128-bit wide vector (although ThunderX2 has two FPUs per core).
- SG2044 tracks Skylake but increased number of cores crucial
- EPYC outperforms all, but interesting it and SG2044 follow same performance shape

Integer Sort (IS) benchmark



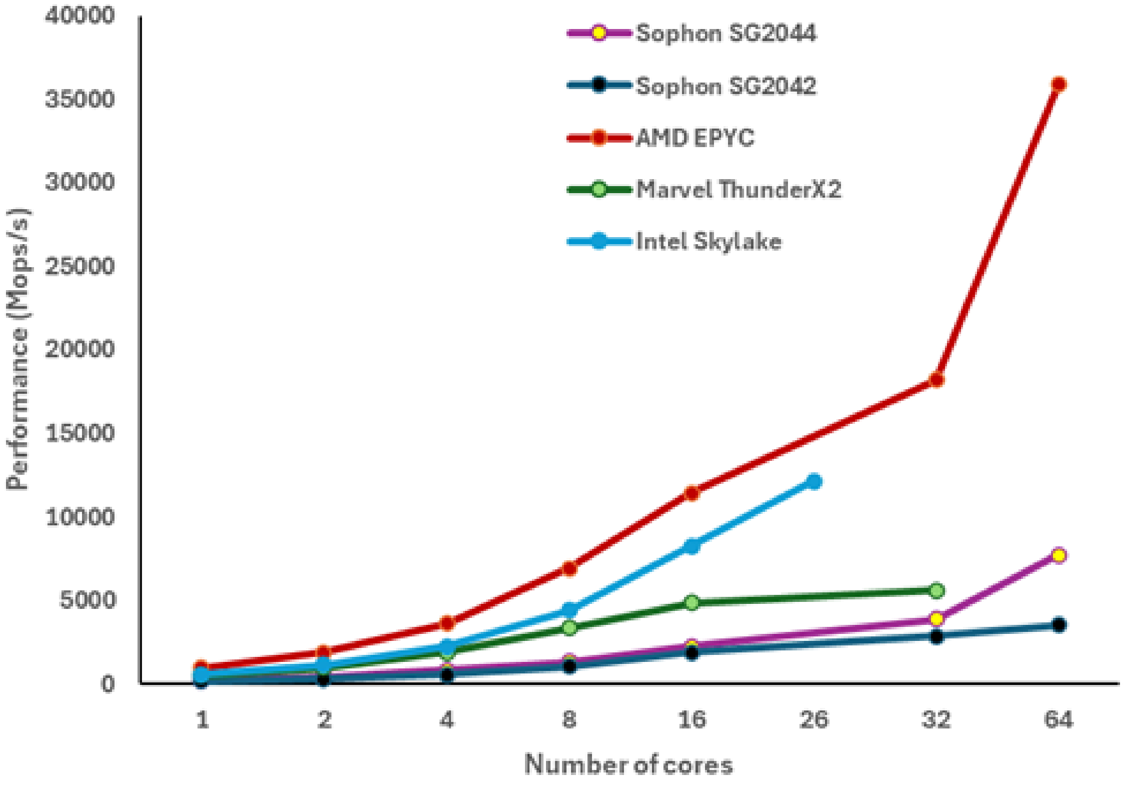
- Integer comparison and indirect, random, memory accesses
- SG2042 plateaus at 16 cores and performs worse than all the others
- SG2044 is considerably better than SG2042 at increased cores, but still slower than others
  - Can clearly see link back to STREAM benchmark
  - Limitations in individual memory controllers likely causing fundamental slowdowns

MultiGrid (MG) benchmark

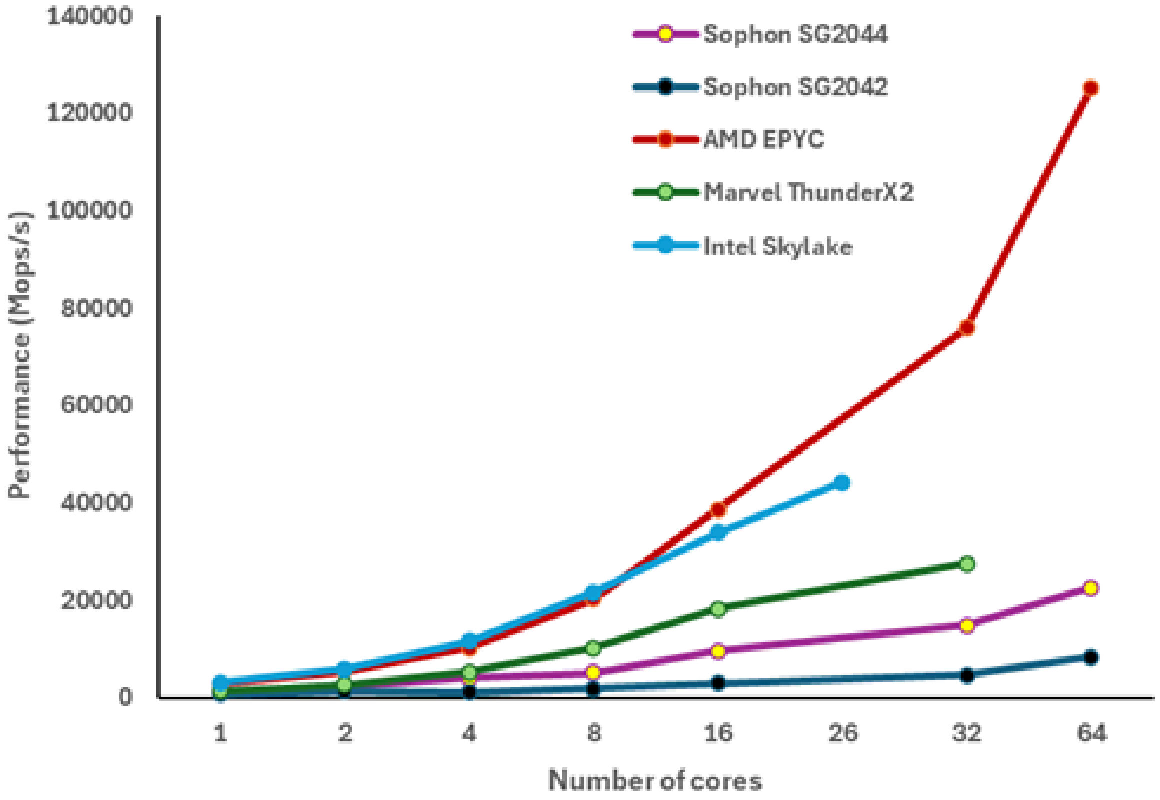


- Memory bandwidth bound
- EPYC provides best performance, ThunderX2 and Skylake are similar and plateau at 16 cores
- SG2042 is always lowest performance here
- EPYC: 8 memory channels, 8 controllers connected to DDR4-3200
- Skylake & ThunderX2: 2 memory controllers (6 channels for Skylake, 8 for ThunderX2). Connected to DDR4-2666

CG and FT benchmarks

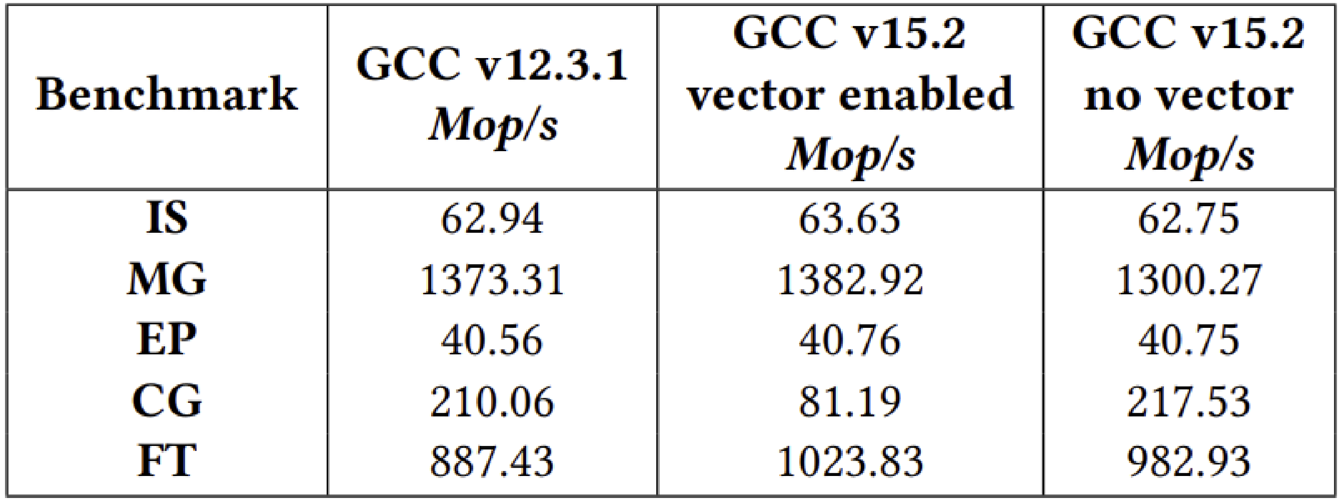


CG benchmark (nearest neighbour communications)



FT benchmark (all-to-all communications)

Compiler versions and vectorisation: Single core

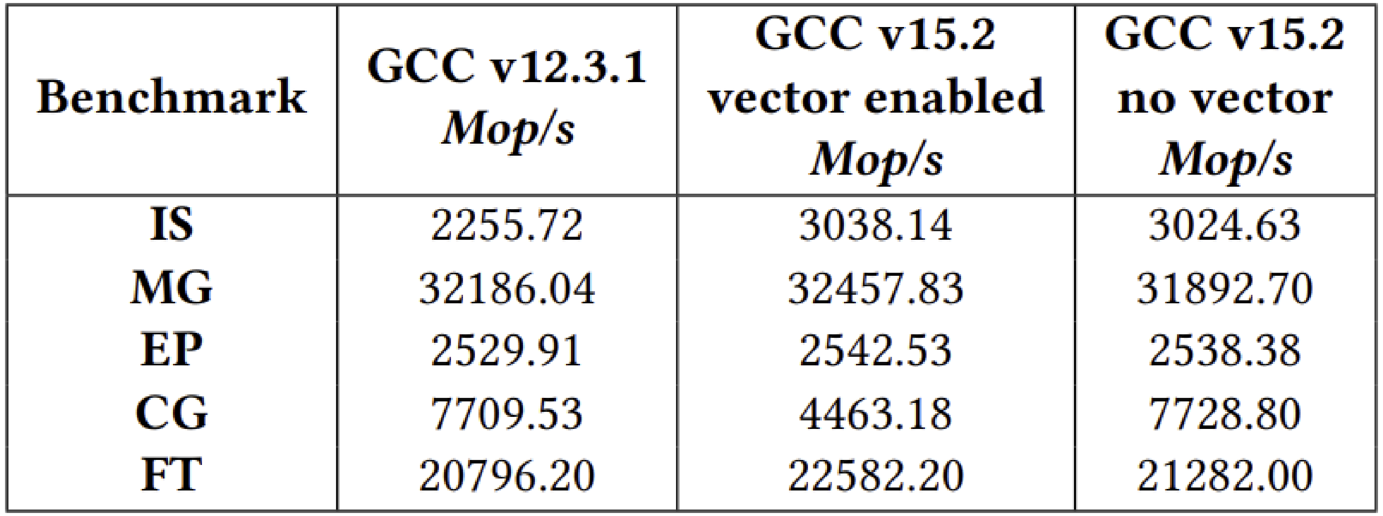


Benchmark	GCC v12.3.1 *Mop/s*	GCC v15.2 vector enabled *Mop/s*	GCC v15.2 no vector *Mop/s*
IS	62.94	63.63	62.75
MG	1373.31	1382.92	1300.27
EP	40.56	40.76	40.75
CG	210.06	81.19	217.53
FT	887.43	1023.83	982.93

- System was running openEuler Linux operating system which ships with GCC version 12.3.1
- The latest release of GCC is version 15.2 (August 2025)
  - Lots of improvements between these versions, especially for RVV

- CG is the outlier here, enabling RVV resulted in significant slowdown!
  - Experimented with alternatives to matrix multiplication which are provided by the kernel, unrolling the kernel two or eight times. These improved performance, but still slower
  - Perf reported double the number of branch misses for vectorised version, and vectorised version has lower IPC

Compiler versions and vectorisation: Multi-core



Benchmark	GCC v12.3.1 *Mop/s*	GCC v15.2 vector enabled *Mop/s*	GCC v15.2 no vector *Mop/s*
IS	2255.72	3038.14	3024.63
MG	32186.04	32457.83	31892.70
EP	2529.91	2542.53	2538.38
CG	7709.53	4463.18	7728.80
FT	20796.20	22582.20	21282.00

- System was running openEuler Linux operating system which ships with GCC version 12.3.1
- The latest release of GCC is version 15.2 (August 2025)
  - Lots of improvements between these versions, especially for RVV

- Similar story for CG when running over all 64-cores
- IS benefits the most from GCC v15.2, but all kernels also benefit from the later GCC so worth using latest GCC regardless
  - GCC 16 will have target support for XuanTie CPUs including C920v2.

Conclusions and further work

- We have been waiting for the SG2044 for some time
- Impressive improvement over the SG2044 across all benchmarks that we tested
  - When comparing to other RISC-V cores that are available, the C920v2 in the SG2044 clearly wins hands down
  - But still some way to go for HPC, my feeling is that single core performance is (still) being limited by the memory controllers.

- XuanTie have announced their C930 core to be released in 2026, providing RVA23 and 512-bit RVV, there is huge potential here for HPC workloads.