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Evaluating RISC-V processor as an alternative for High Performance Computing

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Outline

- Motivation
- Objective
- Methodology
- Hardware Setup
- Application Used
- Performance Analysis
- Conclusion

Motivation

Dominance of x86

x86 processors (Intel, AMD) dominate HPC due to performance and software maturity.

Rise of ARM

ARM is preferred for its energy efficiency and offering Competitive HPC performance

Entry of RISC-V

RISC-V offers an open, modular ISA enabling innovation via hardware-software co-design

Need for Evaluation

A detailed performance and scalability analysis is essential to determine RISC-V's readiness for real-world HPC workloads

Objectives

Analyze the performance of the SOPHGO SG2042, a 64-core RISC-V processor

Benchmark comparison with Intel Sapphire Rapids, AMD Genoa, and Fujitsu A64FX

Employ applications based on Berkeley Dwarfs for diverse workload coverage

Evaluate scalability, memory bandwidth, and network communication efficiency

Methodology

Applications

12 computational kernels from the Berkeley Dwarfs classification.

Compilation

Compiled using GCC v12.2 with -O3 optimization.

Parallelism

OpenMP v5.0 for threading, OpenMPI v5.0.6 for network performance tests.

Thread Setup

Used 48-thread baseline and architecture-specific max threads.

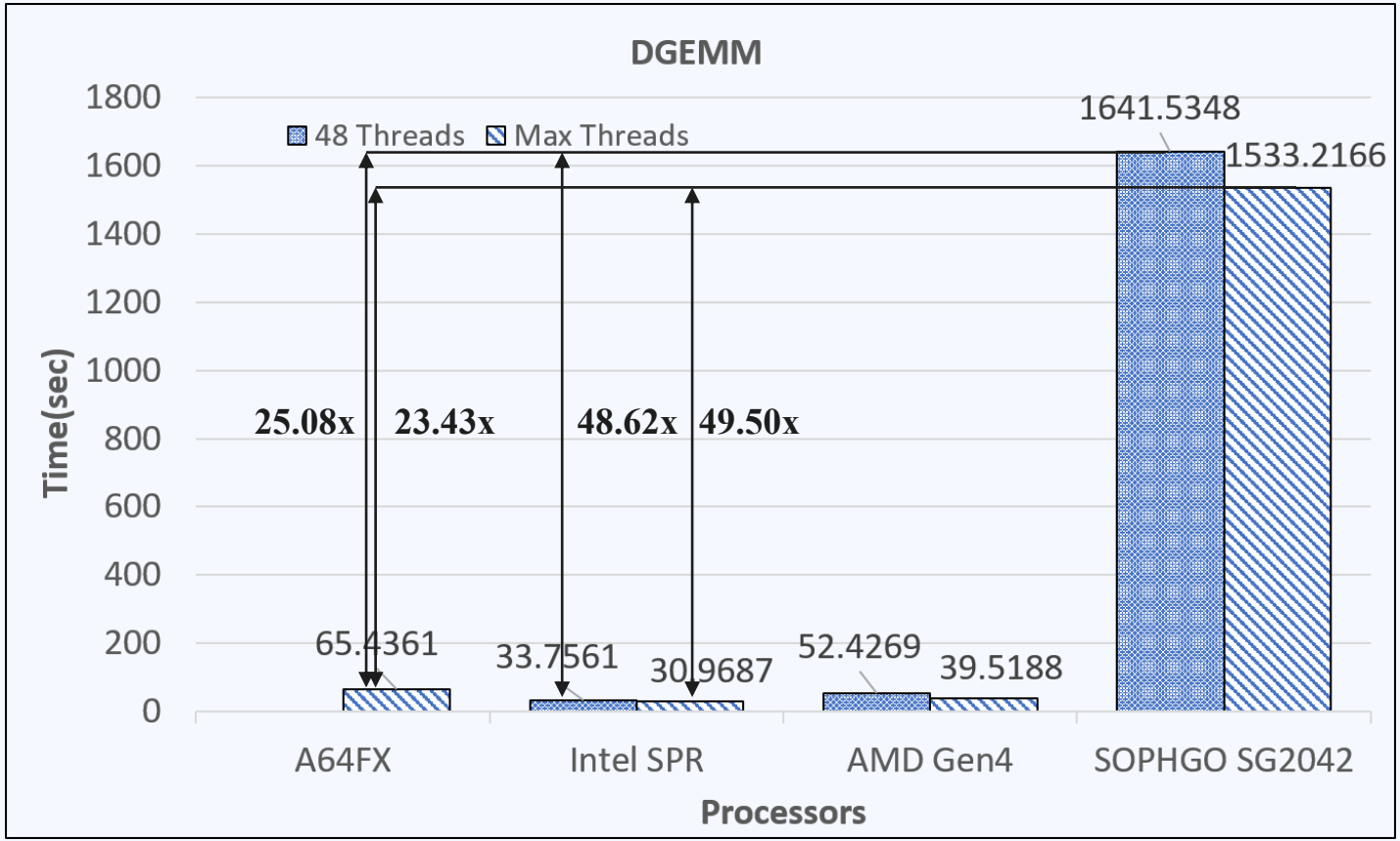
Hardware Setup

Category	Processors			
	Fujitsu A64FX	**Intel SPR**	**AMD Genova**	**SOPHGO SG2042**
Architecture	ARM	X86	X86	RISC-V
Number of Cores	48	64	192	64
Frequency	2 GHz	3.4GHz	2.4GHz	2GHz

Application Used	Problem Size
DGEMM using OpenBLAS	32k x 32k
SpMM	2 million rows and column
FFT(Cooley-Tukey Radix-2 Decimation)	2^{25}
Nbody	40000
Convolution	32k x 32k
Laplace Equation	102400 x 204800
Pi Calculation	1 billion
Encryption	163 MB
Knapsack(DP)	500k
BFS	50 million
Knapsack(backtracing+ branch& bound)	64
Hidden Markov Models	2048
MPI	100MB

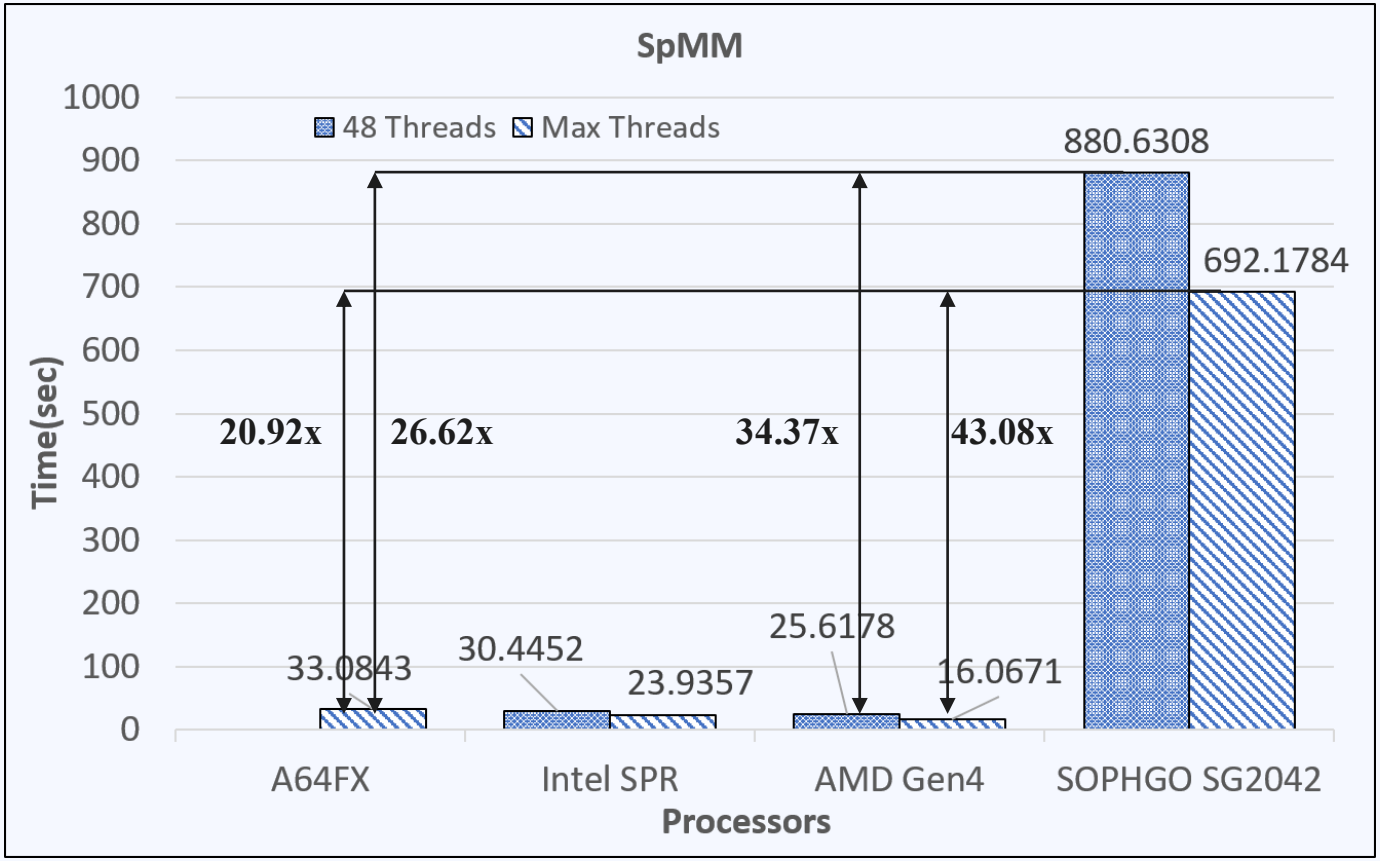
Performance Analysis of DGEMM

Dwarf Covered: Dense Linear Algebra



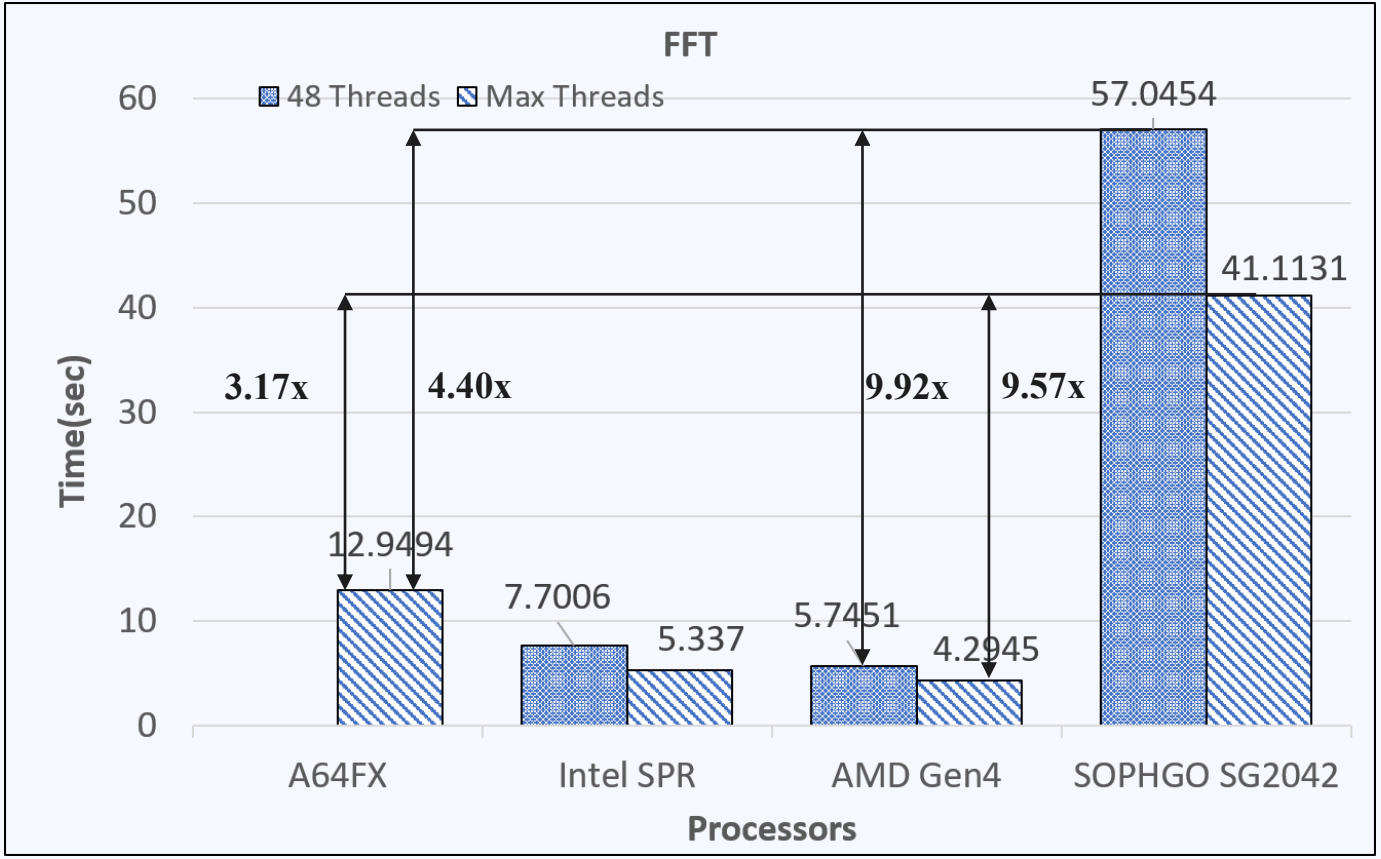
Performance Analysis of SpMM

Dwarf Covered: Sparse Linear Algebra



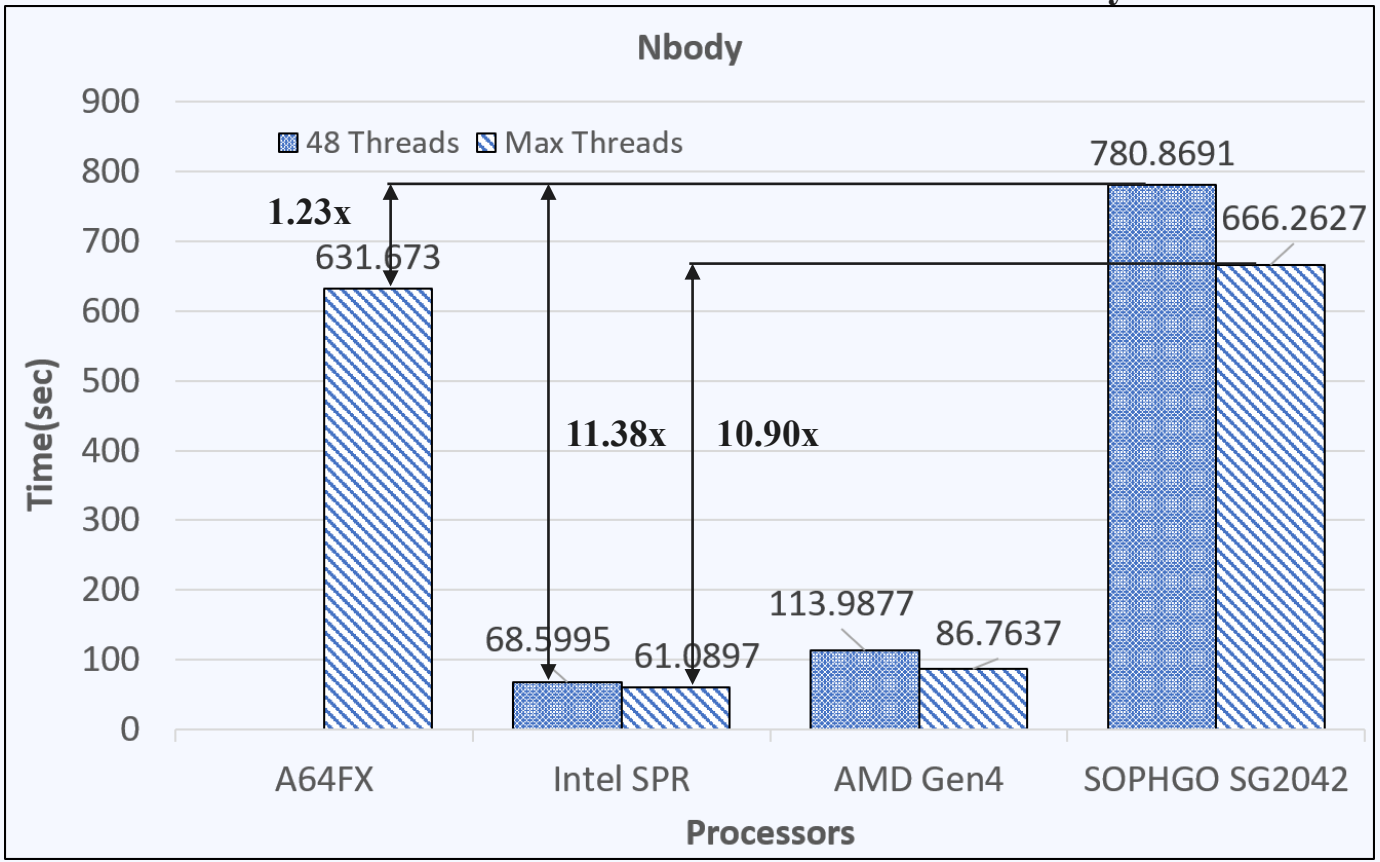
Performance Analysis of FFT

Dwarf Covered: Spectral Methods



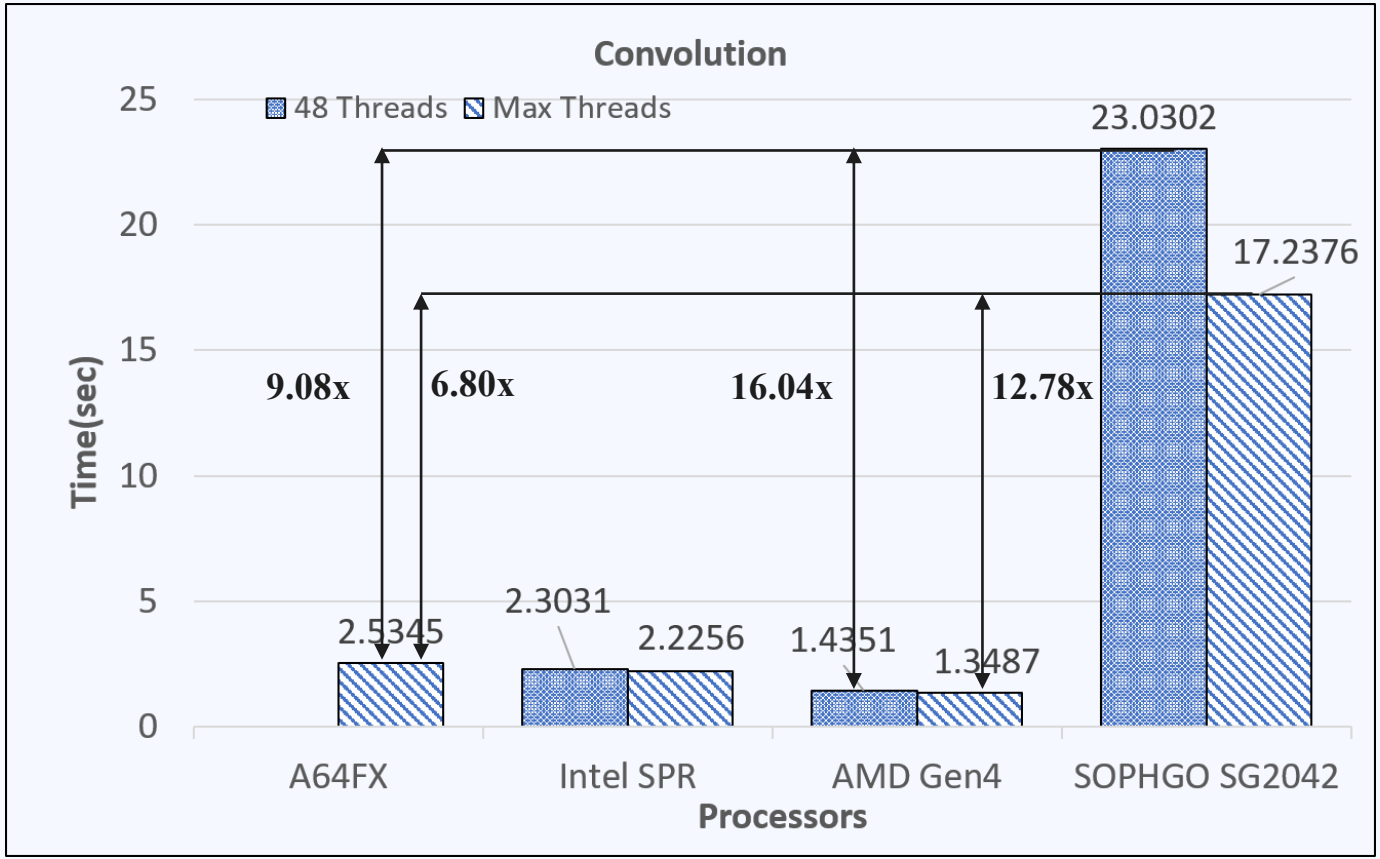
Performance Analysis of Nbody

Dwarf Covered: N-body Simulation



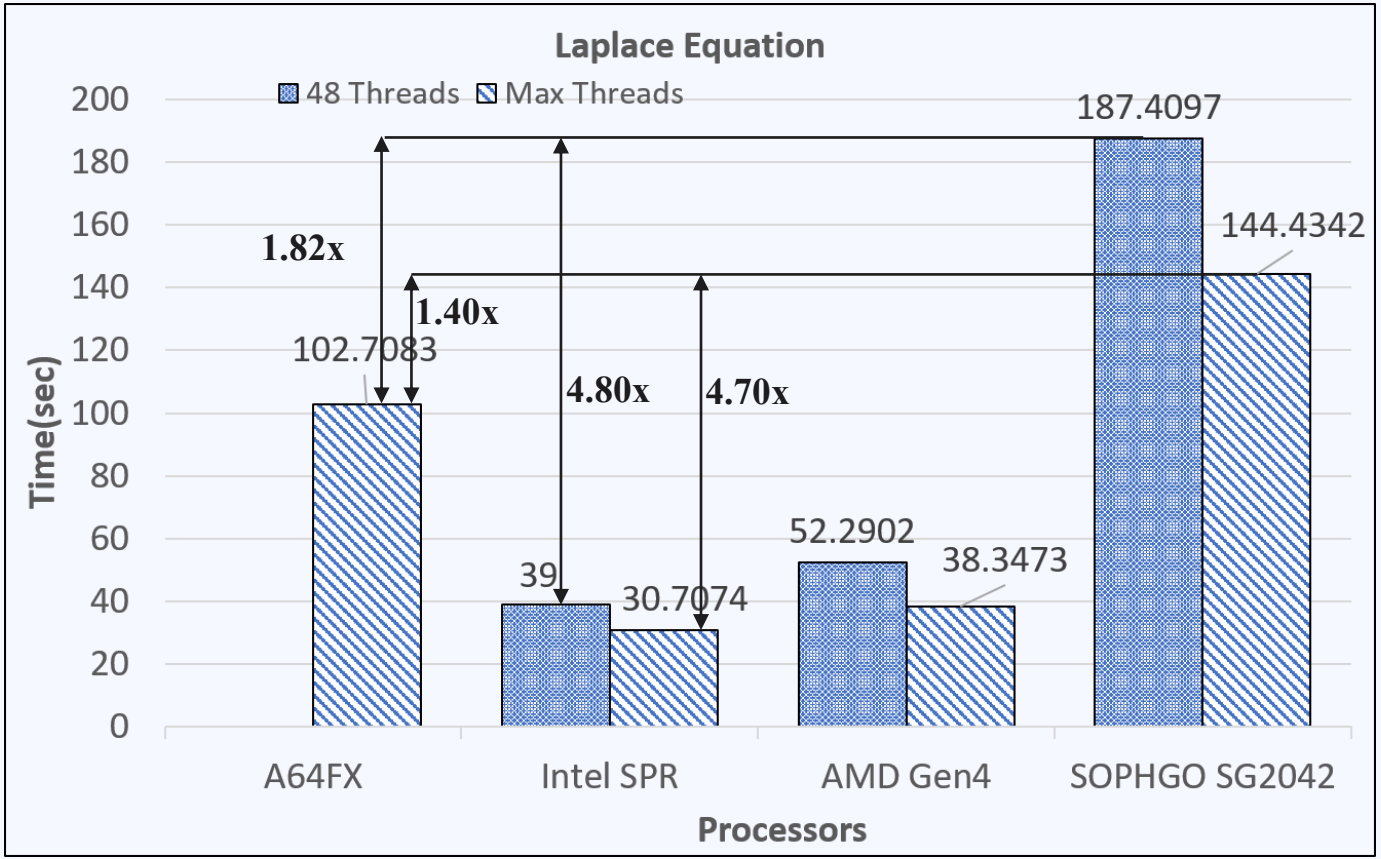
Performance Analysis of Convolution

Dwarf Covered: Structure Grid



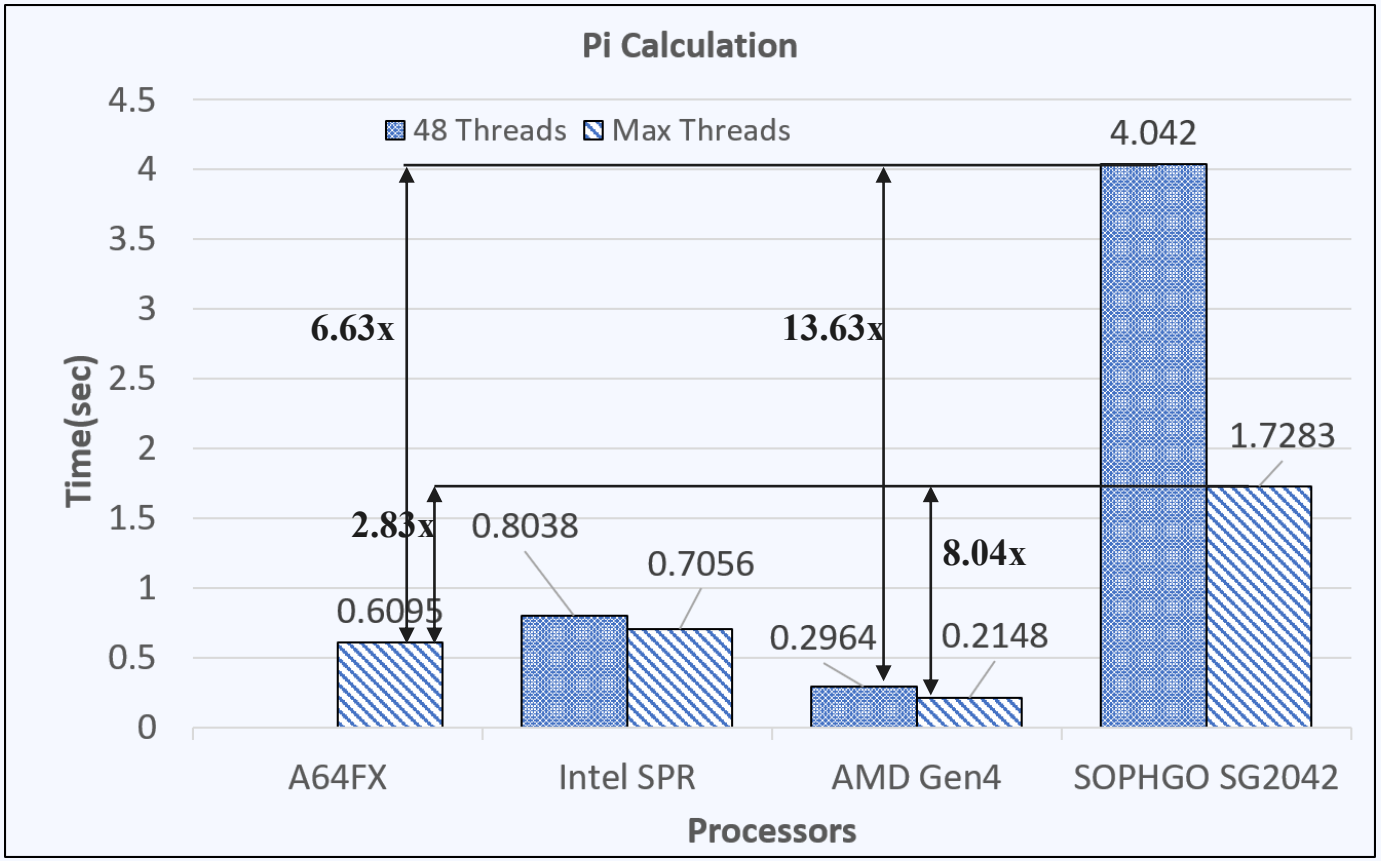
Performance Analysis of Laplace Equation

Dwarf Covered: Unstructured Grid



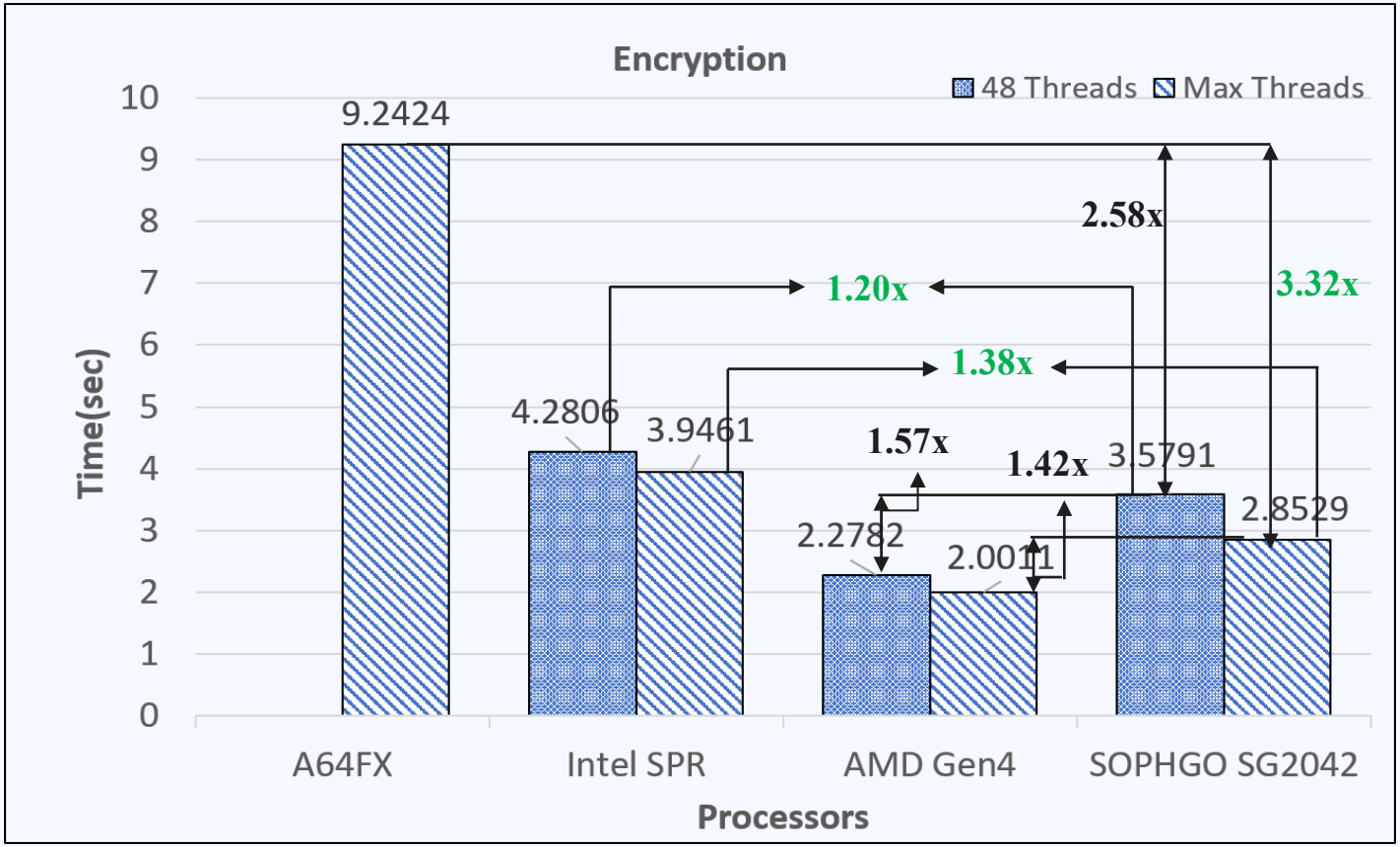
Performance Analysis of Pi Calculation

Dwarf Covered: Map Reduce



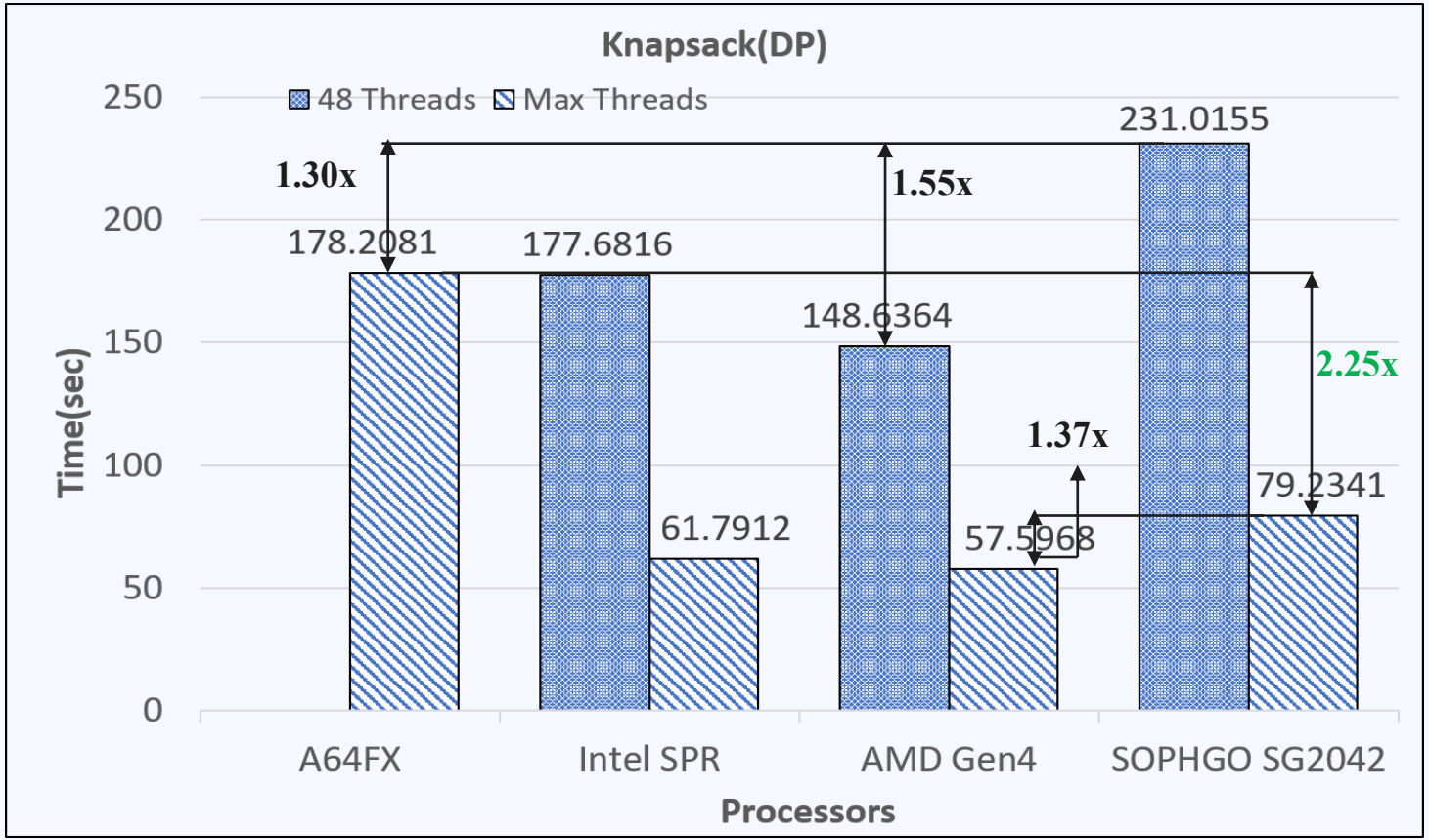
Performance Analysis of Encryption

Dwarf Covered: Combinational Logic



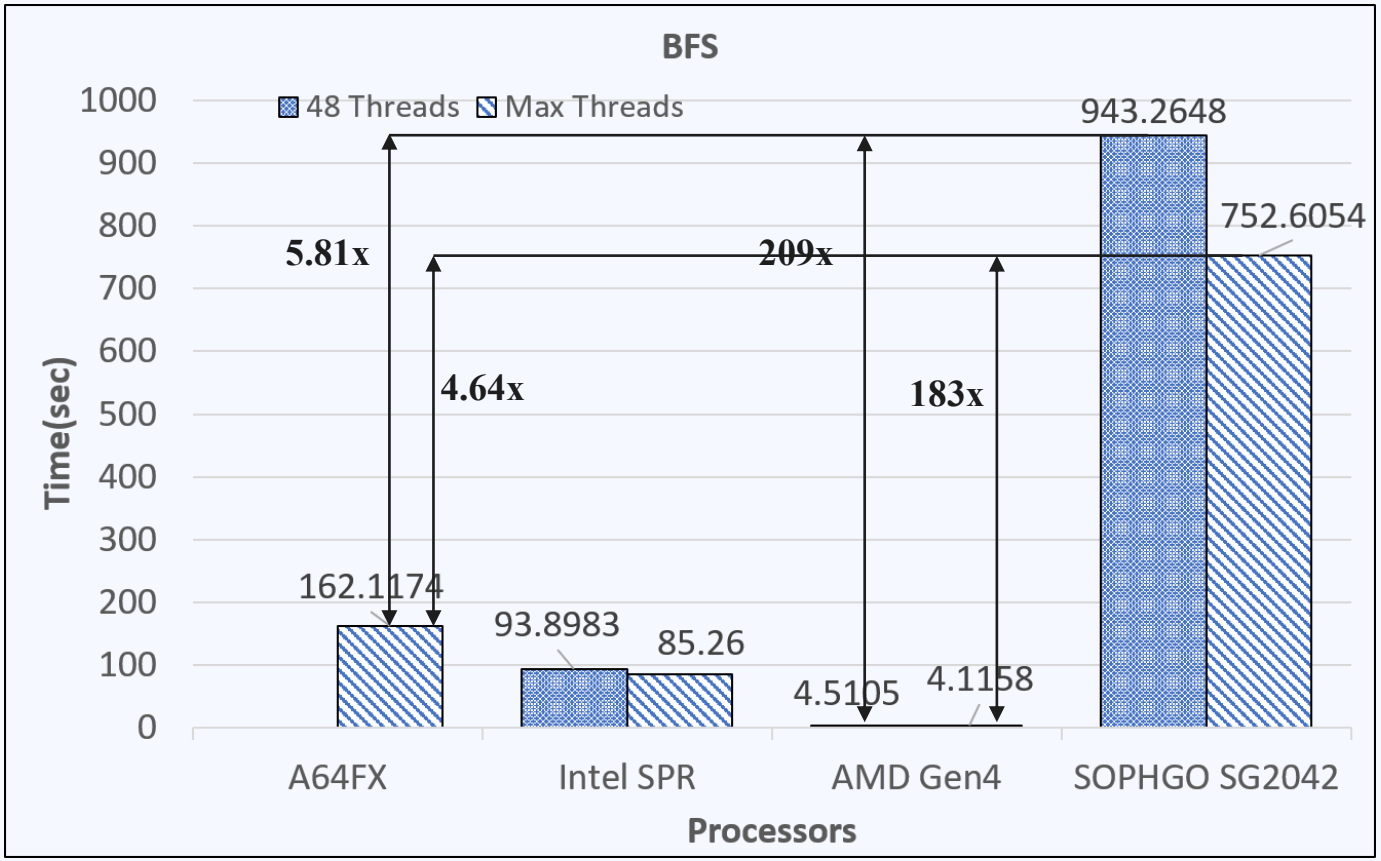
Performance Analysis of Knapsack(DP)

Dwarf Covered: Dynamic Programming



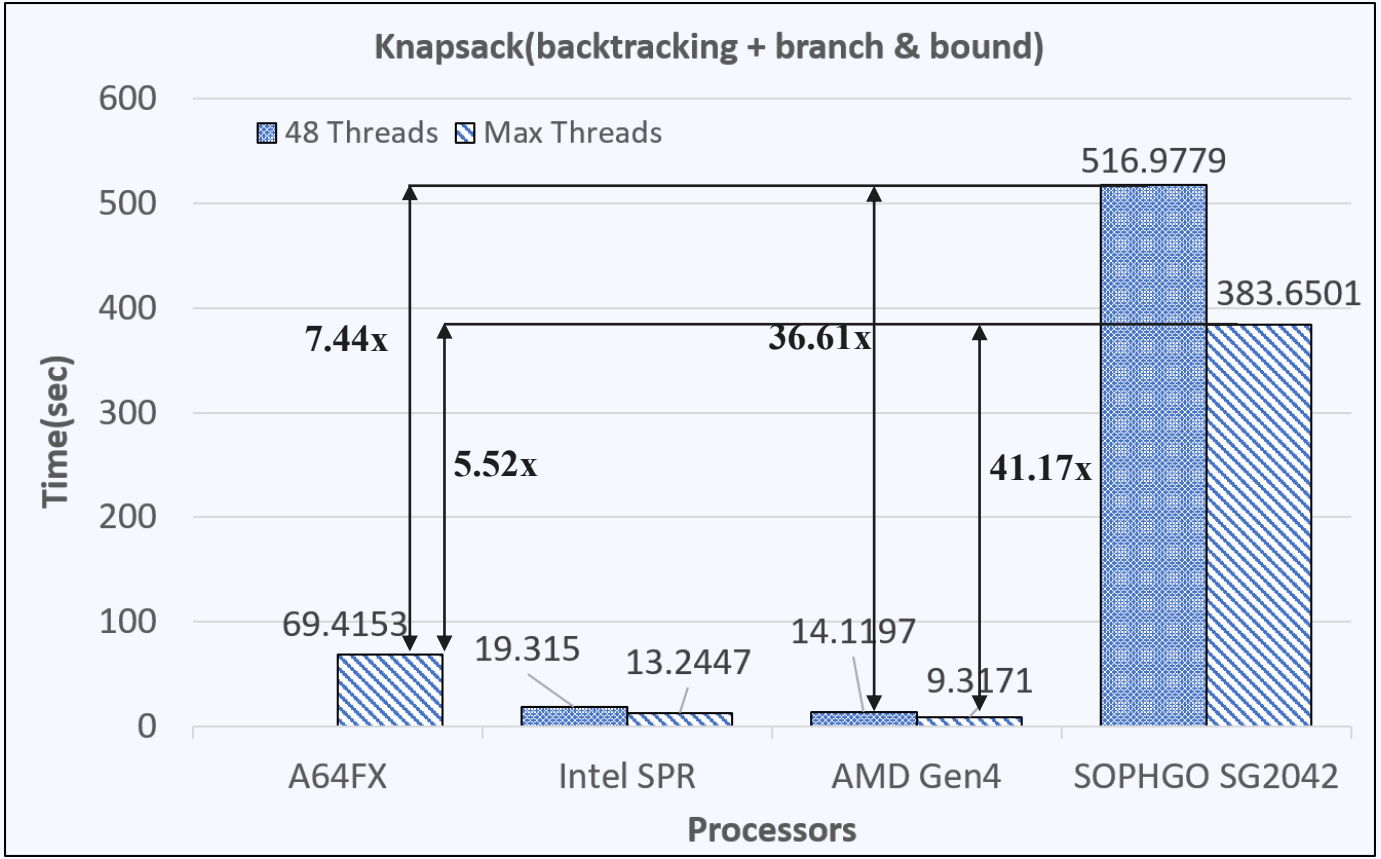
Performance Analysis of BFS

Dwarf Covered: Graph Traversal



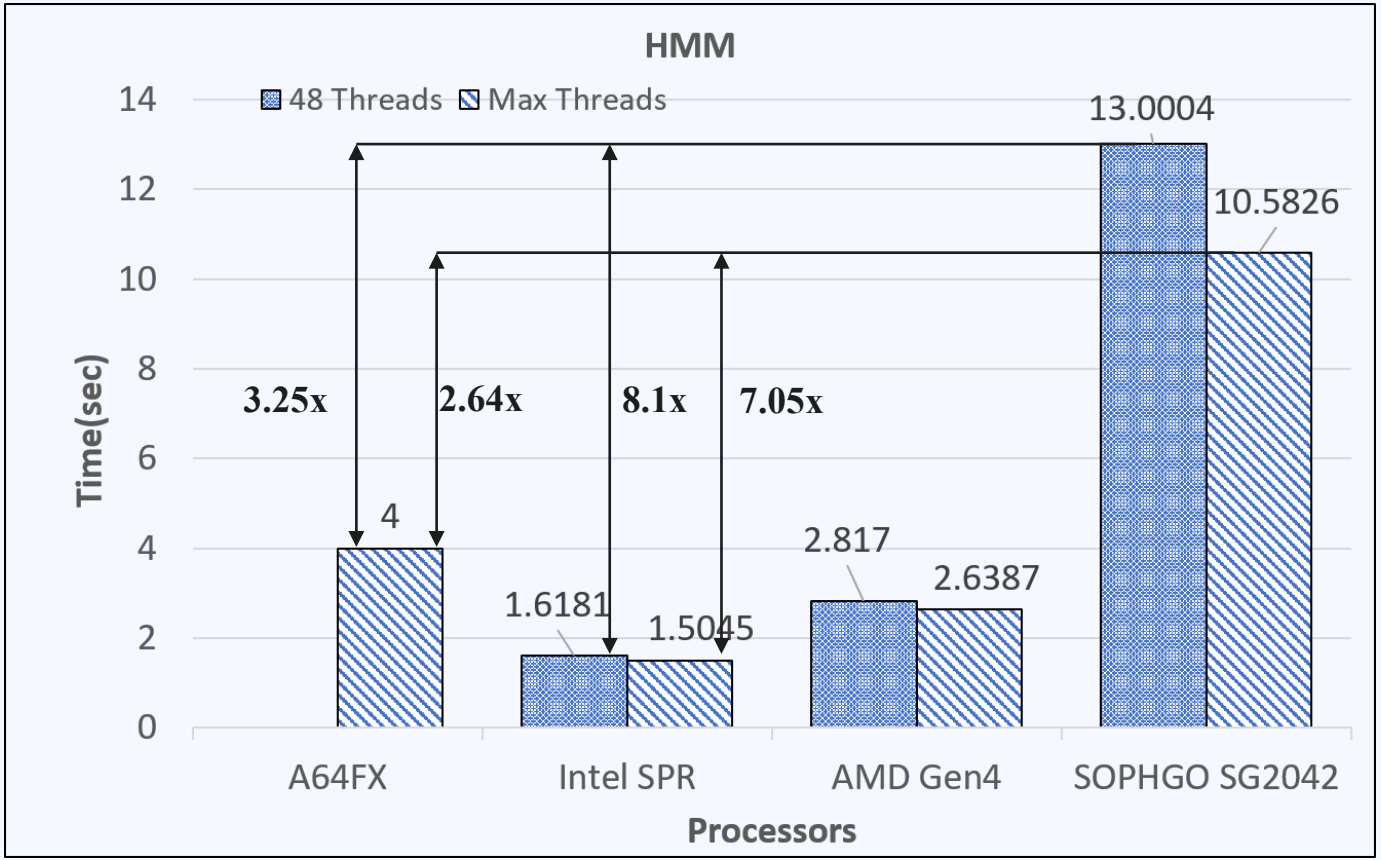
Performance Analysis of Knapsack_bb

Dwarf Covered: Backtracking & Branch and Bound

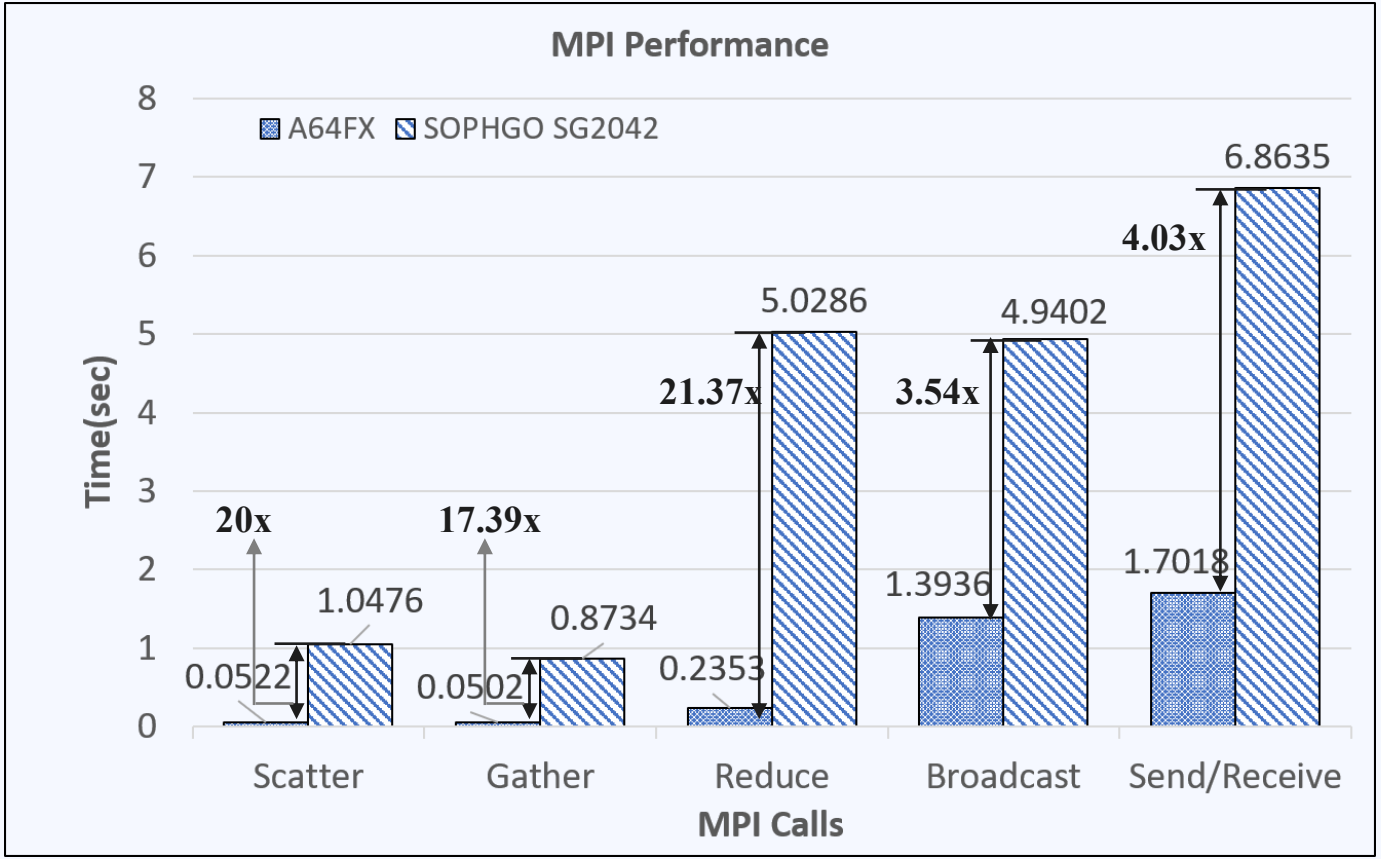


Performance Analysis of HMM

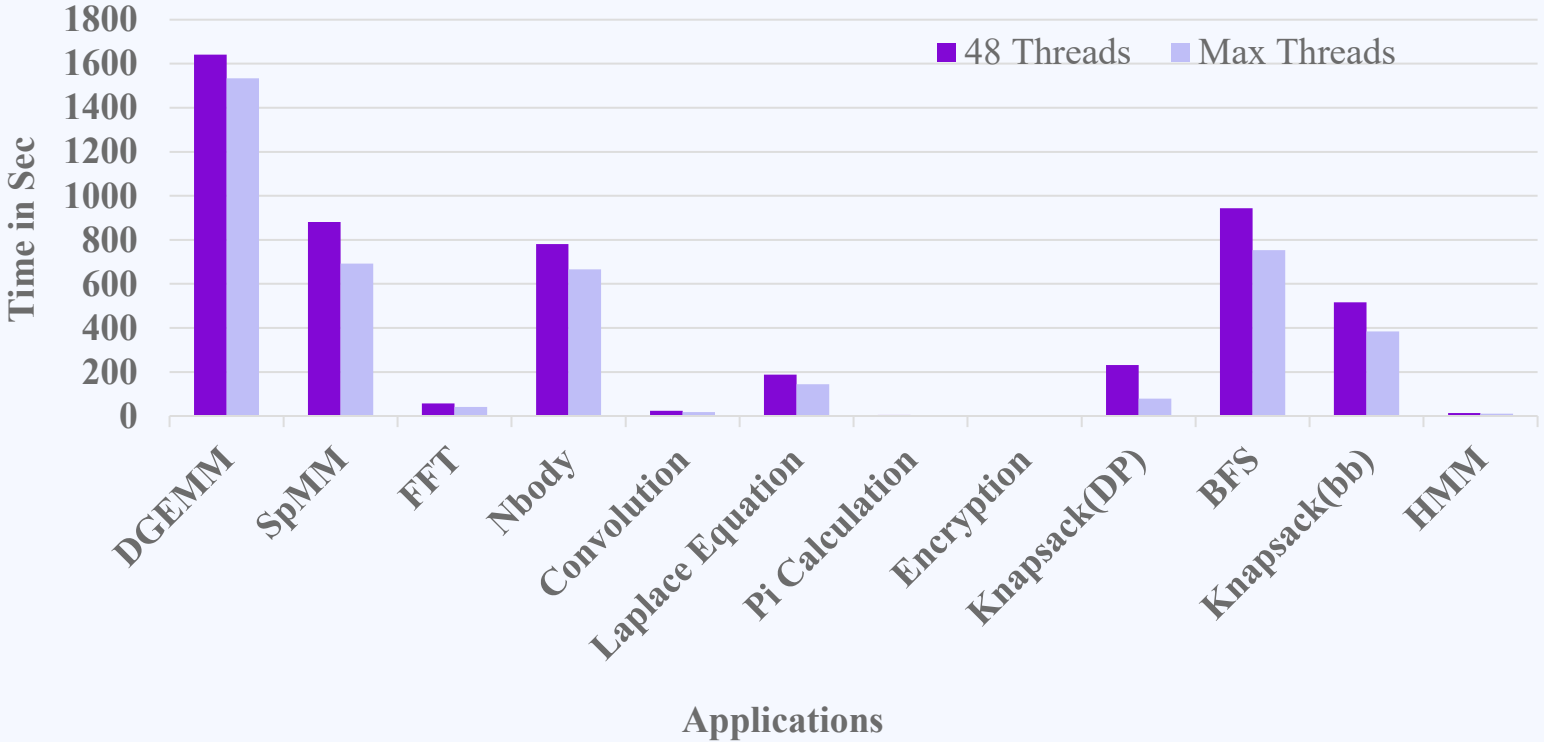
Dwarf Covered: Construct Graphical Models



Performance Analysis of MPI



Performance of SOPHGO with Increasing Thread Count



Performance gains after increasing thread count

Application Used	Intel SPR	SOPHGO SG2042
Dense Linear Algebra	1.09x	1.07x
Sparce Linear Algebra	1.271x	1.272x
Spectral Methods	1.44x	1.38x
Structured Grids	1.03x	**1.34x**
Unstructured Grids	1.27x	**1.29x**
N-body Simulations	1.12x	**1.17x**
Map Reduce	1.13x	**2.33x**
Combination Logic	1.08x	**1.25x**
Dynamic programming	2.87x	**2.91x**
Graph Traversal	1.10x	**1.25x**
Backtracking + Branch and Bound	1.45x	1.34x
Construct Graphical Models	1.07x	**1.22x**

Advantages of SOPHGO SG2042

Scales effectively with increasing thread count.

Delivers notable performance in combinational logic and dynamic programming.

Built on an open and customizable RISC-V ISA.

Low Power Design: Energy-efficient for light and mid-range compute workloads.

Bottlenecks of SOPHGO SG2042

- Memory bandwidth utilization remains low, with ~43% STREAM benchmark efficiency
- Insufficient architectural and compiler support for advanced SIMD vectorization
- Inefficient inter-node communication, with MPI operations considerably slower than on A64FX
- Software Ecosystem Gaps

Future Improvements

Adopt enhanced vector support in next-generation hardware to improve vectorization performance.

Leverage MPI across nodes and OpenMP within nodes to optimize memory usage and parallel performance.

Improve RISC-V HPC readiness by porting OpenMP to LLVM and tuning performance-critical libraries including math and communication Libraries.

Apply low-level kernel optimizations through RVV intrinsic, loop unrolling, prefetching, and cache-aware blocking techniques.

Conclusion

Evaluation Framework

Benchmarked SOPHGO SG2042 (RISC-V) using Berkeley Dwarfs against high-performance ARM and x86 processors.

Identified Strengths:

SG2042 excelled in combination logic and dynamic programming workloads.

Scaling Advantage:

Demonstrated better scalability compared to Intel Sapphire Rapids in nearly half of the evaluated dwarfs.

Future Outlook:

With advancing software support and ongoing optimization efforts, RISC-V is poised to become a competitive HPC architecture..

Thank You