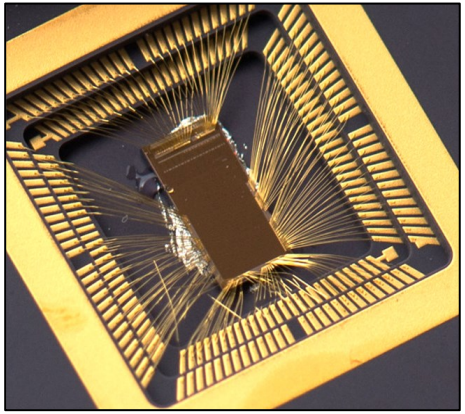
HPC from the RISC-V International perspective

Jeff Scheel - RISC-V Director of Technical Programs (jeff@riscv.org)
November 20, 2024

Global standards are a catalyst to accelerate technical innovation

Standards have been critical to technology innovation, adoption, and growth for decades

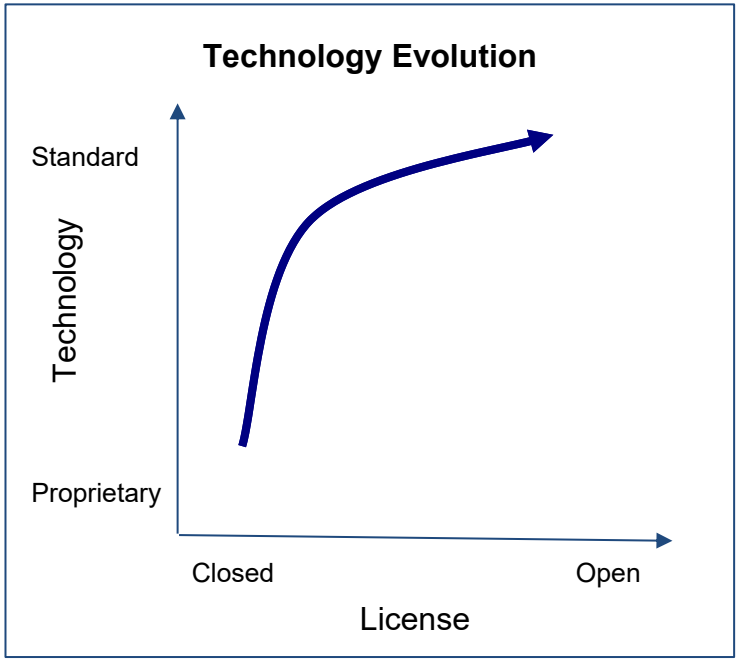
Standards create access to opportunities and spur growth for a wide range of stakeholders



RISC-V is a standards-defined Instruction Set Architecture developed by a global community

What's important about RISC-V?

Open standards are strategic for hardware and software



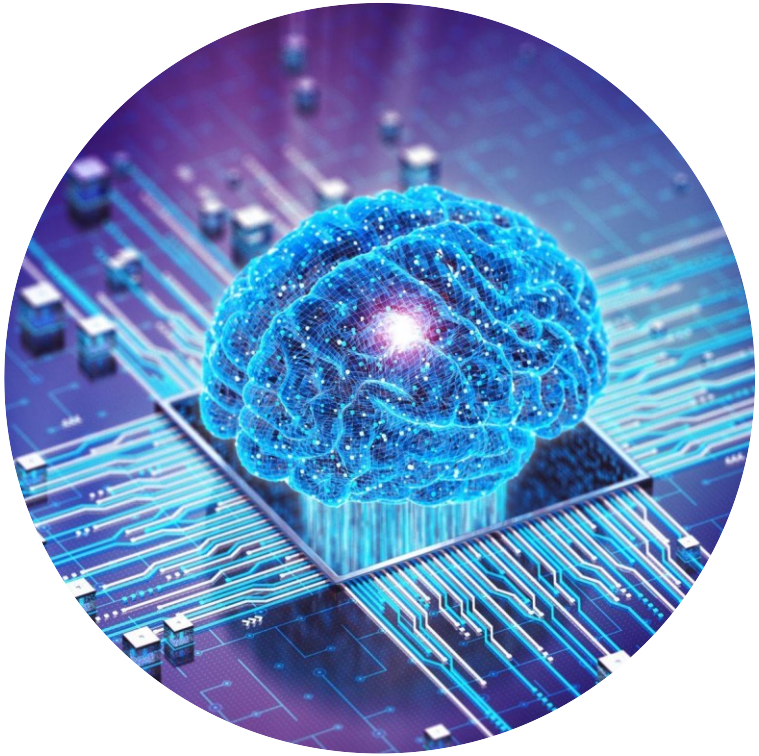
Open standards and **collaboration** are strategic to hardware and software **across industries** and **geographies**.

Entering the Era of Workload-designed Silicon

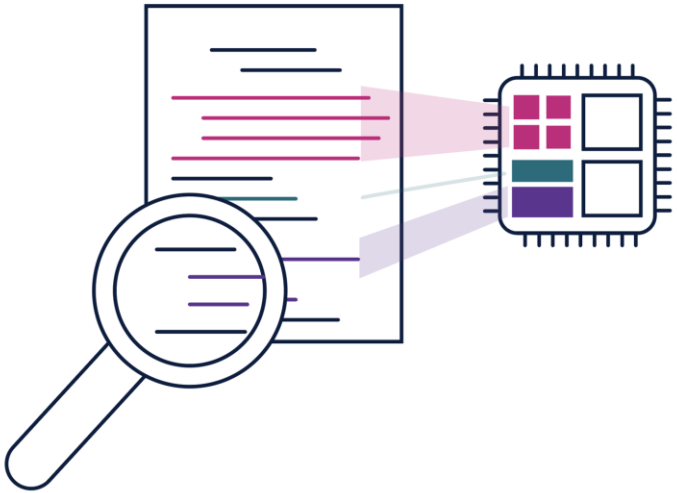
Mainframe

PC

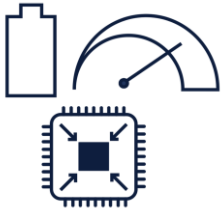
SoC



Workload-designed Silicon



Profile your workload, identify bottlenecks and optimize hardware & software architecture



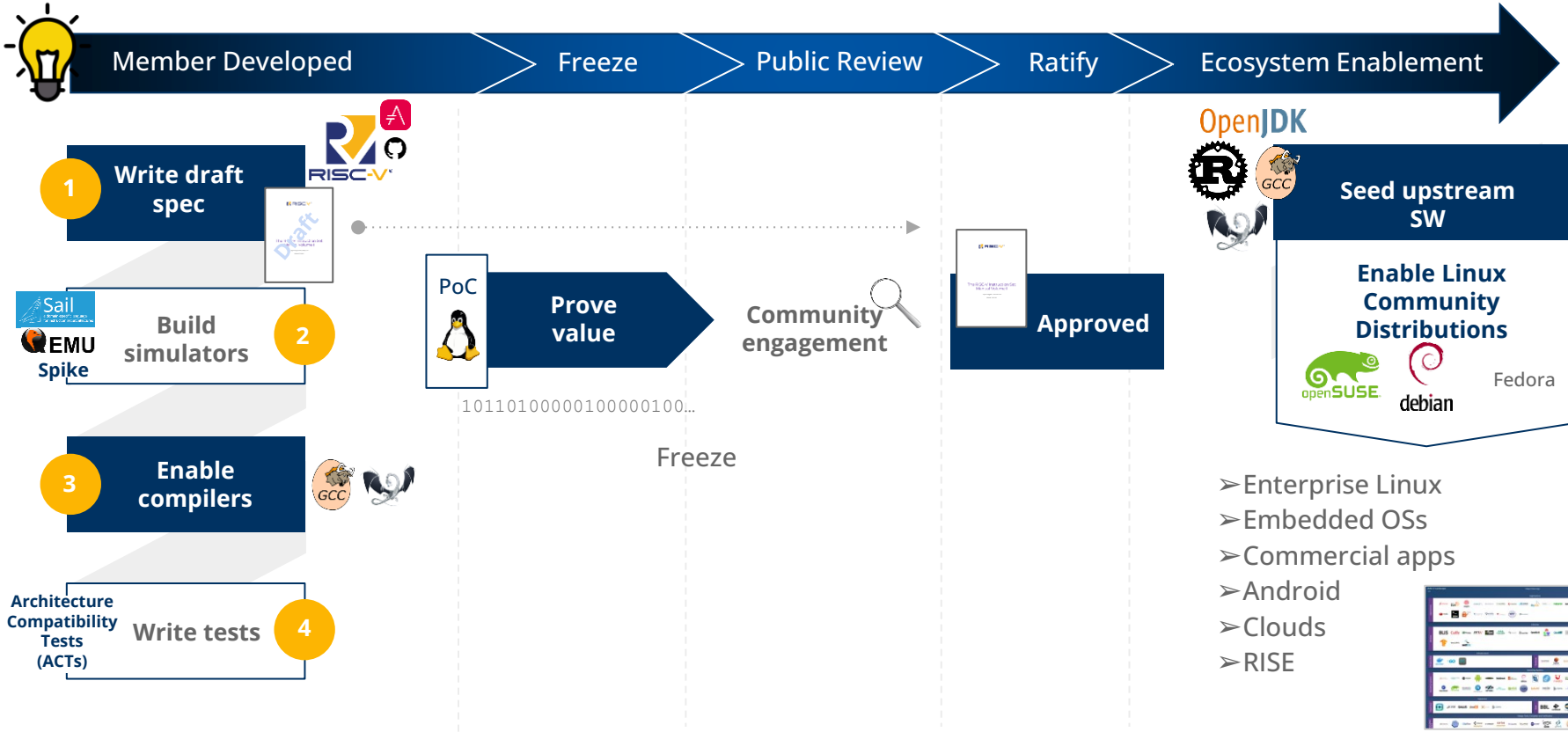
Better Power Performance Area

Optimize for scale from tiny IoT to HPC

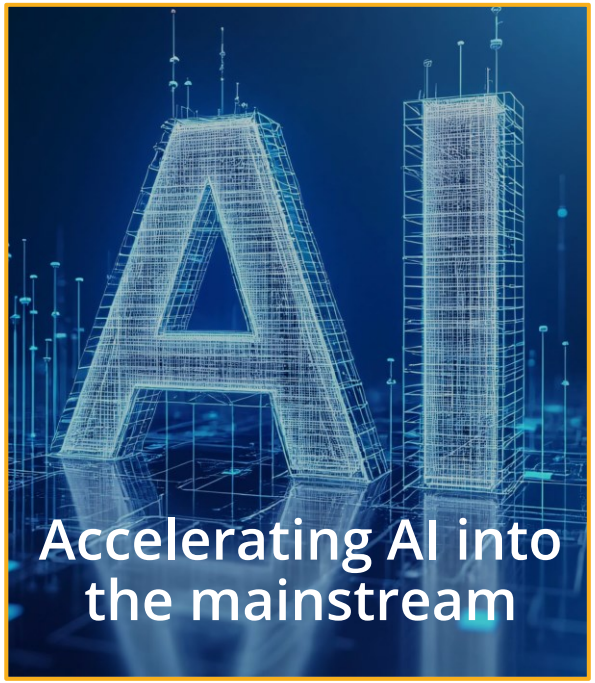
Shortened design cycles through collaboration in task groups

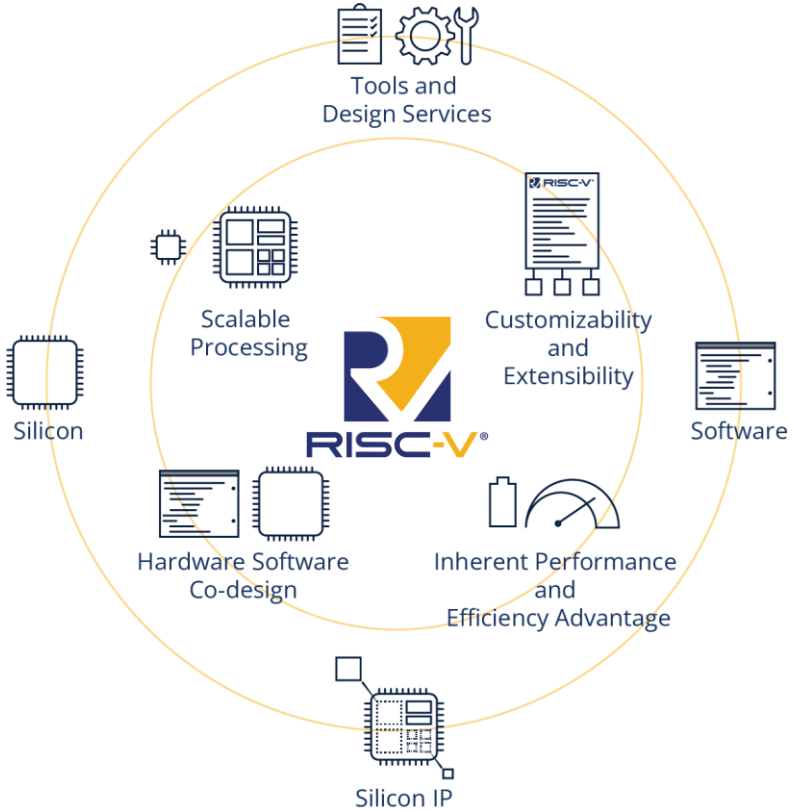
Design freedom and greater speed of innovation

RISC-V enables Linux, Linux enables the World



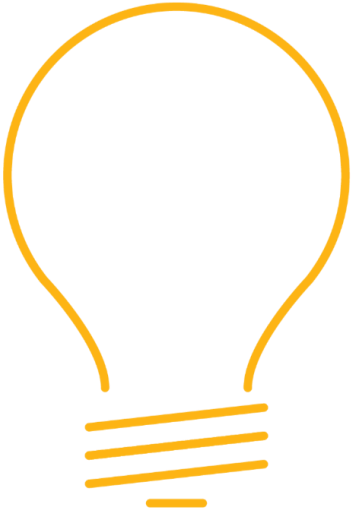
RISC-V is Redefining the Computing Landscape





RISC-V ISA and Ecosystem

+



Your Innovation

This is just the beginning.

This is your time, it starts now.

Thank you!


RISC-V®
Backup

What are the key, unique, benefits that RISC-V can offer to the HPC/AI community?

- RISC-V is an open standard where members decide what extensions should be designed
- RISC-V has been designed with extensibility/flexibility in mind. Extensions, Profiles, and (coming soon) Platforms.
- RISC-V enables open innovation

What are the most important challenges that must be solved for RISC-V to be adopted by HPC and AI?

Of course, the software ecosystem: that is understood

BUT we need to

- Ensure people recognize RISC-V as an innovation catalyst instead of "just another platform"
- Continue to modify software to support the base platform and identify the owners for places when continued optimization is required

What specific parts of the RISC-V ecosystem should the HPC/AI community be looking to influence and would benefit from our contribution?

- Tough question, but a few thoughts:
  - First, HPC-specific ISA Extensions not yet considered on ANY platform
  - Second, open source processor designs for HPC as basic building blocks
  - Third, SOC designs specific for HPC compute
- Other ideas:
  - Heterogeneous core SOCs
  - Specialized "in-band" acceleration nodes
  - Standard open hardware "framework" for CPU/SOC design
  - Your "crazy idea"

Processors

esperanto.ai

ET-SoC-1 inference chip with over a thousand RISC-V processors on a single chip, delivering a massively parallel, flexible architecture for AI and HPC

InspireSemi™

Thunderbird “supercomputer cluster-on-a-chip” accelerated computing architecture is based on an array of thousands of modern, efficient, and powerful 64-bit RISC-V CPU cores

tenstorrent

Tenstorrent ultra high performance RISC-V CPUs and AI accelerators for AI and HPC

semidynamics

silicon design and verification services

Semidynamics' Atrevido™ 423 RISC-V processor core for AI and HPC workloads, which typically need to rapidly access very large amounts of data from memory

VENTANA

Veyron V2 high performance RISC-V processor, offered in the form of chiplets and IP. Features industry leading UCIe chiplet interconnect, and Domain Specific Accelerator technology

算能
SOPHGO

SOPHON SG2042 features 64 RISC-V cores, up to 32 PCIe Gen 4.0 channels. Available on Milk-V Pioneer board in standard mATX form factor Pioneer Box for developers now!

Brazil

Government

Universities & Research Institutes

Companies

- RISC-V is at the core of Brazil's strategy
- Brazil is leading Latin America in RISC-V adoption
- Brazilian AI Act allocates over USD 100 million for RISC-V-based accelerators
- Brazil's major semiconductor training program uses RISC-V
- Leading R&D institutions have fully embraced RISC-V
- Numerous public and private universities have integrated RISC-V into their curricula

China

Projects

Universities & Research Institutes

Alliances

Companies

成为资本 CHENGWEI CAPITAL

PLCT Lab

- BOSC One Student One Chip (OSOC) initiative teaches undergraduate students to build real chips
- Xiangshan Open Source processor targets high performance applications, with the third generation (Kunminghu) under development
- PLCT Lab a member of RISC-V Labs, providing computing resource to developers

Europe

Government & Agencies

Projects & Initiatives

Companies & Alliances

- Chips-JU Tristan and Isolde projects targeting industrial and high performance processors
- European Processor Initiative for low-power European processors targeting high performance computing
- New HORIZON-JU project targeting high performance RISC-V Automotive Processors
- Quintauris formed to advance the adoption of RISC-V by Robert Bosch GmbH, Infineon Technologies AG, Nordic Semiconductor ASA, NXP® Semiconductors, STMicroelectronics, and Qualcomm Technologies, Inc.
- European Space Agency adopting RISC-V with Frontgrade Gaisler

USA

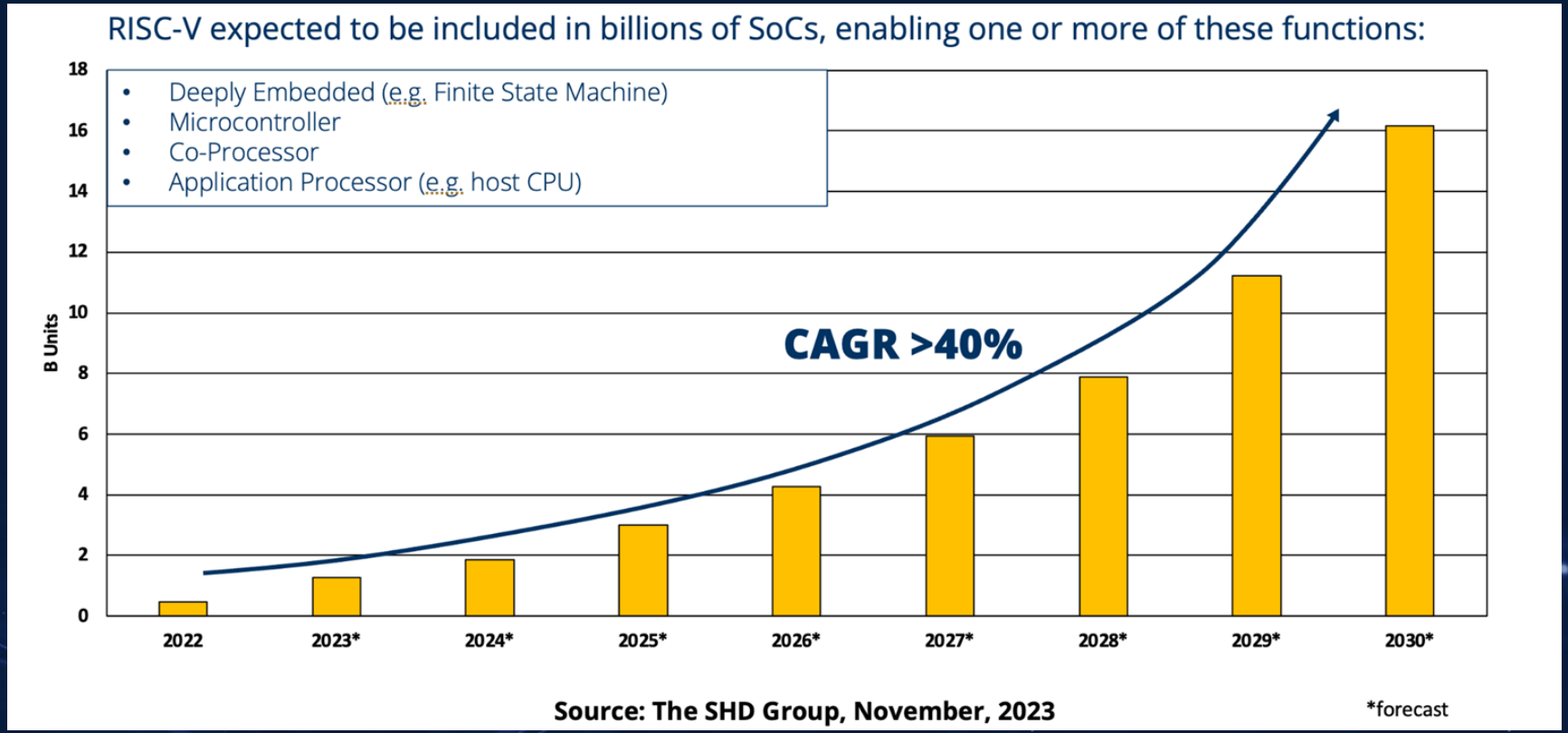
Universities & Research Institutes

Projects

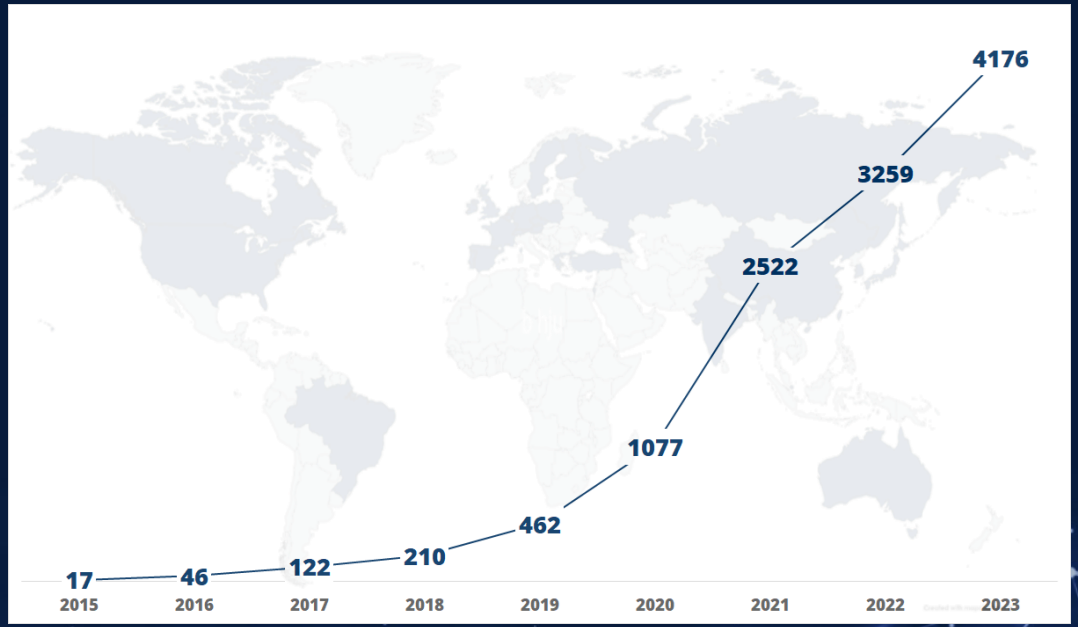
Companies

- RISC-V originally developed at UC Berkeley, initially for research and education
- RISC-V adopted by existing tech companies, and a new generation of startups
- Microchip selected by NASA to develop a High-Performance Spaceflight Computing processor, which features SiFive CPU cores

RISC-V will be in more than 16 billion SoCs by 2030



More than 4,100 RISC-V Members across 70 Countries



Dec 2023 update

121 Chip
SoC, IP, FPGA

4 Systems
ODM, OEM

3 I/O
Memory, network, storage

14 Industry
Cloud, mobile, HPC, ML, automotive

23 Services
Fab, design services

165 Research
Universities, Labs, other alliances

59 Software
Dev tools, firmware, OS

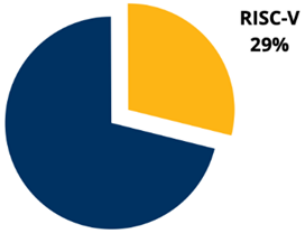
3k+ Individuals
RISC-V engineers and advocates

RISC-V membership up 28% in 2023

RISC-V®

Selected Market Share Projections for RISC-V in 2030

Wearables
MCU

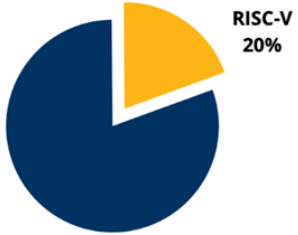


TAM: 2.6B units

Computing
Notebooks

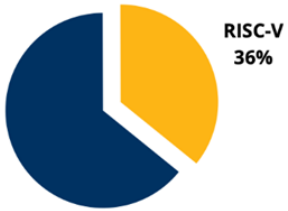
TAM: 2.7B units

Communications
5G Infrastructure



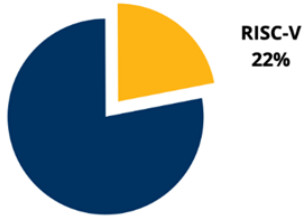
TAM: 1.8B units

Consumer
AI Acceleration



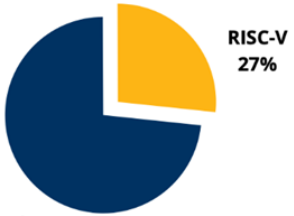
TAM: 6.4B units

Industrial
Smart Grid



TAM: 670M units

Automotive
AI Acceleration



TAM: 260M units

Based on projected SoC volumes

Source: The SHD Group, November, 2023

the SHDgroup

New RISC-V processors

Codasip

Codasip first commercial CHERI security implementation

semidynamics
silicon design and verification services

RISC-V Tensor Unit for ultra-fast AI solutions

SiFive

Performance P870 and Intelligence X390 for generative AI and ML

VENTANA

Data center CPU chiplet solution with I/O hub, DDR memory, PCIe, up to 192 cores

芯来科技 NUCLEI

NA900 certified compliant ASIL D of ISO 26262 standard

Tiempo SECURE

TESIC RISC-V IP passes SERMA CC EAL5+ security tests

CAST

BA5x™ RISC-V processors for low power and EMSA5-FS for functional safety

ICT

Use of AI to design RISC-V CPU in under 5 hours

Applications

Qualcomm RISC-V wearable platform with Google Wear OS

First generative AI RISC-V appliance

RISC-V tablet, portable Linux console, and cluster

Vega, the first RISC-V 10 gigabit Ethernet switch

First RISC-V IoT security Towngas Chip has sold over 1,000,000 units

Two self-developed RISC-V communications chips

Andes N25F for performance and low power in enterprise SSD controller, AndesCore™ RISC-V multicore vector processor

MTIA v1: Meta's first generation AI inference accelerator

Developers

Android added RISC-V to list of supported CPU architectures

ASUS IoT Tinker V board based on AndesCore AX45MP

Industrial edge solutions including High Level Synthesis for C/C++, vector SDKs for AI/ML inferencing

Debian GNU/Linux officially Supported on RISC-V architecture

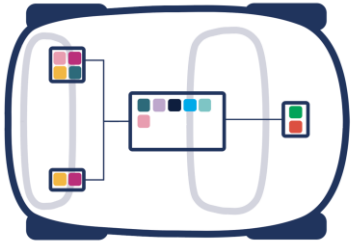
BeagleV Ahead single board computer released

Terapines ZCC toolchain supports Andes RISC-V processors

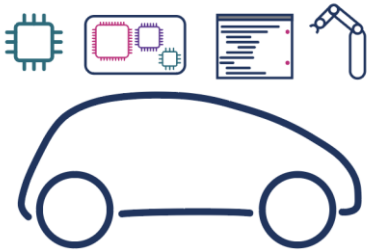
Imperas to Provide Simulation Model of Tenstorrent Ascalon RISC-V Core

nanoCH32V003 is a sub 10c 32-bit RISC-V microcontroller with a $1.50 dev board available

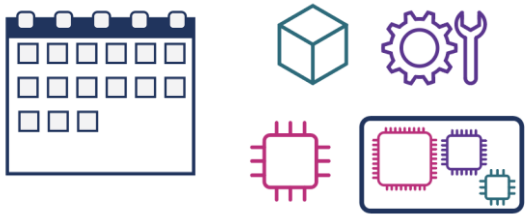
Industry outlook: Automotive



RISC-V scales across every compute application in the vehicle



RISC-V enables the supply chain to work together while enabling innovation and differentiation



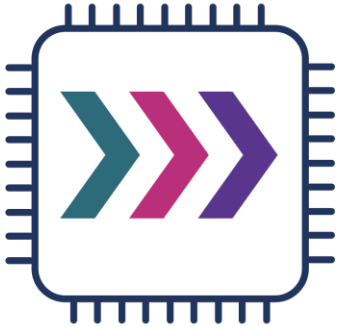
Ecosystem offers wide breadth of choice, as well as support and expertise required for auto

RISC-V will capture 27% of automotive AI acceleration by 2030

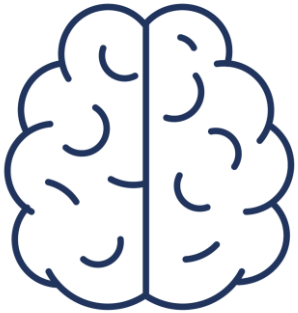
The SHD Group, November 2023

RISC-V®

Industry outlook: Datacenter & Cloud



RISC-V offers unique opportunity for accelerators



Custom computing for AI and other emerging workloads

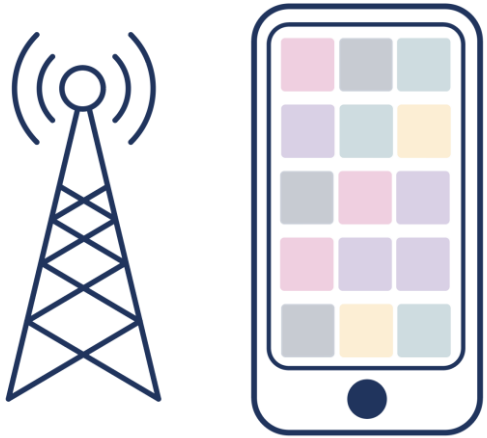
Achieve your performance and power targets

RISC-V CPU core market will grow 115% CAGR, capturing >14% of all CPU cores by 2025

Semico Research, December 2021

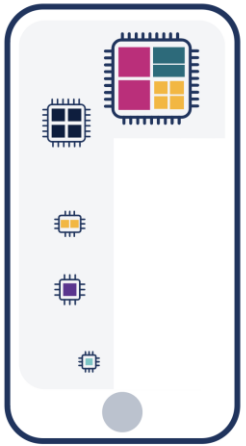
RISC-V®

Industry outlook: Telecom & Consumer Devices



Innovation across the industry, from handsets to infrastructure

Android support



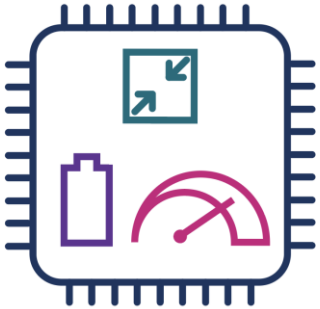
Diverse smartphone workloads, from central processing to connectivity to sensors

RISC-V will capture 20% of Communications 5G infrastructure by 2030

Semico Research, December 2021

RISC-V®

Industry outlook: Internet of Things



Streamlined instruction set enables efficient and compact code for improved performance and energy efficiency

Strong fit for localized workloads such as machine learning, sensors, and security

Advanced custom processing for workloads like AI to run at the edge

RISC-V will command 28% of the IoT market by 2025

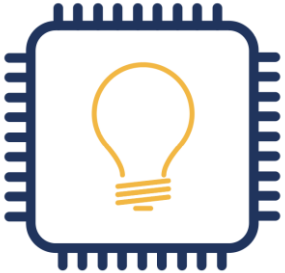
Counterpoint Technology Market Research, September 2021

By 2028, the number of RISC-V processors shipping into IoT will approach 20 billion

Omdia Research, May 2022

RISC-V®

Industry outlook: HPC



HPC is on the technology leading edge requiring customized hardware solutions for many HPC domains

HPC is tackling grand challenges that benefit from the Global Technology ecosystem

An Open ISA complements Open Source Software and combines to create an open Ecosystem

SIG-HPC Vision & Mission: RISC-V: IoT to HPC

Vision:
The technical and strategic imperatives that guide the RISC-V ecosystem development to enable an Open HPC Ecosystem...

Mission:
...enable RISC-V in a broader set of new software and hardware opportunities in the High Performance Computing space, from the edge to supercomputers, and the software ecosystem required to run legacy and emerging (AI/ML/DL) HPC workloads.

HPC in Europe

EuroHPC
Joint Undertaking

European
Processor
Initiative

HPC Projects

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

The definition of open computing is RISC-V

RISC-V is the most prolific and open Instruction Set Architecture in history

RISC-V is inevitable

Mission: RISC-V is the industry standard ISA across computing

- Adoption moving rapidly across all domains
- Demand at every performance level (low to ludicrous)
- Shared investment driving ecosystem

RISC-V enables the best processors

RISC-V enables profound innovation from low end to high end applications

- Inherent and sustainable performance and efficiency advantage
- Design flexibility and freedom
- Supported by massive community enabling the most efficient designs for full spectrum of applications
- Modern design for fewer instructions

RISC-V is rapidly building the strongest ecosystem

RISC-V instrumented with software top of mind

- Open standards enable software choice Applications keen to run on RISC-V.
- Toolchain and OS support required for Extension ratification
- Single hypervisor standard to simplify and unify application support
- Thousands of software developers
- Strategic investment by industry and geographies

RISC-V®

Building the strongest ecosystem

Total market cap of $5.5T

Funding of $8.5B

landscape.riscv.org

Engage with RISC-V

Join RISC-V as a member
www.riscv.org

Elevate Industry Leadership

- Deepen expertise in Special Interest Groups
- Show technical and industry leadership
- Leverage Industry Market development
- Engage global reach of RISC-V marketing, media, and social channels

Achieve Business ROI

- Reduce technical overhead and accelerate roadmap with global open standard
- Reduced strategic risk implicit in collective investment of global stakeholders
- Accelerate sales pipeline with RISC-V support across channels
- Showcase solutions on RISC-V Exchange and Ecosystem Landscape
- Qualify products as RISC-V Compatible™

Build Strategic Network

- Cultivate partner, supply chain and customer strategic relationships
- Align and leverage global, local and industry networks, alliances, and events
- Amplify visibility online, and at events

Gain Technical Advantage

- Gain insight and access to technical deliverables in motion
- Infuse your technical directions in specifications
- Accelerate technical knowledge working with domain experts, cultivate and retain talent
- Be part of local developer groups and industry developer networks