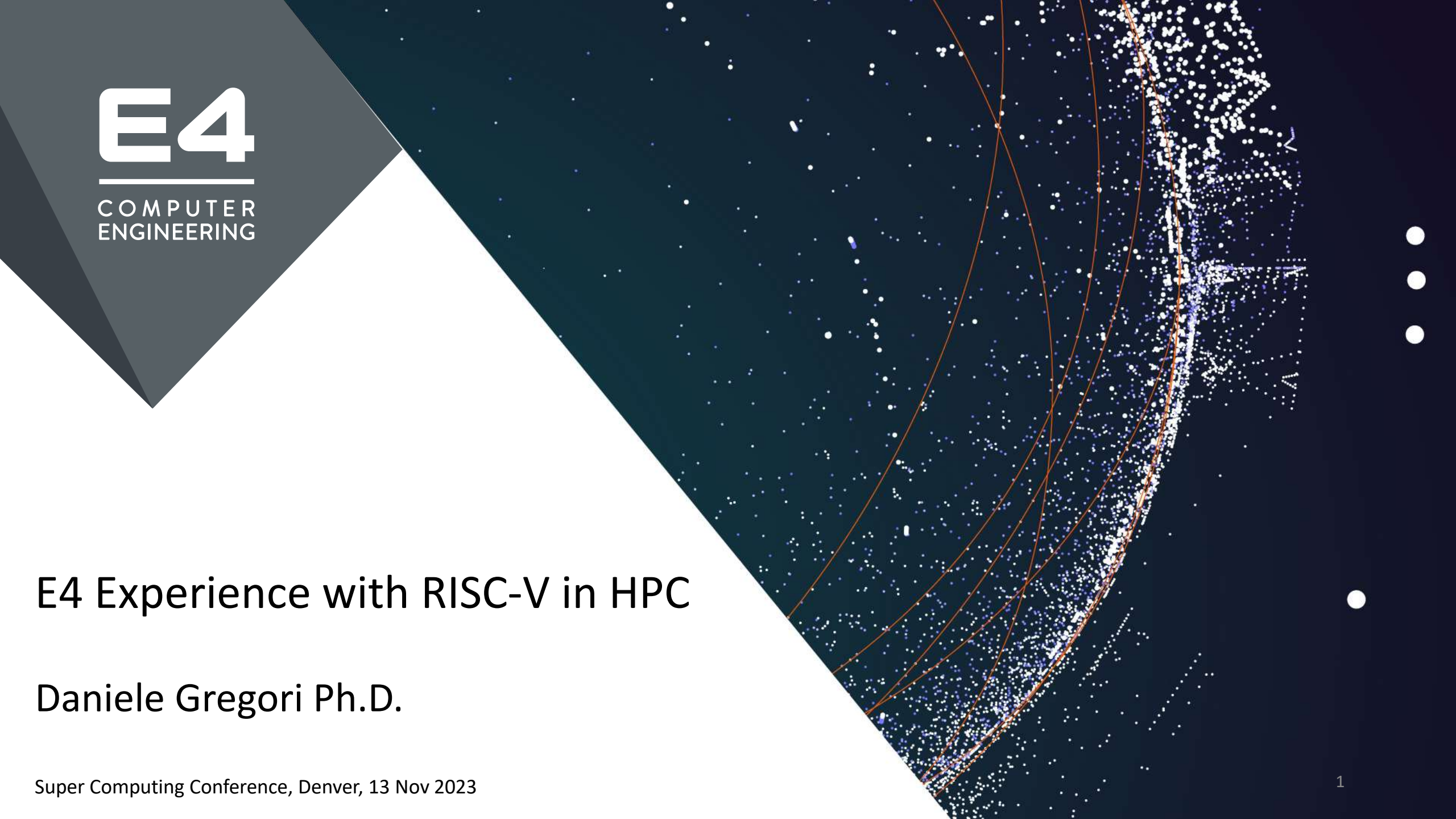


E4 Experience with RISC-V in HPC

Daniele Gregori Ph.D.

Super Computing Conference, Denver, 13 Nov 2023

E4 IN A NUTSHELL

20 YEARS ANNIVERSARY
2002 - 2022

Strategic Members
https://riscv.org/

WHO WE ARE
E4 Computer Engineering designs and manufactures highly technological solutions for HPC Clusters, Cloud, Data Analytics, Artificial Intelligence and Hyper-Converged infrastructure for the Academic and Industrial markets. We have been collaborating for years with the main research centers at national and international level (Cineca, CERN, ECMWF, LEONARDO) and we are involved in national and European projects in the HPC and AI fields (EuroHPC JU EPI, EUPEX, Horizon Europe)

VISION
We explore future scenarios to find solutions for highly performing computational needs in application areas that are unimaginable today.

MISSION
We anticipate the ever-accelerating disruptive transformation of our era, providing mature solutions in sophisticated technological contexts with a dizzyingly innovative approach

APPROACH
Each E4 solution is UNIQUE, like each of our customers; TESTED in every single component; VALIDATED to verify the actual performance of each system and SERVED by technicians who provide assistance in the most extensive and complex Italian and European computing infrastructures.

E4 TECH FACTORY

- Integration Facility where our technicians build servers or storage systems
- Burn In Room to improve E4 systems reliability with at least 72 hours of test that involves all components
- R&D Lab, with 6 standard racks with heterogeneous systems, 100kW, remote access available on demand to perform benchmarking, co-design, prototyping

E4 PROTOTYPE – MONTE CIMONE RISC-V CLUSTER (2022)

https://www.e4company.com/en/2021/12/e4-announces-breakthrough-innovative-technologies-spanning-silicon-software-and-power-management-tools-integrated-in-the-risc-v-based-monte-cimone-cluster/

Preprint "Monte Cimone: Paving the Road for the First Generation of RISC-V High-Performance Computers" available online: http://arxiv.org/abs/2205.03725

Paper: https://ieeexplore.ieee.org/document/9908096

E4 is at the forefront of the adoption of RISC-V,
E4 is a strategic Member of the RISC-V Foundation

- The accelerator of EPI/SGA2
- In-house R&D
- First real HPC cluster
- Early adopters as main target

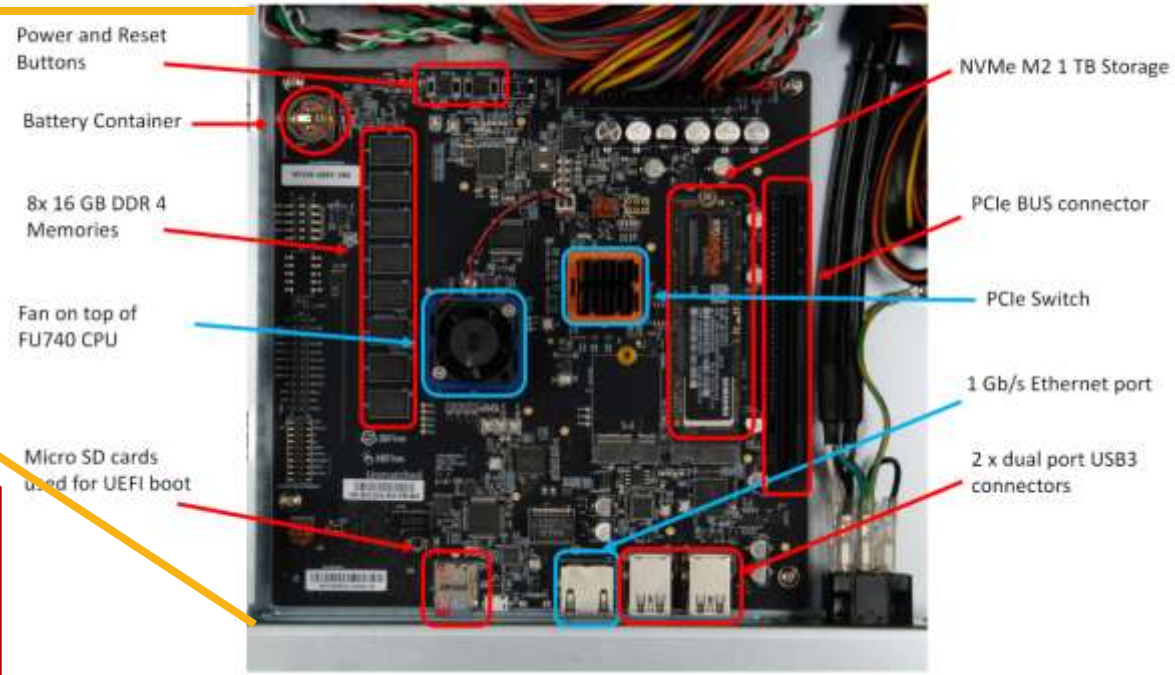
Monte Cimone was built by E4 and is currently operated by Bologna University

QUESTION:

How mature is the RISC-V ecosystem? Is the **RISC-V ecosystem mature enough to build HPC production clusters**?

THIS WORK:

We designed and built Monte Cimone, the first physical prototype and test-bed of a complete RISC-V (RV64) compute cluster integrating compute, interconnect, *a complete software stack for HPC and a full-featured* ***system monitoring infrastructure***.



4x E4 RV007 1U Custom Server Blades:

- **2x SiFive U740 SoC** with **4x U74 RV64GCB** cores
- 16GB of **DDR4**
- 1TB node-local **NVME storage**
- **PCIe expansion** card **w/InfiniBand HCAs**
- **Ethernet networks**

RESULTS:

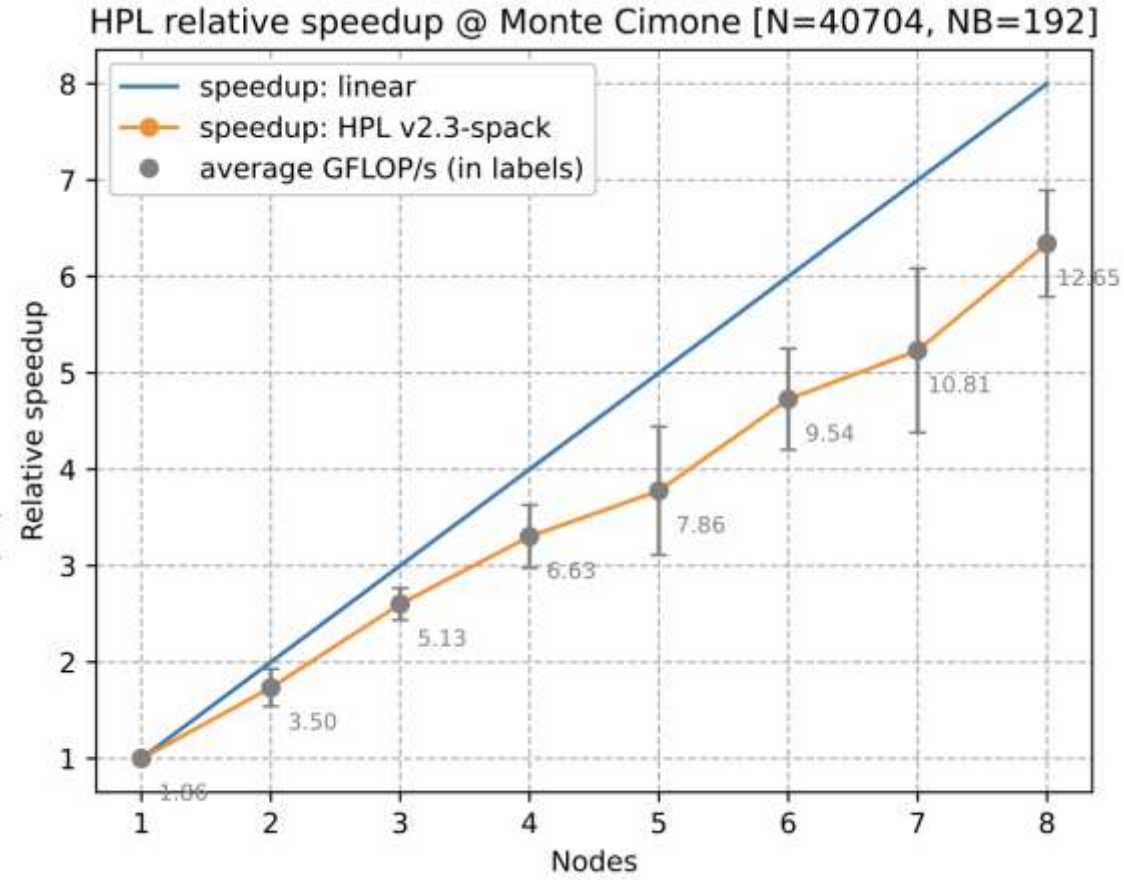
We Installed Ubuntu 21.04, deployed from riscv64 server images without modifications and mount a remote NFS. We leveraged the Spack package manager to deploy the full software stack and make it available to all system users via environment modules. We installed also SLURM and LDAP**.**
ISSUE: ***Infiniband card*** *does not work properly!*

Deployed Packages

Package	Version
gcc	10.3.0
openmpi	4.1.1
openblas	0.3.18
fftw	3.3.10
netlib-lapack	3.9.1
netlib-scalapack	2.1.0
hpl	2.3
stream	5.10
quantumESPRESSO	6.8

Stream Test Results

Test	STREAM.DDR	STREAM.L2
	1945.5 MiB [MB/s]	1.1 MiB [MB/s]
copy	1206 ± 3.26	7079 ± 2.11
scale	1025 ± 4.94	3558 ± 3.72
add	1124 ± 4.93	4380 ± 3.72
triad	1122 ± 5.63	4365 ± 3.56



HPL strong scaling tests on Monte Cimone. Average attained throughput values are shown in labels. Standard deviations are calculated on 10 repetitions.

CONCLUSIONS:

With Monte Cimone, the first physical prototype and test-bed of a complete RISC-V (RV64) compute cluster, *we demonstrated that it is possible to run real-life HPC applications on a RISC-V system today.*

MISSION:

Making high-performance RISC-V processors and accelerators ready for future RISC-V-based HPC systems.

Meet Monte Cimone: exploring RISC-V high performance compute clusters. CF'22

Monte Cimone: Paving the Road for the First Generation of RISC-V High-Performance Computers https://arxiv.org/abs/2205.03725

E4 SUPPORTED STUDENT CLUSTER COMPETITION 2022 WITH MONTE CIMONE

https://www.nextplatform.com/2022/06/09/strong-showing-for-first-experimental-risc-v-supercomputer/

https://arxiv.org/abs/2205.03725

https://open-src-soc.org/2022-05/media/slides/RISC-V-International-Day-2022-05-05-11h05-Calista-Redmond.pdf

NEXT STEPS IN THE RISC-V WORLD

E4 is member of the TRISTAN & ISOLDE (2023-2025) consortia to develop a European RISC-V Framework for the Space Use Case
https://tristan-project.eu/
https://www.isolde-project.eu/

E4 is member of the DARE (2024-2030) consortium to develop a EU RISC-V Based Computing System
https://eurohpc-ju.europa.eu/system/files/2023-11/Decision%2039.2023%20Approving%20RISC-V%20Call%20Results.pdf

NEXT STEPS IN THE RISC-V WORLD

E4 and BSC will co-organize the international workshop at HiPEAC Conference:

«RISC-V: the cornerstone ISA for the next generation of HPC infrastructures»

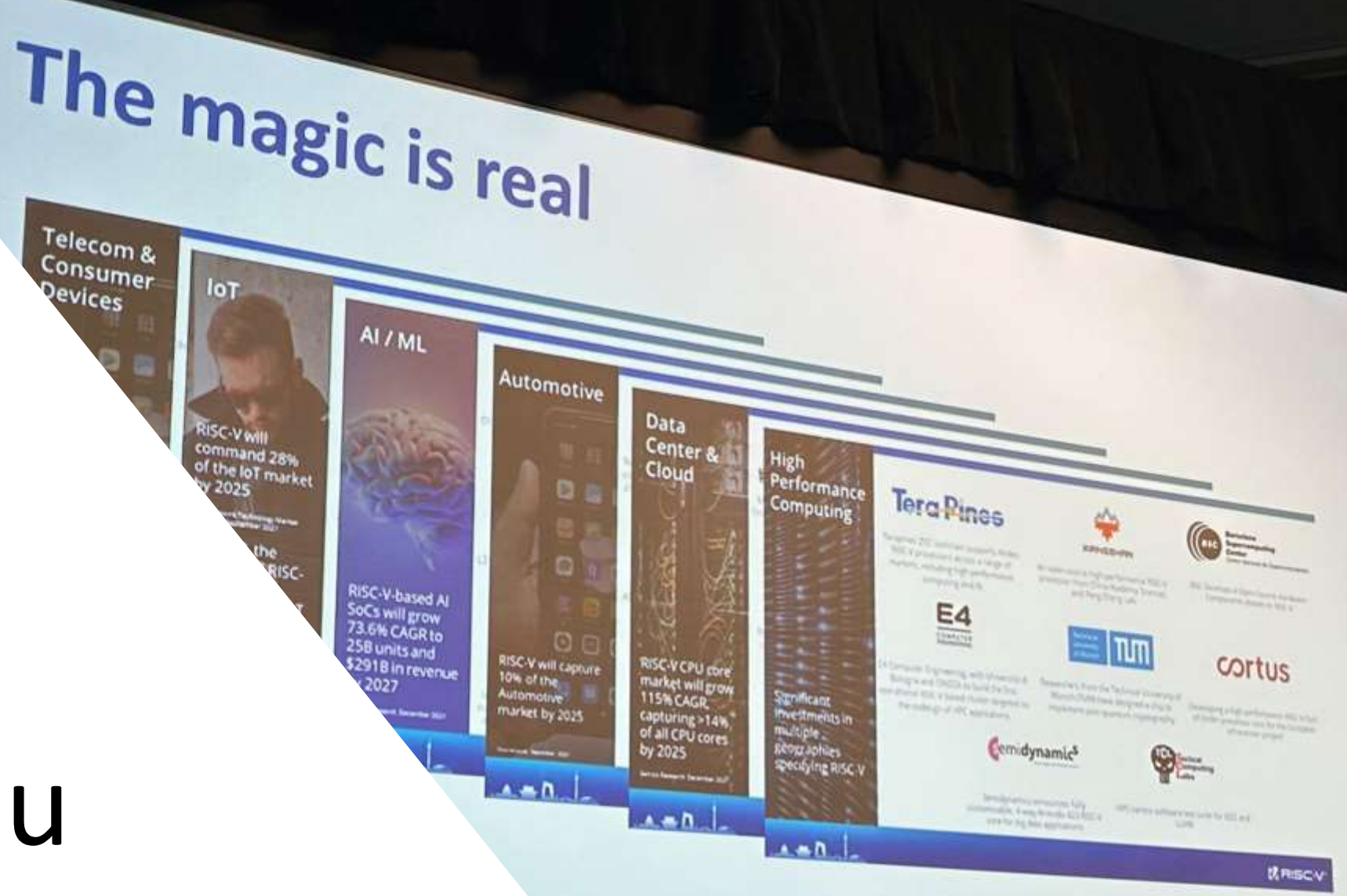
Munich, Germany, Wednesday, 01/17/2024
10:00 am – 5:30 pm

https://www.e4company.com/en/eventi/workshop-riscv-hpc-hipeac-2024/

In 2024 E4 will improve Monte Cimone with a new E4-developed board, featuring more cores at higher frequency, while maintaining the overall system efficiency --> Stay Tuned

E4 COMPUTER ENGINEERING

Thank you



Picture from RISC-V Summit 2023 Santa Clara CA

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