FOUNDATION
OPENHW™
PROVEN PROCESSOR IP

OpenHW Foundation RISC-V Cores: Empowering the Hardware Revolution

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Agenda

- Industrial Grade, Open Source RISC-V Cores, is that working?
- Motivations to join OpenHW and make the Hardware revolution happening
- OpenHW Cores lineup

  Cores, Compilers, Organization

Industrial Grade, Open Source RISC-V Cores, is that working?

Case Studies

Open Hardware is Shaping the Future of AI, Cloud, and Beyond

The RISC-V CPU market is projected to grow at a **34.9% compound annual growth rate** through 2027.

RISC-V International, 2022

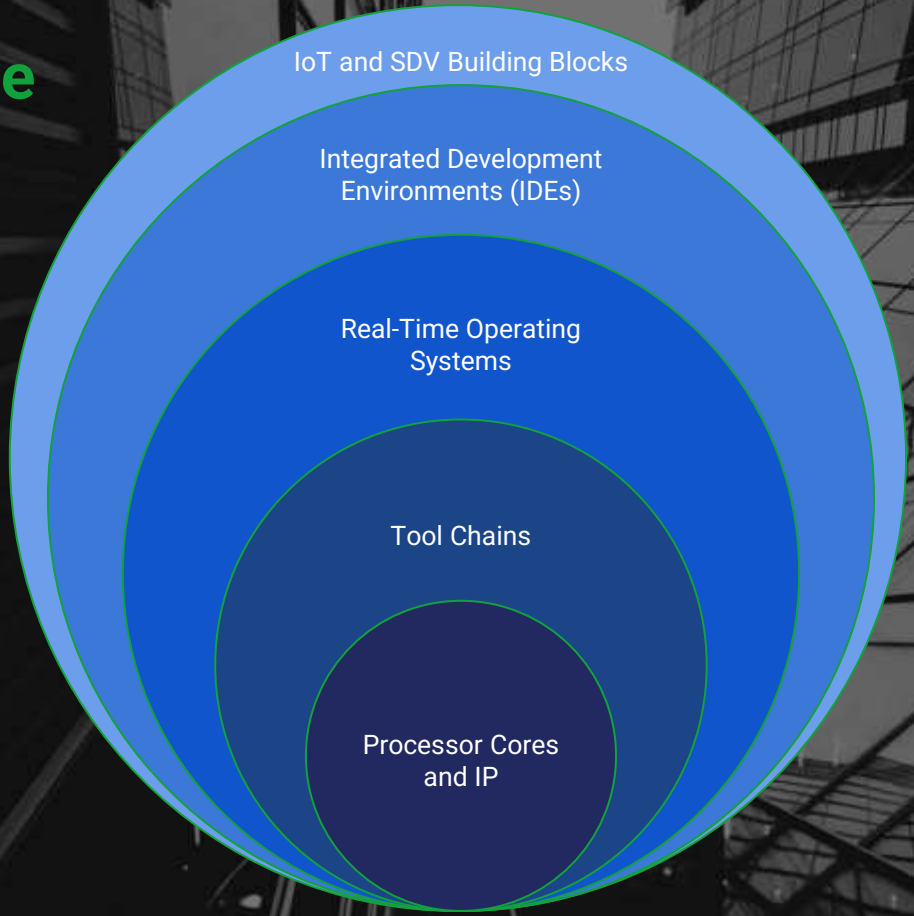
Proprietary hardware architectures often hinder innovation due to high costs and licensing restrictions, slowing down technological progress. **RISC-V addresses these challenges by offering an open source solution that enables faster development, improved interoperability, and lower costs**, especially in industries that require rapid advancements.

Over **16 billion RISC-V cores** are forecasted to be deployed by 2030, driven by sectors like AI, auto, and telecom.

RISC-V International, 2023

As the adoption of RISC-V accelerates in industries such as AI, automotive, and telecommunications, the **demand for robust, industry-grade cores is increasing.** These RISC-V cores ensure the **reliability, scalability, and security essential for mission-critical applications** in these sectors.

Towards a Comprehensive Open Source Embedded RISC-V stack



eclipse

eclipse iot

THEIA

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FOUNDATION OPENHW PROVEN PROCESSOR IP

AI for Inference

Meta’s in-house AI Accelerator

- Training is infrequent, but inference is forever
- Enterprise Datacenters
- Significant power consumption (10’s of watts)
- Large engineering teams

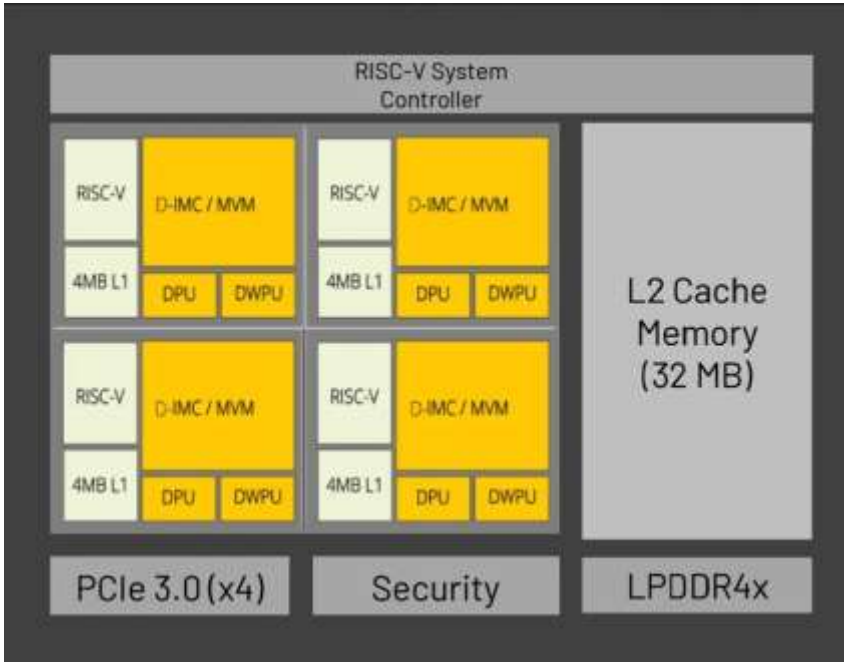
- Yet, a simple design
  - Make a Processing Element (PE)
  - Copy it a few times
  - Add some IO’s
  - Be the best in suggesting yet another Cat video (YACV) to watch

AI at the Edge

Axelera.AI edge AI

- Low-power (Could run on battery)
- Suitable for deeply embedded applications
- Available in M.2 form factor

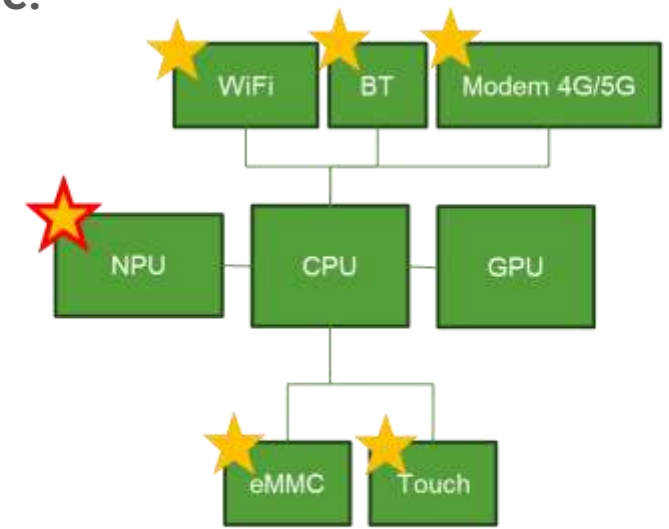
- Again, a simple design
  - Again: Common building blocks with RISC-V Controller
  - Important: Security on-chip!



AI in Your Pocket

AI powered by RISC-V is already in your phone!

- Several ARM-based SOCs feature specialised cores powered by RISC-V
  - Yes, including “fruity” ones
  - Excludes the Nokia 3390



= RISC-V already today by some manufacturers, sometimes multiple Cores

Motivations to join OpenHW and make the Hardware revolution happening

Why commercial Company’s join?

The Value of OpenHW Membership

Engage in the development and verification of high-quality open source cores, contributing to the advancement of RISC-V architecture.

Collaborate with other industry leaders to drive shared goals and projects.

Shape the direction of key technologies and initiatives participation in projects and committees.

Access cutting-edge RISC-V hardware IP, influence industry standards, and leverage OpenHW's industrial-grade cores in your projects.

Gain visibility through association with leading open source initiatives and promotion via OpenHW's global communications channels.

Ensure the sustainability and longevity of your technological investments by engaging in strategic initiatives.

Industry Members 100+ Members & Partners

What Our Members Say

“As a leader in secure, intelligent wireless technology for a more connected world, Silicon Labs products need efficient, low-cost, customizable processor cores to realize our customers’ performance requirements.

The OpenHW CORE-V CVE4 family of open-source RISC-V cores satisfy these requirements, and Silicon Labs has taken a leadership position within the OpenHW ecosystem to help drive the execution of various CORE-V CVE4 projects.

A range of Silicon Labs SoC products have adopted various CVE4 cores and have launched into high-volume production," said Daniel Cooley, Silicon Labs CTO & Board Member, OpenHW Group.

SILICON LABS

“In 2018, Thales joined the RISC-V Foundation to help design the RISC-V open instruction set and above all to rally manufacturers and academics around a subject that is crucial for our sovereignty.

In 2019, Thales was a founding member of the OpenHW Group and has taken a leadership role within open-source hardware communities to design processors for critical embedded systems, particularly in the aerospace, defence and cybersecurity sectors with a particular focus on the OpenHW CORE-V CVA6 processor.

Open-source solutions for hardware as well as software are becoming more integral than ever to Thales's innovation strategy.” said Daniel Glazman, VP Software Technologies at Thales.

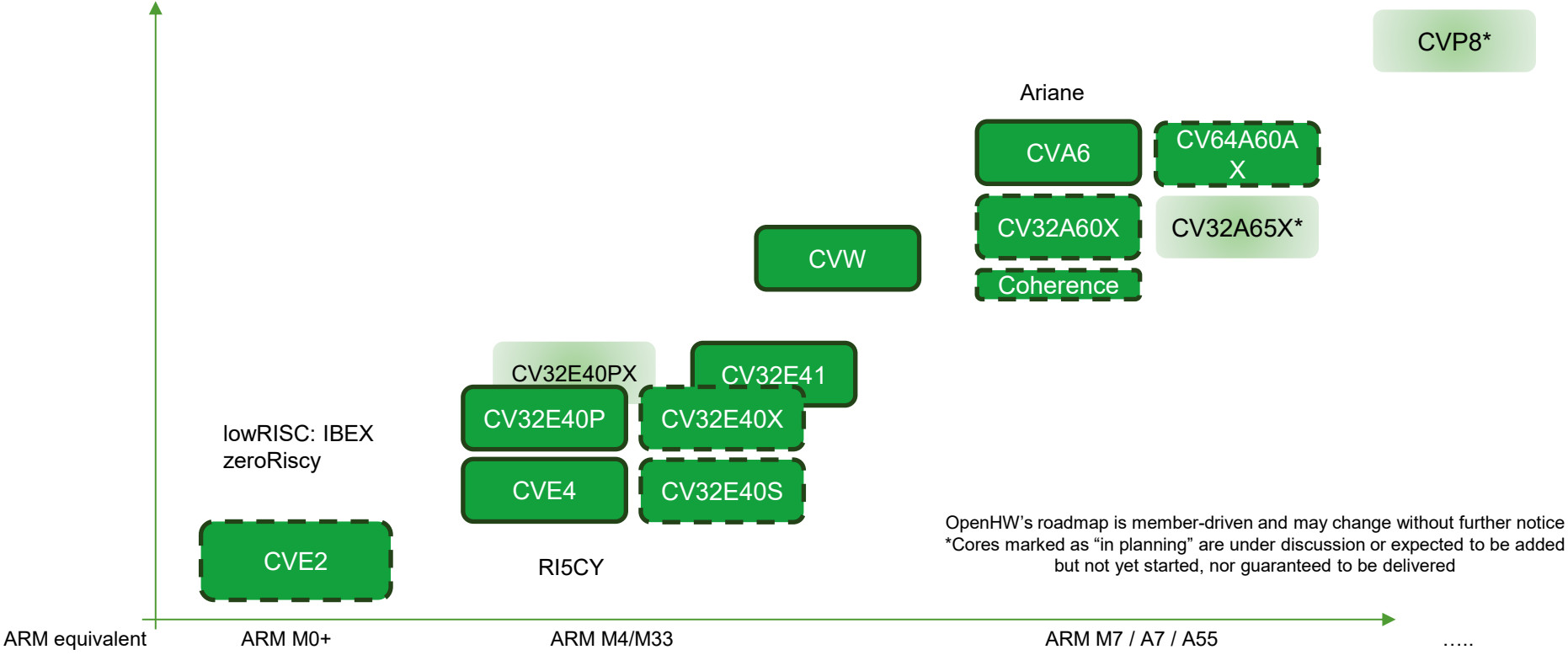
THALES

Where do I Find Industrial-Grade Open Source RISC-V Cores?

OpenHW Foundation has them?

For Free?

OpenHW RISC-V Roadmap



OpenHW Foundation Deliverables

- **License**
  - Apache 2.0/Solderpad
- **Cores**
  - System Verilog

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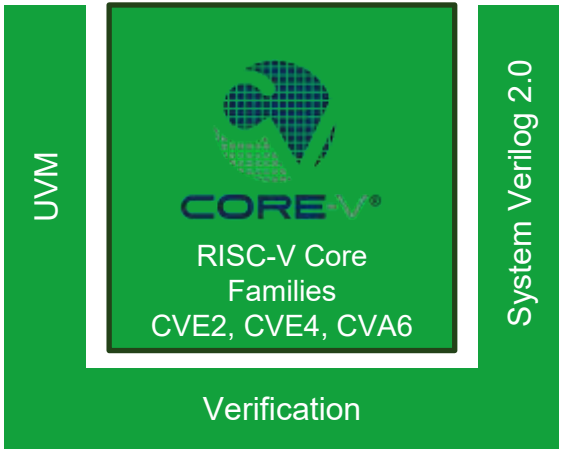
  - UVM, System Verilog, a little python and tcl
- **Tools**
  - Siemens Mentor Questa, Cadence, Synopsys, Imperas, …



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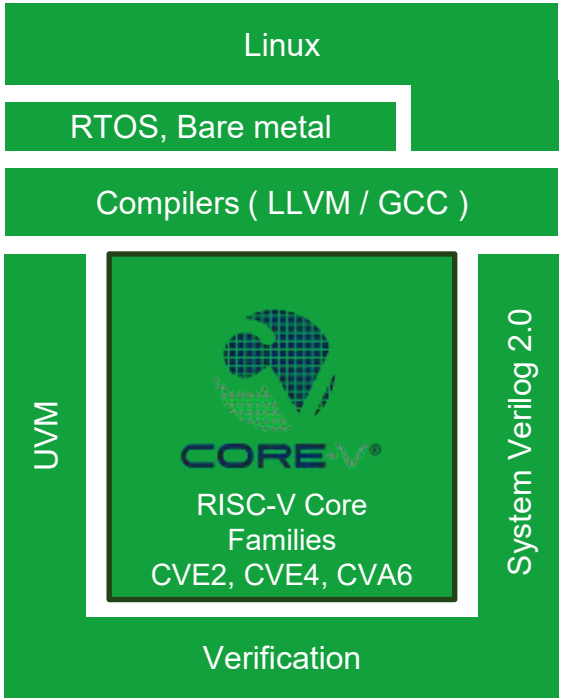
  - Compilers (LLVM, GCC)
  - RTOSes (FreeRTOS, Eclipse ThreadX)



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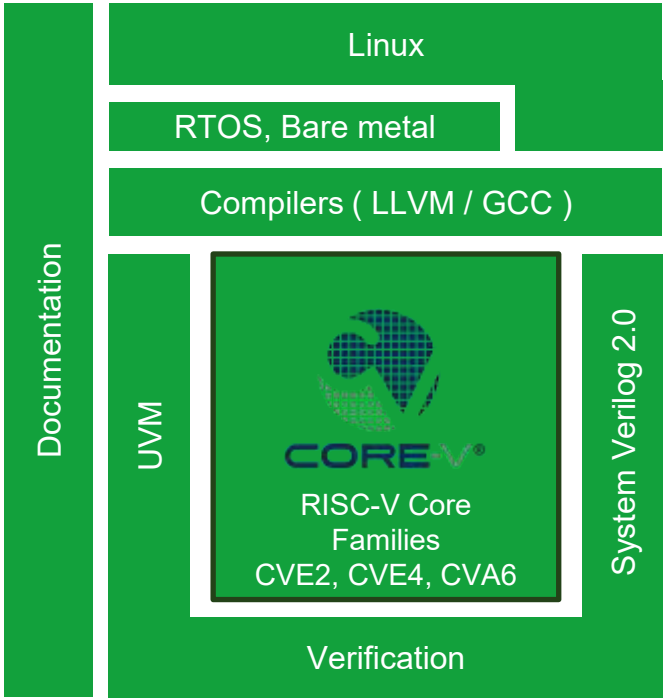

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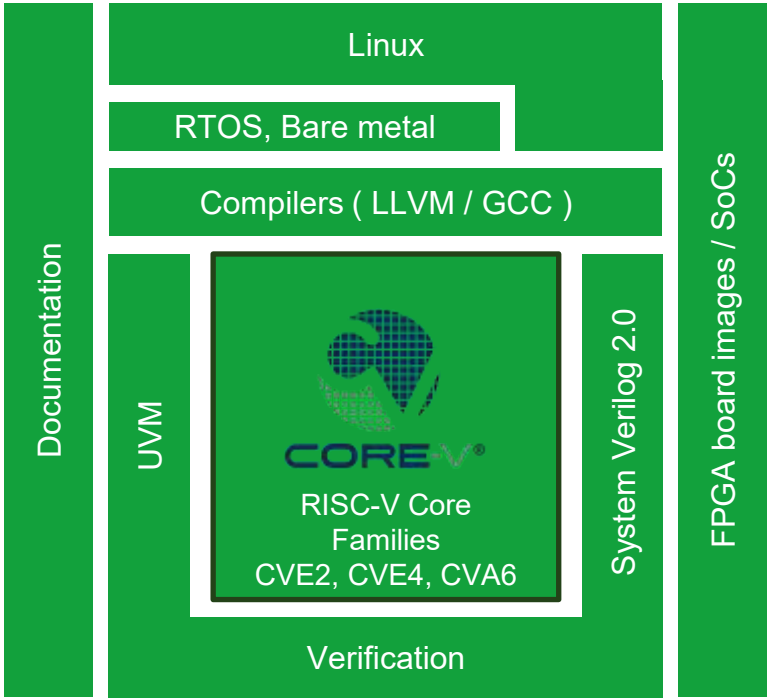
- **Documentation**
- **FPGA Board Images / SOCs**
  - Digilent Nexys A7
  - Digilent Genesys 2



How to work with us

How to contribute

Working Groups & Task Groups

- Steering Committee approves elected Chairs of Working Groups and has final approval of working group recommendations

- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - SW Task Group
  - HW Task Group
  - Safety & Security Task Group

- Marketing Working Group
  - University Outreach Task Group

Technical Working Group (TWG)

- Co-Chair: Jérôme Quévremont, Thales Research & Technology

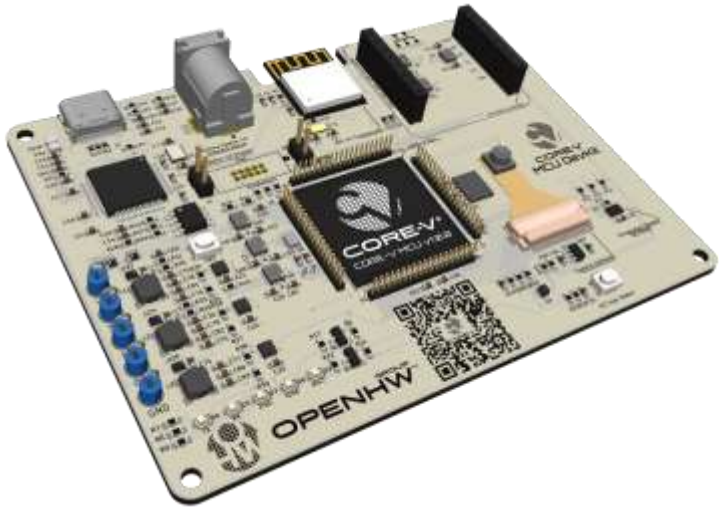
- Drive the overall technical direction, development roadmap and project execution for all technology related activities within the OpenHW Group and oversee the Task Groups
- TWG is essentially the OpenHW Foundation’s “R&D / Engineering Organization”
- OpenHW Foundation’s engineering release methodology is based on the Eclipse Development Process

Technical Working Group (TWG)

- Chair: Arjan Bink, Silicon Laboratories
- Vice-Chair: Jérôme Quévremont, Thales Research & Technology

- Define and develop
  feature and functionality roadmap and
  the open-source IP for the cores
  within the OpenHW Group.

- Currently monthly meetings



Get Your Compiler Right

Software Will Make or Break Your AI Chip

OpenHW Software Task Group

- Chair: Paolo Savini, Embecosm
- Define, develop and support toolchains, operating system ports and firmware for the cores and IP developed within the OpenHW Foundation
- Active Projects:
  - GCC / LLVM
  - IDEs
  - FreeRTOS
  - HAL
  - CORE-V MCU SDK
- Emerging: Cooperation with the Eclipse ThreadX project

Compilers

- We intend to contribute all of our compiler patches upstream for CV32E40Pv2 and other cores
  - GNU Tools/GCC 14.1 to be fully up streamed for CVE4 by Apr 2024
  - Clang/LLVM 18 to be fully up streamed for CVE4 by Jan 2024

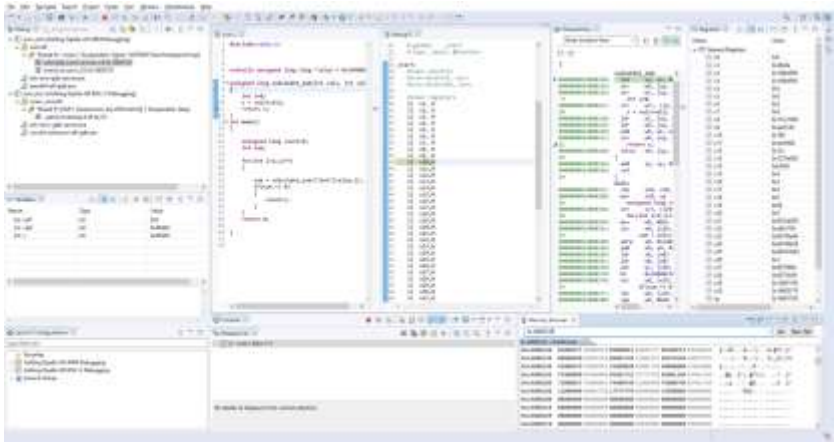
- Features:
  - Core awareness
  - Integration of CORE-V specific instructions
  - Native HWloop support

Operating Systems and Virtualisation

- **QEMU**
- **RTOS support**
  - FreeRTOS => 10.3.0
  - Zephyr 2.4, 2.5, …
- **Upcoming: Eclipse ThreadX support**
  - Only OSS RTOS certified for safety-critical applications
  - Best-performing open source RTOS
- **Linux**
  - Linux Kernel 6.2 Support
  - uBoot and OpenSPI
  - Buildroot
  - Fedora and RedHat working on Linux Support

CORE-V IDE

- CORE-V IDE is an open-source project under the SW TG at the OpenHW Group
- Based on Eclipse IDE, with native support for CORE-V development
- Includes the GCC Toolchain for CORE-V
- OpenOCD Debug Support
- “Ready-to-run” examples for Digilent FPGA boards
- Getting started guides



Why Work With Us?

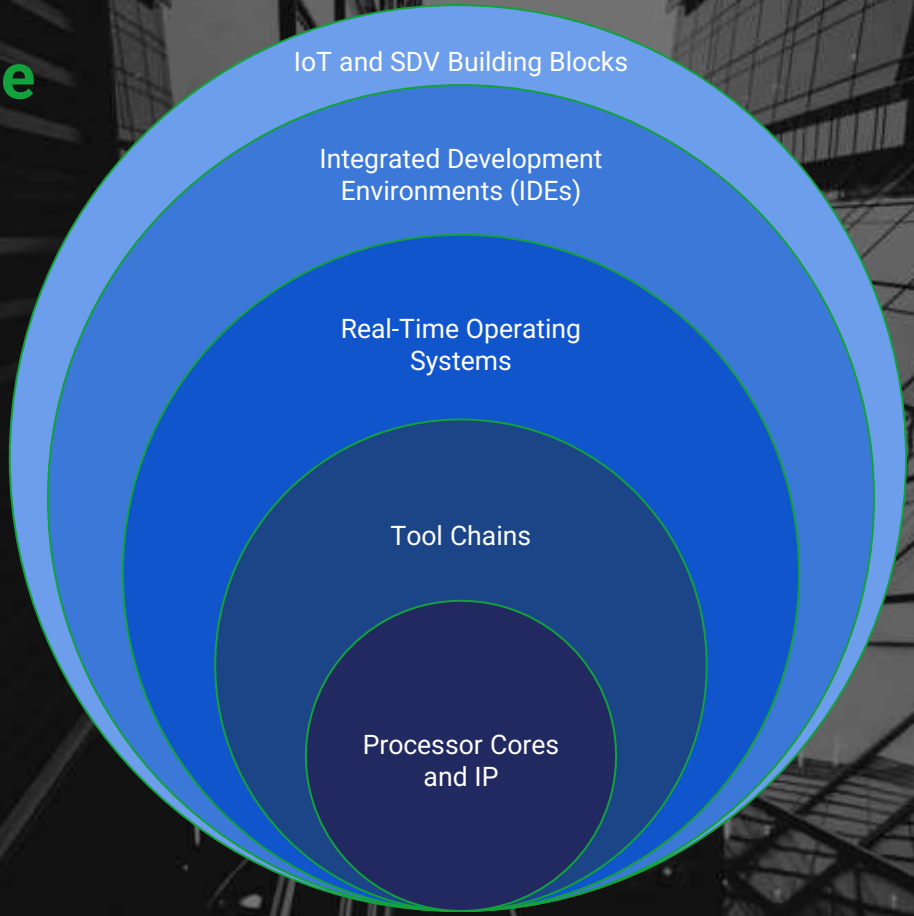
Why Build Your Own AI Chip With our IP?

- RISC-V is already everywhere in AI
- OpenHW as a platform to host, maintain and verify high quality, industrial-grade cores
  - Open
  - Transparent
  - Meritocratic
- Academia and industry working together
- Fully open cores (RTL, Verification)
  - Challenge our RTL!
- Fully customizable, high quality, fully open source permissive license

Call to Action

- Learn
  - Visit openhwfoundation.org
  - Watch OpenHW TV episodes on YouTube
- Try
  - Get the code on GitHub
- Engage: https://www.openhwgroup.org/get-involved/

Towards a Comprehensive Open Source Embedded RISC-V stack



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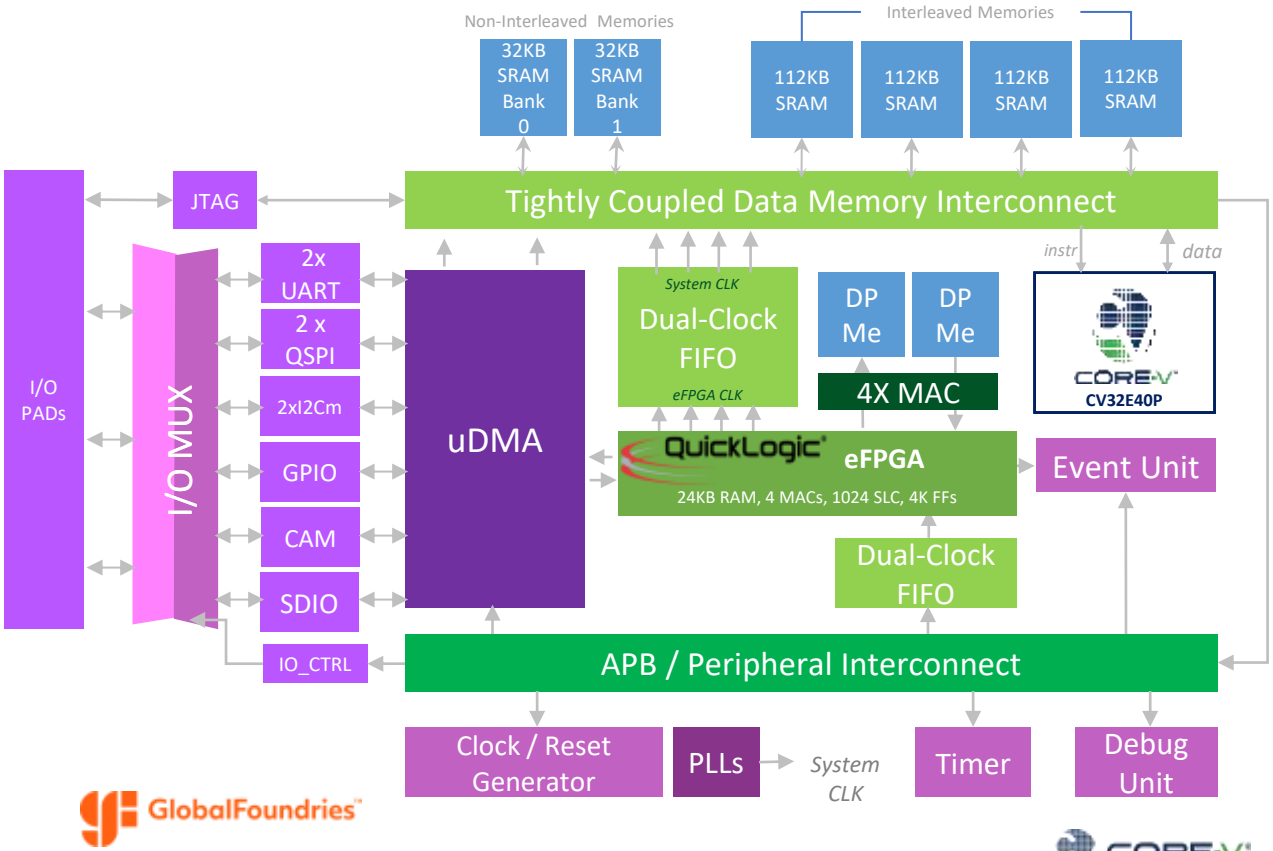
Thank you!

openhwfoundation.org

Backup

CORE-V MCU

- Real Time Operating System (e.g. FreeRTOS) capable ~400+MHz CV32E4 MCU
- Embedded FPGA fabric with hardware accelerators from QuickLogic
- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules
- Built in 22FDX with GlobalFoundries



CORE-V DevKit

- CORE-V MCU SoC
  - CV32E40P processor core
  - Quicklogic ArticPro eFPGA
  - Global Foundries 22FDX
- Ashling Opella-LD onboard JTAG debug module
- USB-C for terminal and onboard debug access
- JTAG connector for external debug access
- Espressif AWS IoT ExpressLink Module for AWS IoT cloud interconnect
- mikroBUS onboard socket, allowing access to a vast range of mikroBUS modules
- 40 pin expansion header
- I2C temperature sensor