Monte Cimone v2: HPC RISC-V Cluster Evaluation and Optimization

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Outline

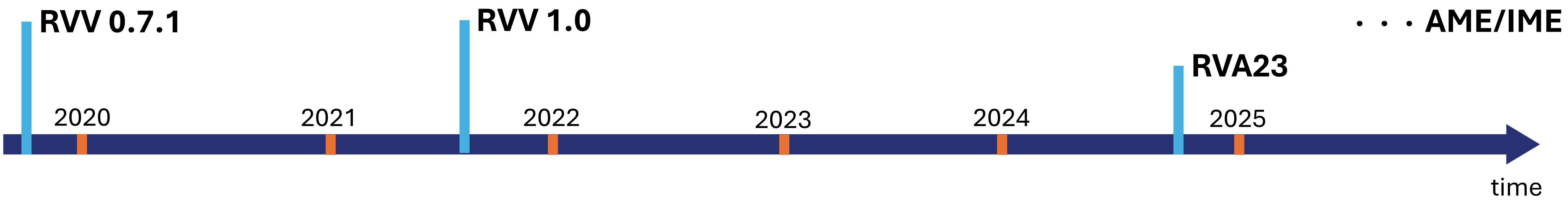
- RISC-V & HPC
- Monte Cimone evolution
- Performance evaluation
- BLAS vectorization
- Results

RISC-V & HPC

- HPC compute node requirements:
  - High core count + vector/matrix extensions
  - Large amount of system memory
  - PCIe support (accelerators, network cards, fast storage)
  - Software: OS, job schedulers, monitoring systems, packages and libraries

- RISC-V is mature in embedded domain
- How to foster RISC-V ISA uptake in HPC?

RISC-V HPC & Monte Cimone timeline



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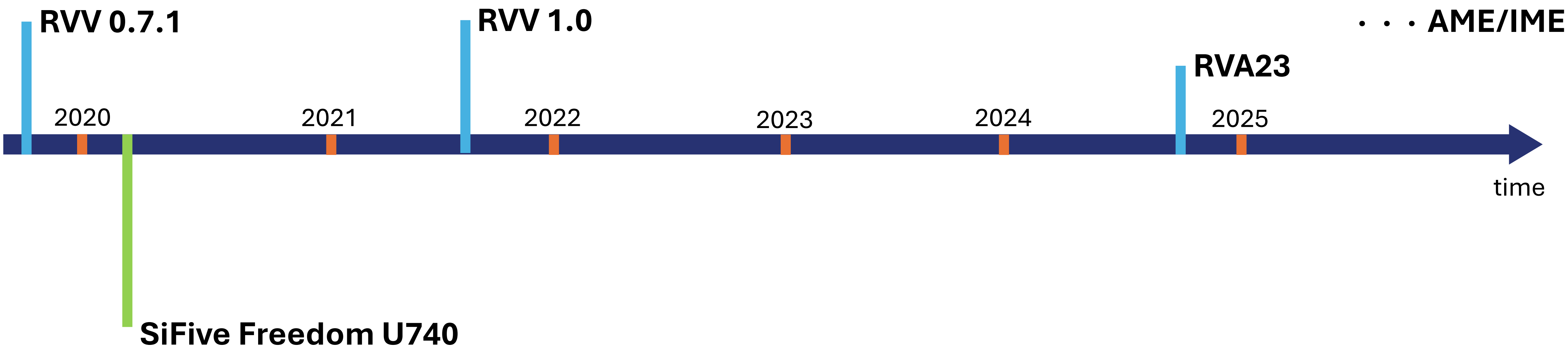
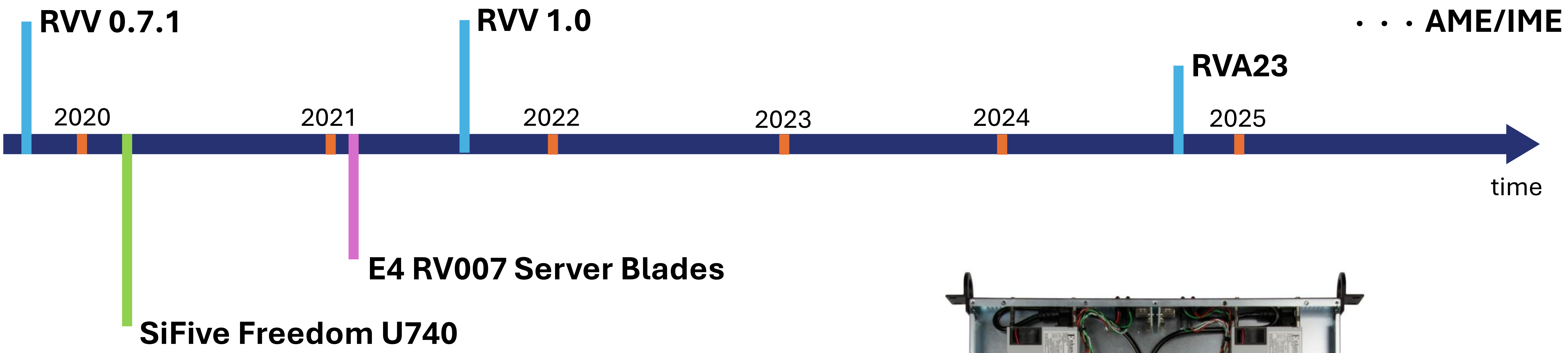


SiFive Freedom U740

- First RISC-V PC
- 4 core system RV64GC
- 16 GB DDR4
- PCIe Gen 3
- Linux ready

RISC-V HPC & Monte Cimone timeline



E4 RV007 Server Blades

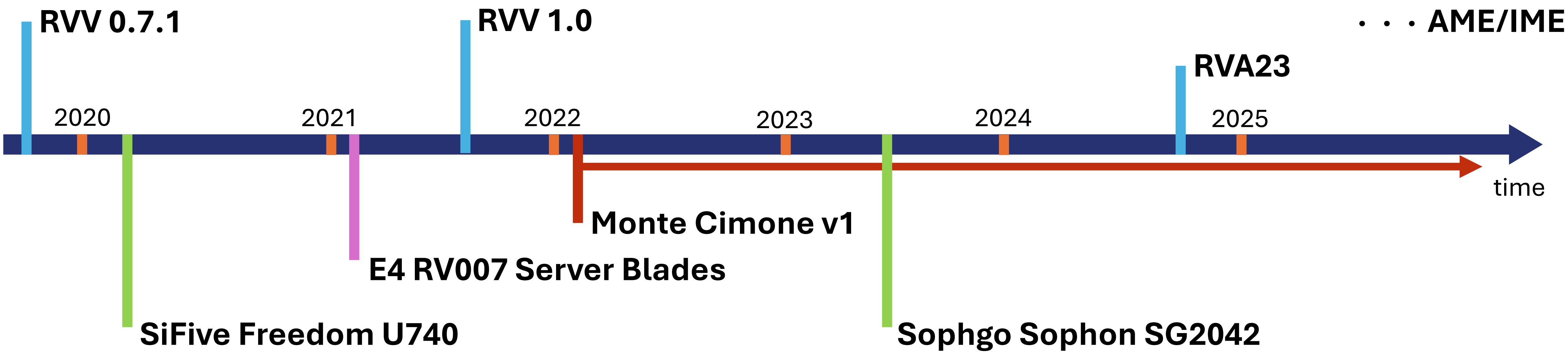
- Two SiFive Freedom U740
- Server form factor

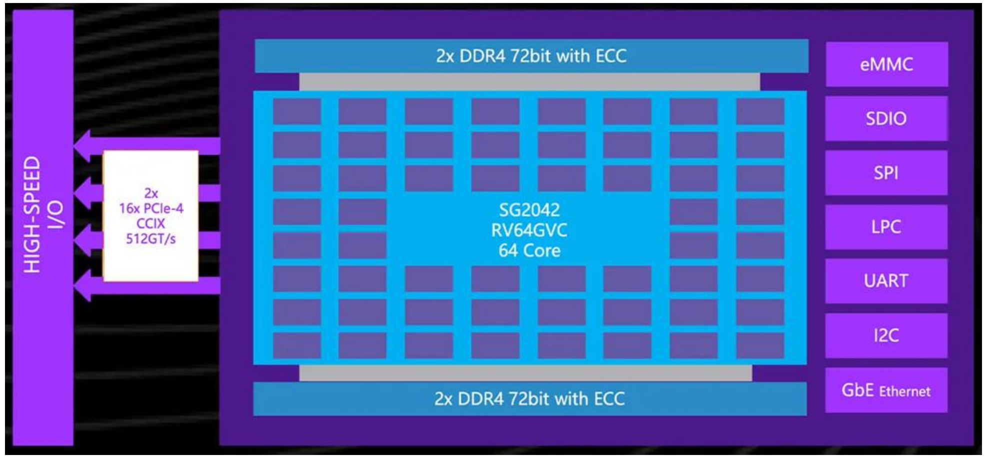
RISC-V HPC & Monte Cimone timeline

Monte Cimone v1

- First RISC-V cluster
- Four E4 RV007 blades
- 32 cores in total + 128 GB distributed system memory
- Scope: infrastructure + software validation

RISC-V HPC & Monte Cimone timeline

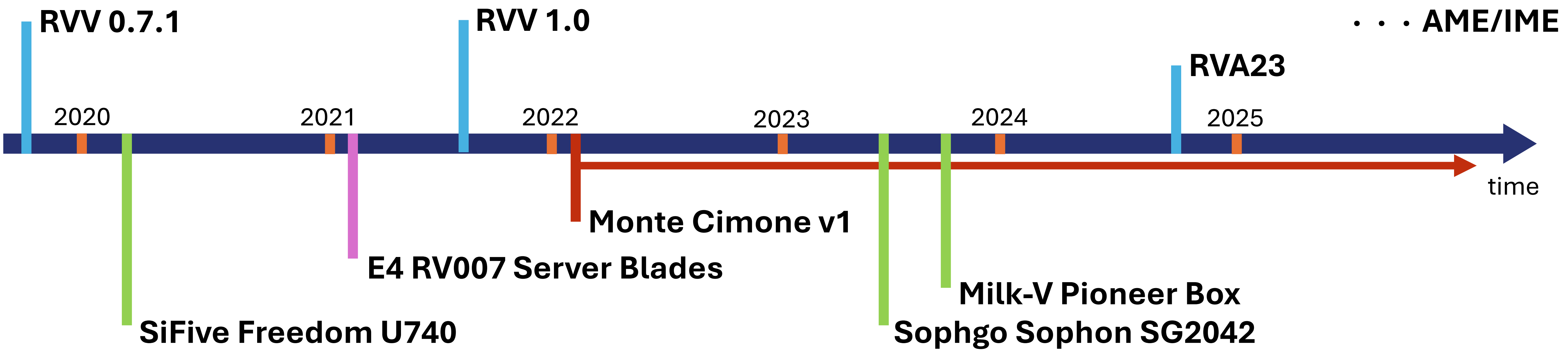




Sophgo Sophon SG2042

- First server class platform
- 64 cores RV64GC_0p7V
- 3-levels cache system
- ECC DDR4 memory
- 32 PCIe Gen 4 lanes

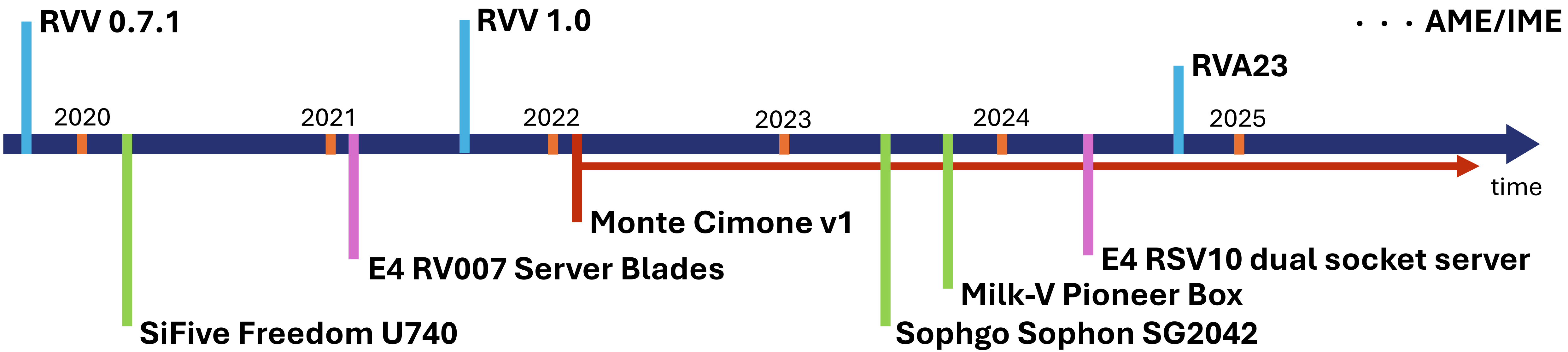
RISC-V HPC & Monte Cimone timeline



Milk-V Pioneer Box

- Single socket SG2042
- 128 GB RAM

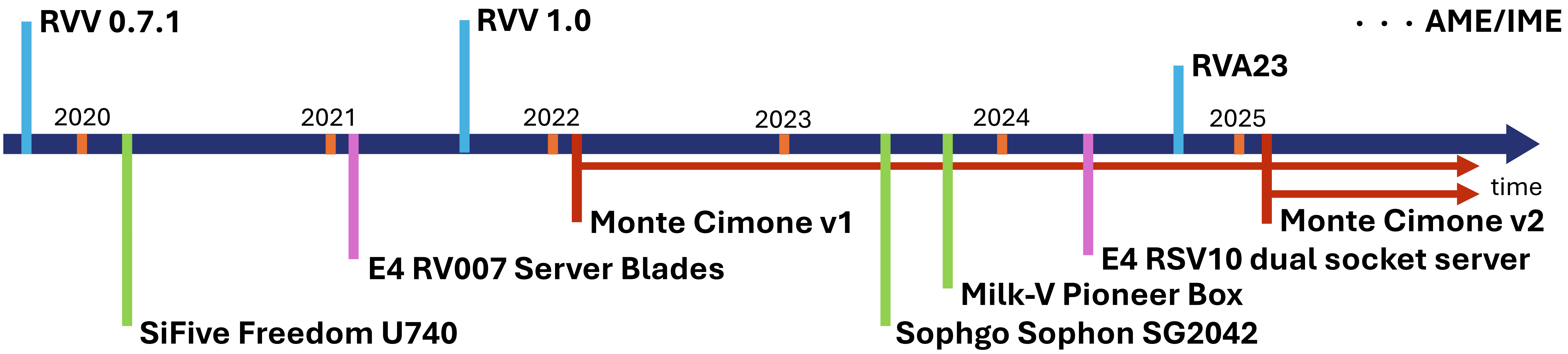
RISC-V HPC & Monte Cimone timeline



E4 RSV10 dual socket server

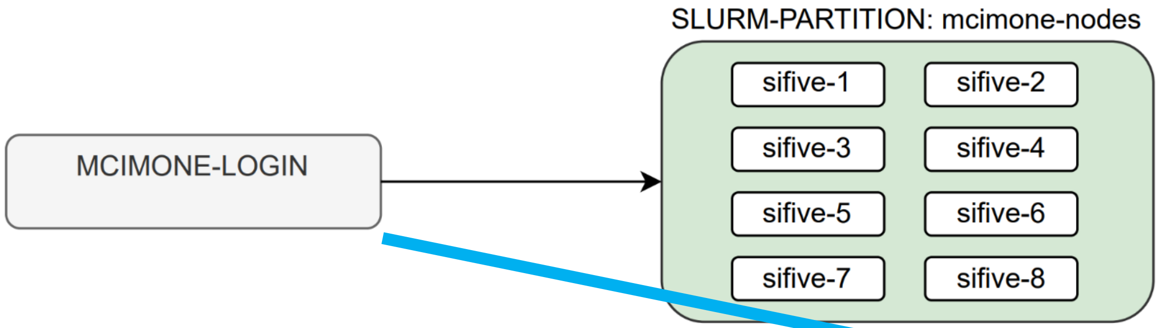
- Dual socket SG2042
- 256 GB RAM

RISC-V HPC & Monte Cimone timeline



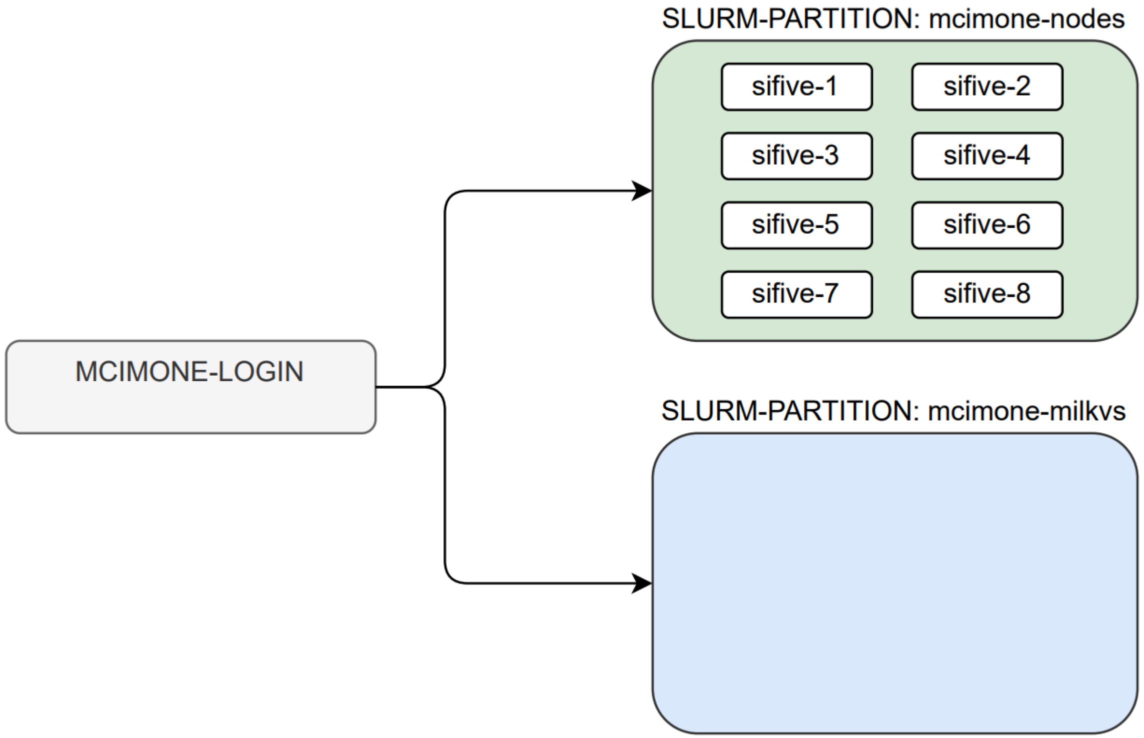
Monte Cimone v2 bring up

Starting from Monte Cimone v1



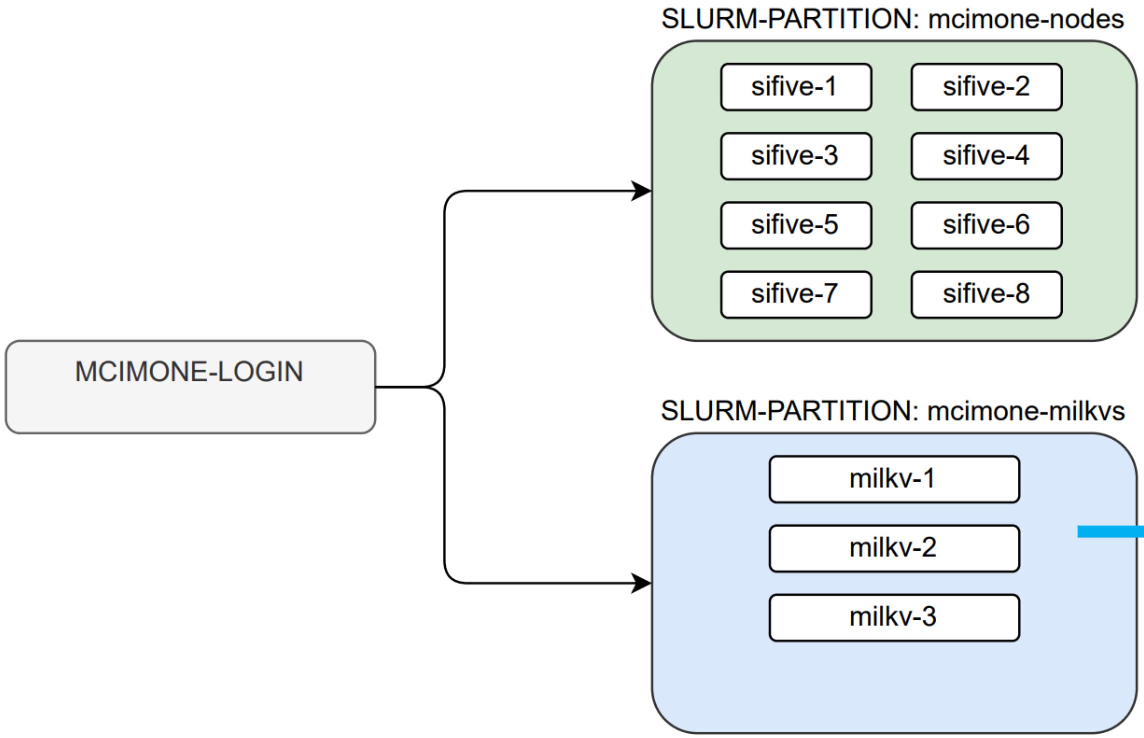
Monte Cimone v2 bring up

- New SLURM partition



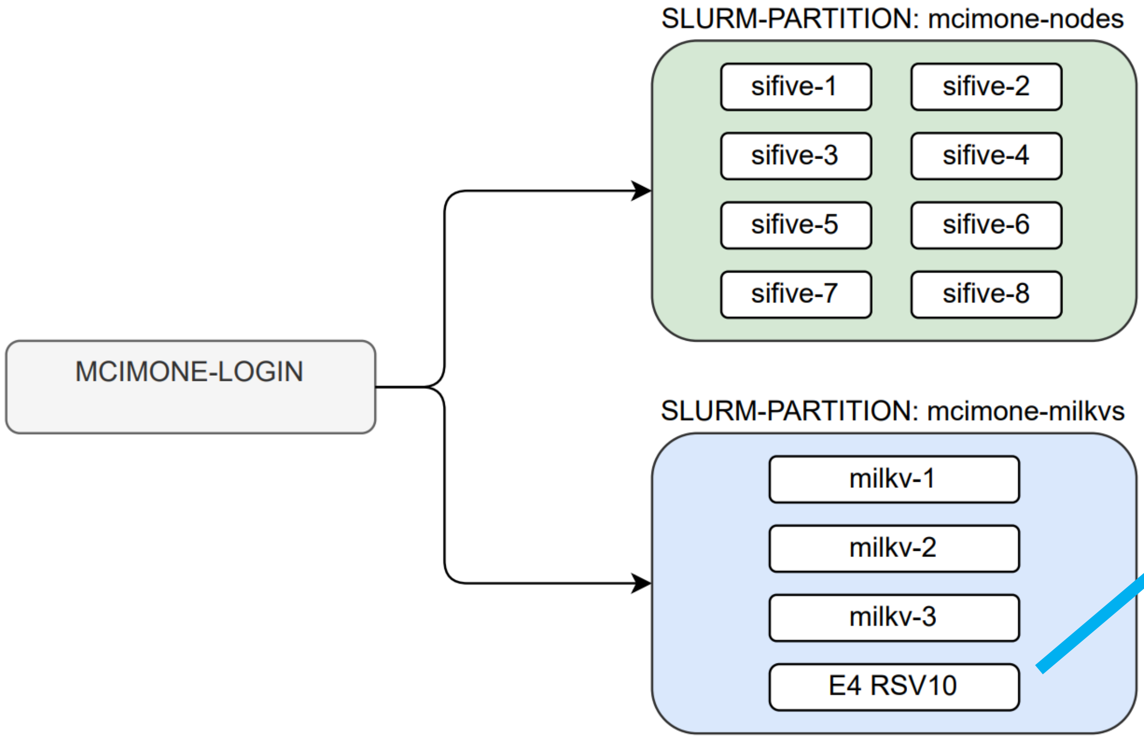
Monte Cimone v2 bring up

- New SLURM partition
  - 3 Milk-V Pioneer Box



Monte Cimone v2 bring up

- New SLURM partition
  - 3 Milk-V Pioneer Box
  - 1 E4 RSV10 Dual Socket RISC-V Server



Cluster environment

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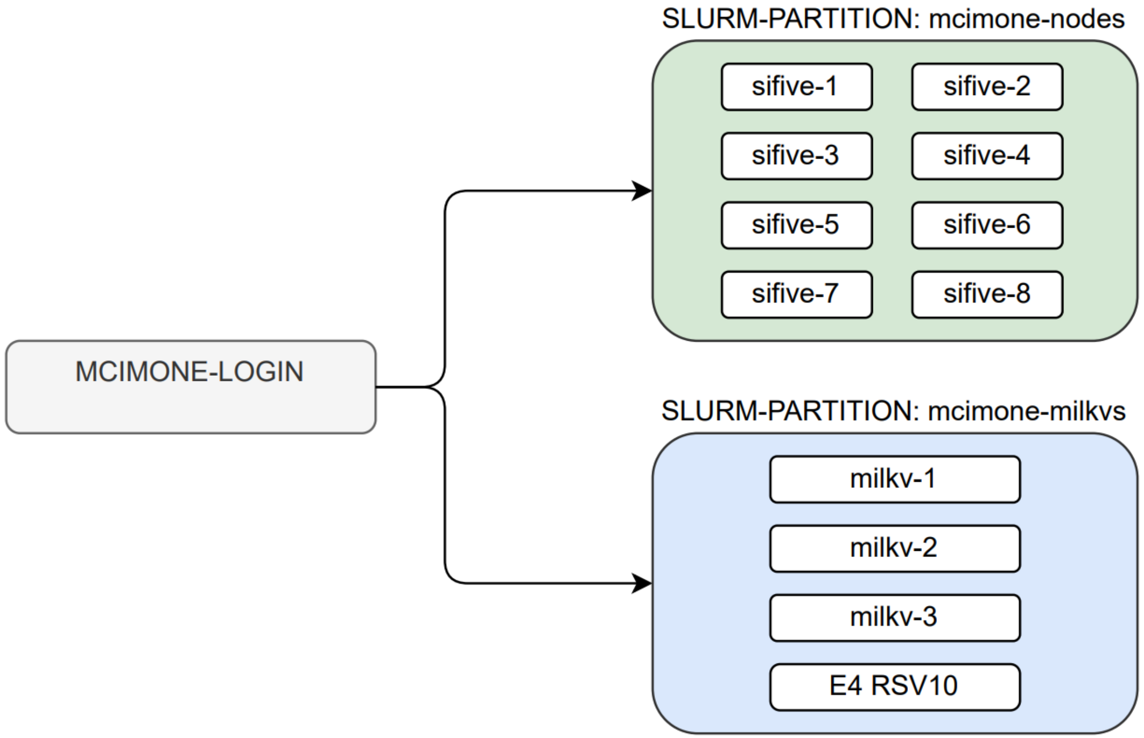
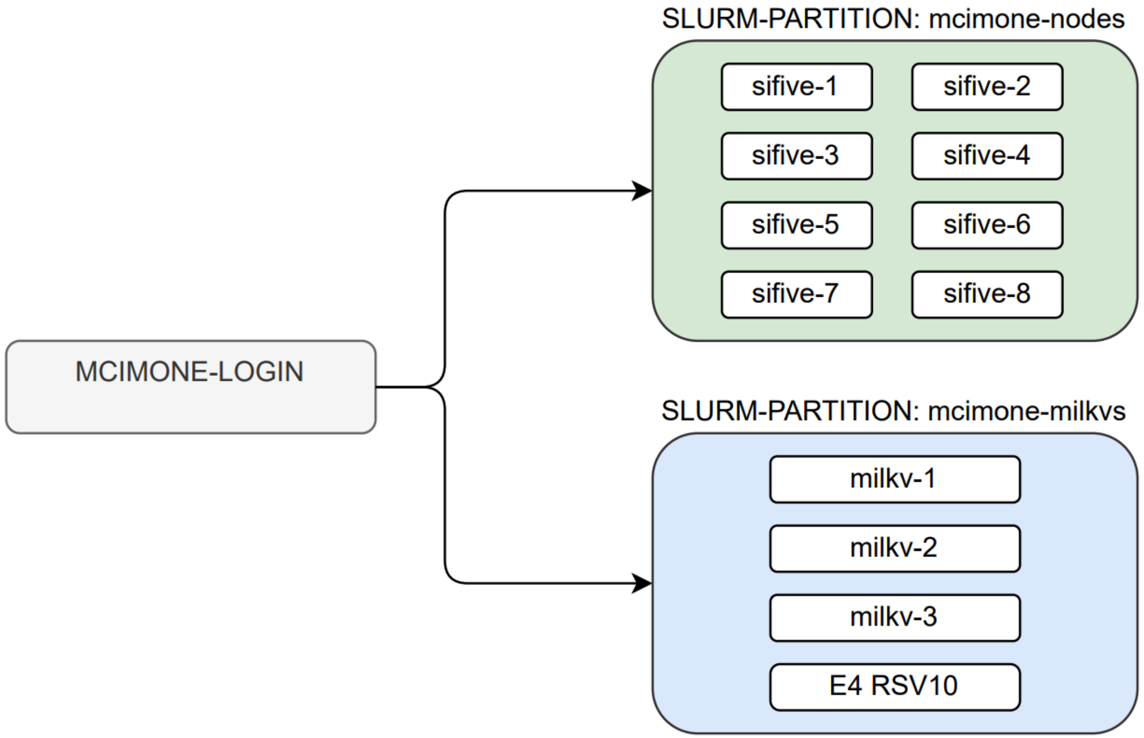


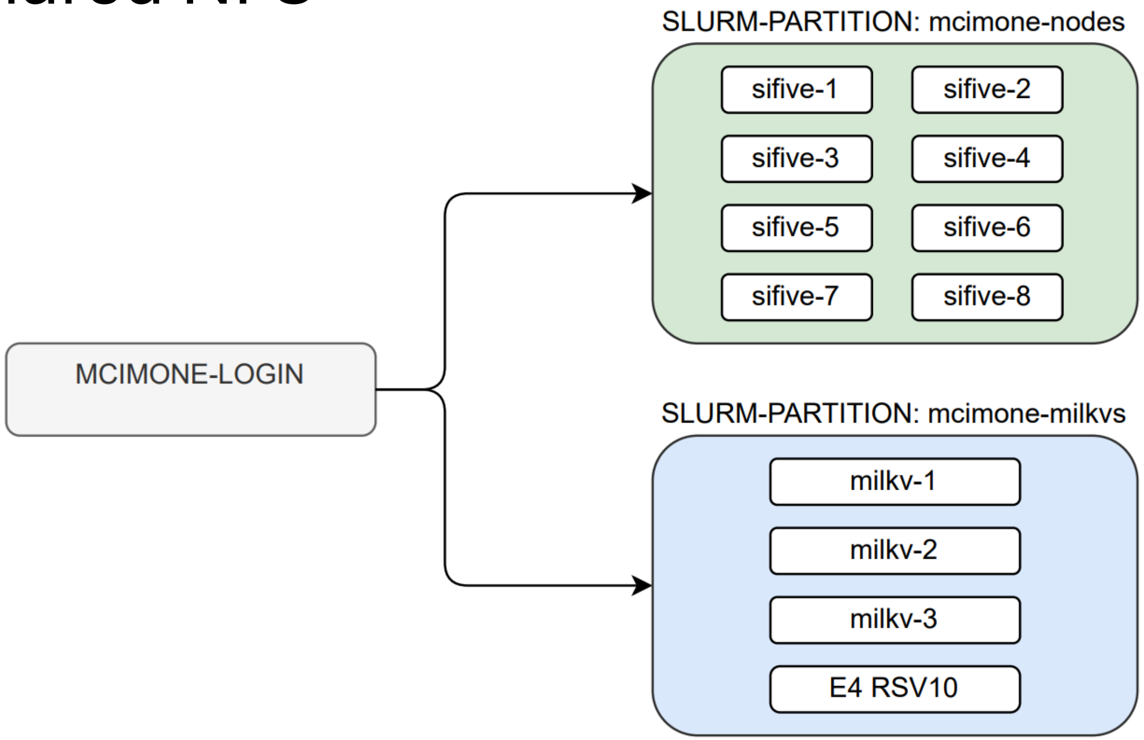
Cluster environment

- SLURM
- Examon



Cluster environment

- SLURM
- Examon
- Shared NFS



Cluster environment

- SLURM
- Examon
- Shared NFS
- Spack + tools

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berkeley-db/18.1.40/gcc-13.1.1-lxhzsx5                    m4/1.4.19/gcc-13.1.1-i4vpilc
berkeley-db/18.1.40/gcc-13.2.1-hp5nxny                    m4/1.4.19/gcc-13.2.1-yxpwh6s
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libtool/2.4.6/gcc-13.2.1-3t47ydt
```

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- SLURM
- Examon
- Shared NFS
- Spack + tools
  - Added compilers:
    - Xuantie GNU Toolchain (vendor GCC w. RVV 0.7.1 support)
    - GCC 14 (first version w. xtheadvector)

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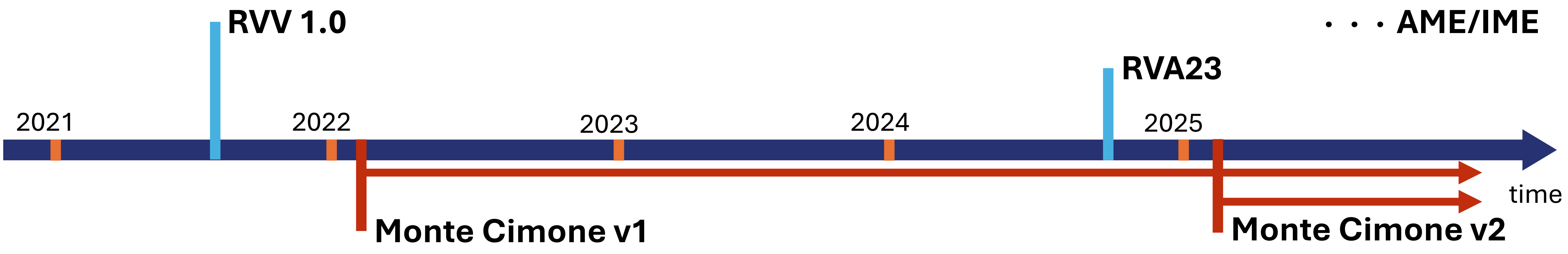
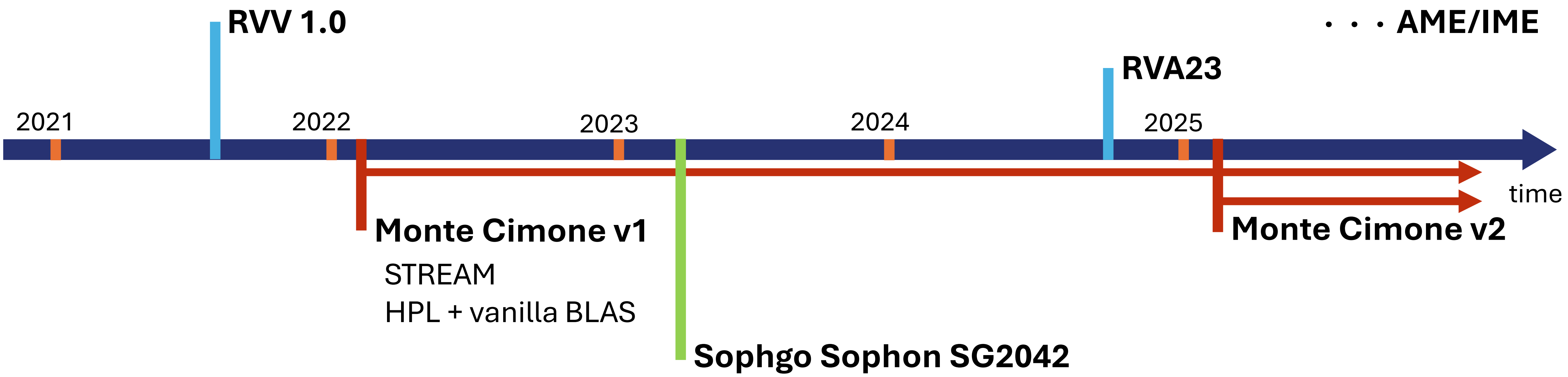
    - GCC 14 (first version w. xtheadvector)
  - Added BLAS libraries:
    - OpenBLAS (vanilla no RVV, vendor optimized)
    - BLIS with proposed optimized kernels

Monte Cimone v2 benchmark



STREAM
HPL + vanilla BLAS

Monte Cimone v2 benchmark



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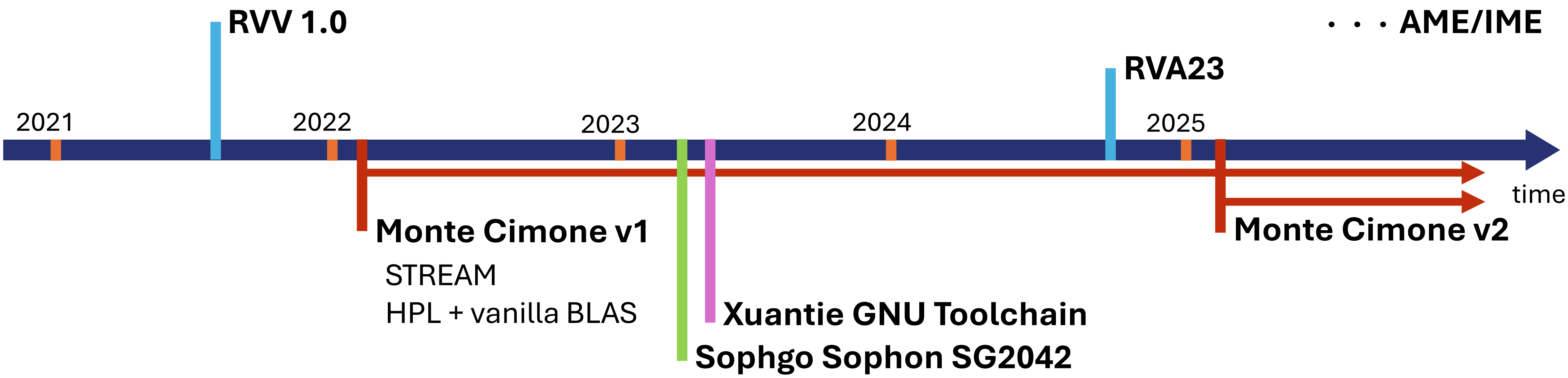

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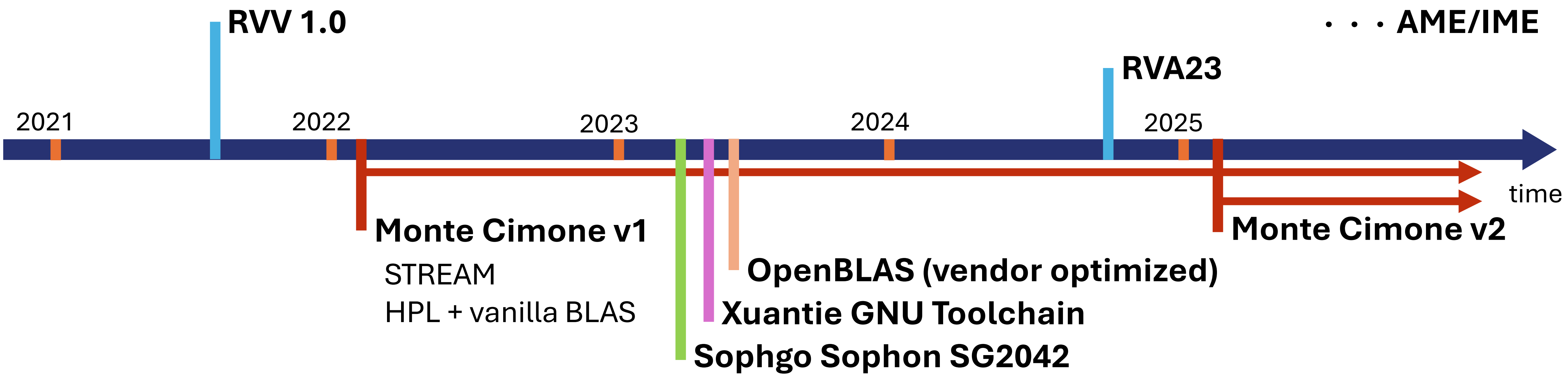

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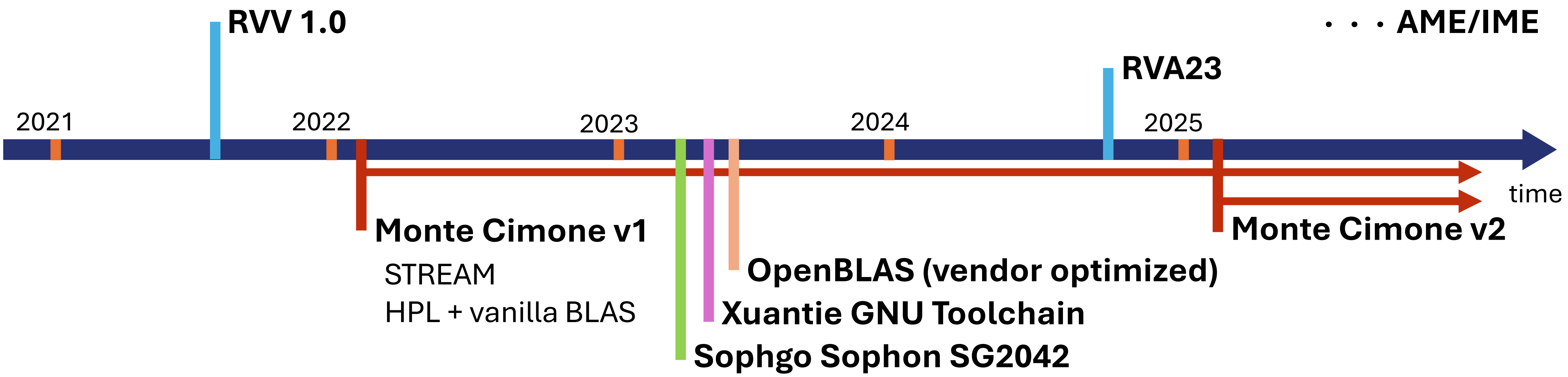

- **Performance assessment of new hardware:**
  - STREAM
  - HPL + OpenBLAS w/ Xuantie GNU Toolchain

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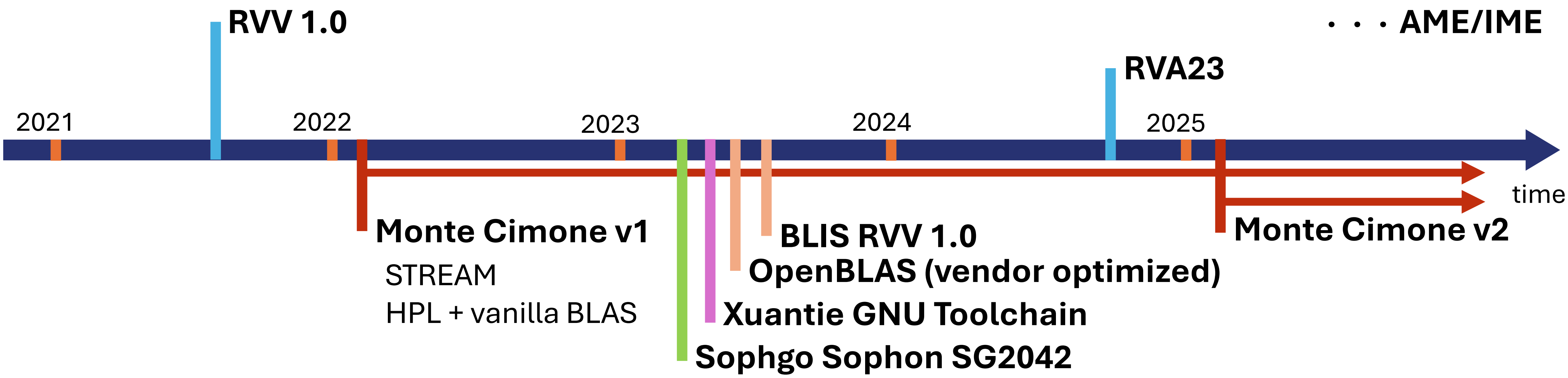

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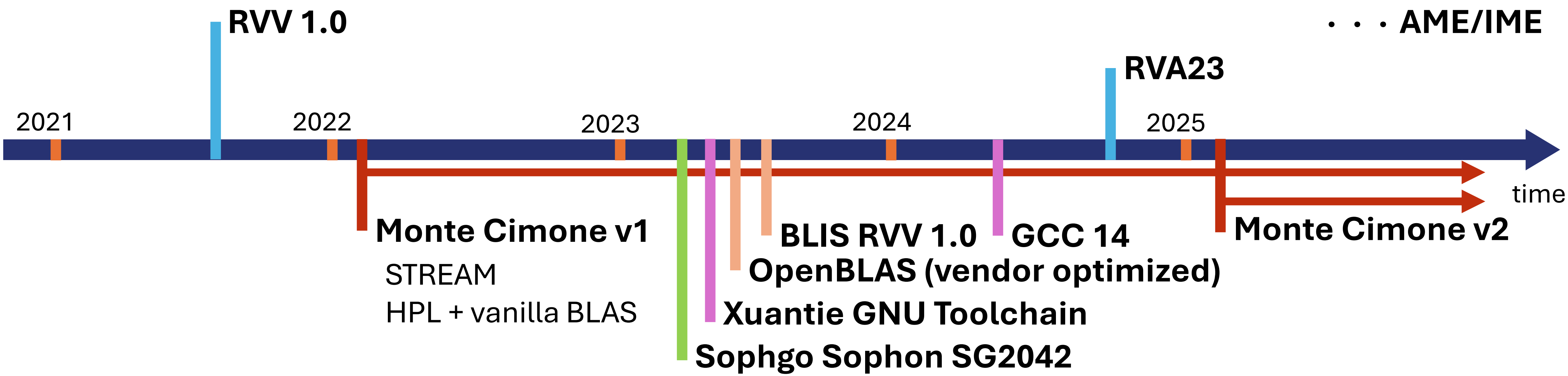

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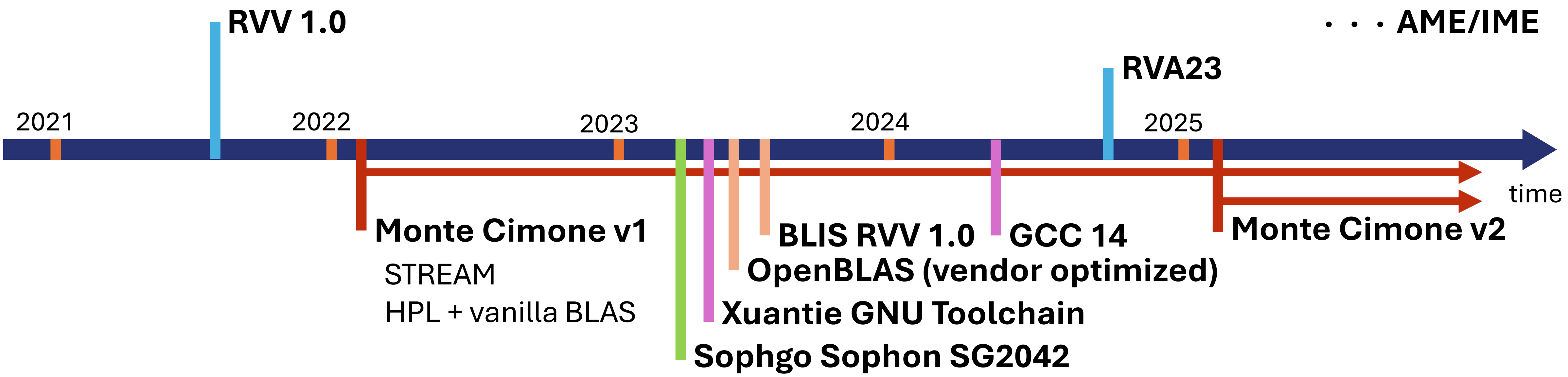

- **Performance assessment of new hardware:**
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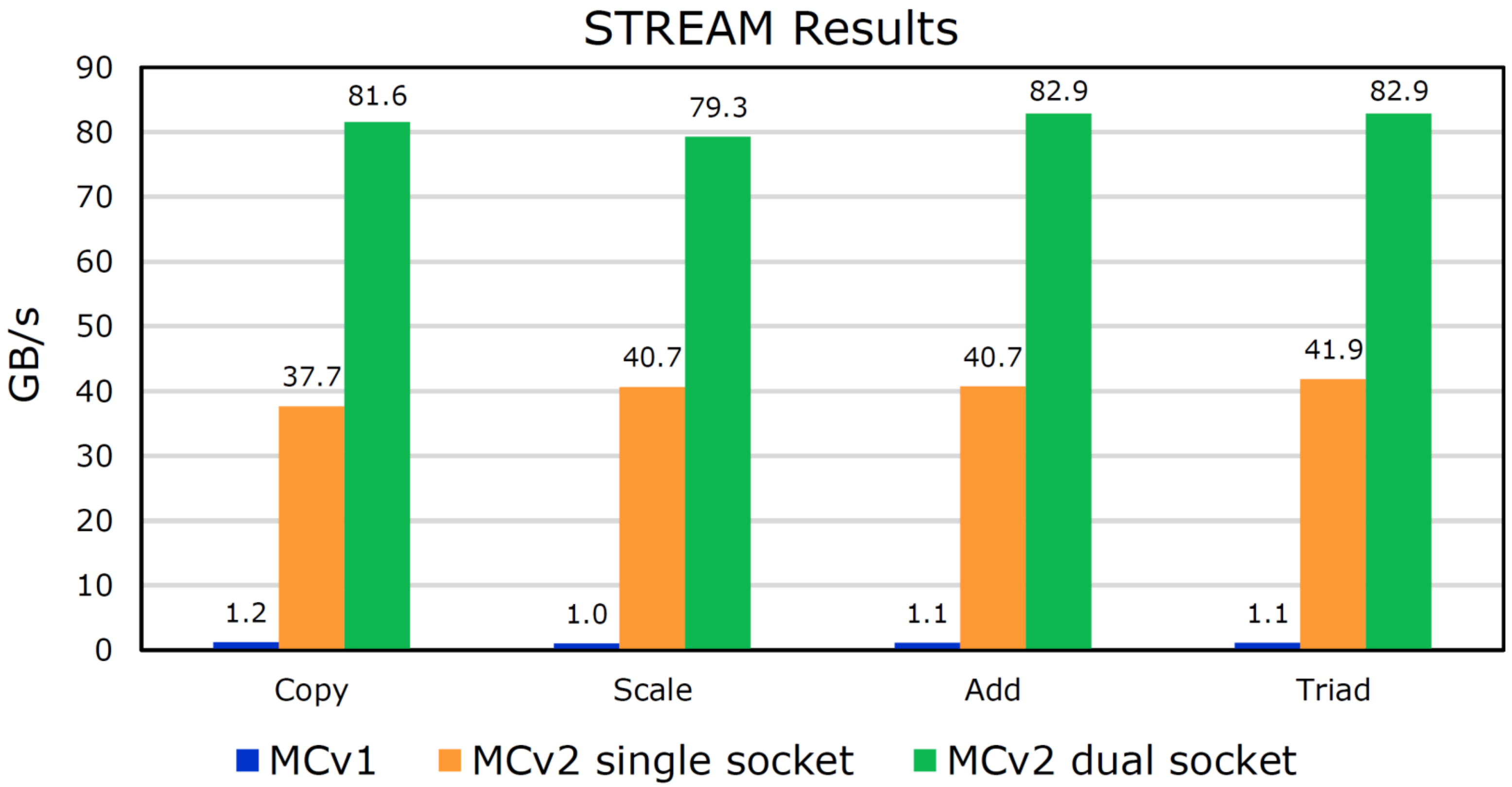
  - HPL + OpenBLAS w/ Xuantie GNU Toolchain
- **BLIS library porting and optimization**

STREAM Results

- **Monte Cimone v1 node:**
  - Max: 1.2 GB/s

- **Milk-V Pioneer Box:**
  - 64 threads
  - 4 memory channels
  - Max: 41.9 GB/s



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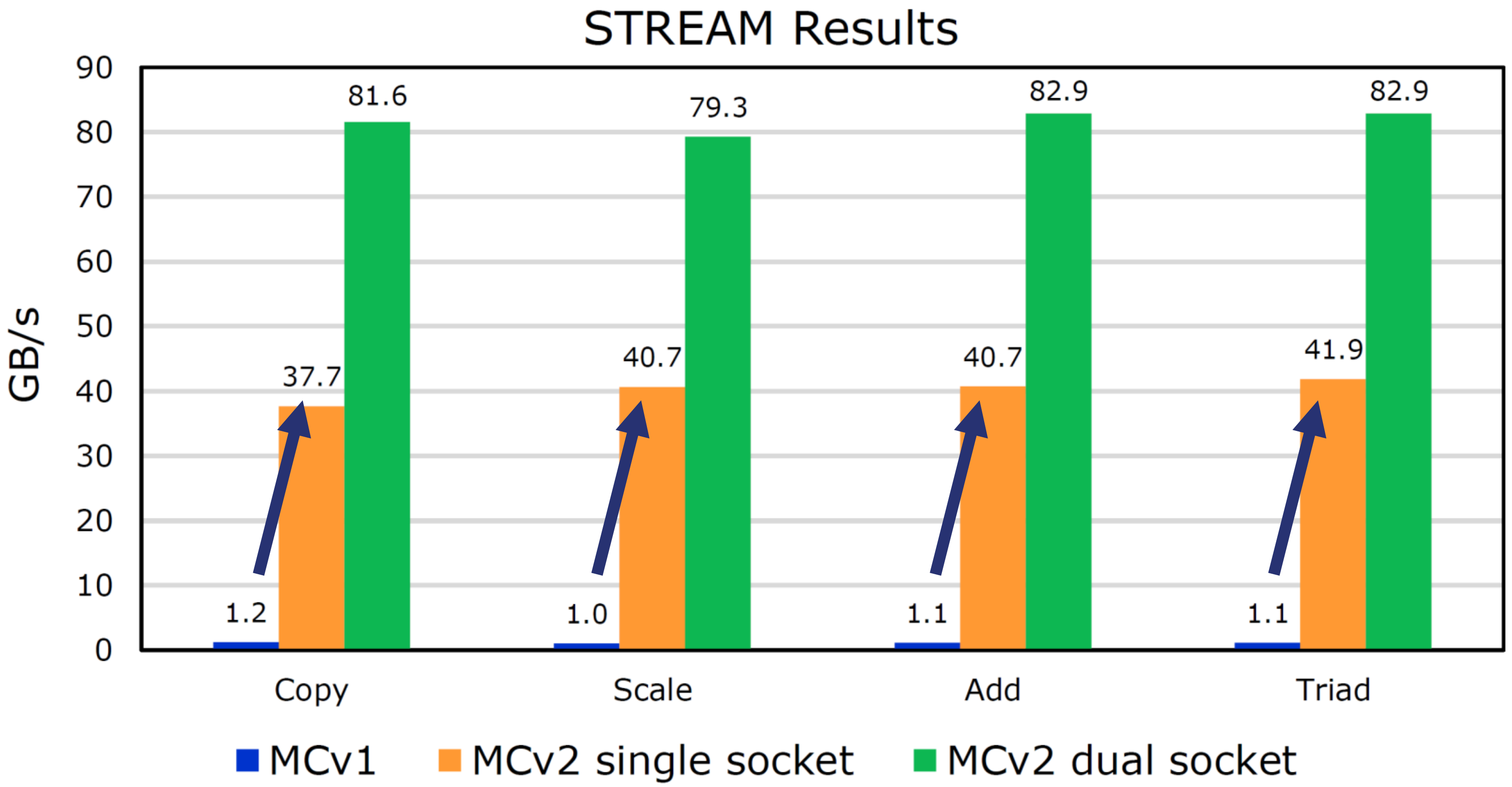

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- **Milk-V Pioneer Box:**
  - 64 threads
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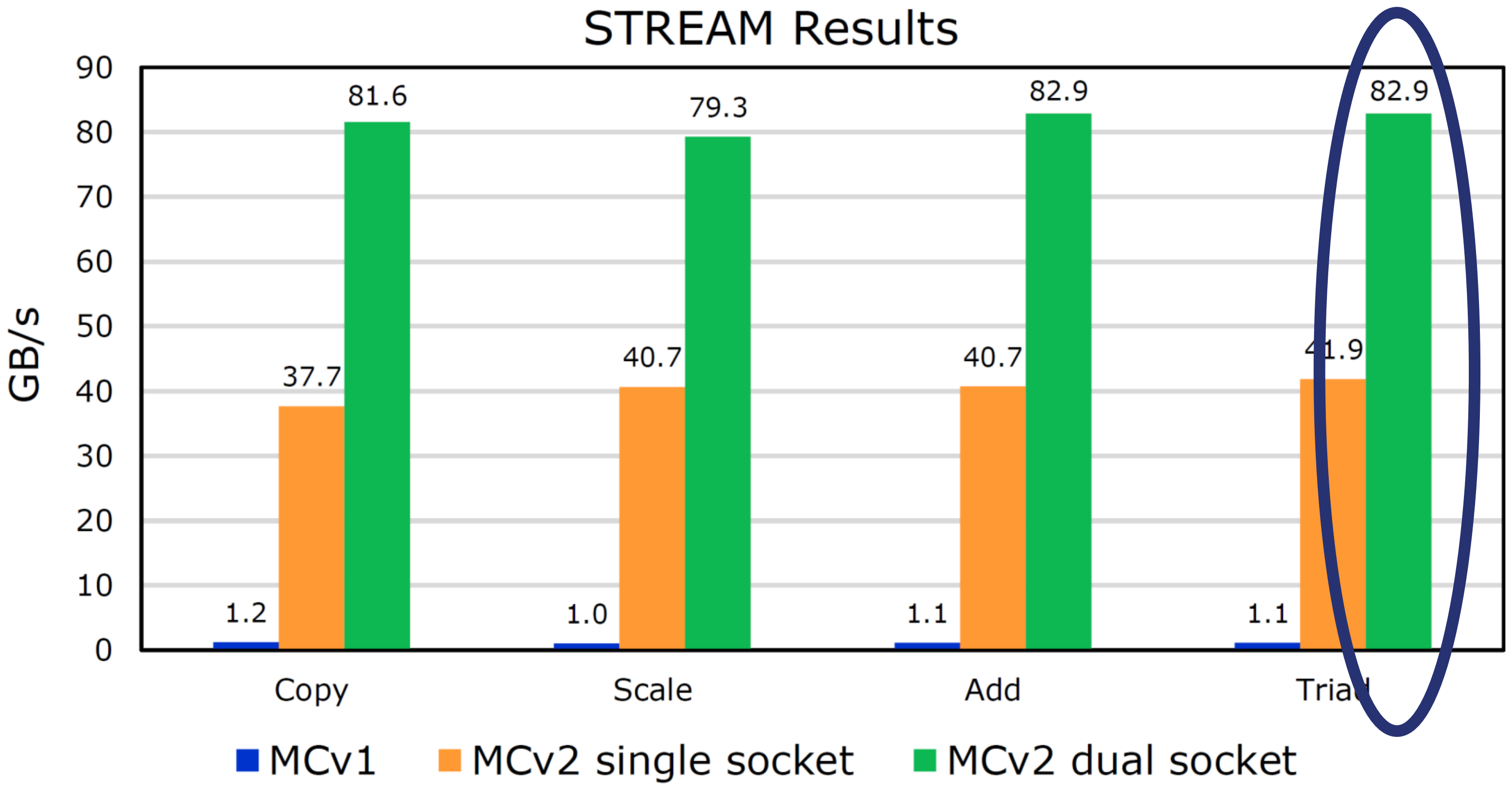
  - Max: 41.9 GB/s
- **E4 RSV10 dual socket:**
  - 64 threads
  - 8 memory channels
  - Max: 82.9 GB/s



HPL Single Node Results

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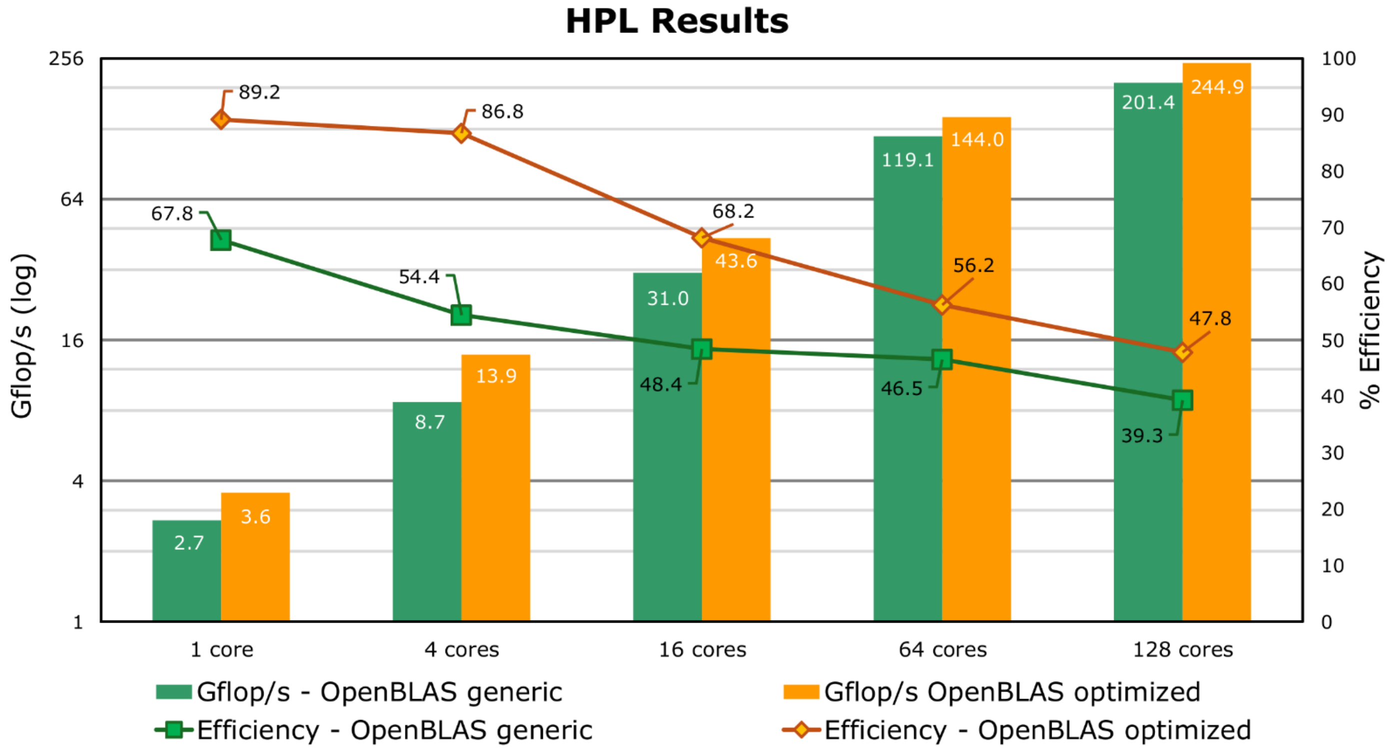
  - HPL + vanilla OpenBLAS
  - HPL + optimized OpenBLAS



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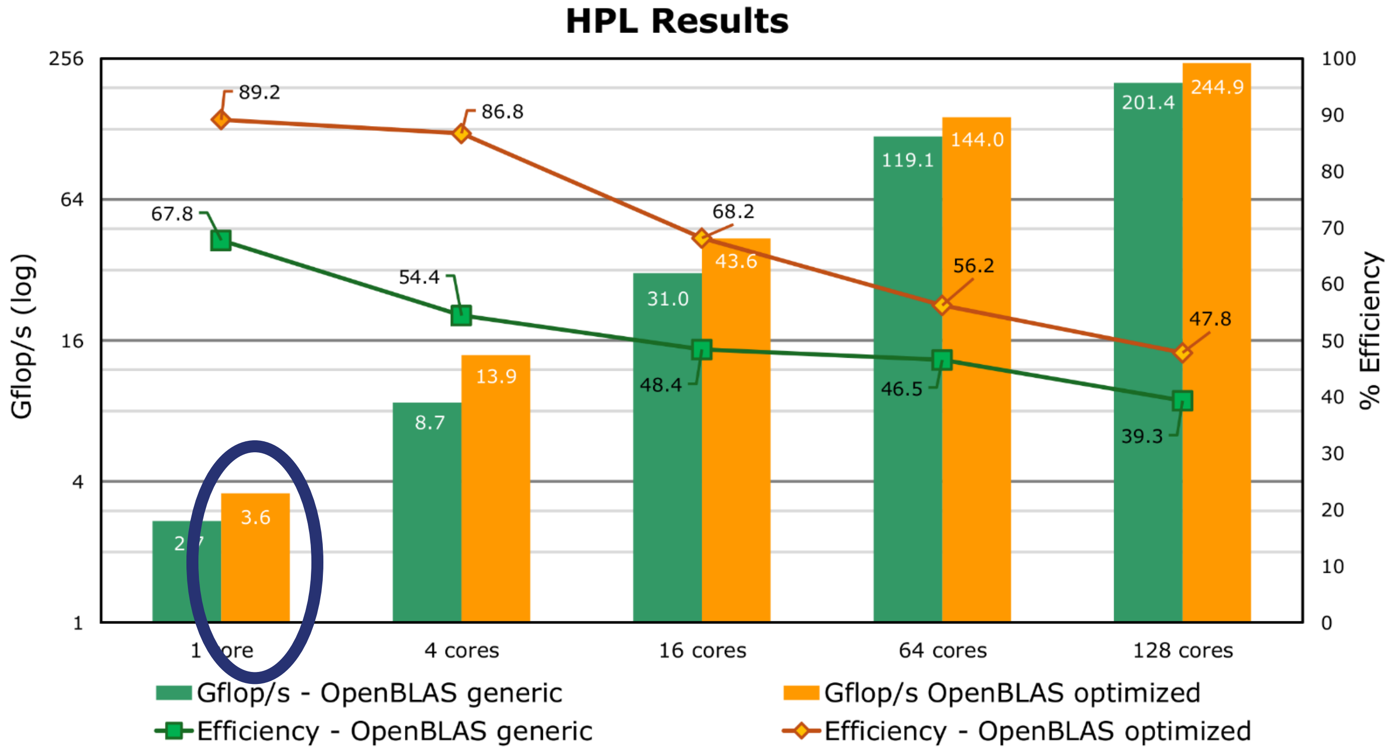

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  - 64 cores:
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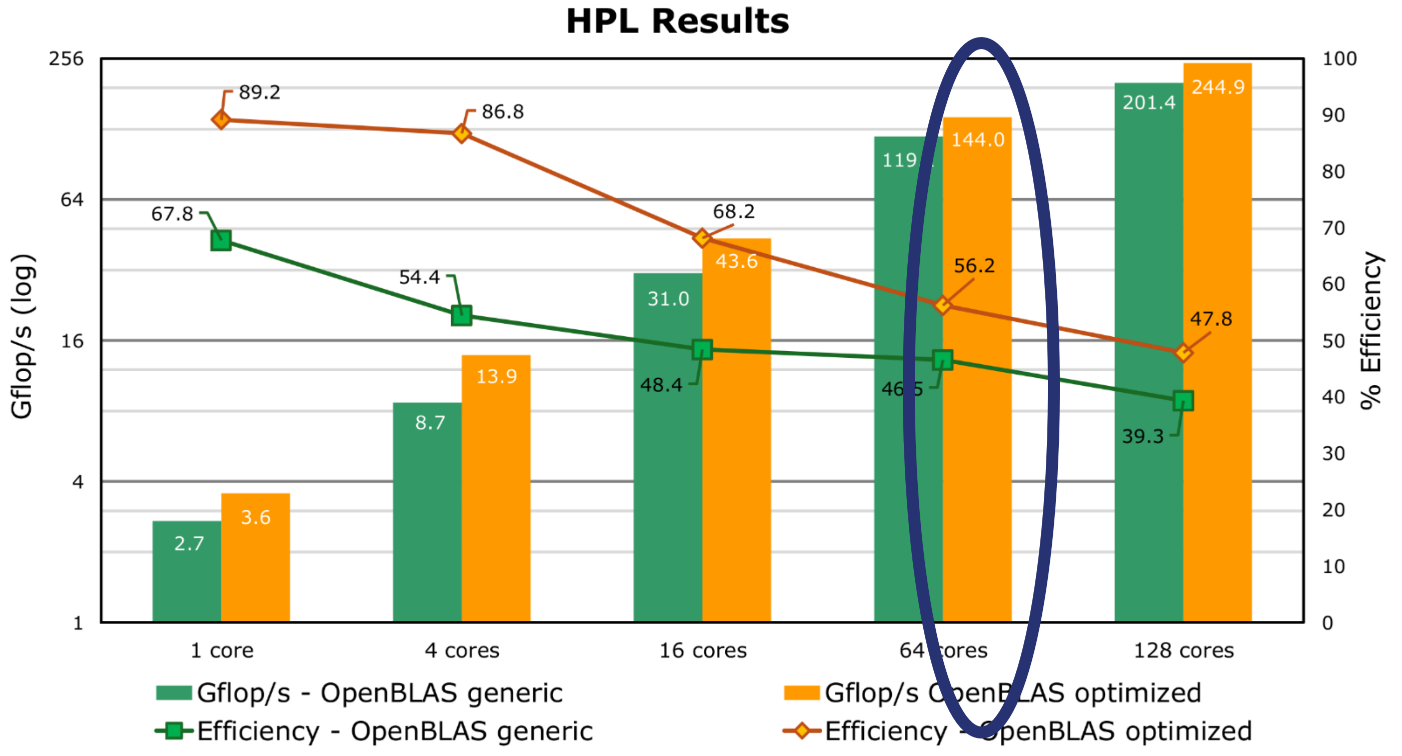

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  - 128 cores:
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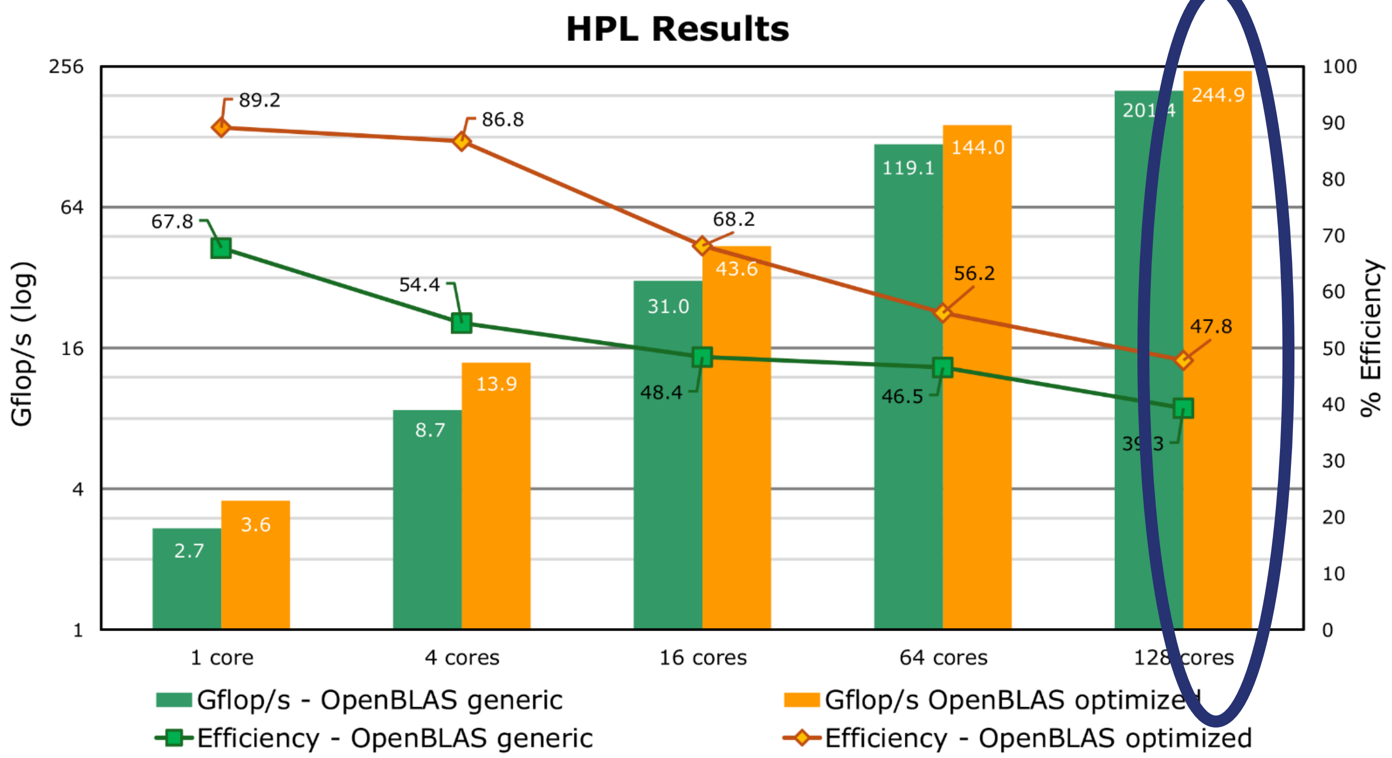

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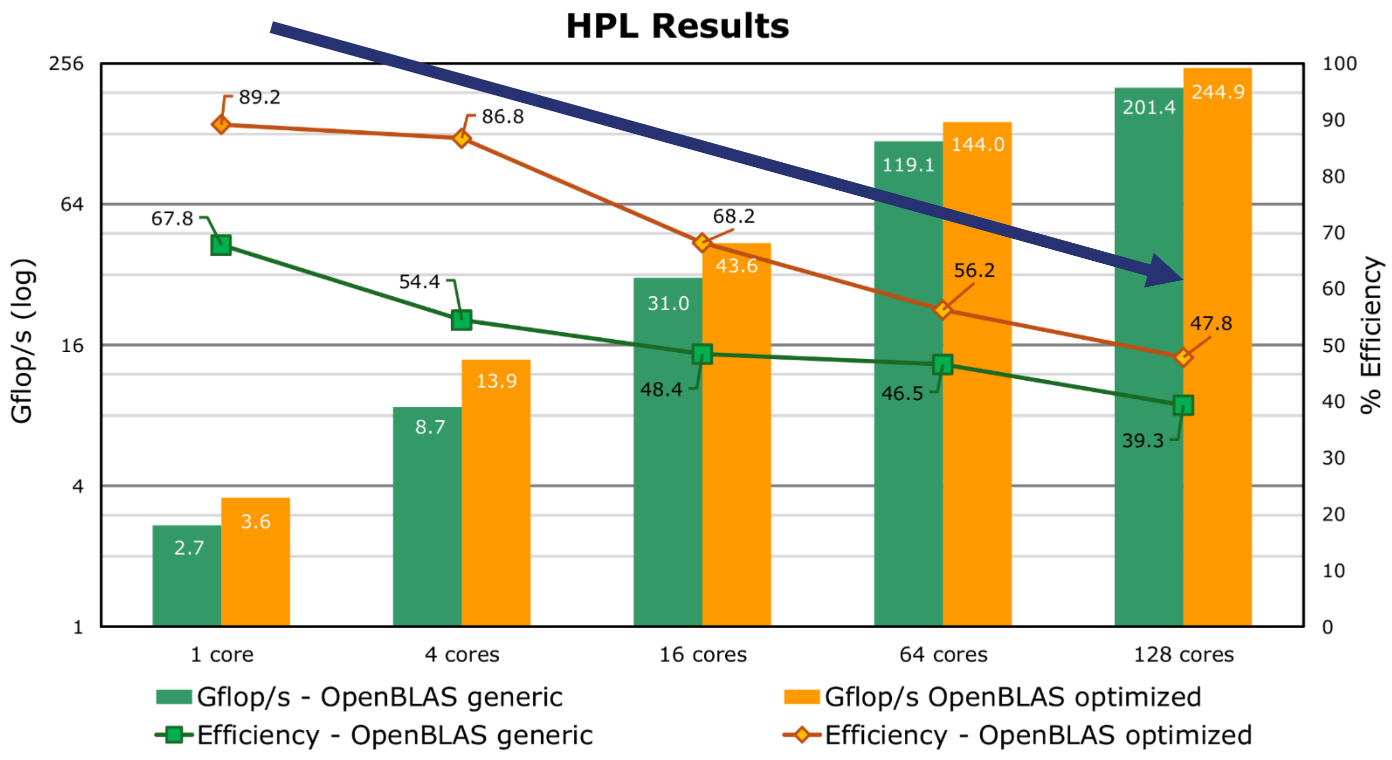

- Decreasing efficiency with incremental core count

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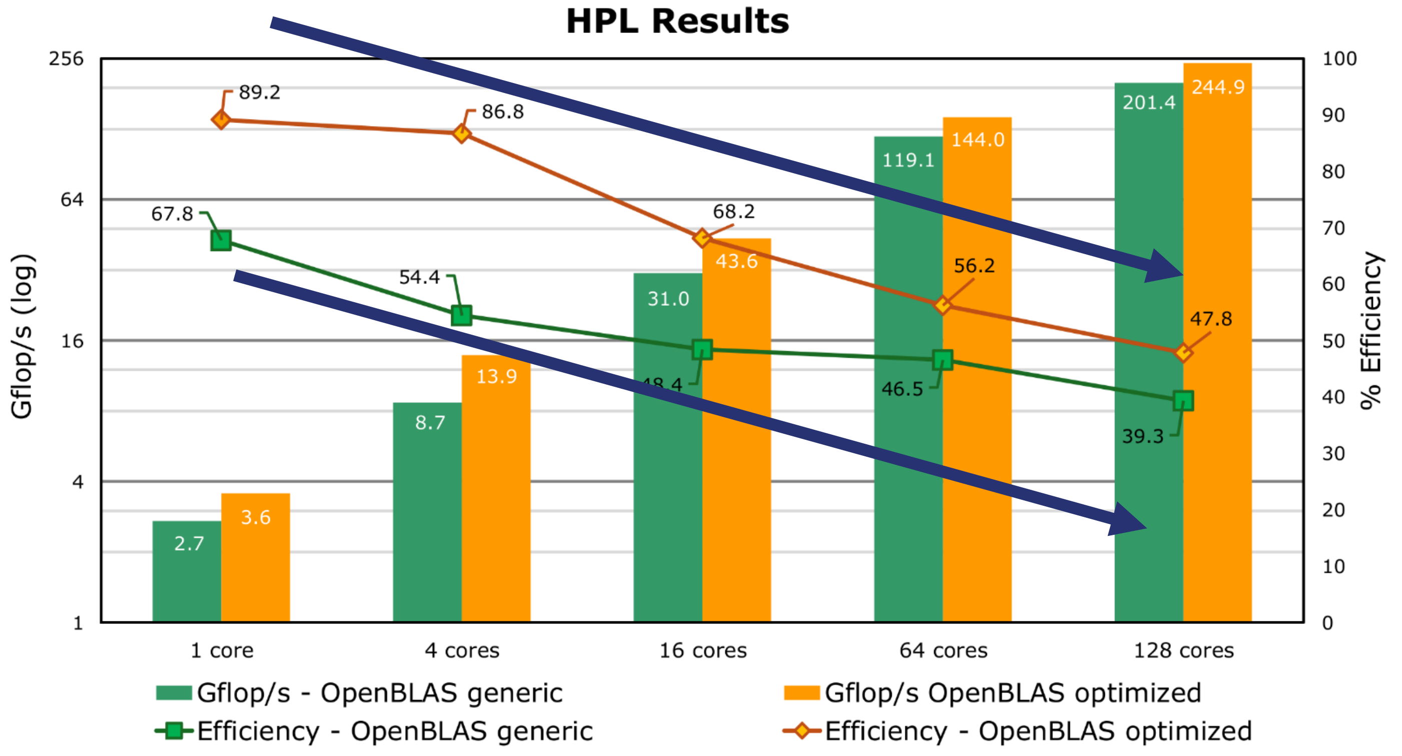

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- Optimized OpenBLAS experience the same bottlenecks as vanilla ones

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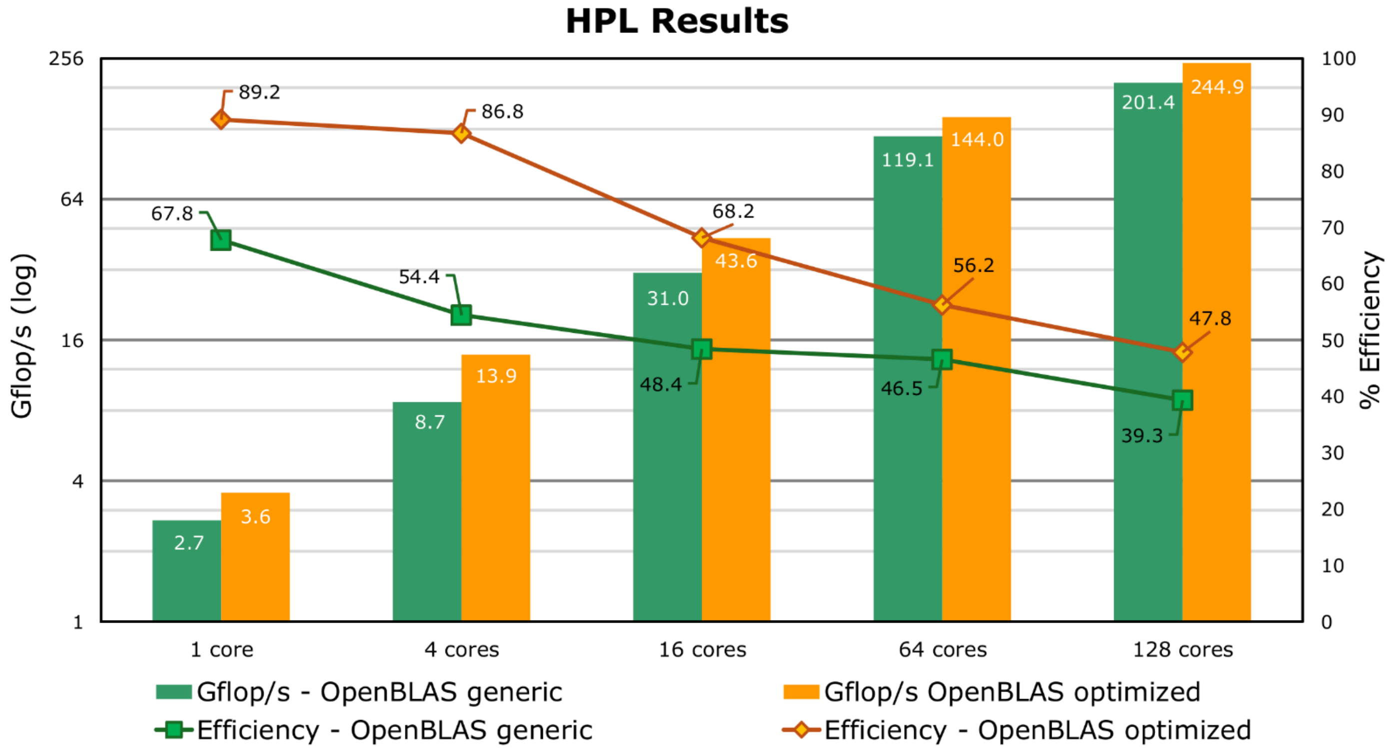
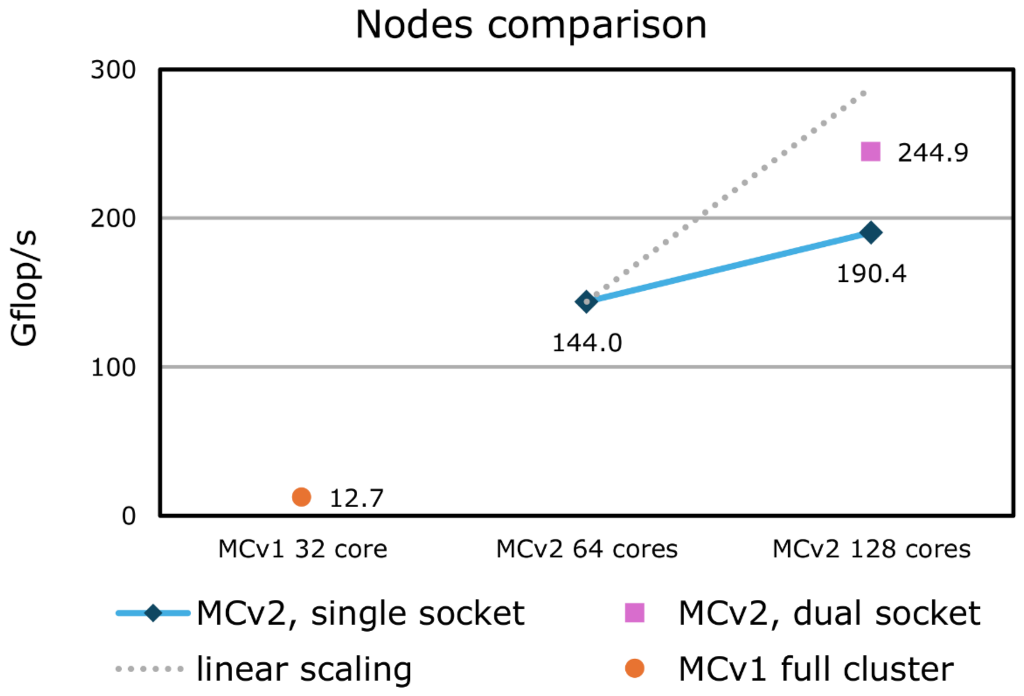


- Decreasing efficiency with incremental core count
- Optimized OpenBLAS experience the same bottlenecks as vanilla ones
- The bottleneck was identified as the memory subsystem

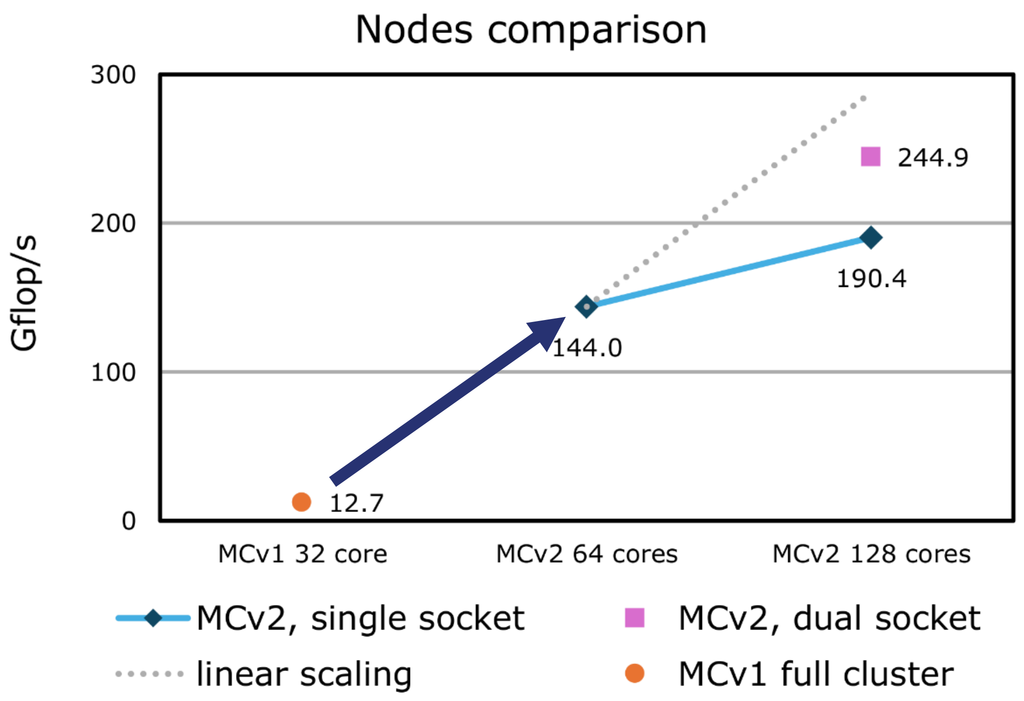
HPL Multi Node Results



HPL Multi Node Results

- **MCv1 full cluster:**
  - Linear scaling in multi node runs
  - HPL: 12.65 Gflop/s

- **MCv2 single node, single socket:**
  - 64 cores
  - HPL: 144.0 Gflop/s



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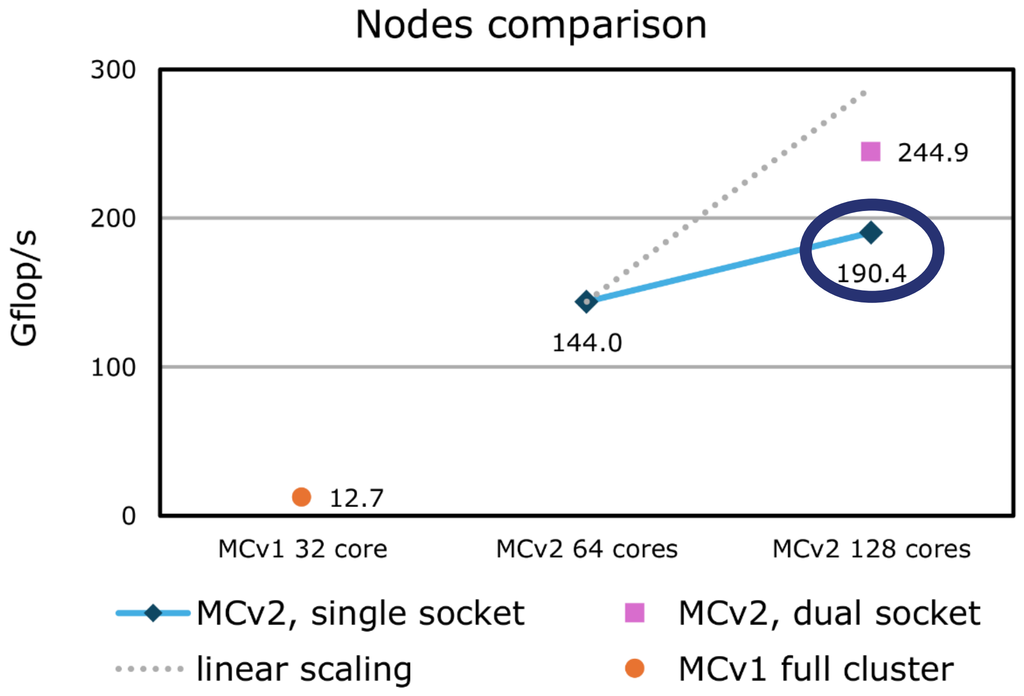
- **MCv2 single node, single socket:**
  - 64 cores
  - HPL: 144.0 Gflop/s
- **MCv2 dual node, single socket:**
  - 128 cores
  - Ethernet 1Gbit/s network
  - HPL: 190.4 Gflop/s



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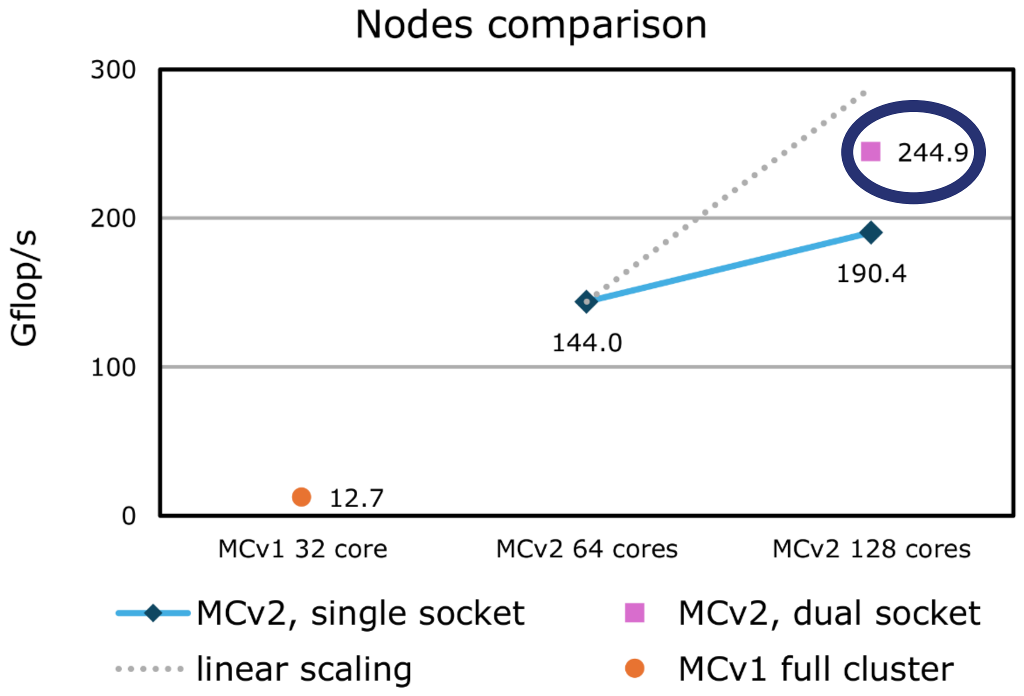

- **MCv2 dual node, single socket:**
  - 128 cores
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  - HPL: 190.4 Gflop/s
- **MCv2 single node, dual socket:**
  - 128 cores
  - On board communication
  - HPL: 244.9 Gflop/s

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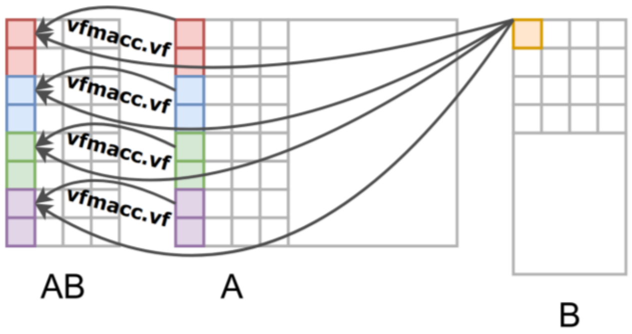

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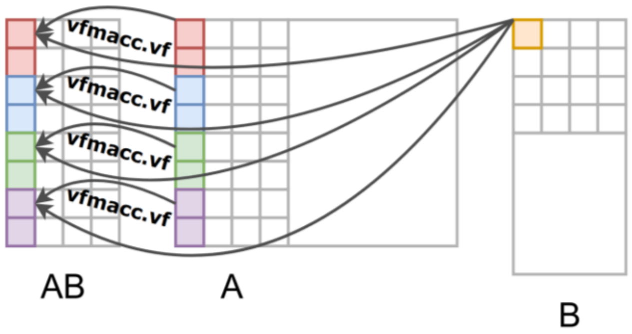

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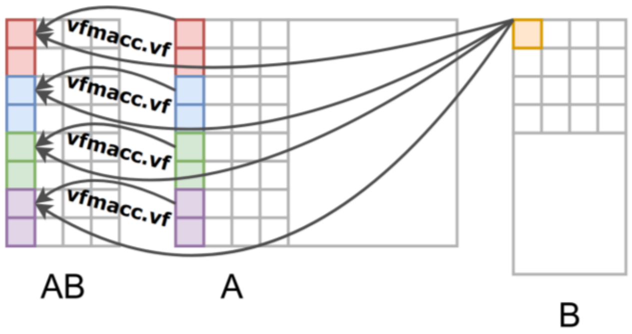

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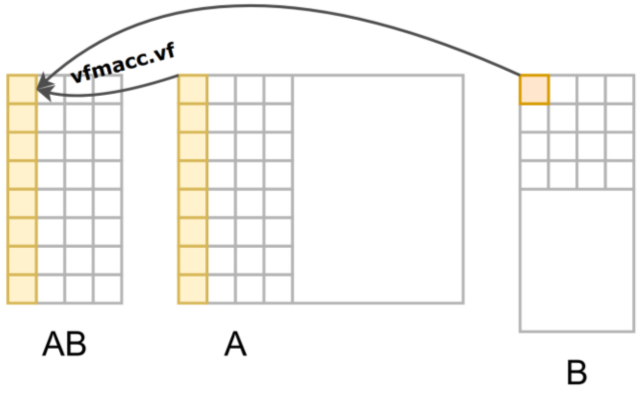
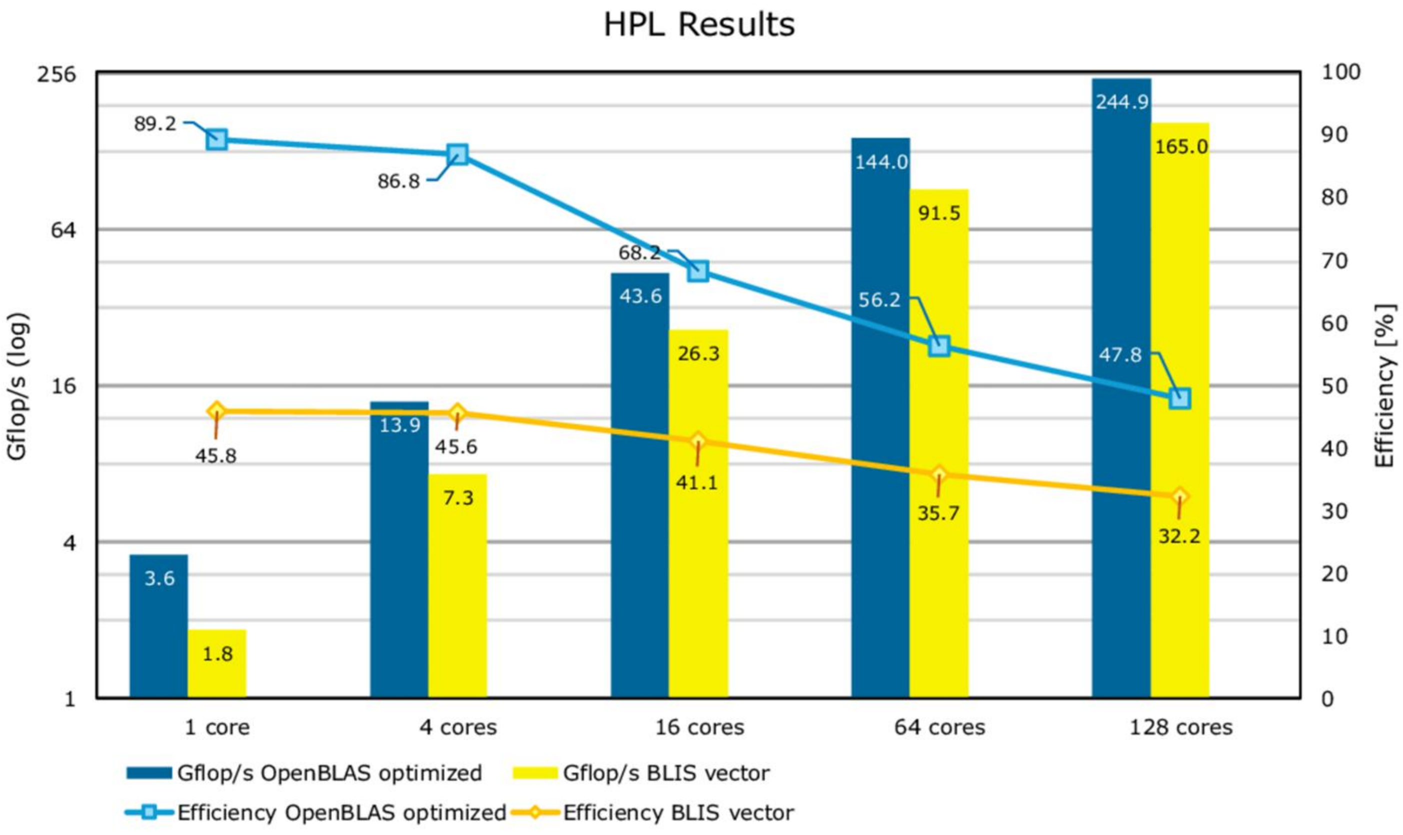


Proposed optimization strategy

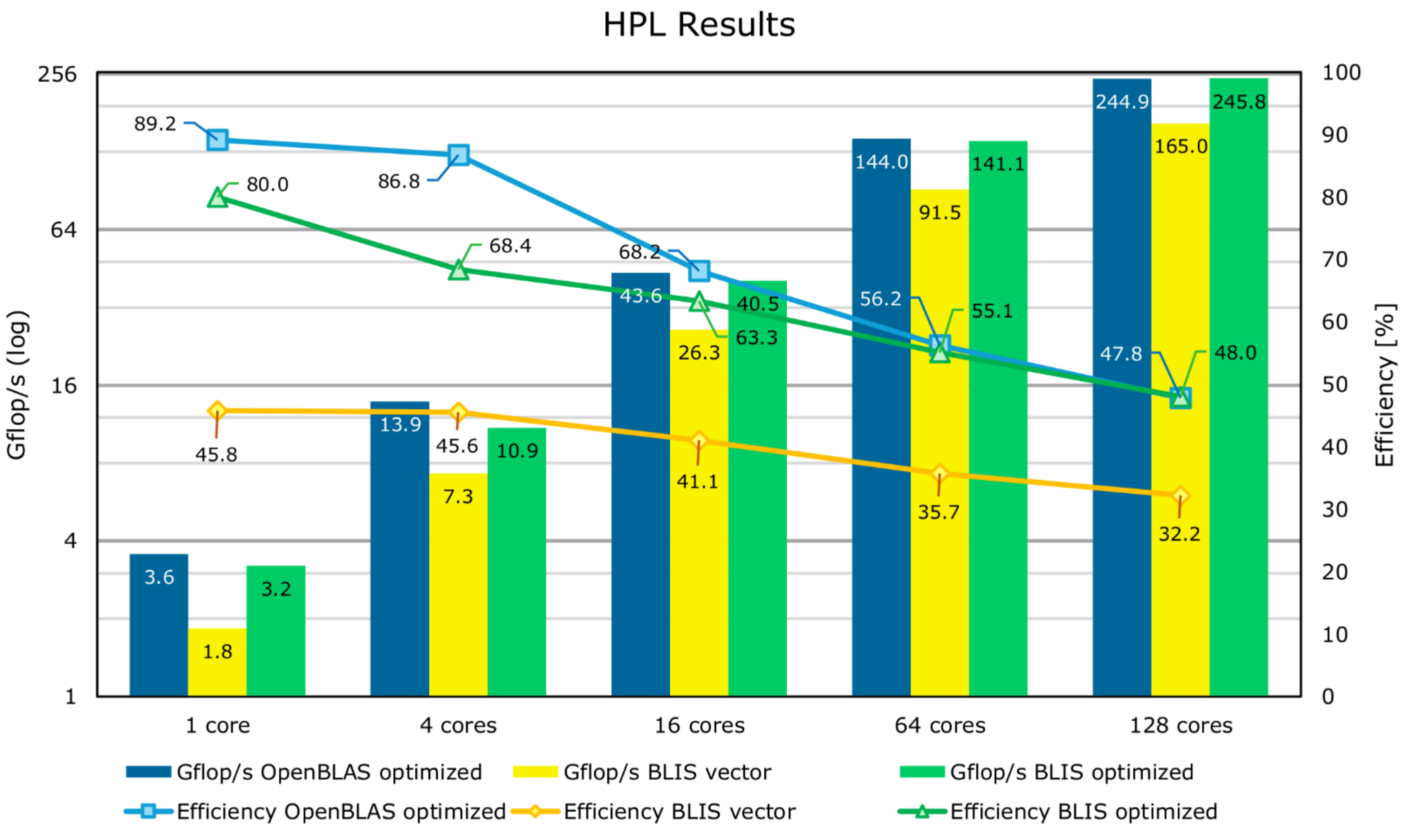
HPL BLIS Results

- The available vectorized BLIS micro-kernel performed poorly



HPL BLIS Results

- The available vectorized BLIS micro-kernel performed poorly
- **Boost in performance post optimization:**
  - 49% improvement w.r.t. original vectorized BLIS (dual socket and 128 core runs)
  - Performance on par with vendor OpenBLAS
  - Effectiveness of register grouping



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