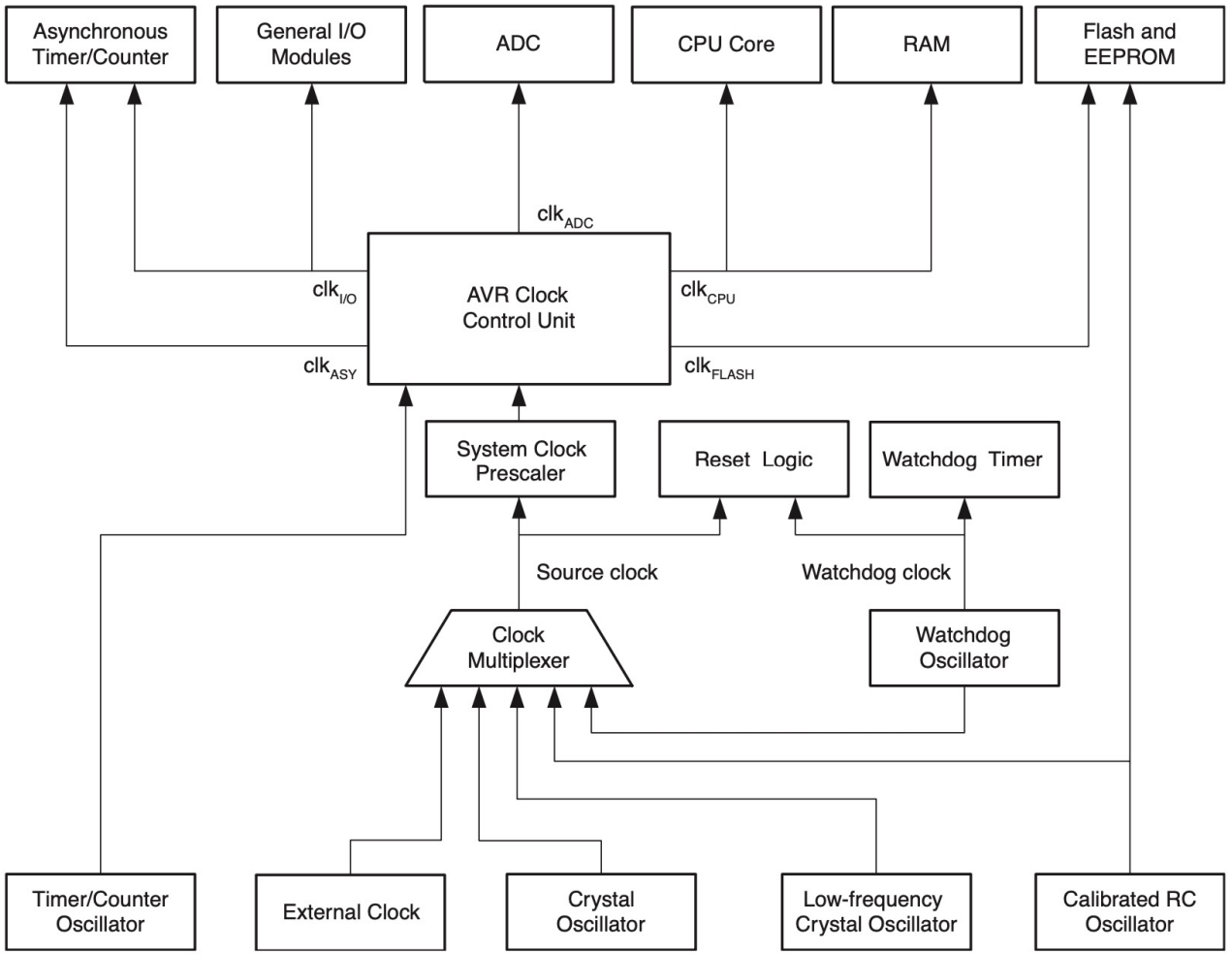
Power Management and Sleep Modes

AVR Clock Distribution



- Clocks to modules not being used can be halted to reduce power consumption by using different sleep modes
- The device is shipped with internal RC oscillator at 8.0MHz and with the fuse CKDIV8 programmed, resulting in 1.0MHz system clock

AVR Sleep Modes: Mode Description

- Sleep modes can be used to shut down unused modules to save power
- AVR provides various sleep modes allowing the user to tailor the power consumption to the application's requirements.

	Active Clock Domains					Oscillators		Wake-up Sources							
	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other I/O	Software BOD Disable
Idle			X	X	X	X	X(2)	X	X	X	X	X	X	X	
ADC Noise Reduction				X	X	X	X(2)	X	X	X(2)	X	X	X		
Power-down								X	X				X		X
Power-save					X		X(2)	X	X	X			X		X
Standby(1)						X		X	X				X		X
Extended Standby					X(2)	X	X(2)	X	X	X			X		X

AVR Sleep Modes: Enable

- To enter any of the six sleep modes, the SE bit in SMCR must be written to logic one and a SLEEP instruction must be executed.
- The SM2, SM1, and SM0 bits in the SMCR Register can be used to select the sleep mode
- The MCU wakes up from sleep when any enabled interrupt occurs
- Interrupt must be disabled before enter any sleep mode

AVR Sleep Modes: Register Description

SMCR – Sleep Mode Control Register

The Sleep Mode Control Register contains control bits for power management.

Bit	7	6	5	4	3	2	1	0	
0x33 (0x53)	–	–	–	–	SM2	SM1	SM0	SE	SMCR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

SM2	SM1	SM0	Sleep Mode
0	0	0	Idle
0	0	1	ADC Noise Reduction
0	1	0	Power-down
0	1	1	Power-save
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Standby(1)
1	1	1	External Standby(1)

Power Reduction Register (PRR)

- PRR provides a method to stop the clock to individual peripherals to reduce power consumption
- Module shutdown can be used in Idle mode and Active mode to significantly reduce the overall power consumption. In all other sleep modes, the clock is already stopped.

Bit	7	6	5	4	3	2	1	0	
(0x64)	PRTWI	PRTIM2	PRTIM0	–	PRTIM1	PRSPI	PRUSART0	PRADC	PRR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

AVR Sleep Modes: Sample Code

```
#include<avr/sleep.h>
#include <avr/power.h>

ISR (..._vect) {

}

int main() {
    // initialize peripheral
    sei();

    set_sleep_mode(SLEEP_MODE_PWR_SAVE);
    sleep_enable();

    power_twi_disable();
    ...
}
```

SLEEP_MODE_IDLE
SLEEP_MODE_ADC
SLEEP_MODE_PWR_DOWN
SLEEP_MODE_PWR_SAVE
SLEEP_MODE_STANDBY
SLEEP_MODE_EXT_STANDBY

Set sleep mode using SLEEP_MODE_... macros

Disable/Enable peripherals to save power
See: https://www.nongnu.org/avr-libc/user-manual/group__avr__power.html

AVR Brown-out Detection Circuit (BOD)

- Brown-out Detection circuit monitors the VCC level during operation by comparing it to a fixed trigger level adjustable by the BODLEVEL fuses.
- Brown-out Reset is activated after the voltage drop for longer than t_{BOD}. Operation resumes after the voltage rise for longer than t_{TOUT}

High Fuse Byte	Bit No	Description	Default Value
BODLEVEL2(4)	2	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL1(4)	1	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL0(4)	0	Brown-out Detector trigger level	1 (unprogrammed)

AVR Brown-out Detection Circuit (BOD)

High Fuse Byte	Bit No	Description	Default Value
BODLEVEL2[4]	2	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL1[4]	1	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL0[4]	0	Brown-out Detector trigger level	1 (unprogrammed)

BODLEVEL 2:0 Fuses	Min. V_{BOT}	Typ V_{BOT}	Max V_{BOT}	Units
111	BOD Disabled			
110	1.7	1.8	2.0	V
101	2.5	2.7	2.9	
100	4.1	4.3	4.5	
011	Reserved			
010				
001				
000				

ATMega328P Maximum frequency vs Vcc

The Maximum Frequency vs. VCC curve is linear between
1.8V < VCC < 2.7V and between 2.7V < VCC < 4.5V