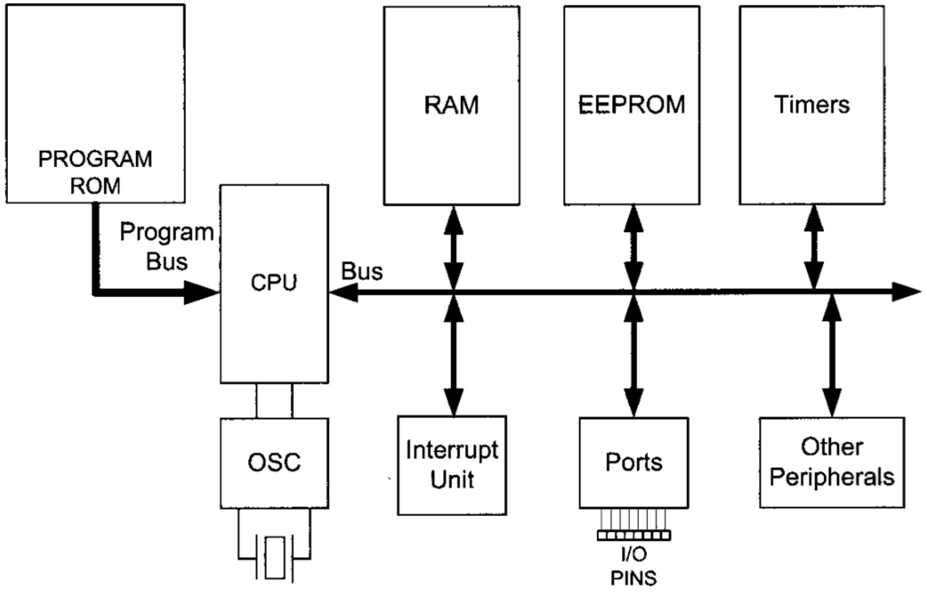
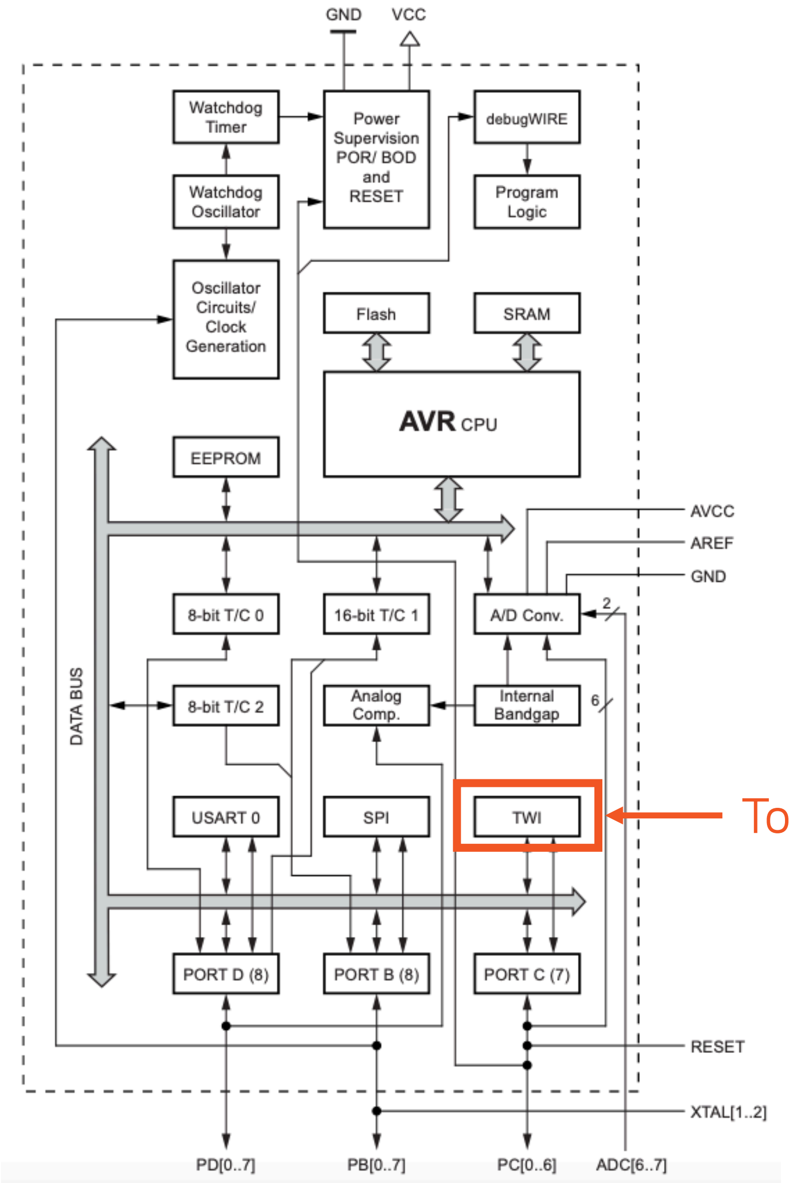
Inter-Integrated Circuit (I^2C) Protocol

Recall AVR Architecture



Simplified AVR Architecture



Today’s Topic

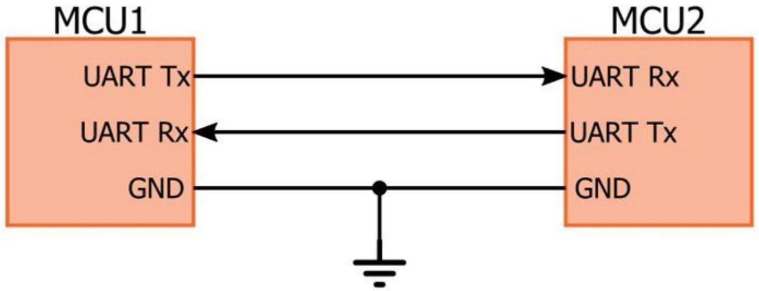
ATMega328P Architecture

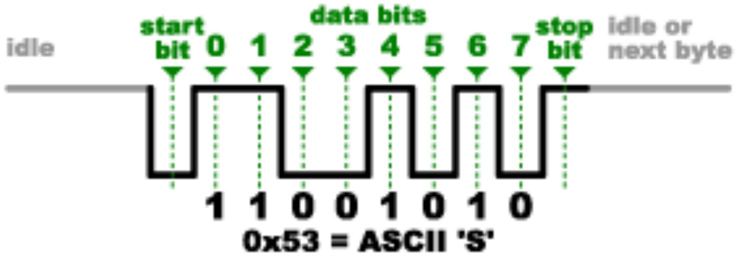
Recap: UART Communication

- Full duplex asynchronous serial communication protocol using 3 wires (TX, RX, GND)
- Widespread availability on PC

Drawbacks

- Erroneous transmission when both sides aren't operated at the same speed
- Single transmitter and receiver





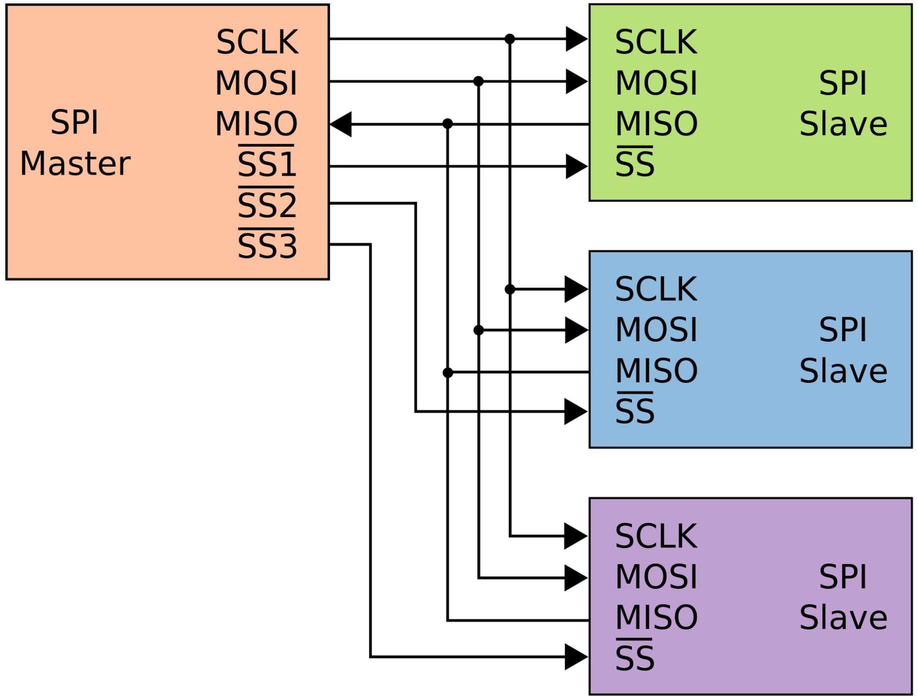
Recap: Serial Peripheral Interface (SPI)

- Full duplex synchronous serial communication protocol using 5 wires (SCK, MOSI, MISO, ~SS, GND)
- High data rate due to the additional clock signal

Drawbacks

- High number of signal wires required (3 + number of devices)

SPI connection with multiple slave devices

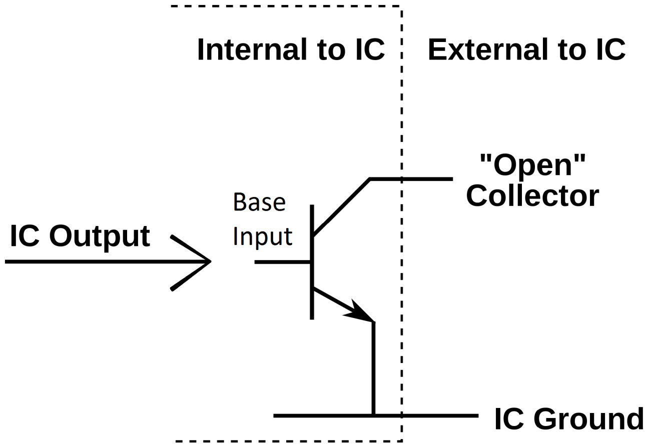


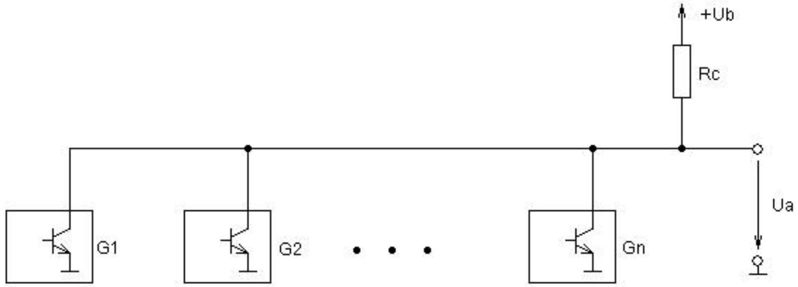
Inter-Integrated Circuit (I^2C): General Features

- Developed in 1982 by Philips for various Philips chips
- Use two "open drain" wires: SDA (data signal) and SCL (clock signal)
- Support up to 112 peripheral devices using 7-bit addresses (due to some reserved addresses)
- Support a multi-controller system, allowing more than one controller to communicate with all peripherals on the bus
- Data rates fall between asynchronous serial and SPI at 100kHz or 400kHz (three additional modes including fast-mode (1MHz), high-speed (3.4MHz), ultra-fast mode (5MHz))

Open Collector / Open Drain Output

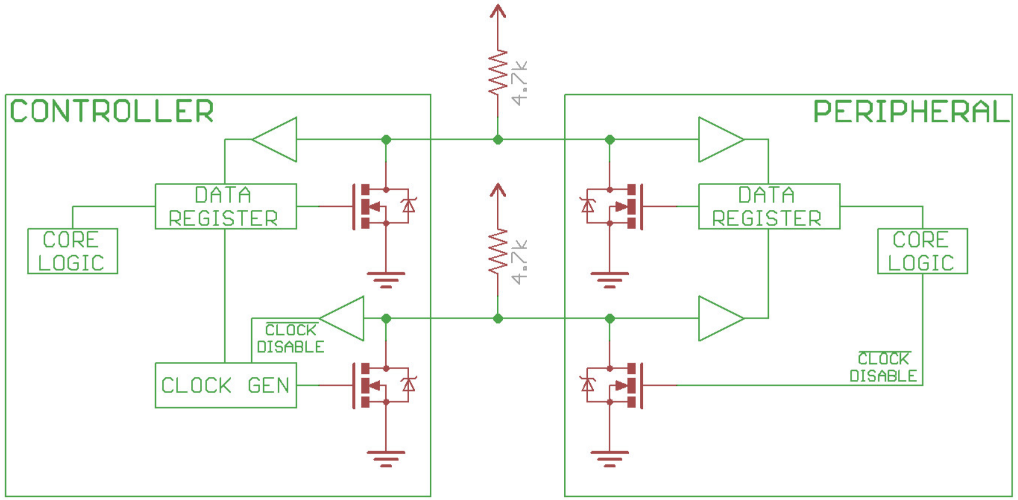
- Common type of output in many ICs which behaves like a switch that is either connected to ground or disconnected
- Flexible voltage level as pull-up resistor is external and connect to external supply voltage
- Several open-collector outputs can be connected to a single line called “wired AND” e.g. connect multiple devices to one interrupt request signal
- High power consumption as pullup resistor dissipates power whenever the output is pulled low





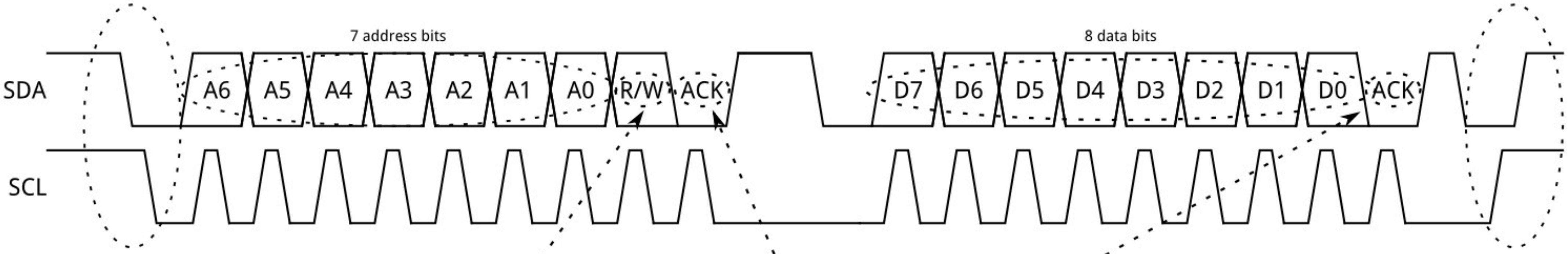
Inter-Integrated Circuit (I^2C): Circuit Connection

- The SDA and SCL signal are "open drain" to avoid bus contention
- Each signal line has a pull-up resistor (usually 4.7K or lower depend on speed and number of devices) on it to pull the logic to high when no device asserts it low



Inter-Integrated Circuit (I^{2}C): Protocol

- Two frame types: address frame and data frame
- Address frame indicates which peripheral should receive the message
- Address frame is followed by one or more data frame. Each data frame passes 8-bit data from controller to peripheral or vice versa



Start condition:
SDA goes low before SCL

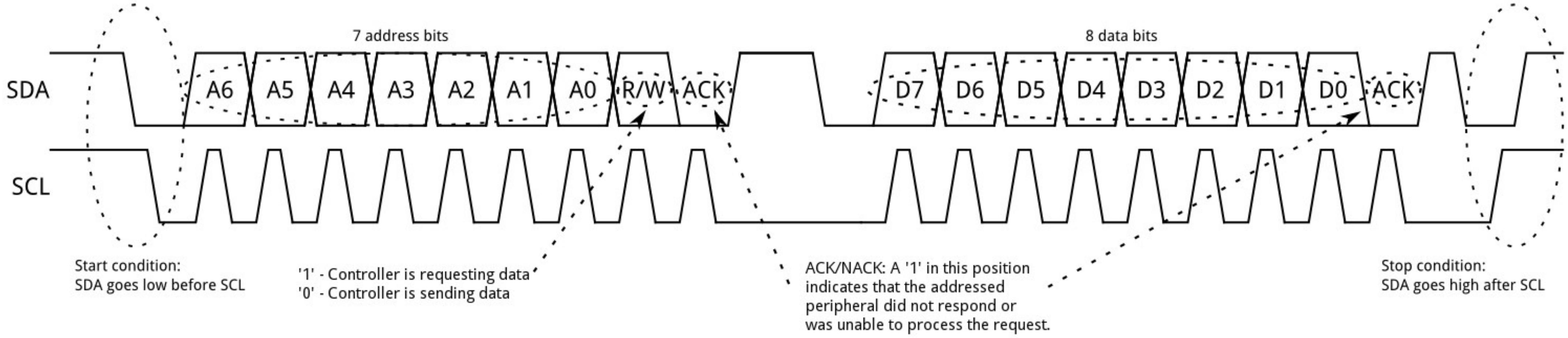
'1' - Controller is requesting data
'0' - Controller is sending data

ACK/NACK: A '1' in this position indicates that the addressed peripheral did not respond or was unable to process the request.

Stop condition:
SDA goes high after SCL

Inter-Integrated Circuit (I^2C): Start Condition

- The controller device leaves SCL high and pulls SDA low
- When two controllers wish to take ownership of the bus at one time, whichever device pulls SDA low first wins the race and gains control of the bus



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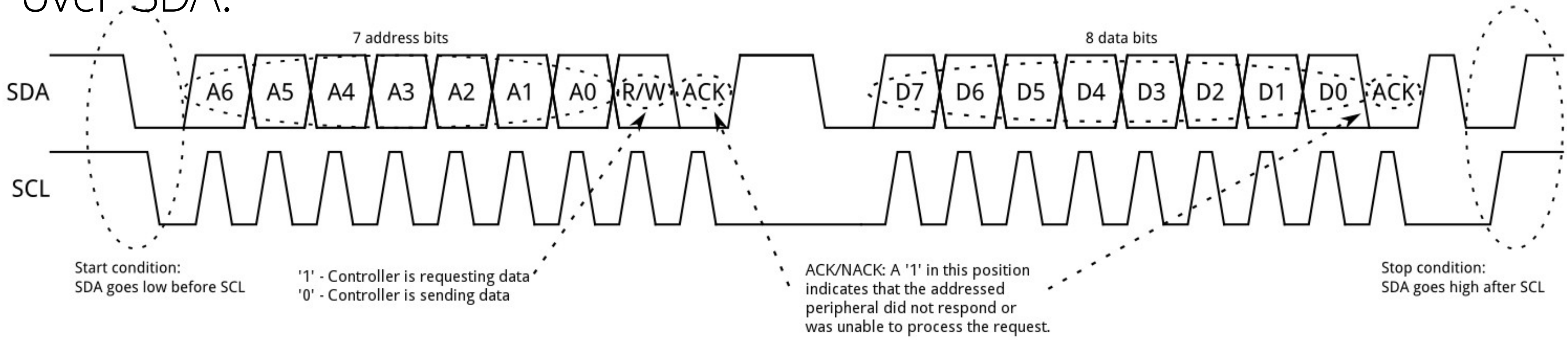
Stop condition:
SDA goes high after SCL

Inter-Integrated Circuit (I^2C): Address Frame

- Address is clocked out most significant bit (MSB) first, followed by a R/W bit indicating whether this is a read (1) or write (0) operation
- The 9th bit of the frame (data or address) is the NACK/ACK bit. Once the first 8 bits of the frame are sent, the receiving device is given control over SDA.



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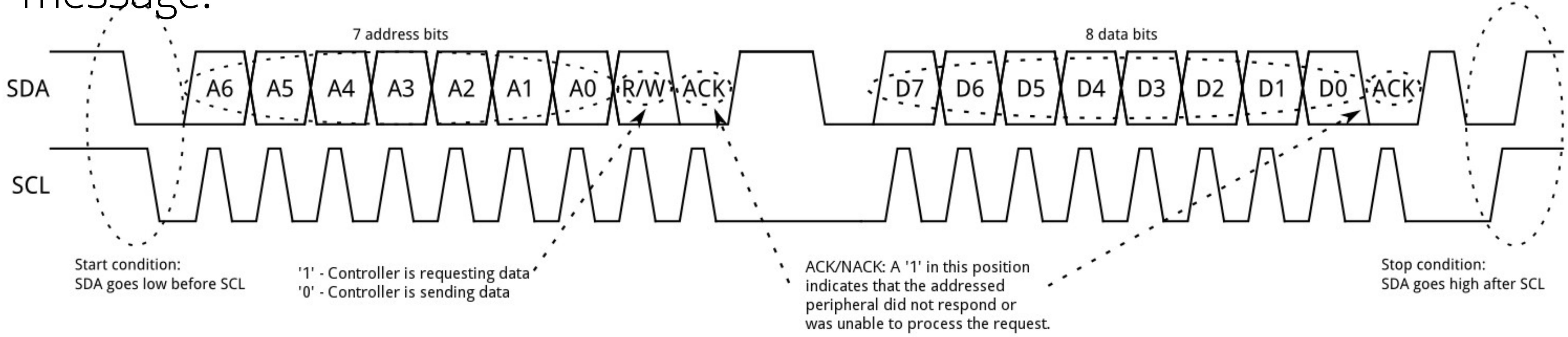
Stop condition:
SDA goes high after SCL

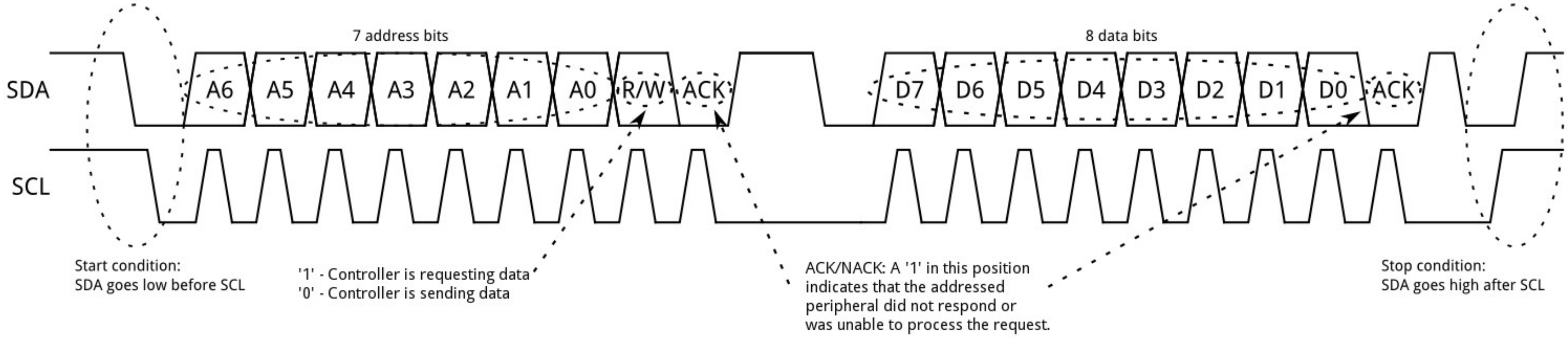
Inter-Integrated Circuit (I^2C): NACK/ACK

- The receiving device must pull the SDA low to indicate a successful transfer. Otherwise, the SDA line will be HIGH by the pull up resistor.
- If SDA is HIGH (by the receiving device or pull up resistor), the receiving device may not receive the data or did not know how to parse the message.


7 address bits
8 data bits
SDA
SCL
A6
A5
A4
A3
A2
A1
A0
R/W
ACK
D7
D6
D5
D4
D3
D2
D1
D0
ACK
Start condition:
SDA goes low before SCL
'1' - Controller is requesting data
'0' - Controller is sending data
ACK/NACK: A '1' in this position
indicates that the addressed
peripheral did not respond or
was unable to process the request.
Stop condition:
SDA goes high after SCL

Inter-Integrated Circuit (I^{2}C): Data Frame

After the address frame has been sent, the controller continue generating clock pulses at a regular interval, and the data will be placed on SDA by either the controller or the peripheral, depending on whether the R/W bit indicated a read or write operation.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A0
R/W
ACK
D7
D6
D5
D4
D3
D2
D1
D0
ACK
Start condition:
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'1' - Controller is requesting data
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Stop condition:
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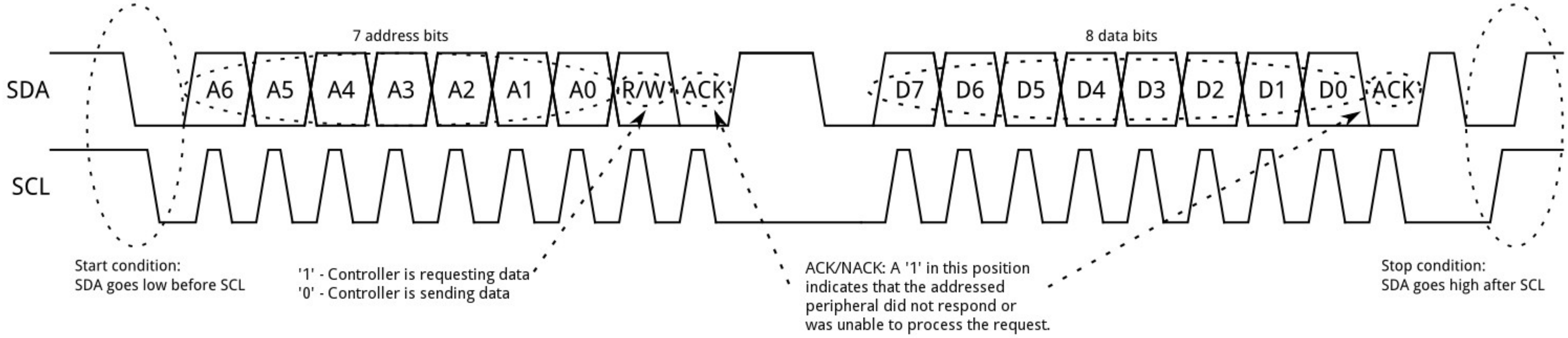
Inter-Integrated Circuit (I^2C): Data Frame

The number of data frames is arbitrary, and most peripheral devices will auto-increment the internal register, meaning that subsequent reads or writes will come from the next register in line.



7 address bits
8 data bits
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SCL
A6
A5
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A0
R/W
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D7
D6
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D3
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D0
ACK
Start condition:
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'1' - Controller is requesting data
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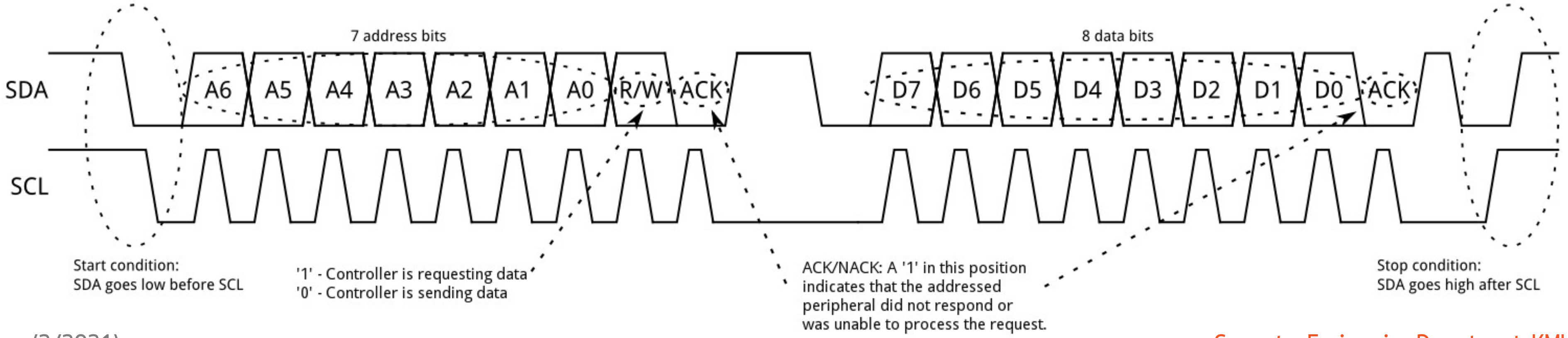
Stop condition:
SDA goes high after SCL

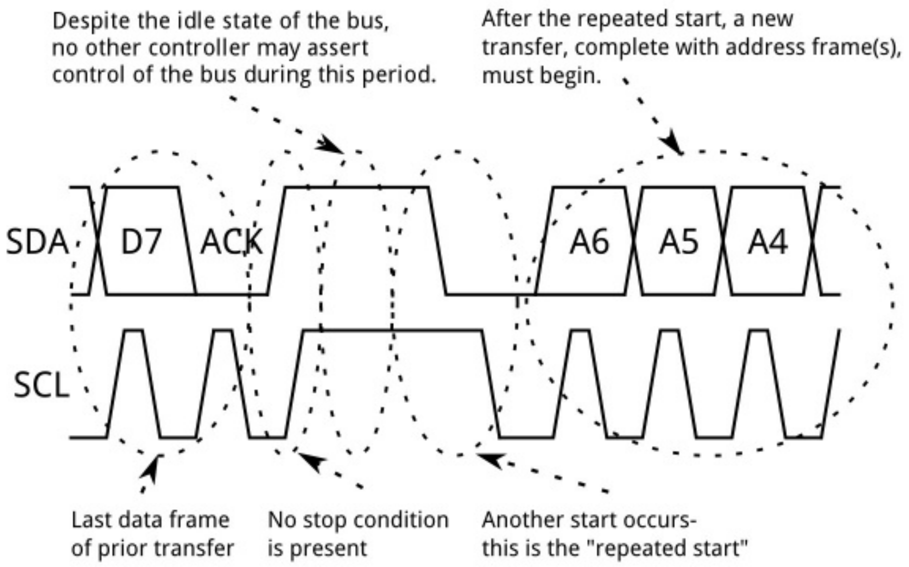
Inter-Integrated Circuit (I^2C): Stop Bit

- The controller generates a stop bit after all data frames have been sent
- Stop conditions are defined by a 0->1 (low to high) transition on SDA after a 0->1 transition on SCL, with SCL remaining high.
- During normal data writing operation, the value on SDA should not change when SCL is high, to avoid false stop conditions.


7 address bits
8 data bits
SDA
SCL
A6
A5
A4
A3
A2
A1
A0
R/W
ACK
D7
D6
D5
D4
D3
D2
D1
D0
ACK
Start condition:
SDA goes low before SCL
'1' - Controller is requesting data
'0' - Controller is sending data
ACK/NACK: A '1' in this position indicates that the addressed peripheral did not respond or was unable to process the request.
Stop condition:
SDA goes high after SCL

Inter-Integrated Circuit (I^{2}C): Repeat Start

- Controller can be allowed to exchange several messages without allowing other controllers on the bus to interfere
- Set SDA to high while SCL is low. Then, the controller begin another start condition



Despite the idle state of the bus, no other controller may assert control of the bus during this period.

After the repeated start, a new transfer, complete with address frame(s), must begin.

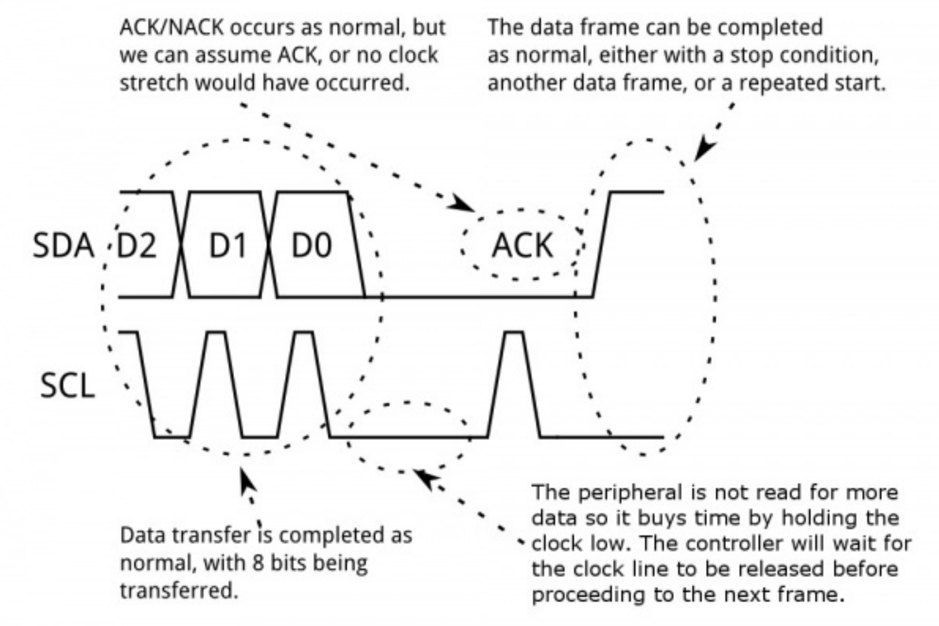
Last data frame of prior transfer

No stop condition is present

Another start occurs- this is the "repeated start"

Inter-Integrated Circuit (I^2C): Clock Stretching

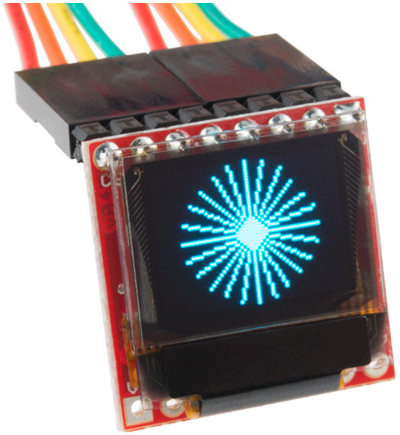
- The peripheral can hold the SCL line low when it isn't ready to response to the controller e.g. the analog-to-digital may still converting data or the EEPROM may still writing to non-volatile memory

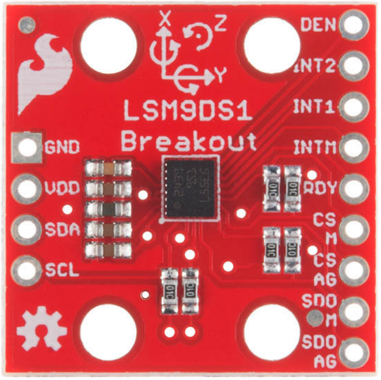


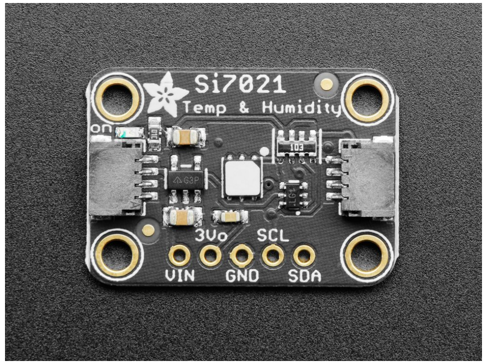
ACK/NACK occurs as normal, but we can assume ACK, or no clock stretch would have occurred.
The data frame can be completed as normal, either with a stop condition, another data frame, or a repeated start.
SDA
D2
D1
D0
ACK
SCL
Data transfer is completed as normal, with 8 bits being transferred.
The peripheral is not read for more data so it buys time by holding the clock low. The controller will wait for the clock line to be released before proceeding to the next frame.

Example of I^{2}C devices

- Sensor (Environment, Motion, Proximity, etc.)
- Actuator (Small OLED Display, LED Driver etc.)
- Microcontroller

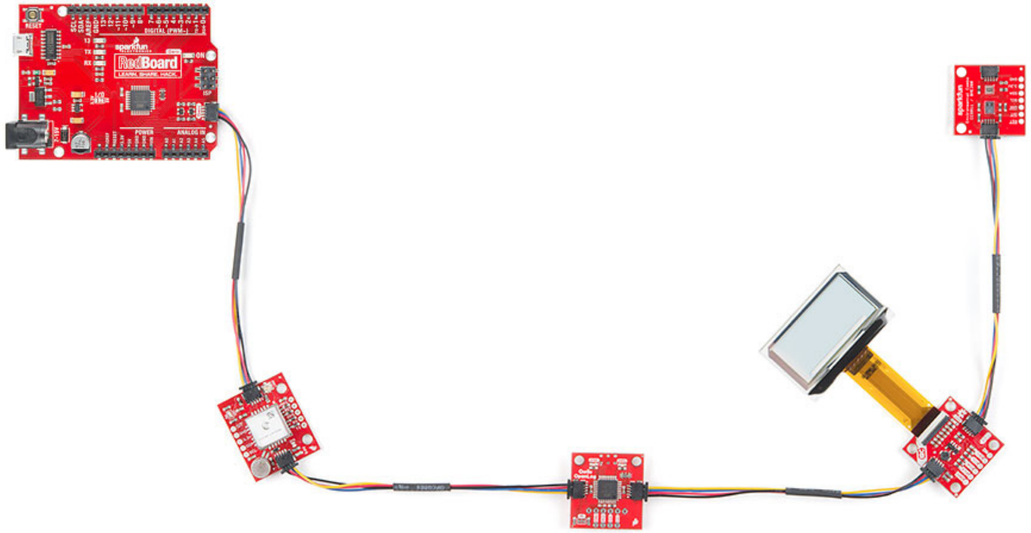


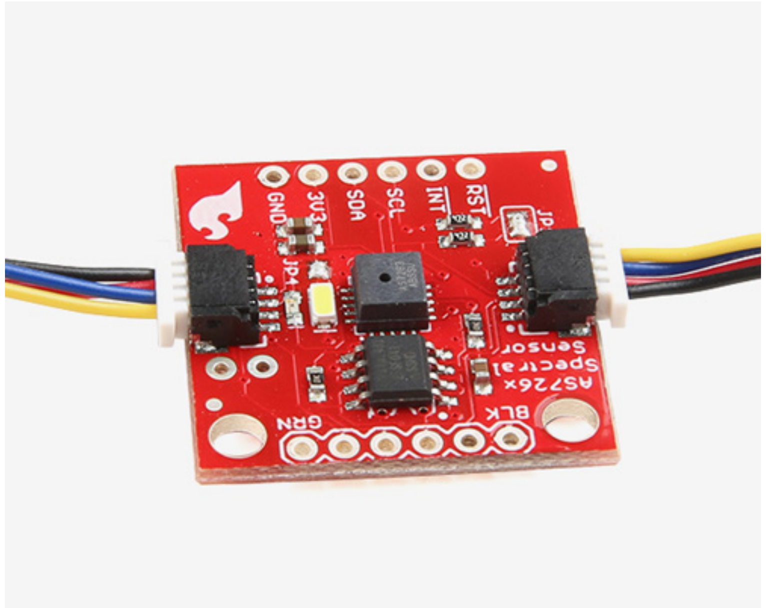




SparkFun's Qwiic / STEMMA QT

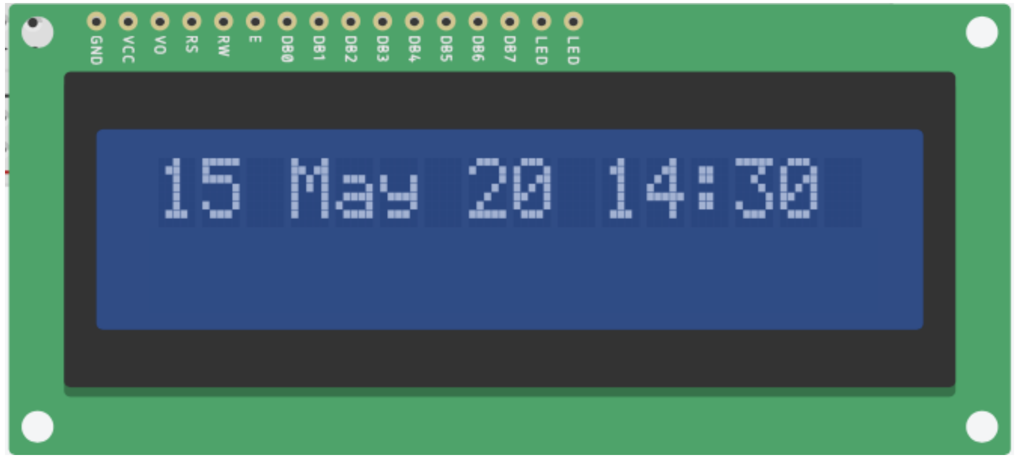
SparkFun's Qwiic Connect System uses 4-pin 1mm pitch polarized JST connectors to quickly interface development boards including sensors, LCDs, relays and more through the I^{2}C interface





Lab 6: AVR I^{2}C Programming

1. Connect a circuit with an ATMega328P and DS1307 (realtime clock IC) and write a program to display the current date and time on the 16x2 alphanumeric LCD screen


GND
VCC
VO
RS
RW
E
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
LED
LED
15 May 20 14:30