E6xx Chipset Microcode release Notes
For CMC C0_22211
Dated 6/25/2011

Please Note: The Usage of the files included in this package requires a valid INTEL PROGRAM AND LICENSE AGREEMENT ("IPLA").

Please contact your Intel Field Application Engineer or Intel Account representative to verify that a valid IPLA is in place prior to using or integrating these files.

For questions related to integration or usage of the following binary packages, please refer to the latest Intel Processor E6xx (Tunnel Creek) BIOS Writers Guide for detail.

CMC package Name: CMC_Rev2.2_B1.zip
- Build Date: 06/25/2011
- File name: C0_22211.BIN

Changes:
- Moved the B unit throttle bit setting from BIOS to CMC to fix image flickering issue.
- Resolved the PCNT disabling issue (in C0_12311). Previously the firmware did not keep the value written to the PCNT register. Now the developer can read the same value as was written to the PCNT register.
- Fixed backward compatibility issue - C0_13511 could only be used on Tunnel Creek B1 stepping. C0_22211 is B1 aware and can identify the silicon stepping to set display chicken bit-15 on B1 stepping.
- No Changes have been applied to memory configuration support, this CMC binary will support the memory configurations listed in C0_12311.BIN

Known Issues:
- None

CMC package Name: CMC_Rev2.1_B1.zip
- Build Date: 05/25/2011
- File name: C0_13511.BIN

Changes:
- The display controller's chicken bit-15 has been set to fix clipped video images.
- No Changes have been applied to memory configuration support, this CMC binary will support the memory configurations listed in C0_12311.BIN

Known Issues:
- None

CMC package Name: CMC_Rev2_B1.zip
- Build Date: 04/05/2011
- File name: C0_12311.BIN

- There is a single version of CMC binary in this package (C0_12311.BIN): CMC_rev2_B1.zip

Changes:

- LTEC video enable delay adjusted from 820ns to 766ns
- Thermal sensor is now enabled by default.
- Disabled external throttling which may cause hang; Disabled processor throttling in firmware.
- Support for B1, B0 and A0 - Merging TNC A0 and B0 CMC by detecting the revision ID.
- IERR have been observed when reading from Display controller; Removed dynamic clock gating configuration from G-unit.

- This CMC binary will support the following memory configurations:
  - 1rank, 256 Mbit, x8, DDR2,
  - 1rank, 512 Mbit, x8, DDR2,
  - 1rank, 1 Gbit, x8, DDR2,
  - 1rank, 2 Gbit, x8, DDR2,
  - 1rank, 512 Mbit, x16, DDR2,
  - 1rank, 1 Gbit, x16, DDR2,
  - 1rank, 2 Gbit, x16, DDR2,
  - 2rank, 512 Mbit, x16, DDR2,
  - 2rank, 1 Gbit, x16, DDR2,
  - 2rank, 2 Gbit, x16, DDR2
  - 2rank, 256 Mbit, x8, DDR2,
  - 2rank, 512 Mbit, x8, DDR2,
  - 2rank, 1 Gbit, x8, DDR2,
  - 2rank, 2 Gbit, x8, DDR2

Known Issues:

- None

CMC package Name: CMC_rev05.zip

- Build Date: 05/11/2010
- File name: C0_190210

Changes:

- First external release that enables Tunnel Creek B0 Stepping.
- Updated PORT: 80h Reg: 60h bit 1's value is now set to 0 to disable fencing on Tunnel Creek processor versus the original value of 1. Tunnel Creek is now set to disable fencing by default.
- Included code to drive SLPMODE, SLPRDY#, RSTRDY# to 0 at the same instance to indicate a catastrophic event, without this inclusion, if a catastrophic event/trigger occurs the platform will not shut down.

- There is a single version of CMC binary in this package (C0_190210.BIN): CMC_rev05.zip

- This CMC binary will support the following memory configurations:
  - 1rank, 256 Mbit, x8, DDR2,
  - 1rank, 512 Mbit, x8, DDR2,
  - 1rank, 1 Gbit, x8, DDR2,

- 1rank, 2 Gbit, x8, DDR2,
- 1rank, 512 Mbit, x16, DDR2,
- 1rank, 1 Gbit, x16, DDR2,
- 1rank, 2 Gbit, x16, DDR2,
- 2rank, 512 Mbit, x16, DDR2,
- 2rank, 1 Gbit, x16, DDR2,
- 2rank, 2 Gbit, x16, DDR2
- 2rank, 256 Mbit, x8, DDR2,
- 2rank, 512 Mbit, x8, DDR2,
- 2rank, 1 Gbit, x8, DDR2,
- 2rank, 2 Gbit, x8, DDR2

Known Issues:

- None

CMC package Name: CMC_rev04.zip

- Build Date: 02/08/2010
- File name: C0_060510_CFG1.BIN & C0_060510_CFG2.BIN

Changes:

- Updated DDR RCOMP Slew rate look up table with more optimized values
- Disable internal fencing mechanism to address "SMI and VLW" failure.
- Set Port: 01 Reg: 11h to enable the glitch filter.
- Resolved issue of memory transaction failure during high temperature.
- Resolved issue related to system hangs at C6 when Windows boots.
- Enables B-unit snoop when transition from C2->C0 instead of C3->C0

Known Issues:

- None

CMC package Name: CMC_rev03.zip

- Build Date: 12/09/2009
- File Name: B0_500309_CFG1.BIN & B0_500309_CFG2.BIN

Changes:

- Since cDMI fencing feature will be removed from the Tunnel Creek silicon, the code was removed from CMC and BIOS that controlled self-enable/disable on cDMI fencing when CPU enters/exits C6.
- Removed HPOC register locking from CMC, the BIOS is now responsible to lock the register.

Known Issues:

- None

CMC package Name: CMC_rev02.zip

- Build Date: 11/23/2009
- File Name: B0_450509_pwrperf_CFG1.BIN & B0_450509_pwrperf_CFG1.BIN

Changes:

- Resolved windows hang issue in video playback

Known Issues:

- None
