Intel® Atom™ Processor E6XX Memory Drive Strength Application Note

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Introduction

This document was created to assist system designers and developers with memory subsystem designs that are outside the specifications defined in the Intel® Atom™ E6xx Processor Platform Design Guide, document #433311.

The memory drive strength for the Intel Atom™ E6xx processor can be modified by making changes to the Chipset Microcode (CMC), to better align with memory load requirements. However, it should be noted that the Intel® Atom™ E6xx processor is limited to two memory drive strength configurations: 39 Ω and 24 Ω

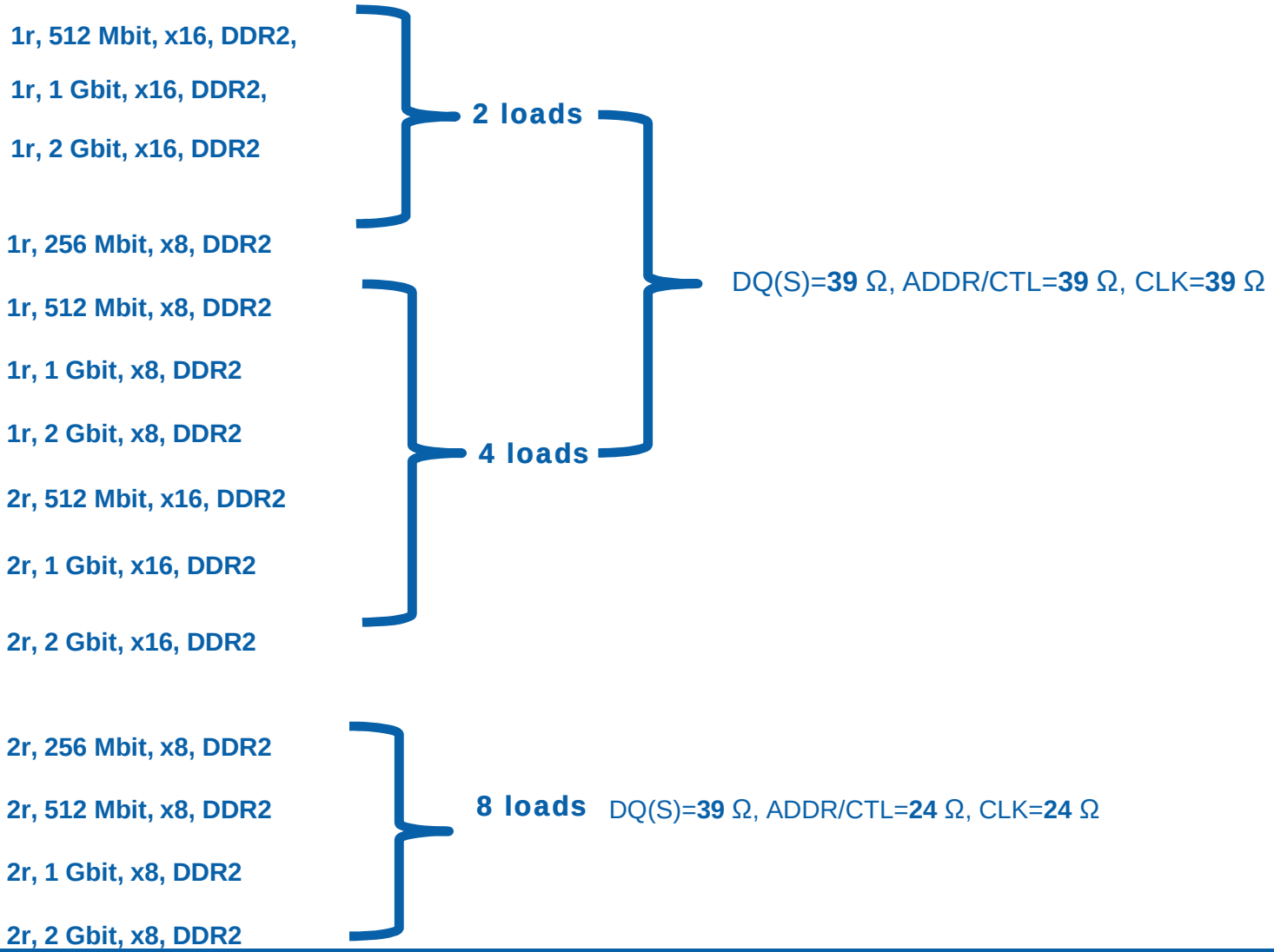
Intel strongly recommends that if memory drive strength changes are introduced, system designers must perform thorough signal integrity and timing simulations for each memory configuration.

Design considerations

- The Intel Atom™ E6xx processor Chipset Microcode (CMC) sets the memory drive strength
- Memory drive strengths are mainly affected by the number of memory devices. Minimal impact from trace length and trace width (board form factor design)
- Current CMC configures the memory drive strength according the number of devices (number of loads). The Intel Atom™ E6xx processor CMC calculates the load based on the GPIO strapping for memory. Refer to section 7.7 in the Intel® Atom™ Processor E6xx Series based Platform Design Guide – Doc#433311.
- The default for 2/4 loads is DQ/DQS/RCVen (39 Ω), CK (39 Ω) and CMD/CTRL/ADD (39 Ω)
- The default for 8 loads is DQ/DQS/RCVen (39 Ω), CK (24 Ω) and CMD/CTRL/ADD (24 Ω)
- The customized CMC sets the desired configuration which will override how the GPIO strapping is set on the platform.

Intel E6XX processor memory configurations

Supported memory drive strength (Defaults)



Potential drive strength combinations

Configuration	DQ/DQS (Ω)	CK (Ω)	ADD/CTRL (Ω)	To use CMC File name:
2/4 loads	**39**	**39**	**39**	**C0_22111.bin ***
	39	24	24	C0_22111_DQ39_ADDRCTR24_CLK24.bin
	39	39	24	C0_22111_DQ39_ADDRCTR24_CLK39.bin
	39	24	39	C0_22111_DQ39_ADDRCTR39_CLK24.bin
8 loads	**39**	**24**	**24**	**C0_22111.bin ***
	24	24	24	C0_22111_DQ24_ADDRCTR24_CLK24.bin

* (Default CMC)

Calculating memory loads

The E6XX memory controller supports **a single**, **32 bit channel** with **x8** and **x16 data width** DRAMs.

8 loads would be:

$$\frac{32bits/_{rank}}{8bits/_{load}} \times 2rank$$

4 loads can be:

$$\frac{32bits/_{rank}}{8bits/_{load}} \times 1rank \quad \text{or} \quad \frac{32bits/_{rank}}{16bits/_{load}} \times 2ranks$$

2 loads would be:

$$\frac{32bits/_{rank}}{16bits/_{load}} \times 1rank$$

E6XX supports 8 loads,4 loads and 2 loads. Refer to PDG section 4.4 for configurations.

File locations

The Intel® Atom™ Processor E6xx Series Chipset Microcode, additional drivers & documentation can be found on the Intel® Embedded design center website under:

http://www.intel.com/p/en_US/embedded/hwsw/hardware/atom-e6xx/software