Technologies for Future Vertex and Tracking Detectors at CLIC

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Abstract

CLIC is a proposed linear e^+e^- collider with center-of-mass energies of up to 3 TeV. Its main objectives are precise top quark and Higgs boson measurements, as well as searches for Beyond Standard Model physics. To meet the physics goals, the vertex and tracking detectors require not only a spatial resolution of a few micrometers and a very low material budget, but also timing capabilities with a precision of a few nanoseconds to allow suppression of beam-induced backgrounds.

Different technologies using hybrid silicon detectors are explored for the vertex detectors, such as dedicated readout ASICs, small-pitch active edge sensors as well as capacitively coupled High-Voltage CMOS sensors. Monolithic sensors are considered as an option for the tracking detector, and a prototype using a CMOS process with a high-resistivity epitaxial layer is being designed. Different designs using a silicon-on-insulator process are under investigation for both vertex and tracking detector.

All prototypes are evaluated in laboratory and beam tests, and newly developed simulation tools combining Geant4 and TCAD are used to assess and optimize their performance. This contribution gives an overview of the R&D program for the CLIC vertex and tracking detectors, highlighting new results from the prototypes.

Keywords: CLIC, Silicon Detectors, HR-CMOS, HV-CMOS, Allpix Squared

1. Introduction

The Compact Linear Collider (CLIC) [1, 2] is a proposed linear e^+e^- collider to be built at CERN, Geneva, Switzerland. It uses a novel two-beam acceleration scheme achieving field gradients of more than $100 \, \mathrm{MV \, m^{-1}}$, which enables the design of a compact accelerator. The construction is foreseen in three stages with center-of-mass energies of 380 GeV, 1.5 TeV and 3 TeV, each with a different physics focus ranging from precision measurements of the Higgs boson and Top quark to exotica and beyond the Standard Model physics.

The design of the vertex and tracking detectors is strongly influenced by the beam structure at CLIC. Trains of 312 bunches with a bunch spacing of 0.5 ns are repeated with a frequency of 50 Hz. To obtain luminosities of up to $5.9 \times 10^{34} \, \mathrm{cm^{-2} \, s^{-1}}$, the bunches are focused to a size of a few nanometers at the interaction point. The resulting high bunch density leads to interactions between colliding bunches which create background particles. At the highest collision energy, about 100 particles per bunch crossing are expected within the acceptance of the tracking systems, leading to pixel occupancies of up to 3% per bunch train in the innermost layers. Timing information is required to reduce the effect of these pile-up hits on the reconstruction.

The current model for a detector at CLIC [3] features an all-silicon vertex and tracking system with very stringent requirements on resolution and material budget. To limit multiple scattering, the material budget is limited to about 0.2% X_0 per vertex detector layer and 1% X_0 per layer of the tracking detector. A low power consumption of below $50 \, \mathrm{mW \, cm^{-2}}$ in the vertex detector is required in order to enable passive air-flow cooling.

Single-point resolutions of about 3 μm in the vertex and 7 μm in the tracking detector are required for optimal flavor tagging and track reconstruction performance. To allow efficient reduction of background, time stamping capabilities with a precision of about 5 ns are required.

The CLIC vertex and tracking detectors thus need to achieve an order of magnitude reduction both in material budget and cell size, while maintaining a similar hit-time resolution, compared to the current LHC detectors.

2. Silicon Technologies

A variety of silicon technologies are currently explored in order to find the best match with the requirements for a detector at CLIC. This section provides a brief overview of the considered technologies and showcases the investigated prototypes.

2.1. Hybrid Pixel Detectors

Hybrid detectors represent the traditional design of silicon pixel detectors in high-energy physics and consist of two independent parts: the high-resistivity sensor and the CMOS readout chip. The connection between the individual channels is established by solder bumps. With this design, extensive functionality can be placed in the pixels of the readout chip, while the sensor can be fully depleted to maximize charge collection.

Pixel cell sizes of 25 μm – 250 μm have been achieved, but the bump bonding process is both the main cost driver and the limiting factor for the pixel pitch and the device thickness.
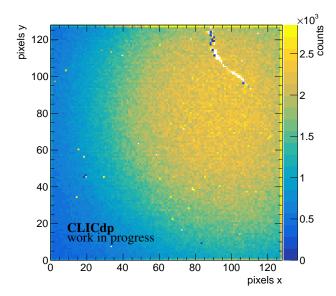
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Figure 1: Sr-90 measurement of a CLICpix2 prototype bonded to a planar sensor with 130 μm thickness. A notch can be observed in the top-right corner, where 55 bumps were lost when lifting the chip from the tape. The isolated unresponsive pixels have been identified as dead channels of the readout ASIC.

The *CLICpix2* prototype [4] is a readout ASIC designed to meet the requirements for the CLIC vertex detector. It features a 128 × 128 pixel matrix with a total active area of 3.2 mm × 3.2 mm, implemented in a 65 nm CMOS process with a pixel pitch of 25 μm x 25 μm. The pixel cells feature simultaneous measurement of the charge and time-of-arrival. The data acquisition is shutter-based, and the pixel matrix can be powered down between shutters.

Promising results have been achieved recently for single-chip bump bonding using a support wafer process with SnAg bumps, which is a challenge at the pixel pitch of 25 μm, due to the requirements on the diameter and uniformity of the solder balls and on the alignment precision. Figure 1 shows a Sr-90 source measurement of a *CLICpix2* prototype bonded to a planar silicon sensor, indicating a high bump yield of more than 99.6 %. The prototype has been successfully tested in laboratory and beam tests, its detailed characterization is still ongoing.

2.2. Monolithic High-Voltage CMOS Sensors

In monolithic High-Voltage (HV) CMOS sensors, electronics and sensor are placed on the same wafer [5]. This facilitates fully integrated designs comprising amplification as well as discrimination and readout, which feature lower mass and do not require bump bonding. The readout electronics is surrounded by a deep collection diode which also acts as shield from the electric field in the sensor bulk. By this, higher bias voltages of about 60 V can be applied to increase the depleted volume. The large collection diode however entails a large input capacitance.

For the CLIC tracking detector, the *ATLASpix_Simple* prototype [6] is being investigated. This fully integrated chip designed for the ATLAS ITk upgrade has been produced in an
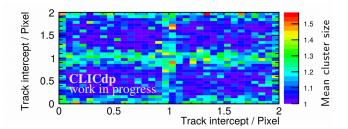

Figure 2: Mean cluster size as a function of the incidence position of the particle for the *ATLASpix_Simple* prototype. Here, tracks from the full pixel matrix are plotted with respect to their relative position within a 2 × 2 pixel area.

AMS 180 nm HV-CMOS process with substrate resistivities of $20 - 1000\,\Omega\,\text{cm}$. The chip has 25 x 400 pixels with a pitch of 130 μm x 40 μm and features in-pixel charge amplifier and discriminators, while the charge and arrival time measurement is performed in the periphery. Promising results have been achieved in first beam tests. Figure 2 shows the mean cluster size as a function of the particle position within a 2 × 2 pixel area. The expected charge sharing is clearly visible at the boundaries between pixel cells, where the mean cluster size increases while staying close to one inside the individual pixels. A position resolution of 13 μm has been reached, the efficiency of 99.5 % has been measured at a charge threshold of 1500 e.

The prototype is currently being integrated into the CaRIBou DAQ system [7] which allows to characterize the timing performance and provides the capacity to record data at higher rates.

2.3. Monolithic High-Resistivity CMOS Sensors

Monolithic High-Resistivity (HR) CMOS sensors represent an alternative to HV-CMOS sensors. Here, the electronics is placed outside the charge-collection diode and is separately shielded. Depletion is achieved by using a high-resistivity substrate and a lower bias voltage, and no dedicated high-voltage design rules by the foundry have to be taken into account. The small collection diode reduces the input capacitance and thus reduces the noise. Recent process modifications allow full lateral depletion [8].

The *Investigator* chip designed by the ALICE collaboration has been used to evaluate this technology in view of the CLIC tracking detector. The chip is an analog prototype, where the digitization of the signals is performed off-chip in the data acquisition system. Two variants of a TowerJazz 180 nm HR-CMOS process have been investigated and resolutions of 4 μm in space and 5 ns in time have been measured for a pitch of 28 μm × 28 μm [9].

A prototype of a fully integrated sensor dedicated to the CLIC tracking detector, *CLICTD*, is currently being designed in this technology exploiting the very low noise and minimum detection threshold. Given the excellent achievable resolution, this technology is also of interest for the CLIC vertex detector.

2.4. Monolithic Silicon-on-Insulator Sensors

Another option to isolate the sensitive CMOS electronics from the high-field region in the sensor is the silicon-on-insulator (SOI) approach, where the electronics is separated
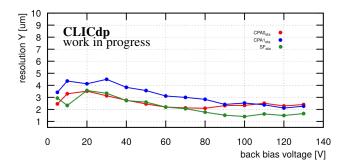
Figure 3: Position resolution of the SOI test chip as a function of the applied back bias voltage. The three data sets correspond to the different pixel circuit designs, two with a charge pre-amplifier (CPA) and one source follower (SF) design.
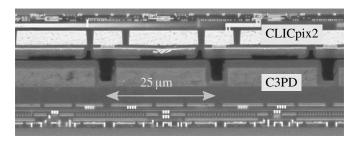

Figure 4: Cross-section of a glue assembly with *CLICpix2* and *C3PD* with a pixel pitch of 25 μm.

by an insulation oxide layer from the sensor on a single high-resistivity wafer.

To evaluate this technology, an SOI test chip has been manufactured in a LAPIS 200 nm SOI process [10]. It combines different parameters on a single chip, such as different pixel pitches as well as different amplification and readout schemes. First test beam results for a sensor with a thickness of 500 μm and a pitch of 30 μm × 30 μm show an excellent position resolution of about 2 μm as indicated in Figure 3.

Analysis of prototype test beam data is ongoing, and a dedicated prototype chip for the CLIC vertex detector, *CLIPS*, has been designed and is currently in production.

2.5. Capacitively Coupled Detectors

In order to overcome the limitations of bump bonding in traditional hybrid detectors, capacitively coupled hybrids are being investigated, where an active HV-CMOS sensor with analog signal amplification is glued to a CMOS readout chip and the amplified signal coupled capacitively through the glue layer.

This approach permits using the full feature set of standard CMOS processes for the readout chip while keeping the required circuitry in the HV-CMOS chip to a minimum. Investigations have shown that precise alignment and uniform glue dispensation are key to a good assembly performance.

CLICpix2 prototypes have been glued to *C3PD* sensors [11], a second-generation active sensor designed in an AMS 180 nm HV-CMOS process with a matching pixel pitch of 25 μm × 25 μm. A cross-section of such an assembly is shown in Figure 4. First test beam measurements show a temporal and

spatial resolution of approximately 7 ns and 8 μm, respectively. Extensive simulations of the sensor using TCAD [12] and of the capacitive coupling via finite-element analysis [13] have been conducted for comparison with the measured performance.

Further assemblies with high-resistivity substrate sensors are under investigation, and the gluing process is being optimized further.

2.6. Enhanced Lateral Drift Detectors

A novel sensor concept explored for the CLIC vertex detector are Enhanced Lateral Drift (ELAD) sensors [14], which are an attempt to break the paradigm of ever-decreasing pixel pitch. In thin sensors, the position resolution is limited to $p/\sqrt{12}$, where p is the pixel pitch, since almost no charge sharing takes place.

By introducing additional deep implants in the sensor bulk, the electric field is altered such that the lateral spread of charge carriers is increased during their drift. The implants are designed in a way that the resulting charge sharing is close to the theoretical optimum of a linear charge distribution. Challenges to overcome for this type of sensor are the complex production process and the exact placement of the implants to avoid low-field regions and the resulting recombination of charge carriers.

This sensor design performs very well in finite-element device simulation, and a first production batch with test structures as well as sensors with 55 μm pitch is expected still in 2018.

3. Simulation Tools

Advanced simulation tools help in understanding the performance of new prototypes and to optimize the design of new detectors. The Monte-Carlo approach is widely used to account for the stochastic nature of the processes under investigation, and a new software framework has been developed to combine this with information obtained from detailed device modeling.

The Allpix Squared silicon detector simulation framework [15] combines the detailed description of particle interactions provided by Geant4 [16–18] with electric fields simulated using TCAD, and implements fast algorithms for charge carrier propagation in silicon as well as front-end electronics simulations. It provides access to the main detector characteristics such as position resolution, charge collection efficiency, or tracking efficiency.

The simulation framework has been validated using test beam data, and very good agreement between data and simulation has been found. An example is shown in Figure 5, comparing the cluster size distribution of a 50 μm thick planar silicon sensor as simulated and measured in test beam data.

The software sees continuous development and a new feature version has recently been released [19]. Among other improvements, it adds support of magnetic fields and Lorentz drift, new particle source types and the possibility to record particle tracks as Monte Carlo truth information.

Currently, a detailed transient simulation using weighting fields is under development with the goal to better model the timing behavior of silicon detectors.
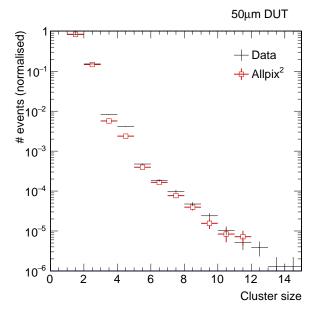
50μm DUT

Figure 5: Comparison of the cluster size distribution from test beam measurements with a 50 μm thick planar silicon sensor and a simulation of the device using Allpix Squared. Figure taken from [15].

4. Summary and Outlook

The beam conditions and physics goals at the proposed CLIC linear e^+e^- collider pose challenges to the vertex and tracking detectors. An excellent spatial and temporal resolution is required while maintaining a minimum material budget and power consumption.

A comprehensive R&D program is underway to qualify silicon technologies for the vertex and tracking detectors at CLIC. Many different concepts are being investigated and most initial requirements have been shown to be achievable. However, the desired position resolution of 3 μm in the vertex detector remains a challenge, and prototypes fulfilling the full set of requirements are yet to be built.

A dedicated prototype using the HR-CMOS technology is currently being designed. Productions of the SOI technology prototype as well as the first ELAD silicon sensor are ongoing.

New and validated simulation tools combining precise device modeling and the Monte-Carlo approach ease the R&D and prototyping processes.

5. Acknowledgements

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