CPU & Clock

File: CPU.kicad_sch

Input/Output

File: InpOutp.kicad_sch

Memory – RAM/ROM

File: Memory.kicad_sch

Revisions:

1.0–000 –> 000A:
  1/18/2021: Sullins cartridge connector is not designed as row_first, so the footprint has to be flipped in order to work. Also added input power filtering and large filter cap.
  1/20/2021: Added cassette output header for future cassette use.
  1/23/2021: Added additional power input filtering; fixed power bus on clock oscillator pull–ups.

1.0–001 –> 1.1–001
  1/1/2022: Updated/compared to 251027–01D. Rearranged LS245 signal orderings.

1.1–001 –> 1.1–002
  4/24/2022: Updated/compared to 251027–01D. Discovered that a transcription error was introduced on the 6116 R/W pin. Moved to VR/W. Screen is better, but not perfect so swapped char ROM and now it's perfect. Seemingly there is corrpution in the ROM I was using.

1.1–002 –> 1.1–002A/B
  5/3/2022: Minor changes. B version adds card edge for User Port.

1.1–002B –> 1.1–002C
  5/7/2022: Realigned top and right side connectors/switches to match measurements in the prototype; added second header for user port.

1.1–002C –> 1.1–002D
  5/14/22: removed ground trace round VIC to improve routing. Added spot for a Polyfuse in case of using external keyboard encoder, and a main system fuse.

NOTE: Commodore used some very odd schematic/board revision references and it's hard to determine which is which. This redraw is shown as sub–version "C" but is referenced elsewhere as the "Revision N" schematic. They are drawn consistent with this (i.e., three schematic pages with the same parts on each).

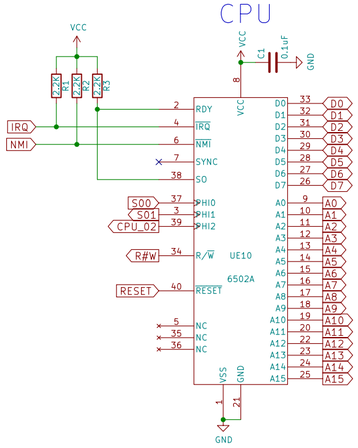
ECO 830151 4/12/83
Transcribed from CBM VIC–20cr schematics 251027–01D
Steve J. Gray and Rich Cini

Sheet: /
File: VIC20Reloaded–1.1–002.kicad_sch

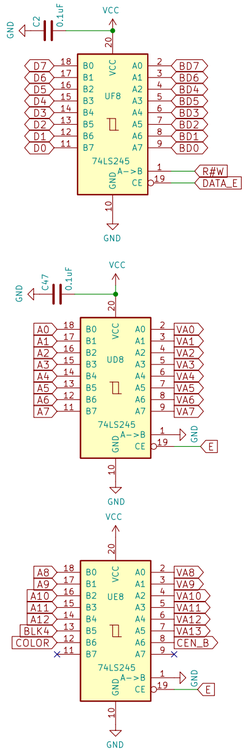
Title: VIC RELOADED

Size: USLetter	Date: 2022–05–14	**Rev: 1.1–002D**
KiCad E.D.A. kicad (6.0.4–0)		Id: 1/4

CPU

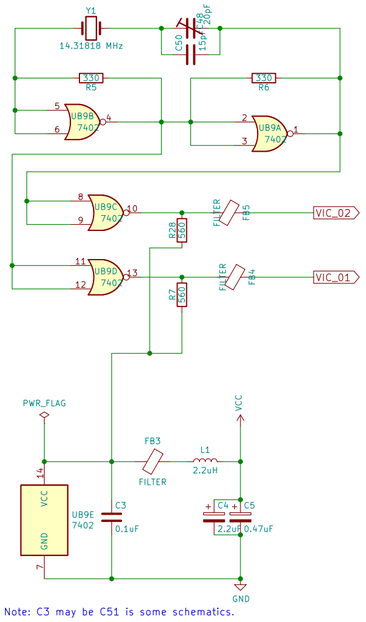


DATA BUFFER



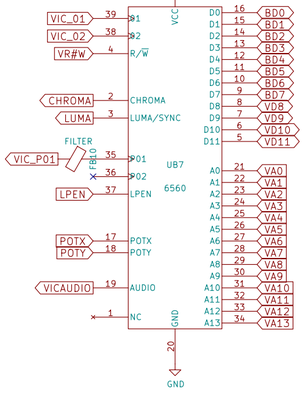
ADDRESS BUFFERS

CLOCK

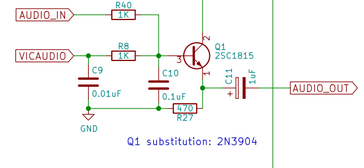


Note: C3 may be C51 is some schematics.
Some schematics have R7/R28 as 220 ohm. Can put a 360 ohm resistor in parallel for testing purposes.

VIC-I
$9000-900F



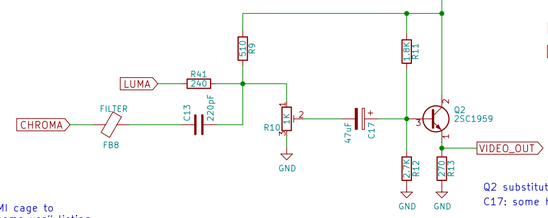
AUDIO



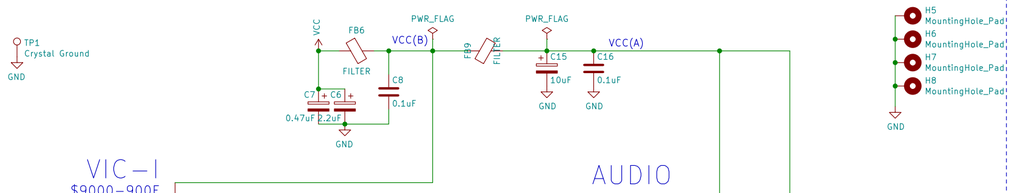
Q1 substitution: 2N3904

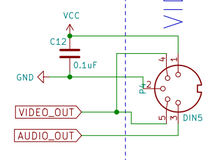
Sometimes listed as FB7

VIDEO



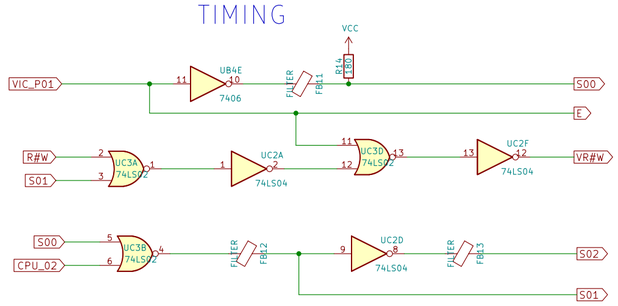
Q2 substitution: 2N2222
C17: some have 10uF



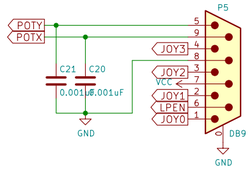


VIDEO/AUDIO PORT

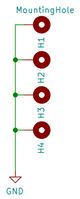
TIMING



CONTROLLER PORT



MountingHole

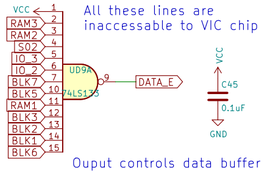


Design Note
==========

Commodore used LS245 octal bus transceivers set to one direction rather than LS244 octal buffer/line drivers (which are grouped in nibbles). The schematic had the "A" and "B" sides backwards when considering the direction pin 1. Later designs corrected this and changed the A-> B orientation.

Signals have been re-ordered from the original.

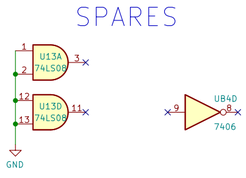
NOTE: VIC uses upper Address lines as a chip select. BLK4 used as CS for VIC E (pin 19): 0=CPU Access, 1=VIC Access

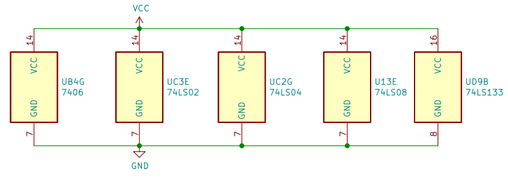


All these lines are inaccessable to VIC chip

Ouput controls data buffer

SPARES



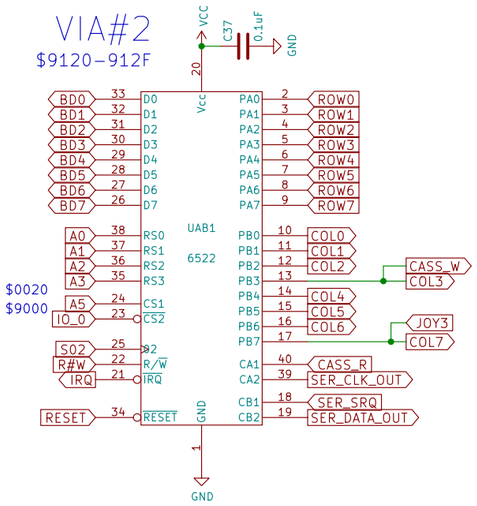


ECO 830151 4/12/83
Transcribed from CBM VIC-20cr schematics 251027-01D
Steve J. Gray and Rich Cini
Sheet: /CPU & Clock/
File: CPU.kicad_sch

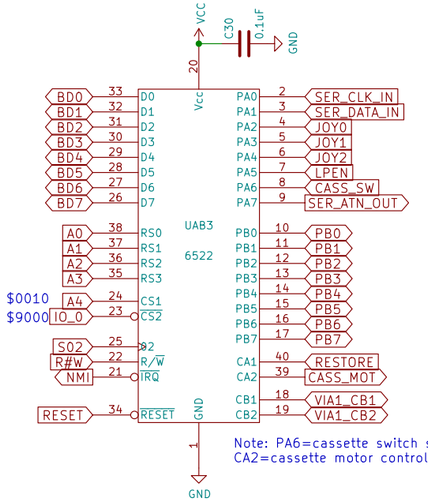
Title: VIC RELOADED

Size: C	Date: 2022-05-14	**Rev: 1.1-002D**
KiCad E.D.A. kicad (6.0.4-0)		Id: 2/4

VIA#2
$9120-912F

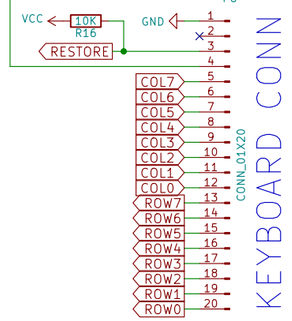


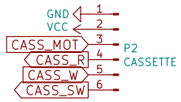
VIA#1
$9110-911F



Note: PA6=cassette switch sense.
CA2=cassette motor control.

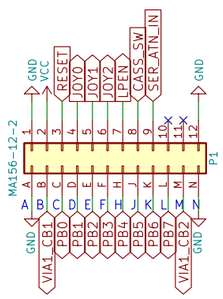
F1
Polyfuse 0.25A
VCC





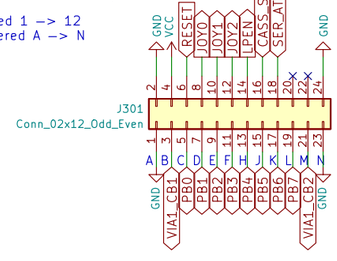
Note: CASS_MOT is a logic-level control signal. To use with a cassette deck, an external control circuit will be needed.

USER PORT

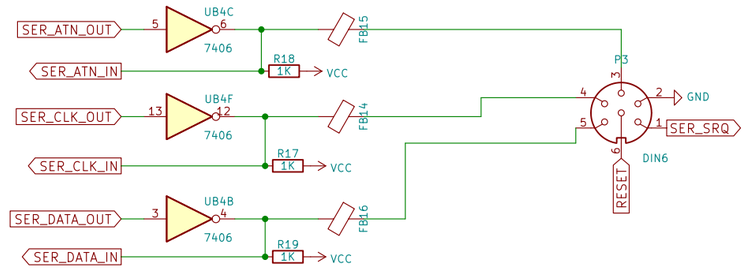


Note: Pins 10/11 were connected to 9VAC from the power input socket. Frankly I thought it was odd to have 9VAC at the user port.

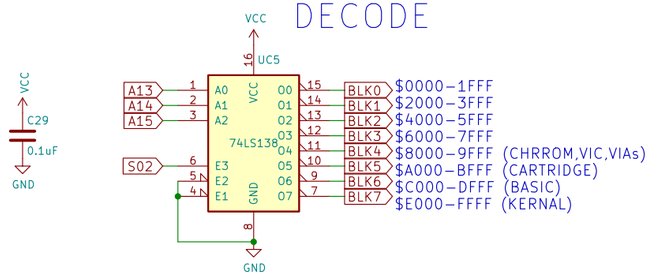
TOP is numbered 1 -> 12
BOTTOM is lettered A -> N



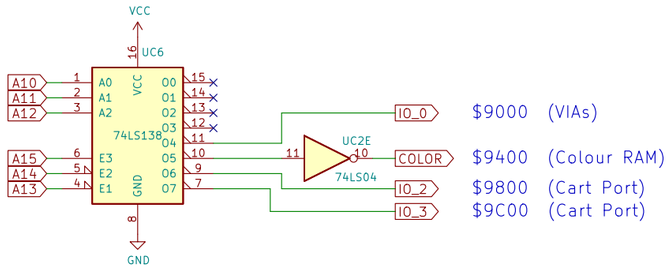
IEC PORT



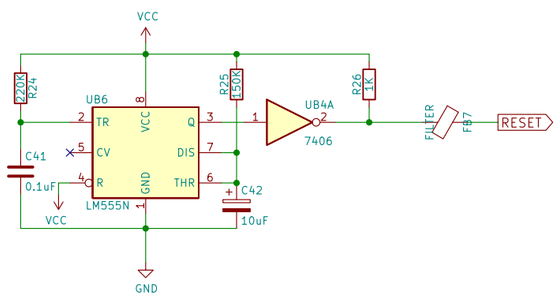
DECODE

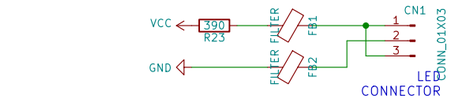


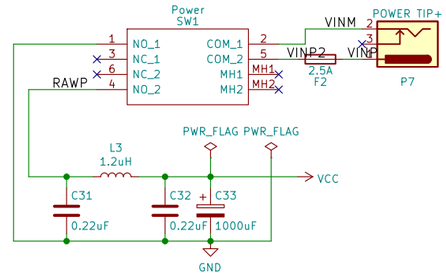
A15 14 13 12 11 10 > ADDR
100 000 > $8000 > 0
100 001 > $8400 > 1
100 010 > $8800 > 2
100 011 > $8C00 > 3
100 100 > $9000 > 4
100 101 > $9400 > 5
100 110 > $9800 > 6
100 111 > $9C00 > 7

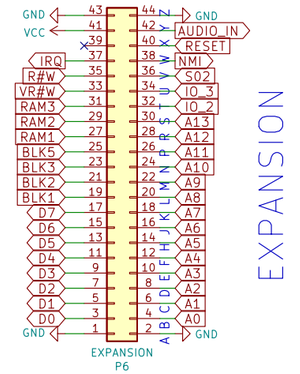


RESET









Cartridge is about 6" wide with the plastic or 5.25" without.

Note: On the prototype, pin Y is listed as NC.
Edac 337-044-520-202 or -558-201 (R/A)
Sullins EBM22DRXH or DRAS (R/A) but row pitch is 0.156" rather than 0.200"

ECO 830151 4/12/83
Transcribed from CBM VIC-20cr schematics 251027-01D
Steve J. Gray and Rich Cini

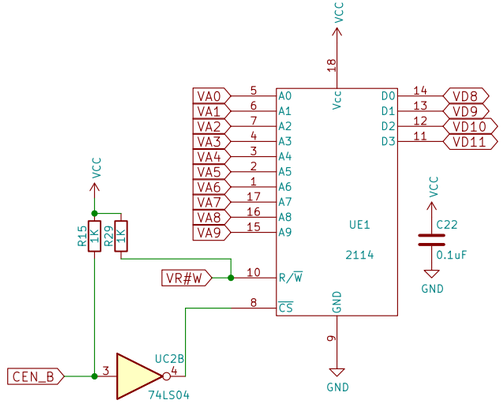
Sheet: /Input/Output/
File: InpOutp.kicad_sch

Title: VIC RELOADED

Size: B	Date: 2022-05-14	**Rev: 1.1-002D**
KiCad E.D.A. kicad (6.0.4-0)		Id: 3/4

COLOR RAM

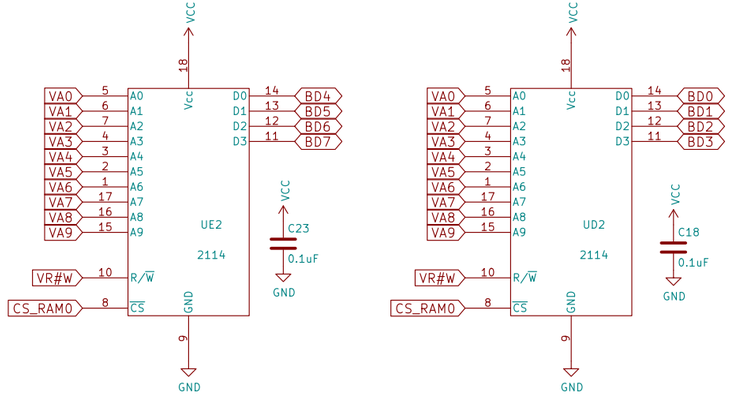
$9600–97FF



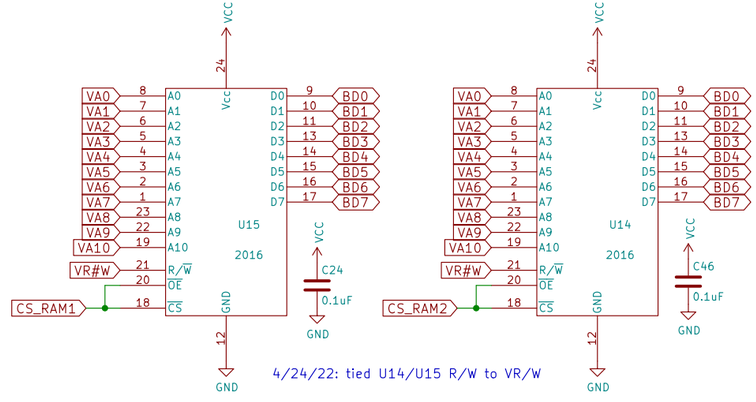
Some schematics show R29 at 470 ohms. Add 890 ohm in parallel to 1k for testing.

RAM — $0000 — $03FF

Note: On the prototype, the 2114 data pins are drawn backwards.
D0–>D3 is 11–>14

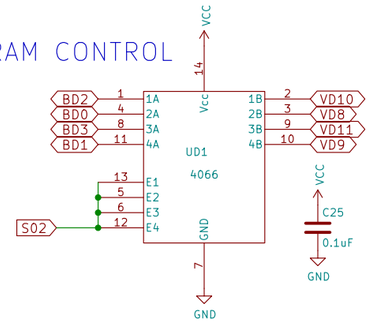


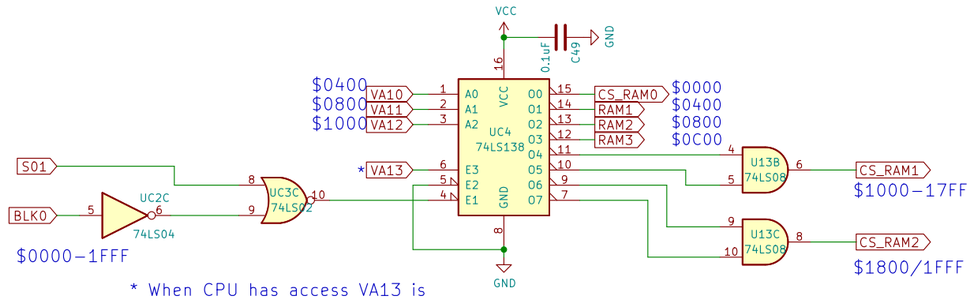
RAM — $1000 — $1FFF



4/24/22: tied U14/U15 R/W to VR/W

COLOR RAM CONTROL





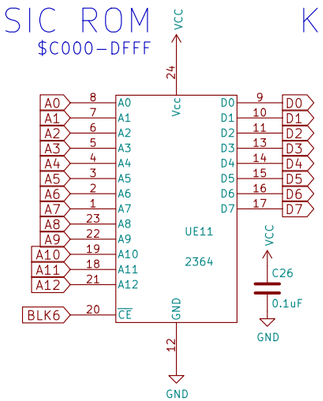
* When CPU has access VA13 is substituted with BLK4 line.

4/24/22: Newly–discovered prototype of a VIC20CR had eight 6116 (2kx8) RAM chips in addition to the original three 2114AL (1kx4) chips. This configuration would fill BLK1 (8k) and only part of BLK2 (4K) because two would have been used for the CS_RAM1 and CS_RAM2 blocks above. It would seem that the decoding may still leave out the area occupied by the SuperExpander so that it can still be used. The SuperExpander contained six 2114AL chips mapped to RAM1, RAM2, and RAM3, and also using VR/W. Not sure the RAM could be disabled in the SuperExpander.

This was called a "16k VIC–20"

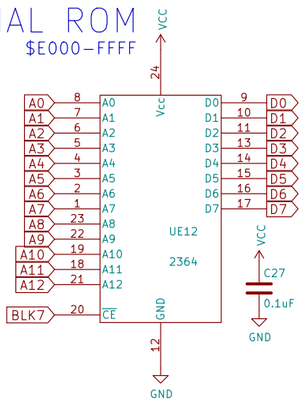
BASIC ROM

$C000–DFFF



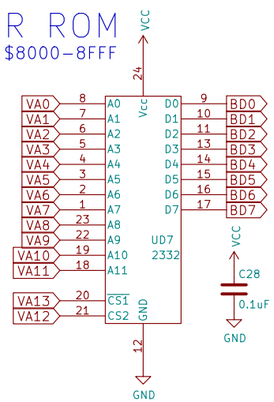
KERNAL ROM

$E000–FFFF



CHR ROM

$8000–8FFF



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Sheet: /Memory – RAM/ROM/
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Title: VIC RELOADED

Size: B	Date: 2022–05–14	**Rev: 1.1–002D**
KiCad E.D.A. kicad (6.0.4–0)		Id: 4/4