1. Overview

GN1621 is a 128-dot matrix memory-mapped multifunctional LCD driver circuit. The S/W structure of GN1621 makes it suitable for dot matrix LCD display, including LCD module and display subsystem, GN1621 also has power saving function. Its main features are as follows: **l**

Working voltage: 2.4Vÿ5.5V **l** Internal 256kHz RC oscillator **l** External 32kHz crystal oscillator or 256kHz frequency input **l** Optional 1/2 or 1/3 bias and 1/2, 1/3 or 1 /4 duty cycle LCD display

lInternal time base frequency source

l Buzzer drive signal frequency can be selected 2kHz or 4kHz

l Has a shutdown command to reduce power consumption **l** Internal time base generator and WDT watchdog timer

l Internal time base or WDT overflow output

l Eight clock sources of time base/WDT clock

l 32×4 LCD driver

lInternal 32×4bit display RAM

l Four-way serial interface **l** Internal LCD drive frequency source

l Available commands to control operation **l** Data mode and command mode command **l** R/W address automatic accumulation **l** Three data access modes **l** VLCD pin is used to adjust LCD working voltage **l** Working environment temperature: -40~85ÿ **l** Package type: SOP16 /SOP24/SSOP24/SOP28/QFP44/SSOP48/LQFP48 **l** The packaging specifications are as follows (the following packages are recommended):

l GN1621 SSOP48 30PCS/tube 80 tubes/box 2400PCS/box 24000PCS/box (plastic package size: 15.9mm×7.5mm pin spacing: 0.635mm) **l** GN1621C SOP28 25PCS/tube 80 tubes/box 2000PCS/box 20000PCS/box (plastic package Size: 17.9mm×7.5mm pin pitch: 1.27mm) **l** GN1621B QFP44 96PCS/board 10 boards/box 960PCS/box 5760PCS/box (plastic package size: 10.0mm×10.0mm pin pitch: 0.8mm) **l** GN1621DT SSOP24 60PCS/tube 160 tubes/box 9600PCS/box 96000PCS/box (plastic package size: 8.7mm×3.9mm pin spacing: 0.635mm) **l** GN1621CB SSOP48 30PCS/tube 80 tubes/box 2400PCS/box 24000PCS/box (plastic package size : 15.9mm×7.5mm pin pitch: 0.635mm)

If there is any change, please refer to the actual situation.

2. Functional block diagram and pin description

2.1. Functional block diagram

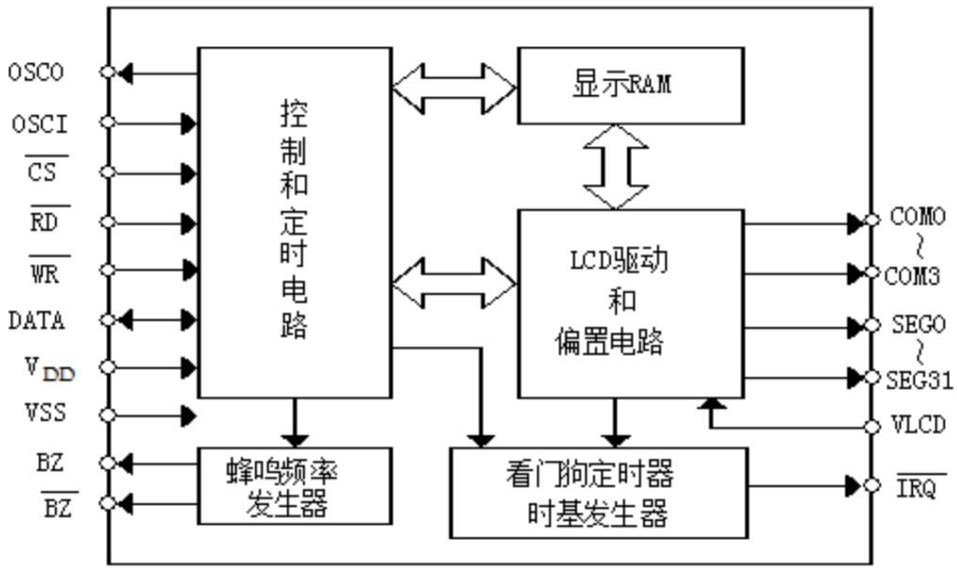


Figure 1 Functional block diagram

Note:

[1] CS : Chip Select

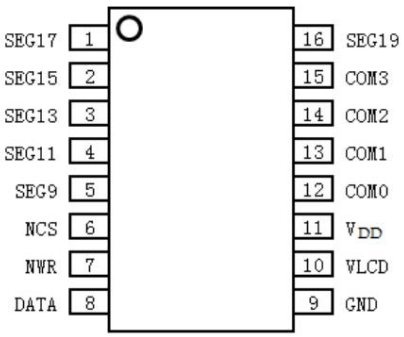
[2] BZ, BZ : Buzzer output

[3] WR、RD、DATA: serial interface

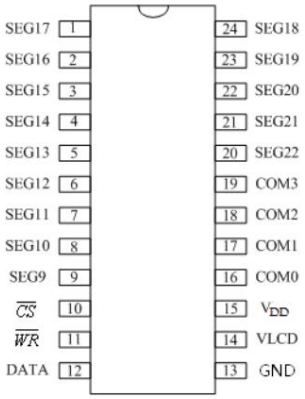
[4] COM0~COM3, SEG0~SEG31: LCD output

[5] IRQ— : Time base or WDT overflow output

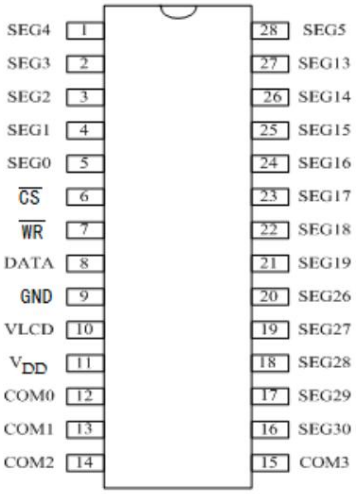
2.2. Pin arrangement diagram



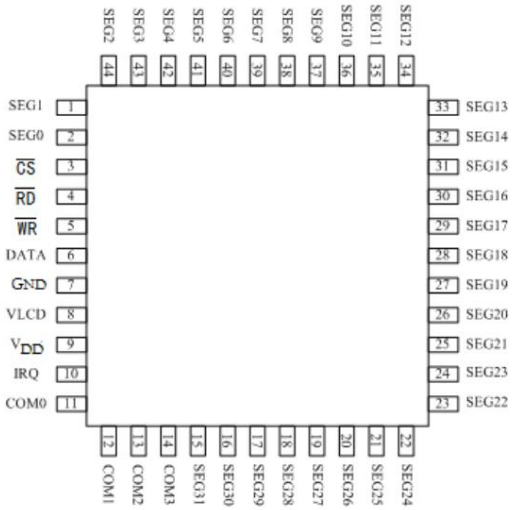
SOP16



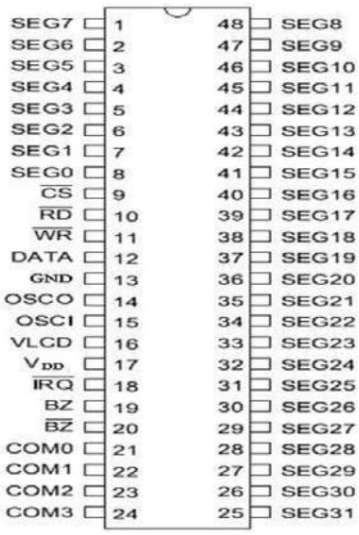
SOP24/SSOP24



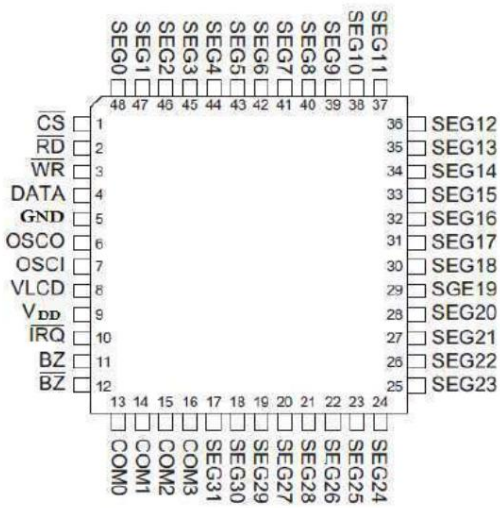
SOP28



QFP44



SSOP48



LQFP48

2.3. Pin description

serial number						Name I/O		Function Description
SOP16	SOP24/ SSOP24	SOP28	QFP44	SSOP48	LQFP48			
6	10	6	3	9	1	CS	I	Chip select signal input terminal (with pull-up resistor). CS for When logic high, data and commands cannot be read and written, and the serial interface circuit is reset. but when When CS is logic low level, the controller and GN1621 Data and commands can be transferred between them.
— — —	4			10	2	RD	I	READ clock input (with pull-up resistor). RAM The data in the RD The falling edge of the signal is output to the DATA line, the host controller can rise on the next edge to latch this data.
7	11	7	5	11	3	WR I		Write clock input (with pull-up resistor). signal at WR The rising edge of the DATA line is latched into the GN1621ÿ
8	12	8	6	12	4	DATA I/O		Serial data input/output (with pull-up resistor).
9	13	9	7	13	5	GND P		negative supply, ground
-	— — —	14			6	OSCO O		The OSCI and OSCO ports are connected to a 32.768KHz crystal oscillator, used to generate system clock. If the external system clock is connected, it will pass through the OSCI terminal. If using the on-chip RC oscillator, OSCI and OSCO can be left floating.
-	— — —	15			7	GO	I	
10	14	10	8	16	8	VLCD I		LCD power input
11	15	11	9	17	9	VDD	P	Positive power supply
-	— —	10		18	10	IRQ O		Time base or WDT overflow flag, NMOS open drain output.
-	— — —	19			11	BZ	O	Buzzer output
-	— — —	20			12	BZ	O	Buzzer output
12	16	12	11	21	13	COM0 O		LCD COM output terminal
13	17	13	12	22	14	COM1 O		LCD COM output terminal
14	18	14	13	23	15	COM2 O		LCD COM output terminal
15	19	15	14	24	16	COM3 O		LCD COM output terminal
-		—	15	25	17	SEG31 O		SEG output of LCD
— —	16		16	26	18	SEG30		SEG output of LCD
— —	17		17	27	19	SEG29 O		SEG output of LCD
— —	18		18	28	20	SEG28 O		SEG output of LCD
— —	19		19	29	21	SEG27 O		SEG output of LCD
— —	20		20	30	22	SEG26 O		SEG output of LCD
-		—	21	31	23	SEG25 O		SEG output of LCD

— — — 22				32	24	SEG24 O	SEG output of LCD
— — — 24				33	25	SEG23 O	SEG output of LCD
— 20 — 23				34	26	SEG22 O	SEG output of LCD
— 21 — 25				35	27	SEG21 O	SEG output of LCD
— 22 — 26				36	28	SEG20	SEG output of LCD
16	23	21	27	37	29	SEG19 O	SEG output of LCD
— 24		22	28	38	30	SEG18	SEG output of LCD
1	1	23	29	39	31	SEG17 O	SEG output of LCD
— 2		24	30	40	32	SEG16 O	SEG output of LCD
2	3	25	31	41	33	SEG15	SEG output of LCD
— 4		26	32	42	34	SEG14 O	SEG output of LCD
3	5	27	33	43	35	SEG13 Oh	SEG output of LCD
— 6 — 34				44	36	SEG12 O	SEG output of LCD
4	7 — 35			45	37	SEG11	SEG output of LCD
— 8 — 36				46	38	SEG10 O	SEG output of LCD
5	9 — 37			47	39	SEG9 O	SEG output of LCD
— — — 38				48	40	SEG8 O	SEG output of LCD
— — — 39				1	41	SEG7 O	SEG output of LCD
— — — 40				2	42	SEG6 OR	SEG output of LCD
— — 28			41	3	43	SEG5 O	SEG output of LCD
— — 1			42	4	44	SEG4 O	SEG output of LCD
— — 2			43	5	45	SEG3 O	SEG output of LCD
— — 3			44	6	46	SEG2 O	SEG output of LCD
— — 4			1	7	47	SEG1 O	SEG output of LCD
— — 5			2	8	48	SEG0 O	SEG output of LCD

3. Electrical characteristics

3.1. Limit parameters

(Tamb=25ÿ unless otherwise specified)

Parameter Name Symbol	condition	rated value	unit
Power Voltage VDD	-	-0.3ÿ7	IN
Input Voltage VIN	-	GND-0.3ÿVDD+0.3	IN
Storage Temperature	-	-50ÿ125	ÿ
Tstg Working	-	-40ÿ85	ÿ
Temperature Tamb Welding Temperature TL	10 seconds	250	ÿ

3.2. Electrical characteristics

3.2.1. DC parameters

(Unless otherwise specified, Tamb=25ÿ, GND=0V)

Parameter Name Symbol		Test Conditions		Min Typical Max Unit			
Operating Voltage	VDD	-		2.4 — 5.5 V			
Working current	IDD1	no load On-chip RC oscillator	VDD=3V — 150			300	uA
			VDD=5V — 300			600	uA
	IDD2	no load crystal oscillator	VDD=3V — 60			120	uA
			VDD=5V — 120			240	uA
	IDD3	no load external clock	VDD=3V — 100 VDD=5V —			200	uA
			200 VDD=3V — 0.1 VDD=5V			400	uA
stand-by current	ISTB	no load shutdown mode	— 0.3 VDD=3V VDD=5V			5	uA
			VDD=3V VDD=5V VDD=3V			10	uA
Input low level VIL		DATA, WR . CS . RD		0 — 0.6 V			
				0 — 1.0 V			
Input high level VIH	DATA, WR	. CS . RD		2.4 — 3.0 V			
				4.0 — 5.0 V			
DATA, BZ, BZ , IRQ	IOL1	VOL=0.3V		0.5	1.2 — mA		
		VOL=0.5V	VDD=5V	1.3	2.6 — mA		
DATA, BZ, BZ	IOH1	VOH=2.7V	VDD=3V	-0.4	-0.8 — mA		
		VOH=4.5V	VDD=5V	-0.9	-1.8 — mA		
LCD COM port Sink current	IOL2	VOL=0.3V	VDD=3V	80	150 - uA		
		VOL=0.5V	VDD=5V	150	250 - uA		
LCD COM port pull current	IOH2	VOH=2.7V	VDD=3V	-80	-120 - uA		
		VOH=4.5V	VDD=5V	-120	-200 - uA		
SEG terminal of LCD Sink current	IOL3	VOL=0.3V	VDD=3V	60	120 - uA		
		VOL=0.5V	VDD=5V	120	200 - uA		
SEG terminal of LCD pull current	IOH3	VOH=2.7V	VDD=3V	-40	-70 - uA		
		VOH=4.5V	VDD=5V	-70	-100 — uA		
Pull-up resistor	RPH	DATA, WR . CS . RD	VDD=3V	40	80	150 kÿ	
			VDD=5V	30	60	100 kÿ	
Built-in resistor Rvlcd at VLCD		VLCD		— 110 — kÿ			

3.2.2. AC parameters

parameter name	symbol	Test Conditions		Min	Typical	Max	Unit	
system clock	fSYS1	on-chip RC oscillator	VDD=3V	—	256	—	kHz	
			VDD=5V	—	256	—	kHz	
	fSYS2	crystal oscillator	VDD=3V	—	32.768	—	kHz	
			VDD=5V	—	32.768	—	kHz	
	fSYS3	external clock	VDD=3V	—	256	—	kHz	
			VDD=5V	—	256	—	kHz	
LCD clock	fLCD	On-chip RC oscillator		—	fSYS1/768	—	Hz	
		Crystal Oscillator - fSYS2/96 - Hz						
		External Clock - fSYS3/768 - Hz						
LCD COM terminal period tCOM		n: COM fraction		—	n/fLCD	—	s	
serial data clock (WR PIN)	fCLK1	Duty cycle 50%	VDD=3V	4	—	150	kHz	
			VDD=5V	4	—	300	kHz	
serial data clock (RD PIN)	fCLK2	Duty cycle 50%	VDD=3V	—	—	75	VDD=5V — — 150	kHz
			kHz					
Buzzer output frequency fTONE		On-chip RC oscillator		—	2.0 or 4.0	—	kHz	
Serial interface reset pulse width (Figure 4)	tCS	CS		—	250	—	ns	
WR RD Input pulse width (figure 2)	tCLK	write mode	VDD=3V	3.34	—	—	us	
		read mode		—	6.67	—	us	
		write mode	VDD=5V	1.67	—	—	us	
		read mode		—	3.34	—	us	
Serial data clock rise/fall time (figure 2)	tr, tf		VDD=3V	—	120	—	ns	
			VDD=5V	—	120	—	ns	
Serial data to WR RD clock The settling time (Figure	tSU		VDD=3V	—	120	—	ns	
			VDD=5V	—	120	—	ns	
3) of serial data to WR RD clock The hold time of the (Figure 3)	th		VDD=3V	—	120	—	ns	
			VDD=5V	—	120	—	ns	
CS to WR RD clock establishment time (Figure 4)	tsul		VDD=3V	—	100	—	ns	
			VDD=5V	—	100	—	ns	
CS to WR RD clock hold time (Figure 4)	th1		VDD=3V	—	100	—	ns	
			VDD=5V	—	100	—	ns	

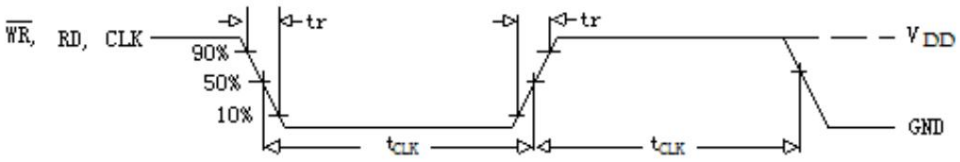


Figure 2 AC parameter timing diagram 1

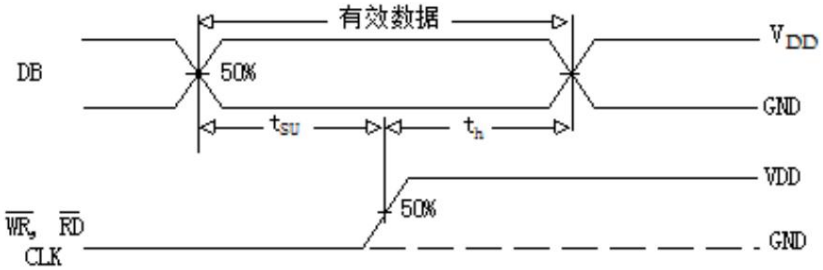


Figure 3 AC parameter timing diagram 2

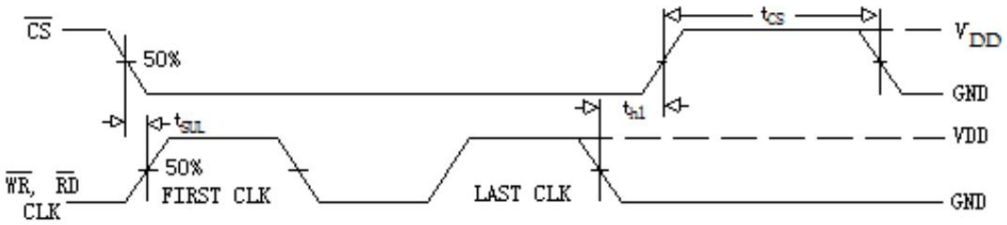


Figure 4 Timing sequence of AC parameters Figure 3

4. Function description

GN1621 is a 32×4 dot-matrix LCD control driver with microcontroller interface and RAM mapping. Power up the circuit

It can be cleared at time, and the working state can be set through the command terminal, and then the RAM data can be read, written,

For modification operation, the contents of RAM correspond to the contents of LCD display driver one by one. The circuit is a dot-matrix LCD drive display, each SEG

The terminals are independent of each other, and it is easy to modify the RAM data, so the content of the displayed dot matrix is flexible and can be customized by the user.

4.1ÿRAM

The static display memory (RAM) has a structure of 32×4 bits and stores the displayed data. The contents of RAM are directly mapped to the contents of the LCD driver. Data in RAM can be accessed by READ, WRITE and READ-MODIFY-WRITE commands. The process of mapping the content in RAM to the LCD structure is shown in the figure below:

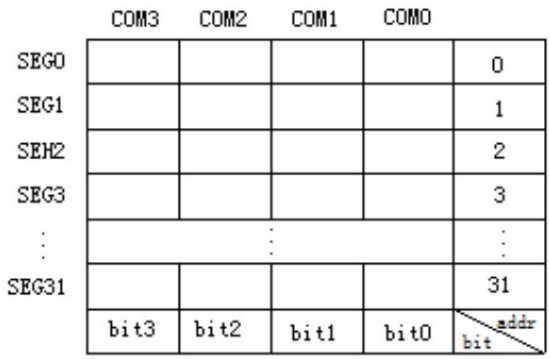


Figure 5 RAM map

4.2. System oscillator

GN1621 system clock is used to generate reference clock/watchdog circuit clock, LCD drive clock and buzzer frequency. The clock can come from on-chip RC oscillator (256kHz), crystal oscillator (32.768kHz) or external 256kHz clock set by S/W. The system oscillator structure is shown in the figure below. After executing the SYS DIS command, the system clock stops and the LCD bias generator also stops working. This command is only applicable to the on-chip RC oscillator (256kHz) and crystal oscillator. Once the system clock is stopped and the LCD display goes dark, the time base/WDT will lose its function.

The LCD OFF command is used to turn off the LCD bias generator. After the LCD OFF command turns off the LCD bias generator, use the SYS DIS command to reduce power consumption, which is equivalent to the system POWER DOWN command. But when an external clock is used as the system clock, the SYS DIS command can neither turn off the oscillator nor enter POWER DOWN mode. A crystal oscillator can be used to connect a 32kHz external frequency source to the OSCI pin. Therefore, the system entering POWER DOWN mode is somewhat similar to the operation of an external 256kHz clock. system initial After power on, GN1621 is in SYS DIS state.

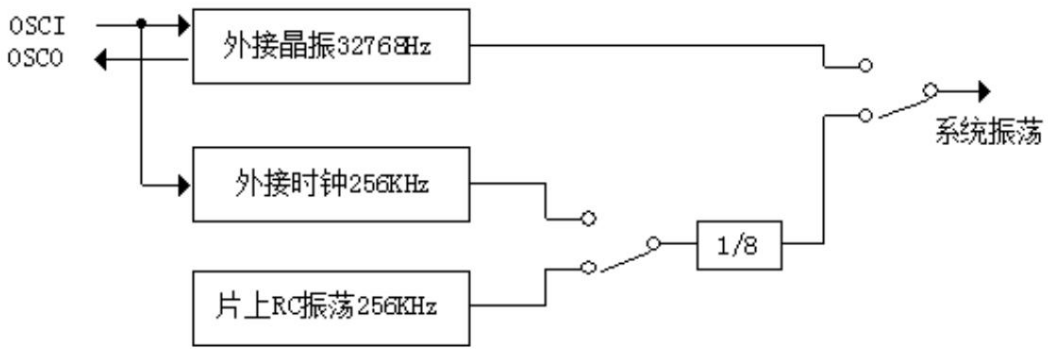


Figure 6 System Oscillator Structure

4.3. Time Base and Watchdog Timer

The time base generator is composed of 8-stage increment counters, which are designed to produce an accurate time base. The Watchdog Timer (WDT) consists of an 8-stage time base generator and a 2-stage up-counter, used to stop the host controller during abnormal conditions (unknown or undesired jumps, execution errors, etc.) or other subsystems. WDT overflow, a WDT overflow flag will be set. time base

The output of the generator and the output of the WDT pause flag can be connected to the IRQ output by command. There are a total of 8 frequencies suitable for the time base generator and WDT clock. Its frequency is obtained by the following formula fWDT=32kHz/2n , the value of n changes between 0 and 7 through commands, and 32kHz in the equation indicates that the system frequency is composed of a 32.76832kHz crystal oscillator and an on-chip oscillator (256kHz) or external 256kHz frequency driver. If an on-chip oscillator (256kHz) or an external 256kHz frequency is used as the system frequency, the system frequency is preset to 32kHz by a 3-stage frequency divider. Since the time base generator and WDT use the same 8-stage counter, the commands related to the time base generator and WDT need to be used with care. For example, calling the WDT DIS command is invalid for the time base generator, while WDT EN is not only applicable to the time base generator but also can activate

Active WDT overflow flag output (WDT overflow flag connected to IRQ pin). After the TIMER EN command is input, the WDT and IRQ pins are disconnected, and the content of the time base generator is cleared by the CLR WDT or CLR TIMER command. The CLR WDT or CLR TIMER command is executed before the WDT EN or TIMER EN command respectively. CLR TIMER command must be executed before WDT mode transition to time base mode. one

Once the WDT overflow mode occurs, the IRQ pin will be logic low until a CLR WDT or IRQ DIS command occurs. After the IRQ output is deasserted, the

The feet will be in levitation. Make the IRQ output active or inactive by executing the IRQ EN or IRQDIS command. IRQ EN enables IRQ

The output of the time base generator or WDT overflow flag is applied to the IRQ pin. The structure of the time base generator and WDT is shown in the figure below:

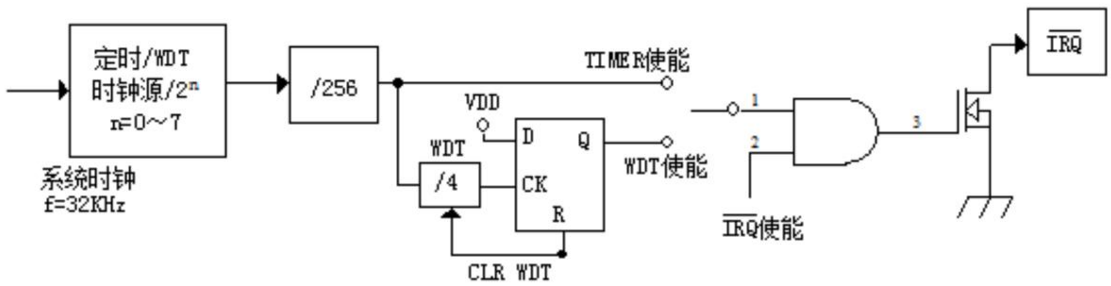


Figure 7 Schematic diagram of the structure of the time base generator and WDT

4.4. Buzz output

A simple buzzer oscillator is provided in GN1621. The buzzer oscillator can provide a pair of buzzer driving signals BZ and BZ for

Produces a simple beep. Executing the TONE4K and TONE2K commands can generate two beep frequencies,

The TONE4K and TONE2K commands set the buzzer frequency to 4kHz and 2kHz respectively, and the buzzer driving signal can call TONE ON or TONE OFF command to turn on or off. BZ and BZ are a pair of anti-phase drive outputs, used to drive the electric buzzer. Once the system fails or the beep input

out of stop, BZ and BZ outputs are at low level.

4.5. LCD driver

GN1621 is a 128 (32×4) dot matrix LCD driver, it can drive 1/2 or 1/3 bias, 2, 3 or 4 LCD display on the COM side, this feature makes GN1621 suitable for a variety of LCD displays. The LCD drive clock is generated from the system Clock, whether the system clock comes from 32.768kHz crystal oscillator frequency or on-chip RC oscillator frequency or external frequency, when LCD driving The frequency of the clock is always 333Hz. See the table below for the commands corresponding to the LCD.

name instruction code		Function
LCD off LCD	10000000010X	to turn off LCD output
on	10000000011X	Turn on the LCD output
BIAS & COM	1000010abXcX	c=0:1/2 bias state c=1:1/3 bias state ab=00: 2COM port ab=01: 3COM port ab=10: 4COM port

The first three digits of the command code 100 indicate the command mode ID, if there are consecutive command mode IDs (except the first command) will be ignored slightly. The LCD OFF command turns off the LCD display by interrupting the LCD bias generator, while the LCD ON command turns off the LCD bias generator by The generator turns on the LCD display. BIAS &COM is a command related to LCD display, through which GN1621 can drive many type of LCD display.

4.6. Instruction format

GN1621 can be set via S/W. There are two modes for setting GN1621 and transmitting LCD display data. For command mode and data mode. The setting of GN1621 is called command mode, its ID is 100, it is controlled by system setting command, system frequency It consists of frequency selection command, LCD setting command, buzzer frequency selection command and operation command. Data schema includes READ, WRITE, and READ-MODIFY-WRITE operations. The following table is the data mode ID and command mode ID:

operate	Mode	**ID**
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND		100

Command Command mode occurs before data and command transfers. If there are consecutive commands, the command mode ID100 will be ignored. When the system works in Discontinuous command or discontinuous address data mode, CSThe pin should be set to 1 and the previous operating mode will be reset. Once CS The pin is 0, a new working mode ID will appear.

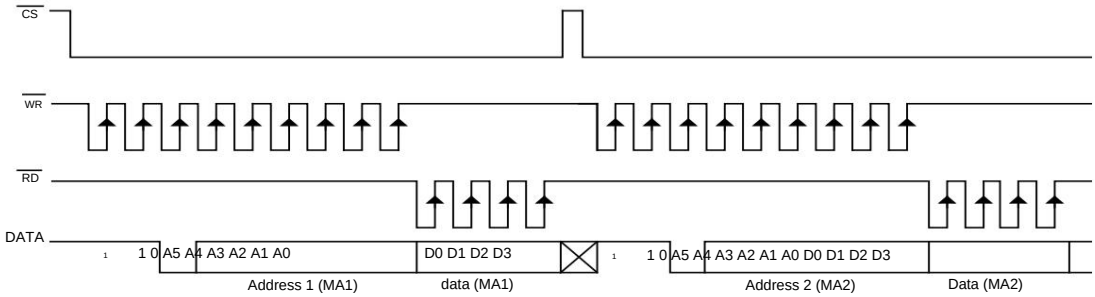
4.7. Interface

GN1621 only needs 4 wires to interface. CS initializes the serial interface circuit and terminates the communication between the host controller and GN1621. When CS is 1, the data and commands between the main controller and GN1621 are prohibited and initialized. Before command modes and mode transitions occur, the A high pulse initializes the serial interface of the GN1621. The data lines are serial input/output lines. Read and write data or write commands must through the data line. The RD line is the READ clock input. The data in the RAM is read out at the falling edge of the RD signal, and the read data will be displayed on the DATA online. The master controller reads the correct data between the rising edge and the next falling edge of the READ signal. The WR line is the WRITE clock input.

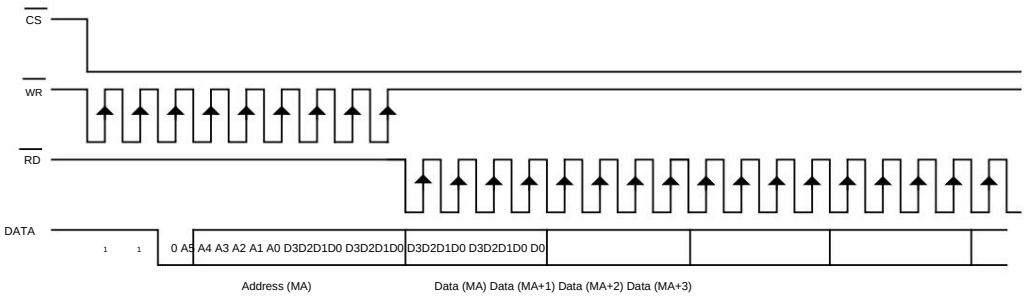
The data, address and command on the data line are in the WR The rising edge of the signal is all read to GN1621. IRQ line is used as master controller and GN1621 Of
interface between. IRQpin as timer output or WDT overflow flag output, set by S/W. The main controller connects the IRQ of GN1621
pin performs a time reference or WDT function.

4.8. Sequence Diagram

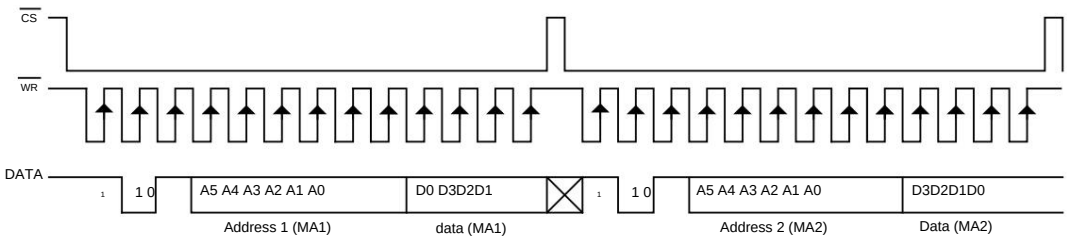
4.8.1, READ mode (command code: 110)



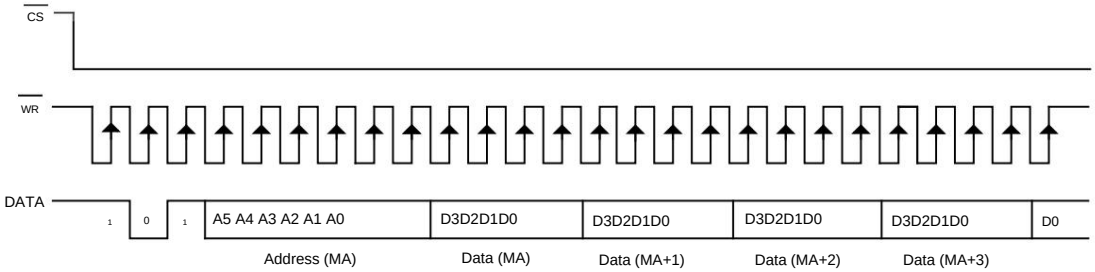
4.8.2, READ mode (sequential address reading)



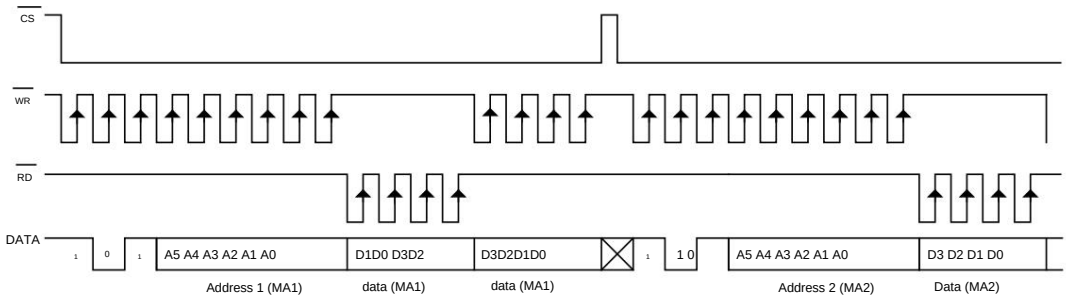
4.8.3, WRITE mode (command code: 101)



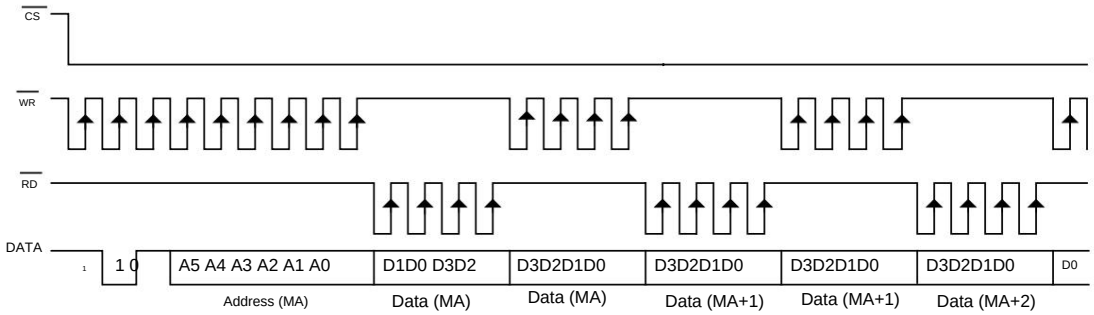
4.8.4, WRITE mode (sequential address write)



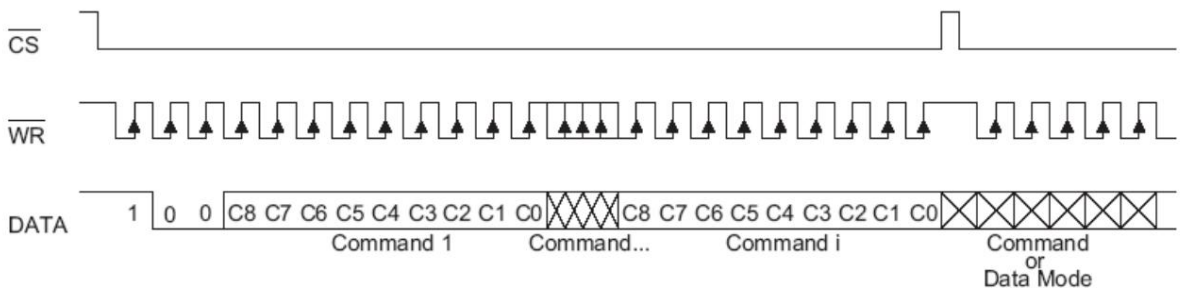
4.8.5, READ-MODIFY-WRITE mode (command code: 101)



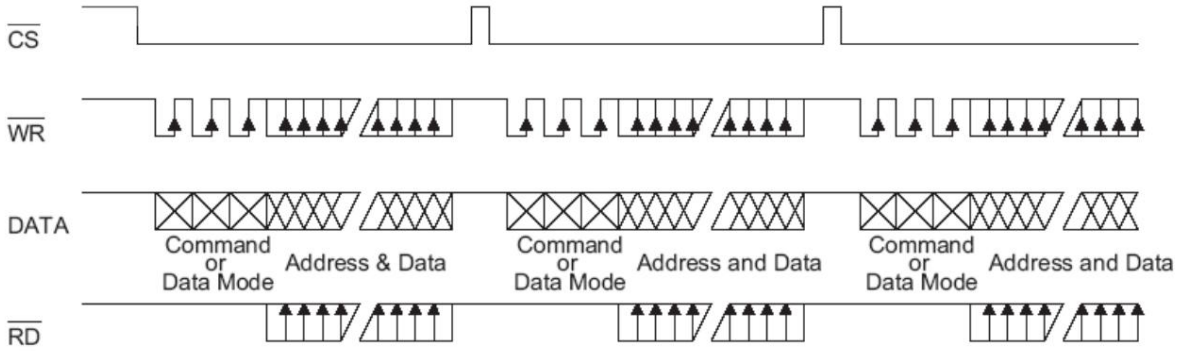
4.8.6, READ-MODIFY-WRITE mode (sequential address access)



4.8.7, command mode (command code : **100)**



4.8.8, mode (data and command mode)



Note: It is recommended that the master controller should be on the RD Rising edge with the next cycle RD Read data from the DATA terminal between falling edges.

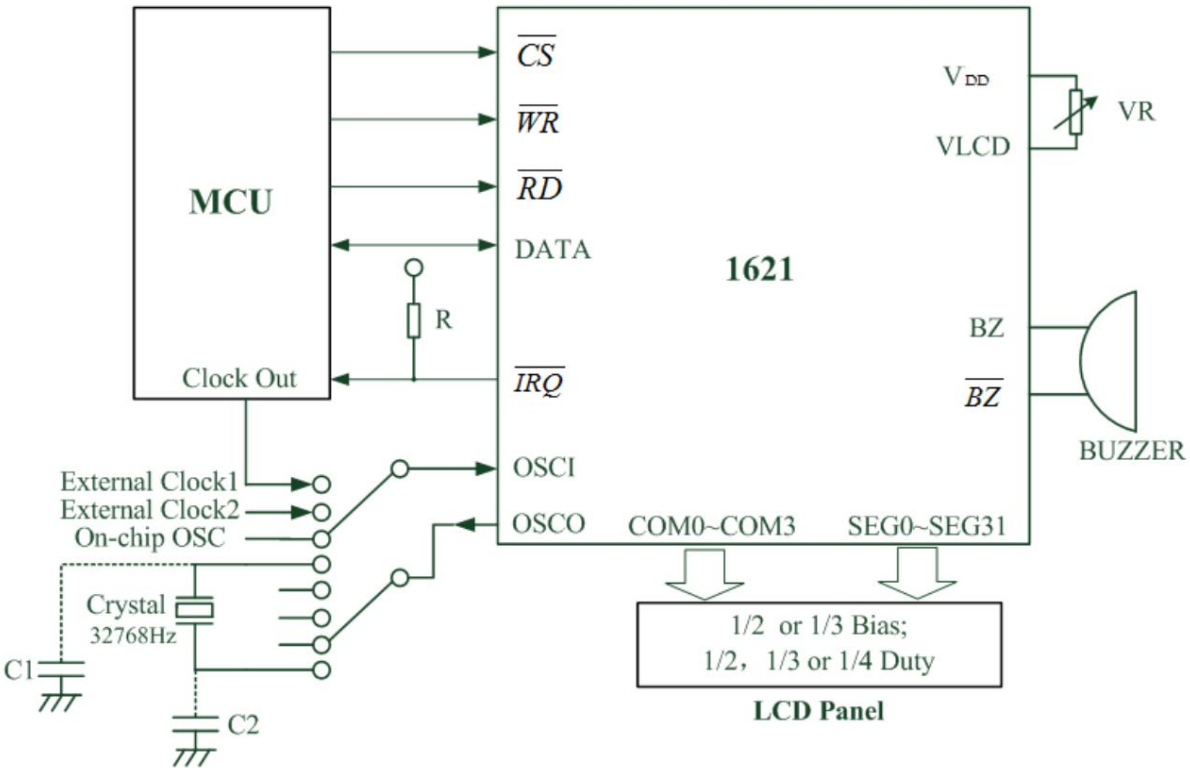
4.9. Command list

name	ID	command code	D/C	Function	Turn on preset reset
READ	110 A5	A4A3A2A1A0D0D1D2D3 D		Read data in RAM	-
WRITE	101 A5	A4A3A2A1A0D0D1D2D3D		Write data to RAM	-
READ MODIFY -WRITE	101 A5	A4A3A2A1A0D0D1D2D3 D		Read and write RAM	-
SYS DIS	100	0000_0000_X	C	Turn off the system oscillator and LCD at the same time The bias generator	Yes
SYS EN 100		0000_0001_X	C	turns on the system oscillator	-
LCD OFF 100		0000_0010_X	C	Turn off the LCD bias generator	Yes
LCD ON 100		0000_0011_X	C	Turn on the LCD bias generator and disable	-
TIMER DIS 100		0000_0100_X	C	the time reference output	-
WDT DIS	100	0000_0101_X	C	Disable WDT pause flag output and enable	-
TIME ONE 100		0000_0110_X	C	time reference output	-
WDT EN 100		0000_0111_X	C	Allow WDT pause flag output to turn off	-
TONE OFF 100		0000_1000_X	C	buzzer output to	Yes
TONE ON 100		0000_1001_X	C	turn on buzzer output	-
CLR TIMER	100	0000_10XX_X	C	Clears the contents of the time base generator	-
CLR WDT 100		0000_111X_X	C	Clear WDT content	-
XTAL 32K 100		0001_01XX_X	C	system clock is crystal oscillator	-
RC 256K 100		0001_10XX_X	C	system clock is on-chip RC oscillator	Yes
EXT 256K 100		0001_11XX_X	C	System clock is external clock LCD 1/2 —	
BIAS 1/2	100	0010_abX0_X	C	LCD 1/2 Bias Status ab=00: 2COM port ab=01: 3COM port ab=10: 4COM port	-
BIAS 1/3	100	0010_abX1_X	C	LCD 1/3 Bias Status ab=00: 2COM port ab=01: 3COM port ab=10: 4COM port	-
TONE 4K 100		010X_XXXX_X	C	Beep frequency: 4KHz	-

TONE 2K 100		011X _XXXX_X	C	Buzzer frequency: 2KHz	-
IRQ— DIS	100	100X _0XXX_X	C	Disable *IRQ* output	Yes
IRQ— IN		100X _1XXX_X	C	Enable *IRQ* output	-
F1	100	101X -X000_X	C	Time base/WDT clock output: 1Hz WDT Pause Flag Delay: 4s Time	-
F2	100	101X _X001_X	C	Base/WDT Clock Output: 2Hz WDT Pause Flag Delay: 2s Time	-
F4	100	101X _X010_X	C	Base/WDT Clock Output: 4Hz WDT Pause Flag Delay: 1s Time	-
F8	100	101X _X011_X	C	Base/WDT Clock Output: 8Hz WDT Pause Flag Delay: 1/2s Time	-
F16	100	101X _X100_X	C	Base/WDT Clock Output: 16Hz WDT Pause Flag Delay: 1/4s Time	-
F32	100	101X _X101_X	C	Base/WDT Clock Output: 32Hz WDT Pause Flag Delay: 1/8s Time	-
F64	100	101X _X110_X	C	Base/WDT Clock Output: 64Hz WDT Pause Flag Delay: 1/16s Time	-
Q128	100	101X _X111_X	C	Base/WDT Clock Output: 128Hz WDT pause flag delay: 1/32s test	Yes
TOP	100	1110 0000 X	C	mode	-
TNORMAL 100		1110 _0011_X	C	standard mode	Yes

5. Typical application circuit

5.1. Application circuit



5.2. Instructions for use:

host of the The connection of the pins depends on the requirements

controller. and RD ÿ IRQ ÿ The voltage of the VLCD pin

must be lower than VDD. ÿ Adjust VR to suit LCD display voltage. VDD=5V, VLCD=4V, VR=27.5kÿ±20%. ÿ Adjust R (external

pull-up resistor) to adapt to the user's reference clock. **ÿIn** order to obtain the best

performance, two additional load capacitors C1 and C2 need to be added, and the capacitance value affects the accuracy of the crystal oscillator

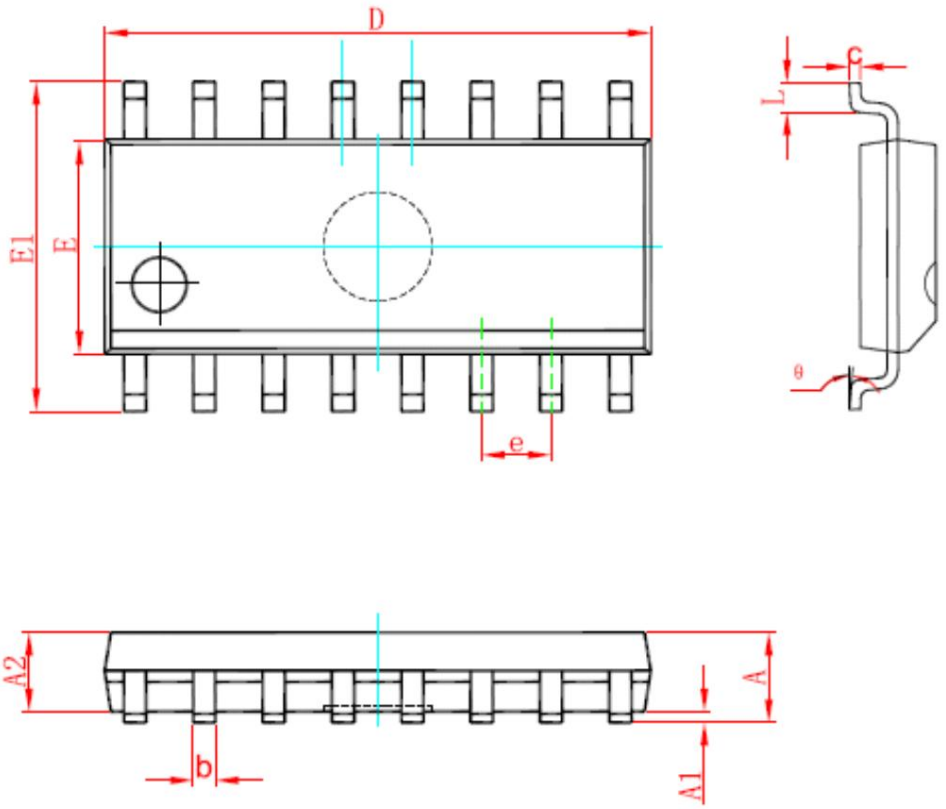
It is recommended to select the value according to the table.

C1, C2 capacitor value description:

Oscillation accuracy	Capacitance
±10ppm	0~10p
10~20ppm	10~20p

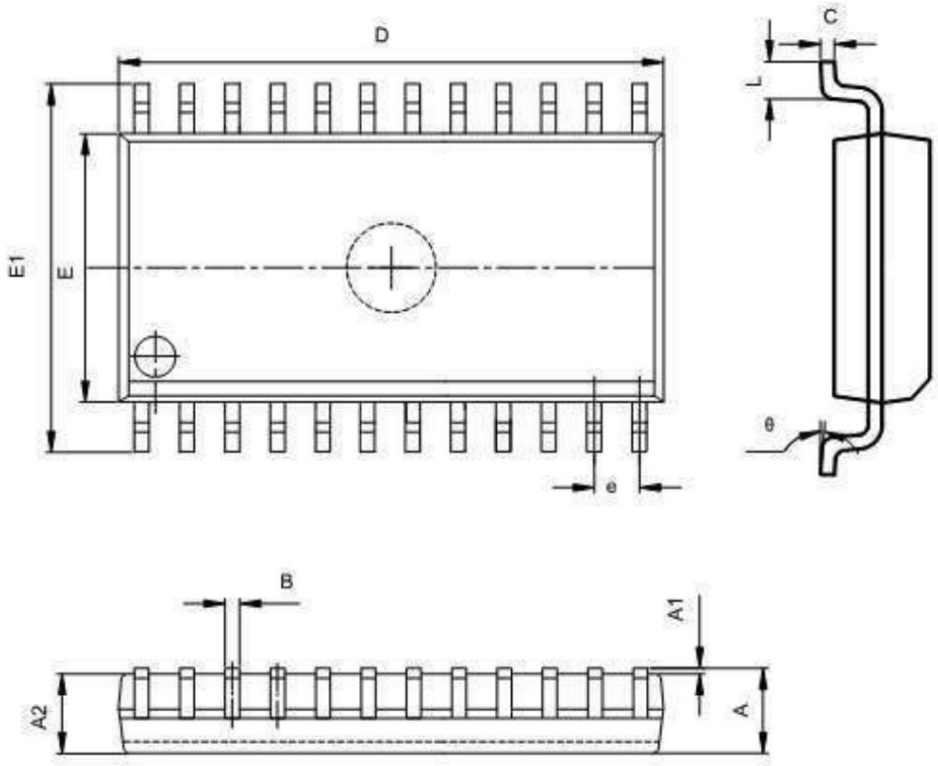
6. Package size and outline drawing

6.1, SOP16 outline drawing and package size



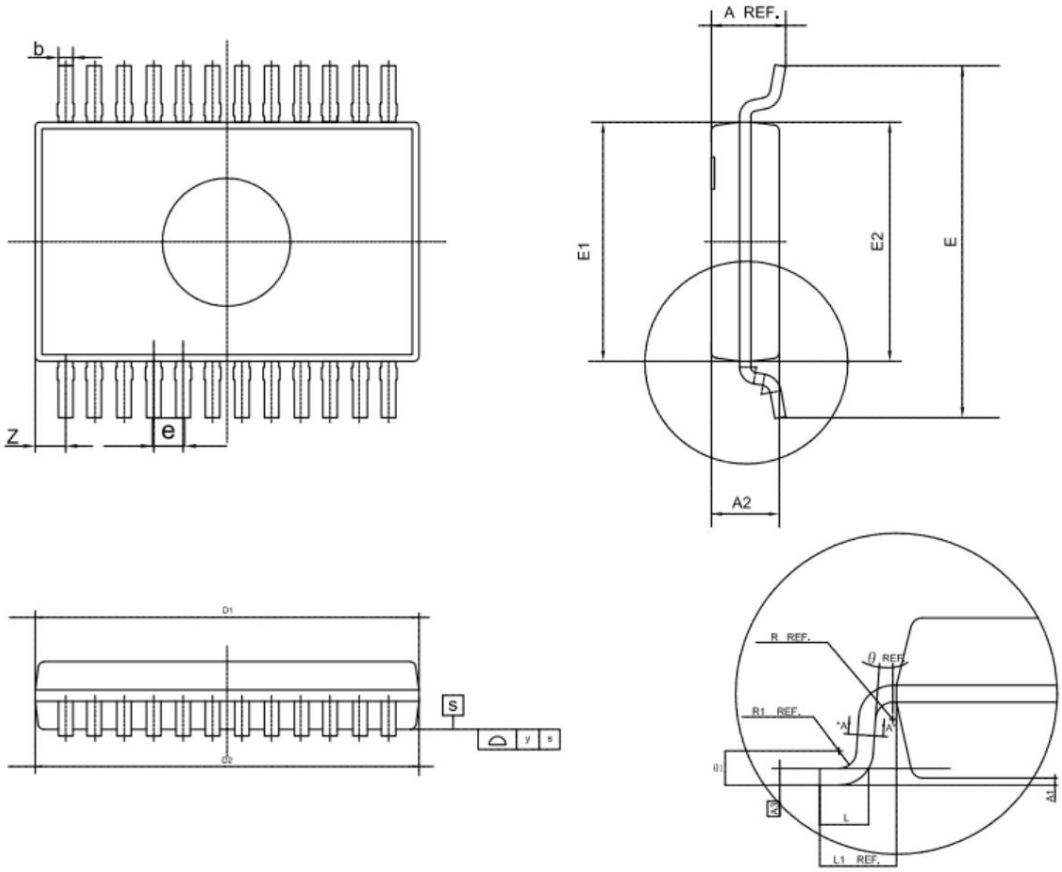
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

6.2, SOP24 outline drawing and package size

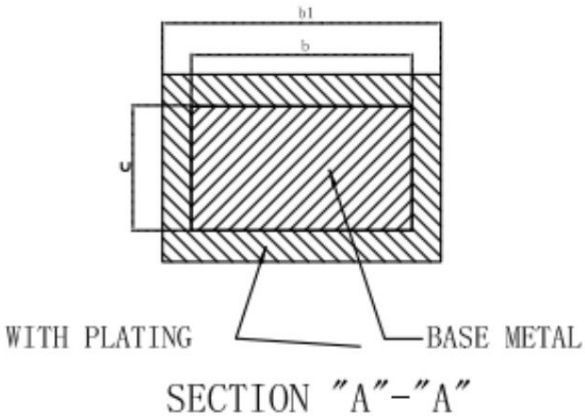


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.280	2.630	0.090	0.104
A1	0.100	0.300	0.004	0.012
A2	2.180	2.330	0.086	0.092
B	0.350	0.510	0.014	0.020
C	0.204	0.360	0.008	0.014
D	15.200	15.600	0.598	0.614
E	7.400	7.600	0.291	0.299
E1	10.000	10.650	0.394	0.419
e	1.270(TYP)		0.050(TYP)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

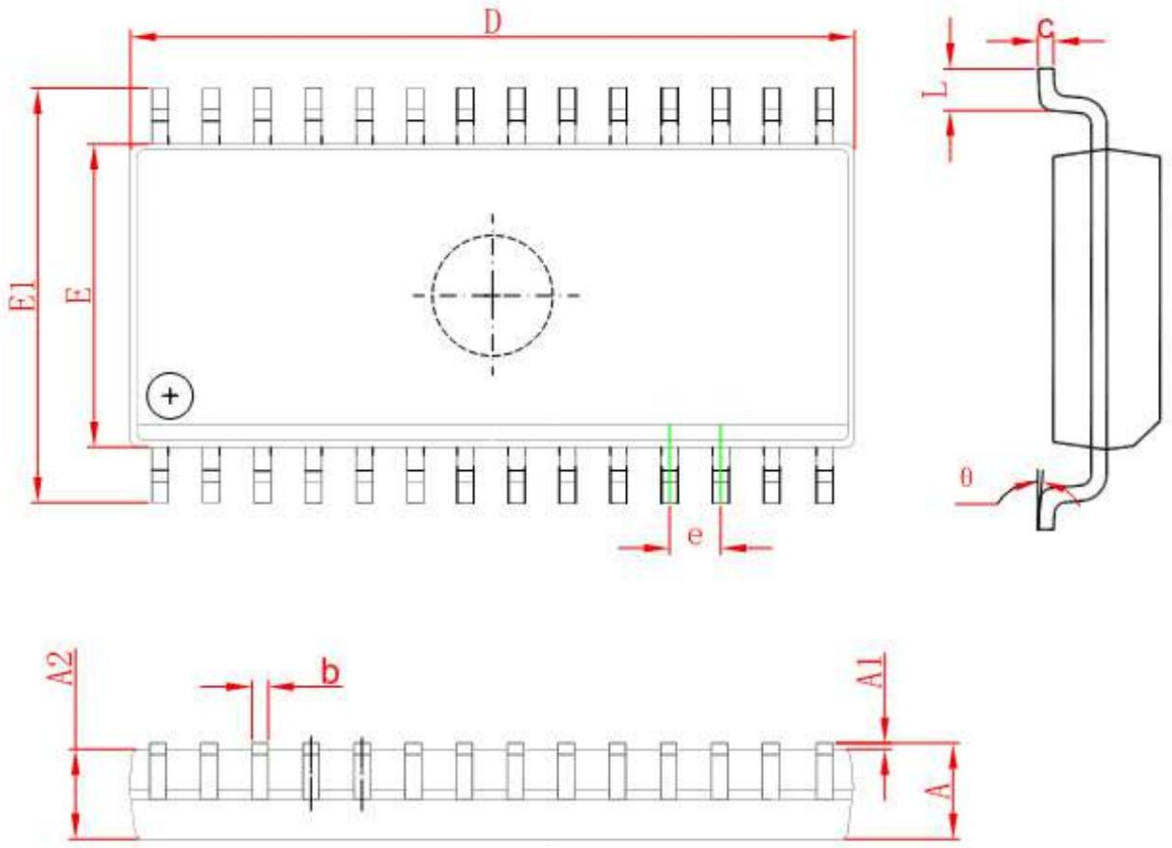
6.3, SSOP24 outline drawing and package size



Symbol	Min	Nom	Max
A	1.500	1.600	1.700
A1	0.100	0.150	0.200
A2	1.400	1.450	1.500
A3	--------	0.203	------
b	———	0.254	——
b1	0.260	0.320	0.380
c	------	0.203	-----
D1	8.600	8.650	8.700
D2	8.610	8.660	8.710
E	5.800	6.000	6.100
E1	3.800	3.900	4.000
E2	3.850	3.950	4.050
e	------	0.635	------
L	0.560	0.660	0.760
L1	0.950	1.050	1.150
R	-------	0.120	-----
R1	-------	0.200	-----
θ	0	-------	------
θ1	0	-------	8°
y	------	-------	0.1
Z	-------	0.838	-----

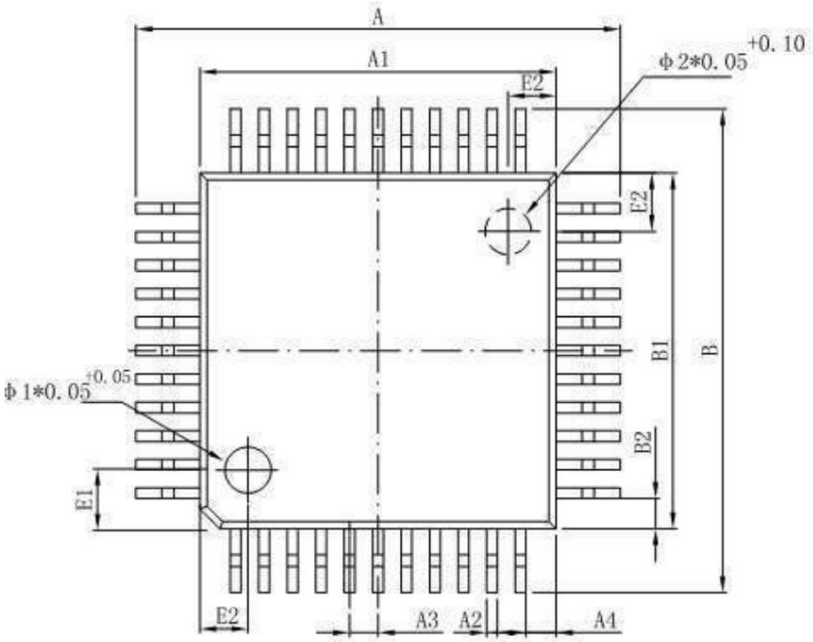


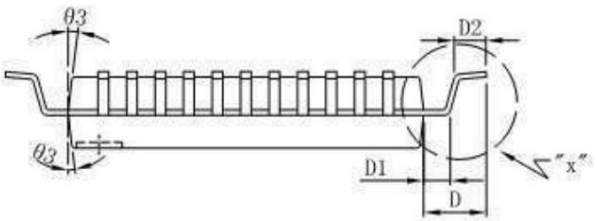
6.4, SOP28 outline drawing and package size

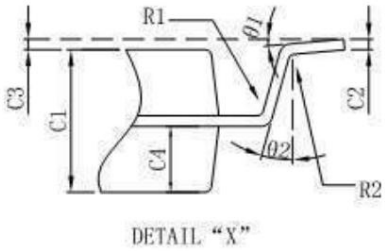


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.290	2.500	0.09	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	17.700	18.100	0.697	0.713
E	7.400	7.700	0.291	0.303
E1	10.210	10.610	0.402	0.418
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

6.5, QFP44 outline drawing and package size



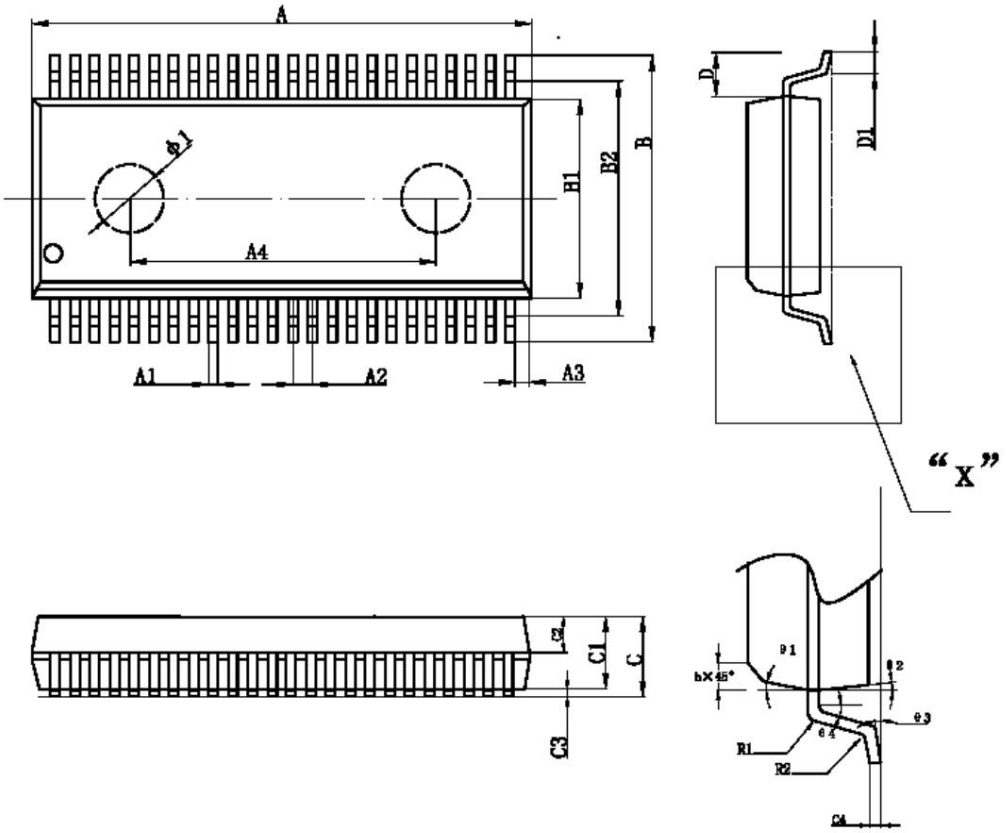




DETAIL "X"

尺寸 / 标注	最小（mm）	最大（mm）	尺寸 / 标注	最小（mm）	最大（mm）
A	13.20	14.00	D	1.8TYP	
A（短脚）	12.90	13.50	D（短脚）	1.6TYP	
A1	9.90	10.10	D1	0.80TYP	
A2	0.30	0.375	D2	0.60	1.00
A3	0.67	0.93	E1	1.34	1.42
A4	0.85TYP		E2	1.37	1.45
B	13.20	14.00	R1	0.13MIN	
B（短脚）	12.90	13.50	R2	0.13	0.3
B1	9.90	10.10	φ1	1.5TYP	
B2	0.85TYP		φ2	1.5TYP	
C1	1.90	2.10	θ1	4° TYP	
C2	0.11	0.23	θ2	20° TYP	
C3	0.05	0.20	θ3	8° TYP	
C4	0.904	0.944			

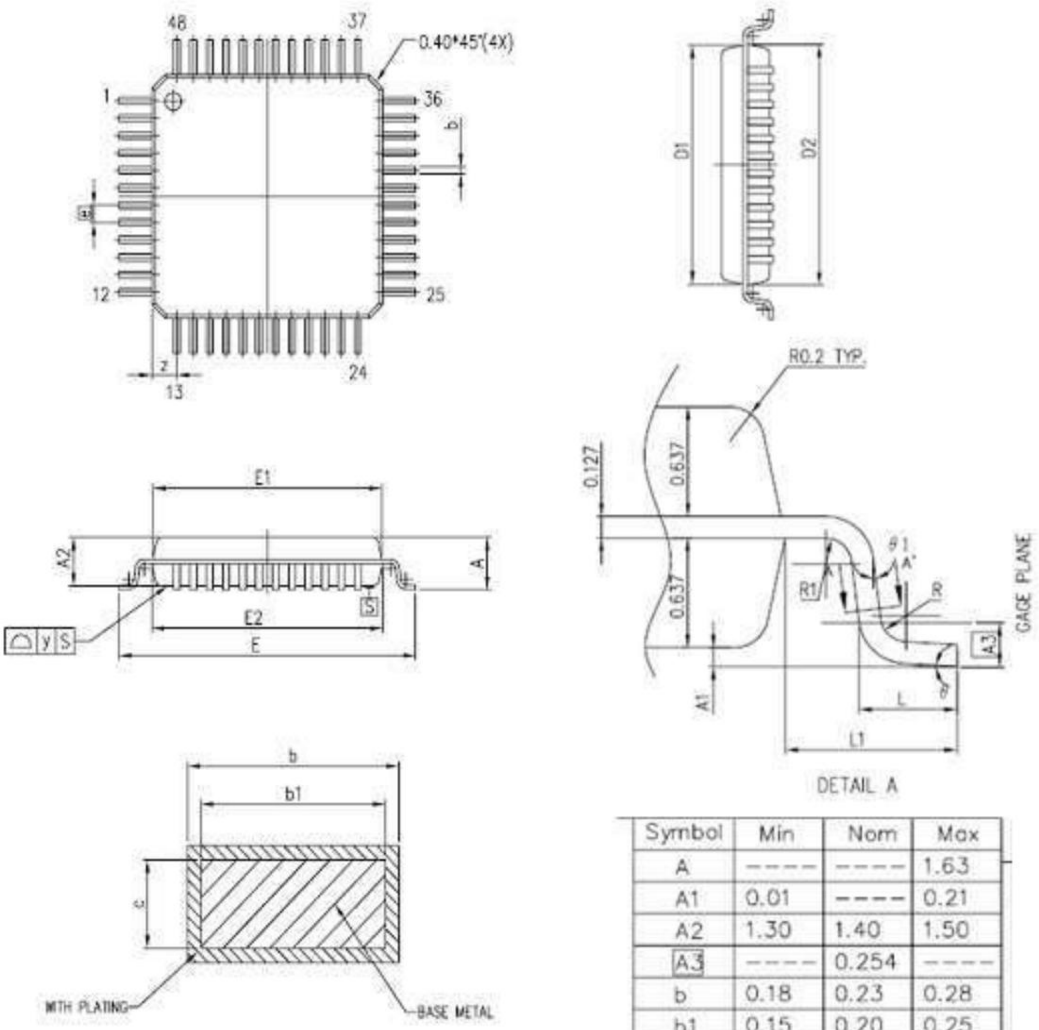
6.6, SSOP48 outline drawing and package size



DETAIL "X"

尺寸 / 标注	最 小（mm）	最 大（mm）	尺寸 / 标注	最 小（mm）	最 大（mm）
A	15.77	15.97	C3	0.2	0.4
A1	0.20	0.35	C4	0.12	0.25
A2	0.635TYP		D	1.41TYP	
A3	0.5TYP		D1	0.61	0.91
A4	10.2TYP		h	0.381	0.635
B	10.01	10.61	φ1	2.2TYP	
B1	7.39	7.59	θ1	15° TYP	
B2	8.6TYP		θ2	15° TYP	
C	2.41	2.78	θ3	4° TYP	
C1	2.18	2.38	θ4	8° TYP	
C2	1.067TYP				

6.7, LQFP48 outline drawing and package size



Symbol	Min	Nom	Max
A	----	----	1.63
A1	0.01	----	0.21
A2	1.30	1.40	1.50
A3	----	0.254	----
b	0.18	0.23	0.28
b1	0.15	0.20	0.25
c	----	0.127	----
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10
e	----	0.50	----
L	0.43	----	0.71
L1	0.90	1.00	1.10
R	0.1	----	0.25
R1	0.1	----	----
θ	0	----	10°
θ1	0	----	----
y	----	----	0.1
Z	----	0.75	----

7. Declaration and precautions:

7.1. Name and content of toxic and harmful substances or elements in the product

part name	Toxic and hazardous substances or elements									
	lead ÿPbÿ	HG ÿHgÿ	cadmium ÿCdÿ	Chromium VI ÿCr (WE))	PBBs benzene ÿPBBs ÿ	PBBs ether ÿPBDEs ÿ	Phthalate Formic acid two Butyl ester ÿDBP)	Phthalate Butyl formate Benzyl ester ÿBBP)	Phthalo Acid two (2-Ethyl base) ester ÿDEHP)	Phthalo diisobutylate Ester (DIBP)
Lead frame • Plastic	•	•	•	•	•	•	•	•	•	•
package resin	•	•	•	•	•	•	•	•	•	•
Chip •		•	•	•	•	•	•	•	•	•
Inner lead • Mounting		•	•	•	•	•	•	•	•	•
adhesive •		•	•	•	•	•	•	•	•	•
illustrate	•: Indicates that the content of the toxic and hazardous substance or element is below the detection limit of the SJ/T11363-2006 standard. ×: Indicates that the content of the toxic and hazardous substance or element exceeds the limit requirement of the SJ/T11363-2006 standard.									