DGP01467AAA

GSS6450 Data Format
(Patent Applied for 1111305.7)

ABSTRACT

This DCS document defines the data format for the GSS6450. It covers the low level format, the file structures and header information.

N.B. Only documents bearing the Document Status 'APPROVED SPIRENT DOCUMENTATION' in the panel below are deemed official literature.

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RECORD OF ISSUE

Issue	Date	Author	Reason for Change
1-00	17 Nov. 16	MA	First Issue
1-10	23 Nov 16	PA	Section 4.3: Update for GSS6450 10.23MHz sample Frequency and BW table
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3-00	16 Mar. 18	PA	Section 3: Addition of RF Inputs specification Section 4.2: Additional Filenames added Section 4.3: Sample Frequencies x6 and x8 added and signals for RF2 and RF3 added to table Section 5.1: Example scenario file updated for header GSS6450V3

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1.1 SCOPE & APPLICABILITY

This document defines the data format for the GSS6450. It covers the low level format, the file structures and header information.

1.2 REFERENCED DOCUMENTS

a) DGP01444AAA GSS6450 RPS Manual [latest issue]

1.3 GLOSSARY OF TERMS

2 INTRODUCTION

This document defines the data format for the GSS6450. It covers the low level format, the file structures and header information.

3 TOP LEVEL SPECIFICATION FOR GSS6450 FORMAT

No of channels:	1 to 4
Bits per channel	2 to 16 (I &Q)
Number of files	Normally one data file per FPGA, with up to 2 channels per file. GSS6425 compatibility mode supports 3 channels on FPGA in one File
Header info	Included in .scn file and at start of data files Include channel format (no of bits, decoding)
Synchronous data	Up to 2 bits per channel, required on all channels
RF inputs	Up to 3 RF inputs, listed as _RF1, _RF2 or _RF3 in the signal names

4 GSS6450 FILES AND SAMPLE FREQUENCIES

4.1 NUMBER OF FILES

The GSS6450 has an architecture with two FPGA's with separate interfaces to the processor system, this means that:

- There will be a separate data file per FPGA, resulting in either two data files for GSS6450 mode or one data file for GSS6425 mode
- Data files from FPGA A will have the suffix .A.gns, and from FPGA B will have the suffix .B.gns
- The channels recorded on one FPGA must have the same number of Bits and Bandwidth.
- Each FPGA (and file) will normally contain one or two channels
- In the GSS6425 compatibility mode, FPGA A will support three channels, and there will be three channels in the data file. There will be no channels configured for FPGA B. In this mode the data file name will be .gns. See the GSS6425 data format document for more information on the compatibility mode data format

4.2 FILENAMES

Each GSS6450 Recording will have a scenario file (See section 6 for content), and the data files with a .gns suffix. There will be a timestamped file name, with an ".A" or ".B" for the two FPGA.s, followed by the .gns suffix, e.g. 150910092552.A.gns and 150910092552.B.gns

The GSS6450 Recordings can also have the following files depending on the configuration:

- AGC File logging AGC and LNA settings during recording 150910092552.agc
- Asynchronous Serial data Logged from Serial Port during recording 150910092552.com1
- NMEA file generated from internal GNSS Receiver during recording 150910092552.nmea
- NMEA file generated from internal GNSS Receiver during playback 150910092552.nmea.play
- Video Recordings from webcams
    - Webcam 1 150910092552.mpg
    - Webcam 2 150910092552a.mpg
    - Webcam 3 150910092552b.mpg
    - Webcam 4 150910092552c.mpg

4.3 SAMPLE FREQUENCIES

The sampling frequencies available are multiples of 10.23MHz, i.e.

- x1 = 10.23MHz (**Note** for GSS6450 mode is 10.23x136/135 MHz, for GSS6425 compatibility mode 10.23MHz)
- x3 = 30.69MHz
- x5 = 51.15MHz
- x6 = 61.38MHz
- x8 = 81.84MHz

and support 2, 4, 8, 16 bits I and Q (see 4.1)

The centre frequencies for each signal down converted to DC are given in the following table

Index	Signal	BW	Centre Frequency Down-Converted to DC (MHz)	RF
1	L1: GPS/GAL E1	10,30,50	1575.42	RF1
2	L1: GLONASS	10,30	1602.018	RF1
3	L1: GPS/GLO	50	,1591.788	RF1
4	L1: GPS/GLO/BEI/GAL	50,80	1583.604	RF1
5	B1: BEIDOU	10,30	1561.098	RF1
6	L1: GPS/BEI B1	30	1567.236	RF1
7	L2: GPS	30	1227.6	RF1
8	L2: GLONASS	30	1246.014	RF1
9	L2: GPS/GLO	50	1239.876	RF1
10	L5: GPS/GAL E5A	30	1176.45	RF1
11	L5: IRNSS	50	1176.45	RF1
12	B2: BEI B2b/GAL E5b	30	1207.14	RF1
13	E5: BEI B2/GAL E5ab/ GPS L5/GLO G3	50,60	1191.795	RF1
14	E5: BEI B2/GAL E5ab/ GPS L5/GLO G3 L2/GPS	80	1199.979	RF1
15	B3: BEIDOU	30,50	1268.52	RF1
16	E6: GAL/BEI B3	50	1278.75	RF1
17	L6: QZSS	30	1278.75	RF1
18	WIFI 2.4GHz	80	2440.878	RF3

19	WIFI 5GHz Ch 36-48	80	5210.139	RF3
20	WIFI 5GHz Ch 149-161	80	5774.835	RF3
21	LTE Band 12	10,30,50,60	734.514	RF2
22	LTE Band 4	10,30,50	2132.955	RF2
23	LTE Band 17	10,30	740.652	RF2
24	LTE Band 30	10	2354.946	RF2
26	Inmarsat SBAS	30,50	1536.546	RF1
28	IRNSS S BAND	30,50	2491.005	RF3
User Defined Signals				
25	RF2 User Defined	10,30,50,60,80	N x 1.203 Overall Recordable Frequency Range for RF2 is 690-2400MHz	RF2
27	RF3 User Defined	10,30,50,60,80	N x 1.023 Overall Recordable Frequency Range for RF3 is 100-6000MHz	RF3

Table 1 Centre frequencies for each signal down converted to DC

4.4 BANDWIDTH OPTIONS BETWEEN FPGA'S

The bandwidths of the Channels recorded on the separate FPGAs must be the same, or binary multiples of each other, the permitted options are shown in the following table.

		FPGA A Bandwidth (MHz)		
		10.23	**30.69**	**51.15**
FPGA B Bandwidth (MHz)	**10.23**	Y	N	N
	20.46	Y	N	N
	30.69	N	Y	N
	40.92	Y	N	N
	51.15	N	N	Y
	61.38	N	Y	N
	81.84	Y	N	N

Table 2 Permitted bandwidth options

5 HEADER INFORMATION

5.1 EXAMPLE GSS6450 SCENARIO FILE (*.SCN)

The GSS6450 is an extension of the GSS6425 scenario file, include a header line and bit resolution.

```
<Header> GSS6450V3
<Filename> 171107144950
<Signal Recorded>  1, GPSL1_RF1, Bandwidth 30 MHz, Freq 1575.420 MHz, Bits 8, Sync a, Sync b
<Signal Recorded>  2, GPSL2_RF1, Bandwidth 30 MHz, Freq 1227.600 MHz, Bits 8, Sync a, Sync b
<Signal Recorded>  3, GLONASSL1_RF1, Bandwidth 30 MHz, Freq 1602.018 MHz, Bits 8, Sync a, Sync b
<Signal Recorded>  4, GLONASSL2_RF1, Bandwidth 30 MHz, Freq 1246.014 MHz, Bits 8, Sync a, Sync b
<Description> Unknown
<Location> Unknown
<External Trigger> False
<Master/Slave> OFF
<Input Gain> RF1 Auto. RF2 Auto. RF3 Auto.
<Start Time> 14:49:50 07/11/17 GMT
<Local Start Time> 14:49:50 07/11/17
<Stop Time>
14:54:59 07/11/17 Local time
```

5.2 EXAMPLE GSS6425 COMPATIBILITY MODE SCENARIO FILE (*.SCN)

```
<Header> GSS6425
<Filename> 130422142345.gns
<Signal Recorded> 1, GPS:L1--GAL:E1, Bandwidth 30 MHz, Freq 1575.420 MHz, Sync a
<Signal Recorded> 2, GPS:L2, Bandwidth 30 MHz, Freq 1227.600 MHz
<Signal Recorded> 3, GLONASS:L1, Bandwidth 30 MHz, Freq 1602.018 MHz
<Description> Unknown
<Location> Unknown
<Start Time>
14:23:45 22/04/13 GMT
15:23:45 22/04/13 Local time
<Stop Time>
14:24:45 22/04/13 GMT
15:24:45 22/04/13 Local time
```

6 FORMAT OF GSS6450 DATA FILE (*.GNS)

6.1 GSS6450 STARTUP SYNCHRONISATION PATTERN

The GSS6450 data file (*.gns) is a binary file. The start of the file contains a copy of the .scn file (excluding the <Stop Time> field), terminated by <End of Header> and then word aligned to the next 4 byte boundary by the addition of dummy data (usually spaces). There can then be a further 4 bytes of dummy data before the synchronization pattern commences. The first few synchronization patterns have the top byte replaced by a counter (e.g. “04111111”) followed by the repeated synchronization pattern of up to 64Kbytes, followed by the start of the recording. Both the synchronization pattern and the recorded data are in 32bit words. Note that the end of the synchronization pattern indicates the start of a 32bit frame for 2, 4, 8, 16 bit recordings. The 32bit synchronization patterns are as follows.

FPGA A
Signal 1: "11111111"
Signal 2: "22222222"
Signal 3: "33333333" (Only in GSS6425 compatibility mode)
FPGA B
Signal 1: "11111111"
Signal 2: "22222222"

The alignment point between the two FPGA files is offset from the start of the full synchronisation pattern as described below.

First full synchronisation pattern with “11111111” is at address “Address A” in word32

Number of Channels Recorded on FPGA	Alignment Point in file (Word32 address)
1	“Address A” -4
2	“Address A” -8
3	“Address A” -12

Table 3 Table 6-1 Synchronisation pattern

6.2 CHANNELS AND BITS TO BE RECORDED

Each channel has the option to support 2, 4, 8 or 16 bits of data:

ADC Bits	I+Q bits per sample	Samples per word32
2	4	8
4	8	4
8	16	2
16	32	1

Table 4 Channel Bit Options

6.3 DATA ENCODING

GSS6425 compatibility mode files uses two bit I and two bit Q data as per the table below.

10 = -3
11 = -1
00 = +1
01 = +3

GSS6450 mode files will use 2's complement, and use that format directly in the file format.

ADC Bits	Sample Encoding
2	2 's complement (2 bits I, 2bits Q)
4	2 's complement (4 bits I 4bits Q)
8	2 's complement (8 bits I, 8bits Q)
16	2 's complement (16 bits I, 16bits Q)

Table 5 Two bit I and two bit Q compatibility data

6.4 LOW LEVEL DISK FORMAT

32 bit words, big endian

BYTE ORDER ON DISK (Big Endian)			
1	**2**	**3**	**4**
32 bit word			
31			**0**

Table 6 Byte order on disk (Big Endian)

NOTE when reading data from the disk the byte order is reversed e.g. when reading a 4 byte word swap bytes 1 & 4 and 2 & 3

6.5 LOW LEVEL DATA FRAMES

The GSS6450 uses a 32 bit frame for the 2, 4, 8 and 16 bit recordings.

6.6 SYNCHRONISED DATA

For the GSS6450 synchronised data will be available as:

Standard Up to 2 bits of sync data per channel
Replace bit 0 of I and Q in every 32 bit word

6.7 WORD FORMATS WITHOUT AND WITH SYNCHRONOUS DATA

2 Bit Data, No Synchronous Data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[1:0]		Q_{t0}[1:0]		I_{t1}[1:0]		Q_{t1}[1:0]		I_{t2}[1:0]		Q_{t2}[1:0]		I_{t3}[1:0]		Q_{t3}[1:0]	
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	I_{t4}[1:0]		Q_{t4}[1:0]		I_{t5}[1:0]		Q_{t5}[1:0]		I_{t6}[1:0]		Q_{t6}[1:0]		I_{t7}[1:0]		Q_{t7}[1:0]	

2 Bit Data, With Synchronous Data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[1:0]		Q_{t0}[1:0]		I_{t1}[1:0]		Q_{t1}[1:0]		I_{t2}[1:0]		Q_{t2}[1:0]		I_{t3}[1:0]		Q_{t3}[1:0]	
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	I_{t4}[1:0]		Q_{t4}[1:0]		I_{t5}[1:0]		Q_{t5}[1:0]		I_{t6}[1:0]		Q_{t6}[1:0]		I_{t7}[1]	S1b	Q_{t7}[1]	S1a

4 Bit Data, No Synchronous Data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[3:0]				Q_{t0}[3:0]				I_{t1}[3:0]				Q_{t1}[3:0]			
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	I_{t2}[3:0]				Q_{t2}[3:0]				I_{t3}[3:0]				Q_{t3}[3:0]			

4 Bit Data, With Synchronous Data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[3:0]				Q_{t0}[3:0]				I_{t1}[3:0]				Q_{t1}[3:0]			
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	I_{t2}[3:0]				Q_{t2}[3:0]				I_{t3}[3:1]			S1b	Q_{t1}[3:1]			S1a

8 Bit Data, No Synchronous Data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[7:0]								Q_{t0}[7:0]							
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	I_{t1}[7:0]								Q_{t1}[7:0]							

8 Bit Data, With Synchronous Data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[7:0]								Q_{t0}[7:0]							
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	I_{t1}[7:1]							S1b	Q_{t1}[7:1]							S1a

16 Bit Data, No Synchronous data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[15:0]															
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	Q_{t0}[15:0]															

16 Bit Data, With Synchronous data

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	I_{t0}[15:1]															S1b
Bit (cont)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	Q_{t0}[15:1]															S1a

Table 7 Word formats without and with synchronous data

6.8 STORAGE OF 32 BIT WORDS INTO FILE

a. 1 channel data (2, 4, 8, 16 bits)

Bit	31 0
Word 0	Channel 0 Word 0
Word 1	Channel 0 Word 1
Word 2	Channel 0 Word 2
Word 3	Channel 0 Word 3
Word 4	Channel 0 Word 4

b. 2 channel data (2, 4, 8, 16 bits)

Bit	31 0
Word 0	Channel 0 Word 0
Word 1	Channel 1 Word 0
Word 2	Channel 0 Word 1
Word 3	Channel 1 Word 1
Word 4	Channel 0 Word 2
Word 5	Channel 1 Word 2
Word 6	Channel 0 Word 3
Word 7	Channel 1 Word 3

c. 3 channel data (2 bits FPGA_A only)

Bit	31 0
Word 0	Channel 0 Word 0
Word 1	Channel 1 Word 0
Word 2	Channel 2 Word 0
Word 3	Channel 0 Word 1
Word 4	Channel 1 Word 1
Word 5	Channel 2 Word 1
Word 6	Channel 0 Word 2
Word 7	Channel 1 Word 2
Word 8	Channel 2 Word 2

Table 8 Storage of 32 Bit words into file