	FE	DE	EX	ME	WB	
Instruction	or r4,r4,r3					Pipeline Model
FETCH	100	102	103	110	115	`// INITIAL STATE AT FETCH`
	101	102	103	110	115	`cpu.pl[FE] += fetch(0x00000868);`
	102	102	103	110	115	`if (cpu.pl[FE] < cpu.pl[DE])` `  cpu.pl[FE] = cpu.pl[DE];`
DECODE	102	102	103	110	115	`// INITIAL STATE AT DECODE`
	102	105	103	110	115	`cpu.pl[DE] = max3((cpu.pl[FE]+1),` `  opd1, opd2);`
	102	105	103	110	115	`if (cpu.pl[DE] < cpu.pl[EX])` `  cpu.pl[DE] = cpu.pl[EX];`
EXECUTE	102	105	103	110	115	`// INITIAL STATE AT EXECUTE`
	102	105	106	110	115	`cpu.pl[EX] = cpu.pl[DE] + 1;` `*dst1  = cpu.pl[EX];`
	102	105	110	110	115	`if (cpu.pl[EX] < cpu.pl[ME])` `  cpu.pl[EX] = cpu.pl[ME];`
MEMORY	102	105	110	110	115	`// INITIAL STATE AT MEMORY`
	102	105	110	111	115	`cpu.pl[ME] = cpu.pl[EX] + 0;` `*dst2  = cpu.pl[ME];`
	102	105	110	115	115	`if (cpu.pl[ME] < cpu.pl[WB])` `  cpu.pl[ME] = cpu.pl[WB];`
WRITEBACK	102	105	110	115	115	`// INITIAL STATE AT WRITEBACK`
	102	105	110	115	116	`cpu.pl[WB] = cpu.pl[ME] + 1;`
	102	105	110	115	116	`// FINAL PIPELINE STATE`
	Per Pipeline Stage Cycle Count					